Technical Program/Final Summaries

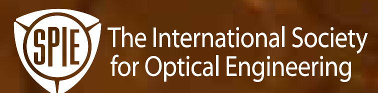
SPIE

Photomask Technology

18–22 September 2006

Monterey Marriott and Monterey Conference Center • Monterey, California USA

26th Annual BACUS Symposium



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SPIE

Photomask Technology

18-22 September 2006

Monterey Marriott and Monterey Conference Ctr. • Monterey, California USA

Welcome to BACUS Photomask 2006!

On behalf of SPIE, the Sponsor, and the organizing committee we would like to welcome you to the BACUS Photomask Technology Symposium. Now in its 26th year, BACUS is the world's premier photomask technology conference and is expected to attract over 1000 attendees from all over the globe

This year's conference will be opened by Martin van den Brink, Executive Vice President of Marketing and Technology from ASML. Mr. van den Brink's keynote talk, "Challenges and Opportunities to Keep Lithography Scaling on Track", will provide valuable insight into the changes and challenges that could alter the industry as we know it. He brings more than 20 years of research and engineering experience to the content of his talk. Don't miss it...

This year, the conference received over 200 presentation submissions and will continue with the presentation format as in past years that offers as many oral presentations as possible. In addition to the extended oral sessions, the poster session, held on Tuesday night, provides a unique opportunity for attendees to engage the authors in a more detailed discussion than would be possible during the oral presentations.

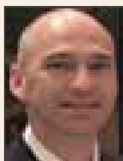
Tuesday and Wednesday the exhibition will be open. Please stop in and see what's new from the folks that are really the backbone of the photomask industry. Without their active participation and support it would be very difficult to manufacture a photomask.

Closing out the BACUS week (on Friday) is the increasingly popular, "one stop overview of the key issues facing the industry". This year's special session will follow previous year's format by addressing the hottest technical issues, development barriers, and potential roadblocks in the form of a critical review. We have an outstanding series of topics and speakers lined up for this session. If you are thinking of leaving early you will miss what is typically one of the highlights of the conference.

We challenge you to do three things while you are in Monterey... attend and participate in the technical sessions (challenge the authors, question assumptions and raise the technical sessions to the next level), visit the exhibition, and most of all... have fun!

Sincerely,

2006 Symposium Chairs



Patrick M. Martin,
Photronics, Inc.

Robert J. Naber,
Cadence Design Systems, Inc.

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Special Session: *"DFM: Are We There Yet? Remaining Challenges and Proposed Solutions"* **16**

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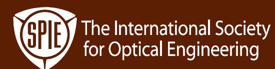

The international technical group of SPIE dedicated to the advancement of photomask technology.

Daily Schedule

Monday September 18	Tuesday September 19	Wednesday September 20	Thursday September 21	Friday September 22
Professional Development	**Conference**			
SC505 **Data to Silicon: Understanding the Fundamentals of MDP, Frame Generation, RET and DFM** *(Morse)* 8:30 am to 5:30 pm, $440 / $520, p.18	6349 **Photomask Technology** *(Martin, Naber)* p.9–p.16			**Special Session on DFM,** p.16
	Exhibition 10 am - 4 pm	**Exhibition** 10 am - 4 pm		
SC579 **Photomask Fabrication and Technology Basics** *(Duff)* 8:30 am to 5:30 pm, $440 / $520, p.18	**Exhibit/Poster Session** 6 - 7:30 pm			
SC707 **Basics of Optical Imaging in Microlithography: A Hands-on Approach** *(Milster, Brooker)* 1:30 to 5:30 pm, $270 / $310, p.19				
SC723 **The Limits of Optical Lithography** *(Pierrat)* 8:30 am to 12:30 pm, $270 / $310, p.19				
SC724 **Optical Lithography Extension: Design for Manufacturing and New Resolution Enhancement Techniques** *(Pierrat)* 1:30 to 5:30 pm, $270 / $310, p.20				
SC779 **Polarization for Lithographers** *(Kye, McIntyre)* 8:30 am to 12:30 pm, $270 / $310, p.20			**Banquet & Entertainment Program** 6 - 9:30 pm	

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Maps

Marriott Floorplan

Monterey Conference Center Floorplan

Level 3

Jeffers Plaza

Colton

III

II

I

Ferrante

Stevenson Terrace

Steinbeck Forum

I

II

III

Covered bridge to Marriott

Level 1

II

Serra Grand Ballroom

I

III

De Anza Ballroom

II

I

Lobby to Portola Plaza

SPIE Registration

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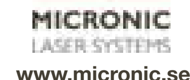

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General Refreshments

DNP Co. America, Inc. • Microlithography Inc. • Mitsui Chemicals America

Meet us at the Banquet!

Thursday 21 September, 6:00 to 9:30 pm
Serra Grand Ballroom

- **Reception • 6 to 7 pm**
  Entertainment by **The San Jose Taiko Drummers**
- **Banquet • 7 to 8:30 pm**
- **Entertainment Program • 8:30 to 9:30 pm**

Featuring
Comedian Henry Cho

Tickets may still be available - check with the SPIE cashier.

Floor plan as of 8 August 2006

Serra II
Serra
Serra I
Tricord Service Desk
Poster Area
119 218
117 216
115 214
116 114 112 108 106 104
219 217 316 215 314
319 418 317 315 414
421 419 417 415
Exit Only
Exit Only
COFFEE AND DESSERT AREA
109 208 107 206 105 204
310 209 308 207 205 304
311 410 309 408 406 305 404
407
Portola Lobby Registration Area
Lit 2
Lit 1
502 504 508 512
PHOTOMASK 2006
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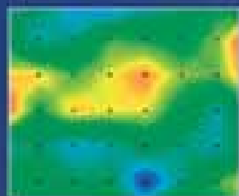
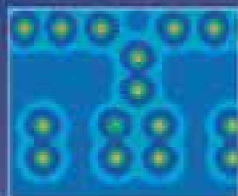
Carl Zeiss Mask Solution Provider


Global CDU Map - quality assessment of total mask area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26th Annual BACUS Symposium

Photomask Technology Exhibition

19-20 September 2006
Monterey Marriott and Monterey Conference Center
Monterey, California USA

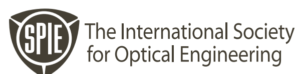
Make Time for the Photomask Industry's Top Exhibition

Exhibition Hours

Monterey Conference Center • Serra Ballroom

Tuesday .... 10 am to 4 pm; 6 to 7:30 pm
Wednesday .... 10 am to 4 pm

Find detailed exhibitor information in the Exhibition Guide available onsite or visit **spie.org/events/pmexhibit** for a full exhibitor listing.



Tuesday-Friday 19-22 September 2006 • Proceedings of SPIE Vol. 6349

Photomask Technology

Conference Chairs: **Patrick M. Martin**, Photronics, Inc.; **Robert J. Naber**, Cadence Design Systems, Inc.

Program Committee: **Ki-Ho Baik**, Intel Corp.; **Artur P. Balasinski**, Cypress Semiconductor Corp.; **Ron R. Bozak**, Rave LLC; **Ute Buttgereit**, SCHOTT Lithotec AG (Germany); **J. Fung Chen**, ASML MaskTools Inc.; **Frank A. Driessen**, Takumi Technology Corp. (Netherlands); **Roxann L. Engelstad**, Univ. of Wisconsin/Madison; **Benjamin G. Eynon, Jr.**, KLA-Tencor Corp.; **Donis G. Flagello**, ASML US, Inc.; **Emily E. Gallagher**, IBM Corp.; **Brian J. Grenon**, Grenon Consulting, Inc.; **Woo-Sung Han**, SAMSUNG Electronics Co., Ltd. (South Korea); **Naoya Hayashi**, Dai Nippon Printing Co., Ltd. (Japan); **Johnson C. Hung**, **John C. H. Lin**, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan); **Mark E. Mason**, Texas Instruments Inc.; **Wilhelm Maurer**, Infineon Technologies AG (Germany); **Richard D. Morse**, Morse Consulting; **Thomas H. Newman**, Micronic Laser Systems Inc.; **Wolfgang Staud**, Cadence Design Systems, Inc.; **J. Tracy Weed**, Synopsys, Inc.; **Craig A. West**, Toppan Photomasks, Inc.

Tuesday 19 September

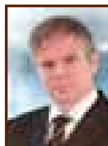
Introduction

Room: Steinbeck Forum .... Tues. 8:00 to 8:10 am

Chairs: **Patrick M. Martin,** Photronics, Inc.; **Robert J. Naber,** Cadence Design Systems, Inc.

SESSION 1: Invited Session

Chairs: **Patrick M. Martin**, Photronics, Inc.; **Robert J. Naber**, Cadence Design Systems, Inc.



Room: Steinbeck Forum .... Tues. 8:10 to 10:05 am

Keynote Presentation

8:10 am: **Challenges and opportunities to keep lithography scaling on track** *(Invited Paper, Presentation Only)*, M. A. van den Brink, ASML Netherlands B.V. (Netherlands) .... [6349-01]

8:50 am: **Mask Industry Assessment: 2006**, G. V. Shelden, Shelden Consulting; P. Marmillion, SEMATECH, Inc. .... [6349-02]

9:15 am: **PMJ Best Paper: Comparative study of bi-layer attenuating phase-shifting masks for hyper-NA lithography** *(Invited Paper)*, M. Yoshizawa, V. Philipsen, L. H. A. Leunissen, E. Hendrickx, R. M. Jonckheere, G. Vandenberghe, IMEC (Belgium); U. Buttgereit, H. W. Becker, SCHOTT Lithotec AG (Germany); C. Köpernik, M. Irmscher, Institut für Mikroelektronik Stuttgart (Germany) .... [6349-03]

9:40 am: **EMLC Best Paper: A correlation for predicting film pulling velocity in immersion lithography** *(Invited Paper)*, S. D. Schuetter, T. A. Shedd, K. Doxtator, G. F. Nellis, Univ. of Wisconsin/Madison; C. K. Van Peski, SEMATECH, Inc. .... [6349-04]

Coffee Break .... 10:05 to 10:35 am

Sessions 2-3-4 run concurrently with sessions 5-6-7.

SESSION 2: Resist Process

Chairs: **Ki-Ho Baik**, Intel Corp.; **Johnson C. Hung**, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan)

Room: Steinbeck Forum .... Tues. 10:35 am to 12:15 pm

10:35 am: **Chemical flare long-range proximity effects in photomask manufacturing with chemically amplified resists**, D. B. Sullivan, IBM Corp.; Y. Okawa, K. Sugawara, Toppan Electronics; Z. Benes, IBM Corp.; J. Kotani, Toppan Electronics .... [6349-05]

11:00 am: **PAB and PEB temperature gradient methodology for CAR optimization**, T. H. Dam, A. T. Jamieson, M. Lu, K. Baik, Intel Corp. . [6349-06]

11:25 am: **An ultra-uniform, ultra-thin resist deposition process**, B. J. Grenon, Grenon Consulting, Inc.; G. Picard, J. Schneider, Nanometrix (Canada) .... [6349-07]

11:50 am: **The challenges and requirements of photomask resist and coat track for 32-nm technology and beyond** *(Invited Paper)*, K. Baik, Intel Corp. .... [6349-202]

Lunch/Exhibition Break .... 12:15 to 1:30 pm

SESSION 3: Etch

Chairs: **Ki-Ho Baik**, Intel Corp.; **Patrick M. Martin**, Photronics, Inc.

Room: Steinbeck Forum .... Tues. 1:30 to 3:10 pm

1:30 pm: **A novel process of etching EUV masks for future generation technology**, B. Wu, A. Kumar, M. Chandrachood, I. M. Ibrahim, A. Sabharwal, Applied Materials PPC .... [6349-201]

1:55 pm: **Controlling CD uniformity for 45-nm technology node applications**, J. Plumhoff, S. Srinivasan, R. J. Westerman, D. J. Johnson, C. Constantine, Unaxis USA, Inc. .... [6349-10]

2:20 pm: **Mask CD correction method using dry-etch process**, H. Jung, T. Ha, J. Shin, K. Jeong, Y. Kim, O. Han, Hynix Semiconductor Inc. (South Korea) .... [6349-11]

2:45 pm: **The study of optical performance for quartz dry etching quality in ArF lithography**, W. Ahn, SAMSUNG Electronics Co., Ltd. (South Korea) .... [6349-12]

Coffee Break .... 3:10 to 3:40 pm

SESSION 4: DPI/DFM

Chairs: **J. Tracy Weed**, Synopsys, Inc.; **Robert J. Naber**, Cadence Design Systems, Inc.

Room: Steinbeck Forum .... Tues. 3:40 to 5:45 pm

3:40 pm: **Mask complexity reduction, quality assurance, and yield improvement through smart design**, A. P. Balasinski, J. Cetin, Cypress Semiconductor Corp. .... [6349-13]

4:05 pm: **Litho-friendly design (LfD) methodologies applied to library cells**, R. März, K. Peter, S. Gröndahl, W. Maurer, Infineon Technologies AG (Germany) .... [6349-14]

4:30 pm: **Integrated DFM framework for dynamic yield optimization**, F. G. Pikus, Mentor Graphics Corp. .... [6349-15]

4:55 pm: **Application of Dosemapper for 65-nm gate CD control: strategies and results**, N. N. Jeewakhan, N. Shamma, Cypress Semiconductor Corp. .... [6349-16]

5:20 pm: **Fast dual-graph-based hot-spot detection**, X. Xu, A. B. Kahng, C. Park, Univ. of California/San Diego .... [6349-148]

SESSION 5: Mask Substrate and Materials

Chairs: **Ute Buttgereit**, SCHOTT Lithotec AG (Germany); **Roxann L. Engelstad**, Univ. of Wisconsin/Madison

Room: Ferrante .... Tues. 10:35 am to 12:15 pm

10:35 am: **Multi-layer resist system for 45-nm-node and beyond, part I**, M. Hashimoto, H. Shiratori, K. Horii, Y. Yokoya, HOYA Corp. (Japan); H. Takamizawa, Y. Fujimura, J. Morimoto, A. Manoshiro, M. Shimizu, T. Yokoyama, Dai Nippon Printing Co., Ltd. (Japan); T. Enomoto, M. Nagai, Nissan Chemical Industries, Ltd. (Japan) .... [6349-18]

11:00 am: **Process window enhancement for 45-nm and 65-nm node using alterable transmission phase-shifting materials**, H. W. Becker, M. Renno, U. Buttgereit, SCHOTT Lithotec AG (Germany); C. Koepernik, L. Nedelmann, M. Irmscher, Institut für Mikroelektronik Stuttgart (Germany); R. Birkner, A. M. Zibold, Carl Zeiss SMT GmbH (Germany) .... [6349-19]

11:25 am: **Optical issues of thin organic pellicles in 45-nm and 32-nm immersion lithography**, K. D. Lucas, Freescale Semiconductor, Inc. (France); J. S. Gordon, Toppan Photomasks, Inc.; M. Saied, W. E. Conley, S. P. Warrick, Freescale Semiconductor, Inc. (France); M. Pochkowski, KLA-Tencor Corp.; C. A. West, F. D. Kalk, Toppan Photomasks, Inc. .... [6349-20]

11:50 am: **Solid immersion masks**, M. J. Cangemi, IMEC (Belgium) and Photronics; L. H. A. Leunissen, V. Philipsen, IMEC (Belgium); D. Taylor, Photronics, Inc. .... [6349-21]

Lunch/Exhibition Break .... 12:15 to 1:30 pm

SESSION 6: Metrology I

Chairs: **Craig A. West**, Toppan Photomasks, Inc.; **Thomas H. Newman**, Micronic Laser Systems AB

Room: Ferrante .... Tues. 1:30 to 3:10 pm

1:30 pm: **Contact hole CD and profile metrology of binary and phase-shift masks: effect of modeling strategies in application of scatterometery**, K. M. Lee, M. Tavassoli, Intel Corp.; S. K. Yedur, Timbre Technologies, Inc.; K. Baik, Intel Corp. .... [6349-22]

1:55 pm: **Improved prediction of across chip linewidth variation (ACLV)**, E. R. Poortinga, Carl Zeiss SMT Inc.; A. M. Zibold, Carl Zeiss SMS GmbH (Germany); W. E. Conley, L. C. Litt, Freescale Semiconductor, Inc.; B. S. Kasprowicz, M. Cangemi, Photronics, Inc. .... [6349-23]

2:20 pm: **Design-based mask metrology hot spot classification and recipe making through pattern recognition**, Y. Cui, K. Baik, R. E. Gleason, M. Tavassoli, Intel Corp. .... [6349-24]

2:45 pm: **Determination of spatial CD signatures on photomasks**, C. S. Utzny, Advanced Mask Technology Ctr. (Germany); M. Rößiger, Infineon Technologies AG (Germany) .... [6349-25]

Coffee Break .... 3:10 to 3:40 pm

SESSION 7: Inspection

Chairs: **Benjamin G. Eynon, Jr.**, KLA-Tencor Corp.; **Wilhelm Maurer**, Infineon Technologies AG (Germany)

Room: Ferrante .... Tues. 3:40 to 5:45 pm

3:40 pm: **Reticle requalification and disposition of defects in a 193-nm wafer fab environment**, R. M. Schmid, Carl Zeiss SMT Inc.; K. Gutjahr, Infineon Technologies AG (Germany); S. M. Labovitz, KLA-Tencor Corp.; E. R. Poortinga, Carl Zeiss SMT Inc.; A. M. Zibold, Carl Zeiss SMS GmbH (Germany) .... [6349-26]

4:05 pm: **Analysis of optical lithography capabilities of pixelized photomasks and spatial light modulators**, A. M. Latypov, KLA-Tencor Corp. .... [6349-27]

4:30 pm: **High-resolution mask inspection in advanced fab**, S. Maelzer, A. Poock, Advanced Micro Devices, Inc. (Germany); K. Bhattacharyya, F. Mirzaagha, S. Cox, M. Lang, B. W. Reese, KLA-Tencor Corp. .... [6349-28]

4:55 pm: **Limitations of optical reticle inspection for 45-nm node and beyond**, S. Teuber, J. P. Heumann, C. Holfeld, A. C. Dürr, Advanced Mask Technology Ctr. (Germany) .... [6349-29]

5:20 pm: **Wafer fab mask qualification techniques and limitations**, A. Poock, S. Maelzer, Advanced Micro Devices, Inc. (Germany); C. Tabery, C. Spence, Advanced Micro Devices, Inc.; M. Lang, G. Schnasse, KLA-Tencor Corp. (Germany); K. Bhattacharyya, KLA-Tencor Corp. .... [6349-30]

✔ Posters—Tuesday

The following poster papers will be displayed after the morning coffee break on Tuesday (closed from 4:00 to 6:00 pm) and on Wednesday until 3:00 pm in the Exhibit Hall. Authors will be present during the Exhibition/Poster Reception from 6:00 to 7:30 pm Tuesday evening to answer questions and provide in-depth discussion regarding their posters. All posters are part of the Photomask Best Poster Contest

Authors may set-up their posters Tuesday between 10:30 am to 4:00 pm, and will leave them up until Wednesday afternoon at 3:00 pm. Posters not set-up by the 4:00 pm cut-off time may be considered no-show and their manuscripts will not be published. All poster authors will be present during the Poster Reception 6:00 to 7:30 pm Tuesday evening to answer questions and provide in-depth discussion regarding their poster. Any posters not removed by Wednesday at 3:00 pm will be considered unwanted and will be discarded. SPIE assumes no responsibility for papers left up after 3 pm on Wednesday.

Advanced RET

✔ **The study of chromeless phase lithography (CPL) for 45-nm lithography**, S. Tan, Q. Lin, Chartered Semiconductor Manufacturing Ltd. (Singapore); C. J. Tay, C. Quan, National Univ. of Singapore (Singapore) .... [6349-98]

✔ **A novel approach for hot-spot removal for sub-100-nm manufacturing**, C. Wu, M. W. Ma, Aprio Technologies, Inc. .... [6349-99]

✔ **A novel Alt-PSM structure: isn't this embedded atten-PSM?**, S. Nakao, K. Hosono, S. Maejima, K. Narimatsu, K. Suko, Renesas Technology Corp. (Japan) .... [6349-100]

✔ **Real-time ultra-sensitive ambient ammonia monitor for advanced lithography**, E. R. Crosson, E. H. Wahl, C. W. Rella, Picarro; K. Nishimura, Y. Sakaguchi, Horiba, Ltd. (Japan) .... [6349-101]

Cleaning

✔ **Qualitative analysis of haze defects**, J. Choi, Samsung Electronics Co., Ltd. (South Korea) .... [6349-103]

✔ **Haze detection and haze-induced process latitude variation**, S. Kim, J. B. Park, Hanyang Univ. (South Korea); S. Kim, Samsung Electronics Semiconductor (South Korea); Y. Kang, J. Kim, S. Park, I. An, H. Oh, Hanyang Univ. (South Korea) .... [6349-105]

✔ **Nonchemical cleaning technology for sub-90-nm design node photomask manufacturing**, R. Chen, M. Kozuma, Toppan Chunghwa Electronics Co., Ltd. (Taiwan) .... [6349-106]

✔ **Novel cleaning techniques to achieve defect-free photomasks for sub-65-nm nodes**, J. H. Ryu, D. W. Lee, J. S. Ryu, S. P. Kim, O. Han, Hynix Semiconductor Inc. (South Korea) .... [6349-109]

✔ **Cleaning of MoSi multilayer mask blanks for EUVL**, V. Kapila, A. Rastegar, SEMATECH, Inc.; Y. Ikuta, Asahi Glass America; S. K. Eichenlaub, K. Goncher, P. Marmillion, SEMATECH, Inc. .... [6349-110]

✔ **Mechanism of megasonic damages for micro-patterns**, S. Shimada, Y. Suwa, A. Shigihara, H. Ishii, Y. Shoji, M. Ohtsuki, S. Sasaki, A. Naitoh, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan) .... [6349-113]

✔ **A novel photoreactive surface processing system**, D. J. Elliott, V. M. Chaplick, UVTech Systems, Inc. .... [6349-114]

DPI/DFM

✔ **An effective layout optimization method via LFD concept**, C. Wang, C. Hung, Semiconductor Manufacturing International Corp. (China); G. Gao, Mentor Graphics Corp. (China) .... [6349-115]

✔ **Bringing the GDSII to silicon flow into design to improve design manufacturability** *(Presentation Only)*, P. Hurat, Clear Shape Technologies, Inc. .... [6349-116]

✔ **Adding grayscale layers to chrome photomasks**, G. H. Chapman, D. K. Poon, J. Dudas, J. Wang, C. Choo, Y. Tu, Simon Fraser Univ. (Canada); A. G. Zanzal, P. Reynolds, Benchmark Technologies .... [6349-117]

✔ **Poly-silicon gate and poly-silicon wire CD/EPE defect detection and classification**, B. Su, W. W. Volk, X. Li, S. Chen, H. Du, S. D. Andrews, B. Kumar, R. Pulusuri, KLA-Tencor Corp. .... [6349-198]

Etch

✔ **Chrome etch challenges for 45-nm and beyond**, I. M. Ibrahim, M. Chandrachood, M. N. Grimbergen, E. Gabriel, X. Chen, A. Kumar, S. J. Panayil, Applied Materials PPC .... [6349-118]

✔ **Quartz etch challenges for 45-nm phase-shift masks**, M. Chandrachood, S. A. Anderson, B. T. Y. Leung, I. M. Ibrahim, S. J. Panayil, A. Kumar, Applied Materials PPC .... [6349-119]

✔ **Multi-layer resist system for 45-nm-node and beyond, Part III**, Y. Abe, J. Morimoto, T. Yokoyama, Dai Nippon Printing Co., Ltd. (Japan); A. Kominato, Y. Ohkubo II, HOYA Corp. (Japan) .... [6349-120]

✔ **Multi-layer resist system for 45-nm-node and beyond, Part II**, Y. Fujimura, J. Morimoto, A. Manoshiro, M. Shimizu, H. Takamizawa, Dai Nippon Printing Co., Ltd. (Japan); M. Hashimoto, H. Shiratori, K. Horii, Y. Yokoya, Y. Ohkubo II, HOYA Corp. (Japan); T. Enomoto, T. Sakaguchi, M. Nagai, Nissan Chemical Industries, Ltd. (Japan) .... [6349-121]

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✔ **Current status of Mo-Si multilayer formation in ASET for low-defect-density mask blanks for EUV lithography**, K. Hiruma, Y. Tanaka, S. Miyagaki, J. Cullins, H. Yamanashi, I. Nishiyama, Association of Super-Advanced Electronics Technologies (Japan) .... [6349-122]

✔ **Predicting the influence of trapped particles on EUVL reticle distortion during exposure chucking**, V. Ramaswamy, K. T. Turner, R. L. Engelstad, E. G. Lovell, Univ. of Wisconsin/Madison .... [6349-123]

✔ **Experimental verification of finite element model prediction of EUVL mask flatness during electrostatic chucking**, M. Nataraju, J. Sohn, A. R. Mikkelson, K. T. Turner, R. L. Engelstad, Univ. of Wisconsin/Madison; C. K. Van Peski, SEMATECH, Inc. .... [6349-124]

✔ **Evaluation of bi-layer TaSix absorber on buffer for EUV mask**, K. Kanayama, S. Tamura, Y. Nishiyama, T. Matsuo, A. Tamura, Toppan Printing Co., Ltd. (Japan) .... [6349-125]

✔ **Measuring force uniformity in electrostatic chucking of EUVL masks**, J. Sohn, S. Veerarghavan, K. T. Turner, R. L. Engelstad, E. G. Lovell, Univ. of Wisconsin/Madison; C. K. Van Peski, SEMATECH, Inc. .... [6349-126]

✔ **Dependency of EUV mask defects on substrate defects**, S. K. Eichenlaub, A. Rastegar, SEMATECH, Inc.; Y. Ikuta, Asahi Glass America; K. Goncher, K. Vivek, P. Marmillion, SEMATECH, Inc. .... [6349-127]

✔ **Rigorous FEM-simulation of EUV-masks: influence of shape and material parameters**, J. Pomplun, S. Burger, F. Schmidt, L. W. Zschiedrich, Zuse Institute Berlin (Germany); F. Scholze, Physikalisch Technische Bundesanstalt (Germany) .... [6349-128]

✔ **Adhesion measurements on mask blank surfaces relevant to EUV lithography**, R. W. Huebner, SUNY/Univ. at Albany; S. K. Eichenlaub, A. Rastegar, SEMATECH, Inc.; R. E. Geer, SUNY/Univ. at Albany .... [6349-129]

✔ **Mask programmed defects for EUV mask metrology studies**, P. Gabella, SEMATECH, Inc. .... [6349-130]

✔ **Process development for EUV mask production**, T. Abe, A. Fujii, S. Sasaki, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan); T. Shoki, T. Yamada, O. Nozawa, R. Ohkubo, M. Ushida, HOYA Corp. (Japan) .... [6349-131]

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✔ **Characterization of inverse SRAF for trenches on 45-nm technology active layer**, J. Urbani, J. Chapon, STMicroelectronics (France) . [6349-132]

✔ **Comparative study of variable rim and fixed rim approximation to 3D mask topographic effect for a single boundary layer type mask**, S. Kim, S. Suh, S. Lee, Y. Kim, S. Lee, S. Lee, H. Cho, J. Moon, SAMSUNG Electronics Co., Ltd. (South Korea) .... [6349-133]

✔ **45-32-nm node photomask technology with water immersion lithography**, T. Adachi, Y. Inazuki, T. Sutou, Y. Morikawa, N. Toyama, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan) .... [6349-134]

✔ **The effects of the photomask on multi-phase test monitors**, G. R. McIntyre, A. R. Neureuther, Univ. of California/Berkeley .... [6349-135]

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- ✔ **Study of chromeless mask quartz defect detection capability for 80-nm post structure**, J. Lu, Toppan Chunghwa Electronics Co., Ltd. (Taiwan) .... [6349-136]
- ✔ **Single pass die-to-database tritone reticle inspection capability**, B. W. Reese, KLA-Tencor Corp.; J. P. Heumann, Advanced Mask Technology Ctr. (Germany); N. J. Schmidt, KLA-Tencor Corp. (Germany) .... [6349-137]
- ✔ **Development of next-generation mask inspection method by using the feature of mask image captured with 199-nm inspection optics**, Y. Tsuji, N. Kikuiri, S. Murakami, K. Takahara, K. Matsumura, K. Yamashita, I. Isomura, R. Hirano, M. Tateno, Y. Tamura, N. Takayama, K. Usuda, Advance Mask Inspection Technology, Inc. (Japan) .... [6349-138]
- ✔ **A cost model comparing image qualification and direct mask inspection**, T. Higashiki, Toshiba Corp (Japan); K. Bhattacharyya, V. Hazari, D. Sutherland, KLA-Tencor Corp. .... [6349-139]
- ✔ **Inspectability and printability of lines and spaces halftone masks for the advanced DRAM node**, A. C. Dürr, Advanced Mask Technology Ctr. (Germany); K. Gutjahr, Qimonda AG (Germany); J. P. Heumann, Advanced Mask Technology Ctr. (Germany); M. Stengl, AMTC (Germany); F. Katzwinkel, A. Frangen, Qimonda AG (Germany); T. Witte, Advanced Mask Technology Ctr. (Germany) .... [6349-140]
- ✔ **Mask defect inspection system using backscattered electron image**, K. Takahashi, M. Ataka, T. Namae, Holon Co., Ltd. (Japan) .... [6349-199]
- ✔ **Optimization of development process using after develop inspection in mask manufacturing**, H. Y. Kim, D. H. Hwang, S. P. Kim, O. Han, Hynix Semiconductor Inc. (South Korea); K. Park, N. Kim, KLA-Tencor Corp. (South Korea); D. H. Kim, KLA-Tencor Corp. .... [6349-200]
- ✔ **Defining defect specifications to optimize photomask production and requalification,** P. Fiekowsky, AVI-Automated Visual Inspection . [6349-203]

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- ✔ **The automatic back-check mechanism of mask tooling database and automatic transmission of mask tooling data**, R. Xu, M. G. Peng, L. Tu, HeJian Technology Co., Ltd. (China) .... [6349-141]
- ✔ **Distributed-computing in mask data preparation for 45-nm node and below**, W. Zhang, E. Y. Sahouria, S. F. Schulze, Mentor Graphics Corp. .... [6349-142]
- ✔ **Incoming database verification and management for mask data preparation**, F. Chen, Toppan Chunghwa Electronics Co., Ltd. (Taiwan) .... [6349-143]
- ✔ **Parallel processing of layout data with selective data distribution**, M. Pereira, M. Pereira, SoftJin Technologies Pvt. Ltd. (India) .... [6349-144]
- ✔ **Advanced manufacturing rules check (MRC) for fully automated assessment of complex reticle designs: part II**, J. A. Straub, D. Aguilar, P. D. Buck, D. Dawkins, R. Gladhill, S. Nolke, J. Riddick, Toppan Photomasks, Inc. .... [6349-145]
- ✔ **Load balancing using DP management server for commercial MDP software**, J. Kim, W. Ki, J. Choi, S. Choi, W. Han, SAMSUNG Electronics Co., Ltd. (South Korea) .... [6349-146]
- ✔ **Mask rule checker: SmartMRC**, K. Kato, SII NanoTechnology Inc. (Japan) .... [6349-147]

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- ✔ **Advanced CD AFM metrology for 3D critical shape and dimension control of photomask etch processing**, T. Bao, Veeco Instruments Inc.; A. Zerrade, Micron Technology Inc. .... [6349-149]
- ✔ **Introduction of a die-to-database verification tool for mask geometry NGR4000**, T. Kitamura, NanoGeometry Research Inc. (Japan); M. J. Hoffman, NanoGeometry Research Inc. .... [6349-150]
- ✔ **A new algorithm for SEM critical dimension measurements for differentiating between lines and spaces in dense line/space patterns without tone dependence**, J. Matsumoto, Y. Ogiso, M. Sekine, Advantest Corp. (Japan); J. M. Whittey, Vistec Semiconductor Systems, Inc. .... [6349-152]
- ✔ **Automate mask qualification with new CD metrology in a CATS™ environment**, H. Boerland, R. J. Lesnick, Jr., Synopsys, Inc. .... [6349-153]
- ✔ **Utilize AIMS simulation to estimate profile side-wall angle**, C. Lu, Photronics Semiconductor Mask Corp. (Taiwan) .... [6349-154]
- ✔ **Multi-point CD measurement method to evaluate pattern fidelity and performance of mask**, M. Kim, Y. Choi, O. Han, Hynix Semiconductor Inc. (South Korea) .... [6349-155]
- ✔ **Through-pellicle CDU assessment of masks at wafer level based on aerial image measurements**, R. M. Schmid, E. R. Poortinga, Carl Zeiss SMT Inc.; A. M. Zibold, Carl Zeiss SMS GmbH (Germany) .... [6349-156]
- ✔ **A new critical dimension metrology for chrome-on-glass substrates based on s-parameter measurements extracted from coplanar waveguide test structures**, C. A. Nwokoye, M. Zagloul, George Washington Univ.; M. W. Cresswell, R. A. Allen, C. E. Murabito, National Institute of Standards and Technology .... [6349-157]
- ✔ **Revisiting mask contact hole measurements**, M. Higuchi, Toppan Electronics; R. R. Bowley, Jr., A. E. McGuire, E. E. Gallagher, IBM Microelectronics Div. .... [6349-158]
- ✔ **Investigation of adhesive energy of micro-patterns for under 65-nm node**, S. Shimada, Y. Yoshida, S. Sasaki, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan) .... [6349-161]
- ✔ **Novel technique for critical dimension measurements of phase-shift masks using broadband transmittance spectra in conjunction with RCWA**, A. Gray, Univ. of California/Davis; J. C. Lam, S. S. Chen, n&k Technology, Inc. .... [6349-162]

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- ✔ **A general framework for multi-flow, multi-layer, multi-project reticles design**, A. B. Kahng, X. Xu, Univ. of California/San Diego .... [6349-165]

Patterning

- ✔ **CP mask optimization for enhancing the throughput of MCC systems**, M. Sugihara, Institute of Systems & Information Technologies/KYUSHU (Japan); K. Nakamura, Y. Matsunaga, K. Murakami, Kyushu Univ. (Japan) .... [6349-166]
- ✔ **Evaluation of writing strategy with one and two pass on OPC technology using EBM writing system**, C. Tseng, K. Cheng, D. Lee, S. Yang, C. Wu, Taiwan Mask Corp. (Taiwan) .... [6349-167]
- ✔ **Self-aligned resist patterning on Cr/MoSiN patterns by backside flood exposure in photomask**, T. Ha, B. Gyun, O. Han, Hynix Semiconductor Inc. (South Korea) .... [6349-168]

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- ✔ **Production defect repair performance: analysis of advanced repair processes on production masks**, C. Ehrlich, Carl Zeiss SMS GmbH (Germany); K. Edinger, J. Oster, NaWoTec GmbH (Germany) .... [6349-170]
- ✔ **Precise and high-throughput femtopulse laser mask repair of large defects**, T. E. Robinson, J. LeClaire, R. White, D. A. Lee, Rave LLC .... [6349-171]
- ✔ **Advanced femtosecond DUV laser mask repair tool for large area photomasks**, L. Treyger, J. W. Heyl, M. Fink, Controlled Semiconductor, Inc.; Y. Li, Intel Corp.; F. Small, J. Sung, B. Xian, Controlled Semiconductor, Inc. .... [6349-172]
- ✔ **Repair specification for 45-nm node photomask repair**, M. G. Sung, SAMSUNG Electronics Co., Ltd. (South Korea) .... [6349-173]

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- ✔ **Thermal modeling of photomask precision baking system**, K. Matsubara, Niigata Univ. (Japan); S. Miyazaki, MTC Co., Ltd. (Japan); T. Hoshino, MTC Co., Ltd (Japan); S. Rack, Convergent Manufacturing Technology Inc.; M. Kobayashi, Niigata Univ. (Japan) .... [6349-174]
- ✔ **More evolved PGSD (proximity gap suction developer) for controlling movement of dissolution product**, H. Sakurai, Y. Oppata, K. Murano, M. Sakai, T. Higaki, M. Itoh, H. Watanabe, Toshiba Corp. (Japan); H. Funakoshi, K. Ooishi, Y. Okamoto, M. Kaneda, S. Kamei, Tokyo Electron Kyushu Ltd. (Japan); N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan) .... [6349-175]

RET/OPC

- ✔ **No-forbidden-pitch SRAF rules for advanced contact lithography**, C. Wang, C. Hung, Q. Liu, Semiconductor Manufacturing International Corp. (China); L. Zhang, Mentor Graphics Corp. (China) .... [6349-177]
- ✔ **Accounting for lens aberrations into the OPC model calibration**, L. Depre, Synopsys, Inc. (France); C. M. Cork, Synopsys, Inc. .... [6349-178]
- ✔ **Correlation between OPC model accuracy and image parameters**, C. Kallingal, N. S. Chen, Advanced Micro Devices, Inc. .... [6349-179]
- ✔ **Minimizing yield-loss risks through post-OPC verification**, T. Wang, Semiconductor Manufacturing International Corp. (China); T. E. Brist, Mentor Graphics Corp.; C. Hung, Semiconductor Manufacturing International Corp. (China); R. Zhang, G. Gao, Mentor Graphics Corp. (China); S. D. Shang, T. M. Donnelly, Mentor Graphics Corp. .... [6349-180]

✔ **The effect of sub-layer condition on the OPC model**, J. Y. Choi, J. Kang, Y. A. Shim, K. H. Yun, J. Lee, Y. Lee, K. Kim, DongbuAnam Semiconductor Inc. (South Korea) .... [6349-181]

✔ **Efficient approach to improving pattern fidelity with multi-OPC model and recipe**, M. Do, J. Kang, J. Lee, Y. Lee, K. Kim, DongbuAnam Semiconductor Inc. (South Korea) .... [6349-182]

✔ **Model-based lithography verification using the new manufacturing sensitivity model**, D. N. Zhang, L. S. Melvin III, Synopsys, Inc. .. [6349-183]

✔ **On objectives and algorithms of inverse methods in microlithography**, Y. Granik, Mentor Graphics Corp. .... [6349-184]

✔ **Auxiliary pattern for cell-based OPC**, C. Park, A. B. Kahng, Univ. of California/San Diego .... [6349-185]

✔ **Inverse lithography technology at low-k1**, D. S. Abrams, L. Pang, A. J. Moore, Luminescent Technologies, Inc. .... [6349-186]

Simulation

✔ **Parametric uncertainty in optical image modeling**, J. E. Potzick, E. Marx, National Institute of Standards and Technology; M. P. Davidson, Spectel Research Corp. .... [6349-187]

✔ **Illumination optimization for 65-nm technology node**, C. Wang, C. Hung, Q. Liu, Semiconductor Manufacturing International Corp. (China); L. Zhang, Mentor Graphics Corp. (China) .... [6349-188]

✔ **Printability of sub-wavelength mask features and defects**, W. Cheng, Intel Corp. .... [6349-189]

✔ **Beyond rule-based physical verification**, W. Hoppe, Qimonda AG (Germany); T. C. Rössler, Infineon Technologies AG (Germany); A. Torres, Mentor Graphics Corp. .... [6349-190]

✔ **Theoretical modelling and experimental verification of the influence of Cr edge profiles on microscopic-optical edge signals for COG masks**, B. Bodermann, D. Bergmann, A. Diener, G. Ehret, W. Haessler-Grohne, Physikalisch-Technische Bundesanstalt (Germany) .... [6349-191]

✔ **Rigorous simulation of 3D masks**, S. Burger, Zuse Institute Berlin (Germany); R. Köhle, Infineon Technologies AG (Germany); L. W. Zschiedrich, Zuse Institute Berlin (Germany); H. Nguyen, Infineon Techologies SC300 GmbH & Co. OHG (Germany); F. Schmidt, Zuse Institute Berlin (Germany); R. März, Infineon Technologies AG (Germany); C. Noelscher, Infineon Techologies SC300 GmbH & Co. OHG (Germany) .... [6349-192]

✔ **Propagation of resist heating mask errors to wafer level**, S. V. Babin, Abeam Technologies; L. N. Karklin, Sagantec North America ...... [6349-193]

Substrate/Materials

✔ **A new criterion of mask birefringence for polarized illumination**, K. Iwase, B. Thunnakart, T. Kaneguchi, K. Ozawa, Sony Atsugi Technology Ctr. (Japan); T. Yokoyama, Y. Morikawa, Dai Nippon Printing Co., Ltd. (Japan); F. Uesawa, Sony Atsugi Technology Ctr. (Japan) .... [6349-194]

✔ **Reticle carrier material as ESD protection**, D. Helmholz, M. Lering, Advanced Mask Technology Ctr. (Germany) .... [6349-195]

✔ **Experimental investigation of photomask with near-field polarization imaging**, T. Chen, T. D. Milster, S. Yang, College of Optical Sciences/The Univ. of Arizona .... [6349-196]

✔ **The effect between mask blank flatness and wafer print process window in ArF 6% att. PSM mask**, J. Tzeng, Toppan Chunghwa Electronics Co., Ltd (Taiwan) .... [6349-197]

Wednesday 20 September

SESSION 8: Patterning

Chairs: **Thomas H. Newman**, Micronic Laser Systems AB; **Naoya Hayashi**, Dai Nippon Printing Co., Ltd. (Japan)

Room: Steinbeck Forum .... Wed. 8:00 to 10:05 am

8:00 am: **Multipass VSB writing strategies for the 45-nm node and beyond**, A. T. Sowers, M. Kamna, N. Wilcox, D. M. Cole, M. Chandramouli, A. Carlos, R. Nagpal, S. Sampat, Intel Corp. .... [6349-31]

8:25 am: **Pattern density related CD corrections in mask making and their implications for model-based OPC at 45-nm node and beyond**, Z. Benes, IBM Corp.; J. Kotani, Toppan Electronics .... [6349-32]

8:50 am: **Study of the beam blur and its effect on the future mask fabrication**, S. Lee, B. Kim, S. W. Choi, W. S. Han, SAMSUNG Electronics Co., Ltd. (South Korea) .... [6349-33]

9:15 am: **Improved photomask accuracy with a high-productivity DUV laser pattern generator**, T. Öström, J. Måhlén, A. Karawajczyk, M. Rosling, P. Carlqvist, P. Askebjer, T. Karlin, J. Sallander, A. Österberg, P. Högfeldt, H. J. Sjöberg, Micronic Laser Systems AB (Sweden) .... [6349-34]

9:40 am: **Metrics to assess fracture quality for variable shaped beam lithography**, M. Blöcker, Advanced Mask Technology Ctr. (Germany); R. Gladhill, P. D. Buck, Toppan Photomasks, Inc.; M. Kempf, Advanced Mask Technology Ctr. (Germany); D. Aguilar, Toppan Photomasks, Inc.; R. B. Cinque, Advanced Mask Technology Ctr. (Germany) .... [6349-169]

Coffee Break .... 10:05 to 10:35 am

Sessions 9-10-11 run concurrently with sessions 12-13-14.

SESSION 9: Extreme NA/Immersion

Chairs: **John C. H. Lin**, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan); **Donis G. Flagello**, ASML US, Inc.

Room: Steinbeck Forum .... Wed. 10:35 am to 12:15 pm

10:35 am: **Process window results using pitch decomposition at k1eff<0.20**, J. A. Huckabay, Cadence Design Systems, Inc.; R. J. Socha, S. D. Hsu, ASML MaskTools Inc.; R. J. Naber, Cadence Design Systems, Inc.; M. V. Dusa, ASML MaskTools Inc. .... [6349-36]

11:00 am: **32-nm node flash contact hole printing using double patterning, CPL mask, and hyper-NA immersion lithography with optimized illumination**, T. Chen, ASML MaskTools Inc. .... [6349-37]

11:25 am: **Image degradation due to phase effects in chromeless phase lithography**, K. Bubke, M. Sczyrba, R. Neubauer, K. Park, Advanced Mask Technology Ctr. (Germany); R. Pforr, R. Ziebold, Infineon Technologies AG (Germany) .... [6349-38]

11:50 am: **Imaging performance at 45-nm of various PSM technologies**, W. E. Conley, Freescale Semiconductor, Inc.; E. R. Poortinga, Carl Zeiss SMT Inc.; A. M. Zibold, Carl Zeiss SMS GmbH (Germany); L. C. Litt, Freescale Semiconductor Inc.; B. S. Kasprowicz, M. Cangemi, N. Morgana, Photronics, Inc. .... [6349-39]

Lunch/Exhibition Break .... 12:15 to 1:30 pm

SESSION 10: MDP/MRC

Chairs: **Richard D. Morse**, Morse Consulting; **J. Fung Chen**, ASML MaskTools Inc.

Room: Steinbeck Forum .... Wed. 1:30 to 3:10 pm

1:30 pm: **Advanced non-disruptive manufacturing rule checks (MRC)**, T. Do, B. Moore, R. E. Morgan, Synopsys, Inc. .... [6349-40]

1:55 pm: **A generic method for the detection of electrically superfluous layout features**, M. M. H. Hofsaess, T. C. Roessler, E. Nash, Infineon Technologies AG (Germany) .... [6349-41]

2:20 pm: **Mask spec projection for wafer process optimization**, L. Chen, P. E. Freiberger, Intel Corp. .... [6349-42]

2:45 pm: **A memory efficient large mask data handling method using repetition**, J. Choi, SAMSUNG Electronics Co., Ltd. (South Korea) ... [6349-43]

Coffee Break .... 3:10 to 3:40 pm

SESSION 11: Simulation

Chairs: **Donis G. Flagello**, ASML US, Inc.; **Frank A. J. M. Driessen**, Takumi Technology Corp. (Netherlands)

Room: Steinbeck Forum .... Wed. 3:40 to 5:20 pm

3:40 pm: **Sensitivity of VT5 model toward process and modeling parameters**, M. Saied, Freescale Semiconductor, Inc. (France); F. Foussadier, STMicroelectronics (France); Y. Trouiller, CEA-LETI (France); I. Shanen, Ecole Nationale Superieure d'Electronique et de Radioelectricite de Grenoble (France); J. Belledent, Philips Semiconductors (France); K. D. Lucas, Freescale Semiconductor, Inc. (France); A. Borjon, C. Couderc, Philips Semiconductors (France); C. Gardin, Freescale Semiconductor, Inc. (France); L. Le-Cam, Y. F. Rody, Philips Semiconductors (France); F. Sundermann, J. Urbani, STMicroelectronics (France); E. Yesilada, Freescale Semiconductor, Inc. (France) .... [6349-44]

4:05 pm: **Imaging behavior of high-transmission attenuating phase-shift mask films**, M. S. Hibbs, IBM Corp.; S. Nemoto, IBM Burlington; T. Komizo, Toppan Printing Co., Ltd. (Japan) .... [6349-45]

4:30 pm: **Optical properties of alternating phase-shifting masks**, B. Gleason, W. Cheng, Intel Corp. .... [6349-46]

4:55 pm: **Optimization of process window simulations for litho friendly design framework**, M. Al-Imam, Mentor Graphics Corp. (Egypt); A. Torres, Mentor Graphics Corp.; R. S. Fathy, H. Diab, M. M. Fakhry, Mentor Graphics Corp. (Egypt) .... [6349-47]

SESSION 12: Repair

Chairs: **Ron R. Bozak**, Rave LLC; **J. Tracy Weed**, Synopsys, Inc.

Room: Ferrante .... Wed. 10:35 am to 12:15 pm

10:35 am: **Impact of AFM scan artifacts on photolithographic simulation**, T. E. Robinson, D. A. Lee, Rave LLC; J. Lewellen, S. Hoffer, P. Brooker, Sigma-C .... [6349-49]

11:00 am: **Advanced photomask repair technology for 65-nm lithography**, F. Aramaki, SII NanoTechnology Inc. (Japan) .... [6349-50]

11:25 am: **New application results from advanced review and repair toolkit for 45-nm node masks and beyond**, C. Ehrlich, Carl Zeiss SMS GmbH (Germany); K. Edinger, NaWoTec GmbH (Germany); A. M. Zibold, R. Richter, W. Degel, Carl Zeiss SMS GmbH (Germany) .... [6349-51]

11:50 am: **Mask repair using layout-based pattern copy for the 65-nm node and beyond**, V. A. Boegli, NaWoTec GmbH (Germany); U. Hofmann, GenISys GmbH (Germany) .... [6349-52]

Lunch/Exhibition Break .... 12:15 to 1:30 pm

SESSION 13: Cleaning

Chairs: **Brian J. Grenon**, Grenon Consulting, Inc.; **Naoya Hayashi**, Dai Nippon Printing Co., Ltd. (Japan)

Room: Ferrante .... Wed. 1:30 to 3:10 pm

1:30 pm: **A new model of haze generation and storage-life-time estimation for mask**, S. Shimada, N. Kanda, N. Takahashi, H. Nakajima, H. Tanaka, H. Ishii, Y. Shoji, M. Ohtsuki, A. Naitoh, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan) .... [6349-53]

1:55 pm: **Real-time monitoring based on comprehensive analysis**, J. Choi, Samsung Electronics Co., Ltd. (South Korea) .... [6349-54]

2:20 pm: **Sulfur-free cleaning strategy for advanced mask manufacturing**, L. M. Kindt, A. J. Watts, IBM Microelectronics Div.; J. Burnham, W. A. Aaskov, IBM Corp. .... [6349-107]

Coffee Break .... 3:10 to 3:40 pm

SESSION 14: Metrology II

Chairs: **Artur P. Balasinski**, Cypress Semiconductor Corp.; **Johnson C. Hung**, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan)

Room: Ferrante .... Wed. 3:40 to 5:45 pm

3:40 pm: **Simulation of critical dimension and profile metrology based on scatterometry method**, R. Chalykh, I. Pundaleva, S. Kim, S. Lee, H. Cho, J. Moon, SAMSUNG Electronics Co., Ltd. (South Korea) .... [6349-57]

4:05 pm: **Segmentation-assisted edge extraction algorithms for SEM images**, H. Feng, Stanford Univ.; J. Ye, Brion Technologies, Inc. and Stanford Univ.; F. Pease, Stanford Univ. .... [6349-58]

4:30 pm: **Analysis of the Leica LMS IPRO3 performance**, G. Antesberger, S. Knoth, F. Laske, J. Rudolf, E. P. Cotte, B. L. Alles, Advanced Mask Technology Ctr. (Germany); C. Bläsing, W. Fricke, Vistec Semiconductor Systems GmbH (Germany); K. Rinn, FH Giessen-Friedberg (Germany) .... [6349-59]

4:55 pm: **CD measurement evaluation on periodic patterns between optic tools and CD-SEM**, Y. Choi, M. Kim, O. Han, Hynix Semiconductor Inc. (South Korea) .... [6349-60]

5:20 pm: **Fast nondestructive optical measurements of critical dimension uniformity and linearity on AEI and ASI phase-shift masks**, A. Gray, Univ. of California/Davis; J. C. Lam, n&k Technology, Inc. .... [6349-61]

Thursday 21 September

Sessions 15-16-17-18 run concurrently with sessions 19-20-21-22.

SESSION 15: Advanced RET I

Chairs: **John C. H. Lin**, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan); **Mark E. Mason**, Texas Instruments Inc.

Room: Steinbeck Forum .... Thurs. 8:00 to 10:05 am

8:00 am: **Extension of 193-nm dry lithography to 45-nm half-pitch node: double exposure and double processing technique**, A. M. Biswas, J. A. Hiserote, J. Li, L. S. Melvin III, Synopsys, Inc. .... [6349-62]

8:25 am: **Identification of subresolution assist features that are susceptible to imaging through process**, L. S. Melvin III, Synopsys, Inc. .... [6349-63]

8:50 am: **A fresh look at the cell-wise process effect corrections**, D. Lapanik, Cadence Design Systems (Japan) .... [6349-64]

9:15 am: **Phase-shift reticle design impact on patterned linewidth variation and LWR**, J. E. Vasek, C. Fu, G. Chen, Freescale Semiconductor, Inc. .... [6349-65]

9:40 am: **Implement alternating PSM in sub-80-nm DRAM with gate shrinkage via single exposure**, K. Chen, Nanya Technology Corp. (Taiwan) .... [6349-66]

Coffee Break .... 10:05 to 10:35 am

SESSION 16: Advanced RET II

Chairs: **Frank A. J. M. Driessen**, Takumi Technology Corp. (Netherlands); **Woo-Sung Han**, SAMSUNG Electronics Co., Ltd. (South Korea)

Room: Steinbeck Forum .... Thurs. 10:35 am to 12:15 pm

10:35 am: **Feasibility study of mask fabrication in double exposure technology**, J. Doh, SAMSUNG Electronics Co., Ltd. (South Korea) . [6349-67]

11:00 am: **High-transmission attenuated phase-shift mask for ArF immersion lithography**, Y. Kojima, T. Mizoguchi, T. Haraguchi, T. Konishi, Y. Okuda, Toppan Printing Co., Ltd. (Japan) .... [6349-68]

11:25 am: **Mastering double exposure process window aware OPC by means of virtual targets**, H. Haffner, Infineon Technologies AG; Z. Baum, C. A. Fonseca, S. D. Halle, L. W. Liebmann, IBM Microelectronics Div.; A. P. Mahorowala, IBM Thomas J. Watson Research Ctr. .... [6349-69]

11:50 am: **Finding the needle in the haystack: using full-chip process window analysis to qualify competing SRAF placement strategies for 65 nm**, M. E. Mason, Texas Instruments Inc. .... [6349-70]

Lunch Break .... 12:15 to 1:30 pm

SESSION 17: RET/OPC I

Chairs: **Artur P. Balasinski**, Cypress Semiconductor Corp.; **J. Fung Chen**, ASML MaskTools Inc.

Room: Steinbeck Forum .... Thurs. 1:30 to 3:10 pm

1:30 pm: **Present challenges and solutions in sampling and correction for 45 nm**, I. C. Graur, IBM Microelectronics Div.; M. Imam, P. J. LaCour, Mentor Graphics Corp. .... [6349-71]

1:55 pm: **PPC model build methodology: sequential litho and etch verification**, A. Mokhberi, Invarium Inc. .... [6349-72]

2:20 pm: **Correcting lithography hot spots during physical design implementation**, G. T. Luk-Pat, A. Miloslavsky, F. Tseng, L. Wen, Synopsys, Inc. .... [6349-73]

2:45 pm: **Combined resist and etch modeling and correction for the 45-nm node**, M. Drapeau, Synopsys, Inc. (Belgium); D. F. Beale, Synopsys, Inc. .... [6349-74]

Coffee Break .... 3:10 to 3:40 pm

SESSION 19: Mask Business and Management

Chairs: **Patrick M. Martin**, Photronics, Inc.; **Brian J. Grenon**, Grenon Consulting, Inc.

Room: Ferrante .... Thurs. 8:00 to 10:05 am

8:00 am: **Benchmarking the productivity of photomask manufacturers**, C. N. Berglund, Northwest Technology Group; C. M. Weber, Portland State Univ. .... [6349-80]

8:25 am: **Required mask specification for mass production devices below 65-nm design node**, D. Nam, J. Doh, H. Lee, S. Lee, S. Choi, B. Kim, S. Choi, W. Han, SAMSUNG Electronics Co., Ltd. (South Korea) .... [6349-81]

8:50 am: **Assessing the impact to the photomask industry from external funding for infrastructure development**, M. J. Lercel, SEMATECH, Inc. and IBM Corp.; A. Grenville, SEMATECH, Inc. and Intel Corp.; P. Marmillion, SEMATECH, Inc. and IBM Corp. .... [6349-82]

9:15 am: **Mask factory automation: getting started**, P. Gabella, SEMATECH, Inc. .... [6349-83]

9:40 am: **A procedure and program to calculate shuttle mask advantage**, A. P. Balasinski, Cypress Semiconductor Corp.; A. B. Kahng, Univ. of California/San Diego; W. Sachs-Baker, Cypress Semiconductor Corp.; X. Xu, Univ. of California/San Diego .... [6349-164]

Coffee Break .... 10:05 to 10:35 am

SESSION 20: Imprint

Chairs: **Craig A. West**, Toppan Photomasks, Inc.; **Mark E. Mason**, Texas Instruments Inc.

Room: Ferrante .... Thurs. 10:35 am to 12:15 pm

10:35 am: **NIL template making and imprint evaluation**, Y. Yoshida, A. Kobiki, S. Sasaki, K. Itoh, N. Toyama, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan) .... [6349-85]

11:00 am: **Direct die-to-database electron-beam inspection of fused silica imprint templates**, M. Tsuneoka, NanoGeometry Research Inc. (Japan); D. J. Resnick, E. Thompson, Molecular Imprints, Inc.; M. Yamamoto, T. Hasebe, T. Tokumoto, C. Yan, NanoGeometry Research Inc. (Japan); W. J. Dauksher, E. S. Ainley, K. J. Nordquist, Motorola, Inc.; H. Wakamori, M. Inoue, Topcon Corp. (Japan) .... [6349-86]

11:25 am: **Systematic approach to reducing imprint template defectivity**, J. G. Maltabes, J. Brown, Photronics, Inc.; J. Perez, Molecular Imprints, Inc. .... [6349-87]

Lunch Break .... 12:15 to 1:30 pm

SESSION 21: EUV Infrastructure I

Chairs: **Emily E. Gallagher**, IBM Microelectronics Div.; **Ute Buttgereit**, SCHOTT Lithotec AG (Germany)

Room: Ferrante .... Thurs. 1:30 to 3:10 pm

1:30 pm: **PMJ Panel Discussion Overview: Mask technologies for EUVL** *(Invited Paper)*, M. Sugawara, Association of Super-Advanced Electronics Technologies (Japan); H. Sano, Dai Nippon Printing Co., Ltd. (Japan) .... [6349-89]

1:55 pm: **Manufacturing of the first EUV full-field scanner mask**, U. Dersch, R. Buettner, C. M. Chovino, S. Franz, T. Heins, H. Herguth, J. H. Peters, T. Rode, Advanced Mask Technology Ctr. (Germany); F. Letzkus, J. Butschke, M. Irmscher, Institut für Mikroelektronik Stuttgart (Germany) .... [6349-90]

2:20 pm: **Simplified model for absorber feature transmissions on EUV masks**, M. C. Lam, Mentor Graphics Corp.; A. R. Neureuther, Univ. of California/Berkeley .... [6349-91]

2:45 pm: **Profile metrology of EUV masks using scatterometry based optical digital profilometry**, S. Cho, SAMSUNG Advanced Institute of Technology (South Korea); S. K. Yedur, Timbre Technologies, Inc.; M. Tabet, Nanometrics Inc. .... [6349-92]

Coffee Break .... 3:10 to 3:40 pm

Sessions 18 and 22 run concurrently.

SESSION 18: RET/OPC II

Chairs: **Richard D. Morse**, Consultant; **Wilhelm Maurer**, Infineon Technologies AG (Germany)

Room: Steinbeck Forum .... Thurs. 3:40 to 5:45 pm

3:40 pm: **Application challenges with double patterning technology (DPT) beyond 45-nm node**, J. C. Park, S. D. Hsue, D. J. Van Den Broeke, J. F. Chen, ASML MaskTools Inc. .... [6349-75]

4:05 pm: **The effect of OPC optical and resist model parameters on the model accuracy, run-time, and stability**, A. Y. Abdo, IBM Microelectronics Div.; R. S. Fathy, Mentor Graphics Corp. (Egypt); J. M. Oberschmidt, S. M. Mansfield, M. Talbi, IBM Microelectronics Div.; A. Seoud, Mentor Graphics Corp. (Egypt) .... [6349-76]

4:30 pm: **Managing high-accuracy and fast convergence in OPC**, K. Herold, Infineon Technologies North America; N. S. Chen, Advanced Micro Devices, Inc.; I. P. Stobert, IBM Microelectronics Div. .... [6349-77]

4:55 pm: **Influence of design shrinks and proximity influence distance on flattening of optical hierarchy during RET**, J. L. Nistler, PSIDA Lithography Software .... [6349-78]

5:20 pm: **Empirical OPC rule inference for rapid RET application**, A. P. Kulkarni, Oasis Tooling, Inc. .... [6349-79]

SESSION 22: EUV Infrastructure II

Chairs: **Ron R. Bozak**, Rave LLC; **Emily E. Gallagher**, IBM Microelectronics Div.

Room: Ferrante .... Thurs. 3:40 to 5:45 pm

3:40 pm: **Development of EUVL mask blank in AGC**, T. Sugiyama, H. Kojima, M. Ito, K. Otsuka, M. Yokoyama, M. Mikami, K. Hayashi, K. Matsumoto, S. Kikugawa, Asahi Glass Co., Ltd. (Japan) .... [6349-93]

4:05 pm: **Point cleaning of mask blanks for extreme-ultraviolet lithography**, M. E. Brown, J. G. Hartley, SUNY/Univ. at Albany; K. Roessler, Rave LLC; A. Rastegar, S. K. Eichenlaub, P. Marmillion, SEMATECH, Inc. .... [6349-94]

4:30 pm: **Implementation of EUV mask pattern inspection for memory mask fabrication in 45-nm node and below**, D. Y. Kim, S. M. Huh, D. H. Chung, B. C. Cha, J. W. Lee, S. Choi, W. Han, SAMSUNG Electronics Co., Ltd. (South Korea) .... [6349-95]

4:55 pm: **Multilayer defects nucleated by substrate pits: a comparison of actinic inspection and non-actinic inspection techniques**, A. Barty, Lawrence Livermore National Lab.; K. Goldberg, Lawrence Berkeley National Lab.; P. A. Kearney, SEMATECH, Inc.; S. B. Rekawa, Lawrence Berkeley National Lab.; O. R. Wood II, SEMATECH, Inc.; J. S. Taylor, Lawrence Livermore National Lab.; H. Han, SEMATECH, Inc. .... [6349-96]

5:20 pm: **Recent imaging results from the RIM-13 high-resolution EUV aerial image microscope**, M. C. Gower, M. Booth, A. Brunton, J. S. Cashmore, P. Elbourn, G. Elliner, J. Greuters, L. Kling, N. McEntee, P. Richards, I. Wallhead, M. D. Whitfield, Exitech Ltd. (United Kingdom)................ [6349-97]

Friday 22 September

SESSION 23: Friday Special Session on DFM: Are We There Yet? Remaining Challenges and Proposed Solutions

Room: Steinbeck Forum .... Fri. 8:00 am to 1:00 pm

8:00 am: **Introduction**
Chair: **Robert J. Naber,** Cadence Design Systems, Inc.

8:10 am: **Michael J. Lercel,** Director, Lithography, SEMATECH, Inc.

8:30 am: **Christopher A. Spence,** Fellow and 2005 SPIE Microlithography Keynote Presenter, Advanced Micro Devices, Inc.

8:50 am: **Naoya Hiyashi,** Senior Researcher and General Manager of the Electronic Device Lab., Dai Nippon Printing Co., Ltd. (Japan)

9:10 am: **Wojtek J. Poppe,** Graduate Student, and the 2006 Recipient of the SPIE/BACUS Scholarship, Univ. of California/Berkeley

9:30 am: **Mark E. Mason,** Resolution Enhancement Technology Manager and Senior Member of Staff, Emeritus, Texas Instruments Inc.

9:50 am: **Artur P. Balasinski,** Manager, Technology-Design Integration, Cypress Semiconductor Corp.

Coffee Break .... 10:10 to 10:30 am

10:30 am: **Sunit Rikhi,** Director, Advanced Design, Logic Technology Development, Intel Corp.

10:50 am: **Tim Horel,** Vice-President, Hardware Development, Tabula, Inc.

11:10 am: **Peter D. Buck,** Senior Member, Technical Staff, Toppan Photomasks, Inc

11:30 am: **David Lan,** Senior Manager, DeSign Automation Applications, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan)

11:50 am: **Hidetoshi Ohnuma,** DFM Deputy General Manager, Lithography & Device Technology Dept., Sony Atsugi Technology Ctr. (Japan)

12:10 pm: **Kevin D. Lucas,** DFM Integration, Freescale Semiconductor, Inc. (France)

12:30 pm: **Christopher J. Progler,** 2007 Advanced Lithography Symposium Cochair, Chief Technology Officer, Photronics, Inc.

12:50 pm: **Closing Remarks**
Chair: **Robert J. Naber,** Cadence Design Systems, Inc.

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Data to Silicon: Understanding the Fundamentals of MDP, Frame Generation, RET and DFM

More than ever before, the creation and conversion of design data has become an integral part of the process of creating semiconductor chips. Historically, data preparation largely consisted of complex Boolean operations, fracturing, frame generation and job decks. The focus was on cycle time, cost and accuracy. Subwavelength manufacturing required for today's advanced technologies requires extraordinarily complex and expensive simulation-based software tools and a focus on manufacturability. These new elements require an even broader understanding of the entire process from design to lithography. Nevertheless, the process by which IC design data defined and turned into write-ready photomask manufacturing data still is not universally understood. This course will provide a basic overview of the entire design-to-silicon data flow. It will describe the fundamentals of a GDS2 design database and how this relates to the selection of manufacturing equipment, and the relationship to the final photomask and wafer images. The use of Boolean operations and other manipulations of the design data to create photomask layer data, including 'dummy-data,' OPC and PSM, will also be described. DFM will be defined and a general overview of the work being done in the DFM arena to enable high end manufacturing will be presented. In addition, more traditional backend functions like reticle layout optimization, frame generation, job decks, and fracturing will be covered along with an overview of the use of the SEMI P-10 standard.

LEARNING OUTCOMES

This course will enable you to:
- understand many of the terms related to tapeout
- describe the structure of a GDS2 database, the use of layers and datatypes
- explain the different kinds of grids and address units and their impact on manufacturing strategy
- use basic "Booleans," understand what "dummy-data" is, and avoid the misuse of "biases"
- understand frame generation, job decks, and SEMI P-10 automation
- become familiar with the various MPW (Multi-Project Wafer) layout strategies
- identify the basic functions of OPC and PSM, and describe the data processing issues
- summarize the key issues related to DFM and some of the solutions being developed
- understand the key elements and issues in preparing design data for chip manufacturing

INTENDED AUDIENCE

The course is intended for anybody in the IC design to manufacturing flow including, of course, mask makers. It presumes at least a basic understanding of what a photomask is and how it is used, including a general knowledge of the major manufacturing steps and equipment. However, the concentration will be on a layman's approach to the understanding of the principals without complex scientific discussion. Designers, CAD engineers, data prep/planning operators, anybody involved in tapeout, chip-finishing and of course, those in manufacturing who use, make, or specify masks. Management will develop an appreciation for the strategic manufacturing issues which start back in design and the earliest stages of technology development.

INSTRUCTOR

Richard Morse has worked in tapeout and mask data-prep positions for most of his 30+ years in the industry. He was Director of Mask Engineering at Cirrus Logic for over 14 years and the founder of D2W, the industry's first DFM and data preparation services company. Mr. Morse has been the session chair for the SPIE/BACUS Data Preparation and Design session since its inception in 1999.

Course level: Introductory

SC505 CEU .65 $440 / $520 USD
Monday 8:30 am to 5:30 pm

Photomask Fabrication and Technology Basics

This course provides attendees with a basic knowledge of photomasks. The course focuses on mask technology and the challenges associated with design data conversions, lithography, process, metrology, inspection, and advanced mask manufacture. Other topics such as the application of SPC, signature matching, etc., will also be covered.

LEARNING OUTCOMES

This course will enable you to:
- Have an understanding and appreciation of mask making
- Understand mask specification and its impact
- Comprehend the constraints and impact of design conversion and replication on the mask
- Compare the benefits of various mask writing tools and their respective writing strategies
- Identify potential challenges in current and future design, lithography, and metrology strategies

INTENDED AUDIENCE

This material is intended for anyone who needs to learn about the basics of mask making and where it fits in the microlithography process. As there is a focus on design data conversion and its impact, those who work with advanced semiconductor designs or deal with mask specification will find this course valuable.

INSTRUCTOR

John Duff has been involved in the photomask industry in an engineering/R&D capacity for 19 years. His focus has been on design database conversion, e-beam and laser lithography, metrology, SPC, inspection, and design for manufacturability. John received his B.Sc. from Glasgow University, Glasgow, Scotland, and has worked with Texas Instruments, Toppan, and Photronics. He recently joined Molecular Imprints, Inc., a manufacturer of systems for the patterning of sub-100 nm features. John is an ISO Certified Lead Assessor.

Course level: Introductory

SC579 CEU .65 $440 / $520 USD
Monday 8:30 am to 5:30 pm

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Basics of Optical Imaging in Microlithography: A Hands-on Approach

A basic 'hands on' lecture is presented, in which students are given various optical components, including a source, lenses, gratings, etc., that are used to build a personal optical bench. Basic concepts of imaging, resolution, coherence factor, on-axis illumination, off-axis illumination, binary masks, phase-shift masks, etc., are examined by the students operating in small groups under the direction of the instructor. These concepts are related to real lithographic systems using basic principles and simulation. This course is intended to provide a foundation for the follow-on course, "Imaging and Optics Fundamentals in Microlithography" (SC706).

LEARNING OUTCOMES

This course will enable you to:

- describe the basic components and relationships of a source-condenser-projector lithography system using Kohler illumination
- understand the role of the coherence factor in resolution and contrast for two-beam and three-beam lithographic systems
- describe and explain the similarities and differences of on-axis and off-axis illumination
- specify the differences in imaging properties of two-beam and three-beam optical systems
- understand the role of binary and phase-shift masks in image formation
- relate the concepts listed above to real-world lithographic problems and systems

INTENDED AUDIENCE

This course is targeted at the lithographic engineer, scientist, manager or technician with an interest in understanding basic imaging concepts with an emphasis on doing experiments and "seeing" the results.

INSTRUCTORS

Thomas Milster has worked at IBM as an optical engineer and is now an Assistant Professor at the Optical Sciences Center at the University of Arizona. Professor Milster regularly teaches a graduate core lecture class and an associated laboratory course on physical optics, which includes the topics presented in this short course. His research interests are optical data storage, micro-optics and near-field optics. He has over 100 publications and holds two patents. He is a Fellow of the SPIE and the OSA.

Peter Brooker is presently a senior engineer at Sigma-C. He provides application support as well as technical guidance to the SOLID-C lithography simulator development. Before, joining Sigma-C, he was a Motorola assignee at Sematech where he managed projects involved with the production and characterization of EUV masks. Prior to his Sematech assignment, Dr. Brooker's experience at Motorola included providing lithography simulation for advanced projects, process and device TCAD simulation, device integration as well etch process engineering.

Those interested in the course should register as early as possible, as the class size will be limited to 25 students.

Course level: Introductory

SC707 CEU .35 $270 / $310 USD
Monday 1:30 to 5:30 pm

The Limits of Optical Lithography

Over the past decade, optical lithography has remained at the forefront of the patterning of ICs in spite of the ever decreasing feature sizes required. Incremental improvements of the optical systems in combination with the use of resolution enhancement techniques (RET) have made this transition possible. The implementation of some of these techniques has lead to major infrastructure adjustments and changes covering a wide spectrum of fields including the EDA industry, the photo-mask industry, and the semiconductor equipment industry.

This course will explain the fundamental limits of optical lithography from a theoretical standpoint including the description of partially coherent imaging as well as polarization and aberration effects on the imaging quality. Commonly used resolution enhancement techniques such as off-axis illumination, phase-shifting mask, and proximity effect correction will be explained and their practical implementation will be reviewed. This course is the first part of a two part sequence but each part can be taken separately.

LEARNING OUTCOMES

This course will enable you to:

- describe partially coherent imaging, vector model, polarization and aberration effects as well as mask 3D effects
- list the benefits and limitations of resolution enhancement techniques like off-axis illumination, phase-shifting mask (alternating, attenuating, chromeless), optical proximity effect correction (OPC)
- explain the infrastructure changes required for using resolution enhancement techniques in production and their implication on data conversion, photo mask manufacturing and photo lithography processing
- explain the theory and practical ways of optimizing the illumination conditions and the mask layout for a given resolution enhancement technique

INTENDED AUDIENCE

The course is intended for those involved in the semiconductor lithography business, including but not limited to engineers, scientists, and technicians.

INSTRUCTOR

Christophe Pierrat is the director of Research and Development at the Advanced Mask Technology Center (AMTC), a joint venture between AMD, Infineon, and Toppan Photomasks. With his experience at AT&T Bell Laboratories, Micron Technologies, Numerical Technologies and Takumi, Dr. Pierrat provides comprehensive solutions to lithography issues covering the fields of data conversion, photo-mask manufacturing, and lithography. He has authored over 30 technical papers and over 100 patents in the field.

Course level: Advanced

SC723 CEU .35 $270 / $310 USD
Monday 8:30 am to 12:30 pm

Optical Lithography Extension: Design for Manufacturing and New Resolution Enhancement Techniques

Optical lithography has been extended through the use of resolution enhancement techniques (RET) like off-axis illumination, phase-shifting mask, and proximity effect correction. As these techniques reach their limits, their practical implementation becomes more dubious and requires a careful consideration of their use at the design phase in order to achieve sufficient yields.

Recently the field of design for manufacturing (DFM) has enjoyed a large success in part because of the poor ramp-up of the latest technology nodes due to limited process latitude at low k1.

At the same time, the industry is looking for new ways to improve the resolution and the process latitude on the wafer by using new resolution enhancement techniques going beyond the established techniques (off-axis illumination, phase-shifting mask, and proximity effect correction). These new techniques include immersion lithography, the use of polarized sources, or the use of multiple exposures.

This course will describe the most relevant design for manufacturing techniques and their practical implementation. The fundamentals of the new resolution enhancement techniques will also be explained and their implementation will be discussed. This course is the second part of a two part sequence but each part can be taken separately.

LEARNING OUTCOMES

This course will enable you to:

- describe design for manufacturing techniques and their implementation including the concepts of lithography-friendly designs and manufacturability check at the design phase
- use design intent information in order to speed up OPC and mask data preparation as well as reduce mask complexity and cost
- list the benefits and limitations of new resolution enhancement techniques like immersion lithography, polarized illumination, and multiple exposures
- describe the infrastructure changes required for these new resolution enhancement techniques to be transferred to production
- explore more exotic resolution enhancement techniques that might be implemented in the future

INTENDED AUDIENCE

The course is intended for those involved in the semiconductor lithography business, including but not limited to engineers, scientists, and technicians.

INSTRUCTOR

Christophe Pierrat is the director of Research and Development at the Advanced Mask Technology Center (AMTC), a joint venture between AMD, Infineon, and Toppan Photomasks. With his experience at AT&T Bell Laboratories, Micron Technologies, Numerical Technologies and Takumi, Dr. Pierrat provides comprehensive solutions to lithography issues covering the fields of data conversion, photo-mask manufacturing, and lithography. He has authored over 30 technical papers and over 100 patents in the field.

Course level: Advanced

SC724 CEU .35 $270 / $310 USD
Monday 1:30 to 5:30 pm

Polarization for Lithographers

The advent of ultra high numerical aperture (NA) systems enabled by immersion lithography has quickly brought polarization toward the top of the lithographer's list of concerns. A high index liquid between the resist and the last lens element allows better resolution by enabling larger angles of incidence, and thus more diffraction energy to couple into the resist. However various polarizing effects can become severe with these large angles of incidence. Most notably contrast from the TM component drops to near or below zero. Thus, the engineering of polarization states is becoming a necessary resolution enhancement technique. Consequently, understanding and controlling polarization throughout all components of the optical system become critical.

This course provides the lithographer a basic knowledge of polarization and its application to high-NA imaging. After an introduction to the concept of polarization and the various ways it can be represented, both the benefits and limitations of its application to lithography are discussed. The polarizing effects of each component of the optical system are addressed, offering an understanding of their ultimate impact on imaging.

LEARNING OUTCOMES

This course will enable you to:

- demonstrate a fundamental understanding of the basic concepts of polarization
- compare the various mathematical representations of polarization and understand the physical mechanisms that cause changes in polarization state
- summarize the benefits and limitations of polarization control in high numerical aperture lens systems enabled by immersion lithography
- identify the impact that each tool component has on polarization state and its implication for imaging
- explain the current status and techniques of polarization implementation and metrology in the industry
- understand the concept of polarization aberrations and their various representations

INTENDED AUDIENCE

This course is intended for lithographers who want to understand polarization. Those who try to apply polarization for lithography application will find this course valuable. This course has no prerequisites.

INSTRUCTORS

Jongwook Kye has been involved in advanced optical lithography development for more than a decade. He has been worked on optical lens issues regarding lithography application.

Gregory McIntyre is completing a Ph.D. with Professor Andrew Neureuther at UC Berkeley. Much of his dissertation work has focused on various issues in polarization for optical lithography.

Course level: Intermediate

SC779 CEU .35 $270 / $310 USD
Monday 8:30 am to 12:30 pm

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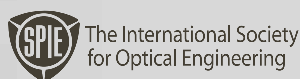

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Tuesday-Friday 19-22 September 2006

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6349-01, Session 1

Challenges and opportunities to keep lithography scaling on track

M. A. van den Brink, ASML Netherlands B.V. (Netherlands)

No abstract available

6349-02, Session 1

Mask Industry Assessment: 2006

G. V. Shelden, Shelden Consulting; P. Marmillion, SEMATECH, Inc.

Microelectronics industry leaders routinely name the cost and cycle time of mask technology and mask supply as top critical issues. A survey was created with support from SEMATECH and administered by SEMI North America to gather information about the mask industry as an objective assessment of its overall condition. The survey is designed with the input of semiconductor company mask technologists, merchant mask suppliers and industry equipment makers. This year's assessment is the fifth in the current series of annual reports. With continued industry support the report can be used as a baseline to gain perspective on the technical and business status of the mask and microelectronics industries. The report will continue to serve as a valuable reference to identify the strengths and opportunities of the mask industry. The results will be used to guide future investments on critical path issues. This year's survey is basically the same as the 2005 survey. Questions are grouped into categories: General Business Profile Information, Data Processing, Yields and Yield Loss Mechanisms, Delivery Times, Returns and Services, Operating Cost Factors, and Equipment Utilization. Within each category is a multitude of questions that create a detailed profile of both the business and technical status of the critical mask industry.

6349-03, Session 1

PMJ Best Paper: Comparative study of bi-layer attenuating phase-shifting masks for hyper-NA lithography

M. Yoshizawa, V. Philipsen, L. H. A. Leunissen, E. Hendrickx, R. M. Jonckheere, G. Vandenberghe, IMEC (Belgium); U. Buttgereit, H. W. Becker, SCHOTT Lithotec AG (Germany); C. Köpernik, M. Irmscher, Institut für Mikroelektronik Stuttgart (Germany)

No abstract available

6349-04, Session 1

EMLC Best Paper: A correlation for predicting film pulling velocity in immersion lithography

S. D. Schuetter, T. A. Shedd, K. Doxtator, G. F. Nellis, Univ. of Wisconsin/Madison; C. K. Van Peski, SEMATECH, Inc.

Immersion lithography seeks to extend the resolution of optical lithography by filling the gap between the final optical element and the wafer with a liquid characterized by a high index of refraction. There are several engineering obstacles associated with the insertion of the immersion fluid. One issue that has recently been identified is the deposition of the immersion liquid onto the wafer from the receding contact line during the scanning process; any residual liquid left on the wafer represents a potential source of defects. The process of residual liquid deposition is strongly dependent on the behavior of the receding three-phase contact line and this paper focuses on an experimental investigation of this behavior under conditions that are relevant to immersion lithography. Specifically, the static and dynamic contact angle and the critical velocity for liquid deposition are presented together with a semi-empirical correlation developed from these measurements. The correlation allows the film pulling velocity to be predicted for a given resist-coated surface using only a measurement of the static receding contact angle and knowledge of the fluid properties. This correlation represents a useful tool that can be used to approximately guide the development of resists for immersion systems as well as to evaluate alternative immersion fluid candidates in order to minimize film pulling and defects while maximizing throughput.

6349-05, Session 2

Chemical flare long-range proximity effects in photomask manufacturing with chemically amplified resists

D. B. Sullivan, IBM Corp.; Y. Okawa, K. Sugawara, Toppan Electronics; Z. Benes, IBM Corp.; J. Kotani, Toppan Electronics

As critical dimension uniformity requirements tighten for advanced technology nodes, it becomes increasingly important to characterize and correct for systematic sources of error in mask manufacturing. A long range proximity effect has been previously reported in the industry to occur in chemically amplified resists. This appears to be related to the develop process and we call this phenomenon chemical flare.

Several attempts to modulate this effect have been characterized and at least one develop nozzle modification has been found to reduce chemical flare by ~50%. In addition, develop time and surfactant have been evaluated as methods of minimizing chemical flare effects in ebeam lithography applications. Multiple positive and negative chemically amplified ebeam resists have been evaluated and compared for chemical flare including the impact of modulating the resist thickness.

6349-06, Session 2

PAB and PEB temperature gradient methodology for CAR optimization

T. H. Dam, A. T. Jamieson, M. Lu, K. Baik, Intel Corp.

CAR resist performance can be greatly influenced by PEB and PAB conditions. The difficulty with optimizing these conditions for photomask process is cost and time. In typical wafer CAR resist development, multiple wafer splits and skews can be rapidly processed with relatively low cost, whereas in photomask processing each ebeam-written mask with a set of DOE conditions can be expensive and time consuming to produce.

This paper discusses a novel mask design and testing methodology that allow for many combinations of PEB and PAB conditions to be evaluated with one mask. In brief, this methodology employs orthogonal PAB and PEB thermal gradients across a plate. Some thermal profile, darkloss, resist top down CD's, and cross section results will be shared and discussed.

6349-07, Session 2

An ultra-uniform, ultra-thin resist deposition process

B. J. Grenon, Grenon Consulting, Inc.; G. Picard, J. Schneider, Nanometrix (Canada)

Uniform deposition of photo and e-beam resists have consistently been challenging for photomask substrates. While quality coatings can be achieved by spin coating, the high quality demands for uniform coating to the edge of the mask substrate are becoming ever more important with larger field sizes and ever-increasing area requirements on the substrate.

This unique resist deposition process provides the capability to produce uniform defect-free films over the complete area of the mask substrate. Additionally, the process provides a cost-effective method by which small amounts of resist are used and little waste is generated.

6349-202, Session 2

The challenges and requirements of photomask resist and coat track for 32-nm technology and beyond

K. Baik, Intel Corp.

No abstract available

6349-10, Session 3

Controlling CD uniformity for 45-nm technology node applications

J. Plumhoff, S. Srinivasan, R. J. Westerman, D. J. Johnson, C. Constantine, Unaxis USA, Inc.

The ITRS roadmap indicates that significant improvements in photomask processing will be necessary to achieve the design goals of 45nm technology node masks. In the past, etch systems were designed to produce an etch signature that was as “flat” as possible to avoid introducing undesirable signatures in the final product. However, as error budgets are shrinking for all tools in the process line, the signatures produced by etch systems are used to compensate for some of the upstream CD issues. Process modifications have been used successfully in this fashion, but frequently process adjustment alone is not sufficient.

CD uniformity results from a complex interaction between the system and the sample. An etch system must be capable of adjusting radial, linear, and loading etch uniformity components to compensate for the specific needs of each sample. The adjustments should also be as independent of process as possible. Towards this end, experiments were conducted with various etch technologies to create specific, controllable etch signatures on demand without the need for hardware changes. Etch rate data collected from both quartz and binary chrome photomasks was used to verify performance of the uniformity adjustment technologies. CD uniformity data was also collected on binary chrome photomasks to further demonstrate the utility of these systems in reticle production.

6349-11, Session 3

Mask CD correction method using dry-etch process

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In this study, the method for achieving precise CD MTT (critical dimension mean to target) in manufacturing attenuated PSM (phase shift mask) is investigated. As the specification for photomask becomes tighter, more precise control of CD is required. There are several causes to result in CD MTT error. In general mask patterning process which is from blank material to dry etch, it is difficult to detect CD MTT error before final CD measurement and correct it. It is necessary to apply new process to mask production to correct CD error and control CD MTT precisely. Reducing number of factors which can have an effect on CD MTT and introducing reliable method to correct CD error are important to achieve accurate CD. For the correction of CD error, the reliability of CD in etch measurement step such as resist CD or Cr CD, effect on items related with CD like CD uniformity, iso-dense CD difference, etc and the possibility of defect generation should be considered and evaluated. In this method to correct CD MTT error, Cr CD is measured before MoSiN dry etch and corrective Cr dry etch using Cr CD information and MoSiN dry etch are performed. The rate of CD change in corrective Cr etch is found and necessary corrective Cr etch time is applied to CD correction process. The CD MTT error is canceled by corrective Cr dry etch step. Accurate CD control and significant increase in yield of CD MTT is achieved using this CD correction method.

6349-12, Session 3

The study of optical performance for quartz dry etching quality in ArF lithography

W. Ahn, SAMSUNG Electronics Co., Ltd. (South Korea)

Dry etching has become critical to manufacture the resolution enhancement technique (RET) mask in the ArF lithography. Among RET masks, alternating phase shift mask (PSM) and chrome-less phase lithography (CPL) mask require the formation of 180 degrees phase differences by quartz dry etching. There are many error factors, which can influence CD uniformities on mask and wafers, in Quartz dry etch step such as sidewall angle, phase MTT and uniformity, micro-trench, and morphology. Furthermore, quartz depth is hard to control because there is no stopping layer for quartz etching. Additionally, Pattern profile of Chrome layer is very important, Because Chrome profile affect sidewall angle for quartz. We have simulated and investigated to identify the influences of many error factors on RET. Consequently, we investigated characteristics of quartz dry etching process performance and the influences on resolution, which can be improved by dry etch parameters.

6349-201, Session 3

A novel process of etching EUV masks for future generation technology

B. Wu, A. Kumar, M. Chandrachood, I. M. Ibrahim, A. Sabharwal, Applied Materials PPC

Studies on pattern transfer of next generation lithographic (EUV) photomask were carried out. Based on current absorber layer material candidates, thermodynamic calculations were performed and plasma etch gas system and composition were investigated. The gas systems have advantages of all etch products in volatile condition to ensure the etch process and etch chamber clean. For etch CD bias challenge in EUV photomask etch, self-mask and corresponding gases and process methods were investigated, which makes anti-reflective (AR) sublayer of the absorber layer function as a hard mask for the bulk absorber layer beneath. It significantly reduces etch CD bias and improves pattern transfer fidelity. For common candidates of EUV mask absorber layers such as TaBO/TaBN and TaSiON/TaSi, reactive gas systems were proposed according to thermodynamic calculations with all products volatile. AR sub-layers, TaBO or TaSiON were etched in one gas composition with volatiles. Once the AR sub-layer is etched through, gas composition was changed so that the bulk absorber sub-layer beneath is etched with volatile products, but the AR sub-layer cannot be etched significantly due the nonvolatile products on it, i.e. a high etch selectivity between bulk and AR sub-layers. Excellent results in profiles, CD bias, CD uniformity, and underneath capping layer impact have been demonstrated.

6349-13, Session 4

Mask complexity reduction, quality assurance, and yield improvement through smart design

A. P. Balasinski, J. Cetin, Cypress Semiconductor Corp.

Is it maskmaker’s responsibility to help qualify design such that the product on silicon would perform as expected? Perhaps not as the first line of gate keeping, but as the last resort. Maskmakers often assume that design has the ultimate authority in optimizing and ensuring full functionality of the layout. After all, design has the tools and skills to simulate and verify the logical, electrical, and physical parameters of the product. How would the maskshop become capable of identifying the issues not found by design? Partial answer to this is in the tapeout procedure. True to this, many maskshops would only accept layout with full QA process completed and documented. It is the task of the responsible managers to ensure that there are no errors in the product design that can be found only on wafers. The maskmaking and manufacturing processes take too much time and money not to be careful about mistakes or errors. As part of verification procedure at design level, maskshops are developing tools to selectively check for OPC over critical areas such as MOSFET channels or contacts. However, such

checks may not be sufficient for highly sensitive analog circuits with enhanced model requirements for multiple types of devices. In addition to the well-advertised design-for-manufacturability and design-for-yield rule sets, analog devices such as the ones used to build wireless systems on chips (SoC), need additional quality procedures. These procedures, which we may call design-for-functionality and design-for-reliability, include rules for electromigration, hot carrier injection, power distribution, signal integrity, would come in several groups which would also impact mask making process. Comparing the subsequent technology generations and their respective product applications in the nodes from 500 down to 45 nm, the number of design rule types increased by about an order of magnitude. It is in everyone's best interest to ensure that all the new rules would be adequately covered by design verification procedures, with maskmakers sharing the responsibility. This may be especially important for the captive maskmakers which must not waste company resources on designs that fail on silicon. However, one can expect that similar qualification criteria would also phase in for independent mask vendors. First one of the new rule categories, with multiple types of verification procedures, is design-for-functionality. We have found that even with faithful pattern reproduction on wafer, a number of apparently similar design options can result in dramatically different circuit performance. One critical subset of rules would be related to device matching which impacts the gain of operational amplifiers. We will demonstrate how dummy pattern placement and extraction impacts signal path frequency. Another issue in RF analog design is that design may be compelled to use larger than minimum design rules. While this may sound like desired news to maskshops which can breathe more easily as design is filling the gap between the leading edge technology and advanced product requirements, it actually means tighter CD limits and less room for defects, proximity effects, and context sensitivity. In summary, new generations of SoC design would set up new challenges to design verification flow ending at mask shop, where the latter is expected to have a watchful eye.

6349-14, Session 4

Litho-friendly design (LfD) methodologies applied to library cells

R. März, K. Peter, S. Gröndahl, W. Maurer, Infineon Technologies AG (Germany)

During the last years, various DfM (Design for Manufacturability) concepts have been proposed and discussed. The contributions resolution enhancement technologies providing a good printability over the whole process window and their control by print image simulation (PW-ORC) form crucial aspects of DfM today. In addition, the layouters are increasingly involved in yield discussion to identify and remove yield issues imprinted in the drawn layout. Such a lithography-aware design data flow, which we call LfD (Litho friendly Design) will be a very important step towards a fully developed DfM environment.

During the last year, the tools of the leading EDA vendors providing efficient process window analysis and a scoring of lithography issues became productive. We report in this paper the implementation of a LfD design flow used for library cells at 90 and 65 nm. Specific aspects of LfD flow, like the availability of robust process models in early development stages are discussed as well as appropriate scorings of optical rule check results.

6349-15, Session 4

Integrated DFM framework for dynamic yield optimization

F. G. Pikus, Mentor Graphics Corp.

Design for manufacturability and yield optimization of modern integrated circuits presents significant challenges, primarily because a multitude of factors contribute to the manufacturing yield. These factors are often in conflict with each other. Common yield-enhancement techniques, such as via doubling, wire spreading, wire widening, grid placement, etc, compete for the limited area on the chip as well as timing budget. Furthermore, some of the factors contributing to yield loss are volatile: they change over time, due to process maturation, and vary from one manufacturing facility to another. A thorough yield analysis may require use of tools from multiple vendors, and even then some of the yield optimization criteria are not well known or cannot be determined within the constraints on design time or cost. On the other hand, it has been shown that a simplistic fix for a particular yield-loss problem can reduce the overall yield instead of increasing it. For example, aggressive via doubling can increase vulnerability to bridging and decrease the total yield.

We present a new methodology for a balanced yield-optimization and a new DFM framework which implements it. Our approach allows designers to dynamically balance multiple factors contributing to yield loss and quickly select optimal combination of DFM enhancements based on the current information about the IC layout, the manufacturing process, and known causes of failures. We bring together the information gained from layout analysis, layout-aware circuit analysis, resolution enhancement and optical proximity correction tools, parasitics extraction, timing estimates, and other analysis tools, to suggest the DFM solution which is optimized within the existing constraints on design time and available data. The framework allows us to integrate all available sources of yield information, characterize and compare proposed DFM solutions, and quickly adjust them when new data or new analysis tools become available.

Our framework also includes a flexible toolkit which allows designers to integrate multiple analysis and DFM tools. Using this toolkit, a process engineer can fine-tune DFM optimization for a particular design and process and provide the IC designer with a customized solution which quickly characterizes the manufacturability aspects of the design, identifies and classifies areas with the most opportunities for yield improvement, and suggests possible DFM solutions.

The proposed methodology replaces the ad-hoc approach to DFM which targets one yield loss cause at the expense of other factors with a comprehensive analysis of competing DFM techniques and trade-offs between them.

6349-16, Session 4

Application of Dosemapper for 65-nm gate CD control: strategies and results

N. N. Jeewakhan, N. Shamma, Cypress Semiconductor Corp.

Aggressive linewidth control requirements for leading-edge IC fabrication necessitate integration of novel techniques such as Dosemapper into the lithography process flow. Dosemapper is based on the simple concept that CD uniformity (CDU) can be improved through compensation of CD errors by using the scanner actuators. Specifically, the Dosemapper system allows for compensation of interfield and intrafield CD non-uniformity, based on the spatial distribution of in-line CD measurements or end-of-line electrical parameters for a stable process. This approach is supported by the fact that small variations of linewidth are correlated to exposure dose in a linear fashion. In this work we describe strategies for and results of the application of Dosemapper in a lithographic process for gate layer in a 65nm technology. In an initial attempt the 3-sigma distribution of the gate CD's were improved by over 40% from 4.2nm 2.4nm. Based on these and other results we will highlight the potential strengths and weaknesses of various Dosemapper strategies to ultimately improve device performance and die yield. For instance, we have learned that dose adjustments which are based on post-etch CD signature can lead to degradation of the lithography-based process window especially for 2-dimensional features due to high MEEF. Therefore, it is asserted that application of Dosemapper in a high-volume manufacturing process requires consideration of such rational tradeoffs as mentioned above. Since mask CD variation is another significant source of wafer CD error, relevant results showing compensation of mask CD errors by the Dosemapper system will be discussed. This has the potential to have a significant impact on manufacturability of photomasks for the 65nm node and beyond.

6349-148, Session 4

Fast dual-graph-based hot-spot detection

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As advanced technologies in wafer manufacturing push the patterning processes toward lower k1 sub-wavelength printing, the accelerating shift toward much smaller geometries in CMOS devices poses difficulties concerning lithography for mass production. In regard to optical lithography, the manufacturability is roughly defined by the k1 factor from the Rayleigh equation. Below 45nm CMOS technology node, even using a high-end optical exposure system such as immersion lithography with higher NA, k1 factor is lower than 0.35. Lower k1 could decrease patterning fidelity and result in generation of many hot spots, which are actual device patterns with relatively large CD and image errors with respect to the targets on wafers. Hot spots can be formed under a variety of conditions such as the original design being unfriendly to the RET that is applied, unanticipated pattern combinations in rule based OPC, or inaccuracies in model based OPC. When these hot spots fall on locations that is critical to the electrical performance of a device, the yield and device performance can be significantly degraded.

Park et al. proposed a rule-based hot spots detection method which generates look-up tables according to line and space parameters. However, the number of parameters for detection increases for complex pattern with reduced speed. Simulation-based approach has been a mainstream and been able to detect hot spots accurately. However, hot spots may change with different process conditions. Model generations corresponding to the process variation bring significant overhead in terms of test, measurement and parameter calibration.

In this paper, we first describe a novel detection algorithm for hot spots induced by lithographic uncertainty. Our goal is to fast detect all lithographic hot spots without significant accuracy degradation. The first step of the hot spot detection algorithm is to build a layout graph which reflects the pattern related CD variation. Given a layout L, the layout graph G consists of nodes which represent features, corner edges and proximity edges. A face in the layout graph includes several close features and the edges between them. Edge weight can be calculated from a traditional 2-D model or a look-up table. Then we use three-level hot spot detection: (1) Edge-level detection finds the hot spot caused by two close features or ¡°T-shaped¡± features; (2) Face-level detection finds the pattern related hot spots which include several close features; (3) Merged-face-level detection finds the hot spots with more complex patterns. To find the merged face which captures the pattern related hot spots, we propose to convert the layout into a planar graph. Then we construct its dual graph GD and sort the dual nodes according to their weights. We merge the sorted dual nodes (i.e., the faces in G) which share the same feature in sequence.

We have tested our flow on industry testcases. The experimental results show that our method is promising: for the metal layer with 17 hot spots detected by commercial ORC tools, our method can detect all of them while the runtime improvement is more than 50X.

6349-18, Session 5

Multi-layer resist system for 45-nm-node and beyond, part I

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Development of 45nm-node reticle will be driven by the innovation for resolution improvement. To improve the resolution, super thin resist on new chrome blanks for 65nm-node was released in 2004. For the next stage, the resist resolution has to be fundamentally improved.

Chemically amplified resist shows resolution degradation by interaction between chrome and resist. The interaction induces the excess footing in positive-tone CAR and the under-cutting in negative-tone CAR. BARC (bottom anti-reflective coating) is one of the ideas to prevent the interaction. However, BARC needs specific thickness for the prevention. It induces resist pattern degradation and CD bias during BARC etching process.

The bottom-insulating-layer (BIL) material has been developed. BIL was designed for dry-etching friendly, which means thin functional thickness with higher etch rate. The functional thickness is around 200A. The multi-layer resist system (CAR on BIL) can bring out 100% capability for resist resolution and no stress on dry-etching. Therefore, CD performance and pattern fidelity will be improved.

In this paper, BIL blanks performance on practical mask-making process, will be described, including defect point of view. Finally, the feasibility for 45nm-node reticle fabrication will be concluded.

6349-19, Session 5

Process window enhancement for 45-nm and 65-nm node using alterable transmission phase-shifting materials

H. W. Becker, M. Renno, U. Buttgereit, SCHOTT Lithotec AG (Germany); C. Köpernik, L. Nedelmann, M. Irmscher, Institut für Mikroelektronik Stuttgart (Germany); R. Birkner, A. M. Zibold, Carl Zeiss SMT GmbH (Germany)

Phase shift mask are playing an important role in lithography to print ever-decreasing pitches with sufficient large process window. Increased attention for advanced 193nm lithography is given to the influence of different Phase Shift Mask (PSM) materials with variable transmission. Different materials with varying transmission impact process windows which are important for the successful printability of the mask features. These effects on the lithography will be analyzed based on optical aerial image measurement tools for the 65nm and 45nm node.

SCHOTT has introduced a new attenuated PSM material consisting of a Tantalum layer topped by a Silica layer. This stack offers the advantage of independent adjustment of transmission and phase shift. The Ta layer thickness controls the transmission. Two mask material types for 6% standard and 30% high transmission have been investigated in this study. A 180° phase shift is achieved by adding an appropriate Silica layer. Alternatively, SiON has been used as the phase shifting material. On three different PSM stacks the impact of transmission and phase shift material on lithographic relevant parameters, especially on the process window has been evaluated. All stacks are topped with Schott's U60 chrome absorber.

The patterning process has been developed and performed by Institut f. Mikroelektronik Stuttgart (IMS Chips), using VSB E-beam writer Leica SB350, Steag Hamatech resist processing tools and an UNAXIS Gen 3 / 4 cluster for dry etching. It has been applied a four step process for patterning the different material stacks: (1) standard chrome etch stopping on the SiO2 or SiON layer, (2) SiO2 / SiON etching with a fluorine based chemistry and high selectivity to chrome hardmask and tantalum etch stop, (3) Ta etching with chlorine chemistry and high selectivity to quartz and chrome and (4) removing of chrome hardmask with the standard chrome etching process. This combination of etching processes allows perfect etch stops on every single layer and thereby guarantees remaining the outstanding phase and transmission uniformities of the material. A dense line resolution of sub 100 nm has been achieved.

After characterization of the processed mask pattern by CD and profile metrology the printability of the masks has been investigated. ZEISS AIMS™ tools were used to measure the mask features under scanner equivalent settings of numerical apertures NA 0.93 and NA 1.2. Through-focus measurements were made on both AIMS™ fab 193i with max NA of 0.93 as well as on the novel alpha tool of the upcoming AIMS™ 45-193i. The latter one is based on a complete new platform and capable of hyper NA emulation. Based on the AIMS™ results the different mask performances are analyzed in regards to lithographic relevant parameters such as CD variations, Bossung curves, process latitude and process window size.

6349-20, Session 5

Optical issues of thin organic pellicles in 45-nm and 32-nm immersion lithography

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The semiconductor industry will soon be putting >=1.07NA 193nm immersion lithography systems into production for the 45nm device node and in about three years will be putting >=1.30NA systems into production for the 32nm device node. For these very high NA systems, the maximum angle of light incident on a 4X reticle will reach ~16 degrees and ~20 degrees for the 45nm and 32nm nodes respectively. These angles can no longer be accurately approximated by an assumption of normal incidence. The optical diffraction and thin film effects of high incident angles on the wafer and on the photomask have been studied by many different authors. Extensive previous work has also investigated the impact of high angles upon hard (e.g., F-doped silica) thick (> 700um) pellicles for 157nm lithography. However, the interaction of these high incident angles with traditional thin (< 1um) organic pellicles has not been widely discussed in the literature [1].

In this paper we analyze the impact of traditional thin organic pellicles in the imaging plane for hyper-NA immersion lithography at the 45nm and 32nm nodes. The use of existing pellicles with hyper-NA imaging is shown via simulation and experiment to have a definite negative impact upon lithographic process windows and optical proximity correction (OPC) model accuracy. This is due to the traditional method of setting organic pellicle thickness to optimize normally incident light transmission intensity. Due to thin film interference effects with hyper-NA angles, this traditional pellicle optimization method will induce a loss of high spatial frequency (i.e., high transmitted angle) intensity which is similar in negative impact to a strong lens apodization effect. Therefore, using simulation we investigate different pellicle manufacturing options (e.g., multi-layer pellicle films) and OPC modeling options to reduce the high spatial frequency loss and its impact. We also propose the optimization of pellicle thickness for a non-normal incident angle and investigate the positive and negative effects this optimization will have upon process window and OPC of different feature types. Non-normal incident pellicle plane transmission optimization of hard thick pellicles has been previously shown to be beneficial to lithographic resolution [2].

References:

[1] Chris Progler. The optics of photomasks, from shadowy past to scattered future. Invited talk at SPIE Microlithography Conference 6154, Feb. 21, 2006.

[2] Bruce Smith, Houyoung Kang. Spatial frequency filtering in the pellicle plane. Proceedings of SPIE, Vol. 4000, 2001.

6349-21, Session 5

Solid immersion masks

M. J. Cangemi, IMEC (Belgium) and Photronics; L. H. A. Leunissen, V. Philipsen, IMEC (Belgium); D. Taylor, Photronics, Inc.

Towards hyper-NA lithography (50nm half pitch node and smaller) the mask induced polarization becomes significant. As the mask pitch decreases, higher diffraction orders transition from forward propagating to evanescent diffracted orders. Besides polarization effects related to the small pitches, the transmission of the diffraction orders also becomes important: the so-called Wood's Anomalies [1]. This effect is different for TE and TM polarized light, leading to mask induced polarization [2].

During normal operation, between the spacing of the absorber on the mask, air is present. If the index of refraction (n) of the diffraction pattern is increased above the air level (n=1.0), the pitch at which the transition higher order occurs is reduced resulting in an increased diffraction efficiency and a decrease of polarization effects. This can be accomplished by a deposition of a material after fabrication of the binary photo mask with n >1.0 (the extinction coefficient should be small to avoid transmission losses), creating a solid immersion of the photo mask. This additional coating serves to effectively lower the wavelength of the evanescent waves propagating across the grating surface. Note that the solid immersion material need not fill the entire region between the photo mask and the first lens element of the projection optics.

This paper explores the fabrication of solid immersion masks by depositing a transparent material on top of a patterned binary mask. The study will evaluate the diffraction efficiency and polarization effects by simulation using Solid-E 3.2.0.2 (Sigma-C) and measurements using an ellipsometer (Woollam VUV-VASE). Moreover, simulations will allow us to investigate the imaging performance of solid immersion masks towards hyper-NA lithography. A comparison between normal binary masks and solid immersion masks will be performed.

References:

[1] Lord Rayleigh, "On the Remarkable Case of Diffraction Spectra Described by Prof. Wood", Philosophical Magazine, July, 1907. [2] M.H. Bennett et al., "Experimental measurements of diffraction for periodic patterns by 193nm polarized radiation compared to rigorous EM simulations", Proc. of SPIE 5754, 599 (2005).

6349-22, Session 6

Contact hole CD and profile metrology of binary and phase-shift masks: effect of modeling strategies in application of scatterometery

K. M. Lee, M. Tavassoli, Intel Corp.; S. K. Yedur, Timbre Technologies, Inc.; K. Baik, Intel Corp.

Scatterometers are widely used for line/space or 2D structure measurements in both wafer and mask industries. This technology is now gaining more acceptance and is being applied 3D structures such as contacts and pads. Contact CDs and trench depth in photomasks are critical monitoring parameters in mask industry and are discussed here.

We are reporting contact CDs and profile results measured from targets from Binary, PSM, and Crless plates. The strategies of model creation such as using simple trapezoid versus more advanced shapes affect how well SWA and footings can be measured and reported from these structures. We are reporting CD and profile information obtained with Scatterometer, and then comparing CD SEM, AFM, and cross section SEM. Multiple different modeling configurations were used with different levels of complexity, and we report on optimum modeling strategy to obtain profile information from 3D structures. The relationship between the modeling strategy versus cross correlation between different parameters is discussed. CD linearity, uniformity, and other correlation parameters to the reference CD SEM tool are reported. Target CDs ranged from 60nm up to 600nm. Linearity R2 values are generally higher than .996, and CD uniformity reported from Scatterometry is 20~30% less than that from CD SEMs. This CD uniformity improvement is due to the fact that scatterometer beam samples dozens to hundreds of samples and 'averages' profile parameters, thus eliminating local effect such as line edge roughness. Contact depth are also measured and compared to AFM, in which the bias between the two tools are usually around 3nm or less.

Application of scatterometry method to mask contacts and pads leads to accurate and fast measurement of 3D profiles, and opens up possibility of in-line monitoring of profile information due to the higher runrate compared to traditional metrology tools.

6349-23, Session 6

Improved prediction of across chip linewidth variation (ACLV)

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Critical dimension (CD) metrology is an important process step within the wafer fab. Knowledge of the CD values at resist level provides a reliable mechanism for the prediction of device performance. Ultimately tolerances of device electrical performance drive the wafer linewidth specifications of the lithography group. Staying within this budget is influenced mainly by the scanner settings, resist process and photomask quality. At the 65nm node the ITRS roadmap calls for sub-3nm photomask CD uniformity to support a sub-3nm wafer level CD uniformity. Meeting these targets has proven to be a challenge. What can be inferred from these specifications is that photomask level CD performance is the direct contributer to wafer level CD performance. With respect to phase shift masks, criteria such as phase and transmission

control are also tightened with each technology node.

A comprehensive study is presented supporting the use of photomask aerial image emulation CD metrology to predict wafer level Across Chip Linewidth Variation (ACLV). Using the aerial image can provide more accurate wafer level prediction because it inherently includes all contributors of the real 3D mask topography to image formation such as the physical CD, phase, transmission, sidewall angle, and other material properties. Aerial images from different photomask types were captured to provide across chip CD values. Aerial image measurements were completed using an AIMS™fab193i with its through-pellicle data acquisition capability including the Global CDU Map™ software option for AIMS™ tools. The through-pellicle data acquisition capability is an essential prerequisite for capturing final CD data (after final clean and pellicle mounting) before the photomask ships or for requalification at the wafer fab. Data was also collected on these photomasks using a conventional CD-SEM metrology system with the pellicles removed. A comparison was then made to wafer prints demonstrating the benefit of using aerial image CD metrology.

6349-24, Session 6

Design-based mask metrology hot spot classification and recipe making through pattern recognition

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Current mask metrology is a mask based metrology, i.e., it focuses on the manufacturability and pattern fidelity of the mask pattern itself. This is not necessarily the ideal case considering the ultimate goal of the mask metrology is to ensure the functionality of the circuits on the waffer. The limitation lies in the fact that a mask is only one of the many layers that contributes to the functionality of the circuits on the wafer, when doing metrology on the mask, it is limited to that layer.

This paper investigates methods to enable design based mask metrology, with the goal to add the value of the mask metrology beyond the mask pattern fidelity check. The feasibility and challenges of such approach will be evaluated, and methods were developed to overcome the barriers.

Design intents are usually checked through rules which will create hot spots if violations are found. These hot spots are the critical dimensions in the sense that these CDs' impact to the circuit functionality is siginificant and would be suitable candidates for design based mask metrology. The diffuculty is the patterns of these hot spots are randown and unknown, specially the ones derived from interlayer rules. This creates major limitation to use these hot spots to create metrology measurement sites.

Conventional pattern recognition techniques usually involve one or more reference patterns to match to. And, it can be very expensive to attempt to do any pattern recognition with too many degrees of freedom. This paper proposes a technique that is developed to optimize the pattern recognition for the purpose of the mask metrology, with the goal to create measurement sites automatically. All these factors are considered into creating a metrology matrix which will then be used to optimize the pattern recognition process. This approach will weight both the design interests and metrology tool capability to create recipes that is directly reflects the design goal.

The paper will evaluate the feasibility of such approach, from design fidelity, success rate, and computing cost, etc. Also, it will compare the new approach to the conventional mask based metrology.

6349-25, Session 6

Determination of spatial CD signatures on photomasks

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The production process of photo-masks for memory devices is highly demanding since homogeneity of mask quality parameters plays a pivotal role in the mask performace. Spatially homogeneous mask designs - which are dominant on memory devices - should in the best case be transferred into a mask exhibiting the same homogeneous behavior. This means that the CD deviations from the mean should ideally bear no systematic signature but at most some random noise. However, many steps in the mask production process can introduce spatial correlations so that CD deviations are not only stochastically distributed over the mask but exhibit a pronounced signature. Thus, the determination and quantification of these deviations plays an important role in a) assessing the mask quality and b) driving process improvements that remove CD signatures.

The most common data analysis method for separating signatures from noise is to average over a number of samples. Unfortunately, due to the nature of mask manufacturing often there is only one sample available.

In this paper we propose the technique of Thin Plate Spline Smoothing for the determination and quantification of the CD signature of a given single mask. This analysis is complemented by two statistical tests which assess the fit quality by analyzing the residual for normality and correlations.

6349-26, Session 7

Reticle requalification and disposition of defects in a 193-nm wafer fab environment

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With each next generation technology node, mask shops and wafer fabs have to deal with an increasing number of even smaller defects on reticles. This is due to shrinking structure sizes on masks, more complicated, more complex mask manufacturing processes, and the use of the 193nm exposure wavelength in the manufacturing process that can accelerate contamination with progressing defects (crystal growth) on masks.

A new "Advanced Reticle Defect Disposition" (ARDD) process has been established. It uses STARlight systems for reticle inspection and defect binning, together with an aerial image measurement system (AIMS™ fab 193) for review and disposition of defects suspected of reducing wafer yield. The latest networked data connectivity between these systems allows for the exchange of alignment and defect images, as well as the updating of the inspection report. This speeds up the overall defect disposition through an integrated process thereby enabling the traceability of defect data.

The ARDD process was employed on various real life cases on production reticles in a 193nm wafer fab environment. The objective was to make the overall defect disposition process as efficient as possible, on the one hand, without compromising yield on the other. The total number of defects was reduced to lithographically relevant defects which then were sent to the actinic aerial image tool for enhanced disposition under stepper / scanner equivalent settings. Since printability depends on the illumination wavelength and the stepper settings, an actinic defect review tool based on aerial image technology with through-focus capability provides the only comprehensive defect printability strategy together with the defect inspection. The integration of the defect inspection and review technologies in this study demonstrates the overall effectiveness and economic benefits of employing this reticle requalification strategy.

6349-27, Session 7

Analysis of optical lithography capabilities of pixelized photomasks and spatial light modulators

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The models based on pixelized representation of the photomask have been employed by several authors in order to provide the systematic framework for design of photomask patterns resulting in images with desired optimal properties [1-3]. One possibility to directly implement such pixel-based optimal mask patterns arises in Optical Maskless Lithography (OML) [4].

In one implementation of OML, spatial light modulators (SLMs) are used instead of the photomask. Each SLM may have millions of pixels that can individually change their optical properties utilizing one or the other physical modulation principle (e.g. pistoning micro-mirror pixels or tilting micro-mirror pixels).

One important question, applicable to both SLMs used in OML and pixelized photomasks, is: how well is a particular pixel modulation principle suited to obtain the optimal image? We present the way to answer this question, derived from the methodology of OML rasterization algorithms described in [4]. The illustrating examples are presented for photomasks consisting of graytoning pixels, phase-varying pixels and the SLMs with tilting or pistoning micro-mirror pixels.

Based on this analysis, we present new examples demonstrating the concept and advantages of "truly maskless" optical maskless lithography [4].

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6349-28, Session 7

High-resolution mask inspection in advanced fab

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High resolution mask inspection in advanced wafer fabs is a necessity. Initial and progressive mask defect problem still remains an industry wide mask reliability issue. Defect incidences and its criticality vary significantly among the type of masks, technology node and layer, fab environment and mask usage. A usage and layer based qualification strategy for masks in production needs to be adopted in wafer fabs.

With the help of a high-resolution direct reticle inspection, early detection of critical and also non-critical defects at high capture rates is possible. A high-resolution inspection that is capable of providing necessary sensitivity to critical emerging defects (near edge) is very important in advanced nodes. At the same time, a way to disposition (make a go / no-go decision) on these defective masks is also very important. As the impact of these defects will depend on not only their size, but also on their transmission and MEEF, various defect types and characteristics have to be considered.

In this technical report the adoption of such a high-resolution mask inspection system in wafer fab production is presented and discussed. Data on this work will include inspection results from advanced masks, layer and product based inspection pixel assignment, defect disposition and overall wafer fab strategies in day-to-day production towards mask inspection.

6349-29, Session 7

Limitations of optical reticle inspection for 45-nm node and beyond

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Pushing the limits of optical lithography with immersion technology results in smaller feature sizes on the reticle. At the same time the k1-factor will be pushed in the region of the theoretical limit, e.g. the OPC structures on the reticle become very aggressive. For the mask shop it is essential to manufacture defect free masks. With decreasing feature sizes the minimum defect size, which needs to be found reliably, becomes smaller. Consequently optical inspection of masks for the 45nm node and below will be challenging.

In this paper the limits of existing KLA-inspection tools by systematic inspection of different structures without and with programmed defects were investigated. A test mask with isolated and dense lines/space patterns including programmed defects was manufactured, completely characterized by CD-SEM and inspected with state-of-the-art inspection system. AIMS(TM) measurements were used to evaluate the defect printing behavior. The analysis of the measurement data gives an input for requirements of reticle inspection of upcoming 45nm node and beyond.

6349-30, Session 7

Wafer fab mask qualification techniques and limitations

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Mask inspection and qualification is a must for wafer fabs to ensure and guarantee high and stable yields. Single defect events can easily cause a million dollar loss through a defect duplicating onto the wafer.

Several techniques and methods for mask qualification within a wafer fab are known but not all of them are neither used nor understood regarding their limitations. Increasing effort on existing tool platforms is necessary to detect the defects of interest which are at the limit of the tools specification - On the other hand next generation tools are very sensitive and therefore consume only a negligible amount of time for recipe optimization. Knowing the limits of each inspection tool helps to balance between effort and benefit.

Masks with programmed defects of 90nm and 65nm design rule were used in order to compare the different available inspection techniques. During the course of this technical work, the authors concentrate mainly on two inspection techniques. The first one inspects the reticle itself using KLA-Tencor's SLF27 (TeraSTAR) and SL536 (TeraScan) tools. As the reticle gets inspected itself this is the so called "direct" mask defect inspection. The second inspection technique discussed is the "indirect" mask defect inspection which consists of printing the pattern on a blank wafer and use KLA-Tencor's bright-field wafer inspection tool (2xxx series) to inspect the wafer. Data of this work will include description of the techniques, inspection results, defect maps, sensitivity analysis, effort estimation as well as limitations for both techniques for the used design rule.

6349-31, Session 8

Multipass VSB writing strategies for the 45-nm node and beyond

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Aggressive 193nm optical lithography solutions have in turn led to increasingly complex model-based OPC methodologies. This complexity married with the inevitable march of Moore's Law have produced a figure count explosion at the mask writer level. VSB beam manufacturers have tried to mollify the impact of this figure count explosion on the write time by the introduction of new technologies such as increased beam current density, faster DAC amplifiers and more efficient stage algorithms. Despite these efforts, mask manufacturers continue to explore ways of increasing writer throughput and available capacity. This paper explores the modulation of writing pass count and its impact on throughput and writing accuracy for two common VSB writer platforms. Specifically, local pattern placement, stitching, and CD uniformity will be correlated with writing pass count. Finally, tradeoffs between throughput and accuracy are discussed along with additional methods of reducing these errors.

6349-32, Session 8

Pattern density related CD corrections in mask making and their implications for model-based OPC at 45-nm node and beyond

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With the CD uniformity requirements becoming tighter with each new technology node, mask makers have to employ a wide range of corrections during the mask manufacturing process to meet the CD specifications - proximity effect correction, fogging effect correction, global etch loading effect correction, global process correction, etc. Most of these have a direct impact on the CD behavior of structures used by the wafer OPC modeling teams. With the ITRS roadmap quoting 1.5nm as a target specification for repeatability of such CD behavior for the 45nm node it is important to increase the awareness of the various correction methods among the OPC community, process integrators and people responsible for mask qualifications.

This paper discusses the various CD correction algorithms employed by mask manufacturers to meet the CD uniformity specifications and how the particular methods of correction impact the OPC integrity of any given mask.

6349-33, Session 8

Study of the beam blur and its effect on the future mask fabrication

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For the DRAM half pitch below 40nm, the required sub-resolution feature size is about to be 50nm, and the uniformity to be below 3nm for the mask fabrication. To achieve this requirement, the reduction of beam blur is necessary. On the mask patterning using 50keV electron beam, the beam blurring due to coulomb interaction and develop process is the main effect on the pattern image degradation and the limit of CD uniformity.

In this report, we present the effect of the beam blur induced by coulomb interaction and develop process. And we report the recent simulated and experimental results. Finally, we conclude that the reduction of beam blur can improve the mask quality and there is a compatible condition between the beam blur and the mask fabrication.

6349-34, Session 8

Improved photomask accuracy with a high-productivity DUV laser pattern generator

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A strategy for sub-100 nm technology nodes is to maximize the use of high-speed DUV laser pattern generators, reserving e-beam tools for the most critical photomask layers. With a 248 nm excimer laser and 0.82 NA projection optics, the Sigma7300 increased the application space of laser pattern generators. A programmable spatial light modulator (SLM) is imaged with partially coherent optics to compose the photomask pattern. Image profiles are enhanced with phase shifting in the pattern generator, and features below 200 nm are reliably printed.

The Sigma7500 extends this architecture with improvements to CD uniformity and placement accuracy, resulting from an error budget-based methodology. Among these improvements is a stiffer focus stage design with digital focus servos, resulting in improved focus stability. Tighter climate controls and improved dose control reduce drifts during mask patterning. As a result, global composite CD uniformity below 5 nm (3s) has been demonstrated, with placement accuracy below 8 nm (3s) across the mask.

Additional self-calibration methods have been developed to optimize and monitor system performance, reducing the need to print test plates. The SLM calibration camera is used to view programmed test patterns, making it possible to evaluate image metrics such as CD uniformity and line edge roughness. The camera can also be used to characterize image placement over the optical field.

The ProcessEqualizerTM function has been developed to correct long range CD errors arising from process effects on production photomasks. Mask data is sized in real time to compensate for pattern-dependent errors related to local pattern density, as well as for systematic pattern-independent errors. Corrections are made in the pixel domain in the advanced adjustments processor, which also performs global biasing, stamp distortion compensation and corner enhancement.

In the Sigma7500, the mask pattern is imaged with full addressability in each writing pass, providing the means of additionally improving write time by reducing the number of exposure passes. Photomask write time is generally under two hours in the 2-pass mode, compared to three hours with 4-pass writing.

With a through-the-lens alignment system and both grid matching and pattern matching capabilities, the tool is also suitable for 2nd layer patterning in advanced PSM applications. Improvements in alignment algorithms and writing accuracy have resulted in demonstrated layer-to-layer overlay below 15 nm (mean+3s).

6349-169, Poster Session

Metrics to assess fracture quality for variable shaped beam lithography

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Variable Shaped Beam (VSB) mask lithography systems (“write tools”) compose the mask pattern by the sequential exposure of discrete rectangular and triangular “shots”. Mask data preparation (MDP) software is used to decompose (“fracture”) the polygonal data supplied in GDS or OASIS stream formats into a set of basic trapezoidal shapes (“figures”). The figures are subsequently further divided into shots by the write tool. Due to the exposure sequence in VSB write tools the number of shots closely correlates with the required write time on the tool.

Since the critical feature size in advanced node patterns is typically less than the maximum shot size (determined by write tool hardware constraints) figures are often equivalent to shots since no further decomposition is necessary to expose the figures. This is also driven to some extent by the increasing complexity of Optical Proximity Compensation (OPC), which has the effect of breaking long, straight edges into short jogs. This results in an increased number of vertices that need to be considered during fracturing.

CD control for VSB write tools is somewhat dependent on the post-fracture figure layout. Shot linearity, shot size repeatability, and shot placement repeatability can affect CD control differently based on the figure layout. A simple example is the case of a critical feature composed of one vs. two figures in the critical axis. The constituent errors that affect CD control are different in these two cases.

During fracturing MDP software has to satisfy two potentially conflicting requirements: To reduce the number of shots required to compose the mask layout for write time optimization as well as to divide the layout polygons in a manner that has the least CD influence. Although an optimal polygon division may exist, MDP software uses simplified algorithms to meet compute time and resource limitation requirements. Furthermore these tools offer methods to influence the fracture results by prioritizing between write time optimization and CD control.

CD control requirements for advanced node masks are now in the low single digit nanometer range. The potential CD error contribution from poorly optimized fracture strategies can be a significant contributor to total CD error. In this paper we will show the impact of different fracture strategies on CD control. We will present a set of fracture quality metrics based on the impact on mask CD control and methods using EDA software to grade fracture strategies based on these fracture quality metrics.

We also discuss applications of this metric for fracture tool design and the implementation of different fracture strategies into mask manufac-

turing including examinations of the predictability of fracturing results. Finally, we will discuss the usage of existing information about the design (such as design intent) in conjunction with the proposed quality metrics to judge different fracture strategies.

6349-36, Session 9

Process window results using pitch decomposition at k1eff<0.20

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1. INTRODUCTION

The industry is approaching the challenges of features printing at */4, going to */6. Since lambda is now frozen at 193nm, none of this would be possible without strong RET. While immersion lithography is providing a push into hyper-NAs, parallel development of these strong Resolution Enhancement Techniques is needed, and one solution is Double Exposure Lithography.

2. ABSTRACT

In conventional IC processes, the smallest size of any features that can be created on a wafer is severely limited by the pitch of the processing system. A pitch is a combination of the width of a feature plus the spacing between features. A photolithographic process can make a narrow line by adjusting the threshold or dose, but not a smaller pitch. This paper discusses a method for decomposing the design to be printed into two or more exposures, each of which could go as low as the minimum pitch. Together, these multiple exposures print a design that could not be printed in one exposure alone. The effective k1-factor can be dropped below 0.2, while the individual image process in this double exposure remains >0.35.

This approach is a key enabler of printing mask features on wafers without requiring new manufacturing equipment and with minor changes to existing manufacturing processes. The approach also does not require restrictions on the design of the chip. This paper will present Wafer Results for the Double Exposure method using both dry and wet printing techniques.

6349-37, Session 9

32-nm node flash contact hole printing using double patterning, CPL mask, and hyper-NA immersion lithography with optimized illumination

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At k1>0.31, feasibility of patterning 45nm and 55nm node Flash contact hole mask (min. pitch 120nm) has been demonstrated both in simulation and on wafer using 6% attPSM with advanced OPC and optimized illumination on ArF hyper-NA (1.2) immersion lithography imaging platform. In a single exposure approach, a common process window ~0.15um at 6% EL can be achieved before additional DOE enhancement techniques such as focus scans are used. As we look forward to 32nm-node device manufacturing, k1 can be further reduced to below the limit of 0.25, using conventional patterning techniques on the same imaging platform. The extreme low-k1 renders the conventional patterning approaches such as single exposure with binary low-transmission phase shift masks completely incapable of manufacturing even with optimized illumination source and the latest imaging hardware.

In this work, we report our results on printing a 32nm (40nm target CD and 93nm min. pitch, therefore k1=0.24) node Flash contact hole layer using the double exposure and/or patterning technique (DPT), CPL mask and ArF hyper-NA immersion lithography imaging platform. We begin with model-based design pattern “splitting” which results in two component masks, therefore two separate exposure/patterning processes. To achieve sufficient baseline process latitude, we use CPL (100% transmitting phase shifted) mask. Illumination source optimization is performed for each mask for optimal imaging contrast in a double-BARC resist stack and key manufacturability requirements for the source shaping are fully taken into account during the optimizations. With the optimized source(s), model-based scattering bars (SB) and OPC (biasing) are implemented to achieve the optimal pattern fidelity in-focus and maximum process latitude as required for manufacturing.

Our results show that for this 32nm node, 93nm minimum pitch contact-hole pattern and using ASML XT:1700i at NA=1.0-1.2, both optimized illumination source and immersion lithography are the necessary starting point of the patterning process optimization. 6% attPSM is no longer sufficient as it produced much lower usable EL and DOF (<50nm), even after the design layer split. Using a CPL mask (100% transmission PSM in this case), using the optimized illumination source and before model-based SB and OPC, the worse-case DOF \@ 6% EL is >100nm, with excellent in-focus printing. This pre-OPC process performance is the same as (or better than) that was achieved for 45nm node patterning using the same imaging platform (see attached graphs). With model-based (IML™) SB placement and OPC (biasing), we expect to achieve >150nm common DOF process latitude, therefore making our approach a good candidate for extreme low-k1 manufacturing. Finally patterning the contact-hole layer is accomplished by exposing both masks, and depending on manufacturing considerations, pros and cons of double exposure and double patterning are discussed. Two customized polarizations are considered in the above simulations to demonstrate the polarization effects on imaging and process latitude for pattern-specific designs. Possible DOF enhancements will be demonstrated using the focus scan technique to show the feasibility of pushing common DOF to >200nm. These simulation results are compared with the wafer results, when available, using the available combination of illumination sources and with polarization.

6349-38, Session 9

Image degradation due to phase effects in chromeless phase lithography

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Chromeless Phase Lithography (CPL) is seen as a viable option for the 65nm node and beyond offering high resolution and small Mask Error Enhancement Factor. However, it was shown recently that at high NA CPL masks can exhibit large polarization and also phase effects. A well known phase effect occurring for CPL semi dense lines are through focus Bossung tilts.

However, another manifestation of phase effects for dense lines and spaces is a reduced contrast for a symmetrical off-axis illumination due to phase errors between 0th and 1st diffraction order. In this paper it is shown that these phase effects can lead to a significant contrast loss for dense structures smaller than 60nm half pitch. While also present for trench structures, the contrast reduction is more pronounced for mesa style structures. It is shown that an adjustment of etch depth can not compensate for these phase effects and hence recover an effective pi-phase shift. Furthermore, significant polarization effects are observed. As an example, the optimum mesa structure for TE polarization is shifted to small lines which are hard to fabricate.

For an experimental validation, a CPL mask containing dense lines and spaces was fabricated at the AMTC. Aerial images of structures were characterized with an AIMS 45i offering NA’s greater than 1 and linearly polarized illumination. Lines and spaces structures with pitches down to 100 nm with varying duty cycles were measured with TE, TM and unpolarized dipole illumination. Very good agreement between measurement and simulation confirmed the validity of theoretical predictions.

6349-39, Session 9

Imaging performance at 45-nm of various PSM technologies

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The accelerated development of immersion based lithography tools for the semiconductor industry requires a closer look at the photomask technology to be used with such tools. At a fixed numerical aperture, immersion lithography provides increased depth of focus over conventional 'dry' lithography. This benefit enables two roads to be taken by the lithography engineer: one of relaxing current RET applications at a set k1 and the other pushing k1 even lower using aggressive phase shift strategies and polarization illumination. Prior work has shown that the use of either high transmission attenuated material or chromeless phase lithography provide imaging advantages over traditional PSM's.

A comprehensive study of the imaging performance of various phase shift technologies is presented. The viability of using standard 6% MoSi EAPSM is compared to the use of High-T EAPSM and CPL strategies for the 45nm node. An alpha version of an AIMS™ 45-193i with NA of 0.93 with linear polarization is used to characterize the image in resist performance through-pitch and mask induced polarization effects. Full 3-dimensional vector simulation of identical features is exercised and compared to the AIMS™ latent image in resist results. Wafer prints from a polarization capable scanner are used as final validation of imaging performance. In addition measurements performed at NA of 1.2 will be discussed to assess the wafer printability under future lithographic settings.

6349-40, Session 10

Advanced non-disruptive manufacturing rule checks (MRC)

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With feature sizes getting smaller and more complex it is imperative that there be more efficient and effective ways to check designs for rule violations before the manufacturing stage. For designers this is referred to most often as DRC (Design Rule Check) and for the mask manufacturers this rule check is referred to as MRC, or Manufacturing (Mask) Rule Checks. To avoid the high cost of redesigns and large mask cycle times it is crucial that the manufacturability and the inspectability of the mask be verified.

Mask makers must be able to specify a wide range of parameters, enabling efficient detection of violations such as small figure widths (including long edge capability), jogs (as are often introduced by OPC), notches in figures, abutting figures and small separation between figures. This process should be integrated and automated to maximize productivity while minimizing variability. Consistent performance should be maintained regardless of the increase in mask complexity.

By operating on mask data, the rule checks are performed on the precise data to be printed, after all OPC and other corrections are applied. These rule checks can be performed on a wide variety of mask writer formats including those of all major toolmakers, avoiding time-consuming and inconvenient conversion between data formats.

This paper describes the new CATSTM (MDP) mask rule checking (MRC) software used to inspect mask layout patterns for rule violations using "DRC-Enabled" type functionality. Results will be presented for single, multi-layer, and jobdeck rule checking in both a stand-alone and automated mode running multithreading and distributed processing.

6349-41, Session 10

A generic method for the detection of electrically superfluous layout features

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"Sub-resolution assist features" (SRAFs) are a standard "resolution enhancement technique" (RET) to ensure the lithography process window of narrow lines for critical mask levels. Since placement rules for SRAFs commonly demand a fixed, constant separation from the edges of the main features to be assisted, small jogs and notches in the layout of the main features force an SRAF interruption. As a consequence, locally the process window is reduced. In addition, jogs and notches increase the data amount and may cause an increase of run time of "design rule check" (DRC), "optical proximity correction" (OPC), and "mask data preparation" (MDP). In most cases, these jogs and notches are completely unnecessary for the electrical functionality of the circuit and the design rule compliance of the layout. In order to detect such superfluous layout features and give the physical designer the opportunity to remove them, a new approach to design rule checking was developed. This approach is based on the decomposition of the layout of one mask level into its basic geometrical features (e.g., corners, line ends, junctions) and a subsequent classification of these features according to their topology under consideration of electrically related other mask levels (e.g., metal + via = contact pad). We describe the implementation of a generic DRC for the detection of jogs and notches using this approach and highlight the stability and ease of maintenance of this method.

6349-42, Session 10

Mask spec projection for wafer process optimization

L. Chen, P. E. Freiberger, Intel Corp.

Mask Spec has been playing ever-increasing role for wafer process optimization with Design rule tightening. It is very critical to define the proper spec and predict the room for continuous improvement with new mask-making processes in order to define cost ownership for high volume manufacturing. In this paper, key parameters for mask spec affecting wafer litho process window, including OPC performance will be discussed. Examples of how to derive key mask specification based on the feedback of customers will be examined. The mask CD targeting control and plate to plate CD variation reduction strategy will be discussed.

6349-43, Session 10

A memory efficient large mask data handling method using repetition

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The size of mask data is increasing beyond the limit that the current software and the hardware can handle. One of 512M DRAM mask data files was 29 GB in the GDSII format after the model-based OPC and the layer generation. The file size could be reduced to 1.7 GB by transforming into the OASIS format. Even though the file sizes can become small using the OASIS format, the memory usage of the mask data preparation software is not changed since the data structures are the same as before.

In the GDSII format, the repetition of shapes cannot be encoded. Inspired by the ideas in the OASIS format, we introduce a data structure that utilizes the repetition of mask data. Mask data is saved in the OASIS format and the repetition information of the OASIS formatted file is loaded onto memory as it is. The data structure is the basis for the mask data preparation operations such as region query, AND, XOR and so on. The concept could be applied to layout viewer and mask data comparison software. Especially, we enforced the mask data comparison software with the idea of relative coordinates to reduce the memory usage further since the software needs to load two files at the same time. The data structure with repetition has reduced the memory usage to between 2 and 22 times less than the method that keeps the coordinate and attributes of each shape individually. The file loading time and the file writing time have improved 4~73 times and 1.5~14 times, respectively.

6349-44, Session 11

Sensitivity of VT5 model toward process and modeling parameters

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The quality of model-based OPC correction depends strongly on how the model is calibrated in order to generate a resist image as close to the target layer as possible. As the k1 process factor decreases and design complexity increases, the correction accuracy and the model stability become more important. It is also assumed that the stability of one model can be tested when its response to a small variation in one or several parameters is small. In order to quantify this, the small-variation method has been tested on a variable threshold based model (VT5) initially optimized for the 65nm node using measurements done with a test pattern mask. This method consists of introducing small variations to one input model parameter and analysing the induced effects on the simulated edge placement error (EPE).

In this paper, we study the impact of small changes in the optical and resist parameters (beamfocus, inner and outer sigmas, NA, resist thickness) on VT5-based model stability. And then, we quantify the sensitivity of the model towards each parameter shift. We also study the effects of modeling parameters (kernel count, eigenvalue, optical diameter) on the resulting simulated EPE. This kind of study allows us to detect coverage or process window problems.

The process and modeling parameters have been modified one by one. The ranges of variations correspond to those observed during a typical experiment. Then the difference in simulated EPEs between the reference model and the modified one has been calculated. Simulations show that the loss in model accuracy is essentially caused by changes in beamfocus, outer sigma and NA and lower values of optical diameter and kernel count and higher eigenvalues. Model results agree well with a testcase layout.

6349-45, Session 11

Imaging behavior of high-transmission attenuating phase-shift mask films

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The properties of phase shifting attenuator films are quantified in a variety of ways. Transverse dimensions are measured by optical microscopes or scanning electron microscopes. Vertical dimension and profiles are measured by atomic force microscopes or indirectly by optical scatterometry. The complex refractive index of an attenuator film can be characterized by ellipsometry or by spectroscopic analysis of reflected and transmitted light. Transmission and phase measurements can be made with optical interferometric techniques. Data acquired in these ways can be used as inputs to simulation programs to model the image forming characteristics of the films. For simplicity and speed of calculation, the simulation programs typically use a thin-mask approximation, in which the vertical absorber geometry is ignored and the phase shifting attenuator regions are characterized only by their transmission, phase shift, and two-dimensional geometric shapes. Inclusion of the full three-dimensional profile and complex refractive index of the absorber can be done, but at the cost of greatly increased calculation time and a loss of the simplicity of understanding afforded by the thin-mask model. For example, the thin-mask model assumes that every geometrical feature etched into a given attenuator film will have the same phase and transmission properties. Comparison of thin-mask modeling results with the full three dimensional model shows that this assumption is not true. The effective dimensional bias, phase, transmission, and defocus are strong functions of the feature size, pitch, and complex refractive index of the film. Three dimensional simulations were run for several commercial and developmental high-transmission phase-shifting attenuator films. The effective phase, transmission, and dimensional printing bias were calculated as a function of pitch for each film. Surprising differences were found in the results for the various film types. Masks were built using several of the films and aerial image measurements were compared to the simulation results.

6349-46, Session 11

Optical properties of alternating phase-shifting masks

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The 2005 edition of the International Technology Roadmap for Semiconductors specifies that phase errors of alternating phase-shifting masks (APSM) should approach 1 degree by 2008. This specification is reasonably motivated by the desire to keep imaging effects of mask errors below those of aberrations of projection optics, but it implies a questionable assumption that the phase of a feature is a well-defined quantity. Variations of both phase and amplitude across apertures are significant. Although one can define a measure such as the phase of the integral of the amplitude of the electric field over an aperture, this suffers from several drawbacks. Spatial variation of phase, which this measure does not capture, affects images significantly compared to lithographic tolerances. Second, in addition to variables we expect mask manufacturers to control, such as trench depths, sidewall slopes, and bottom-surface flatness, phase also depends on polarization, illumination angle, widths of apertures, and proximity of other features. Dependences of phase and amplitudes on these variables are not easily separable. We have applied Fourier-modal and finite-difference time-domain field calculations to quantify dependence of APSM properties on polarization, pitch, and aperture width. Effects of these variables are large compared to the desired tolerance of one or two degrees. Some of these difficulties vanish if, instead of attempting to define a measure of phase for a single aperture, we measure phases in the far-field diffraction patterns of photomasks. These are more useful because of their direct relation to image quality, and they provide important information about trench shapes to assist mask process control.

Modifying the simple Kirchhoff model of APSM imaging by introducing an effective phase explains many important behaviors, but misses others that become significant as we reduce widths of absorbers separating apertures. For symmetric patterns with alternating phases, the APSM balance condition reduces to selecting trench depths and aperture widths that minimize energy diffracted into zero-order. As shown here, the trench depth that produces this null condition depends on pitch, the ratio of widths of alternating apertures, illumination angle, and polarization. Consequently, the desired depth corresponding to the null condition varies with pattern dimensions and illumination conditions. Because it is not practical to manufacture a mask with multiple depths, this may impose restrictions on layout rules for patterning with APSM. Furthermore, we achieve the null condition only for zero-order light. Other diffraction orders that vanish in the Kirchhoff approximation are present. The consequences include reduced depth of focus and complication of the solution to optical proximity correction.

6349-47, Session 11

Optimization of process window simulations for litho friendly design framework

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Cutting edge technology node manufacturers are always researching how to increase yield while still optimally using silicon wafer area, this way these technologies will appeal more to designers. Many problems arise with such requirements, most important is the failure of plain layout geometric checks to capture yield limiting features in designs, if these features are recognized at an early stage of design, it can save a lot of efforts at the fabrication end. A new trend of verification is to couple geometric checks with lithography simulations at the designer space.

A lithography process has critical parameters that control the quality of its resulting output. Unfortunately some of these parameters can not be kept constant during the exposure process, and the variability of these parameters should be taken into consideration during the lithography simulations, and the lithography simulations are performed multiple times with these variables set at the different values they can have during the actual process. This significantly affects the runtime for verification.

In this paper the authors are presenting a methodology to carefully select only needed values for varying lithography parameters; that would capture the process variations and improve runtime due to reduced simulations. The selected values will depend on the desired variation for each parameter considered in the simulations. It is known that by making a design more robust to lithographic variability (more regular) ,the more consistent the parametric behavior of the devices will be. However there is ample debate about what this regularity means in terms of area penalty and design flexibility. The objective of this study is to accelerate the qualification of different design techniques. Results of different designs through different variations are presented to show the impact of large variations on circuit performance.

6349-48, Session 11

Model calibration using simulation-based full-chip verification tool

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High quality process model calibration becomes more critical for optical proximity correction/resolution enhancement techniques (OPC/RET) and their verification flow at extremely low k1 processes. This is because a very tight Critical Dimension (CD) prediction control is required at the CD measurement points. The reliability of the contour prediction of 2D features depends on a highly quality process model calibration. Since there are empirical components in statistically calibrated models for OPC/RET in full-chip layout, the coverage of test pattern types and sizes, and empirical data points are crucial to get accurate and reliable calibrated model. This requires a cumbersome iteration of model recalibration process when the actual full-chip layout has certain types of pattern features that the calibrated model does not cover well.

Simulation based full-chip verification has been used for various applications such as mask sign-off decision, OPC/RET recipe qualification and lithography process development. In this study, we will introduce the model calibration flow considering lithographic patterning behavior of actual full-chip layout using lithography simulation based full-chip verification tool. The cases will include both nominal process modeling and process window modeling, comparing the typical model calibration flow and the modeling flow with full-chip verification tool. The study will highlight the importance of model calibration considering the full chip layout instead of the traditional model calibration methodology which uses a small test pattern for 65nm process nodes and beyond.

6349-49, Session 12

Impact of AFM scan artifacts on photolithographic simulation

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This work represents one in a series of ongoing papers demonstrating the potential utility of integrating advanced photolithographic simulation software into a mask repair tool to provide immediate defect or repair printability feedback. The equipment used here is an AFM-technology based nanomachining photomask repair tool where the high-accuracy AFM surface topography data is fed directly into software applying rigorous solutions to Maxwell's equations. The nature of these systems allows for process endpoint printability evaluation, not restricted by the optical limitations of any given apparatus, of any micro to nano-scale region of the mask concurrent with the normal defect repair process. However, known AFM scan artifacts can impact the accuracy and stability of the photolithographic simulation results, especially for mask or pattern types which have not been previously studied by the user. The relevant sources of these artifacts are identified and improvements in the AFM operation are discussed which could minimize them. The quantitative relationships between the various artifact measures and their corresponding effects on various simulation results (including relative transmission and CD) are examined for both AIMS™ aerial imaging and wafer print. From this examination, error baselines are established and software, as well as model setup, optimizations are proposed.

6349-50, Session 12

Advanced photomask repair technology for 65-nm lithography

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Repair technology for 65nm generation photomasks requires achieving more accurate shape reconstruction and higher transmittance. At BACUS 2005, we reported that FIB etching process with low acceleration voltage provides higher transmittance than that with high acceleration voltage. The objective of the present study is to evaluate the actual repair performance with low acceleration voltage. Imaging impact, edge placement accuracy, minimum repairable size and process reliability were evaluated. In conclusion, we confirmed the FIB repair system with low acceleration voltage is applicable to 65nm generation photomasks. Further study of repair performance of the system is under way. The results from our latest research will be reported in the presentation.

6349-51, Session 12

New application results from advanced review and repair tool-kit for 45-nm node masks and beyond

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The continuing decrease of feature sizes in conjunction with yield-driven costs for current high-end photomasks has resulted in an increased focus on defect printability, mask repair, repair validation and repair cycle times. The increasing complexity of future generations of photomasks and their projections of the costs emphasize the relevance of a shortened and closed mask repair cycle even more.

Clearly, a viable repair methodology includes options for:

- pre-repair defect printability analysis with actinic optical scanner emulation
- process choices for mask type (binary, PSM, EUV, others)
- repair technology choices with respect to defect sizes and defect types
- post-repair printability assessment for repair verification.

Such repair methodology enables a cost effective and safe repair cycle to enhance the production yield and significantly reduce production costs for complete mask sets.

Within Carl Zeiss SMT a concerted development effort has succeeded in developing a novel mask review and repair tool-kit capable in achieving the above described methodology for all types of advanced masks, such as quartz binary masks, phase shift masks, EUV masks and S-FIL imprint templates. The individual tools and their options for repair and printability assessment that make up this tool-kit are described in the paper with respect to mask sets for the ITRS 45nm node specifications.

Pre- and post-repair images and printability assessments under stepper/ scanner specific illumination and imaging settings will be shown for a variety of defect types, such as intrusions, extrusions, pin-dots and extended defects.

Small defect repairs obtained with the MeRiTTM electron-beam based repair solution will be discussed against the background of the ultra high resolution and accuracy features that have been demonstrated on early 45nm node masks.

Pre- and post-repair assessments have been performed with the AIMSTM 45-193i and the resulting data will be discussed. In the printability discussion a strong focus will be on new effects anticipated in conjunction with the employed lithography schemes. Namely polarization effects from imaging and their relevance for defect dispositioning and repair validation will be described. The way of including these effects in the overall mask qualification and repair process will be outlined.

Brief overviews of the physical tool platforms will be presented, aspects of linking those tools' data path in order to achieve a high degree of automation and short cycle time will be shown. Repeatability, resolution and the speed of the repair cycles in a production environment are

discussed and performance parameters of repairs are outlined. An outlook against the ITRS requirements and the extendibility of the presented solution to further technology nodes will be provided in the summary.

6349-52, Session 12

Mask repair using layout-based pattern copy for the 65-nm node and beyond

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Recent advances in mask repair technology have slowed the projected cost explosion in mask production. As we progress towards the 45nm node, electron-beam induced deposition and etching has proven to be the most likely candidate capable of meeting the stringent repair specifications. This technology employs a method frequently called “pattern copy”, which derives the repair structure by comparing a high-resolution image of the defective area with the same image of a non-defective area. The repair shape is generated as the difference of these two images, and adjusted for processing purposes.

Traditionally, the pattern copy reference image is taken from the mask under repair. For this method to work, a suitable area containing a non-defective feature, identical to the defective feature, has to be identified on the mask and imaged. In general, this works well, however there are several drawbacks. For one, all the inaccuracies of the reference feature, like line edge roughness (LER), CD error, and imaging artifacts will be transferred to the repaired spot. Secondly, a slight variation from the target size of the scan field is not noticed and leads to additional CD error after repair. Furthermore, logic designs make it hard to find identical reference areas, especially for larger defects.

To overcome these drawbacks, we have developed layout based pattern copy (“die-to-database”). In this case, the reference is generated using information taken from the original mask design file. This is the file which was used to write the mask in the first place, and it contains the exact reference information we need to perform a pattern copy step. We create an image of the features inside the applicable field of view, and render this image according to a specified set of criteria, with the aim to make it look exactly like the image taken from the mask. The rendering step is necessary to emulate and compensate the basic characteristics of mask writer, manufacturing process, and image formation in our e-beam tool. The pattern copy process then continues as usual, only with the “ideal” reference image instead of the “real” reference image from the mask. As a result, we achieve a reduction in the CD error of repaired features, with the side benefit of greatly improved work flow, since the reference is automatically generated and aligned to the defect.

In this paper we compare mask repair using conventional pattern copy (reference taken from the mask) to layout based pattern copy, and demonstrate the overall improvement in repair quality. This is manifested in reduced CD variation of repaired features, and verified by CD-SEM as well as AIMS™ measurements. We also highlight the improvements in work flow, and show the potential of further automation in the repair process.

6349-53, Session 13

A new model of haze generation and storage-life-time estimation for mask

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Recently it has been reported that there are some photomasks with haze issue by radiation of much lower accumulate dosage than that on most of other masks. These photomasks are regarded as a serious problem for wafer production control, because it is difficult to control mask usage without haze issue by using accumulate dosage on masks as a parameter. Some haze mechanisms have been reported, however it is difficult to explain the root cause of the low dosage haze issue for the previous mechanisms. In this paper, we will report a new haze mechanism from results of the ArF test bench. For the new mechanism, the total amount of sulfate ion on mask, not only mask manufacturing line origin but also wafer fab’s mask storage environment origin, was found to play an important roll for haze occurrence. In detail, there is a threshold for haze occurrence as a function of amount of sulfate ion on masks, and we have found that the total ion amount plays a more important role in mask lifetime than the accumulate dosage. Furthermore, from the new mechanism, we will estimate storage life time for masks and also propose a mask storage strategy in order to use our masks for long time stably.

6349-54, Session 13

Real-time monitoring based on comprehensive analysis

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The understanding of the conditions that create haze defects is very essential for the future development of haze-free cleaning processes for 193 nm lithography. The industry has been using various analysis tools to investigate contributions to haze defect growth and chemical components of defects. For example, IC-MS is used for the examination of cleaning residues from photomask surface and TOF-SIMS for the direct surface analysis of the photomask. However, real time monitoring of mask surface during exposure has not been well established mostly because it is very hard to analyze chemical contaminants on the glass surface properly.

We have proposed a method to analyze the space trapped between the pellicle film and the mask surface that creates a highly reactive environment, which has the potential to be utilized as a real-time monitoring of the haze defects. This environment is believed to trigger photochemical reaction providing the opportunity for haze crystal growth, which results in the formation of killer (printable) defects on the mask. In this paper, we further perform chemical analysis of the gaseous environment and the mask surface after haze defects are formed. We believe that the analysis of the gaseous environment of the trapped space along with that of the mask surface could provide important clues to the characterization of haze contributions. This fundamental study will help the invention of reliable real-time monitoring methodology for haze-free cleaning processes.

6349-107, Session 13

Sulfur-free cleaning strategy for advanced mask manufacturing

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Existing cleaning technology using sulfuric acid based chemistry has served the mask industry quite well over the years. However, the existence of residue on the mask surface is becoming more and more of a problem at the high energy wavelengths used in steppers for wafer manufacturing. This is evident by the emergence of sub-pellicle defect growth and backside hazing issues. A large source of residual contamination on the surface of the masks is from the manufacturing process, particularly the cleaning portion involving sulfuric acid. Cleaning strategies can be developed that eliminate the use of sulfuric acid in the cleaning process for advanced photomasks and alternative processes can be used for cleaning the masks at various stages of the manufacturing process. Implementation of these new technologies into manufacturing will be discussed as will the resulting improvements, advantages, and disadvantages over pre-existing mask cleaning processes.

6349-57, Session 14

Simulation of critical dimension and profile metrology based on scatterometry method

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As the on-wafer transistor sizes shrink, and gate nodes reduce below 90 nm, it is becoming very important to precisely measure and control the critical dimension (CD) on the mask. Phase shift technology for masks is essential for decreasing of the feature size, therefore CD and profile metrology on the phase shifting materials becomes critical. Scatterometry provides fast and nondestructive method of profile and CD measurements

In this paper the conditions of determining of profile and CD measurement are analyzed. In the real experiment scattered spectrum from structure with unknown profile is measured. Before experiment the library of spectra is generated. Spectra in the library correspond to structures with various parameters (such us thickness, CD, sidewall angle, etc.). For calculation of this library rigorous coupled-wave analysis (RCWA) was used. This method allows us to get precise solution of Maxwell equations and find directly amplitude of zero diffraction order which is measured in the experiment. To determine the possibility of measurement of sidewall angle various spectra with different sidewall angle value were calculated. Calculated spectrum is changed by adding or deduction of random value. The randomly changed spectrum is compared with spectra in the library in order to find spectrum with best fit. Therefore sidewall angle and CD can be determined. Precision, possibility and maximum allowed error in the spectra measurements is obtained. Moreover, influence of polarization of incident light on precision of extracted results was found.

6349-58, Session 14

Segmentation-assisted edge extraction algorithms for SEM images

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Photomask inspection requires a combination of high resolution and high throughput. Scanning electron microscopy (SEM) has excellent resolution but at high throughput yields noisy images. Hence we are developing algorithms for extracting pattern information from noisy SEM images.

One big challenge in processing SEM images is edge extraction. SEM images have their own characteristics so many existing edge extraction algorithms based on gradient signal analysis do not work well in that they either yield strong signal for non-edge areas or yield weak signal for true edge areas. We describe several new edge extraction algorithms targeting noisy SEM images. The essence of these new algorithms is analyzing the “ridge” signal, i.e., the bright stripes.

We first propose edge extraction based on image segmentation. Image segmentation, which is mostly used in image content analysis, is defined as the partition of a digital image into multiple regions (sets of pixels) so that the objects of interest are separated from the background. In our approach, we adapt image segmentation to edge extraction. In particular, we apply a fast segmentation algorithm to separate the bright area from the dark area, and use the difference of average pixel values as the “ridge” signal. The advantage of this approach is that no assumption on the edge shape is involved and the computational complexity is low.

A second algorithm is based on second-order polynomial regression. Based on the observation that the pixel values around edges in SEM images behave approximately as second-order polynomial functions of coordinates, we compute the “ridge” signal using the coefficients of such polynomial functions obtained from regression. This algorithm generally yields very accurate estimation of the edge locations, especially for straight edges.

In the approach based on second-order polynomial regression, it is implicitly assumed that the edge is (approximately) straight. We thus propose a further improvement on this algorithm and assume that edge shapes can be well approximated by second-order curves, even at sharp turns. This approximation leads to a fourth-order polynomial regression with a slightly higher computational complexity.

Finally, we propose a hybrid algorithm combining the segmentation approach and the polynomial regression approach, yielding a “segmentation-assisted” algorithm that incorporates the advantages of both approaches. Simulation on a wide range of SEM image types yields quite satisfactory results, even for very noisy images. We will present detailed algorithm flows and demonstrate extraction results from real images.

6349-59, Session 14

Analysis of the Leica LMS IPRO3 performance

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In the current mask makers world the most advanced reticles are manufactured in a photo-lithographic way. The customers electrical circuit layout is split into several layers, which are written on separate resist coated blanks. After developing the photo-resist the masks can finally patterned by different kind of etch process steps. Keeping in mind, that recent complex circuits involves up to 40 different reticles (layers), which has to be aligned to each other properly in the wafer fab, one can imagine that the establishment of a stable coordinate system is one of the most important tasks. As a mask shop having customers who might mix reticles from different mask suppliers one also has to focus on providing an euclidean coordinate system as the most common used one.

As a consequence we are heavily committed to establish the best possible euclidean coordinate system in our mask shop in measuring coordinates with the most advanced tool in the market, the Leica LMS IPRO3, and trying to apply elaborate coordinate correction algorithms in order to meet this target as close as possible. This ensures best layer to layer matching for our customers.

In this publication we will present an analysis of the Leica LMS IPRO3 capability. We are using the statistical method of “analysis of variances” (ANOVA) in order to quantify different measurement error contributors. In our case we separate short-term, long-term, orientation dependant and tool matching error components. We end with a determination of the total coordinate measurement error.

Whereas the short-term repeatability and long-term reproducibility is more or less given by the tool set up and physical facts, the orientation dependant part is a result of a software correction algorithm. Most commonly different orientation measurements are taken into account, forcing that the software back-rotated measurements has to fit the zero degree ones. After applying the Leica’s build in correction we check measurements on different reticles for systematic residual grid distortions. For that we classify different kinds of distortions and discuss how further accuracy improvements could be implemented in the existing tools and future tools.

6349-60, Session 14

CD measurement evaluation on periodic patterns between optic tools and CD-SEM

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As feature size is shrinking and MEEF (Mask error enhancement factor) is increasing, CD measurement accuracy is more important, and CD SEM is widely used to replace optic tools because of their resolution. But CD-SEM is not representing the effect of Cr profile or transmittance of light which is transferred to wafer. Recently, new OCD (optic CD) tool which use spectroscopic ellipsometer is introduced to compensate the demerit of SEM of low through-put and reflected surface information of mask. This OCD tool can be used only on periodic pattern like DRAM. But this OCD tool must be calibrated on each pattern type and shapes. This calibration is the barrier to use this OCD to mask process.

In this paper, new optical CD measurement method will be introduced which use conventional optic microscope of transmitted and reflected light with high resolution lens of DUV on periodic patterns. And CD measurement results by optic CD and CD-SEM will be compared.

6349-61, Session 14

Fast nondestructive optical measurements of critical dimension uniformity and linearity on AEI and ASI phase-shift masks

A. Gray, Univ. of California/Davis; J. C. Lam, n&k Technology, Inc.

The fabrication of a production-worthy phase shift mask requires, among other things, excellent uniformity of critical dimensions (trench width and depth) and optical properties of the phase shift material (MoSi). Traditionally, CD-SEM has been the instrument of choice for the measurement of width; AFP (Atomic Force Profilometer) or conventional profilometer for the measurement of depth; and Interferometer for the measurement of phase shift and transmittance of the phase shift material. We present an innovative optical metrology solution based on broadband reflectometry, covering a wavelength range from 190 to 1000 nm, in one nanometer intervals. The analysis is performed using Forouhi-Bloomer dispersion equations, in conjunctions with Rigorous Coupled Wave Analysis (RCWA). The method provides accurate and repeatable results for critical dimensions, thickness, and optical properties (n and k spectra from 190 - 1000 nm) for all materials present in the structure.

In the current study, the method described above was used to examine photomasks at two stages of mask manufacturing process: After Etch Inspection (AEI) and After Strip Inspection (ASI). The results were compared with the measurements taken on the same samples using conventional CD-SEM. Two comparison studies were conducted - global CD uniformity and CD linearity. The CD linearity study demonstrated excellent correlation between the values of grating line width obtained using this new optical reflectometry approach and a CD-SEM for the grating structures of two pitches (760 nm and 1120 nm) and two orientations (perpendicular and parallel to the plane of incidence). The global CD uniformity study revealed that this presented reflectometry method can be used to produce CD uniformity maps which demonstrate excellent correlation with the results obtained using a conventional CD-SEM. The advantages of the optical method are high throughput, non-destructive nature of the measurements and capability to measure a wider variety of structures pertinent to the photomask manufacturing process.

6349-62, Session 15

Extension of 193-nm dry lithography to 45-nm half-pitch node: double exposure and double processing technique

A. M. Biswas, J. A. Hiserote, J. Li, L. S. Melvin III, Synopsys, Inc.

Immersion lithography and multiple exposure techniques are the most promising methods to extend lithography manufacturing to the 45nm node. Although immersion lithography has attracted much attention recently as a promising optical lithography extension, it will not solve all the problems at the 45-nm node. The ‘dry’ option, (i.e. double exposure/etch) which can be realized with standard processing practice, will extend 193-nm lithography to the end of the current industry roadmap. Double exposure/etch lithography is expensive in terms of cost, throughput time, and overlay registration accuracy. However, it is less challenging compared to other possible alternatives and has the ability to break through the k1 barrier (0.25). This process, in combination with attenuated PSM (att-PSM) mask, is a good imaging solution that can reach, and most likely go beyond, the 45nm node. Mask making requirements in a double exposure scheme will be reduced significantly. This can be appreciated by the fact that the separation of tightly-pitched mask into two less demanding pitch patterns will reduce the stringent specifications for each mask. In this study, modeling of double exposure lithography (DEL) with att-PSM masks to target 45nm node (k1~0.2) is described. In addition, mask separation and implementation issues of optical proximity corrections (OPCs) to improve process window will be studied. Significant improvement in the focus latitude has been achieved using present pattern decomposition scheme.

6349-63, Session 15

Identification of subresolution assist features that are susceptible to imaging through process

L. S. Melvin III, Synopsys, Inc.

Subresolution Assist Features (SRAFs) are powerful tools to enhance the focus margin of drawn patterns. SRAFs are sized so they do not print on the wafer, but the larger the SRAF, the more effective it becomes at enhancing through-focus stability. The size of an SRAF that will image on a wafer is highly dependent upon neighboring patterns and models of SRAF printability are, at present, unreliable. Conservative SRAF rules have been used to ensure that SRAFs never print on a pattern. More accurate models of SRAF printing should allow SRAF rules to be relaxed, resulting in more effective SRAF placement and broader focus margins.

The process models that are used during Optical Proximity Correction have never been able to reliably predict which SRAFs will print on a pattern. This appears to be due to the fact that OPC process models are generally created using data that does not include subresolution patterns. In addition, the definition of a printing SRAF is not clear, as it can range from a photoresist film left on a wafer to a pattern that is transferred to the substrate during the etch process. This paper will demonstrate a model that identifies SRAFs which appear in photoresist and those which survive the etch step. Initial experimental results demonstrate that the model form is capable of accurately finding printing SRAFs, as well as finding the point when SRAF scum begins to appear on the wafer.

6349-64, Session 15

A fresh look at the cell-wise process effect corrections

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With moving from one process node to another, process effect corrections such are becoming a very challenging task. High quality models, long run times and extensively large computer resources are needed to perform a typical modern process effect correction procedure.

One of the main features of the modern process effects that make the corrections such a difficult task is the fact that these effects can no longer be considered as local. The value of a characteristic variable (exposure dose, edge position, etc) in each point of the wafer depends on the behavior of the variable in that point’s neighborhood, called “influence region” or “proximity region”. With the process node shrinkage, the typical size of this region has become large enough to include multiple layout features. The features (polygons, standard cells, memory cells) start to “see” each other. Corrections made to one feature lead to the necessity of re-correcting many neighboring features correspondingly.

Since all IC layouts are highly redundant and many layout features are repetitive, all the modern process correction algorithms try to take advantage of this redundancy to decrease processing time and computer resources requirements. However, currently used high accuracy process effect correction algorithms are becoming less and less advantageous because of the non-locality of the process effects.

There are simpler algorithms such as the “cell wise OPC”. The central idea of the cell wise optical proximity correction is to correct each cell as it were “isolated”. The whole layout containing many instances of the cells is then corrected by mere replacement of the cell instances with their corresponding counterparts. This approach is nearly optimal in terms of time and resource requirements, but its accuracy is questionable.

In this paper, we are trying to analyze feasibility of the cell wise OPC by using our own recipe. The recipe can be implemented with commercially available OPC tools. We use one of these tools to analyze the accuracy of the method.

6349-65, Session 15

Phase-shift reticle design impact on patterned linewidth variation and LWR

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Across-chip and across-wafer patterned linewidth variation (ACLV and AWLV respectively) as well as line-width roughness (LWR) are key contributors to device performance variation. In particular, polysilicon gate patterning enhancements are generally directed at reducing these sources of variation. Phase-shift mask (PSM) patterning techniques are known to improve process margin, ACLV and LWR. However, reticle manufacturing and optical proximity correction (OPC) are significantly more complex for aggressive PSMs used in low-k1 patterning at the 90nm and 65nm technology nodes. For polysilicon gate patterning, a direct comparison of the linewidth control possible through various PSM approaches is needed to select the most manufacturable process, as well as assess the extendibility of each technique.

Embedded attenuated PSM (6% EAPSM), chromeless PSM (CPL) and alternating aperture PSM (AAPSM) designs were selected for comparison. We will discuss different mask manufacturing technologies, their associated limitations and the impact of these limitations to on-wafer linewidth control. A full-field layout design consisting of a regular matrix of linewidth control monitors and OPC verification structures was used, and the design was treated with the available 65nm-node OPC models. The PSM reticles were then manufactured at the same mask shop. Polysilicon wafers were exposed with 193nm lithography using these reticles, and after selection of features to minimize through-pitch variation, lithography process latitude was measured for each feature. Additional wafers were patterned at best exposure and focus conditions and etched, and then ACLV, AWLV and LWR were measured for each PSM process. A high-transmission (30%) EAPSM reticle was also evaluated, as was the impact of different OPC models for EAPSM and CPL.

6349-66, Session 15

Implement alternating PSM in sub-80-nm DRAM with gate shrinkage via single exposure

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The technique challenge in sub 80nm, along with the insurmountable difficulties in illumination setting, has driven the DRAM into the low k1 lithography. To achieve the better critical dimension (CD) shrinkage, there are a lot of implementation, OPC (Optical Proximity Correction), SB (Scattering Bar), SRAF (Sub-Resolution Assist Features) and DDL (Double Dipole Lithography). Extending the lithography towards low k1 on the resolution enhancement technology (RET) is very essential as well. Alternating PSM is one of candidate in RET, however, there is also weak point in alternating PSM technique, such as the double exposure for phase conflict error. There is no more difference between the double exposure and alternating PSM, if the phase conflict error was no avoidable. Therefore, trying to implement to alternating PSM in GC layer without double exposure and phase conflict error is the main purpose of this study. There are a lot of kinds of pattern designs in main cell and periphery. It is necessary to study each of them and verify the key points.

6349-67, Session 16

Feasibility study of mask fabrication in double exposure technology

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With decreasing the design node, there are some candidates for the optical lithography technology. Double Exposure Technology (DET) is the one of the solution to extend the resolution limit down to k1 less than 0.25 for the next generation devices. To accomplish DET, photomask MTT, CD uniformity, and the overlay between the layers for the dual exposure are important as the photomask process aspect.

MTT and CD uniformity have been frequently discussed for Single Exposure Technology(SET), but the overlay and the registration have not been discussed yet with the view of DET.

In this work, the feasibility of mask fabrication, especially the overlay and the registration for DET are analyzed. The current mask limit of DET is discussed considering MTT, uniformity, and overlay.

6349-68, Session 16

High-transmission attenuated phase-shift mask for ArF immersion lithography

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Attenuated phase-shift mask (att.PSM) is one of resolution enhancement technologies (RET) and has been widely adapted for several device layers because of its simple structure and no necessity of double exposure. ArF immersion becomes the main lithography for 45nm node and the high resolution of att.PSM is expected with the combination of High NA and strong off-axis illumination (OAI). In our previous works, we found it is important to control the transmission of att.PSM film for the fine pattern imaging. Therefore, high-transmission att.PSM and tri-tone structure need to be evaluated in more detail.

In this work, we optimized the transmission and tri-tone structure for gate line and contact hole. The performances of optimized att.PSM were compared with other RETs. The investigations were performed by rigorous 3D mask electro-magnetic field simulation on mask topographies. We simulated mask error enhancement factor (MEEF), normalized image log slope (NILS), and the process window. To achieve the high resolution of mask patterns, improvement of mask-making accuracy becomes more important. So, the impact of mask-making error was studied and the error margin was estimated. The performances of att.PSM were confirmed by optical images using Aerial Image Measurement System.

6349-69, Session 16

Mastering double exposure process window aware OPC by means of virtual targets

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Optical proximity correction (OPC) has been successfully implemented throughout the microelectronics industry to improve patterning accuracy at nominal exposure conditions. Extensions of this OPC capability to improve dimensional control over a range of process variations, typically called process window OPC (PWOPC) [1] are still in development or early implementation [2, 3]. This paper addresses a further challenge to the concept of PWOPC by investigating the dimensional control of non-printing features to improve the process window (PW) of the primary layout.

The benefits of restricted design rules (RDR) have been praised in many publications. Especially the PW enhancements of placing critical features on a fixed grid seem particularly enticing. The RDR used for the layout discussed herein allowed line-width critical poly-conductor features to be designed in a single orientation at the contacted device pitch and integer multiples thereof [4]. These layout restrictions make the otherwise almost intractable challenge of double exposure alternating phase shift design trivial. By inserting sacrificial phase transitions at larger than minimum pitches of the same size as the poly-conductor feature size, the layout can be homogenized to a single pitch on the alternating phase mask.

The additional phase transitions are simply erased along with all other residual phase edge images in the subsequent trim exposure and do not leave a permanent resist image. Therein lies the challenge which is discussed in this paper: how do the mask dimensions of the non-printing features impact the through-process line-width control of the primary layout and how can OPC successfully control the dimensions of those sacrificial phase transitions?

When using off-the-shelf double-exposure OPC, one could easily miss a potentially introduced strong focus window dependency. The phase mask edge fragments forming the sacrificial phase transitions contribute only marginally to the simulated contour response of any neighbor-

ing real critical line. This makes their potential movement in the course of OPC mainly supporting a quick convergence and not considering the initial assumption of all phase areas being of approximately same width. A typical OPC result generates sacrificial phase transitions of significantly smaller widths than the phase transitions forming gates.

As a consequence, the focus window of gates without neighbors on a minimum pitch design on one or both sides is significantly reduced. Both, simulation and experiment prove the necessity to control the dimensions of the effectively non-printing, sacrificial phase transitions during OPC. For the investigated application, the OPC needs to match the mask dimensions of the sacrificial phase transitions with those phase transitions actually forming gates.

Besides simple rules-based solutions, the paper focuses on a model-based implementation for which virtual OPC targets were introduced into the OPC flow. The originally designed sacrificial phase transitions are turned into sacrificial gates serving as such virtual targets. Their purpose is to providing additional OPC targets which do not really exist in resist after both masks have been exposed. The paper describes details of the mechanics of how those virtual targets support an efficient model based process window aware OPC solution with the added benefit of being independent of specific litho processes.

Experimental proof is shown that introducing non-printing, virtual targets being considered as actual targets during OPC ensures enhanced through focus line width stability and hence making the OPC solution well aware of process window aspects.

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6349-70, Session 16

Finding the needle in the haystack: using full-chip process window analysis to qualify competing SRAF placement strategies for 65 nm

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It is widely understood that the IC Industry's adherence to Moore's Law is widening the gap between the wavelength of light used in semiconductor manufacturing and the features that they define. Increasingly, the patterning community has turned to higher complexity imaging solutions to fill the gap . This steadily increasing complexity is placing a new burden on lithographers and resolution enhancement technology engineers to guarantee that the highly complex patterning strategies will work for all patterns. Traditionally, lithography strategies have been characterized using relatively simple one-dimensional "litho test patterns." Real circuits are highly randomized however, and complex two-dimensional interactions are the rule rather than the exception.

This paper extends the paradigm for use of newly available post-OPC verification (POV) technology to the realm of RET development. We offer a case study where two competing 65-nm logic node sub-resolution assist feature (SRAF) strategies for poly layer patterning are evaluated on a full chip using commercially available post-OPC verification technology. We are able to evaluate differences in CD control process window, SRAF printability, MEEF sensitivity, and catastrophic defect propensity. In several critical cases, we show silicon confirmation of the simulated results. This methodology allows leveraging of existing full-chip POV technology to enable the selection of the best SRAF strategy with minimal use of costly split lot silicon.

6349-71, Session 17

Present challenges and solutions in sampling and correction for 45 nm

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Conventional OPC, also known as site-based OPC, has relied on rules-based fragmentation and site placement since its inception. The issues that arose in earlier generations around imprecise site and fragmentation placement, relative to the exact location of proximity effects, has been illustrated in earlier works [Reference 1], and generally did not produce catastrophic results. However, when coupled with the large process biases, strong RET, and accuracy requirements for 45 nm and future nodes, this imprecision can produce catastrophic results. This work will report on efforts to use model-directed site and fragmentation placement, as well as inclusion of process window knowledge into the site-based OPC flow to address varied sources of errors and relative results with different approaches.

In addition to the conventional site-based OPC, a new breed of tool that avoids sites in favor of fully gridded, or dense, simulation is rapidly maturing. The new approach allows more intelligence to be built into the OPC engine such that fragmentation and error sampling are more automated and thus less error prone. Using the same layout data, we will also present a snapshot of the new tool's results. This snapshot will include runtime analysis, since it is projected that grid-based simulation will become more compute-efficient than sparse simulation at some future site/layout density beyond the current 45 nm technology designs.

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6349-72, Session 17

PPC model build methodology: sequential litho and etch verification

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An important component of the mask-synthesis flow is the computational model used for process proximity compensation (PPC). One of the most significant modeling challenges is to obtain predictive models, i.e. models that achieve the required accuracy on layout features that have not been part of the initial calibration set. As in any other modeling approach attempting to describe physical phenomena both empirical and physical models typically can be adjusted such that they provide good "fitting" results on the calibration sets. In fact, for empirical models it is typically easier to achieve good model fits on the calibration even if the data provided contain erroneous data for example caused by improperly calibrated SEM magnifications. However, the primary purpose of PPC models is not to provide a good fit to limited calibration set, but rather it has to perform well on a large variety of layout geometries. Unfortunately for such geometries data sets outside the predictive qualities of empirical models are at best questionable. Only models capturing the essential physical and chemical mechanisms provide a reasonable foundation on which to expect good predictive performance of the model.

In this paper we will discuss our methodology of building through process physics-based litho and etch models which result in both accurate AND predictive models. First step is the calibration of litho and etch models. The litho model parameters are inverted using DI data collected on a set of standard test-structures for a set of exposure dose and defocus conditions (through process calibration). The litho model includes effects such as resist diffusion, chromatic aberrations, defocus bias, lens aberrations, and flare. Etch model, which includes (but is not limited to) pattern density and particle collision effects, is calibrated independently using DI and FI data also on standard test-structures. The two model components are then combined, but before being exported for use in PPC, the combined model is signed-off using a set of verification structures. These verification structures are highly 2D geometries that are placed on the test-reticle in close vicinity to the calibration test-structures. Using through-process DI and FI measurement and images from verification structures, model prediction is compared

to wafer results, and model performance both in terms of accuracy and predictability is thus evaluated and verified. In summary, we have developed a model build methodology which results in a highly accurate and predictive computational model for process proximity compensation.

6349-73, Session 17

Correcting lithography hot spots during physical design implementation

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As the technology node shrinks, printed-wafer shapes show progressively less similarity to the design-layout shapes, even with optical proximity correction (OPC). Design tools have a restricted ability to address this shape infidelity. Their understanding of lithography effects is limited, taking the form of design rules that try to prevent “Hot Spots.” A Hot Spot is a location that may demonstrate some lithographic-printing problem such as pinching, bridging, or line-end shortening that results in device failure, or unacceptable shrinking of the process window. Meanwhile, design rules are becoming increasingly complex and ultimately less useful in addressing the lithography challenges. Design tools that have a better understanding of lithography are becoming a necessity for technology nodes of 65 nm and below.

For the 90 nm technology node, Hot Spot likelihood may be reduced with a flow that iterates between a Lithography Compliance Check (LCC), and physical design implementation in a Place and Route (P&R) system. While the implementation phase is automated from netlist (the output of logic synthesis) to tapeout, an iterative process is required to manually fix Hot Spots that are detected after tapeout. There are several problems with this flow. First, the run time for detection is already unacceptable at 90 nm, and will only worsen at 65 nm since the number of Hot Spots will increase. Second, multiple iterations of detection and correction are generally required since fixes may create new Hot Spots. The long run time for each iteration may not allow sufficient convergence in a limited time. Third, it may be unclear how to manually fix the Hot Spots.

The goal of correcting lithography Hot Spots during physical design implementation is to automatically fix a majority of the Hot Spots in the Metal 2 layers and above, with a run time on the order of a few hours per layer. To achieve this goal, the current flow will be modified as follows. First, Hot Spot detection will become faster by using rule-based detection. Second, Hot Spot correction will become automatic by using rule-based correction. Third, convergence of corrections will be avoided by performing correction locally, which means that correcting one Hot Spot should not create new Hot Spots.

There are three stages in this flow. Stage 1 is Rule-Based Detection, which identifies possible Hot Spot locations or “Hot Spot candidates.” In Stage 2, these candidates are confirmed or rejected by Model-Based Detection, which is *localized*: only the local vicinity around each candidate is passed to the Model-Based stage. Localization provides a significant run-time advantage since (i) it reduces the total layout size that is sent to Model-Based Detection, and (ii) Model-Based Detection dominates the total run time. Finally, in Stage 3, the confirmed Hot Spots are fixed by Rule-Based Correction, which is implemented in the Place & Route system.

6349-74, Session 17

Combined resist and etch modeling and correction for the 45-nm node

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Emerging resist and etch process technologies for the 45 nm node exhibit new types of non-optical proximity errors, thus placing new demands on OPC modeling tools. In a previous paper (SPIE Vol. 6283-75) we had experimentally demonstrated a full resist and etch model calibration and verified the stability of the model using 45nm node standard logic cells. Building upon those results, this paper focuses on the correction of patterns.

Resist and etch corrected patterns have been placed on a 6% reticle for experimental verification. The patterns were corrected using three different approaches: 1) using the traditional rules based correction; 2) with the model-based two stage correction; 3) with a lumped model single-stage correction. Here we compare in silicon results from the three approaches.

6349-75, Session 18

Application challenges with double patterning technology (DPT) beyond 45-nm node

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Double patterning technology (DPT) has been investigated in the recent years as a strong candidate to extend optical lithography to 45nm node and beyond [1, 2, 3]. This has been mainly driven by the timely concern for the readiness of immersion hyper NA scanners versus EUV exposure tools for R/D device development, which must be started two years before manufacturing. Double exposure technology, such as Double Dipole Lithography (DDL), is an imaging method with two optically correlated exposures. The k1 (= (half pitch)*(numerical aperture)/(exposure wavelength)) is limited to 0.25. [2] DPT refers to an imaging process where a pattern etch transferring step occurs between the 1st and the 2nd exposure. That is, there is no optical imaging correlation except for the wafer alignment impact between the two separate patterning steps. In DPT method, one can relax the design pattern pitches by decomposing the dense patterns into two half-dense pattern masks and produce the intended design patterns on wafer after combining two mask patterning steps. Thus each individual exposure has a higher k1 factor simplifying the imaging. With composed patterning, we are able to achieve a very low k1 pattern that is beyond traditional Rayleigh resolution limit.

For DPT, the split method is the key element of the technology. There are two different approaches of achieving the intended design pattern that have been suggested. [2,3] One is Color Line method (CLN), or “positive” tone process, and the second is Color Space method (CSP), or “negative” tone process. The CLN defines critical features with 2X of the intended design pitch, and the combined result of two exposures reproduces the original design. While the CSP defines one edge of the critical feature per one exposure, each exposure works as feature defining and trimming step for the critical feature. Both methods can be easily applied to dense memory gate type of patterns with acceptable CD uniformity (CDU). [3] However, it is more difficult when trying to print complex 2D array structures or random logic lines that are connected with each other. In many cases, both the critical and non critical features need to be decomposed in a specific way to avoid printing a feature pitch or spacing smaller than the resolution capability of a single mask exposure.

For a successful manufacturing with DPT, we need to pay a close attention to the likely impact on mask making specifications and the exposure process optimization for each of the double patterning step.

One important area is how to ensure a “right” amount of pattern stitching. In order to assure CDU and process window, the OPC for critical pattern stitching must factor in the imaging tolerance due to mask making and exposure overlay. Moreover, the patterning fidelity of complex 2D shapes such as line-ends and corners are much more suspect to form stronger OPE, especially for those of critical feature dimensions on the 4X mask that are smaller than exposure wavelength. For DPT, it is clearly insufficient to just consider k1 factor for imaging. This paper will discuss DPT application challenges beyond 45nm node. We attempt to define how to best achieve a full-chip DPT patterning in manufacturing, more specifically related to defining mask making specifications, and critical OPC requirements to achieve necessary pattern fidelity for the critical 2D structures.

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6349-76, Session 18

The effect of OPC optical and resist model parameters on the model accuracy, run-time, and stability

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Model Based Optical Proximity Correction (MB-OPC) is essential for the production of advanced Integrated Circuits (ICs). As the speed and functionality requirements of ICs production always require reducing the Critical Dimension (CD), the demand is continuously increasing for more accurate and representative OPC models.

Model calibration with measured test patterns is the most critical step in building accurate OPC models. The optical and resist model parameters selected during model calibration have a significant impact on the OPC model accuracy, run time, and model stability. In order to avoid unpractical run times, a compromise between the run time and model accuracy has to be performed. The modeler has to optimize the necessary model parameters in order to find a good trade-off that achieves acceptable model accuracy with reasonable run time. In this paper, we investigate the effect of some selected optical and resist model parameters on the final OPC model accuracy, run time, and stability. An OPC model that is believed to be one of the best models, was used as a reference model. Optical model parameters were varied and the impact on the model accuracy, run time, and stability was recorded. This was performed by checking the resulting OPC model for each test case with a representative IC layout and compared with wafer images to check the model accuracy and stability. The run time was recorded for each case to perform the comparative study. Similar work was performed for the resist model parameters. The result from this is very important for the OPC modelers in order to improve the quality of the OPC models.

6349-77, Session 18

Managing high-accuracy and fast convergence in OPC

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The requirement of tighter tolerances is one of the key challenges to optical proximity correction (OPC) within the transition to 65nm technology node. This might result either in excessive OPC runtime or limited accuracy. During development stage we sacrifice runtime in favor of accuracy, but this might cause resource conflicts by switching to large designs in volume production. OPC strategy needs to be adjusted to reduce the runtime without any loss of accuracy.

Commonly we use a rather pragmatic approach for adjusting OPC parameters: one global parameter for all features. This makes coding much easier, albeit it results in a compromise of various aspects. Fragments differ from each other in respect to geometries, tolerances, process windows (PW), and mask error factors (MEF). For example, a straight fragment on gate needs a very high accuracy, which can never be reached on a corner fragment. Or on the other hand, a fragment with a high MEF reacts more sensitive to edge movements than a straight one with non critical dimensions. In the end we might not reach the best possible accuracy for all features and need more OPC iterations than necessary. In some cases we even might end up with rather large errors due to non fitting parameters.

This paper discusses methodologies to address both criteria's: OPC runtime and accuracy.

At first we need to separate our design into fragments of distinguished categories. The separation can be based on geometrical parameters or process parameters. Geometrical parameters might be corners, line ends, and straight edges where process parameters might be process window, mask error factor, and required tolerances. Both approaches have advantages and disadvantages and will be discussed in more detail.

Once we have divided the fragments into several categories we can address the issues independently. There are several parameters which can be adjusted to improve accuracy and to reduce runtime.

We can now adjust the feedback value independently to improve the convergence of a certain feature. By doing this we have to understand the side effects or otherwise we create more problems than we solve. A worst case scenario would be an oscillating fragment, where we always overshoot the edge correction.

Another parameter might be the tolerance value, which affects the reachable accuracy for a specific fragment. This value must match the conditions of the accordant fragment or otherwise there might be no convergence possible. For example, a structure with a high MEF will never converge to a very high accuracy.

The resulting OPC solution has a significant reduced number of iterations although it converges to a higher level compared to a standard OPC approach. This methodology satisfies the need for a fast turn around time, which is highly appreciated in manufacturing, and the demand on high quality photo masks, which is necessary to support timing critical circuits.

6349-78, Session 18

Influence of design shrinks and proximity influence distance on flattening of optical hierarchy during RET

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As geometries become smaller the common practice of global design shrinks combined with the PID, proximity influence distance of the optical system illumination, mask type and numerical aperture, NA has a tendency to further flatten the database hierarchy. The use of optical hierarchy rebuild1 has been used previously to reduce the amount of RET data sent to the mask manufacturer. But as geometries shrink and tighter density of features at specific levels is obtained, a large increase in data can occur by just blindly flattening the hierarchy. This increase in data leads to numerous problems of mask making and inspection2,3. In this paper techniques for reducing the impact on data increase as geometries shrink, also taking into account final machine fracturing is explored through the judicial use of PID during the RET generation and subsequent DRC operations. One method explored for reducing data size is to use a smaller PID during RET generation, and then using a larger PID during ODRC or RDRC to look for litho hotshots that were missed by too small of a PID during RET, reticle enhancement techniques application. By identifying only the failed areas and extracting using the SmartExtract algorithm for further optimization, the litho hot spots are addressed with only a very small percentage of increase in the data. Significant reductions in data can be addressed with this method versus a global application of RET that is not required for all geometries.

6349-79, Session 18

Empirical OPC rule inference for rapid RET application

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A given technological node (45 nm, 65 nm) can be expected to process thousands of individual designs. Iterative methods applied at the node consume valuable days in determining proper placement of OPC features, and manufacturing and testing mask correspondence to wafer patterns in a trial-and-error fashion for each design. Repeating this fabrication process for each individual design is a time-consuming and expensive process.

We present a novel technique which sidesteps the requirement to iterate through the model-based OPC analysis and pattern verification cycle on subsequent designs at the same node. Our approach relies on the inference of rules from a correct pattern at the wafer surface it relates to

the OPC and pre-OPC pattern layout files. We begin with an offline phase where we obtain a “gold standard” design file that has been fab-tested at the node with a prepared, post-OPC layout file that corresponds to the intended on-wafer pattern. We then run an offline analysis to create these rules. During the analysis, our method implicitly derives contextual OPC rules for optimal placement of RET features on any design at that node.

We demonstrate our method on several designs of varying sizes and show that the resulting photomasks produce images with error comparable to those produced under traditional production strategies. The method offers a rapid and accurate alternative to these methods. Beyond providing time-to-market advantages for mask manufacturers, it also creates an opaque mechanism for the interchange of RET and OPC strategies from foundries to designers without revealing proprietary information about the model or technology node.

6349-80, Session 19

Benchmarking the productivity of photomask manufacturers

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This paper describes an empirical study that investigates the productivity of photomask manufacturing, which drives the cost of photomasks. Data for this study comes from a set of 79 productivity-oriented questions that were attached as a supplement to Sematech’s annual survey of photomask manufacturers. Questions regarding operating factors solicited quantitative information regarding clean room space, operating personnel and engineering support. Questions regarding equipment utilization solicited quantitative information regarding output of product plates, output of engineering plates, scheduled equipment downtime and unscheduled equipment downtime. Questions in all categories were highly differentiated, so as to enable a detailed breakdown of the results with respect to factors such as clean room class, direct labor, various engineering efforts (process control, yield, maintenance/installation, R&D/new product development, data processing and sustaining) and 15 equipment categories.

Seven of the eight participants in the survey answered the majority of questions, indicating that the interest in this subject among photomask manufacturers is very strong. Data analysis yielded 79 normalized, cost-related or productivity-oriented indicators that assured the anonymity of the participants. An index which assesses the technological sophistication of the participants was developed from the product mix of the participants. Participants that produce a greater proportion of plates with small geometries rate commensurately higher on the technology index.

The following results were found to be significant:

- Variations in excess of an order magnitude between the mask shop with the highest value and the one with the lowest value were observed in many indicators, suggesting that all participants may have significant cost-reduction opportunities within their operations.
- A strong correlation between the technology index and the number of engineers per plate produced has been observed. This suggests that making masks, which print small geometries, require a disproportionate engineering effort.
- For participants that produce more than 20,000 product plates per year, there exists a direct correlation between the technology index and the number of plates produced.
- The technology index for the most advanced participant was more than 3.5 times as high as that of the least advanced participant. Some technologically advanced participants used up a much higher proportion of (non-sellable) engineering plates than technologically less advanced participants.
- There was no significant correlation between the technology index and the fraction of the mask shop containing a Class 1 clean room.
- The engineering effort in mask making is asymmetric. The investment in maintenance and installation, R&D/new process development and sustaining is significantly higher than the investment in process control, yield and data processing.
- No correlation between the various engineering efforts and yield could be established.
- There was no significant correlation between yield and the fraction of the mask shop containing a Class 1 clean room.
- Scheduled and unscheduled downtime of pattern generation was higher than downtime of other equipment, even though pattern generation equipment has a very high cost of ownership and frequently limits the throughput of the mask shops.

6349-81, Session 19

Required mask specification for mass production devices below 65-nm design node

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In the photo-lithography process, a mask is the one of the most important items because its imperfection transfers its CD error to the CD error on the wafer. And the CD error amplification from the mask CD to the wafer CD is denoted using Mask Error Enhancement Factor (MEEF).

As the device shrinks so fast, MEEF increases conspicuously and massive OPC is necessary to secure the target pattern CD and the proper process margin on the wafer. Therefore the mask CD uniformity and the just mean-to-target (MTT) are very important to minimize the CD variation on the wafer level.

In most cases, MTT and CD uniformity for a certain device are not defined exactly. What we know is that the smaller, the better. Because, however, just small value of MTT and CD uniformity is not the reasonable guideline for the mask fabrication and induces high mask cost, defining the logical MTT and CD uniformity prospect for a certain device or layer is very important.

As the necessity of the low k1 process increases, MTT and CD uniformity specifications are tightened. However the proper mask specification for sub-65nm real device has not been defined yet and not been studied considering OPC and MEEF.

In this study MTT and CD uniformity specification of the sub-65nm real device patterns are discussed with respect to OPC and MEEFs. MTT and CD uniformity tolerance is defined by OPC tolerance, and OPC tolerance is directly related to the pattern layouts and MEEF. To define the mask MTT specification, MEEF of the critical pattern design is calculated and compared with other pattern design. In the region of the linearity for MEEF and CD variation, MTT and MEEF relationship is commented.

6349-82, Session 19

Assessing the impact to the photomask industry from external funding for infrastructure development

M. J. Lercel, SEMATECH, Inc. and IBM Corp.; A. Grenville, SEMATECH, Inc. and Intel Corp.; P. Marmillion, SEMATECH, Inc. and IBM Corp.

The photomask industry is a small component of the global semiconductor industry, but represents a critical enabling element for both process and product development. Previous mask industry assessment studies have highlighted a critical gap between the amount of research and development funding available for photomask infrastructure based on business return on investment and the amount needed to maintain an aggressive lithography roadmap [1]. This gap has often been bridged by external funding from government agencies and consortia. Significant funding has been provided by consortia such as SEMATECH and the qualitative benefit has been recognized, but little effort has been made to quantify this benefit to the industry.

In 2002, an industry survey by SEMATECH suggested that mask costs could rise by 80% per node and mask set costs could reach >$3M by the 45 nm node. However, the 2005 industry study indicated that mask costs increased by only ~15-20% per node during 2002 to 2005 and overall mask yields had increased [2]. During this same period,

SEMATECH and Selete projects on mask repair yielded new products that became available to the mask industry. Repair yield improvement is not the only reason for the rise in mask costs but hard defects contribute ~50% of the yield losses. Repair technology significantly improves the ability to repair hard defects [3]. Qualitatively, the early availability of mask repair tools provides an obvious benefit to the mask and semiconductor industries, but quantifying the way in which external support for infrastructure benefits the industry is challenging.

This paper attempts to quantify the benefit and return on investment of early industry availability of mask repair tools from the SEMATECH mask repair program. Two analysis methods are compared. A macroeconomic analysis using yield improvements provides an industry view of the benefit, and a mask cost of ownership calculation provides the unit cost benefit.

[1] S. Hector, "The difficult business model for mask equipment makers and mask infrastructure development support from consortia and governments," Proc. SPIE 5992 (2005).

[2] G. Sheldon, "Mask Industry Assessment 2005," Proc SPIE 5992 (2005).

[3] B. Grenon, S. Hector, "Mask Costs: A New Look," European Mask and Lithography Conference proceedings (Jan 2006).

6349-83, Session 19

Mask factory automation: getting started

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Automation of factory information is the key to making manufacturing and yield improvements in today's factory. However, the mask manufacturing industry has not kept pace with the automation improvements and successes exhibited in the semiconductor industry. Many automation standards are currently available. Applying these standards to the mask manufacturing equipment and factory would make material movement and data flow and collection more efficient and reliable. The overall goal of automating the factory is to provide the customer with the saleable goods of interest on time with no errors. Without "immediate" access to tool data, process data, measurement data, cleanroom data, and factory data, making timely decisions that improve factory efficiency and yield is very difficult.

This paper will describe steps to begin automating the mask factory. It also will map out the framework standards, their primary descriptions, and why they are required to get started.

6349-164, Session 19

A procedure and program to calculate shuttle mask advantage

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A well-known recipe for reducing the mask cost of new products is to place non-redundant components of the database (intellectual property, IP) related to that product family on one reticle plate. Such masks are also known as multi-product, multi-layer, or multi-IP masks. While conceptually this is a simple exercise, in practice one must consider a great variety of process flow options, fab volume, and loading using careful calculations. Also it is highly desirable to enable immediate visual verification, because, once the data is transferred to the mask shop and the first reticle is shipped, the cost of changing the mask architecture is significantly more than in the conventional scheme of single product or layer per plate. To enable the calculations, we have proposed an algorithm where mask layers are first lined up according to price and field tone. Then, depending on product die size, expected fab throughput, and scribe line width requirements, the subsequent product layers are placed on the masks with different grades.

Actual reduction of this concept to practice allowed us to make important improvements. One practical manufacturing constraint is that the valid number of layers per plate is very limited, e.g., 2, 3, or 4. More layers per plate are impractical as it would result in smaller exposure area and thus require an excessive number of exposures per wafer. With this restriction, one can create layer databases for technology groups, which mostly benefit from shuttle masks. In these databases, we considered different layer matching options. While the nominal option called for cost-minimization matching, this may not always be the best approach for bringing the product manufacturability up to speed. It became necessary to introduce manual layer grouping to ensure that, e.g., all metal layers would be placed on the same plate, allowing for easy and simultaneous design fixes. Another important modification is to allow non-critical layers, which require low mask quality, to be placed in a less restrictive way. This dramatically reduced the count of "orphan" layers. We proposed a set of matching rules to ensure that a designer is offered the best option, not only from the standpoint of price, but also in terms of flexibility and fab-friendly architecture, which impacts time to market. In summary, we have created a program to automatically propose and visualize shuttle mask architecture for design verification, with significant enhancements to the nominal algorithm due to the actual application of the code.

6349-85, Session 20

NIL template making and imprint evaluation

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Nano-imprint lithography (NIL) is expected as one of the candidates for 32nm node and below. NIL needs 1X patterns on masks and a transit from 4X to 1X means a big and hard technology jump for the mask industry. Therefore, the first and most important investigation to be done from the mask manufacturing side is to confirm if the resolution of current photomask manufacturing and its extension will be sufficient or not. We reported in PMJ20051 and PMJ20062 that we could achieve 25nm isolated spaces, 35nm dense lines, and 40nm holes with a 100keV spot beam exposure tool, mainly by optimizing the resist material and its thickness. As a result, we had reached the resolution target for hp32nm, but for hp22nm the resolution was not enough.

In this paper, we have examined further improvement possibility in resolution limit and have found that to achieve 22nm resolution, improvement of the resist process was inevitable. In particular, the modification of the development process and the pre-dry etch treatment have showed promising results.

We also have investigated the impact of the pattern profile on the imprint performance. By changing the pattern profile intently, we evaluated how the profile and depth of the mask pattern would influence the imprint process and have tried to optimize the profile and depth. Actual mask pattern profiles with imprint results will be shown at the conference and manufacturability of those templates in terms of profile and depth control will be discussed.

6349-86, Session 20

Direct die-to-database electron-beam inspection of fused silica imprint templates

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Step and Flash Imprint Lithography (S-FILTM) is a unique method for printing sub-100 nm geometries. Relative to other imprinting processes S-FIL has the advantage that the template is transparent, thereby facilitating conventional overlay techniques. Further, S-FIL provides sub-100 nm feature resolution without the significant expense of multi-element, high quality projection optics or advanced illumination sources. However, since the technology is 1X, it is critical to address the infrastructure associated with the fabrication of templates. The purpose of this paper is to examine the issues surrounding inspection of the template.

Imprint lithography has been included on the ITRS Lithography Roadmap at the 32 and 22 nm nodes. At these dimensions, an electron beam solution will be required to identify the defects created during template

fabrication and wafer imprinting process. In addition, a die-to-database approach is essential for verifying the patterns written and etched into template. This paper reports the results of a systematic study of die-to-database electron beam inspection of both imprinted wafers and the direct inspection fused silica substrates.

The die-to-database inspection of the patterns was performed on an NGR2100 inspection system. The NGR2100 consists of an Electron Image Acquiring System (EIAS), a Geometry Verification Engine (GVE), and a GUI interface. The key features of the EIAS include high-resolution and high speed secondary electron acquisition capability, a scan generator to acquire images of a large area, and proprietary electron optics to eliminate field distortion over the wide scan field. A die is scanned by a field of view, step-by-step, to acquire the image to be verified. A feature contour is extracted, represented by lines and curves corresponding to the edges of the imaged feature. The contour is then compared to the target design data, to create a differential bias. The bias data is used to output to verify compliance with a known process window or CD measurement.

Previous inspection methods required either templates with indium tin oxide layers or the inspection of imprinted wafers, since the ability to directly inspect a fused silica template at high data rates was not possible. With the introduction of new charge reduction technology, a fused silica imprint template, or a comparable phase shift mask can now be directly inspected. Initial experiments were performed on imprinted wafers and fused silica wafers consisting of arrays of Logic and Metal 1-like patterns with critical dimensions as small as 40 nm. Defects within the patterns as small as 15 nm were readily detected. The methods used to detect and categorize defects will be presented. The extension of the technology to even smaller geometries and the prospects for directly inspecting the template will also be discussed.

6349-87, Session 20

Systematic approach to reducing imprint template defectivity

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Recent publications have addressed the issues surrounding cost, resolution and image placement for imprint templates. Imprint templates with 80nm images are routinely produced and are being used in non-defect sensitive applications and for initial CMOS type structures. The ITRS has added imprint lithography to its options for the 32nm node, and all indications from template fabrication work show good progress in image placement and resolution should be attainable. The remaining issue is one of pattern verification and defect inspection. Many companies are working on e-beam based tools for template inspection however none are available for commercial use today. Current optical inspection tools, while not official supported by their makers for template inspection are currently being used for this work.

In this paper we have built imprint templates with larger feature sizes so that we can use the current inspection equipment at its maximum sensitivity to isolate true template fabrication and use defects from template features that trigger the generation of false defect calls. These works traces plates through the manufacturing process, including dice and polish steps and re-clean after imprinting of wafers.

6349-89, Session 21

PMJ Panel Discussion Overview: Mask technologies for EUVL

M. Sugawara, Association of Super-Advanced Electronics Technologies (Japan); H. Sano, Dai Nippon Printing Co., Ltd. (Japan)

No abstract available

6349-90, Session 21

Manufacturing of the first EUV full-field scanner mask

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In the framework of the European EXTUMASK project, the Advanced Mask Technology Center in Dresden has established in close collaboration with the IMS-Chips in Stuttgart a first integrated mask process suited to manufacture EUV masks for the first EUV full field scanner, the ASML EUV alpha-demo tool. The first product resulting from this process is a mask designed to perform the set-up of the ASML EUV alpha-demo tool.

The mask process was developed using dummy EUV blank material received from Schott Lithotec in Meiningen (Germany). These blanks have a Ta-based absorber and a thin SiO_2 buffer layer. During process development, the e-beam lithographic as well as the patterning behavior of this material was studied and tuned to meet first EUV mask specifications.

For production of the set-up mask the developed process was applied to a high performance EUV blank from Schott Lithotec. This blank has identical absorber and buffer layer as the dummy blanks used for process development but in addition a multilayer is implemented which is deposited on a highly polished ULE substrate. The actinic parameters of the multilayer stack as well as the flatness of the substrate were carefully tuned to match the specifications of the ASML alpha-demo tool. In this article we describe the development of the integrated mask process and show the achieved mask performance.

6349-91, Session 21

Simplified model for absorber feature transmissions on EUV masks

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An absorber feature mask transmission model based on a displaced thin mask with edge line sources is introduced for rapidly assessing the impact of scattering from 2D absorber features on EUV masks. The modeling and simulation of EUV absorber features is challenging due to their electrically thick nature (~5λ). Rigorous simulation can be used to simulate both the absorber material and the multilayer but is extremely time-consuming. This new methodology which also works for off-axis illumination is a key step in enabling the extension of the fast ray tracing methodology [1] to the simulation of the printability of buried non-planar multilayer defects in the presence of absorber features.

The thin mask transmission function is developed by using Finite Difference Time Domain (FDTD) simulations of isolated edge scattering to understand the physical response fields of the absorber edge to the incident field. Figure 1 shows the physical response fields' magnitude and phase for normal incidence. The near fields reaching the multilayer structure were then studied in the Fourier transform domain to identify only those physical effects that would generate significant contributions to an EUV imaging system in the presence of the low pass filtering of the lens. Two effects are shown to be dominant. First, at each edge the absorber effects were found to double the periodicity of the structure and scatter energy into the even diffracted orders. To a large extent, these absorber edge response fields can be characterized by modeling a 2D line source at the top corner of the absorber edge. The second dominant effect, which was found from the odd components in the spectrum of the near fields, is that angularly dependent phase shifts have already occurred in reaching the interface between the absorber and the multi-layer. A suitable method for correcting for these phase shifts to first order is to vertically displace the thin mask transmission function by about half the absorber thickness.

This methodology for isolated edges works well for modeling off-axis transmission through 4X mask openings for the 32nm, 22nm, and 15nm line and space patterns on the wafer. Figure 2 shows the near field

transmission of the new thin mask transmission function relative to the transmission calculated by FDTD for a 22nm feature grating. The fields have been low-pass filtered down to a hypothetical best possible ever scenario of an NA = 1.0 imaging system. This corresponds to restricting the transmitted angular spectrum at the mask to about ±15°. Excellent agreement can be seen for various incident angles.

[1] M.C. Lam and A.R. Neureuther. Proc. of SPIE, vol. 5751, 2005.

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6349-92, Session 21

Profile metrology of EUV masks using scatterometry based optical digital profilometry

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Research and development efforts on EUV technology for the 32 nm node and beyond are progressing rapidly. Although a big concern is defect control in EUV mask blanks, control of linewidth and profile will be an important factor in acceptance of this technology. In this paper, we discuss the issues and strategies surrounding CD and profile metrology of EUV masks. EUV mask blanks from Hoya and Asahi Glass Company were used in this study. The masks were measured on a Nanometrics Atlas-M measurement tool while spectrum data were analyzed for CD and profile using Timbre Technologies' ODP analysis software. The Atlas-M tool has dual optics that enable use of either normal incidence based Reflectometry or oblique incidence based Ellipsometry. Both these technologies are different flavors of Scatterometry. The relative merits of each of these technologies are discussed. The complex EUV stack presents numerous challenges for metrology. A critical task is to accurately measure the optical constants of the numerous layers in the stack. The multilayer MoSi stack is effectively modeled as a single layer for optical constants determination. Photoresist FEP171 was used for the patterning. CD and profile of the resist were measured after which the absorber layer was etched. Parameters characterized in this study include photoresist CD and height, etched Absorber CD and capping layer over etch. Correlation to top-down CD-SEM, cross-sectional SEM, and AFM is reported. No charging or other deformation was observed on the EUV masks. The data show that ODP Scatterometry provides a non-destructive way to monitor resist CD & profile as well as etched structure CD and over/underetch on EUV masks

6349-93, Session 22

Development of EUVL mask blank in AGC

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Recent rapid progress in EUVL technology is ensuring that EUVL will be a primary candidate for the next generation lithography beyond 32-nm node. However, realization of defect-free mask blank is still counted as one of the most critical issues for high volume production in EUVL. AGC has developed comprehensive technologies for manufacturing the EUVL mask blank from polishing glass substrate to surface cleaning, multilayer coating, and evaluating its performances by making use of our long and wide experience in providing high quality processed glass substrate and coating for electronic devices. In this paper, we will present the current status of each aspect of EUVL mask development in AGC toward the specifications required for high volume production. In the effort to meet the specifications, we have introduced a number of key technologies that can be divided into three regions which are materials, glass processings, and evaluations.

We have developed state-of-the-art processes and tools for manufacturing EUV mask blank, such as a new polishing technique for extremely flat substrate, a new cleaning tool for low-defect substrate, and a newly developed deposition tool for ultra-low defect and higher EUV reflective coating with our new optical thin film materials in EUV region for multilayer mirror and absorber. Furthermore, in order to clarify their performances, we also introduced a wide variety of evaluation techniques such as flatness and roughness measurement of substrate, a defect inspection tool, and an EUV reflectometer as well as defect analysis techniques which help us eliminate printable defects in EUVL mask blank.

6349-94, Session 22

Point cleaning of mask blanks for extreme-ultraviolet lithography

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Everyone has had the experience of picking up a nominally clean kitchen utensil and finding a small baked on residue that remained behind after washing. A common response is to scratch off the offending residue and blow away the remains. Mask Blank Development Centre (MBDC) at SEMATECH North, RAVE LLC and the College of Nanoscale Science and Engineering at the State University of New York, Albany have undertaken a study to investigate a nanotech version of this simple process as a final cleaning step in the preparation of defect free EUV mask blanks. Depending on the substrate surface property, there are few nano scale convex defects that can not be removed by conventional mask cleaning processes. These so called hard defects are partially embedded in the glass substrate or adhere with strong forces to the surface. After mask blanks are cleaned using the Sematech North's MBDC Best Known Method (BKM) they are inspected in the Lasertec M1350. Defects later will be reviewed and classified by Lasertec M1350 and hard defects will be identified. The Lasertec uses an integrated nano-indenter to add alignment fiducials to the mask blank and a KLA Reference File (KLARF) file is generated which reports the position of any remaining hard defects. The mask blank and the associated KLARF file are transferred to a RAVE LLC NM650 repair tool where hard defect is located and removed by nanomachining. This is followed by an eco-snow cleaning process to remove the debris, a repeat of the SEMATECH North's MBDC BKM clean and re-inspection. At this point we have successfully aligned mask blanks to the Lasertec alignment targets and successfully imaged residue using the NM650's AFM imaging mode. We will be proceeding shortly to an evaluation of the actual point cleaning process and will report the full results at the conference.

6349-95, Session 22

Implementation of EUV mask pattern inspection for memory mask fabrication in 45-nm node and below

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As the design rule continues to shrink towards 45 nm node and beyond, the lithographers need the new technologies such as immersion lithography and EUV lithography. Also the inspection specification on the printed reticle defects is becoming even more challenging for the reticles used in both lithography methods.

The main purpose of this study is to investigate the pattern defect detection capability on EUV mask with the memory design patterns of 45 nm node and below in the DUV reticle inspection systems at our mask-shop and to compare those results with the absorber defect specification from the EUV lithography simulation in those design rules.

In addition, we investigate the inspection capability on the pattern defects with the test optical mask designed in 45 nm node and below for the immersion lithography and compare the defect detection ability on the EUV mask and the optical mask in the current DUV reticle inspection equipment.

6349-96, Session 22

Multilayer defects nucleated by substrate pits: a comparison of actinic inspection and non-actinic inspection techniques

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Inc.; S. B. Rekawa, Lawrence Berkeley National Lab.; O. R. Wood II, SEMATECH, Inc.; J. S. Taylor, Lawrence Livermore National Lab.; H. Han, SEMATECH, Inc.

The production of defect-free mask blanks remains a key challenge for EUV lithography. Mask-blank inspection tools must be able to accurately detect all critical defects whilst simultaneously having the minimum possible false-positive detection rate. We have recently observed and will report the identification of bump-type buried substrate defects, that were below the detection limit of a non-actinic (i.e. non-EUV) inspection tool. Presently, the occurrence of pit-type defects, their printability, and detectability with actinic techniques, and non-actinic (i.e. non-EUV) commercial tools, has become a significant concern.

We believe that the most successful strategy for the development of effective non-actinic mask inspection tools will involve the careful cross-correlation with actinic inspection and lithographic printing. In this way, the true efficacy of prototype inspection tools now under development can be studied quantitatively against relevant benchmarks. To this end we have developed a dual-mode actinic mask inspection system capable of scanning mask blanks for defects (with simultaneous EUV bright-field and dark-field detection) and imaging those same defects with a zoneplate microscope and 600-1000Å~ magnification.

In this paper we report on the side-by-side comparison of actinic and non-actinic inspection of multilayer defects nucleated by programmed substrate pit defects of varying sizes. We will present cross-calibration measurements revealing the current state of the art defect-detection sensitivity of the tools available to us.

6349-97, Session 22

Recent imaging results from the RIM-13 high-resolution EUV aerial image microscope

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RIM-13 is an actinic reticle imaging microscope which generates aerial images from blank or patterned EUV masks. Its optical system emulates the 0.0625 NA and 6° reticle angle of a 0.25 NA 4x demagnification (hence 0.0625 NA at the reticle) EUV lithographic scanner. It employs a Kohler illumination system with interchangeable partial coherence apertures. A 50μm diameter area of the mask is imaged by a 10x magnification EUV objective onto a scintillator crystal. The resulting green fluorescent image is then projected by a bespoke microscope, at 25x, 50x or 75x magnification onto a cooled, backthinned CCD detector. The optical system is mounted on a vibration-isolated platform within a large vacuum chamber.

The RIM-13 software facilitates analysis of images of mask defects at 250x, 500x or 750x total magnification. It is used to predict defect printability and the effect on the process window for resist exposures. Operation of RIM-13 is fully automated. The only operator intervention required is to load a SMIF pod containing the mask into the receptacle on the front of the tool. The analysis software automatically commands the tool to acquire all images necessary for a given analysis without specific commands from the operator.

In this paper, we present recent results from imaging patterned EUV masks in the RIM-13. We show analysis, using the tool software, of the aerial images generated. Further, we use this software and other analysis techniques to derive the key tool performance parameters such as imaging resolution, magnification, stability, etc.

6349-98, Poster Session

The study of chromeless phase lithography (CPL) for 45-nm lithography

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Chromeless Phase Lithography (CPL) has been used to achieve high resolution by using phase edge interference in addition with high NA and off-axis illuminations such as annular and quasar for sub-wavelength lithography. There are two types of CPL. One is the totally chromeless type and the other is the zebra chrome pattern type for critical line dimensions. Both CPL masks require adding in chrome pads in some structures such as circuit line junction region to improve the resolution. Zebra type CPL mask making has reached the limitation due to small chrome peeling issue during mask cleaning and small space writing resolution issue for sub-45nm technology. In this paper, two types of CPL mask are studied. The investigation shows the differences on mask making and wafer performance. For mask making, process limitation studies such as writing, etching and cleaning will be evaluated. Data on mask CD performance, registration, overlay, phase and transmission are collected and analyzed. For wafer performance, process window comparison, CD through pitch, MEEF and linearity will be characterized for these two CPL mask types. Minimum resolution of less than 160nm pitch with reasonable good process window has been achieved with both mask types. Chromeless type has advantages on mask making while zebra type has the advantages on wafer performance. Further more, assist features are added to improve process windows. Detailed characterization work done on assist features are presented. Assist feature can improve process window by improving the contrast of iso lines.

6349-99, Poster Session

A novel approach for hot-spot removal for sub-100-nm manufacturing

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Recent advances in lithography simulation have made full-chip lithography rule checking (LRC) practical and even mandatory for many fabs, especially those operating with a half-pitches under 100nm. These LRC checks routinely identify marginal or even fatal manufacturability problems (hot-spots), especially when simulated through process corners.

Until recently, when hot-spots were identified, the only options were to reject the tapeout for additional layout modifications, re-run OPC with a different recipe, or use a DRC-tool to do “blind” cut-and-paste repairs under the assumption that making the fatal errors non-fatal is sufficient to make them “good.”

Using a commercial LRC tool we will inspect OPC data on production products to identify a typical volume of real and potential hot-spots. Next, using Halo™-Fix from Aprio Technologies, we will apply local repairs, choosing rule-based or model-based repairs as appropriate for each type of hot-spot. Using this method, “intelligent” changes in the hot-spot areas can be made which accurately account for lithography interactions and process variations, in order to optimize for manufacturing robustness.

To verify that the repairs are acceptable, LRCs will be performed and the results analyzed.

6349-100, Poster Session

A novel Alt-PSM structure: isn’t this embedded atten-PSM?

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A novel mask structure for an Alt-PSM, the effectiveness of which has been confirmed by optical image calculations, is proposed. The mask is essentially the same as a tri-toned embedded Atten-PSM. An attenuating phase-shifting aperture substitutes for a transparent phase-shifting aperture in a conventional Alt-PSM, which is laid out adjustment to a transparent non-phase-shifting aperture. By application of this mask, very fine CD-Focus characteristics for isolated line are obtained such as DOF of over 0.30um for a 50 nm width line with an optics of NA=0.82 under 248 nm wavelength. Due to the very simple mask structure, mask cost of Alt-PSM can be much reduced.

The mask pattern is designed with consulting calculated optical images. Because transmitted intensity of light electric field through an attenuating phase-shifting aperture is lower than that through a transparent aperture, width of the transparent non-phase-shifting aperture

in this structure should be set smaller. The ratio of the widths of phase-shifting and non-phase-shifting apertures is approximately equal to the inverse ratio of electric field intensities at the surface of the apertures, which are proportional to square root of transmission for the apertures. In the case of the same width apertures, the image intensity profile becomes asymmetrical, resulting in poor CD-Focus characteristic and an image shift with defocus. As other feature of this mask, the width of the attenuating phase-shifting aperture, the larger aperture in this Alt-PSM, is needed to be much smaller than exposure wavelength. For the case of large width aperture, precise symmetry in image intensity profile cannot be achieved because of an effect of difference in diffraction light distribution in pupil. It should be noted that the center of fine dark line image formed by this mask is not at the same position of the canter of a opaque line which is located between the apertures. Hence, some DA operation is needed to correct the pattern shift in a usual OPC procedure.

Imaging performance is evaluated by optical image calculations. Optical conditions are NA=0.82, sigma=0.30~0.50 and wavelength=248 nm (KrF). The transmission of attenuating phase-shifting aperture is set at 25%. To form an almost symmetrical image, the width of an attenuating phase-shifting aperture is needed to be smaller than 180 nm. Iso-Focal image slice level is varied with a opaque line width between the apertures. In preliminary evaluations, the opaque line width is set a certain value such that iso-focal image width becomes the minimum one under the restriction of resolution capability in a current KrF photo-resist. The minimum Iso-focal image CD is reduced with coherence of illumination and may become ~50 nm for sigma of 0.30. Image position shift due to defocus of ~0.2 um becomes no more than 0.2 nm even at the case of mask CD imbalance of +/-2 nm on wafer scale, which corresponds +/- 8 nm CD error on mask. Then, no much care is required to the image shift due to the asymmetry in image profile, which can be caused by mask design and fabrication error. CD-DOF of over 0.30 um is obtained for this 50 nm width image.

As a conclusion, this Alt-PSM can replace a conventional Alt-PSM in application for high-speed logic device. Because of simple mask structure and mask fabrication process, much reduction of mask cost can be expected by the application of this mask.

6349-101, Poster Session

Real-time ultra-sensitive ambient ammonia monitor for advanced lithography

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Exposure to even low parts-per-billion concentrations of ammonia during the photolithography process can lead to yield loss and unscheduled equipment downtime. At critical lithography steps, ambient ammonia can alter the photochemical properties of photoresist causing uncontrolled variation in printed wafer features. Ammonia is also photoreactive and can deposit on optical surfaces causing haze. Chemical filters are often used in these critical locations to remove airborne contamination but their lifetime and coverage cannot offer complete protection. Therefore, constant monitoring of airborne ammonia at parts-per-trillion (ppt) levels is critical to insure the integrity of the lithography process and provide insight into the dynamics of ammonia exposure.

Ammonia is known for “stickiness” - its tendency to adsorb to surfaces. Storage and release of ammonia from surfaces is strongly dependent on temperature and humidity. To measure ammonia at the ppt level, instruments must minimize the effects of changing temperature and humidity.

Picarro has developed a highly accurate, highly specific, real-time trace gas monitor that detects ammonia using Cavity Ringdown Spectroscopy (CRDS). The instrument can measure ammonia with 200 ppt sensitivity in two minutes or less with little or no baseline drift. The instrument requires no calibration standards. In addition, the spectral resolution of CRDS makes the instrument less susceptible to interference by other gas components than existing technology.

We will describe CRDS, discuss how CRDS addresses the demands of advanced photolithography for sensitivity, selectivity, and speed, and show comparative results. This work supported by U.S. Department of Energy under Contract No. DE-FG02-03ER83751.

6349-103, Session 13

Qualitative analysis of haze defects

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Time-dependent haze defects have been serious issues for the manufacturing of masks with smaller features in the semiconductor industry. While there are many factors contributing to the formation of haze defects, the sulfate ion (SO42-) left on the mask surface after the conventional SPM cleaning step is known the most important root cause for the haze defects. Following cleaning by the SC1 solution helps remove residual sulfate ions from the mask surface as ammonium ions (NH4+) in the SC1 solution neutralize sulfate ions (SO42-) on the surface to form ammonium sulfate salts that are readily soluble and removed in the following DIW rinsing step.

For the PSM mask, on the other hand, the SC1 cleaning step cannot be applied since ammonium hydroxide (NH4OH) in the SC1 solution dissolves the MoSi layer of the PSM mask, which renders the PSM mask more susceptible to the haze defect formation.

Therefore, SPM-free cleaning strategy such as ozonated water has been adopted for the cleaning of PSM mask. We performed the cleaning of a PSM mask using ozonated water instead of SPM solution and then the haze acceleration test using ArF haze accelerator. This test reveals that haze defects can be formed and grown even while there are no sulfate ions or ammonium ions on the mask surface. The comprehensive analysis of the surface using TOF-SIMS signifies that the defects mainly consist of hydrocarbons, Na, K, Cl, F, Mg, Al, etc. that probably comes from fab environments, storage materials, handling steps, or pellicle materials.

This fact implies that exclusion of sulfate ions or ammonium ions from the mask surface is not enough for the realization of the haze-free PSM mask. In addition, complete removal of residual hydrocarbons deposited through previous procedures and perfect protection against environmental contaminants from fab air, storage materials, handling steps, or pellicle materials should be further accomplished.

6349-105, Poster Session

Haze detection and haze-induced process latitude variation

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Each generation of semiconductor device technology drives many new and interesting resolution enhancement technologies (RET). As minimum feature size of semiconductor devices have shrunk, the exposure wavelength has also progressively shrunk. The 193 nm lithography for low-k1 process has increased the appearance of progressive defects on masks often known as haze or crystal growth. Crystal growth on a mask surface has become an increasing issue as the industry has adopted a 193 nm wavelength in order to increase lithographic resolution and print ever decreasing device line width. Haze is known to be a growing defect on photomask as a result of increased wafer lithography exposure and photochemical reactions induced by combination of chemical residuals on the mask surface.

We build experimental system to create and detect the haze growth. A photomask is enclosed in a glove box where the atmosphere and exposure conditions are controlled and monitored throughout the exposure processing. A test photomask is exposed to accumulate the dose of laser radiation. And then spectroscopic ellipsometry and AFM techniques are used to check the surface conditions of the masks before and after the laser exposure. We found that spectroscopic ellipsometry measurement value del and psi were changed. The results of the spectroscopic ellipsometry analysis show the change of the haze thickness on mask surface. Thickness and roughness of the mask surface is increased with the exposure. This means that haze grows on the mask surface by the exposure. Masks become useless due to transmission loss or defect generation, which is directly related to the formation of the haze. The haze causes the increase of mask thickness, transmis-

sion drop and affects the formation of pattern. So, we investigated the linewidth variation and the process window as a function of haze size and position effects with Solid-E of Sigma-C.

6349-106, Poster Session

Nonchemical cleaning technology for sub-90-nm design node photomask manufacturing

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Cleaning chemistry residue in photomask manufacturing is one of route causes to generate HAZE over surface of photomasks for 193nm and shorter wavelength exposure tools. In order to reduce the residue, chemical free process is one of targets in photomask industry. In this paper novel clean technology without sulfuric acid and Ammonia chemical are shown to manufacture sub-90nm node photomasks. Photo and E-beam resist were removed by plasma and O3/DI water clean instead of sulfuric acid. SPM and APM in final clean sequence before defect inspection were substituted with O3/DI water and H2/DI water respectively. The clean performance was demonstrated in real production of 193nm phase shift mask. Sulfate and Ammonia residue after final clean were controlled same as blank material level without any clean process.

6349-109, Poster Session

Novel cleaning techniques to achieve defect-free photomasks for sub-65-nm nodes

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The ability to eliminate the critical source of haze contamination which can derive from the cleaning chemistry residues and mass production environment has become a major challenge for 193 nm photolithography in semiconductor industry. Furthermore, as the specification for photomask becomes tighter, it is getting harder and harder to eliminate particles with both minimal surface damage and preservation of photophysical properties. Recently, interest in these area continues to produce a strong demand for advanced cleaning techniques. Herein, we design for the smart cleaning strategy to achieve the defect-free photomask as a concern of above current issue with a combination of well-known cleaning technology, such as using the collective effects of functional water (i.e., ozonated water and hydrogen water, .. etc.) for the alternative to piranha, and UV/O3 treatment for the increase of surface wettability and removal efficiency for organic residues. As well as the final cleaning process, it is potentially a rational strategy that judicious modifications of inter- and intra- process sequences and conditions are applicable to individual mask process. Specially, that kind of view is focused on the post-development process which mainly occurred the source of fatal defects on the mask, such as pattern bridge following dry etch process. In this paper we propose a conceptually novel cleaning strategy for the elimination of potential source of haze formation and particle during individual process cleaning and final cleaning.

6349-110, Poster Session

Cleaning of MoSi multilayer mask blanks for EUVL

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Extreme ultraviolet lithography (EUVL) is being considered as the enabler technology for the manufacturing of future technology nodes (30 nm and beyond). EUV mask blanks are Bragg mirrors made of Mo and Si bilayers and tuned for reflectivity at a wavelength * ~13 nm. Implementation of the EUVL requires that the mask blanks be free of defects at 30 nm or above. However, during deposition of MoSi multilayers and later by handling of blanks, defects are added to the blank. Therefore, the cleaning of EUV mask blanks is a critical step in the manufacturing of future devices. The particulate defects on the multilayer-coated mask blanks could either be embedded in or under the MoSi layers or adhered to the top capping layer during the deposition process. The defects can also be added during the handling of photomasks. Our previous studies have shown successful removal of the handling-related defects at SEMATECH's Mask Blank Development Center (MBDC) in Albany, NY. However, cleaning of embedded and adhered defects presents new challenges. The cleaning method should not only be able to remove the particles, but also be compatible with the mask blank materials. This precludes the use of any aggressive chemistry that may change the surface condition leading to diminished mask blank reflectivity. The present work discusses the recent progress made at SEMATECH's MBDC in the cleaning of backside Cr-coated mask blanks, with a MoSi multilayer and a Si cap layer on the top surface. Here we present our data that demonstrates successful removal of sub-100 nm particles added by the deposition process. Surface morphology and defect composition on the surface of the MoSi multilayer is discussed. EUV reflectivity measurements and atomic force microscopy (AFM) images of the mask blank before and after cleaning are presented. The present data shows that no measurable damage to the EUV mask blank is caused by the cleaning processes developed at the MBDC.

6349-112, Poster Session

Study of reticle haze

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It is well known that reticle haze becomes a big issue of yield management at 193nm lithography. Reticle haze is caused by various factors such as reticle cleaning, pellicle, shipping case, environment etc.

It was found that organic-haze formed in early stage of exposure.

We evaluated focusing on reticle shipping conditions, and several materials were compared to minimize defects formation.

6349-113, Poster Session

Mechanism of megasonic damages for micro-patterns

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Megasonic damage is one of major problem for micro pattern cleaning. Thus far it is thought that no cavitation occurs in a liquid radiated by megasonic. However, the experimental results suggesting cavitation can occur by megasonic have been recently reported. Therefore cavitation would be one of cause of megasonic damages for micro pattern. And, to clarify the mechanism of micro pattern damage by megasonic from the information is required in order to improve process yield and cleaning tools. In this study, we will report a new calculation model, which was derived from examining the results of micro pattern damages by megasonic. The model was well corresponding to the experimental results and suggested that damage by megasonic would occur stochastically.

6349-114, Poster Session

A novel photoreactive surface processing system

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A novel dry cleaning system that uses reactive gas mixtures and laser radiation to remove organics from IC wafers is described in this paper. The gas phase photochemical mechanisms employed in this system are fundamentally different from typical ultraviolet photoionization reactions because it uses wavelengths from the near visible regions of the electromagnetic spectrum with a lower energy-per-photon.

Low energy-per-photon reactions are less damaging to the substrate surface than prior art, short wavelength, high energy-per-photon processes. AFM and XPS analysis confirm that the XLC-100 system removes photoresist layers without causing damage to the silicon substrate. AFM data is taken internally and at outside analytical houses; a typical control value is 1.54×, and a typical result after resist removal is

2.43×. Samples for XPS analysis show typical control values of 3.77×, and sample values of 4.26×.

Other potential applications for this technology include photoresist removal from low-K films, removal of ion-implanted photoresist, UV curing, cold annealing, laser assisted deposition, and laser-assisted etching.

The goal of the project was to develop a dry photoresist removal process, implemented in a robust tool with low cost of ownership. It was also specified that the process be compatible with new technologies, such as easily damaged low-K films and ultra-thin gate oxides.

This paper summarizes the data from numerous experiments conducted over a two-year period. In order to achieve statistical significance, several hundred wafers were cleaned with the XLC-100 and analyzed for carbon residue and surface damage. The laser/gas system is described along with basic operating principles and an explanation of the photochemical mechanisms. Test data and analytical results are presented along with conclusions and plans for future work. Several patents are pending on both the process and the apparatus used in these experiments.

6349-115, Poster Session

An effective layout optimization method via LFD concept

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As the advent of advanced process technology such as 65nm and below, the designs become more and more sensitive to the variation of manufacturing process. Though the complicated design rules can guarantee process margin for the most layout environments, some layouts that pass the DRC still have narrow process windows. An effective layout optimization approach based on Litho Friendly Design (LFD), one of Mentor Graphics' products, was introduced to enhance design layout manufacturability. Additional to process window models and production proven Optical Proximity Correction (OPC) recipes, the LFD design kits are also generated and needed, which with the kits and rules people should guarantee no process window issues in a design if the design passes the check of these rules via the kits. Lastly, a real 65nm product was applied full chip OPC and post-OPC checks to process variation. Some narrow process window layouts were detected and identified, then optimized for larger process window based on the advices provided by LFD. Both simulation and in-line data showed that the DOFs were improved after the layout optimization without changing the area, timing and power of the original design.

6349-116, Poster Session

Bringing the GDSII to silicon flow into design to improve design manufacturability

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As the semiconductor manufacturing industry continues to aggressively move deeper and deeper into the sub-90nm gap, and despite the advanced RET techniques extensively used, the printability problems due to RET, OPC and lithography is growing, impacting factory throughput, time-to-market, process window, and yield. The problem is in the design as much as in manufacturing and current DFM solutions, mainly applied post-tape-out, did not explore enough the flexibility which is inherent to design. On the contrary, because of our inability to predict and check the manufacturability throughout design, the industry is starting to over-constrain the design by using radical design rules.

In this paper, we first describe what makes some layouts manufacturing-unfriendly and what are the evolutionary techniques used to check design printability during or before manufacturing.

Then, we outline an innovative solution that enables manufacturing teams to capture the GDSII to silicon on a compact model, enabling design teams to analyze the manufacturability of the design before committing expensive resources to apply RET and manufacture the masks. We report quantified results on the prediction accuracy and runtime of our methodology based on real 90nm and 65nm customer designs.

We will describe how this model can be applied to check the manufacturability of designs, from cells level to full-chip.

We expect to be in a position to have a customer as co-author of this paper.

6349-117, Poster Session

Adding grayscale layers to chrome photomasks

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Recent work has shown that bimetallic films, such as Bi/In and Sn/In, can be used to create laser direct-write grayscale photomasks. Using a controlled laser induced oxidation process, bimetallic films may be made transparent with controllable variations in optical transparency, with >3OD or 0.1% transmittance for unexposed and <0.22OD or 60% transmittance for fully exposed areas. A novel grayscale photolithography technique is presented that utilizes conventional chrome-sputtered photomasks as the pattern defining layer, along with a bimetallic thin film layer deposited on top as the grayscale defining layer. This paper also presents a comparison between traditional grayscale chrome halftone photomask photolithography and combined conventional chrome with laser direct-write bimetallic grayscale photolithography.

First, bimetallic thin films such as Bi/In and Sn/In, with thickness from 40 to 120 nm, are DC-sputtered on the pre-patterned 5" chrome photomask. Both Bi/In and Sn/In showed excellent adhesion to chrome in tape-adhesion tests. The masks were raster-scanned with grayscale patterns using a 488/514 nm CW argon laser on an X-Y table. Grayscale patterns can be produced to match the underlying patterned chrome layer. Laser power and bimetallic thin film thickness were carefully calibrated to ensure that no chrome ablation or conversion occurs and only the bimetallic thin film layer is converted. From these results, the bottom chrome layer, which defines the fine features of underlying patterns, remains unchanged and the bimetallic thin film layer is converted during laser scanning to provide grayscale depth. At high laser power, chrome behaves somewhat like the bimetallic thin films and begins to turn transparent.

Using our bimetallic Sn/In/Cr photomasks, 3D grayscale micro-optics structures have been successfully fabricated in SU-8 photoresists ranging from 60-100 μm in thickness. A standard UV contact mask aligner is used to expose the photomask patterns onto the SU-8. Initial results shows variations in step height from 10-100 microns can successfully be reproduced using this bimetallic grayscale chrome photomask and SU-8 photoresist process. Further measurements are being carried out to more precisely relate 3D structures to gray levels, with the goal of fabricating steps, V-grooves, and microlenses, with 256 gray level mask patterns.

From these preliminary results, a combined Sn/In/Cr grayscale mask is being designed to compare the grayscale performance between chrome halftone and bimetallic gray level photomasks. In the final paper, masks with 16 to 64 grayscale levels patterns will be created on both the chrome halftone and our bimetallic chrome mask. An I-line stepper will be used to expose the underlying photoresist and resulting 3D structures will be used to compare the quality of the two grayscale methods. By introducing this novel combined chrome-bimetallic mask, the fine detail features found in binary lithography may be combined with smoothly-varying 3D microstructures best suited to grayscale methods.

6349-198, Poster Session

Poly-silicon gate and poly-silicon wire CD/EPE defect detection and classification

B. Su, W. W. Volk, X. Li, S. Chen, H. Du, S. D. Andrews, B. Kumar, R. Pulusuri, KLA-Tencor Corp.

As technology advances towards 45nm node and beyond, optical lithography faces increased challenges and resolution enhancement techniques (RET) are imperative for multiple process. With RET implementation and optical proximity correction (OPC) techniques, the mask layout deviates further away from design intended layout. For an OPC

decorated design database, it is important that before making mask, the OPC is verified that it is design related defects free and provide reasonable process window for a given process to ensure manufacturability.

For poly-silicon gate layer, due to tight CD control requirement, the demand for accurate lithography process simulation is even greater. As hyper-NA immersion exposure systems become available, accurately simulate resist image with mask topography effects and partial polarized illumination, at poly-silicon gate layer is a necessary. In this work, we will show simulation results of DesignScan on an advanced poly-silicon gate layer using a logic based customer database. Active layer database is used to separate poly-silicon gate regions and poly-silicon wire regions. Sensitive CD and edge placement error (EPE) detectors are used to identify design related defects. The detector sensitivities can be adjusted based on feature sizes and their natures (gate or wire). In addition, process window inspection will show how CD/EPE changes as functions of exposure dose and defocus. Accurate process window assessment using CD variation is obtained.

6349-118, Poster Session

Chrome etch challenges for 45-nm and beyond

I. M. Ibrahim, M. Chandrachood, M. N. Grimbergen, E. Gabriel, X. Chen, A. Kumar, S. J. Panayil, Applied Materials PPC

Requirements to meet the 45nm technology node place significant challenges on Mask makers. Reticle Enhancement Techniques (RET), employed to extend optical lithography in order to resolve sub-resolution features, have burdened mask processes margins. Also, Yield compromises loom with every nanometer of error incurred on the Mask and the Device platforms. RET techniques, such as Optical Proximity Correction (OPC), require the Mask Etcher to achieve exceptionally tight control of Critical Dimensions (CD). This ensures OPC feature integrity on the mask and resultant image fidelity of OPC structures, as well as, subsequently high and sustainable yields.

In this paper we will discuss Applied Materials Tetra IITM Single DigitTM capability and its ability to deliver the industry's lowest CD Bias. The effects of pressure and temperature as process tuning parameters and the role of bias power in subduing the CD etch bias to <10nm, are discussed. This capability of exceptionally low CD non-uniformities (CDU's) over a wide range of chrome global loads enables the requirements of 45nm technology node to be met at a reasonable R&D and production cost.

6349-119, Poster Session

Quartz etch challenges for 45-nm phase-shift masks

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One means of extending the limits and lifetime of current lithography platforms for 45nm and beyond is the development of resolution enhancement techniques (RET), in the form of optical phase-shifting masks (PSM). By employing optical interference from 180° shifted lithography emission, PSM masks are able to enhance feature resolution at the wafer. This is particularly important for sub-wavelength features (i.e., features with critical dimensions less than the lithography wavelength) where line resolution can be severely degraded without such techniques. For these PSMs, the challenge is to provide highly uniform quartz etch performance across the entire active area of the mask for various feature sizes and load distributions. Micro-loading (a.k.a. RIE lag or reactive ion etch lag) and phase angle range are key performance parameters to control. As the demands for these parameters tighten and mask costs rise, strict performance control is required for all PSM mask varieties utilized in the mask shop.

In this paper we will discuss process improvements for the Chromeless phase lithography (CPL) etch application, on the Applied Materials Tetra™ II Mask Etcher. In particular, the discussion will focus on process improvements in phase uniformity and RIE lag for chrome hard mask (resistless) CPL etch process. Results from modifications to the etch process, including a comparison between optical and AFM uniformity measurements, are presented. Feature profiles are also discussed with examples showing straight sidewalls and no micro-trenching.

6349-120, Poster Session

Multi-layer resist system for 45-nm-node and beyond, Part III

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Precise CD controllability will be required in 45nm-node photomask manufacturing. To achieve CD specifications for the 45nm node photomasks, the improvement of dry-etching process is necessary, because CD quality depends on dry-etching performance. Especially global and micro loading effects strongly affect the CD shift of proximity and linearity pattern in chrome etching process.

These loading effects are caused by several components such as radical contribution, charging, desorption rate of bi-products, reattachment of decomposed bi-products and so on. Generally, among these causes, it is thought that influences of radical and charging are relatively large, and usually it is considered that higher anisotropic dry-etch condition could reduce these influences. However, the etch selectivity of the chrome to the resist is a bottleneck, and, furthermore, applying a thicker resist is not the solution here, because it results in poor resolution.

To overcome this problem, a usage of a hard mask in the photomask manufacturing process has been proposed. The concept of a hard-mask seems very promising, because it has a history in the wafer manufacturing and many other fine etch applications. However, so far no film and patterning process that could be practically used in commercial photomask making was developed.

In this work, we have tried several hard mask films, which can be removed by fluorine base plasma. Specifically, MoSi, MoSiN, SiON, TaBOx and TaBNx were evaluated as hard-mask materials and their characteristics and difficulties, as well as their effectiveness, as a hard mask in photomask manufacturing will be discussed.

This work mainly focuses on hard-mask for att-PSMs, but several results for COGs will also be involved.

6349-121, Poster Session

Multi-layer resist system for 45-nm-node and beyond, Part II

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45nm-node photomask required high resolution. According to the International Technology Roadmap for semiconductors (ITRS) 2005 edition, sub-resolution assist feature is 85nm opaque feature on the reticle. However, 65nm-node technology which used the thinner new Cr and thinner resist system, will be difficult to achieve the 45nm-node requirement. For high resolution reticle, several resist makers propose the new type resist. However unfortunately, the resist which satisfied all of the high resolution, stability and sensitivity doesn't come to practical use. We need to fix 45nm-node process at least end of this year. So, we need to develop the method to improve the resolution used current resist.

Even current resist, the resolution improvement will be possible by using the bottom-insulating-layer (BIL) material technology and much thinner resist thickness combination. However thinner resist has issue of Cr Dry-etch resistance. Also, resolution and CD performance depend on the Cr Dry-etch condition. So, we developed mask-making process with the Dry-etch resistance enhancement bottom-coating (DREC).

As same purpose, the Hard Mask type Blank has been developed. However The DREC has the feature which can make the performance improve by the current Blank construction.

The DREC is the resistant material under Cr Dry-etch condition. The proximity effect caused by Dry-Etch was improved about 50%.

In this paper DREC performance and making-process will be described. Finally, DREC will be evidenced as effective method on 45nm-node mask-making.

6349-122, Poster Session

Current status of Mo-Si multilayer formation in ASET for low-defect-density mask blanks for EUV lithography

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Defect-free masks are critical to the use of extreme-ultraviolet lithography (EUVL) for the high-volume manufacture of LSIs. To make low defect-density mask blanks with Mo-Si multilayers, we have developed a sputter deposition system that can employ either ion-beam sputtering (IBS) or magnetron sputtering (MS). [1] The substrate-target configuration that was found to be most effective in reducing the number of defects in a Mo-Si multilayer is one in which the surfaces of the substrate and target are both aligned vertically (that is, parallel to the direction of gravity). For both IBS and MS, the defect count for 40 Mo-Si bilayers reached a value as low as 1 defect/cm2 for a PSL equivalent size of 70-120 nm, as measured with a laser beam scanning machine (Hitachi LS-6500).

Another essential characteristic of a Mo-Si multilayer mirror for mask blanks is a high reflectivity in the wavelength range of 12-15 nm. We analyzed Mo-Si multilayers formed by IBS and MS using transmission electron microscopy (TEM) and Rutherford back-scattering (RBS) measurements. The results showed that the interface layer (0.5-1.5 nm thick) arising from the intermixing of Mo and Si atoms during coating degrades mirror reflectivity. We speculated that the cause of its formation was the damage due to the bombardment of the substrate with high-energy particles. To reduce its thickness, we tried using Xe rather than Ar as the sputter gas in IBS because Xe is reflected from the target at lower energies. However, TEM revealed no reduction in the thickness of the interface layer. This suggests that the formation of the interface layer is related not to the sputter gas, but to bombardment by the sputtered particles themselves. A comparison of Mo-Si multilayers formed by IBS and MS showed that the interface layer was 30-50% thinner for MS than for IBS. [2] This is why the EUV reflectivity of our Mo-Si multilayer mirrors is 1-2% higher when they are formed by MS rather than by IBS. Using MS, we have achieved an EUV reflectivity as high as 66% for a mask blank with a 60-bilayer Mo-Si mirror while keeping the defect density low.

In the conference, we will describe our advanced technology for the formation of multilayers for mask blanks, including a new coating process that involves surface treatment with an assisted ion beam (AIB).

Acknowledgement: This work was supported by the New Energy and Industrial Technology Development Organization (NEDO), Japan.

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6349-123, Poster Session

Predicting the influence of trapped particles on EUVL reticle distortion during exposure chucking

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The stringent error budget for Extreme Ultraviolet Lithography (EUVL) requires identifying, understanding, and minimizing all sources of image placement (IP) errors. One potential source of IP error is the entrapment of particulates between the chuck and the mask during exposure chucking. Structural deformation of the mask due to particle entrapment during electrostatic chucking causes both in-plane and out-of-plane distortion (IPD and OPD) of the pattern surface and directly contributes to wafer-level IP errors. It has been shown that an effective particle size of 40 nm causes a pattern placement error of approximately 1 nm at the wafer level [1]. Although pin chucks have been proposed as a means of minimizing particle entrapment, experimental results suggest that particles may still reside on the pin surfaces, resulting in mask distortion [2]. Experimental assessment and numerical simulations of the response of the reticle/chuck system to entrapped particles is necessary to understand and mitigate this problem. In the current work, finite element (FE) analyses have been conducted to simulate the effect of particles being crushed and/or embedded between an electrostatic pin chuck and the backside of an EUVL mask.

The crushing and/or embedding behavior of a particle can differ depending on the location of the particle relative to a pin. For instance, a particle located on the top of a pin could have a significantly different effect than one located between two pins. Furthermore, the presence of a metal layer (to facilitate chucking) on the backside of the reticle and a dielectric coating on the top surface of the chucks can have a significant influence on the crushing characteristics of the particle. Finite element simulations were developed to simulate elastic-plastic deformation of particles located either on the pin top surface, between the pins, or lodged against a pin, under typical clamping conditions. Parametric studies have been performed on the crushing/embedding behavior of particles of different material types and sizes to identify desirable backside layer material characteristics, as well as the optimal backside layer thickness. The FE simulation results are currently being used to facilitate the design details of the EUVL electrostatic pin chuck, specifically the height, shape, and spacing of the pins.

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6349-124, Poster Session

Experimental verification of finite element model prediction of EUVL mask flatness during electrostatic chucking

M. Nataraju, J. Sohn, A. R. Mikkelson, K. T. Turner, R. L. Engelstad, Univ. of Wisconsin/Madison; C. K. Van Peski, SEMATECH, Inc.

Stringent flatness requirements have been imposed for the front and back surfaces of Extreme Ultraviolet Lithography (EUVL) masks to ensure successful pattern transfer that satisfies the image placement error budget. During exposure, an electrostatic chuck will be used to support and flatten the mask. The EUVL Mask and Chucking Standards, SEMI P-37 and SEMI P-40 [1,2], specify the flatness of the two mask surfaces as well as the chucking surface to be within 50 nm peak-to-valley (p-v). It is critical that the electrostatic chucking process and its effect on mask flatness be well-understood. The current research is focused on the characterization of various aspects of electrostatic chucking through advanced finite element (FE) models and experiments.

The FE models that were developed previously used flatness measurements of the mask and the chuck to predict the final flatness of the pattern surface [3]. These models used a uniform pressure of 15 kPa to simulate electrostatic chucking. The modeling results were compared against experimental chucking data using an electrostatic pin chuck [4]. In this work, there were cases for which the predicted and the experimental as-chucked shapes were similar; however in some instances, the model and experimental results did not agree [4]. In the current work, to obtain better predictability, FE models have been developed to include the effect of the nonuniformity of the electrostatic forces due to the nonuniform gaps between the backside of the mask and the chucking surface. These models also account for the pin characteristics. Elec-

trostatic chucking experiments have been performed in a clean room, within a vacuum chamber mounted on a vibration isolation cradle, to minimize the effects of particles, humidity and static charges. During these experiments, the chuck was supported on a 3-point mount; the substrate was placed on the chuck with the backside in contact with the chucking surface. A Zygo interferometer was used to measure the flatness of the substrate before and after chucking.

The FE models have been validated by experiments and have been used for a comprehensive analysis of the effects of chuck stiffness, chuck and mask initial nonflatness, pin material, size and location. These results will expedite the design of electrostatic chucks and the development of the SEMI standards.

[1] SEMI P37-1102, SEMI Standard Specification for Extreme Ultraviolet Lithography Mask Substrates.

[2] SEMI P40-1103, SEMI Standard Specification for Extreme Ultraviolet Lithography Mask Substrate Chucking.

[3] M. Nataraju, A. R. Mikkelson, J. Sohn, R. L. Engelstad, and E. G. Lovell, "Electrostatic Chucking and EUVL Mask Flatness Analysis," Proceedings of the 25th Annual BACUS Symposium on Photomask Technology, SPIE, Vol. 5992, 2005.

[4] M. Nataraju, J. Sohn, A. Mikkelson, K. Turner, R. Engelstad, and C. Van Peski, "EUV Mask and Chuck Analysis - Simulation and Experimentation," Proceedings of Emerging Lithographic Technologies X, SPIE, Vol. 6151, 2006.

6349-125, Poster Session

Evaluation of bi-layer TaSix absorber on buffer for EUV mask

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In order to make EUVL mask practical, it is essential to establish defect inspection and repair techniques. Since EUVL mask is a kind of reflective type mask, reflective light, typically DUV laser light, is used for inspection process, also. In addition, EUVL mask before inspection process is characterized as that there lies a stack of layers composed by buffer, capping layer, and Mo/Si multi layer, under absorber layer to be inspected, successively repaired. We have investigated feasible study of bi-layer absorber made by Ta based material added by Si. In this paper, we present evaluation results of fine patterning, defect repair, and/or inspection performance of bi-layer TaSix absorber on a buffer layer. The buffer layer we tried was a novel one, repair tools was used FIB and/or EB ones. Inspection wavelength was used 257nm laser. We estimated Ga ion concentration in buffer layer implanted by FIB repair process, according as repair conditions such as acceleration voltage, ion dosage. Consequently, we confirmed vertical cross-sectional profile, good CD accuracy, and good repair features of bi-layer TaSix absorber on the buffer, which are promising results to apply them to 32nm node EUVL mask fabrication.

6349-126, Poster Session

Measuring force uniformity in electrostatic chucking of EUVL masks

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Electrostatic chucks (ESCs) will be used to support and flatten extreme ultraviolet lithography (EUVL) masks during exposure [1]. Characterizing and predicting the capability of electrostatic chucks to reduce mask nonflatness to meet the required specifications are critical issues. Previous research has assumed that the electrostatic force is uniform over the entire chucking area; however, unexplained results in chucking experiments suggest this may not be the case [1]. Quantifying the spatial nonuniformity in electrostatic force is critical to understanding and modeling the electrostatic chucking of masks in EUV systems.

In the current work, a wafer with lithographically defined mesas is used to measure the electrostatic force locally across a chuck. When the mesa wafer is electrostatically chucked, voids form around the mesas. The size of the void is a function of the geometry and elastic properties of the chuck, wafer and mesa as well as the electrostatic pressure. As the geometry and elastic properties of the wafer and chuck are known, the electrostatic pressure can be determined from measurements of void size using an analysis similar to that developed for particle-induced distortions in EUVL reticles [2]. Two 200-mm wafers were fabricated with 3 ×~ 3 and 4 ×~ 4 arrays of mesas. The individual mesas were 1 ×~ 1 mm2 and 0.5 μm thick. The wafer was chucked on a slab ESC, and surface profiles that allow the void size to be determined (around the individual mesas) were measured using a large area Zygo interferometer. The electrostatic pressure was then calculated from the measurements of the void radius for each mesa using analytical and finite element (FE) models.

This is a novel approach to measuring the spatial nonuniformity of electrostatic pressure during electrostatic chucking, providing information about the clamping characteristics that is not otherwise attainable. The concept can be utilized on either flat-slab or pin-type chucks. Experimental and numerical results are currently being used to facilitate the design and implementation of an electrostatic pin chuck for EUV, but the methodology could be applied to wafer chucking as well.

[1] Nataraju, J. Sohn, A. Mikkelson, K. Turner, R. Engelstad, and C. Van Peski, "EUV Mask and Chuck Analysis - Simulation and Experimentation," Proceedings of Emerging Lithographic Technologies X, SPIE, Vol. 6151, 2006.

[2] R. Tejeda, R. Engelstad, E. Lovell, and K. Blaedel, "Particle-induced Distortion in Extreme Ultraviolet Lithography Reticles During Exposure Chucking," Journal of Vacuum Science and Technology B, Vol. 20, No.,6, Nov/Dec 2002.

6349-127, Poster Session

Dependency of EUV mask defects on substrate defects

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Extreme ultraviolet (EUV) mask blanks must have nearly zero defects larger than 30nm. Mask blank defects are an accumulation of defects present on the substrate, defects added during the multilayer (ML) deposition process, and defects added by handling of the mask blank. Data obtained in SEMATECH's Mask Blank Development Center (MBDC) show a majority of the detectable defects are already present on the substrate before the ML deposition. However, there are very few detectable defects on the substrate before the ML deposition. This raises the question of whether the substrate's surface condition will contribute to the total number of defects on the mask blank. Here we present the results of investigations on the relation between the total number of defects on the multilayer and the substrate surface condition. The final surface condition is determined by the mask cleaning process. We will present correlation studies between defect maps before and after multilayer deposition and will discuss the relation between final defect size on the multilayer and substrate. MBDC has a unique capability to characterize the surface of EUV glass substrates by atomic force microscopy (AFM), scanning electron microscopy (SEM), surface energy measurement, and zeta potential metrology. We have performed a series of experiments in which different cleaning processes were used to modify the substrate surface condition before multilayer deposition. Our results indicate that although there is a direct relationship between the number of defects remaining on the substrate and mask blank defects after multilayer deposition, the variation of the total number of defects on the mask blank mainly corresponds to the quality of the incoming substrate and not the cleaning processes that were used before multilayer deposition.

6349-128, Poster Session

Rigorous FEM-simulation of EUV-masks: influence of shape and material parameters

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Institute Berlin (Germany); F. Scholze, Physikalisch Technische Bundesanstalt (Germany)

We present rigorous simulations of EUV line masks with technological imperfections like side-wall angles and corner roundings. We perform an optimization of three different geometrical parameters in order to fit the numerical results to results obtained from experimental scatterometry measurements. The values obtained from this optimization fit very well to experimental results obtained by quantitative microscopy.

For the numerical simulations we use an adaptive finite element approach on irregular meshes [1]. This gives us the opportunity to model geometrical structures accurately. Moreover we comment on the use of domain decomposition techniques for EUV mask simulations [2]. The obtained results underline the necessity to model shape and material parameters in great detail.

[1] S. Burger, R. Koehle, L. Zschiedrich, W. Gao, F. Schmidt, R. Maerz, C. Noelscher, Proc. SPIE Vol. 5955, 18-26 (2005).

[2] L. Zschiedrich, S. Burger, A. Schaedle, F. Schmidt, Proc. Numerical Simulation of Optoelectronic Devices, 55-56 (2005).

6349-129, Poster Session

Adhesion measurements on mask blank surfaces relevant to EUV lithography

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For advanced optical and extreme ultraviolet (EUV) lithography, mask cleaning continues to become more and more challenging. Mask surfaces must be free of contamination, especially organic contaminants that absorb at exposure wavelengths. Furthermore, the presence of defect particles is deleterious for the lithography process. This is particularly true for EUV mask blank substrates since the negative impact of defect particles is amplified during the deposition of multilayer films required for sufficient EUV reflectance. And concurrent with the continuing scaling-down of feature sizes, smaller and smaller defect particles must be accounted for in cleaning protocols, e.g. in the sub-30 nm range. Additionally, more sophisticated cleaning protocols have to be developed which, however, must not lead to significant roughening or etching of the mask surfaces.

In light of these requirements it is necessary to carry out fundamental investigations regarding mask defects and associated removal mechanisms, specifically, the study of defect particles and their adhesion to mask surfaces. The obtained results can be used to better understand the molecular removal mechanisms for such particles. Here, we present results of a nanoscale adhesion study of EUV mask blanks, Mo-Si multilayers, and Cr-coated substrates. Employing a DI 3100 scanning probe microscope, adhesion measurements were done via a force-distance curve analysis. Commercially available silicon nitride tips with a nominal tip radius of 10 nm were used in addition to silica colloidal spheres with a radius of 500 nm attached to micromachined Si cantilevers. Freshly cleaned mask blanks relevant to EUV lithography served as substrate materials. The measurements were done in air, in de-ionized water, and in selected electrolyte solutions.

Adhesion measurement protocols in air were developed and tested to eliminate effects of static charging on insulating mask blank surfaces. These protocols incorporated an ionizing air gun operated with gaseous nitrogen. Using this approach, adhesion measurements were conducted under comparable conditions. In the case of a silicon nitride tip, the adhesion in air was found to be similar for the different substrates. Depending on the actual tip radius, the adhesion forces F were determined to be $F < 10$ nN. In the case of a silica colloid sphere, the measured forces are by a factor of about 20 higher. In particular, the adhesion for a quartz surface is the same as that for a Mo-Si multilayer with Si cap layer which points to the presence of a native oxide on top of the multilayer. In the case of Cr backside coating, the adhesion force is reduced. Using de-ionized water as well as selected electrolytes, the appearance of the force-distance curves changes, e.g. due to the presence of electrostatic double layer repulsion.

6349-130, Poster Session

Mask programmed defects for EUV mask metrology studies

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Validation and characterization of advanced and next generation metrology tools require a physical standard or physical artifact to confirm operation specifications. Often, the manufacturing of these artifacts is a challenge in itself. The technology cycle requires the metrology platform to be ready and validated earlier than the process tooling that the metrology tool will measure. For one to determine that the metrology tool is measuring the parameter of interest, early standard artifacts are required.

In the field of extreme ultra-violet (EUV) lithography, early standard artifacts are required to validate the mask defect detection metrology tooling. Extensive work in the lithography industry is being applied to get the mask blanks ready for EUV production. Defect detection of the blank and the EUV multi-layer films is very critical. To determine that the EUV defect detection metrology tooling is detecting defect types of interest, a variety of manufactureable programmed defects must be created.

This paper will describe work using focused ion beam technology to manufacture programmed defects in EUV multi-layers for EUV masks. The results will be reported. Additionally, work to simulate sidewall angles for the defects will be described and the results reported.

6349-131, Poster Session

Process development for EUV mask production

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EUVL is considered as one of the leading candidates of next generation lithography for 32nm node and beyond. EUV mask is reflective type mask. EUV mask has absorber layer, buffer layer and capping layer on reflective layer. Different absorber-buffer material combination was proposed by commercial EUV blank suppliers. Among the proposed blank with different film materials, we focused on the blank with the TaBN absorber layer and the CrN buffer layer, because we believed that the extension of conventionally used tantalum and chrome based films have advantages both in blank and mask fabrication. Top of the absorber layer was covered by low reflective layer. In this paper, we will report our results of the absorber material optimization and patterning process development for advanced quality EUV mask production.

EUV mask process needs high resolution patterning technique and pattern defect repair with precise CD control and low multilayer damage. The mask blank material and patterning process were optimized and developed to make clear these technical items.

Absorber material was optimized and EUV absorbance efficiency was increased. Using the optimized absorber material, thinner absorber layer was developed keeping sufficient EUV absorbance. Absorber layer patterning process was improved to satisfy high resolution pattern and high level CD control. To make 100nm and smaller pattern size, under 300nm resist thickness was needed because of resist pattern collapse issue. We developed absorber layer dry etching process for 300nm thickness resist. Absorber layer patterning was done by a consequence of carbon fluoride gas process and chlorine gas process. We evaluated both gas processes and made clear each dry etching character. Sufficient resist selectivity, vertical side wall, good CD control and low buffer layer damage were obtained. Finally, we evaluated how buffer layer dry etching and surface treatment after buffer layer etching affect EUV reflectivity. Sufficient capability was achieved for all properties, and we concluded that the TaBN absorber and CrN buffer would be the optimum candidate blank material for the coming generations of EUV era.

6349-132, Poster Session

Characterization of inverse SRAF for trenches on 45-nm technology active layer

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Patterning isolated trenches for bright field layers such as the active layer has always been difficult for lithographers. This patterning is even more challenging for advanced technologies such as the 45nm (C45) node where optical illumination settings, photo-resists and process conditions are chosen and optimized for the difficult requirements of minimum pitch dense lines and/or isolated lines.

Similar to the use of scattering-bars to assist isolated lines structures, we can use inverse Sub Resolution Assist Features (SRAF) to assist the patterning of isolated trenches structures.

A full characterization work has been done on the C45 Active layer to demonstrate the benefits and potential issues of this a technique:

- optical simulation to screen inverse SRAF parameters (size, distance to main feature)
- silicon process window study to check simulation expectations and ensure sufficient improvement in Depth of Focus and Exposure latitude
- accurate characterization on silicon for measurements of specific test patterns to define inverse SRAF OPC generation script parameters
- mask-shop manufacturability (CD measurements control on mask and inspection capability)
- printability study (defining when inverse SRAF start to be printed on wafer)
- C45 logic inverse SRAF implementation results and statistics

Finally, some first silicon results on a C45 project with high and hyper NA optical illumination settings are given along with conclusions for further optimization of inverse SRAFs for trench layers.

6349-133, Poster Session

Comparative study of variable rim and fixed rim approximation to 3D mask topographic effect for a single boundary layer type mask

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In this work, 3D topographic effect at hyper-NA regime is approximated using variable boundary layers of rim type. Fix rim size is being investigated in the previous works to account for the 3D topography effect assuming that single boundary layer per edge type will be sufficient to account for the process variability. In that, a single boundary layer type may be used for attenuated and binary type mask whereas two differing boundary layers may be used for alternating phase shift mask type. However, multiple edge types exist in a 2D layout with complex patterns and edge-to-edge interaction exists such that variable rim size should be utilized during optical proximity correction for enhanced performance. In this paper, a variable rim relation is defined first using 3D rigorous simulation and experimental results and then, its variable rim sizes are utilized during modeling and correction stages to achieve OPC performance required for sub-50nm half pitch device node using immersion lithography.

6349-134, Poster Session

45-32-nm node photomask technology with water immersion lithography

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As for 32-nm node (minimum half pitch 45-nm) logic device of the next generation, the leading semiconductor device makers propose the following three kinds of lithography techniques as a candidate, multi-exposure with water immersion lithography. So we will evaluate them.

In previous work, we evaluated the resolution limit and printing performance through various pitches of 45-nm node (minimum half pitch 65-nm) lithography. We evaluated the AAPSM of NA=0.93 (Dry and Immersion) and various RETs with off-axis and polarized illumination of NA=1.07(Immersion). The minimum k1 examined at previous time was 0.31 and 0.39 respectively. To achieve 32-nm node of the next generation with water immersion lithography, we must use higher NA but yet severe k1. The combination of the strong RET, polarization and multi-exposure is thought to be required. In order to resolve severe k1 (<0.3), the double patterning is thought as a most candidate technology, though the disadvantageous points will appear such as very severe alignment accuracy and the twice process of wafer. In this report, we will argue some RETs such as DDL (Double Dipole Lithography) that have sufficient printing performance through various pitches of 32-nm node as well as the double patterning. We will evaluate influence of each technique on the mask quality using optical simulation software.

6349-135, Poster Session

The effects of the photomask on multi-phase test monitors

G. R. McIntyre, A. R. Neureuther, Univ. of California/Berkeley

A series of multi-phase, phase shifting test mask patterns have been previously introduced and experimentally verified to monitor various effects in image-forming optical systems. This paper will investigate the practical limitations to these techniques, focusing primarily on the effects of the photomask.

Six novel classes of test mask patterns have been developed for in-situ characterization of polarized illumination [1] [2] [3], aberrations [4], lens birefringence [5], and mask performance [6] in optical lithography. The monitors combine knowledge of optical effects with the topography enabled by state-of-the-art phase shift masks to create patterns that are sensitive to one aspect of projection printing. Each design is believed to be theoretically the most sensitive pattern to the desired effect. A variety of experimental and simulation studies at 193nm wavelength have validated their scientific principles and have helped allow understanding of limitations due to realistic imaging conditions, most notably the electromagnetic (EM) interaction with mask topography and limitations in mask making.

After briefly introducing the concept of these monitors, this paper will focus on these relevant imaging limitations and conclusions will be drawn as to the practicality of these techniques based on experimental results from three multi-phase test reticles. Although many of these four-phase chromeless monitors are not standard topographies found in IC manufacturing, they do offer unique insight into not only the effects of the photomask on imaging, but also to how the photomask interacts with polarization and high-NA vector effects, oblique angles of incidence, partial coherence and proximity effects. By comparing thin and thick mask simulation to experimental data, the relative effects of EM interaction and mask making limitations are compared. As an example shown in Figure 1, the polarization monitors loose roughly 10-20% sensitivity due to EM effects and an additional 60-80% sensitivity due to mask making effects.

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6349-136, Poster Session

Study of chromeless mask quartz defect detection capability for 80-nm post structure

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As trench type of chrome-less mask manufacturing for post structure application down to 80nm generation node, one of the important issues is quartz defect detection capability. This study will base on half pitch 80nm (1X) design and apply different size of chrome-less mask and programming defects, all test pattern will be inspected by KLA-Tencor TeraScan Die-to-Die inspection with different de-focus setting, and check defects detection capability. All the programming defects will be simulated by Zeiss AIMS Fab-193 for wafer CD simulation. Finally we will analyze the relationship between trench size, defect detection capability and printability, and summarize the chrome-less mask quartz defect detection capability for 80nm post structure application.

6349-137, Poster Session

Single pass die-to-database tritone reticle inspection capability

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Tritone reticle designs present many challenges for both photomask manufacturers and defect inspection equipment suppliers. From a fabrication standpoint, multi-write and process steps for tritone layers add levels of complexity and increased cost not encountered with most traditional binary (two tone) masks. For inspection tools, the presence of three distinctive light levels presents a challenge for algorithms originally designed to inspect gray scale data between two tones (black and white): especially for database transmitted light modes.

While most die-to-die and STARlight™ inspections on tritone reticles produce successful results using binary algorithms, database inspections typically require two separate recipes to reveal all lithographically significant defects. With this dual-inspection technique, DNIR (Do Not Inspect Regions) are often added to eliminate the presence of third tone (typically Chrome) features: a process that adds considerable time to recipe creation. Additional workarounds when using binary inspection algorithms include implementing special light calibration techniques during setup in an effort to minimize nuisance defects caused by the presence of a third tone.

As a result of these workarounds, reticle throughput is either reduced or sensitivity compromised when using binary database inspection algorithms on tritone reticles. This paper examines the benefits of using a tritone database inspection algorithm from both productivity and sensitivity standpoints as compared to results obtained from using the aforementioned workarounds and existing binary inspection modes. The results and conclusions contained within are based on data obtained from standard test vehicles and a variety of tritone production reticles.

6349-138, Poster Session

Development of next-generation mask inspection method by using the feature of mask image captured with 199-nm inspection optics

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The usage of ArF immersion lithography for hp 65nm node and beyond leads to the increase of mask error enhancement factor in the exposure process. Therefore, wavelength of inspection tool is required to be consistent with wavelength of lithography tool. Moreover, this consistency becomes more important by the introduction of phase shift mask such as Tri-tone mask.

Then, we have developed the mask inspection system and it's inspection light wavelength is 199nm. This system has transmission and reflection inspection concurrent mode, and throughput is 2hours per mask.

We evaluated mask image captured by this system, and confirmed that 199 nm inspection wave length has advantage for Die-to- Data (D-DB) inspection compared with the system using 257 nm laser. For example, the under shoot of image (gray scale) on Arf-HT mask becomes smaller and optical resolution of scanned image, especially small defect's part, is increased. This feature makes generation of ArF-HT reference image for D-DB inspection easier.

As for the phase shift mask, the difference of gray value between the area with phase defect and without phase defect was relatively clear. D-DB inspection is required to create a high accuracy reference image from the EB data for Alt-PSM or Tri-Tone masks. However, it is difficult to improve on the accuracy of a reference image only by using one layer EB data. Then, it is effective to use two layers EB data in which the phase difference of 0 degree and 180 degree.

We have developed the reference image generation method by using two layers data and the scanned image with 199nm optics. In the case of Alt-PSM, two types of EB data, which have the differential phases such as 0 and 180 degrees, are used. Two types of data are processed using the resizing processing, corner rounding processing and PSF model, based on the filter operations. As a result, the reference image can be created through these three processes.

Tri-Tone pattern reference image can be created from the two-layer EB data such as Cr layer and HT layer,in the same manner.

In order to create a reference image similar to a scanned real image, it is necessary to determine the parameters of the reference generation model which consists of the resize, corner rounding and PSF. These parameters can be automatically calculated by using both two layer EB data and their corresponding scanned image by 199nm optics.

The effectiveness of reference image generation method using two-layer data and 199nm optics was confirmed. As for the Alt-PSM, the gray level difference between 0 degrees phase pattern and 180 degree phase patterns can be expressed well and there was almost no difference between reference image and scanned image, regardless of phase shift difference. As for the Tri-Tone pattern, the gray level difference between HT layer and Cr Layer can be expressed well. Three layer patterns such as Cr ,Ht and Qz are clearly identified.

Wavelength consistency between exposure system and mask inspection system is required so as to obtain high defect inspection sensitivity, we have developed the mask inspection system and it's inspection wavelength is 199nm. This system has transmission and reflection inspection concurrent mode, and throughput is 2hours per mask.

By the evaluation of mask image captured by 199 nm inspection system, some advantages for Die-to-Data (D-DB) inspection were confirmed. Advantages are as follows; less under shoot of image gray scale, optical resolution for small defect, the difference of gray value between the area with and without phase defect.

D-DB inspection is required to create a high accuracy of reference images created from the EB data for Alt-PSM or Tri-Tone masks. However, it is difficult to improve on the accuracy of a reference image only using one-layer EB data. To solve this problem, we have developed the reference image generation method by using two-layer data and it was realized by the use of better feature of mask image with 199nm optics.

The effectiveness of new reference image generation method was confirmed by experimental results. As for the Alt-PSM, the gray level difference between 0 degree phase pattern and 180 degree's can be expressed well and there was almost no difference between a reference image and a scanned image, regardless of phase shift difference. As for the Tri-Tone pattern, the gray level difference between HT layer and Cr Layer can be expressed well. Three layer patterns such as Cr, Ht and Qz are clearly identified.

6349-139, Poster Session

A cost model comparing image qualification and direct mask inspection

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Litho-cluster cycle time will drive the economics for fabs even harder at nodes 65nm and below. Any methods or techniques that can reduce this litho-cluster cycle time need to be looked at seriously. Besides running production, a small part of the litho-cluster time is also used to expose test wafers for mask qualification on a periodic interval. It is common knowledge that incoming mask inspections as well as periodic mask inspections (re-qualification) in advanced wafer fabs are a necessity. This can be achieved via two methods. The first method is indirect, commonly known as image qualification, where a mask is being exposed followed by the inspection of the printed wafer to detect if there is any repeater on the wafer or not. The other method of mask inspection is direct mask inspection (such as STARlight).

A lot has been written on the technical advantages of direct mask inspection over image qualification. This technical report discusses a cost model developed to compare the financial impact of image qualification to direct mask inspection like STARlight. In this model all the inspection and process tool costs are included as well as turn-around-time (TAT) at the litho-cluster for image qualification and TAT for STARlight. Then, the inspection cost and the opportunity cost (for using litho-cluster to expose test wafers other than production wafers) are combined and the net effect is compared. The goal is to find the most cost effective way to do mask qualification in advanced wafer fabs.

6349-140, Poster Session

Inspectability and printability of lines and spaces halftone masks for the advanced DRAM node

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With decreasing pattern sizes the absolute size of acceptable pattern deviations decrease. For mask-makers a new technology requires a review, which mask design variations print on the wafer under production illumination conditions and whether these variations can be found reliably (100%) with the current inspection tools. As defect dispositioning is performed with an AIMS-tool, the critical AIMS values, above which a defect is considered to print, needs to be determined.

In this paper we present a detailed investigation of inspectability of programmed defects on 2 different KLA 5xx tools employing pixel sizes of P125 and P90, respectively, and various sensitivity settings in die-to-die transmitted mode. Comparing the inspection results with the wafer prints of the mask under Disar illumination it could be shown that all critical design variations are reliably detected using a state-of-the-art tool setup. Furthermore, AIMS measurements on defects with increasing defect area of various defect categories were taken under the same illumination conditions as for the wafer prints. The measurements were evaluated in terms of transmission deviation and CD deviation. It could be shown that the AIMS results exhibit a linear behavior, if plotted against the square-root area (SRA) of the defects on the mask as obtained from mask SEM images. The strengths and weaknesses of the different evaluation techniques are discussed and it can be shown that a consistent AIMS spec can be derived for all defect categories.

6349-199, Poster Session

Mask defect inspection system using backscattered electron image

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The optical inspection system has been applied for mask inspection.

The small but fatal detects on the mask can not be detected minutely by the optical system because of the limit of optical resolution.

We have developed Defect Inspection System (DIS-05) using Backscattered electron (BSE) Image.

DIS-05 is composed of 3 units: (1) EB-Viewer with a newly developed BSE detector, (2) CAD computer to create CAD Image and, (3) Main computer to control EB-Viewer and CAD computer.

One of key technologies for DIS-05 is the method of detecting BSE Image at a high contrast.

Moreover, we herewith describe “Superimposed Image”, which compares BSE Image with CAD one.

Finally, we also report the possibility of detecting “haze on masks” using DIS-05.

6349-200, Poster Session

Optimization of development process using after develop inspection in mask manufacturing

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As the design rule continues to shrink towards 65nm and beyond the defect criteria are becoming ever more challenging. Pattern fidelity and reticle defects that were once considered as insignificant or nuisance are now becoming significant yield impacting defects. As a result After Develop Inspection (ADI) has become more important to identify where in the process the small contamination and particles are coming from. The intent of this study is to utilize KLA-Tencor’s SLF die-to-die reflected light mode and ADI algorithm for the post development resist layer inspection, ultimately identifying the defect source.

6349-141, Poster Session

The automatic back-check mechanism of mask tooling database and automatic transmission of mask tooling data

R. Xu, M. G. Peng, L. Tu, HeJian Technology Co., Ltd. (China)

Nowadays, all foundry fabs have payed more attention to reduce the CD width. With the developing of lithography technology, mask price goes up drastically, however, mask data accuracy becomes a big challenge than before. We’ve developped a system called eFDMS(Frame Data Management System) to guarantee the mask data accuracy.

EFDMS is about to do the automatic back-check mechanism of mask tooling database and the transmission of mask tooling data. We set up our own systems to engage with the standard mask tooling system(K2 Mask Compose). So that the upriver and the downriver processes of the mask tooling main body(K2 Mask Compose) should perform smoothly and correctly with anticipation.

Nowadays, the competition in IC marketplace is changed from high-tech process to lower-price gradually. How to control the reduction of the products’ cost more and more plays a significant role in foundries. Before the violent competition’s drawing nearer, we should preparing the cost task ahead of time.

6349-142, Poster Session

Distributed-computing in mask data preparation for 45-nm node and below

W. Zhang, E. Y. Sahouria, S. F. Schulze, Mentor Graphics Corp.

As we develop the technology for 45nm node and below, design data, especially after applying OPC, has exploded exponentially. OPC-ed design data volume starts to surpass 100 gigabytes in disk file size in many cutting-edge real world designs. Effectively handling this huge amount of design data poses an enormous challenge for mask data preparation (MDP), and for fracturing of the design data into mask writer formatted data, in particular. We argue that using hierarchy, directly from the original design hierarchy or re-structuring from the input design data,

and distributed-computing are the keys to solutions of the MDP challenge for 45nm node and below. Using variable shape vector (VSB) format as an example, we showed that our proposed approach will reduce the runtime, memory usage during fracturing and produce smaller VSB fractured pattern data file size. Computer experiment data show that our distributed-computing approach with near linear scalability up to more than 200 CPUs, will ensure that a VSB fracturing job can be processed in minutes or at most hours, and certainly not days.

6349-143, Poster Session

Incoming database verification and management for mask data preparation

F. Chen, Toppan Chunghwa Electronics Co., Ltd. (Taiwan)

We have developed a database verification and management system to ensure incoming database accuracy before mask data prep and optimize computing resource. The system includes incoming database check, CPU resource management and backup/restore management functions. To ensure database accuracy through pre-check function can reduce data confirmation time and prevent data prep re-work if using un-excepting database. CPU resource management function has the possibility to optimize computing resource. Backup/Restore function present automatic archive concept for data management.

6349-144, Poster Session

Parallel processing of layout data with selective data distribution

M. Pereira, M. Pereira, SoftJin Technologies Pvt. Ltd. (India)

With the increase in layout and mask data size due to finer geometries and resolution enhancement techniques such as Optical Proximity Correction (OPC) and Phase Shift Mask (PSM), layout data is proving to be too voluminous to be processed by single CPU machines. Post layout tools have now moved towards distributed computing techniques to process this data more efficiently in terms of speed. Typical distributed computing architectures involve distributing the layout data to various machines and then each machine process a part of the data in parallel. This approach will work well provided the amount of data that is to be distributed is not too large. As the sizes of the layout data is increasing significantly, the time to transfer the layout data is turning out to be a bottleneck.

The focus of this paper is on a smart way of distributing the layout data so that the amount of redundant data transfer is significantly reduced. This is achieved by selective data distribution wherein the layout data is fragmented and each machine is provided with minimal sufficient layout information for it to determine the actual fragments required for its processing.

6349-145, Poster Session

Advanced manufacturing rules check (MRC) for fully automated assessment of complex reticle designs: part II

J. A. Straub, D. Aguilar, P. D. Buck, D. Dawkins, R. Gladhill, S. Nolke, J. Riddick, Toppan Photomasks, Inc.

Advanced electronic design automation (EDA) tools, with their simulation, modeling, design rule checking, and optical proximity correction capabilities, have facilitated the improvement of first pass wafer yields. While the data produced by these tools may have been processed for optimal wafer manufacturing, it is possible for the same data to be far from ideal for photomask manufacturing, particularly at lithography and inspection stages, resulting in production delays and increased costs. The same EDA tools used to produce the data can be used to detect potential problems for photomask manufacturing in the data.

In the previous paper (Gladhill et al., 2005), it was shown how photomask MRC is used to uncover data related problems prior to automated defect inspection. It was demonstrated how jobs which are likely to have problems at inspection could be identified and separated from those which are not. The use of photomask MRC in production was shown to reduce time lost to aborted runs and troubleshooting due to data issues.

In this paper, the effectiveness of this photomask MRC program in a high volume photomask factory over the course of a year as applied to more than ten thousand jobs will be shown. Statistics on the results of the MRC runs will be presented along with the associated impact to the automated defect inspection process. Common design problems will be shown as well as their impact to mask manufacturing throughput and productivity. Finally, solutions to the most common and most severe problems will be offered and discussed.

6349-146, Poster Session

Load balancing using DP management server for commercial MDP software

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Mask data volume is dramatically increasing by using RET like OPC due to scaling design rule. This has become a burden to MDP and a barrier to TAT.

Mask manufacturers have been making various efforts to solve this problem. Although Distribute processing (DP) is one of effective solutions, there remain some limitations: DP needs a lot of CPUs and software license copies, and its management is not efficient at all.

Most of well-known mask data preparation (MDP) commercial softwares require different licenses to each format. Besides, they have no management function to deal with the entire distribute processing (DP) system, on account of which user's DP system is not in a fully dynamic state. Those who use commercial MDP software set up their DP system with CPUs fixed by the number of licenses. [Fig. 1] If user has only one license, this problem does not happen. However, most MDP users have more than one license. If a user wants the DP state which is fully dynamic, he must always consider both the number of licenses and that of available CPUs.

This is reason why we have made a DP management server which allocate MDP software to CPUs. [Fig. 2] It can prevent the loss of CPU time and automate data flow. It's operation is not complicated; effect(or function) is powerful.

In this paper, we will show advantages in using DP management server and different from other load balance tools.

6349-147, Poster Session

Mask rule checker: SmartMRC

K. Kato, SII NanoTechnology Inc. (Japan)

As patterns on photomasks are getting more complex due to RET technologies, mask rule check (MRC) has become an essential process before manufacturing photomasks. Design rule check (DRC) tools in the EDA field have been widely applied for MRC. However, photomask data has unique characteristics different from IC design, which causes many problems when handling photomask data in the same way as the design data.

In this paper, we introduce a novel MRC tool, SmartMRC, which has been developed by SII NanoTechnology in order to solve these problems and show the experimental results performed by DNP. We have achieved high performance of data processing by optimizing the software engine to make the best use of mask data's characteristics. The experimental results show that only a little difference has been seen in calculation time for reversed pattern data compared to non-reversed data. Furthermore, the MRC tool can deal with various types of photomask data and Jobdec in the same transparent way by reading them directly without any intermediate data conversion, which helps to reduce the overhead time. Lastly it has been proven that result OASIS files are several times smaller than GDS files.

6349-149, Poster Session

Advanced CD AFM metrology for 3D critical shape and dimension control of photomask etch processing

T. Bao, Veeco Instruments Inc.; A. Zerrade, Micron Technology Inc.

The critical dimension (CD) specification of photomask for semiconductor integrated circuit patterning at the 90nm node and below is becoming unprecedentedly stringent. To meet the tight ITRS roadmap requirements, reticle makers must rely heavily on advanced dimensional metrology to characterize and control the process for novel materials, new structures, and shrinking mask-enhancement features. The objective of this paper is to evaluate a new-generation atomic force microscope (CD AFM) for imaging and measuring the full three-dimensional (3D) shape of features. Cross-section sidewall profile, linewidth, and depth of etched mask features are evaluated at different steps of the mask-making process. AFM probe characterization's impact on metrology's ability to achieve a nanoscale precision and accuracy is quantified. Tip shape parameters and tip wear are evaluated for a variety of mask materials for depth, linewidth, and sidewall profile measurements. The scanning probe-based technique provides an absolute and direct measure of mask features anywhere within a plate, regardless of the material characteristics. Representative results for linewidth (CD control), depth (phase shift control), and sidewall profile (etch profile control) of etched masks are presented. The CD AFM data can help engineers better characterize, analyze, and control the process for mask development and manufacturing.

6349-150, Poster Session

Introduction of a die-to-database verification tool for mask geometry NGR4000

T. Kitamura, NanoGeometry Research Inc. (Japan); M. J. Hoffman, NanoGeometry Research Inc.

The NGR4000 system enables high precision-verification of mask geometry, by matching and comparing images of the mask geometry with its corresponding mask design data.

Effective mask analysis requires detection of both horizontal and vertical edges to be defined with high accuracy, which can be achieved using secondary electron imaging. This new technique uses a high-resolution image, and a large field of view, which is required for complex mask features. The large field of view introduces imaging challenges, such as field distortion and local area charging caused by pattern density variation. Once addressed, feature edges and mask design data can then be extracted and aligned. An analysis of the actual image vs. mask design can then be performed and analyzed for Critical Dimensions and deviation from design. Outputs of the verification include cell-based correlation of design deviation and CD's and contours of the mask feature images, which are attached to mask data and/or EB writer data in GDSII format.

The key features of the matching techniques include obtaining a 45 degree image without using interpolation, large-scale image having a minimum of 8000 by 8000 pixels, edge vector matching using unique and negative patterns, on-the-fly image distortion correction, 100MHz scan rates, and high speed calculation using a limited area of the large field of view at more than 100Mp/s rate.

Consequently, die-to-database verification tool for the mask geometry can be realized.

6349-152, Poster Session

A new algorithm for SEM critical dimension measurements for differentiating between lines and spaces in dense line/space patterns without tone dependence

J. Matsumoto, Y. Ogiso, M. Sekine, Advantest Corp. (Japan); J. M. Whittey, Vistec Semiconductor Systems, Inc.

In performing SEM Critical Dimension (CD) measurements on photomasks in dense line/space arrays it is often difficult to distinguish between whether or not a feature is a line or space. This is a result of tone shifts that occur affecting contrast on target images. The inability to reliably differentiate lines and spaces leads to inclusion of fliers or inaccurate measurements into automated measurement results. In an effort to combat this phenomenon a new algorithm has been developed to increase the robustness of the CD SEM measurements to insure reliable data acquisition. This new algorithm takes into account apparent tone reversals on a variety of today's photomask material types. This paper will detail the various elements of the new algorithm and show before and after test results showing improved recognition performance.

6349-153, Poster Session

Automate mask qualification with new CD metrology in a CATS(TM) environment

H. Boerland, R. J. Lesnick, Jr., Synopsys, Inc.

With the newer process generations, mask complexity and mask costs continue to rise, making mask qualification more complicated. It is important to know which critical items should be verified during a qualification. In addition to traditional line width and spacing measurements, advanced CD-SEM tools quantify more complex mask properties, such as corner rounding, overlay, and line-edge roughness. Another capability of these tools is the ability to do multiple measurements within one field-of-view.

In advanced mask production facilities, mask qualification recipes are usually generated offline to improve the quality and efficiency of such qualifications. Offline recipe generation has become even more important since new process generations require an increasing number of measurements per mask. This paper describes offline recipe generation procedures using CATSTM marking to utilize the new features of advanced CD-SEM.

6349-154, Poster Session

Utilize AIMS simulation to estimate profile side-wall angle

C. Lu, Photronics Semiconductor Mask Corp. (Taiwan)

In the development of leading-edge devices, high-end mask is required and the request from mask users becomes more and more tightened and complex. Mask users concern not only CD(critical dimention) uniformity, defect condition, registration/overlay, but also haze issue and better pattern profile. There are lots of items which are included in pattern profile, like line-end shortening, edge roughness, corner rounding and side-wall angle, etc. Maskshop's engineers always need to cut blanks and then get cross-section images at CD-SEM. But it wastes lots of time and money. In this paper we try to find the relationship between mask side-wall angle and simulated aerial image by using Carl Zeiss' Aerial Image Measurement System (AIMSTM-fab). For the further study, we compare three types of E-beam writers and two types of etchers to recognize its effect on side-wall angle.

6349-155, Poster Session

Multi-point CD measurement method to evaluate pattern fidelity and performance of mask

M. Kim, Y. Choi, O. Han, Hynix Semiconductor Inc. (South Korea)

As mask feature size is shrinking, required accuracy and repeatability of mask CD measurement is more severe. CD-SEM which is usually used to measure below 0.5um pattern shows the degradation of repeatability by the sparkle noise. To reduce this, larger ROI (range of interest) is recommended on line and space patterns. But this wide ROI is difficult to use on Hole or isolated patterns. In this paper, anisotropic diffusion filtering method will be introduced to replace the ROI, and evaluated on various patterns such as hole and isolated patterns. It can also reduce the effects of defocus of CD-SEM and enhance the repeat-

ability of CD-SEM. And multi-point CD measurement technique will be described to reduce the local CD errors on CD uniformity of mask which is usual on conventional one dimensional CD measurement. Using these methods, local CD uniformity and global CD uniformity of masks which is the key performance of mask quality can be measured more exactly compared to old CD measurement method

6349-156, Poster Session

Through-pellicle CDU assessment of masks at wafer level based on aerial image measurements

R. M. Schmid, E. R. Poortinga, Carl Zeiss SMT Inc.; A. M. Zibold, Carl Zeiss SMS GmbH (Germany)

Reliable prediction of wafer level CD impact of 3-dimensional mask features will play an ever more important role for the next generation technology nodes. Masks are typically delivered to wafer fabs with mask level CD characterization. However, with OPCs, PSM, complex topography, and areas with large MEEF, in addition to physical mask properties, what you see at mask level is not straight forward what you print at wafer level.

Thus we are investigating adequate wafer level characterization metrology to allow assessment of physical mask features once the masks are pellicleized, which is typically the case when they are shipped to the end users. In this paper we used current AIMS™ 193nm technology to characterize mask CD uniformity through-pellicle at the wafer level providing a new quality assurance parameter for the communication and data exchange between mask shops and wafer fabs.

AIMS™ is a metrology tool that determines printability by exposing reticles under illumination conditions identical to steppers/scanners with respect to wavelength, sigma, aperture and illumination shape and then captures magnified aerial images with a CCD at the wafer plane for further analysis. The system supports a wide range of polarization, illumination aperture, sigma and NA settings to match given stepper/ scanner equipment. Thus aerial image measurement assessment of masks inherently takes into account the physical mask properties and assesses their impact at wafer level on the one hand and allows to separate mask contributions from effects of the overall wafer process on the other hand. This technology is established as printability quality standard in all leading edge mask shops. Currently available AIMS™ systems allow wafer level CD measurements at masks with and without pellicles.

We first assessed the performance of a 193nm AIMS™ system for the 65nm node (AIMS™ fab 193i) in terms of repeatability and reproducibility and then compared CDU map type results with other characterization methods, for example mask level CDU maps generated by CD SEMs.

6349-157, Poster Session

A new critical dimension metrology for chrome-on-glass substrates based on s-parameter measurements extracted from coplanar waveguide test structures

C. A. Nwokoye, M. Zagloul, George Washington Univ.; M. W. Cresswell, R. A. Allen, C. E. Murabito, National Institute of Standards and Technology

There are several reports of the extraction of critical dimensions (CDs) from test structures replicated on chrome-on-glass (cog) masks by electrical means. The new idea being introduced here is to estimate the CDs of features by incorporating them into an rf coplanar wave guide (CPW) test structure and matching its as-measured rf-impedance to the values obtained from an e-m field solver.

The near-term objective is to assess whether a new CPW-based CD-metrology applied to features on binary COG photo-masks has sufficient sensitivity and repeatability. An affirmative answer is encouraging because advancing to a non-contact implementation at high frequencies would then seem possible.

The first task is to measure the s-parameters of the as-replicated test structure and compute from them the CPW's characteristic impedance and propagation constant. The distributed transmission line parameters resistance R, inductance L, capacitance C and conductance G, are then calculated from the measured values of the propagation constant, the characteristic impedance, and the frequency. As stated above, the relationship between signal line CD and the measured values of these four parameters can be determined from electro-magnetic (EM) field modeling so that the value of the former can be determined from the latter.

We have derived results which show the dependence of C on the CWG's signal-line CD w and its pitch s relative to the ground lines. They show that that C increases with w at constant s and decreases with s at constant w. On a qualitative basis, both of these results are expected intuitively. A key result is that the sensitivity, dC/dw with s=constant, is large enough for the purpose, although re- configuring the waveguide's architecture may increase this figure-of- merit several times.

We have also observed that the extracted parameter Z0 decreases as w increases, again, as expected. Whereas the sensitivity is not much greater than that for C, it is clear that in the implementation of this new metrology, co-reconciliation of the respective measured and modeled values of both C and Z0 would probably reduce the overall uncertainty of the extracted value of w. Similar advantages could be expected if other rf parameters such as R were incorporated into w- extraction analyses.

Although a mask to enable validation of the new CD-metrology implementation has not yet been ordered, because of the promising results, the design will be finished and a vendor will be selected during the coming month. The test structure layout will certainly be available for inclusion in the symposium proceedings and for slide presentation. All equipment necessary for a making the rf measurements is installed and operational but the only material that the authors can assure prior to the conference is limited to the modeling results. If experimental measurements become available in time, they will be included in the final manuscript, and in the slides, with associated analyses.

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6349-158, Poster Session

Revisiting mask contact hole measurements

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Contact holes represent one of the biggest critical dimension (CD) mask metrology challenges for 45nm technology mask development. The challenge is a consequence of both wafer and mask sensitivities. Large mask error factors and small process windows found when contact holes are imaged on wafers impose very tight mask specifications for CD uniformity. The resultant CD error budget leaves little room for mask metrology. Current advanced mask metrology deploys a CD-SEM to characterize the mask contact hole CD. A contact hole is a complex measurement since it is inherently two-dimensional and is not always well-characterized by one-dimensional x- and y-axis measurements. This paper will investigate contact metrics such as line edge roughness (LER), region of interest (ROI) size, area, and CD sampling methods. The relative merits of each will be explored. In addition, alternative methods of mask contact metrology such as Scatterometry will be tested.

Ultimately, an understanding of the connection between what is physically measured on the mask and what impacts wafer imaging must be understood. Simulations will be presented to explore the printability of a contact hole's physical attributes. The results will be summarized into a discussion of optimal contact hole metrology for 45nm technology node masks.

6349-160, Poster Session

Advanced edge-roughness measurement application for mask metrology

D. C. Colin, R. Katz, R. Falah, Applied Materials (Israel)

Mask Manufacturers are continuously asked to supply reticles with reduced CD (Critical Dimension) specification, such as CD Uniformity and Mean to target. To meet this on-going trend the industry is in a quest for higher resolution metrology tools, which, in-turn, drives the use of SEM metrology into standard mask manufacturing process. As dimensions of integrated circuit features reduce, the negative effects of roughness of the features, and/or of components such as photo-resist and ancillary structures used to produce the features, become more pronounced since there is no corresponding reduction of roughness with dimension reduction. As a result of the increased problems, metrics that quantify roughness of specific sections of an integrated circuit have been developed; for example, line edge roughness (LER) measures the roughness of a linear edge.

This paper continues our previous efforts on the analysis of Roughness in the field of Mask Metrology, using AMAT RETicleSEM. In order to better understand the types of Roughness and the impact of the SEM metrology tool Roughness measurement capabilities on the control of the mask process, a Roughness test mask was created. Using this mask, the sensitivity and accuracy of the Roughness Analysis were qualified, by comparing the measured mask Roughness to the design. We have also performed a precision analysis.

6349-161, Poster Session

Investigation of adhesive energy of micro-patterns for under 65-nm node

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Micro patterns on photomasks become smaller and smaller for under 65nm node. For example, SRAF patterns are typical micro pattern under 100nm width. To measure adhesive energy between the patterns and substrates is important technique for process and material design. However, as far as we know, no quantitative investigation has been reported on the adhesion measurement. In this study, we use AFMs as a measurement tool for adhesive energy and CD, and we succeeded to quantify the energy for under 100nm pattern of both Cr and MoSi on masks.

6349-162, Poster Session

Novel technique for critical dimension measurements of phase-shift masks using broadband transmittance spectra in conjunction with RCWA

A. Gray, Univ. of California/Davis; J. C. Lam, S. S. Chen, n&k Technology, Inc.

For the first time Rigorous Coupled Wave Analysis (RCWA) has been applied to the analysis of the transmittance spectra for the determination of critical dimension (CD) of phase-shift photomask. The use of transmittance spectra proved to be instrumental in improving the sensitivity of the measurement to minor (sub-nanometer) changes in the width of the trench. We present a novel unique metrology solution based on the simultaneous measurement of broadband reflectance and transmittance, covering a wavelength range from 190 to 1000 nm, in one nanometer intervals. The analyses of both types of spectra are performed simultaneously, using Forouhi-Bloomer dispersion equations, in conjunctions with RCWA. The method provides accurate and repeatable results for critical dimensions, thickness, and optical properties (n and k spectra from 190 - 1000 nm) for all materials present in the structure.

In the current study, the method described above was used to examine grating structures on ACI (After-Clean Inspection) phase-shift mask. The use of transmittance spectrum proved to be essential for the accurate measurement of the CD, since the transmittance spectrum is more sensitive to the change in line width, compared to the reflectance spectrum. The results were compared with the measurements taken on the same sample using conventional CD-SEM. The CD linearity study demonstrated excellent correlation with CD-SEM. The advantages of the optical reflectance and transmittance method are high throughput, nondestructive nature of the measurements and capability to measure a wider variety of structures pertinent to the photomask manufacturing process.

6349-163, Poster Session

Development of an actinic 193-nm phase metrology tool

A. J. Merriam, J. J. Jacob, Actinix

Precision metrology of phase-shifting photomasks is vital to the creation and implementation of advanced photomasks. To date, several optical and non-optical approaches have been adapted to this task. Each of these existing approaches has significant limitations of spatial resolution, accuracy or measurement speed. We have previously proposed an all-optical, interferometric architecture that is suitable for high-precision metrology of phase features both small and large, isolated or densely spaced, and all types of phase shifting photomasks. In this paper, we report the latest results in our on-going development of this actinic optical phase metrology tool, that is based on a 193-nm solid-state laser and a high-resolution interferometric, 0.75-NA optical microscope.

6349-165, Poster Session

A general framework for multi-flow, multi-layer, multi-project reticles design

A. B. Kahng, X. Xu, Univ. of California/San Diego

With pervasive use of advanced reticle enhancement technologies such as Optical Proximity Correction (OPC) and Phase Shifting Masks (PSM), mask costs are predicted to reach $10 million by the end of the decade. The high mask costs push prototyping and low-volume production designs beyond the limit of economic feasibility since the costs cannot be amortized over the volume.

Multi-Project Wafers (MPW), or “shuttle” runs, provide an efficient method to reduce the cost. However, one major practical limitation of the multi-project wafer is the delay cost associated with schedule alignment. Worse yet, schedule delay of test chip manufacturing leads in turn to schedule delay of the final product manufacturing, which is too costly to be ignored. Since the savings on mask cost with MPW can be easily surpassed by the profit loss due to schedule alignment, Multi-Layer Reticles, which rely on sharing the reticle space between multiple layers of the same design, typically via blading, is proposed. The delay cost can be minimized since the mask cost is amortized between the layers of the same design. Recently, a more aggressive mask-sharing technique has been proposed, which shares the mask cost between designs of different technology flows.

In this paper, we propose a framework for optimization of Multi-flow Multi-layer Multi-project Reticles (MFMLMPR), which combines all available mask cost-saving technologies to achieve the maximum manufacturing cost saving. MFMLMPR designs introduce complexities not encountered in traditional single-flow or single-layer reticles. To our best knowledge, our formulation and optimizer are the first to consider the design optimization for MFMLMPR. Our flow includes three main steps: (1) schedule-aware project partitioning and multi-flow embedding; (2) multi-frame reticle design; and (3) multi-project frame floorplanning. Our

contributions are as follows. For the first step, a fast iterative matching algorithm is proposed to calculate

the mask cost for multi-flow embedding with consideration of all practical manufacturing costs. We then propose an integer linear programming (ILP) based method for optimal manufacturing cost minimization. Since ILP suffers from impractically long runtimes when the number of projects is large, we propose a sliding time window heuristic to exhaustively search the solution space for the best tradeoff between mask cost and delay cost. For the second step, we propose an ASAP frame embedding heuristic to minimize the mask cost. Finally, a “generalized chessboard” floorplan with simulated annealing is proposed to generate more dicing friendly frame floorplans for multi-flow projects, observing given maximum reticle sizes.

We have tested our flow on production industry testcases. The experimental results show that our schedule-aware project partitioner yields an average reduction of 58.4% in manufacturing cost. The reduction of mask cost is around 46.3% compared with use of traditional single-layer reticles. Our generalized chessboard floorplanner leads to an average reduction of 23.4% in the required number of wafers compared to the previous best reticle floorplanner.

6349-166, Poster Session

CP mask optimization for enhancing the throughput of MCC systems

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The character projection (CP) is utilized for maskless lithography and is a potential for the future photomask manufacture. The throughput of the CP is much higher than the variable shaped beam (VSB). It is, however, needed to be improved, compared with the throughput of photolithography. The throughput improvement can reduce the amortization cost of CP equipment, that is the price rise of ICs. The CP lithography has been researched especially for a single column cell (SCC) system. The weak point of the SCC-based CP lithography is that not all logic cells used for IC design can be placed on a CP mask. The logic cells off the CP mask must be projected with the variable-shaped beam projection. This deteriorates the throughput of the equipment.

It is natural to adopt multiple column-cells for the higher throughput of projection equipment. The MCC (multi-column-cell) system, which has multiple column-cells, is one of the solutions to the low throughput of the CP lithography systems. It accommodates several column-cells each of which has an electron gun and a CP mask for projecting chips in parallel. Parallelizing projections contributes to the increase of the throughput. Simply speaking, the throughput improvement is inversely proportional to the number of column cells.

For MCC systems, a CP mask set of a column-cell is not necessarily same as that of the others even if multiple column-cells are utilized in parallel. This paper proposes a CP mask development methodology for increasing the throughput of MCC systems by optimizing the CP masks of multiple column-cells as a set. A column-cell in the projection equipment naively has the same CP mask set as the others while it has the different CP mask set in the proposed method. In the proposed method, each column-cell doesn’t have to finish projecting a whole IC but project its favorite parts of the IC. The remainder of the IC is projected by the others which have the corresponding characters on their CP masks. The proposed method virtually increases the number of logic cells which are projected with the CP for avoiding the VSB projection as much as possible. The authors examined the number of EB shots required for an SCC system, a two-column-cell system with the uniform CP masks, and a two-column-cell system with the multiform CP masks for validating the effectiveness of the proposed CP mask development methodology. The experimental results show that the proposed CP mask development methodology reduced 71.3% of the number of EB shots for an SCC system to project a benchmark circuit. It also reduced 42.6% of the number of EB shots for the two-column-cell system to project a benchmark circuit with the uniform CP masks. It was experimentally validated that the proposed CP mask development methodology could increase the throughput of CP lithography systems only by optimizing their CP mask set. The authors will present a mathematical model to optimize the CP mask set for MCC systems in the final version of this paper.

6349-167, Poster Session

Evaluation of writing strategy with one and two pass on OPC technology using EBM writing system

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Mask technology development has accelerated dramatically in recent years and sometimes simultaneous introductions of new wavelengths and mask-based resolution enhancement techniques. These are among the factors that have created enormous stress on the mask industry to produce masks with enhanced capabilities, such as phase-shifting attenuators, sub-resolution assist bars, and optical proximity correction (OPC) features, while maintaining or reducing cost and cycle time. In order to improve the critical dimension (CD) accuracy and resolution, several new technologies have been introduced; especially on e-beam lithography is a serious process. In these period, the common use of 50 KeV variable-shaped e-beam writers for the high-end masks making. The main reason for this development is exactly the excellent resolution with 50 KeV e-beam which was suitable for small dimension and optical proximity correction (OPC) technology.

Recent low-k1 lithography to meet industrial requirements for resolution results in unavoidable optical proximity effects. Accordingly, design and OPC verification for manufacturing is necessary and thus essential for 130 nm generation and beyond. However, the aggressive OPC induces data volume explosion, writing time explosion, and other mask process issues. As well known the historical limitation of e-beam lithography is throughput. For shortening of writing time, it is most effective to reduce the number of shots. Resolution Enhancement Technologies (RET) such as OPC and PSM, make the writing shot number increase explosively, and worsens the writing throughput. This is a serious problem for e-beam writing system, and the improvement of a writing throughput is necessary.

Evaluation of the writing strategy effects with one and two pass exposed by EBM-4000 variable-shaped e-beam lithography tool is a new class of masks making, especially writing on the OPC pattern. The EBM-4000 writing system features a variable shaped beam, 50 KeV accelerating voltage, a continuous stage and incorporates some technologies. Obviously, many examples exist of systems which add parallelism to the exposure process using multiple pass. The standard writing strategy of EBM-4000 writing system is four pass. We have confirmed the two pass exposed by EBM-4000 writing system for 130 nm node technology even below successfully. It is directed toward that improves throughput and excellent performances due to the best conditions of exposure and CAR process.

In the present investigation, the one and two pass exposed by EBM-4000 writing system has been investigated. The objective of the present work is indicated the performances for several design of OPC verification like serifs and jogs. We will provide the actual measurement data and images obtained on CD-SEM for the OPC patterns exposed with one and two pass. In this paper, the characterization data will also present the applicable results such as resolution, position accuracy, global and local CD uniformity, CD linearity and corner rounding. We have evaluated and confirmed the writing strategy with one and two pass of EBM-4000 writing system.

6349-168, Poster Session

Self-aligned resist patterning on Cr/MoSiN patterns by backside flood exposure in photomask

T. Ha, B. Gyun, O. Han, Hynix Semiconductor Inc. (South Korea)

As the minimum pattern size decreases, the tolerance of CD and defect gets lower. So a pattern formation and a process control get more and more difficult. To improve these difficulties, we have been developing various patterning techniques; photomask repeater, imprint patterning, AFM lithography and so on. Because the patterning process is not per-

fect, various repair technology is also needed. So we investigated the self-aligned resist patterning on Cr or MoSiN patterns of mask.

We coated the photo-resist on a mask, exposed the KrF light on the backside of the mask and then developed this mask. From this process flow, new resist patterns can be formed on Cr patterns. We call this new patterning technique 'the self-aligned resist patterning by backside flood exposure'. The principle of this self-aligned resist patterning is the difference between the transmittances of Cr and quartz. Resist on quartz region (transmittance, about 100%) is exposed by KrF light which is penetrated from the backside. But resist on Cr region (transmittance, 0%) cannot be exposed by penetrated KrF light. If we use the positive tone resist, resist patterns on Cr are formed.

Faithful resist patterns to Cr patterns can be formed by self-aligned resist patterning and the profiles are good enough to be applied to the production. But resist patterns on MoSiN are different from resist pattern on Cr and are changed with illumination condition. This is caused by transmittance (6%) of MoSiN and light interference between MoSiN and quartz.

We got the self-aligned resist patterns on a photomask and these patterns can be used in mask production.

6349-170, Poster Session

Production defect repair performance: analysis of advanced repair processes on production masks

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The challenge in repairing state of the art photomasks is growing with the increasing complexity of the geometries on the mask, especially against the background of the employed resolution enhancement technologies like optical proximity correction and scatter bars.

In order to overcome these challenges, recently electron-beam based repair solutions have been employed in major high-end mask shops.

A MeRiTTM e-beam mask repair system has been used for repair of production mask defects in an advanced mask facility and the paper will discuss the repair processes involved and outline the achieved results. The repair performance will be demonstrated by means of pre- and post-repair SEM images and as a conclusive proof the respective AIMSTM printability measurements of the repairs will be shown and discussed in this context. The high degree of accuracy that can be achieved with an electron-beam based repair system will be demonstrated on different mask types, binary masks as well as phase-shifting masks.

Special attention will be given to the new level of automation and user friendliness surrounding the core repair application.

A novel productivity enhancing feature named Feature Comparison FC-SEM has been developed and employed. This feature allows the tool operators to quickly measure linewidths and other features on any type of relevant mask or substrate inside the repair tool with almost zero overhead time.

In the summary the achieved results will be put in context with the unfolding ITRS roadmap and the extendibility of the selected approach will be discussed.

6349-171, Poster Session

Precise and high-throughput femtopulse laser mask repair of large defects

T. E. Robinson, J. LeClaire, R. White, D. A. Lee, Rave LLC

Although the minimum allowable defect size continually decreases as mask technologies evolve to produce finer and more densely packed structures, the maximum defect size does not necessarily decrease. The occurrence of these large defects can only be further reduced by the addition of expensive clean room facilities improvements such as SMIF handling systems. As the technology of mask making advances, the potential impact of these large defects increases and the feasibility in their repair also decreases as they can span a large number of adjoining densely packed patterns. The presence of difficult to reproduce OPC, and other sub-resolution features such as scatter bars, as well as the increasing use of embedded phase-shifting masks, can also complicate the timely repair of such defects. Unlike most mask repair techniques which provide either high dimensional resolution or high throughput in large area repair-but rarely both, deep UV (DUV) femtosecond pulse laser mask repair has the potential to provide a unique solution to this defect repair need. Methods and results are discussed for the process optimization for the removal of large (5 μ;m) area repair on both Cr and MoSi absorber films on quartz. Additionally, high repair throughput results are shown for unknown contamination removal, and reproduction of ≥1 μ;m complex unconnected patterns in a single repair run lasting a matter of minutes. Closed-loop CD feedback in-situ with the iterative repair process for such structures can result in an edge placement control within ±25 nm. Prior iterative CD closed-loop repairs on specific structures have reliably yielded results within ±10 nm, as confirmed by AIMS CD error, even after aggressive mask wet clean. The nanometer scale dimensional resolution and repeatability of such repairs is shown with the use of sub-pixel resolution automated pattern reconstruction using integrated high-NA DUV microscope imaging.

6349-172, Poster Session

Advanced femtosecond DUV laser mask repair tool for large area photomasks

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• INTRODUCTION.

Ever shrinking feature size and increasing overall dimensions of the LCD and PDP photomasks pose significant challenges for mask manufacturers. E.g., Generation 7 photomask roadmap has mask size of up to 1.5 meters and above, and features sub-micron resolution / CD. As a result, relatively low yield of "perfect" photomasks dictates necessity in advanced photomask repair tools. While smaller photomasks for semiconductor wafer lithography can be subjected to vacuum repair techniques such as FIB and E-beam, large area photomasks are bound for an air-based repair technology. At this time it almost exclusively means laser mask repair for both opaque and transparent defects.

Recent advances in commercial ultrashort pulse lasers allowed development of non-thermal metal thin film removal process from the glass substrate with minimal damage to its surface. However, many challenges are still needed to be resolved, such as sub-micron positioning accuracy and edge-locking stability of the opto-mechanical system over the extended travel range, as well as reliable and repeatable sub-micron removal and deposition of thin films with specified parameters and required adhesion.

This paper addresses development of the first of its kind advanced mask repair tool (MRT) for large area Chrome photomasks (Generation 7 and beyond), including mechanical gantry system, laser unit, and optical module for navigation, location and repair of both types of mask defects, and laser ablation and CVD process development.

• MOTION SYSTEM AND MASK STAGE.

MRT incorporates high precision air bearing and linear motor gantry stage mounted to a massive granite table. Internal development of the gantry system allowed to achieve unmatched accuracy in positioning at the designated repair areas over the extended range of travel. Developed structure provided stable vibration-proof platform, while high precision encoders with 5 nm resolution steps supplied positioning feedback for supreme accuracy and repeatability of positioning in the defect areas. The standard platform handles masks up to 1600 mm x 1400 mm, while premium gantry system can handle 2200 x 1950 mm substrates. Chart of 3D mapping of our gantry system and comparison of its key parameters with other OEM's is provided. Data confirmed superior characteristics of this gantry system for large area mask repair.

• OPTICAL MODULE AND LASER PROCESSING.

Femtosecond laser characteristics and beam quality has been measured and fine-tuned to MRT requirements. Study of different techniques for laser power attenuation has been performed. Comparison of different attenuators is provided.

Optical system has been designed to meet customer requirements for both large area zaps and for minimal size repairs. Different laser processing techniques such as “imaged aperture” and focused Gaussian beam are discussed. To improve imaging resolution, DUV illumination is provided as an option. Specified minimal repair feature size of 0.4 micron has been achieved for zaps and 0.8 micron for CVD on production masks.

MOCVD process was developed to get required adhesion, optical density, and edge definition. Photolytic and pyrolitic aspects of CVD process are discussed. CVD at two different wavelengths were investigated and 0.4 micron lines were deposited in experiments. Correspondingly, recipes were developed to successfully repair transparent defects on production photomasks in the field.

• REPAIR SYSTEM FEATURES.

Using femtosecond laser technology, the MRT system provided repairs with the following features:

- No Edge Rollup and Splatter
- Precise Line Definition of < 0.4 um
- Minimal Photomask Surface Damage of < 10 nm
- Minimal CVD Repair Size of < 0.8 um
- Maximum travel range / mask size up to 1600 mm x 1400 mm (standard) 2200 mm x 1950 mm (optional)
- Greater than 97% Transmission after Ablation
- Repair Accuracies better than 0.02 um \@ 3sigma
- DUV / VIS Imaging
- SOFTWARE AND INTERFACE.

The MRT uses a Linux and Windows XP operating system running on the latest high speed Pentium processors. The combination of fast processors, increased memory, and upgraded operating system provides quick and seamless system operation through the Graphical User interface (GUI).

6349-173, Poster Session

Repair specification for 45-nm node photomask repair

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The shrink of device node to 65 and 45nm node transfers the key process to repair in decreasing mask cost. Thus, it is very important to define the repair performance accurately and to introduce adequate tools timely. Usually the repair performance has been expressed as edge placement error, transmittance change and quartz damage. We have used the measuring tool like CD SEM, AFM and AIMS to measure those factors and the 2D simulator like Solid C to predict the repair performance. In this case, 3D topographical effect is not considered. However, the 3D topography of pattern becomes quite important for 45 nm node or less.

ArF immersion lithography is the strongest candidate for the 45 nm node. The immersion technology makes it possible to use of hyper NA systems. Hyper NA will increase the polarization effect of illumination source. Therefore, the topography of pattern is quite important with respect to intensity and polarization of the various diffraction orders. This paper presents repair specification based on the Solid E 3D simulator for 45 nm node.

6349-174, Poster Session

Thermal modeling of photomask precision baking system

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Baking processes are widely acknowledged as being crucial steps in Photomask manufacture, and in particular, the Post-Exposure Bake (PEB) is regarded as the most critical. For 45nm-node photomasks, and subsequent technology generations, the performance requirements for baking systems significantly exceed those of currently-available equipment. In comparison with Silicon Wafers, Photomask substrates, (typically 6inch square quartz), exhibit markedly different thermal properties. These differences conspire to make Photomask precision baking far more difficult than is the case for wafers.

Multi-zone heating systems have been developed, and in principle offer a practical tuning method allowing better surface temperature uniformity of Photomasks during critical bake steps to be achieved. The best of these systems compensate, to some extent, for multiple causes of temperature non-uniformity within the baking system.

Generally however, the root causes of temperature non-uniformity in the baking process have not all been identified, still less eliminated, and thus there remains a limit to the degree of control of Photomask surface temperature which can be achieved.

In this study, we devised a “Thermal model” of the Photomask baking process. This model has enabled us to identify root causes of non-uniformity of Photomask surface temperatures, as well as providing a quantitative way of assessing how Photomask baking systems may be improved. We present simulation results from the model, as well as actual test data measured by sensor array plate.

For example, in baking process, the proximity gap between 6025 Photomask back surface and Hot-plate surface is very critical. Simulation result shows Photomask substrate can be warped up to 70um. This warp makes large variation of Photomask surface temperature during temperature ramping up. The actual test data measured by sensor array plate show result similar to simulation.

6349-175, Poster Session

More evolved PGSD (proximity gap suction developer) for controlling movement of dissolution product

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The production of hp 55 nm node devices requires ultimately accurate CD uniformity. To achieve very strict uniformity, process machine and process optimizations have been developed from the aspect of accuracy and costs. We think that it is important to quantify the error caused by each process and to reduce it.

Above all, development is key process to progress CD uniformity. Especially, loading effect which is caused by dissolution product is the most serious problem, which influences on the CD variation in the range from several tens microns to several tens millimetres. And it seems to be difficult to correct this error by another process.

We have been developing novel development equipment named PGSD with the line nozzles to spout developer and suck in dissolution products as an approach of reducing error caused by loading effect, and already presented the basic performances at BACUS2002(1)(2), PMJ2003(3) ,and EMLC2005(4). In the previous papers, we reported that it was quite effective to quickly replace dissolution product with fresh developer in order to reduce CD error by loading effect, and also showed that high-speed flow realized by the narrow gap between nozzles and substrate enabled the quick substitution.

In this study, to obtain better CD uniformity, we propose a better method. In PGSD system, dissolution products are moved forward in the first half of development as the same direction as the nozzle scans and backward in the last half respectively as shown in Figure 1. Here PGSD is able to control the flow of dissolution product by a centrally-located development slit and two suction slits aligned at both sides as shown in Figure 2. By changing the location of each slit, PGSD enables equalized distribution of dissolution products between in the first half development and last half.

As a result, CD error caused by loading effect will be reduced compared to the conventional procedure.

We will introduce this new method to minimize CD error caused by loading effect, report CD dependence on other process parameters, and discuss whether the performance of improved-PGSD is satisfied or not with CD requirement for hp 55 nm node device.

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6349-176, Poster Session

Impact of mask error on OPC for 45-nm node

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As lithography, pushes to smaller and smaller features under the guidance of Moore's Law, patterned features smaller than the wavelength of light must be routinely manufactured. Lithographic yield in this domain is directly improved with the application of OPC (Optical and Process Correction) to the pattern data. Such corrections generally assume that the mask can reproduce these features exactly. The Mask Error Enhancement Factor (MEEF) serves to amplify mask errors, and can reduce the benefits of OPC in some circumstances. A concept of the globalized MEEF is introduced by considering fitting with measured and simulated. In general, global-bias type of OPC model may work well in applications where solution to the EPE calculation is intractable. The range of global bias value that we calculated can estimate the accuracy of this approach. Further studies are required to fully understand and characterize 'localized bias' to cover different type of design instead of global bias approach. In this paper, we present the characterization of the MEEF for 45nm technology attenuated phase shift mask to figure out how to measure the mask errors relative to design and try to figure out new ways to reduce model sensitivity to mask deviations for metal level.

6349-177, Poster Session

No-forbidden-pitch SRAF rules for advanced contact lithography

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To achieve advanced contact layer printing, there always are two key factors need to be handled: resolution and through-pitch common process window. Among all solutions, the most common approach is off-axis illumination (OAI) + attenuated phase-shift mask (att-PSM) + sub-resolution assistant features (SRAF). With adequate/high Numerical Aperture (NA) and OAI settings of the leading edge scanners, the resolution should not be a problem, while even with att-PSM + SRAF, the through-pitch common photo process window still leaves much to be desired. This phenomenon is due to the existence of forbidden pitch - under certain illumination condition, there always exists a pitch range which has no spacing for insertion of SRAF while contrast is still poor and needs some special treatment to enhance the image qualities.

This invention and study is to use special SRAF, we call DAF (Diagonal sub-resolution Assistant Feature), to enhance the process performance of forbidden pitches. The main methodology is to select the so-called "forbidden-pitch" structures from the whole database, then apply our DAF rules. After that, apply Conventional sub-resolution Assistant Feature (CAF) rules on post-DAF full-chip database, finally comes OPC treatment. With this approach, we demonstrate excellent results on 65nm contact layer, showing no forbidden pitch and sufficient large through-pitch photo common process window via simple OAI (ArF, 0.82NA, 1/2Ann.) + att-PSM + SRAF.

6349-178, Poster Session

Accounting for lens aberrations into the OPC model calibration

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To keep track with the resolution requirements of Moore's law without reducing the actinic wavelength has forced exposure tools towards extremely high NA. As NA increases so does depth of focus decrease, and this has required OPC corrections to be able to predict printability through focus window. To predict well through process these models must become increasingly based on physics rather than statistical components.

One of the components of the exposure tool that has often been overlooked in model calibration is that of lens aberrations. These physical effects can include the classical Zernike aberrations, chromatic aberrations and averaging of distortions or stage tilting during scanning. By including the correct physics and regressing on appropriate parameters in an OPC model one can determine the settings of any of the above described aberrations.

A good test for the success of this model is correctly predicting such an aberration pre-programmed into the scanner. The paper describes and gives experimental results of such an experiment.

6349-179, Poster Session

Correlation between OPC model accuracy and image parameters

C. Kallingal, N. S. Chen, Advanced Micro Devices, Inc.

Performing MBOPC (model based optical proximity correction) on layouts is an essential part of patterning advanced integrated circuits. With constantly shrinking CD tolerance and tighter ACLV budgets, the model has to be accurate within a few nanometers. The accuracy of model in predicting wafer behavior dictates the success of the patterning process. Model calibration is a critical procedure in providing the accurate correlation between design and wafer features. Resist calibration process consists of arriving at a threshold polynominal as a function of image parameters - intensity maximum, intensity minimum, slope, contrast etc. In this presentation, a strong correlation between the accuracy of the model and the image parameters are demonstrated. Data from model calibration of line/space layers in 65nm technology node will be shown to demonstrate the dependence of model accuracy on image parameters. Data show that the accuracy of the model degrades a function of resolution, i.e. features with lower resolution are difficult to model than high resolution features. The accuracy of the model is also impacted by the accuracy of measurements of these low resolution features. The accuracy of the model can be improved by increasing the sampling of the low resolution features and by adjusting the weights of the low resolution features during calibration. Suggestions for improving the accuracy of 1D and 2D features based on a detailed analysis of the image parameters will be presented.

6349-180, Poster Session

Minimizing yield-loss risks through post-OPC verification

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In our continued pursuit to keep up with Moor's Law we are encountering lower and lower k1 factors resulting in increased sensitivity to lithography / OPC un-friendly designs, mask rule constraints and OPC setup file errors such as bad fragmentation, sub-optimal site placement, and poor convergence during the OPC application process. While the process has become evermore sensitive and more vulnerable to yield loss, the incurred costs associated with such losses is continuing to increase in the form of higher reticle costs, longer cycle times for

learning, increased costs associated with the lithography tools, and most importantly lost revenue due to bringing a product to market late. This has resulted in an increased need for virtual manufacturing tools that are capable of accurately simulating the lithography process and detecting failures and weak points in the layout so they can be resolved before committing a layout to silicon and / or identified for inline monitoring during the wafer manufacturing process. This paper will attempt to outline a verification flow that is employed in a high volume manufacturing environment to identify, prevent, monitor and resolve critical lithography failures and yield inhibitors thereby minimizing how much we succumb to the aforementioned semiconductor manufacturing vulnerabilities.

6349-181, Poster Session

The effect of sub-layer condition on the OPC model

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OPC (Optical Proximity Correction) is becoming one of the most important technology for sub-wavelength lithography and has become possible highly accurate CD(Critical Dimension) control and design rule shrink. Current model base OPC is a combination of optical and process model to predict lithography process. At this time, the accurate OPC model can be made by accurate empirical measurement data. Therefore empirical measurement data affects OPC model directly.

In the case of gate layer, it affects to device performance significantly and CD spec is controlled tightly. Because gate layer is hanging on between active area and STI area, the gate CD is affected by different sub layer stack and step height. In this paper, it will be analyzed that the effect of sub layer on the OPC model and difference OPC results between single model and combination model.

6349-182, Poster Session

Efficient approach to improving pattern fidelity with multi-OPC model and recipe

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It is becoming difficult to achieve stable device functionality and yield due to the continuous reduction of layout dimensions. Lithographers must guarantee pattern fidelity throughout the entire range of nominal process variation and diverse layout.

Even though we use general OPC method using single model and recipe, we usually expect to obtain good OPC results and ensure the process margin between different devices in the sub-100nm technology node.

OPC model usually predicts the distortion or behavior of layout through the simulation in the range of measured data. If the layout is out of range from the measured data, all other values are interpolated or extrapolated. But this interpolated or extrapolated value from sparse measured data cause the unexpected OPC results.

In addition, as the design rule has decreased, it is extremely hard to obtain the efficient OPC result only with single OPC recipe. We can not extract optimized OPC recipe which cover the all the various device and layout. Therefore, with applying multi OPC model and recipe to the device which contains the various patterns, We can increase the pattern fidelity in sub-100nm technology node.

In this paper, we demonstrate advantages of multi models and recipes correction over the traditional single model and recipe correction. This method will prevent the unexpected OPC result caused by interpolation or extrapolation and can improve the pattern fidelity at the various layouts.

6349-183, Poster Session

Model-based lithography verification using the new manufacturing sensitivity model

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Process depth of focus analysis has always been an important method for determining semiconductor integrated circuit manufacturability. This is becoming even more apparent as process nodes continue to shrink and more aggressive Reticle Enhancement Technology (RET) techniques are adopted to help retain process latitude. Process window is one of the most important factors in product cost. Therefore, pattern verification prior to mask tape-out is designed to save development time, and cost is extremely important.

The concept of focus-sensitive hotspot detection has been recently introduced using a Manufacturing Sensitivity Model (MSM). As the MSM interacts with the pattern, the model produces output that judges the quality of the through-process correction in a single piece of interpreted data. The MSM output can then be readily analyzed to find process sensitive patterns.

In this study, we will apply a process focus sensitivity detection algorithm to various designs using MSM. The results will be compared to conventional depth of focus analysis techniques. The goal is to understand the relationship between the focus sensitivity and the CD error variations. This will be used to understand if focus-sensitive hotspot detection using MSM can be applied for verifying RET process qualities.

6349-184, Poster Session

On objectives and algorithms of inverse methods in microlithography

Y. Granik, Mentor Graphics Corp.

Inverse microlithography solves problem of finding the best mask to print target layout. We present theoretical analysis of objective functions and algorithms that are used for inversion. We analyze

complexity, speed and limitations of inverse algorithms.

6349-185, Poster Session

Auxiliary pattern for cell-based OPC

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Optical proximity correction (OPC) has been a key enabler of the aggressive IC technology scaling implicit in Moore's Law. However, the runtime of OPC has grown unacceptably and is a major bottleneck of turnaround time (TAT) for IC data preparation and manufacturing. The cell-based OPC approach is to run OPC for each cell once per cell definition rather than once per placed instance, i.e., the master cell layouts in the standard-cell library are corrected before placement, and then the placement and routing steps can be completed using the corrected master cells. Unfortunately, proximity effects have a certain interaction radius between pattern geometries. Since the neighboring environment of a cell in a full-chip layout is completely different from that of an isolated cell, the CD difference between cell-based OPC and conventional model-based OPC can be large.

Gupta el al. used dummy features to consider the effects on OPC of different neighboring environments of a cell instance. The dummy features are inserted at predetermined locations before performing OPC, and then taken out from the layout after OPC in order to maintain design-rule correctness (e.g., with respect to poly-to-poly and poly-to-contact spacing rules) of the cell layout. However, such generic dummy features and placements have only a limited ability to capture the proximity effect from pattern geometries of neighboring cells. Thus, CD errors still remain after cell-based OPC.

This paper describes novel auxiliary pattern generation and post-placement optimization techniques for cell-based OPC. We propose the introduction of vertical- and horizontal-auxiliary patterns (APs) which are located in the same cell row and adjacent cell rows, respectively, with respect to a given cell instance. The auxiliary patterns shield patterns near the cell outline from proximity error, and thus minimize the CD difference between cell-based OPC and conventional model-based OPC.

The width of vertical-AP is larger than the minimum linewidth on the poly layer, while the width of horizontal-AP is as small as that of SRAF

(Sub-Resolution Assist Feature). Horizontal-AP differs from the SRAF technique because SRAF locations depend on the distance between poly lines, while the horizontal-AP is exactly located at the cell boundary.

We also describe a new detailed placement algorithm to insert at least one vertical-AP between cells so that cell-based OPC achieves the same accuracy as conventional OPC methods. For benchmark designs in 90nm technology, the AP insertion is fully achievable with cell utilizations less than 70%. Our proposed cell-based OPC based on the AP technique shows that CD errors at line-width and line-end patterns are about 1nm and 1.2nm, respectively, with 3% reduction of process margin in contact coverage pattern. The AP and postplacement techniques together provide substantial improvements for OPC runtime, cell-based timing characterization, and cell re-spins for ECO (Engineering Change Order).

6349-186, Poster Session

Inverse lithography technology at low-k1

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It has long been known that the best lithography that is theoretically possible can be achieved by considering the design of photomasks as an inverse problem — and then solving the inverse problem to find the optimal photomask for a given process, using a rigorous mathematical approach. Superior pattern fidelity, larger process windows, and improved yields can all be achieved, enabling geometries that may be otherwise unattainable. Traditional approaches to mask design, using model-based OPC and rule or model based sub-resolution assist features, are becoming increasingly problematic as semiconductor manufacturers move to low-k1 nodes (45nm, 32nm, and below). As a result, inverse lithography technology (ILT) is becoming essential. In this paper, we discuss the first ILT methodology and implementation that can rapidly solve for optimal photomask designs subject to realistic manufacturing constraints and is suitable for use in a production environment.

6349-187, Poster Session

Parametric uncertainty in optical image modeling

J. E. Potzick, E. Marx, National Institute of Standards and Technology; M. P. Davidson, Spectel Research Corp.

Optical photomask feature metrology and wafer exposure process simulation both rely on optical image modeling for accurate results. While it is fair to question the accuracies of the available models, the model results also depend on several input parameters describing the object and imaging system. Errors in these parameter values can lead to significant errors in the modeled image. These parameters include wavelength, illumination and objective NA's, magnification, focus, etc. for the optical system, and topography, complex index of refraction n and k, etc. for the object.

In this paper two different kinds of optical imaging model were used to simulate the images of isolated lines and spaces on a binary photomask imaged in transmission (as in a microscope or wafer exposure tool). One model uses the rigorous coupled waveguide method and the other uses the integral form of Maxwell's equations. Each input parameter was varied over a range about its nominal value and the corresponding images simulated. Second order parameter interactions were not explored. Using the scenario of the optical measurement of photomask features, these parametric sensitivities were quantified by calculating the apparent change of the measured linewidth for a small change in the relevant parameter. Then, using reasonable values for the estimated uncertainties of these parameters, the parametric linewidth uncertainties can be calculated and combined to give a lower limit to the linewidth measurement uncertainty for those parameter uncertainties.

Results will be shown for a range of isolated linewidths and spacewidths on a photomask, representing hundreds of CPU hours. The same procedure can be used for dense features, but then an additional independent parameter is introduced. For small features especially, differences between the two models are smaller than the parametric uncertainties. These results suggest the photomask linewidth calibration uncertainty for small features may be reduced by using a different image analysis algorithm for small features. For wafer exposure simulation, these results can be divided by 4 as a first approximation, but the magnification difference must be modeled for accurate results.

6349-188, Poster Session

Illumination optimization for 65-nm technology node

C. Wang, C. Hung, Q. Liu, Semiconductor Manufacturing International Corp. (China); L. Zhang, Mentor Graphics Corp. (China)

The most important task of the microlithography process is to make the manufacturable process latitude/window, including dose latitude and Depth of Focus, as wide as possible. Thus, to perform a thorough source optimization during process development is becoming more critical as moving to high NA technology nodes. Furthermore, Optical proximity correction (OPC) are always used to provide a common process window for structures that would, otherwise, have no overlapping windows. But as the critical dimension of the IC design shrinks dramatically, the flexibility for applying OPC also decreases. So a robust microlithography process should also be OPC-friendly. This paper demonstrates our work on the illumination optimization during the process development. The Calibre ILO (Illumination Optimization) tool was used to perform the illumination optimization and provided plots of DOF vs. various parametric illumination settings. This was used to screen the various illumination settings for the one with optimum process margins. The resulting illumination conditions were then implemented and analyzed at a real wafer level on our 65nm critical layers, such as Active, Poly, Contact and Metal. In conclusion, based on these results, a summary is provided highlighting how OPC can get benefit from proper illumination optimization.

6349-189, Poster Session

Printability of sub-wavelength mask features and defects

W. Cheng, Intel Corp.

As silicon processes scale toward the 45 nm node using conventional 0.25 magnification, widths of sub-resolution assist feature (SRAF) on photomasks drop below the ArF laser wavelength. Adoption of polarized illumination and higher numerical aperture (NA) invalidates the scaling relations we used in the past to determine which small mask features or defects will print on wafers. Polarization induced by small mask features may also play a role in mask inspection. As mask features shrink below the wavelength, differences between the optical systems used for inspection and printing become more significant, and may affect the rules for disposition of inspection results. The data presented here combines experimental results from high NA imaging and inspection of subwavelength SRAF and defects, with rigorous calculation of their images based on vector diffraction. The printability of these deep subwavelength mask feature determines the requirements of optical model's rigorousness for SRAF design rule and also mask defect inspection & repair capabilities.

6349-190, Poster Session

Beyond rule-based physical verification

W. Hoppe, Qimonda AG (Germany); T. C. Rössler, Infineon Technologies AG (Germany); A. Torres, Mentor Graphics Corp.

For advanced technology nodes, a large amount of effort must be spent to optimize area critical full-custom layouts with respect to their manufacturability. Due to the strong irregularity and two-dimensionality of these layouts, it appears impossible to fully capture the corresponding complex requirements with design rules in order to be able to perform a rule-based physical verification in form of a "design rule check" (DRC). Alternative approaches have to be found and one of them is presented in this paper. The complexity of the DRC can be significantly

reduced for rules focused on lithography aspects. Those rules can be replaced by a “simulation rule check” (SRC), where at first lithography simulations are done and then a set of straightforward rules is applied to geometrical entities representing the simulation output instead of the layout geometry. Thus, this new set of rules works more directly on the core of the matter. The “litho-friendly design environment” (LFD) provided by Mentor Graphics offers the tools for this approach. The SRC includes intralayer checks like area, width, and space checks as well as interlayer checks, such as overlap. To the physical designer, SRC violations are presented in a DRC like fashion, including error scoring and classification. This paper will demonstrate the application of LFD and highlight the usability of this infrastructure for layout optimization using an SRC for physical verification.

6349-191, Poster Session

Theoretical modelling and experimental verification of the influence of Cr edge profiles on microscopic-optical edge signals for COG masks

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Different type of dimensional metrology instrumentation is in use today for production control of photomasks, namely SEM, AFM as well as optical microscopy and optical scatterometry. High resolution optical microscopy is still important as a reference metrology system, especially because it is sensitive to the optical effects induced e. g. by 2D or 3D details of features on photomasks.

Particularly with regard to accurate optical CD measurements a thorough modelling of the optical imaging process on the basis of rigorous diffraction calculation is essential, which accounts for both polarisation effects and the 2D or 3D geometry of the structures. At PTB we use two different rigorous diffraction models to calculate the intensity distribution in the image plane, i.e. the rigorous coupled wave analysis (RCWA) method and the finite elements (FEM) method.

The question arises how accurate the influence of edge details on the microscopic-optical edge signals can be modelled. To answer this question we performed systematic experimental studies on COG test structures with varying height, edge angles and edge profiles. These geometric profile parameters of the test structures have been characterised by AFM measurements. Additionally top CD’s of the features have been measured using both a CD-SEM and a metrological AFM.

We present UV-optical CD measurements of these test structures and analysed them taking into accout the measured profile details and, for comparison, using a simple binary structure model. The CD values determined are compared with the corresponding AFM and SEM values.

The good agreement obtained for the optical, AFM and SEM top CD values shows that the optical effects of edge profile details can be modelled correctly with the two models applied. The results again demonstrate the necessity of rigorous model based analysis of the optical measurements, taking into account the edge profile details.

6349-192, Poster Session

Rigorous simulation of 3D masks

S. Burger, Zuse Institute Berlin (Germany); R. Köhle, Infineon Technologies AG (Germany); L. W. Zschiedrich, Zuse Institute Berlin (Germany); H. Nguyen, Infineon Techologies SC300 GmbH & Co. OHG (Germany); F. Schmidt, Zuse Institute Berlin (Germany); R. März, Infineon Technologies AG (Germany); C. Noelscher, Infineon Techologies SC300 GmbH & Co. OHG (Germany)

With decreasing feature size rigorous mask simulations have become an important tool for mask design. As has been shown in a previous work some of the presently used methods suffer from low convergence rates and low accuracy of the results and exhibit very long computation times [1].

We address 3D simulation tasks by using a finite-element solver. This solver has been shown to be superior to competing methods by several orders of magnitude in accuracy and computational time for simulations of line masks under perpendicular incidence [1].

We present simulation results for line masks as well as for periodic arrays of contact holes. The results are compared to results obtained with competing methods.

The work for this paper was supported by the EFRE fund of the European Comunity and by funding of the State Saxony of the Federal Republic of Germany (project number 10834). The authors are responsible for the content of the paper.

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6349-193, Poster Session

Propagation of resist heating mask errors to wafer level

S. V. Babin, Abeam Technologies; L. N. Karklin, Sagantec North America

As technology is approaching 45 nm and below IC industry experiencing severe product yield hit due to rapidly shrinking process windows and unavoidable manufacturing process variations. Current EDA tools are unable by the nature to deliver optimized and process centered designs which calls for ‘post design’ localized layout optimization DFM tools.

To evaluate an impact of different manufacturing process variations on final product it is important to trace and evaluate all errors through design to manufacturing flow. Photo mask is one of the critical parts of this flow, and special attention should be paid to photo mask manufacturing process and especially to mask tight CD control.

Electron beam lithography (EBL) is a major technique which is used for fabrication of high-end photo masks. During the writing process, resist heating is one of sources for mask CD variations [1]. Electron energy is released in the mask body mainly as heat, leading to significant temperature fluctuations in local areas. The temperature fluctuations cause changes in resist sensitivity, which in turn leads to CD variations. These CD variations depend on mask writing speed, order of exposure, pattern density and its distribution.

Recent measurements revealed up to 45 nm CD variation on the mask when using ZEP resist [2]. The resist heating problem with CAR resists is significantly smaller compared to other types of resists [3]. It is partially due to higher resist sensitivity and accordingly lower exposure dose required. However, there is no data yet showing CD errors on the wafer induced by CAR resist heating on the mask. This effect can be amplified by high MEEF values and should be carefully evaluated at 45nm and below technology nodes where tight CD control is required.

In this paper, we simulated CD variation on the mask due to resist heating; then a mask pattern with the heating error was transferred onto the wafer.

TEMPTATION (Temperature Simulation) software tool [4] was used to determine temperature values during EBL writing process. Temperature variations were translated into CD error. It was shown that hierarchically arranged chip cells reveal CD variation depending on their order of writing. These time dependent errors are additional to “static errors” like proximity effects, fogging, and microloading effects, which can be corrected during real time or offline data preparation procedures.

Simulations of CD errors on the wafer were done with and without taking into account mask CD error. The results were compared; CD variations on the wafer resulting from resist heating error on the mask were estimated.

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6349-194, Poster Session

A new criterion of mask birefringence for polarized illumination

K. Iwase, B. Thunnakart, T. Kaneguchi, K. Ozawa, Sony Atsugi Technology Ctr. (Japan); T. Yokoyama, Y. Morikawa, Dai Nippon Printing Co., Ltd. (Japan); F. Uesawa, Sony Atsugi Technology Ctr. (Japan)

This paper proposes a new criterion of mask birefringence for polarized light illumination. As it has been reported, polarized illumination imaging with a hyper-NA projection lens enables the extension of the limitation of optical lithography beyond 45-nm node. Mask birefringence is one of the critical properties for polarized light illumination, because the state of polarization of illumination light is disturbed by the intrinsic birefringence of mask. Therefore, it is a challenge for mask users to specify mask birefringence to realize the inherent benefits of polarized illumination. From this point of view, allowable mask birefringence has already been analyzed. In these analyses, only the absolute values of birefringence have been discussed. As it has been pointed out, mask acts as a rotation retarder for the polarized illumination. Therefore, the angle of fast axis of birefringence also affects the state of polarization. We thus propose a new criterion of mask birefringence which adopts the angle of fast axis as well as the absolute value of birefringence. This criterion, named Reticle Birefringence Index (RBI), is based on the nature of rotation retarder, where the state of polarization of linearly polarized light is affected by the angle of fast axis. RBI can describe this effect, as it is defined as: $RBI = B \times |\sin(2q)|$, where B and q denote the birefringence, and the angle of fast axis, respectively.

The RBI is expected to correlate well with printed critical dimensions (CDs). To demonstrate this, printed CDs were calculated as a function of birefringence, B, and RBI by using a lithography simulator. In this simulation, experimentally measured birefringence and angle of fast axis were used. The experimental measurements were done for 11 x 11 points that cover the scanner full-field (26 x 33 mm) area. The simulation showed that there were poor correlation present between printed CDs and birefringence. Especially, if the birefringence became larger than 14 nm/cm at exposure wavelength, no clear correlation became to be present. On the contrary, RBI exhibited a good correlation with the printed CDs even if $B > 14$ nm/cm. The difference can be attributed to the effect of angle of fast axis. For example, a rotation retarder with the angle of fast axis being 0 or 90 degrees does not affect the state of polarization for linearly polarized light. Therefore, even if B is large, there should be negligible impacts on printed CD when the fast angle = 0 or 90 degrees.

The scope of this paper is to specify mask birefringence by using RBI. The specification of RBI will be derived experimentally by using the mask with pre-measured mask birefringence. In the experiment, CD budget analysis will be done. In addition, the impact of noise factors such as uniformity of state of polarization in illuminator will also be discussed. Through these analyses, the requirements of RBI value beyond 45-nm node will be addressed.

6349-195, Poster Session

Reticle carrier material as ESD protection

D. Helmholz, M. Lering, Advanced Mask Technology Ctr. (Germany)

This paper addresses the question of material conductivity (electrically isolating/dissipative/conductive) of the shell and the reticle contact points in reticle carriers and its effect in protecting the reticle from field induced electrostatic discharge damage (ESD). Materials with different electrical properties were investigated; tests included measurements of surface resistivity, resistance to ground, charging, field induced and shielding efficiency. The effect of different materials on protecting reticles from ESD were also studied in an experimental setup using CANARY™ reticles. The analysis was based on Starlight™-- inspections, scanning electron microscope images and atomic force microscope images. A recommendation of ESD protection through material choice and its electrical properties is given.

6349-196, Poster Session

Experimental investigation of photomask with near-field polarization imaging

T. Chen, T. D. Milster, S. Yang, College of Optical Sciences/The Univ. of Arizona

Due to requirements of high throughput, cost-effective and nondestructive properties, optical measurement techniques are important measurement methods in the photomask technology. In this paper, a near-field polarization imaging system using a solid immersion lens (SIL) is introduced, and near-field polarization images of Alt-PSM masks are presented.

The near-field SIL imaging is a high resolution imaging system compared to far-field imaging system, since it can detect the non-propagating evanescent waves very close (~100nm) to the sample surface, which is not detectable to other far-field imaging system. The evanescent waves carry higher spatial frequency information of sample and are re-imaged back through the SIL. The transverse resolution is improved greatly in this way.

In the SIL near-field imaging system, with a linearly-polarized incident illumination light, an orthogonal component of polarization is induced upon reflection from the surface the sample. Also, this orthogonal polarization signal contains information of both air gap height and material properties. With the same way, near-field polarization images are obtained using linearly-polarized incoherent illumination light. By calibration, height information of sample and materials properties are obtained from the near-field polarization images with very high transverse resolution simultaneously. In our experiments, the SIL near-field imaging is used with a modified conventional inverted microscope. A high end Alt-PSM mask sample is studied.

6349-197, Poster Session

The effect between mask blank flatness and wafer print process window in ArF 6% att. PSM mask

J. Tzeng, Toppan Chunghwa Electronics Co., Ltd (Taiwan)

Photomask blank flatness is more important for wafer lithography so far. In view of economic and capital concern, vender of mask blank always provides several level flatness of blank what mask house request. Additionally, wafer fabricators also request the flatter photomask to fit the next generation requirement. However, the 3D effect of photomask should be a contribution of lithography process window. The effect includes quartz substrate flatness and distortion. Besides, the Mask blanks have several shapes that are flat, concave and convex, result from film of Cr and MoSi deposit. This paper provides the relation between mask blank flatness and lithography. We split deferent level flatness of mask blank to verify wafer printing performance. The pattern we use is poly layer of logical 90 nm generation that is more critical among all of lithography process and was exposed by 193nm ArF environment. Primary purpose of the ADI (after develop inspection) performance concern is proximity and process window of wafer print.

SPIE
Photomask Technology

18-22 September 2006

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Monday 18 September .... 7:30 am to 4 pm
Tuesday 19 September .... 7 am to 4 pm
Wednesday 20 September .... 7:30 am to 4 pm
Thursday 21 September .... 7:30 am to 4 pm
Friday 22 September .... 8 am to 10 am

Exhibition Hours

Monterey Conference Center, Serra Ballroom

Tuesday, 19 September .... 10 am to 4 pm; 6 to 7:30 pm
Wednesday, 20 September .... 10 am to 4 pm

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Coffee will be served at the following times and locations. Please check the conference listings for exact times.

Tuesday/Wednesday .... 10 to 10:30 am, 3:10 to 3:40 pm

Monterey Conference Center, Serra Grand Ballroom

Thursday .... 10 to 10:30 am, 3:10 to 3:40 pm
Friday .... 10 to 10:30 am

Monterey Conference Center, Steinbeck Lobby

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Monterey Conference Center, Steinbeck Lobby

Hosted breakfast breads will be served from 7:30 to 8:30 am, Tuesday through Friday for symposium attendees in the Steinbeck Lobby.

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Hosted lunches will be served at the Monterey Marriott in the San Carlos Ballroom at the following times:

Tuesday through Thursday: .... Noon to 1:30 pm

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Dessert will be served Tuesday and Wednesday in the Exhibition located in the Monterey Conference Center Serra Grand Ballroom from 3 to 3:30 pm. A complimentary ticket for dessert will be included in attendee and exhibitor registration packets.

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Monterey Conference Center, Serra Grand Ballroom

Tuesday, 19 September .... 6 to 7:30 pm

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Tuesday 19 September .... 6 to 7:30 pm
Wednesday 20 September .... 10 am to 3 pm

Poster authors may set up their poster papers between 10 am and 4 pm on Tuesday and will leave them up until Wednesday afternoon. Authors will be present during the Poster Reception 6 to 7:30 pm Tuesday to answer questions and provide in-depth discussion regarding their papers. Any papers not removed by Wednesday at 3 pm will be considered unwanted and will be discarded. SPIE assumes no responsibility for papers left up after Wednesday at 3 pm.

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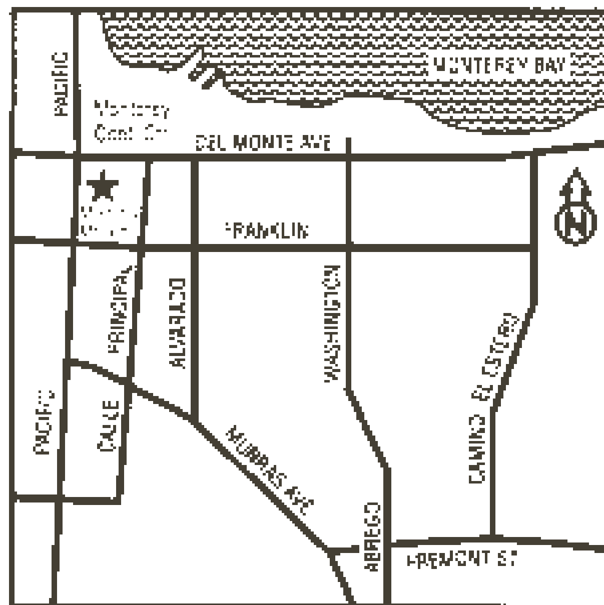

Local Attractions

If time allows, take a day and drive down to the European-style town of Carmel, nestled between the world famous Pebble Beach golf course to the north and the spectacular Big Sur coast to the south. Carmel's rural setting and laid back pace will help you relax while enjoying yourself among the various shops and restaurants.

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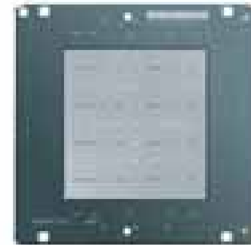

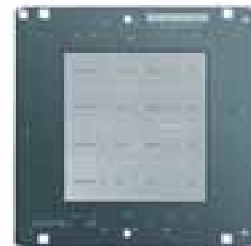

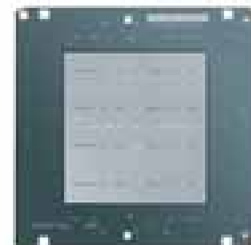

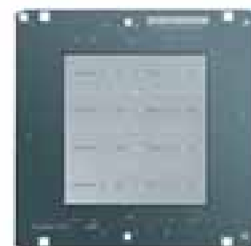

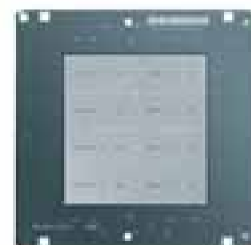

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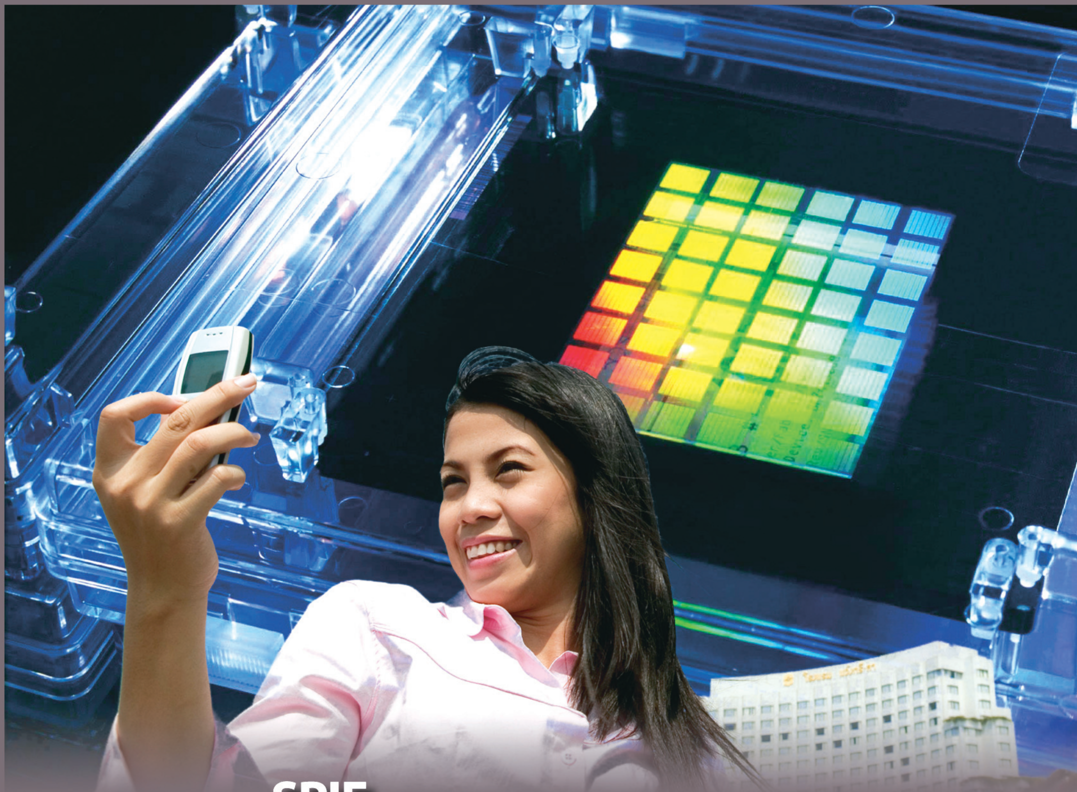

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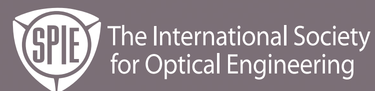

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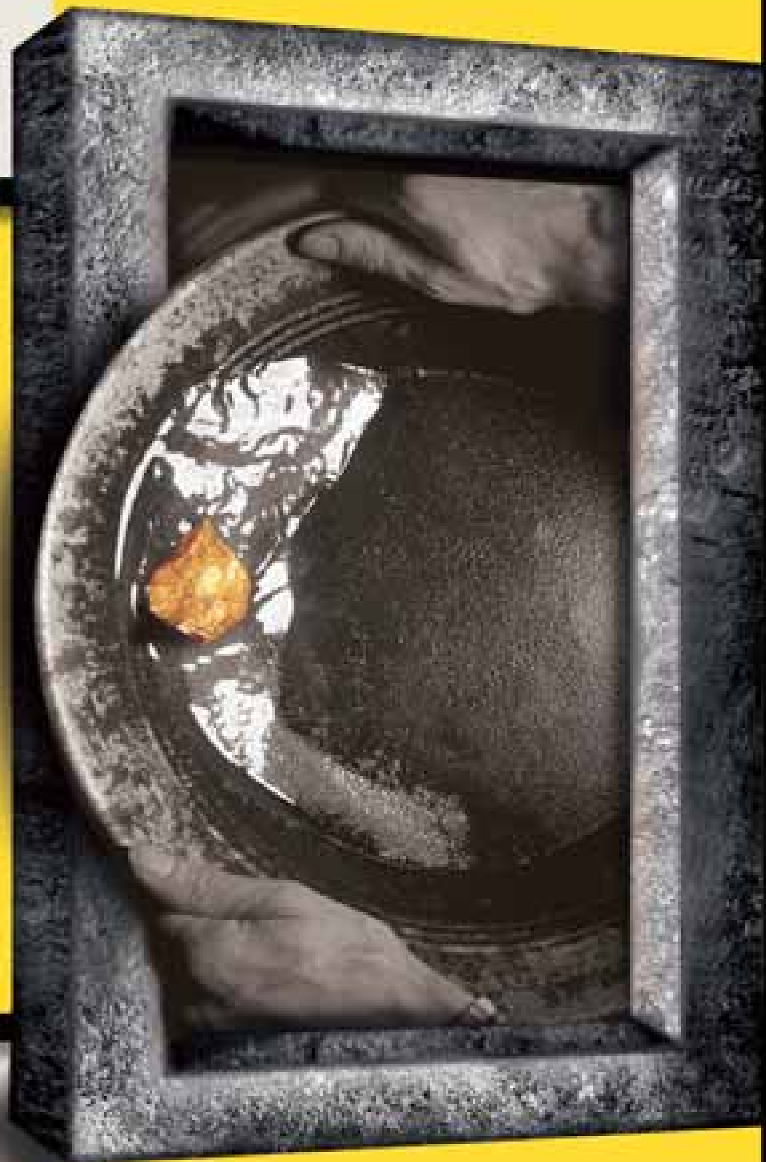

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