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# Conference 8880: SPIE Photomask Technology

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8880-1, Session 1

## Delivering Complexity at the Frontier of Electronics *(Keynote Presentation)*

Michael C. Mayberry, Intel Corp. (United States)

The current era of semiconductor research is heavily dependent on the incorporation of new materials into structures measured in nanometers. We require complexity at not only the functional level but complexity in how these functions work together to make better products. The mask set is the critical element in managing that complexity in a cost effective manner but mask making today is challenged to key up with demands. For the next decade, these trends are expected to continue and will suffice to improve the traditional metrics of performance-power and costs. There are many choices to be made but a rich future lies ahead of us.

8880-2, Session 2

## Effect of chemical composition of Ru capping layer and wet chemical processing EUV mask

Yun Yue Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

In this paper, we present detailed characterization of EUV mask capping layer consisting of pristine Ru and Ru compound deposited on Mo/Si multilayer. To unravel the complex mechanisms leading to Ru surface damage associated with wet chemical treatment, x-ray surface analysis and cluster based first principle simulation are both performed. On the basis of atomic force microscopy (AFM), x-ray spectroscopy (XPS) and simulation results, serious damage and microroughness of Ru surface is mainly attributed to wet chemicals etching effect as shown in Figure 1 and Figure 2. Our study also indicates that design and optimization of Ru capping layer composition is a key factor for improving durability of EUV masks

8880-3, Session 2

## Photomask linewidth roughness and its control

Banqiu Wu, Ajay Kumar, Applied Materials, Inc. (United States)

Line edge roughness (LER) or line width roughness (LWR) is a fundamental challenge in semiconductor industry because LER on transistor gate length is a dominant parameter to determine the variability of threshold voltage, on-current, and off-current; and LER on interconnect impacts breakdown voltages. Integrated circuit (IC) scaling enabled by lithography is the driver to increase device density and improve performance. However, scaling below 32nn feature half pitch CD induces short-channel effect (SCE) because of too short distance between transistor source and drain. Final LER on working layer results from several processes and thus LER controls rely on lithography, resist properties, post-resist-development processing, pattern transfer methods, and LER on photomask. Due to the difference in pattern generation methods for wafer and mask resist layers, it becomes important to understand and characterize LER on photomask and minimize its contribution to wafer layer. Therefore, overview and experimental study on photomask LWR is carried out in this paper.

8880-4, Session 2

## Ultra-low roughness magneto-rheological finishing for EUV mask substrates

Paul Dumas, Chuck McFee, QED Technologies, Inc. (United States); Arun J. Kadaksham, Ranganath Teki, SEMATECH North (United States)

The substrates for EUV lithography photo-masks have to satisfy strict specifications on the allowable surface roughness, flatness and defectivity. These substrates, made of titania-doped fused silica, ideally require sub-Angstrom surface roughness, sub-30 nm peak-valley flatness, and bumps/pits no larger than 1 nm in height/depth. Over the past few years, mask suppliers have been able to gradually improve the quality of the substrates to meet the above specifications, but the yield is still very low.

To achieve the above specifications, the substrates must undergo iterative global and local polishing processes. These processes need to be tightly integrated since the performance of one process adversely impacts the requirements from the other. Typically the local polishing process, like magneto-rheological finishing (MRF®), corrects the figure or flatness but leads to higher surface roughness and the global polishing process, like chemical mechanical planarization (CMP), produces the required roughness but distorts the figure.

MRF polishing is based on a magnetically-sensitive “smart fluid” that stiffens and conforms to the surface of the component being polished, which allows geometries of almost any shape to be polished easily and controllably. The MRF slurry is very stable and does not show wear like a traditional polishing tool; hence the final surface figure can be accurately achieved. Moreover, MRF is numerically controlled and applies sophisticated computer algorithms to ensure that the polishing is deterministic and accurate. This also allows MRF to pre-correct for any predictable distortion which might be induced by stresses or the CMP process. Another distinct advantage of MRF is that its removal is based on a shearing mechanism and applies no normal load, thus eliminating any sub-surface damage on the substrate from the previous coarse polishing steps like grinding and lapping.

Here we show the capability of MRF to achieve sub-30 nm peak-to-valley flatness over the entire 142x142 mm2 substrate area. Since MRF is a directional shear based polishing process, it leaves unidirectional grooves in its wake, and the lowest surface roughness produced by traditional MRF is close to 0.3 nm root mean square (RMS). We also describe the flatness, roughness and defectivity from a new super-fine MRF polishing which can control the unidirectional signature and surface roughness as low as 0.15 nm RMS. Such a surface quality eases the burden on the subsequent CMP process by reducing the removal depth, and hence the polishing time. Lowering the polishing time lowers particle-induced (slurry or contaminant) defectivity and also the extent of figure distortion. This super-fine MRF polishing also has obvious benefits for aspherical polishing of optical mirrors used in EUV scanners.

8880-5, Session 2

## Study of outgassing of electron-beam resists for photomask applications

Gregory M. Wallraff, IBM Almaden Research Ctr. (United States); Steven C. Nash, IBM Corp. (United States); Linda K. Sundberg, IBM Almaden Research Ctr. (United States); William D. Hinsberg, Columbia Hill Technical Consulting (United States); Amy E. Zweber, Ray W. Jeffer, IBM Corp. (United States); Tasuku Senna, Toppan Photomasks, Inc. (United States); Gregory Denbeaux, College of Nanoscale Science & Engineering (United States); Alexander M. Friz, IBM Corp. (United States); Campbell Scott, Luisa D. Bozano, IBM Almaden Research Ctr. (United States)

Resist outgassing during optical exposure has been an issue since the early days of ArF implementation and is currently a subject of significant concern in EUV lithography [1], [2] due to the especially high potential for multilayer optics and photomask contamination. To our knowledge little work has been done to date studying the outgassing of modern electron-beam resists used for photomask fabrication. Since EUV and electron- beam exposure of chemically amplified (CA) resists are thought to trigger similar imaging processes (interaction of secondary electrons with the photoacid generator component), it might be expected that the outgassing effects would be similar for both. However unlike EUV, the potential for significant resist heating exists for e-beam exposure on quartz photomask blanks, as determined both through experiment and simulation [3-5]. As a result, appreciable thermally-activated resist chemistry may occur in the tool leading to greater outgassing and other outgassed products. Such effects will be exacerbated by the long write times, high density patterns and multiple exposure passes used to fabricate today's complex photomasks.

This paper will present criteria used to evaluate outgassing in CA resists, and methods for carrying out such evaluation. We will describe several experiments useful for characterizing outgassing in e beam resists.

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8880-6, Session 3

## 2013 JPM Best Paper: A study of phase defect measurement on EUV mask by multiple detectors CD-SEM *(Invited Paper)*

Isao Yonekura, Hidemitsu Hakii, Shinya Morisaki, Toppan Printing Co., Ltd. (Japan); Tsutomu Murakawa, Soichi Shida, Masayuki Kuribara, Toshimichi Iwai, Jun Matsumoto, Takayuki Nakamura, Advantest Corp. (Japan)

We have studied MVM (Multi Vision Metrology) -SEM® E3630 to measure 3D shape of defects. The four detectors (Detector A, B, C and D) are independently set up in symmetry for the primary electron beam axis. Signal processing of four direction images enables not only 2D (width) measurement but also 3D (height) measurement. At last PMJ, we have investigated the relation between the E3630's signal of programmed defect on MoSi-HT and defect height measured by AFM (Atomic Force Microscope). [1] It was confirmed that height of integral profile by this tool is correlated with AFM. It was tested that E3630 has capability of observing multilayer defect on EUV. We have investigated correlation with AFM of width and depth or height of multilayer defect.

As the result of observing programmed defects, it was confirmed that measurement result by E3630 is well correlated with AFM. And the function of 3D view image enables to show nm order defect.

8880-7, Session 4

## Entering mask process correction era for EUV mask manufacturing *(Invited Paper)*

Christian Buergel, Advanced Mask Technology Ctr. GmbH Co. KG (Germany); Keith P. Standiford, GLOBALFOUNDRIES Inc. (United States); Gek Soon Chua, GLOBALFOUNDRIES Singapore (Singapore)

The 50keV ebeam exposure of EUV blanks leads to additional electron backscattering from the tantalum layer and the mirror portion of the blank substrate that cannot be adequately corrected by in-tool algorithms. Coupling this additional backscatter with process effects, such as develop and etch micro/macro loading, results in significant systematic Critical Dimension (CD) errors for through pitch and linearity patterns on EUV masks. In wafer production EUV masks are targeted as single layer exposure, which requires extremely stringent CD control. The systematic CD errors can easily exceed the CD requirements of a typical EUV mask, facilitating the need for a correction scheme or mask process correction (MPC).

AMTC and GLOBALFOUNDRIES have started a program to evaluate MPC solutions and drive improvements. Working closely with companies that provide solutions for ebeam and process modelling along with the corresponding correction, we have completed several iterations of MPC evaluations. Specifically, we have tested different equipment, processes and process partitioning for model calibration including a verification of the results.

We report on the results of these evaluations, which include simulation of available models, as well as verification data from mask prints. Additionally, the interaction of MPC with other mask process correction schemes is reviewed. We conclude by summarizing the current capabilities of available MPC solutions and present the remaining gaps for model and correction accuracy as well as the remaining questions for fully implementing MPC into the process landscape.

8880-8, Session 4

## Simulation study of multi-beamlet fogging effect on hard mask

Hyuncheong Ha, Sanghee Lee, Inkyun Shin, Shuichi Tamamushi, Chan-Uk Jeon, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

Since the design node of the semiconductor features is shrinking in size and pitch ultimately, the exposure time of the electron beam writer is increasing more extremely. And especially, the single and variable-shaped electron beam writer which is used most widely for the mask lithography is reaching to the physical limit in point of view of the writing time. Therefore, an innovative multi-beamlet writing scheme has been requested for mask fabrication.

For the electron beam mask writing, the fogging effect which is happened from the long range reflection of backscattered electrons is considered as one of the most dominant source of the defects and therefore its correction is well studied for the single electron beam writer. However, behavior of the fogging effect of the multi-beamlet writer is different from that of single electron beam. The effects from the each single beamlet happen in short range simultaneously and the total fogging effect throughout all beamlet need to be considered.

In this study, we introduce a Monte Carlo simulation for the multi-beamlet electron writer for the mask lithography. We present various phenomenological effects from the multiple electron beams on mask. Also we present a correction method for the fogging effect from the multi-beamlet electrons.

8880-9, Session 4

## Automated defect classification and progression monitoring (DPM) in wafer fab reticle requal

Vikram L. Tolani, Luminescent Technologies (United States); T. H. Yen, Rick Lai, Laurent Tuo, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); Dongxue Chen, Peter Hu, Jiao Yu, Y. C. Wei, George Hwa, Suresh Lakkapragada, Kechang Wang, Danping Peng, Luminescent Technologies (United States); Bill Wang, Kaiming Chiang, Luminescent Technologies, Inc. (Taiwan)

As optical lithography continues to extend into low-k1 regime, resolution of mask patterns continue to diminish, and so do mask defect requirements due to increasing MEEF. Post-inspection, mask defects have traditionally been classified manually by operators based on visual review. This approach may have worked down to 55nm node layers. However, starting 40nm and smaller nodes, visually reviewing 50 to sometimes 100s of defects on masks is error-prone, and takes up valuable inspection tool capacity. Both these challenges in manual defect review are met by adoption of the computational solution called Automated Defect Classification (ADC) whereby every mask defect is accurately classified within seconds, and consistent with guidelines used by production operators at both mask shop and wafer fabs.

While mask shops have inspection, repair, and clean tools to ensure that all defects and repairs are fixed to within certain print tolerances, the emphasis in wafer fab is then for the reticle to not change. However, it is well known that extensive use of 193nm reticles in wafer fabs cause the growth of haze-like crystals on the mask. So even though the mask is free of any critical contaminations when initially shipped out from mask shop to the wafer fab, its prolonged storage in the fab environment and extended exposures in 193nm scanners, causes growth of small contamination-looking defects, referred to as haze. Once seeded, haze defects only increase in number, and severity with further use of the reticle often making it OOS rather rapidly. Hence, it is crucial to monitor through periodic inspections, every reticle defect not just in terms of the number and severity in the current inspection, which is enabled by use of ADC, but also in terms of how these defects have potentially changed from previous inspection requals. The purpose of such monitoring is not only to verify that the reticle is currently in-spec but also predict if the mask will still stay in-spec before the next requal cycle.

Furthermore, mask repairs are being done in mask shops in increasingly high MEEF geometries. Repair sites tend to have very thin residues in and around the original defective regions, and contribute to the overall printability of the site. These residues tend to become mobile under the high energy 193nm scanner exposures often causing the effective printability of the repair sites to change. So even though the repair site may have originally met certain stringent printability criteria, it can very well change and become OOS with extended scanner exposures. Hence, it has become essential to also monitor every reticle repair to ensure that it has not changed with scanner exposures. This is the essential concept behind Defect Progression Monitoring (DPM) in wafer fab environment.

ADC-DPM is implemented in by first characterizing defects in the current inspection in terms of various metrics or gauges that indicate defect severity. All this information, including defect x,y locations are saved in an extensive database. Any critical defects in this inspection are first highlighted based on certain guidelines specified through ADC. Next, through DPM, every one of these defects, including haze and repairs, are compared with the corresponding instance in previous inspections. Any substantial deviation in the defect severity levels indicate that the repair or haze site is progressively degrading, and hence the reticle needs to be sent back to the mask shop for further analysis and repel.

Implementation of ADC-DPM in high-volume N40 and N28 manufacturing has detected all real haze defects and repair changes with minimal false rate, establishing an effective early-warning system. It has provided an SPC-like system monitoring every reticle defect for change, and become quintessential for reticle requal defect disposition.

8880-10, Session 5

## Performance of an automatic algorithm for quantifying critical dimensions in actinic aerial images

Douglas Uzzel, Mark Ma, Shad E. Hedges, Photronics, Inc. (United States); Saghir Munir, Reticle Labs. (United States)

This article presents results from an algorithm that can automatically quantify critical dimensions in Aerial images from Mask inspection tools with a very high level of accuracy. It is shown that using such an algorithm the inspection systems can be run with much tighter settings, resulting in more false defect defections, that can then be filtered using the algorithm described here. Such a technique could potentially make the inspection system suitable for inspecting photo-masks beyond its practical limitation.

Automatic defect classification and critical dimension quantification algorithms for analyzing inspection images have been around for over a decade. The goal of this article is to quantify the performance of the Automatic Heuristic Defect Classification (AHDC) algorithm, in terms of not just speed, but the consistency with which it makes the correct Pass or Fail disposition decision.

It is shown that the AHDC algorithm will never pass a failing defect. However due to its conservative nature, it may on rare occasions fail a marginally passing defect. This conservatism is of course by design that the operator can dial down.

The AHDC algorithm can automatically compute the intensity error between the defect and reference images. In addition it can compute the worst case critical dimension, as well as separately report the absolute and percentage critical dimensions of both, the clear and opaque parts of the defective geometry. For contacts and other island geometries, AHDC is capable of computing the percentage area

differences. All these metrics are then used to make a final pass or fail dispositioning decision based on cut off values specified in the recipe table.

Results of critical dimension calculations using AHDC applied to actinic inspection images from programmed defect masks are compared against manually computed critical dimensions. The correlation between the automatic and manual methods is plotted, to present unequivocal evidence that the AHDC algorithm makes decisions that are consistent with how a human will measure and quantify complicated patterns found on high end photo-masks. Thus it is claimed that AHDC will work for any geometry.

AHDC is integrated with a comprehensive reticle defect management system (RDMS), using which all defects and their AHDC metrics can be tracked across multiple inspection of the same reticle with a few mouse clicks.

8880-11, Session 5

## Improve mask inspection capacity with automatic defect classification (ADC)

Eric G. Guo, Blade Gao, Crystal Wang, Steven Ho, Semiconductor Manufacturing International Corp. (China); Kechang Wang, Luminescent Technologies (China); Suresh Lakkapragada, Jiao Yu, Peter Hu, Vikram L. Tolani, Linyong Pang, Luminescent Technologies (United States)

As optical lithography continues to extend into low-k1 regime, resolution of mask patterns continues to diminish. The adoption of RET techniques like aggressive OPC, sub-resolution features,combined with the requirements to detect even smaller defects on masks due to increasing MEEF, poses considerable challenges for mask inspection operators and engineers.Therefore a comprehensive approach is needed in handling defects post-inspections by correctly identifying and classifying the killer defects impacting the printability on wafer, real defects in different types for repair and clean, nuisance defects to ignore, and false defects caused by inspection systems. This paper focuses on the results from the evaluation of Automatic Defect Classification (ADC) product at the SMIC mask shop for the 40nm technology node.

Traditionally, each defect is manually examined and classified by the inspection operator based on a set of pre-defined rules and human judgment. At SMIC mask shop due to the significant total number of detected defects, manual classification is not cost-effective due to increased cycle time, resulting in constrained mask inspection capacity. The Automated Defect Classification (ADC) product offers a complete and systematic approach for defect disposition and classification offline, resulting in improved utilization of the current mask inspection capability. This approach of computationally reviewing defects post mask-inspection ensures noyield lossby qualifying reticles without the errors associated with operator mis-classification or human error.

The ADC engine retrieves the high resolution inspection images and uses a decision-tree flow to classify a given defect. Some identification mechanisms adopted by ADC to characterize defects include defect color in transmitted and reflected images, as well as background pattern criticality based on pattern topology. The final classification uses a matrix decision approach forachieving the final defect disposition. As a first step for qualifying ADC for high volume production, the defect classification results obtained with ADC are compared to the operator classification. Matching rates of greater than 90% were achieved when compared to operator defect classifications. Moreover, no critical defect has been missed. ADC performance was proven to be qualified for deployment in full volume mask manufacturing production flow.

8880-12, Session 5

## Increasing reticle inspection efficiency and reducing wafer print-checks via automated defect classification and simulation

Sung Jae Ryu, Sung Taek Lim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Anthony D. Vacca, Peter J. Fiekowsky, Dan Fiekowsky, AVI-Automated Visual Inspection (United States)

IC fabs inspect critical masks on a regular basis to ensure high wafer yields. These requalification inspections are costly for many reasons including the capital equipment, system maintenance, and labor costs. In addition, masks typically remain in the “requal” phase for extended, non-productive periods of time. The overall “requal” cycle time in which reticles remain non-productive outside scanners is challenging to control. Shipping schedules can be missed when wafer lots are put on hold until the master critical layer reticle is returned to production and unfortunately, substituting backup critical layer reticles can significantly reduce the otherwise tightly controlled process window adversely affecting wafer yields.

One major requal cycle time component is the disposition process of mask inspections containing hundreds of defects. Not only is precious non-productive time extended by reviewing hundreds of potentially yield-limiting detections, each additional classification increases the risk of manual review techniques accidentally passing real yield limiting defects. Even assuming all defects of interest are flagged by operators, how can any person’s judgment be confident regarding lithographic impact of these defects? Lost reticle productivity time away from scanners combined with potential yield loss due to defect lithographic impact uncertainty presents significant cycle time and production cost challenges.

Fortunately, a software program has been developed which automates defect classification with simulated printability measurement greatly reducing requal cycle time and improving overall disposition accuracy. This product, called ADAS (Auto Defect Analysis Software), has been tested in both engineering and high-volume production environments with very successful results. In this paper, data is examined which reveals a significant reduction for costly wafer print checks, improved inspection area productivity, and minimized risk of misclassified yield limiting defects.

8880-13, Session 5

## Your worst nightmare: inspection of aggressive OPC on 14nm masks with emphasis on defect sensitivity and wafer defect print predictability

Karen D. Badger, IBM Corp. (United States); Kazunori Seki, Toppan Photomasks, Inc. (United States); Ian Stobert, Daniel J. Dechene, Donald J. Samuels, IBM Corp. (United States); Vincent A. Redding, William H. Broadbent Jr., KLA-Tencor Corp. (United States)

To prevent catastrophic failures during wafer manufacturing, mask manufacturers employ sophisticated reticle inspection systems to examine every image on every reticle for defects. These advanced systems inspect at resolutions typically 3x higher at the reticle plane than advanced wafer scanners; thus enabling them to detect the small defects necessary to ensure reticle quality.

The most thorough inspection is done using a reticle-to-database comparison that ensures the reticle pattern matches the design pattern. For high defect sensitivity, the database must be carefully modeled to exactly match the reticle pattern. Further, sub-resolution OPC shapes are often at the limit of the mask manufacturing process,

which adds subtle variations on such shapes across the reticle. These modeling errors and process variations can cause high numbers of unwanted detections, thereby limiting inspection system defect detection sensitivity.

OPC designs are expected to become more aggressive for future generations and may stress the performance of current reticle inspection systems. To systematically assess the capability of various inspection approaches and identify needed areas for improvement, a new "Nightmare" test reticle has been designed jointly by the IBM Computational Patterning Team and the IBM Mask House. The test reticle contains various sizes and shapes of sub-resolution features that might appear on reticle generations from today's 22nm to future 7nm. It also contains programmed defects to assess defect detection capability of current and future generation inspection systems.

This paper will discuss the design of the "Nightmare" test reticle, and the inspection results of the current generation reticle inspection methods with emphasis on both inspectability and defect sensitivity. The sub-resolution features will be ranked according to importance for advanced OPC design. The reticle will also be printed using an advanced wafer scanner so lithographic impact of features and defects can be measured and compared against inspection approaches and results.

8880-14, Session 6

## The impact of 14nm photomask variability and uncertainty on computational lithography solutions *(Invited Paper)*

John L. Sturtevant, Edita Tejnil, Steffen F. Schulze, Peter D. Buck, Mentor Graphics Corp. (United States); Franklin D. Kalk, Kent H. Nakagawa, Toppan Photomasks, Inc. (United States); Paul W. Ackmann, GLOBALFOUNDRIES Inc. (United States); Christian Buergel, Fritz Gans, Advanced Mask Technology Ctr. GmbH Co. KG (Germany)

Computational lithography solutions rely upon accurate process models to faithfully represent the imaging system output for a defined set of process and design inputs. These models, which must balance accuracy demands with simulation runtime boundary conditions, rely upon the accurate representation of multiple parameters associated with the scanner and the photomask. While certain system input variables, such as scanner numerical aperture, can be empirically tuned to wafer CD data over a small range around the presumed set point, it can be dangerous to do so since CD errors can alias across multiple input variables. Therefore, many input variables for simulation are based upon designed or recipe-requested values or independent measurements. It is known, however, that certain measurement methodologies, while precise, can have significant inaccuracies. Additionally, there are known errors associated with the representation of certain system parameters. With shrinking total CD control budgets, appropriate accounting for all sources of error becomes more important, and the cumulative consequence of input errors to the computational lithography model can become significant. In this work, we examine with a simulation sensitivity study, the impact of errors in the representation of photomask properties including CD bias, corner rounding, refractive index, thickness, and sidewall angle. The factors that are most critical to be accurately represented in the model are cataloged. CD Bias values are based on state of the art mask manufacturing data and other variables changes are speculated, highlighting the need for improved metrology and awareness. It is shown that traditional mask acceptance specification and post clean acceptance criteria, may be too relaxed for the 14 nm generation.

8880-15, Session 6

## An accurate ILT-enabling mask 3D full chip modeling for all-angle patterns

Hongbo Zhang, Qiliang Yan, Ebo H. Croffie, Lin Zhang, Yongfa Fan, Synopsys, Inc. (United States)

As the technology node keeps shrinking down to sub-28 nm technology node, mask topography effect (Mask3D) is a considerable factor to impact the lithography modeling and full chip OPC process. The modeling on Mask3D effect recently has drawn intensive study. Among different types of modeling work for Mask3D effect, rigorous simulation has been proved to be accurate but too slow for the full chip level implementation. Other previous compact modeling works have shown the capability to use the rigorous simulation as the guideline to fit for the compact models, but due to the limitation of the modeling scheme, only Manhattan type of patterns can be predicted well.

On the other hand, inverse lithography technique (ILT) is a very useful technique which could largely expand the process window and help hotspot fix. However, to enable ILT process need the support of Mask3D modeling which can handle all-angle patterns accurately and efficiently enough.

All those shortages on the existing compact Mask3D modeling call for a new more accurate prediction on Mask3D behavior. In this paper, we propose a novel full chip Mask3D model, which intrinsically supports all-angle patterns and thus enables the ILT process. Instead of straightforward kernel fitting with empirical data as what previous work has done, we adopt a novel modeling process from rigorous simulation to enable the all-angle patterns, and thus a compact model can be achieved for full ship simulation and OPC process. The novel Mask3D model can be combined with ILT process due to its support of all-angle features, and thus much larger process windows can be gained in consequence.

Furthermore, this novel Mask3D model is based on the understanding of the true physical behavior of the mask topography effect and our experimental results have demonstrated strong prediction power and high runtime efficiency for both normal incidence and off-axis optical sources and various types of 1D and 2D patterns.

8880-16, Session 6

## Simulation study of CD variation caused by field-edge effects and out-of-band radiation in EUVL

Weimin Gao, Synopsys, Inc. (Belgium); Ardavan Niroomand, Micron Technology, Inc. (United States); Gian F. Lorusso, IMEC (Belgium); Robert Boone, Kevin Lucas, Synopsys, Inc. (United States); Wolfgang Demmerle, Synopsys GmbH (Germany)

Although extreme ultraviolet lithography (EUVL) remains a promising candidate for semiconductor device manufacturing of 1x nm half pitch and beyond, many technological burdens have to be overcome. The "field edge effect" in EUVL is one of them. The image border region of an EUV mask reflects a few percent of the incident EUV light resulting in a leakage of light into neighboring exposure fields, especially at the corner of the field where three adjacent exposures take place. This effect significantly impacts on CD uniformity (CDU) across the exposure field. To avoid this phenomenon, a light-shielding border is introduced by etching away the entire absorber and multi-layer at the image border region of the EUV mask, also known as "black border" (BB). In this paper, we present a method of modeling the field edge effect (also called the BB effect) by using a rigorous lithography simulation with a calibrated resist model. Firstly, the flare map is created by using the point spread function (PSF) of the EUV scanner and convolving with the pattern density map of the mask. Secondly, an

additional “flare level” is introduced on top of the flare map to account for the BB effect. The parameters in this model include the reflectivity and the width of the BB, which are mainly determining the leakage of EUV light and its influence range, respectivley. Another parameter is the transition width which represents the half shadow effect of the reticle masking blades. By setting the corresponding parameters, the simulation results match well the experimental results obtained at the imec NXE3100 EUV tool. Moreover, these results indicate that the out-of-band (OoB) radiation also contributes to the CDU. Using simulation we can also determine the OoB effect rigorously. The study in this paper demonstrates that the impact of BB and OoB effects on CDU can be well predicted by simulations.

8880-17, Session 7

## Color balancing for triple-pattern lithography with complex designs

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With the minimum feature size keeps shrinking, there are increasing difficulties to print these small features using one exposure (LE) or double exposures (LELE). To resolve the inherent limitations for current lithography techniques, triple patterning lithography (LELELE) has been widely recognized as one the most promising alternatives for 14/10nm technology node. We have presented the first optimal algorithm in the literature to guarantee to find an optimal solution if one exists for standard cell based designs (in ICCAD 2012). In this paper, we will further extend our algorithm to balance the three mask usage for complex designs.

In practice, the designers are more interested in finding an optimal decomposition with none of the three masks overwhelms the other both locally and globally. This color balancing issue is of crucial importance to ensure that consistent and reliable printing qualities can be achieved. By balancing the mask usage both locally and globally, the process variations of the printed features are well controlled and more robust and well-behaved printing characteristics are expected. With three balanced masks, we can maximally benefit from the manufacturing process, and minimize the printing interference of the features in the same mask.

To the best of our knowledge, none of the previous works addresses the global and local coloring balancing issue for both simple and complex designs. A simple heuristic is proposed in our previous work to handle color balancing for simpler designs. However, it is only applicable for simple designs without stitches, and cannot guarantee local coloring balancing, which is more meaningful and crucial in practice. The problem of balancing the three masks, both locally and globally, for complex designs is still a challenging and unresolved issue.

For the previous paper, the algorithm runs in polynomial time, and guarantees to find a legal TPL solution if one exists. For complex designs, our algorithm guarantees to compute the solution with minimum number of stitches. In this paper, we extend our previous optimal algorithm to handle coloring balancing for standard cell based complex designs. We devise an approach which is capable of optimizing coloring balancing and minimizing the number stitches. This new approach is very efficient and robust, and guarantees to find a color balancing decomposition while achieving the optimal number of stitches at the same time. Both global color balancing scheme and local color balancing scheme are addressed. For the largest benchmark with over 10 million features, experimental results show that the new approach achieves almost perfect color balancing with the runtime less than 2 hours.

8880-19, Session 7

## 450mm wafer patterning with jet and flash imprint lithography

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The transition to 450mm wafers for the manufacturing of integrated circuits is now underway, and is primarily driven by the reduction of cost per wafer. Consortiums have been formed to establish the infrastructure necessary to the transition, with a focus on the development of both process and metrology tools. The lithography tool is central to this development, and Molecular Imprints Inc. has provided the industry with the first advanced lithography platform, the Imprio® 450 capable of patterning a full 450mm wafer. The Imprio 450 was accepted by Intel at the end of 2012 and is now being used to support the 450mm wafer process development demands as part of a multi-year wafer services contract to facilitate the semiconductor industry’s transition to lower cost 450mm wafer production. This paper reviews both the performance of the tool as well as the development of the imprint mask that supports the tool.

The Jet and Flash Imprint Lithography (J-FILTM) process uses drop dispensing of UV curable resists to assist high resolution patterning for subsequent dry etch pattern transfer. The technology is actively being used to develop solutions for memory markets including NAND Flash memory. Recent electrical studies performed at 26nm for meter long serpentine structures have resulted in yields for both opens and shorts of over 90%, and the technology is targeted for pilot operation as early as 2014. J-FIL technology has demonstrated 24nm patterning with exceptional line edge roughness (<2nm LER, 3 sigma) and critical dimension uniformity (1.2nm CDU, 3 sigma) with extensibility to 10nm using a simple single patterning step process.

An image of the Imprio 450 is shown in Figure 1. The platform has a new stage and universal substrate chuck design that enables both 300mm and 450mm wafers to be processed without interruption. The system is fully automated for handling both wafers and masks. The maximum field size is 26mm x 33mm. A printed 450mm wafer is shown in Figure 2.

The imprint masks, which are compatible with existing 6025 tooling, are supplied by Dai Nippon Printing. An example is shown in Figure 3a. Early test masks contained a variety of feature types, with a minimum critical dimension of 26nm. An SEM mask image, with lines as small as 26nm, is shown in Figure 3b

First printed images from early test wafers are shown in Figure 4. 28nm lines were completely resolved on the mask, and therefore resolved during the J-FIL process. Figures 4a and 4b show 28nm horizontal and vertical dense features, respectively. 40nm contacts on an 80nm pitch were also resolved. In addition contacts as small as 30nm on a 120nm pitch were printed. Performance updates will be reported for both masks and the tool, and a discussion on future applications of the tool will also be presented.

8880-100, Session 7A

## 2013 Mask Industry Survey *(Invited Paper)*

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A survey supported by SEMATECH and administered by David Powell Consulting was sent to semiconductor industry leaders to gather information about the mask industry as an objective assessment of its overall condition. 2013 marks the 12th consecutive year for this process. The survey has been designed with the input of semiconductor company mask technologists and merchant mask suppliers. Topics include general mask information, mask processing, data and write time, yield and yield loss, delivery times, maintenance,

and returns. Within each category are multiple questions that result in a detailed profile of both the business and technical status of the mask industry.

While each year's survey includes minor updates based on feedback from past years and the need to collect additional data on key topics, the bulk of the survey and reporting structure have remained relatively constant. A series of improvements is now being phased in to add additional value, to a wider audience, while at the same time retaining the historical content required for trend analyses of the key metrics. Additions in 2013 include topics such as critical mask infrastructure and top challenges. The survey will be expanded in 2014 to include input from the mask end users, and suppliers to the mask shops, to provide multiple viewpoints of the mask industry. These expansions beyond the historical topics are aimed at identifying common issues, gaps, and needs. They will also provide a better understanding of real-life mask requirements and capabilities for comparison to the International Technology Roadmap for Semiconductors (ITRS).

8880-56, Session PTue

## High-fidelity dummy fill printing with repair OPC

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Dummy fill plays a crucial role on both controlling topography uniformity and ensuring device performance by manipulating homogenous pattern density. There are several types of fill to achieve this purpose on advanced technologies. The conventional way is to place them out of optical ambit range from main features as reference for Optical Proximity Correction (OPC) procedure, but it degrades the FILL performance due to leaving considerable empty space between FILL and main features. The aggressive way is to place FILL as close as main features to perfectly achieve uniform pattern density. However, in this way, it's challenge to produce defect-free FILL in ORC (Optical Review Check) without applying model-based OPC on FILL which boost the OPC cycle time significantly. In this paper, we propose a novel approach by in-stage Repair OPC technique to not only accurately print aggressive placement FILL but also reduce the impact of run time cost on full chip OPC processing.

8880-57, Session PTue

## Phase preservation study on ArF mask for haze-free mask resist strip and cleaning

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Ozonated water, as an alternative to a Sulfuric - Peroxide Mixture (SPM), was introduced to the resist strip and cleaning processes to prevent surface haze formation through the elimination of sulfuric acid from these processes. [1] [2] [3] [4] [5] However, it also was found to cause significant change of optical characteristics and CD-linewidth shift on ArF 6% attenuation phase shift masks (AltPSM). Although the use of 172nm Excimer UV light irradiation treatment before the clean could improve the above-mentioned shifts, after several clean cycle, this phase/CD preservation effect would be dramatically degraded.[6] [7] [8]

In this paper, a novel approach of phase preservation to use dry treatments based on reactive plasma Asher as part of acid-free resist strip or cleaning process is introduced. [9][10] We have investigated on the surface material integrity and CD stability of MoSi based shifters and compared with above-mentioned approach of 172nm UV light irradiation treatment, and tried to illustrate and explain the principle. Not only Asher process but also UV irradiation, is supposed to be kind of oxygen activation process to accelerate oxidization on MoSi based shifter of ArF AltPSM masks, and created passivation layer would stand out for wet cleaning; furthermore, plasma Asher process is in prior to UV irradiation. As shown in Cross-section profiles on the masks without and with Asher process, although the deference is very limited, it may be proved that a thin passivation layer was created on the surface and side of MoSi based shifter after Asher process.

8880-58, Session PTue

## A new mask linearity specification for EUV masks based on time dependent dielectric breakdown requirements

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When compared to conventional chrome absorber masks, electron beam patterning of EUV masks requires additional corrections to account for intermediate range electron backscattering from the mirror and tantalum based absorber layers. Neither the e-beam systems nor the Optical Proximity Correction software are able to compensate for these effects because the range of the effect is outside their consideration. Hence additional Mask Proximity Correction (MPC) software is needed to correct the mask writer data prior to exposure.

The additional scattering causes Critical Dimension (CD) errors which are dependent on the pattern density in an area surrounding the feature of interest, where the area size is characteristic of the additional intermediate range electron backscatter. Setting the performance requirements and evaluation criteria for such correction software must be done with care. We must choose test configurations which have significant impact on device performance and yield, and we must include the uncorrected residual errors in the error budgets for the wafer fabrication. Choosing poorly has obvious consequences in wafer fabrication. But being too conservative can also be expensive in terms of mask data preparation time and cost.

In order to resolve these questions, we examined the various lithography layers for next generation fin-FET logic fabrication. We considered not only the lithographic layers and their inter-relationships on the wafer, but also the impact of OPC and Design for Manufacturing (DFM) software on the mask design, and the structures allowed by the design rule restrictions.

Most lithography layers in the wafer stack exhibit very low pattern densities, even for single layer patterning with EUV. With low peak densities, we do not expect significant errors which would require MPC. The first metal layers, however, have densities of about 50% and are among the tightest pitches printed on the wafer.

Time Dependent Dielectric Breakdown (TDDB) requirements are very significant for the early metal layers. Lateral spacing between metal wires and inter-layer vias must be maintained above a minimum value to insure long term reliability. All sources of relative edge placement error between the edges of concern must be considered in the wafer processing error budgets. For the metal to via cases, this includes Critical Dimension Uniformity (CDU), Line Edge Roughness (LER) and Overlay between layers.

A new mask linearity specification is needed for the TDDB requirements. Dense lines through pitch (equal lines and space) cannot have TDDB issues except at minimum metal spacing. MPC retargets isolated features so we do not have printing issues with isolated minimum size metal lines. We propose a specification on the minimum metal space through pitch as the critical feature for TDDB. The residual error after MPC correction must be quite small to satisfy the wafer processing budgets, since the error will be systematic.

8880-59, Session PTue

## A study on the chromium surface damage in the structure of a silicon oxynitride hardmask on the chromium surface of PSM blank

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A thin silicon oxynitride hard mask on the PSM blank is needed for the feature patterning with the size smaller than 70 nm. It is a good material for hard mask. However, the electrical property of silicon oxynitride with the thickness smaller than 10 nm causes the chromium surface damage during the mask processes. From the measurement of the surface damage, we figure out that the chromium surface damage is originated from the charging and the dielectric breakdown phenomena.

In our present work, two types of silicon oxynitride film with the thicknesses of 5, 10, 15 nm are tested for verifying optimal mask fabrication processes. We find that the occurrence of ESD damage is related to the thickness of silicon oxynitride hard mask and mask fabrication process conditions. The optimal fabrication process condition for silicon oxynitride thin film hard mask structures which never break down will be discussed.

8880-60, Session PTue

## In-die mask registration measurement on 28nm-node and beyond

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As semiconductor go to smaller node, the critical dimension (CD) of process become more and more small. For lithography, RET (Resolution Enhancement Techniques) applications can be used for wafer printing of smaller CD/pitch on 28nm node and beyond. SMO (Source Mask Optimization), DPT (Double Patterning Technology) and SADP (Self-Align Double Patterning) can provide lower k1 value for lithography. In another way, image placement error / overlay control also become more and more important for smaller chip size (advanced node). Mask registration (image placement error) and mask overlay are important factors to affect wafer overlay control/performance especially for DPT or SADP.

In traditional method, the designed registration marks (cross type, square type) with larger CD were put into scribe-line of mask frame for registration and overlay measurement. However, these patterns are far way from real patterns. It does not show the registration of real pattern directly and is not a convincing method. In this study, the in-die (in-cell) registration measurement is introduced. We extract the dummy patterns that are close to main pattern from post-OPC (Optical Proximity Correction) gds by our desired rule and choose the patterns that distribute over whole mask uniformly. The convergence test is demonstrated in this study.

8880-61, Session PTue

## Alternative material to mitigate chrome degradation on high volume ArF layers

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One of the objectives of a robust optical proximity correction (OPC) model is to simulate the process variation including 3D mask effects or mask models for different mask blanks. Assuming that the data of different reticle blanks is the same, the wafer data should be a close match for the same optical proximity correction (OPC) model. In order to enhance the robustness of the OPC model, the 3D mask effects need to be reduced. A test of this would be to ensure a close match of the so called fingerprints of different reticle blanks at the wafer level. Features for fingerprint test patterns include “critical dimension through pitch” (CDTP), “inverse CDTP”, “tip-to-tip” and “linearity patterns” and CD difference of disposition structures. In this manuscript the proximity matching of 2x metal and implant layers on different reticle blanks will be demonstrated. The results of the investigation of the 3D mask effects including the influence of the reticle writer, as the proximity matching will be affected by the 3D mask even if the same writer is used, and etch process will be presented. We will also investigate the influence of reticle blank material including reticle process on isolated and dense features upon the proximity matching for 28 nm 2x metal and implant layers.

8880-62, Session PTue

## OPC modeling using AFM CD measurement

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Most important factors in OPC model building will be sampling data for model calibration. Sampling pattern coverage and its wafer CD can directly impact to model’s prediction accuracy. Normally wafer CD extraction can be performed by CD-SEM(Secondary Electron Microscophy). However CD-SEM has its own metrology errors due to electron charging effect and top-view measurement algorithm. Shrinkage of photo resist during SEM measurement could enhance the error. Therefore, models calibrated with CD-SEM data always are exposure to the risk to lose prediction accuracy. To get rid of such risk, physical CD measurement by AFM(Atomic Force Microscopy) tool have been introduced. We will demonstrate that how CD-AFM data can be used in OPC modeling and will show possibility to get a more predictive model by using CD-AFM data.

8880-63, Session PTue

## Increased depth of focus through wave-front coding: using an off-axis zone plate lens with cubic phase modulation in an EUV microscope

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The SHARP-instrument (SEMATECH High-NA Actinic Reticle review Project) is a microscope designed for pattern and blank inspection on EUV-Lithography masks at 13.5 nm wavelength. The authors are extending the capabilities of the tool by implementing wave front coding as a complementary imaging mode.

Wave front coding is a technique that increases the depth of focus of an incoherent imaging system without affecting its resolution and light gathering power. This is achieved by altering the phase of the light in the pupil plane by adding a cubic term. The point-spread function of the resulting system is virtually focus-independent over a range exceeding the depth of focus of the unmodified system by an order of magnitude. Modulation of the phase produces an intentionally disturbed image. Deconvolving the data provides the undisturbed image. The computational power of contemporary processors allows doing this calculation in less than a second, depending on the image

size. The resolution of the resulting image is close to the diffraction limit of the unmodified system. Increased depth of focus is achieved at the expense of some dynamic range.

Cubic phase modulation is commonly realized by adding a phase mask to the imaging optics. The authors have designed and nanofabricated zone plate lenses with a modified pattern that combines focusing power and wave front coding in a single optical element.

SHARP uses Fresnel zone plate lenses in an off-axis configuration as the objective lenses. In this geometry, the image plane is tilted with respect to the detector, leading to a focal gradient across the image. Using wave front coding, a depth of focus can be achieved that allows sharp images to be obtained across the instrument's entire field of view.

The focal length of Fresnel zone plate lenses is a function of wavelength. This causes chromatic aberrations and limits the acceptable bandwidth of the source. Wave front coding reduces the chromatic aberrations significantly. This allows systems relying on Fresnel zone plate lenses to operate at higher power by using higher bandwidth.

The influence of partial coherence on the performance of wave front coding can be studied using SHARP's Fourier-synthesis illuminator, which provides controllable illumination coherence. The study clears the path to further applications of wave front coding zone plates in lab- and synchrotron-based microscopes and metrology tools.

The authors have demonstrated wave front coding in visible-light optical systems using Fresnel zone plate lenses in an off-axis configuration similar to SHARP. Experiments using EUV light are currently in preparation.

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8880-64, Session PTue

## A study of the defect detection technology using the optic simulation for the semiconductor device

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As the design rule of the semiconductor device shrinks down, the importance of the defect inspection on semiconductor fabrication is increasing because of the effect of small defects on chip failure. Usually, both e-beam inspection equipments and optic inspection equipments are used to detect defects on semiconductor wafers, while optic equipments are primarily used because of their much higher throughput compared to e-beam tools. However, due to the limit of the optical resolution, it has been very hard to detect sub-20nm pattern defects. To detect these defects we have tried to reduce the wavelength and enhance the contrast of optical images. Since it takes much cost to reduce the wavelength below 200nm, the enhancement of optical image contrast is becoming the powerful method.

In most cases, optic inspection equipments use spatial apertures in illumination and collection part to enhance the contrast of optical images. However, it is very difficult and tedious to find the optimized inspection condition for all pattern defects using S/N ratio analysis with the experimental data. The optical imaging simulation tool based on FDTD (Finite Difference Time Domain) calculation and Fourier optics can give the estimated signal intensity with a given optical condition. As we simulate defect signal intensity with available inspection conditions, we can reduce the experimental S/N ratio analysis time.

With the optical imaging simulation tool we analyzed sub-20nm defects in the pattern which consists of 20nm-line and 20nm-space, and has three layers on silicon substrate. Especially, we simulated the pattern defect which is at the bottom layer not on the pattern surface. Since the defect is at the bottom layer, it is very difficult to find the best inspection condition with the experimental S/N ratio analysis method. However, if we use the optical imaging simulation, it is much easier to find the optimized inspection condition. We analyzed the defect signals for various wavelengths and the polarization effect. The signal represents the defect contrast calculated as following formula. (Defects Signal = (Background level – Defect level) / Background level) The dramatic dependency of the wavelength was got in this result. It can be understood by the difference of the penetration depth in accordance with the illumination wavelength. The longer wavelength can reach the defect location, but the light with the shorter wavelength may be blocked at the surface poly-silicon material. In analyzing the polarization effect, the vertical direction (90o) to the pattern showed much greater signal compared to the parallel polarization (0o). Since the poly-silicon pattern absorbs the light of parallel polarization, 0o polarization cannot travel into the bottom layer. With this condition we inspected the wafer which has this kind of bottom defects. As a result, we were able to get the same result as that of the simulation.

FDTD based optic simulation tool is investigated to find an optimal condition for detecting a defect using optic inspection tools. The simulation results give us the suitable wavelength, the polarization condition, and the results that are coincident with the experimental data. It is expected that the proposed simulation methodology helps engineers get more accurate optic condition in shorter time.

8880-67, Session PTue

## Mask contamination study in electron and ion-beam repair system

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At 32nm technology node and beyond, the number of defect to be repaired increases because pattern size is shrunk and the detection ability of inspection tool is higher than before.

In repair step, mask surface is exposed to the various contaminations such as contaminations from vacuum chamber wall, reaction gas for repair etc.

Although contaminations deposited on mask surface are removed by followed cleaning process, it makes surface reflectance differences detected by high resolution inspection step.

This reflectance change of repair scan area is detected during inspection which is big burden for mask making because the number of scan area requires more time to confirm and it needs AIMS simulation if there is any issue on the area. Especially, this issue is serious on MoSi absorber of BIN mask.

In this paper, we demonstrate the findings of contamination source and the root cause of contamination using surface analyzing methods, ToF-SIMS and XPS.

Also, we propose the strategy to minimize and remove the contamination without damage on mask surface.

8880-68, Session PTue

## Model-driven design target movement to resolve design hot spots through image quality enhancement

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Nowadays, increasing numerical aperture (NA) and reducing wavelength of exposure tool are no more available to meet shrinkage demands of device nodes. For several years, the scanner is remaining in ArF immersion of 1.35NA. The size of NA is not able to enlarge due to failure of finding high refractive index materials for the projection lens. The real employment of EUV takes more time to resolve problems such as source power, mask defects, resist, etc. Double patterning technology (DPT) is developed and takes position as the alternative patterning solution to device node shrinkage. Although DPT is applied, decomposed layer confronts its resolution limit due to rapid shrinkage speed. Pixelated source and mask correction using process aware OPC and inverse lithography method are actively employed to enhance process margin. The process margin enhancement by moving design target location is tried but not actively used. The rule based design target movement cannot be applied to random patterns but be applied to limited numbers of patterns. Model driven design target movement is necessary to cover general random patterns.

In this paper, random 1-dimensional line and space patterns are used as design layouts. Image qualities of hot spot points are below resolution limit. The pixelated source and mask correction using inverse lithography technology are used to maximize process margin of hot spot points. However, image qualities of them don't reach resolution threshold and cannot be resolved. The design target locations are moved to release their pitches and maximize the image qualities. Image slope, Imin, Imax, and controlled CD/space enlargement are used as governing cost functions and are optimized automatically throughout the interesting region. The boundaries of hot spot fixed regions are also blended by automatic treatments. NILS and MEEF of hot spot regions are observed to increase above patterning threshold after design target location optimization. We obtain 50% enhancement of image quality and succeed to resolve hot spot patterns.

8880-70, Session PTue

## Sensitivity analysis for OMOG and EUV photomasks characterized by UV-NIR spectroscopic ellipsometry

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Microelectronics development proceeds towards smaller features sizes and higher integration densities. This development demands for high-end photomasks with decreased critical dimensions (CD). The ITRS shrink roadmap specifies the CD uniformity (CDU) with 0.9 nm for EUV masks of the 13 nm node in year 2020. This leads to a major challenge for the accuracy of metrology techniques. It has been demonstrated that optical scatterometry and ellipsometry are very powerful and accurate methods to characterize photomasks non-destructively. Structural parameters on the masks are reconstructed from the optical measurement data by solution of the Maxwell equations, e.g. by rigorous coupled wave analysis (RCWA).

This paper will focus on the application of spectroscopic ellipsometry in the UV-NIR spectral range. The advantage of using the UV-NIR range is the high quality standard reached during decades of equipment development, the relatively low implementation costs as well as the decoupling of the multilayer stack errors from CD deviations on EUV masks.

The goal of this study is the specification of a spectroscopic ellipsometer for photomask characterization. To determine the required accuracy for measuring CD values in the sub-nm range, a sensitivity analysis for the crucial ellipsometer parameters was done. Therefore, the response of the Fourier coefficients ? and ? to variations in critical features (CD and pitch) was characterized for different hardware configurations. The sensitivities are determined by microspot ellipsometer measurements in 300 – 1000 nm spectral range and by data modeling using the RCWA method. Industrial EUV and OMOG photomasks consisting of line/space structures with pitches between 40 and 1000 nm and variable duty cycles were evaluated.

It was found that sensitivities to CD variations are fundamentally different for OMOG and EUV masks. High measurement sensitivities were found in a limited spectral range (~ 100 nm) located near the first order of reflection for the EUV reflection mask. For the OMOG transmission mask, the sensitivity values are smaller but measureable in a broader spectral range. This effect can be understood by Rayleigh singularities, which are different for reflection and transmission masks. The sensitivity analysis shows that ellipsometers for 13 nm node photomask evaluation require a measurement precision of about 0.001 for ? and ? values, within a spectral range depending on mask properties. Furthermore, the data show that pitch variations could be determined with high accuracy down to pitches of 140 nm, where the Rayleigh singularities move out of the spectral range of the applied measurement system.

In this paper we show, that UV-NIR ellipsometry is qualified to characterize photomasks of the 13 nm technology node in 2020. The DUV wavelength range below 300 nm is not required until 2020 to realize the required measurement accuracy.

8880-71, Session PTue

## Fleet matching performance for multiple registration measurement tools

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Currently semiconductor industry drives the 193nm lithography to its limits, using techniques like double exposure, double patterning, mask-source optimisation and inverse lithography. These requirements trend to full in-die measurement capability of photomask metrology for registration. Especially, overlay becomes more and more critical and must be ensured on every die. For this, Carl Zeiss SMS has developed the next generation photomask registration and overlay metrology tool PROVE® which is already well established in the market. To ensure in-die measurement capability, sophisticated image analysis methods based on 2D correlations have been developed. Recently, a second tool generation with reduced fab footprint has been developed and introduced at different mask shops.

A key component for registration tool users is the cross site manufacturing flexibility given by the matching capability of all its metrology tools. Therefore all PROVE® tools offer a tool matching procedure based on 2D Golden Grid references. In this paper we first review the optimal length standard and golden grid matching procedures of modern registration metrology tools. Systematic errors in fleet matching based on illumination differences, thermal expansion-based issues or line width roughness are addressed. The tool matching performance of PROVE® tools is demonstrated by comparing 5 different tools of the first and second generation. All

tools are well within accuracy and longterm repeatability specification which considerably reduces the statistical error contribution of the tool matching performance. For grid matched tools the final cross tool registration error is shown to be below 1nm.

8880-72, Session PTue

## The recovering method of etch chamber condition by using the optical emission spectroscopy monitoring system

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The etch chambers has been cleaned by wet process and replaced with new parts to maintain etch chamber perfectly clean. However, the wet chamber cleaning results in following issues. One of issues is that the critical dimension mean to target (CD MTT) and phase-shift would be changed due to the variation of etch rate, which is generally caused by the new parts and wet chamber cleaning process. Another issue is that the wet cleaning takes too long time to recover the chamber condition. Moreover, the production will be stopped until recovering the chamber condition. Therefore, the recovering time should be minimized to keep the high productivity of etch tool.

The change of chamber condition during the plasma seasoning can be monitored with the optical emission spectroscopy (OES) system. The optical emission intensity represents the concentration of materials in plasma and the surface condition of chamber. The OES peaks were collected during the plasma seasoning, which was applied to remove the moisture and residues from wet cleaning and to recover the chamber condition. The correlation of the OES peak intensity and chamber condition was verified by the CD and phase-shift difference between pre and post chamber cleaning. This methodology was applied to reduce the seasoning time, which occupies 80% of whole preventive maintenance (PM) time.

8880-73, Session PTue

## Analysis of EUV mask durability under various absorber etch conditions

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During EUV exposure, more frequent mask cleaning is essential for removing not only particles from lack of pellicle but also the carbon contamination due to accumulative EUV exposure. Because of this reason, process improvement for minimize corrosion and etching of the Ru capping layer is urgently needed. In this work, the influence of TaBN absorber etch condition on Ru integrity followed by repetitive cleaning was evaluated and the effects on long-term durability of Ru are compared under various cleaning conditions. Consequently, it was shown that Ru durability was strongly influenced by the gas contents and over etch time of absorber dry etch, not only as a function of cleaning conditions.

8880-74, Session PTue

## Finite-element based EMF simulation methods for computational lithography and computational metrology in the DUV and EUV regimes

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Performance of lithography at DUV and EUV wavelengths can be pushed using computational methods. Further, computational methods are an integral part of optical metrology setups in this field.

We develop and investigate finite-element methods for electromagnetic field (EMF) simulations. In previous contributions our methods have been applied to computational lithography tasks like investigations of 3D effects, source-mask optimization, analysis of the impact of line edge/width roughness and defects, as well as to computational metrology tasks like CD metrology at EUV wavelengths and metrology of 3D patterns [1-4].

The challenge for EMF solvers is typically efficiency (i.e., to achieve highly accurate results at low computation times). Finite-element methods allow for high efficiency due to accurate geometrical modelling, adaptive meshing strategies, and higher-order convergence. In simulation tasks requiring high accuracy this can typically outperform other rigorous simulation methods. In this contribution we discuss methods for further performance improvements. We present an efficient finite-element method for computation of derivatives with respect to geometry parameters (sensitivity analysis). We further discuss hp-finite-element methods. hp-FEM uses different classes of finite-element ansatz functions on different patches of the geometry mesh. We present application of these methods to typical simulation setups in computational lithography and computational metrology and we quantify corresponing speed-up factors in a convergence analysis.

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8880-75, Session PTue

## Metrology variability and its impact in process modeling

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Proximity Effects in electron beam lithography impact feature dimensions, pattern fidelity and uniformity. These effects may be corrected by dose and geometrical modulation [1]. In order to correct these effects properly, an accurate modeling of the complete fabrication process behavior is crucial. However, the quality of the estimation relies not only on the model used but also on the procedure employed to determine the values of the parameters of the model [2, 3], namely the calibration. This is better addressed by performing one or several cycles of exposure and measurement, providing the metrology data to an optimization algorithm.

Therefore, it is possible to identify that the reliability of the metrology procedure (and its repeatability) has an impact over the calibration of the model. Hence it affects the accuracy and the possibility of predicting and compensating for proximity effects on a wafer or mask and, above all, the final quality of the exposure after correction.

This paper aims to answer two questions:

1. Observe and quantify the metrology variability;

2. Demonstrate the variability impact over the process model calibration.

The first question was addressed by an experimental evaluation comparing the results of two metrology processes, ran in two different cleanroom environments over the same exposed wafer. The wafer contained 5 identical chips, each presenting over 200 patterns usually employed for model calibration (figure 1). The variability of metrology over the five identical patterns was then extracted. Moreover, the wafer was measured by two different CD-SEMs (from two different companies) in slightly different locations (to prevent degradation impact). In this way, the impact of employing a different recipe (and a different machine) was evaluated. Figure 2 shows (a) the variability between different measurements performed using the same recipe (and, therefore, the same CD-SEM) and (b) the difference between the mean values (out of 5) obtained by each metrology recipe (different CD-SEMs). It is possible to observe a relevant divergence between the two machines, presenting most of the measurements at least 5nm difference. Moreover, in several points this difference is above 15nm, reinforcing the idea that the measurements have an important impact over the model calibration.

The second question was addressed by performing several calibration procedures by comparing the calibration results in the presence of noise injected in the input data. Three different input data sets were used in this experiment: synthetic data from a PSF model, measurement data from CD-SEM 1 and that from CD-SEM 2. For each input data, different variations were applied (either a stochastic variation or deterministic one, of different magnitudes). The impact was then evaluated both for each model parameter value and on the final proximity effect correction result, which reflects the impact of metrology variability on the resulting wafer.

In this work the variability impact over process modeling was demonstrated. Based on this information, it is possible to better determine the number of metrology patterns that are required for increasing the robustness of a model calibration procedure.

8880-76, Session PTue

## Mask topography effect characterization by rigorous model and its implementation for full-chip simulation

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In the 28 nm technology node and beyond, the mask topography (Mask3D) effect has become a considerable factor to largely influence the full chip mask synthesis process. In order to accurately predict the Mask3D effect, multiple approaches have been provided to resolve this issue. Rigorous model has been proved to have the capability to most accurately predict the Mask3D behavior, while the runtime efficiency is too poor to be used for a full chip mask implementation.

Recent study has shown the significant improvement by using emulated data for compact OPC model optimization. The basic idea is to use rigorous model as a guidance for the compact model construction, which can both reduce the amount of input empirical data and increase the flexibility and reliability of the fitting process in the compact model.

In this paper, we can further expand the rigorous-compact modeling flow to help achieve a full chip model for Mask3D. First, through experimental results, we can show that Mask3D effect can be accurately characterized by a rigorous model. The characterization result can be thus further implemented for a full chip simulation. The model flow presented in this paper can finally show an accurate full chip simulation result and hints the necessity of the adoption of the rigorous simulation for the construction of the full chip Mask3D modeling.

8880-77, Session PTue

## Pupil shaping and coherence control in an EUV mask-imaging microscope

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In photolithography, imaging properties are highly sensitive to the mask illumination conditions. While this fact is used to optimize imaging in a variety of ways, it has significant implications for mask-imaging microscopes that are used to study the optical properties of patterns and defects. Current step and scan wafer printing systems rely on customized pupil-fill patterns and off-axis illumination to enhance the aerial image resolution and depth of focus1. Therefore, the study of the optical properties of EUV reticles is improved by tools that provide matching illumination and imaging configurations.

On the new SEMATECH High-NA Actinic Reticle review Project (SHARP), we are investigating the effect of pupil-fill patterns and partial coherence settings on EUV reticle images to deepen our understanding of its performance, and improve the emulation of image formation in arbitrary printing tools. SHARP is an EUV microscope developed as the successor of the SEMATECH Berkeley Actinic Inspection Tool (AIT)2. It is equipped with a unique, MEMS-based Fourier synthesis illuminator3 that generates arbitrary, customized pupil fill patterns to control the illumination partial coherence. The high-magnification objective lenses are an array of interchangeable Fresnel zoneplates with 4xNA values ranging from 0.25 to 0.625.

The AIT's fixed pupil fill pattern and relatively high illumination coherence (? below 0.2) made it difficult to accurately quantify the behavior of phase shifting reticles, buried defects, and inherent mask roughness. Many phase-shifting mask patterns show stronger effects under coherent illumination: while this can be useful for detection, it limits the effective emulation of printing tools.

We have used SHARP to inspect isolated and dense features with half pitch as low as 55 nm using lenses with a range of NA values, and common illumination patterns, such as annular, dipole and QUASAR™. We will show the effect of these parameters on important, measured pattern parameters, including contrast, normalized image log-slope, and depth of focus and we will compare the results with the values obtained with conventional illumination.

We have also studied the effect of partial coherence on the imaging of native and programmed phase defects, and on multilayer roughness observed in bright mask regions. The latter topic is important for expanding our understanding of the causes of LWR, and it is very difficult to measure with other techniques.

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8880-78, Session PTue

## An efficient and accurate full-chip mask 3D model for off-axis illumination with effective mask rigorous library

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In the sub-28 nm technology node, mask topography effect (Mask3D) is a must-do factor that need be considered during the full chip modeling and OPC process. At the same time, off-axis illumination (OAI) is another factor that need be considered together with Mask3D effect modeling. In the existing rigorous-compact flow, although normal incident optics can be easily captured and compact model can be fit on top of the empirical data, to handle all kinds of OAI optical sources with different types of geometries, it is extremely difficult and costly to generate enough empirical data for compact model fitting.

In this paper, we propose a completely novel algorithm to solve the OAI issue altogether with full chip Mask3D model. In this approach, for a specific mask stack, a rigorous-based nearfield library will be constructed, with mask structure and all possible optical source points pre-calculated. Then, once the exact optical source is defined, we can synthesis the effective nearfield based on the nearfield library to finally capture the OAI behavior on top of Mask3D effect.

Our proposed idea has been proven to be efficient for the full chip simulation as well as the following OPC process, without any runtime penalty compared to the normal incidence optic source. Experimental results also show that the CD RMS for 2D patterned test chips with OAI sources could be as small as <1nm. Our approach also successfully predicts the pattern dependent shift of best focus. The efficiency and accuracy proves the capability of our proposed modeling method for OAI with Mask3D.

8880-79, Session PTue

## In-die mask registration for multipatterning

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193nm immersion lithography is the mainstream production technology for the 20nm and 14nm logic nodes. Considering multi-patterning as the technology to solve the very low k1 situation in the resolution equation puts extreme pressure on the intra-field overlay, to which mask registration error is a major error contributor [3]. The International Technology Roadmap for Semiconductors (ITRS [1]) requests a registration error below 4 nm for each mask of a multi-patterning set forming one layer on the wafer. For mask metrology at the 20nm and 14nm logic nodes, maintaining a precision-to-tolerance (P/T) ratio below 0.25 will be very challenging.

Mask registration error impacts intra-field wafer overlay directly and has a major impact on wafer yield

We will discuss a solution to support full in-die registration metrology on reticles.

8880-81, Session PTue

## Improving wafer level CD uniformity for logic applications utilizing mask level metrology and process

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Critical Dimension Uniformity (CDU) is one of the key parameters necessary to assure good performance and reliable functionality of any integrated circuit (IC). The extension of 193nm based lithography usage combined with design rule shrinkage makes process control, in particular the wafer level CDU, an extremely important and challenging task in IC manufacturing.

There are several contributors to the final wafer level CDU such as mask CD uniformity, resist process, scanner fingerprint, wafer topography, etc. In this study the WLCD-CDC closed loop solution offered by Carl Zeiss SMS was examined. This solution aims to improve the intra-filed wafer level CDU without the need to run wafer prints and extensive wafer CD metrology. It combines two stand-alone tools: The WLCD tool which measures CD based on aerial imaging technology while applying the exact scanner-used illumination conditions to the photomask and the CDC tool which utilizes an ultrafast femto-second laser to write intra-volume shading elements (Shade-In Elements™) inside the photomask bulk material. By controlling the lateral density of those shading elements, the light dose going through the photomask down to the wafer is being controlled, hence the wafer level intra-field CDU improves.

Unlike DRAM and FLASH memory devices, logic and system on chip (SOC) devices are comprised of a variety of features which have different CD and MEEF values. In this work several logic features were evaluated on a production-like photomask which provide a good representation of the variety of features existing in logic application. In this work the CDU similarity of the different features was investigated as well as the linearity and proximity behavior. The main findings show that the CDU errors of the targeted (critical) feature have been effectively eliminated, in addition, the CDU of all other features have been significantly improved as well. It was found that the different features share similar global CDU errors which are mainly differentiated by different MEEF. This gives the IC manufacturer the freedom to choose the most critical feature as the process target in order to finally get the best device performance. Furthermore, intensive investigation of the impact of CDC process on CD linearity behavior provides evidence that the applied dose change/light attenuation by CDC shows a linear correlation to CD change at wafer level as measured by WLCD - the linearity behavior is being maintained while applying the CDC process which is an extremely important result.

8880-82, Session PTue

## A fast convolution method using basis expansion for highly efficient intensity calculation in mask optimization

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Inverse lithography technology (ILT) treats mask synthesis as an inverse problem especially when dealing with 45 nm technology node and beyond. Most ILTs use pixel-based mask representation to perform mask optimization. To describing mask patterns more accurately and obtaining better image quality, finer grid representation is inevitable, thus resulting in large-size mask representation and heavy computational cost.

Since convolution is the most computational intensive operation in the mask optimization, in this work we proposed a fast convolution method called convolution using basis expansion (CBE) method to resolve above computational issues. Convolution operation on fine grids is approximated by a few convolutions on coarse grids.

The CBE method process can be elaborated as: 1) Project mask and kernel matrices from fine grid representation to coarse grid representation under certain basis functions. A large size matrix that defined on fine grid representation is divided into many equal-size small matrices. Each small matrix is expanded based on a basis matrix set, similar to DCT or wavelet transformations. The expansion coefficient of all the small matrices under a certain basis matrix then forms a new matrix. This matrix with the reduced matrix size can be considered as the projection of the original large matrix for the given basis matrix. We select several basis matrices to get a series of projections matrices to form the coarse grid representation of the original large matrix; 2) Perform mask and kernel convolutions on coarse grids; 3) the convolution result on fine grids is restored by interpolation method.

The selection of the basis set can be arbitrary. In this paper, we compares the convolution accuracy and computational cost using 1) linear basis function; 2)discrete cosine basis function; 3) basis function based on K-L transform for different fine and coarse matrix size ratios n in both 1-D and 2-D conditions. Also, the quantitative interpolation error of cubic spline interpolation function is discussed. Larger n will increase computational efficiency but lower down the convolution result accuracy. It is found that for n, the error originated from interpolation dominates the total error. The error analysis shows that CBE method could be an effective mask optimization framework since the optical kernels are usually smooth and easy to be approximate well by several basis functions. No matter whether the mask is approximated well or not, the error on coarse grids can be very small.

In numerical verification of aerial image calculation, this new method provides almost the same effectiveness and more than 20X running speed improvement comparing to traditional convolution method. The CBE method will show its large effectiveness and efficiency in mask optimization.

8880-83, Session PTue

## Impact of an etched EUV mask black border on imaging and overlay, part II

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The image border is a pattern free dark area around the die on the photomask serving as transition area between the parts of the mask that is shielded from the exposure light by the Reticle Masking (REMA) blades and the die. When printing a die at dense spacing on an EUV scanner, the reflection from its image border overlaps edges of neighboring dies affecting CD and contrast in this area. This is related to the fact that EUV absorber stack has 1-3% reflectance for actinic light. For a 55nm thick absorber the induced CD drop at the edges was 4-5 nm for 27 nm dense lines. Increasing the die spacing would prevent this unwanted exposure but results in an unacceptable loss of valuable wafer real estate thereby reducing the yield per wafer and is thus not a viable manufacturing solution.

In order to mitigate the reflection from the image border one needs to create a so called black border. The most promising approach is removal of the absorber and the underlying multilayer down to the low reflective substrate by multilayer etching [1]. It was shown in the previous study [2] that the impact on CD was reduced to <1 nm for 27 nm dense lines exposed on ASML NXE:3100. The multilayer etching however has induced a pattern displacement of about 3 nm at reticle level in the areas ~15 micron from the black border.

In this work we will continue the study of a multilayer etched black border impact on imaging and overlay. In particular, 22 nm lines/spaces imaging on ASML NXE:3300 EUV scanner will be investigated in the areas close to the black border as well as die to die effects. We will look closer in the CD uniformity budget including impact of flare and DUV OOB light in these areas. Also the impact of reticle pattern placement will be investigated on resolution features at wafer level and as function of mask flatness change due to the multilayer etch.

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8880-84, Session PTue

## Development of inspection system for EUV mask with novel projection electron microscopy (PEM)

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In order to realize EUV mask pattern defect inspection in 16nm node, we have developed a new inspection system with a novel projection electron microscopy (PEM) system and a new mask handling and imaging system, e.g., a high precision stage, an imaging detector, an imaging processing system, and so. on. This inspection system enables us to make the inspection in high resolution and high speed as compared with conventional DUV and EB inspection systems. The new optical system, which comprises an electron beam exposure and an electron imaging optics, has also been developed. The optics are based on the new design concept using new techniques to achieve the features: high energetic electron imaging optics to have low aberration, high transmittance efficiency, e.g., on the ratio of exposure current/emitted current, in the exposure and the imaging optics, respectively. The new handling and imaging system are also based on the design concept of imaging in high resolution by combination operation among the PEM system, the stage, and the detector. In this paper, we describe the basic performance evaluation as concerning these features and the operation: 1) transmittance efficiency of the developed exposure and imaging optics; 2) MTF in hp44~100nm L/S pattern of the developed imaging optics. 3) combination operation for imaging among the PEM

system, the stage, and the detector. This study is supported by New Energy and Industrial Technology Development Organization (NEDO) and Ministry of Economy, Trade and Industry (METI).

8880-85, Session PTue

## A novel method for utilizing AIMS to evaluate mask repair and quantify over-repair or under-repair condition

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The ZEISS AIMS™ platform is well established as the industry standard for qualifying the printability of mask features based on the aerial image. Typically the critical dimension (CD) and intensity at a certain through-focus range are the parameters which are monitored in order to verify printability or to ensure a successful repair. This information is essential in determining if a feature will pass printability, but in the case that the feature does fail, other metrology is often required in order to isolate the reason why the failure occurred, e.g., quartz level deviates from nominal.

Photronics-nanoFab, in collaboration with Carl Zeiss; demonstrate the ability to use AIMS™ to provide quantitative feedback on a given repair process; beyond simple pass/fail of the repair. This technique is used in lieu of Atomic Force Microscopy (AFM) to determine if failing post-repair regions are “under-repaired” (too little material removed) or “over-repaired” (too much material removed).

Using the ZEISS MeRiT® E-beam repair tool as the test platform, the AIMS™ technique is used to characterize a series of opaque repairs with differing repair times for each. The AIMS™ technique provides a means to determine the etch depth based on through-focus response of the Bossung plot and further to predict the amount of MeRiT® recipe change required in order to bring out of spec repairs to a passing state.

8880-86, Session PTue

## Analysis of edge effects in attenuating phase-shift masks using quantitative phase imaging

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Thick mask electromagnetic edge effects for attenuating phase-shift masks (ATT-PSM) are analyzed by extracting phase effects at the wafer plane from a series of through focus AIMS images at 193nm. The abrupt edges of an ATT-PSM can lead to phase distortion of the incident wavefront, creating asymmetric through focus intensity contrast. Here we measure the intensity images through focus and quantitatively recover phase via the Transport of Intensity Equation (TIE). The TIE can determine the effective phase across the photomask as seen by the imaging system.

The Transport of Intensity Equation is a power conservation equation that relates the phase of light at focus to the change of intensity through focus. It uses the gradient of the phase to determine the directions of the Poynting vectors on a given plane; the divergence of the in-plane Poynting vectors is then proportional to the intensity changes perpendicular to the plane. This relationship between phase and intensity reduces to a second order differential equation that can be solved for phase once the intensities through focus are known.

One of the challenges in this study is the numerical aperture of the imaging system, which limits the spatial resolution of the recovered phase. Another challenge is the partial coherence of the light source that leads to intermixing of intensities in the propagating wavefront, thus reducing the quality of the phase recovered by TIE. However, since the phase effects mostly occur near the edges, these effects can be approximated well by polarization dependent thin mask boundary layers deduced from the recovered phase[1].

This paper first overviews the formulation of the Transport of Intensity Equation and its scope as a phase recovery method for applications in lithography. A dry-lab TIE analysis of through focus intensity images generated by an aerial image simulation tool is performed to determine optimum imaging parameters and fundamental limits in a noise free environment. The analysis also looks at the how the recovered phase is affected by adding thin-mask phase edges at the mask. The simulation is compared with experimental results from through focus images produced by an AIMS tool at 193nm for various patterns and measurement conditions; consequently the effects modeled by thin mask phase edges are demonstrated in the experimental system.

We find that the quadrature phase component of the EM edge effect produces the through focus asymmetry observed in the experimental system at the boundary of the phase transition on the ATT-PSM. Data from an attenuating block feature reveals the difference between TE and TM performance near the edges.

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8880-87, Session PTue

## Recovering effective amplitude and phase roughness of EUV masks using an EUV microscope

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Mask roughness at 13.5-nm-wavelength has been examined using actinic scatterometry to show that the effective roughness is generally less than the roughness measured by AFM, however reflectivity variations were not measured [1]. We have developed a method using through-focus image data, collected on an EUV microscope to extract both effective phase and effective amplitude roughness (reflectivity variation) of the reflective multilayer coating. Additionally, because the roughness is extracted from images, the phase and amplitude roughness measured are aligned to each other, so the relationship between the two can be examined. Several EUV masks will be measured using SHARP, an EUV microscope at Lawrence Berkeley National Laboratory. The masks have different substrate roughness and have been measured using AFM before and after multilayer deposition, so the amplitude and phase roughness PSDs can be compared to what is predicted by AFM.

The effective roughness is recovered from speckle images using a deconvolution by applying a mathematical model derived previously [2]. The model enables speckle to be computed from effective amplitude and phase roughness using a single convolution. There is a separate kernel for phase and amplitude, and they produce speckle that adds independently. The kernels of the convolution depend on defocus and the partial coherence of the system. Depending on the illumination and defocus, different frequencies in the roughness are attenuated and produce speckle. By varying the illumination and measuring the same areas at different defocus, it is possible to intentionally couple the effective roughness predictably into speckle, which can then be measured. The speckle is then deconvolved with the kernels corresponding to the illumination and defocus to recover the mask roughness. By varying the illumination and defocus, we will show that the error on the recovered roughness can be reduced.

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8880-88, Session PTue

## EUV mask scatterometry metrology challenges

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Metrology has an important part to play in advancing EUV (extreme-ultraviolet) lithography towards high-volume production. In particular, optical metrology provides a fast, non-destructive method of observing variations in materials and structure geometries across a mask, monitoring contamination or any changes in a mask during mask usage. We present the results of UV-VIS scatterometry measurements of both thin films and 1D and 2D structures on EUV masks. We show how thin film measurements can be used to characterize the thickness and optical properties (n and k) of the EUV mask materials: the anti-reflective coating, the absorber, the capping layer (figure 1) and the Mo and Si multilayer materials. Scatterometry results correlate well with CD-SEM measurements for a variety of pitches and structures (figure 2). We will also report the scatterometry measurement precision, accuracy and matching for EUV structures and compare them to current and future ITRS requirements. While most of the EUV structures can not be measured by scatterometry, some of the structures are measurable due to current EUV mask stack design and EUV material properties. We will discuss such challenges and limitations of EUV mask scatterometry and give an overview of the current state-of-the-art scatterometry measurements on EUV photomasks. Finally, we discuss future directions and look towards the challenges facing EUV photomask metrology in the years to come.

8880-89, Session PTue

## AF printability check with a full-chip 3D resist profile model

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A single model with predictable 3D resist profile is strongly demanded in the advanced technology node to avoid the potential hotspots due to imperfect resist shape and its subsequent etch process. In order to predict the correct 3D profile, not only the bottom CD but also the cross-section CD, sidewall angle, and/or center resist height are used to help the calibration more reliable. Furthermore, starting from the aerial image inside resist, techniques such as Gaussian blur and threshold shifting were commonly employed in the chemically amplified resists (CAR) models to account for the diffusion and quenching effect during the post-exposure bake (PEB) process. However, these mathematical operations were only performed in the 2D x-y plane (wafer plane) which is not true in the real physics world. The chemical diffusion along z direction including the flux in/out across the interfaces mainly controls the final resist cross-section profile.

The resist 3D model proposed previously is in the sense of "multiple-imagedepth models" that each model calibrates the CD data at its corresponding imagedepth individually.[1] The drawback of this approach is that each model works independently only to the specific imagedepth and has no common free parameters and threshold between them. Therefore, it has no prediction power to other non-calibrated resist plane and cannot be a real single 3D resist model.

In this work, we propose a single 3D resist model that takes z-diffusion effect into account. The chemical reaction between acid and base along z-direction is treated as second order effect that can be absorbed into the anisotropic diffusion length. Meanwhile, the resist model in the x-y plane is still kept in general by applying the solution of 2D reaction-diffusion equation. In order to have the contour predictability for arbitrary imagedepth, all models from all calibration planes are optimized simultaneously with a single cost function so that they share the same free parameters and threshold. To keep the 3D resist model as physical as possible, model behavior between imagedepth are related by the solution of 1D diffusion equation that the analytic forms can be derived for certain boundary conditions. Follow the low energy approximation, the initial acid given by the dillC model is proportional to the aerial intensity: H0(z)=1-exp(-dillC*dose*I(z))~I(z). Therefore, the acid z-diffusion is equivalent to calculate a z-diffused TCC that takes the form of linear combination of pure optical TCCs at discrete sampling imagedepth which can be pre-calculated. With this benefit, the 3D resist model offers a more physical approach but adds no runtime concern on the OPC and verification applications. The predicted resist cross-section profiles from our test pattern are compared with rigorous SLITHO simulations and show good matching results between them. The demonstration of the AF printing predicted directly from the cross-section profile indicates the success of our resist 3D model.

8880-90, Session PTue

## HSQ process development for a superior resolution and a reasonable sensitivity for an EB master-mold fabrication for nanoimprint lithography

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Hydrogen Silsesquioxane (HSQ) has been widely used for demonstration purpose in nano-lithography. And, various approaches in developer chemistry had been proposed, such as TMAH solution, organic solvents, and NaOH / NaCl salty developer, to obtain a superior resolution and a reasonable exposure dose required (EDR). ZE520A is another option to pursue the resolution limit. However, since it is a positive-tone resist, dark erosion is significant between holes particularly when hole pitch is 25nm and below because of EB back-scattering. And, holes in the nearest are not isolated but connected.

Our motivation here in this study is to switch the tone, from positive to negative one, in order to make quality bit patterns in pitch 25nm and below. HSQ, a negative-tone resist, would cause residue between the pillars instead. But the residue can be eliminated by etching back to the bottom. So the bit patterns can be produced.

We then studied how we could reduce EDR on HSQ mainly by examining contrast curves. And, we firstly tried to design and exam a "two-step development" process by a combination of an organic solvent developer and the salty developer:

HSQ spin-coating -> PAB -> 1st solvent develop. -> 2nd the salty develop.

A solvent developer for HSQ provides the least EDR, while the poorest gamma value (contrast). A single MiBK development provides EDR (Eth(50%)) of 3?C/cm2 (@100kV). A single development by the salty developer, on the other hand, requires the highest EDR of 2,000?C/cm2 . A contrast curve was obtained when the two-step development was carried out, i.e. the first development by MiBK followed by the second development by the salty developer. And, the contrast curve was almost the same one as the single salty developer provided. No significant effectiveness of the two-step development was found, to reduce the EDR.

We then tried to design and exam a novel process of "two-step baking and development" also mainly by examining contrast curves. This technique is also the first MiBK development followed by the

second development with the salty developer, but, employing post-development baking (PDB) between the two. After the first MiBK development, we applied an extra baking for HSQ, by a higher temperature baking than the post-apply baking:

HSQ spin-coating -> PAB -> 1st solvent develop. -> PDB -> 2nd alkali develop.

Once the PDB was applied, the EDR (Eth(50%)) was reduced and improved down to 600?C/cm2 (@100kV), so that x0.3 EDR reduction was obtained.

This paper describes HSQ process development and its results particularly on newly designed and developed “two-step baking and development” with varying developers and baking conditions. Patterning results to see the HSQ resolution limit will be also reported.

Keywords: EBL, NIL, mold, HSQ, developer

8880-91, Session PTue

## EUV lithography tool focus monitoring using a 90-degree phase-shift mask

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The expected insertion point of EUV lithography in high volume manufacturing is for printing sub-50nm pitch structures. Mask side non-telecentricity coupled with relatively large aberration levels in EUV optics lead to significant telecentricity errors on wafer resulting from EUV lithography tool focus control errors. In this paper we present experimental results from a 90 degree phase shift EUV mask that is used for EUV lithography tool focus control. The mask structure was optimized to achieve the 90 degree phase shift by tuning the multi-layer stack. A variety of focus monitor structures were fabricated on the mask including segmented, phase shifted box-in-box overlay structures, phase shifted scatterometry gratings and other binary focus monitor targets. Initial results from overlay measurements of a segmented box-in-box structure with an approximately 100 nm wide absorber pattern at various defocus settings exhibited a nearly linear focus response. The observed focus sensitivity of 1 nm overlay error/100nm focus drift agrees well with the simulations. It can also be seen that reducing the width of the absorber pattern will increase the sensitivity of the technique. A second 90 degree phase shift mask design with modified focus monitoring targets is under fabrication in order to increase the focus sensitivity of the technique. In this paper, we will discuss in detail the motivation behind the need for accurate focus control in EUV lithography and propose phase shift focus monitoring as a viable technique for monitoring tool focus.

8880-92, Session PTue

## Under-layer effects for block levels: are they under control?

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Challenges in block levels due to the dilemma of cost control and under-layer effects have been addressed in several papers already, and different approaches to solve the issue have been discussed. Among the known approaches, developable BARC and under-layer aware modeling are the most promising. However, both approach has limitation/inefficiency. The efficiency of dBARC approach is limited by properties of materials. The virtual secondary exposure approach, currently used by most EDA vendor to account for under-layer effects, is fast but less and less accurate as feature dimensions getting sub-wavelength. Rigorous simulation shows that strong optical near-field interference is undermining the assumption and validity of this approach. In addition, as block levels are migrating to etched layers, we also observe under-layer dependent etch behavior that is seen in some of the block levels. All these place great challenges for block level process development.

In this paper, we will discuss possible solutions/improvements including: dBARC thickness optimization for specific block levels; rule based OPC correction; model based OPC correction using simplified empirical models. Our model approach is purely empirical and there’s no need of true optical simulation, which is difficult and slow anyway.

This work was performed at the IBM Microelectronics Div, Semiconductor Research & Development Center, Hopewell Junction, NY 12533

8880-93, Session PTue

## Evaluation results of a newly designed slim column for wide-range application of e-beam lithography

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High resolution capability of electron beam (EB) lithography becomes more important for realizing 1X nm technology node by supporting various applications relating with leading edge Si device manufacturing, e.g. EB direct writing on 300mm wafer, 4x mask and nano imprint template on 6025 blanks, research of materials (ex. resist , directed self-assembly) and other nano fabrications.

We designed novel EB slim column cell that have outer diameters of 60mm and 40mm in width that are more slim columns than that of MCC-POC systems. [1-3] We reported to the SPIE of Advanced Lithography 2013 on the results of the simulation of a novel slim column which have outer diameter of 60mm. [4-6] We estimated that the 12-88% blur at shaped beam edges through the column is enough for exposing 12nm 1:1 L&S patterns and below. The feature of the newly designed column is as follows;

(1) Small aberration.

(2) Available Character projection (CP) exposure function.

(3) Less than 60 mm in diameter of the column principal part.

Now we have been developing a single column system whose column corresponds to that slim column cell for evaluating its actual

performances. In this paper we will introduce some results of this single slim column system with CP for evaluating the matching between design and actual column performance. And we will discuss the effectiveness of slim column unit for 1Xnm technology node. And also we will show some of the examples of nano fabrications not only in Si semiconductor devices but also other nano fabrications such as photonics, MEMS and so on.

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8880-94, Session PTue

## Novel fracturing algorithm to reduce shot count for curvy shape

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The increasing complexity of RET solutions has increased the shout count of advanced photomasks. In particular, the introduction of inverse lithography (ILT) technique brings a significant increase in mask complexity and conventional fracturing algorithms generate much more shots because they are optimized for rectilinear shapes. The several methods have been proposed to reduce shot count for ILT photomasks.

Model-based approaches have been introduced these days to reduce the shot count for ILT photomasks. The model-based approach utilizes precise dose control, shot overlaps, and many other techniques. The drawbacks of model-based approach are huge computation cost and the requirement of new mask writer which supports user-level dose modulation and shot overlaps.

For the shot count reduction, we would like to introduce a new fracturing algorithm based on geometry processing, the combination of shape extraction, and direct manhattanization. This is not a model-based approach, but the benefits are: fast, applicable to current mask writers, and tunable shot reduction ratio.

This algorithm was introduced at first time in the special poster session of Photomask Japan 2013 which will not be published in the proceedings. In this paper, we will explain the details of algorithm, experiments for the shot count reduction, computing time, and data volume. We will also show some updates from Photomask Japan 2013.

8880-95, Session PTue

## Extreme-ultraviolet mask defect observation using an extreme-ultraviolet microscope

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To investigate the impact of mask defects on wafer printing during extreme ultraviolet (EUV) lithography, we have developed at-wavelength observation technique that has a potential to resolve a half-pitch (hp) 20 nm lines-and-spaces (L/S) with the image contrast of 0.5. Our previous work revealed that a prototype EUV microscope has excellent contrasts of 0.64 and 0.52 for hp 225 nm and 88 nm L/S patterns, respectively. [1, 2] In terms of the defect inspection capability, the EUV microscope could detect a 3.7-nm-high residual-type defect in hp 88 nm L/S with more than 40% of EUV light reflectivity decrease compared with reference patterns.[3]

In this study, to predict an impact of the phase defect on wafer printed image, we observed many different sizes of phase defects beneath several widths of L/S absorber pattern. Test masks prepared for this work contain the hp 88 and 64 nm L/S absorber patterns and programmed phase defects. The sizes of the phase defects were 1 and 3-nm-high bump-type and 1-nm-deep pit-type defects with several widths. The phase defects were located at several positions relative to the absorber lines. To analyze the inspection capability of the phase defect in detail, a lithography simulator was employed to calculate EUV microscope images. As a result, the EUV microscope can predict the existence of the phase defect and its impact on wafer printed image even if the EUV microscope does not emulate the image of the EUV scanner completely.

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8880-96, Session PTue

## E-beam GIDC resolution enhancement technology in practical applications

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For nearly all current or future production relevant applications of eBeam lithography (optical /EUV mask write, imprint template write or wafer direct write) the requirements are approaching or exceeding the limits of the available process technologies regarding resolution, process window, line edge roughness, and writing time. For some patterns a so called undersize-overdose treatment of the pattern, where the features are shrunk and the dose is increased respectively, will improve the pattern printing fidelity. That works fine for very sparse patterns with nearly isolated features and - to certain extend - also for patterns with regular dense structures. However, for many dense patterns or pattern parts the undersize-overdose approach increases

the overall deposited electron dose, which due to the increased backscattering diminishes or even eliminates the advantages in pattern printing fidelity.

The GIDC (Geometrical Induced Dose Correction) method combines the undersize-overdose approach with a new short range framing technique even reducing the deposited dose in dense pattern areas. Thus GIDC can be successfully applied for all applications and patterns independently of the presence of certain friendly conditions.

In this paper the achievable improvements for generic test patterns as well as for production patterns, printed on a Vistec SB352HR eBeam writer and finally etched in silicon or chrome, are demonstrated.

8880-97, Session PTue

## Advancement of fast EUV lithography modeling/simulations and applications on evaluating different repair options for EUV mask multilayer defect

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EUV lithography is the leading candidate to replace traditional DUV for high-volume manufacture (HVM) of semiconductor devices at the most advanced node. In addition to using a much shorter wave length, EUV lithography uses reflective mask consisting of 40-50 bi-layers to maximize the reflectivity. The multilayer films are never perfect---bump or pit type of defects of various sizes and shapes are abundant. The evaluation of the impact to the final wafer printing and compare different repair options to ML defect will be critical to the successful deployment of EUV lithography in HVM.

In our prior work, we already presented methods to compensate ML defect by changing absorber layer pattern, by deposit some organic materials (for pit), or by pealing of some layers (for bump). In this study, we will evaluate the impact of different repair options to process window, and demonstrate through simulation that to meet stringent production requirement, real repair should consider a combination of absorber pattern correction plus deposition and pealing.

To explore and evaluate these different possibilities to repair ML defect, we rely on simulations that we developed specifically for EUV lithography which are accurate and efficient in handling complicated geometries, computing the mask near field that include the mask 3D effect due to different polarization, and shadowing effects due to non-telecentric illumination.

We take a modular approach in our modeling of EUV lithography: we model illuminator, mask, projector and resists as separate components, and each components can be further divided into subcomponents. For EUV mask, we decompose it into absorber layer and ML layer, and take different approaches to these two layers. The output from absorber layer model becomes the input to ML layer model, whose reflected diffraction orders are feed into our absorber model again, and finally the contribution from all diffractions are assembled to form the mask near-field. The theoretical foundation of these approaches is the linearity of Maxwell equations, which allow us to decompose arbitrarily modulated waves into plane waves and vise versa.

We will compare the diffraction orders computed via our empirical approaches against results from rigorous Maxwell solver, which is built into our simulator for comparison and automatic model calibration.

After presenting our modeling approaches with rigorous solver, we present our simulation results of different ML defect repair options: absorber compensation only, deposition only (for pit defect), pealing only (for bump defect), and combination of absorber compensation with deposition or pealing. For pealing, we also present the impact of different pealing geometry: conformal removal of whole layer, uniform removal, and wedge shaped removal. Simulation demonstrated that combining absorber compensation with ML deposition or pealing will give the best process windows that are almost comparable to no ML defect case.

8880-98, Session PTue

## The optical SLM: a superior photomask

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An optical spatial light modulator (SLM) is a superior optical mask. Obviously it is more flexible with the pattern controlled in real time by a computerized data path and being able to switch from one pattern to another in a fraction of a millisecond. But the imaging quality is also more ideal due to the high demagnification, 200X vs. 5X for a fixed reticle. Polarisation and physical optics effects at the edges of features are nearly absent. The SLM can mimic all known types of phase-shifting masks: attenuated, alternating, tri-tone, and pixellated. Any number of transmission values can be mixed in the same mask image and different types of phase-shifting can be used in the same design. SLMs for EUV are feasible with sturdy micromechanical deep-etched mirrors. Finally the SLM pattern can not only be aligned electronically, but also warped to compensate for distortion in the substrate, allowing high-resolution lithography on flexible substrates.

8880-101, Session PTue

## Potential of mask production process for finer pattern fabrication

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The performance to fabricate finer pattern by mask production processes is researched, and half pitch

1Xnm patterns are fabricated on mask plate. In this research, EBM-8000 (Nuflare Technology) is used as motif writer, and CAR (Chemically Amplified Resist) is used as mask material to etch chromium hard mask. EBM-8000 has high throughput performance enough to produce photomask of current heaviest data volume, and CAR resist's sensitivity is high and it reduces writing time. So this result shows that the current mask processes have possibility to fabricate finer pattern and productivity for mass production at the same time.

Today, various lithography ways like EUV lithography, mask-less lithography and imprint lithography have been discussed for next generation patterning means. In each ways, the ability to fabricate finer pattern is expected at higher priority. That expectation is reflected to specification of mask production. In ITRS2011, minimum 22nm size SRAF pattern is required on EUV mask, and minimum 6nm image size is required on imprint template. This roadmap leads the result that the mask production will face a difficulty to fabricate finer pattern in near future. The EB mask writer has been used to produce high specification mask. EB writer is suitable tool for fabricating finer pattern because it has high resolution beam. But in producing photomask, minimum future size on mask is around 40nm, and this target is easy to achieve by current EB writer. So development of the EB mask writer has been directed for overcoming writing time issue and accuracy enhancement issue. A performance to fabricate finer pattern by EB writer have already reported, but most of them are experimental challenge. An EB writer with 100kV of acceleration voltage and Gaussian beam is often used for researching the limit of pattern resolution. But if this system is used for finer pattern mask production, it takes more than few weeks to write one mask. To get enough productivity, it is necessary to use VSB (Variable Shaped Beam) type EB writer which is used in today's mask production line.

We will present an actual performance for fabricating finer pattern by mask production processes, taking into account with productivity.

8880-102, Session PTue

## Patterning of EUVL binary etched multilayer mask

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Extreme ultraviolet lithography (EUVL) is one of the most promising next generation lithography. A mask plays a key role in lithography and should be regarded as an integral part of a lithographic system. A major requirement for EUVL mask is its high lithographic performance that addresses factors such as high image contrast, and low shadowing effect owing to reflective mask and oblique illumination. In EUVL process development, absorber type masks are commonly used, where absorber layers are placed on top of a Ru capped reflective multilayer. On the other hand, other types of EUVL mask structure has been proposed for fine pitch pattern targeting for lower shadowing effect, such as binary etched multilayer mask. 1), 2)

In this paper, we present process development of patterning binary etched multilayer mask. We introduce hard mask process on reflective multilayer blank for fine patterning and will present etched multilayer pattern of hp80nm (on mask) and potential process capability for hp40nm (on mask) and beyond.

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8880-103, Session PTue

## Modeling and correction of reactive-ion-etch contributions to mask CD nonlinearities

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As printed mask features continue to shrink, non-linearities of the exposure and pattern transfer process become a limiting factor to the total yield. Mask Process Corrections (MPC) will not only allow to remove the mask induced process signature, but more importantly decouple mask process effects from wafer process effects (both are combined into the OPC models today) and thereby provide business choices that don’t exist today.

State-of-the-art MPC models [1] are typically based on convolution kernels and are sufficient to model electron-solid interactions (electron scattering) and various tool-induced effects (shot-size dependent focus and blur effects). These turn out to be sufficient to model 1D pattern scenarios such as line linearity, 1:1 dense pitch linearity, space linearity and maybe through-pitch linearity. However, 2D pattern scenarios such as line ends, inverse line ends, hammer heads and contacts exhibit are strong CD non-linearity that cannot be explained by simple convolution kernels.

Various etch models have been suggested to better mimic the experimental artifacts, including density dependent etch rates and open area dependent etch rates [2]. However, some pattern scenarios such as inverse line ends show such a strong effect that even these extensions turn out to be insufficient. Resist development and reactive ion etching (RIE) process effects need a separate (physics based) model, taking into account the influence of the 3D resist profile on the pattern transfer during RIE (plasma and ion densities, etch selectivity), yet simple enough to be easily calibrated and applicable to full mask process corrections in reasonable time. We suggest a novel etch model that takes into account resist side wall angles and an etch behavior that depends on that.

The model has a small number of parameter, which can be calibrated using standard CD-SEM measurements on simple calibration patterns that also include 2D features. Fig. 1 and Fig. 2 show an overall calibration that is capable to reflect all 1D non-linearities within 2nm, and all 2D non-linearities within less than 6nm max error.

As the model is capable of reflecting the experimental process “finger-print”, standard shape correction using the same kernels is capable to correct for it. The computational effort for the correction algorithm is comparable to standard convolution algorithms, enabling the correction within the industrial throughput requirements. This correction technology has the potential to be combined with a new EBL contrast enhancement strategy that increases the image slope only at feature edges by overdosing, while the dose in the center of larger features is maintained to minimize the backscattered energy. The method is compatible with standard VSB writing tools, first results of this method have been recently presented for 50keV multi-beam mask writing [3].

8880-20, Session 8

## Computational mask defect review for contamination and haze inspections

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As optical lithography continues to extend into sub-0.35 k1 regime, mask defect inspection and subsequent review has become tremendously challenging, and indeed the largest component to mask manufacturing cost. The routine use of various resolution enhancement techniques (RET) have resulted in complex mask patterns, which together with the need to detect even smaller defects due to higher MEEFs, now requires an inspection engineer to use combination of inspection modes. This is achieved in 193nm AeraTM inspection platform wherein masks are not only inspected at their scanner equivalent aerial exposure conditions, but also at higher NA resolution, and special reflected-light, and single-die contamination modes, providing better coverage over all available patterns, and defect types. Once the required defects are detected, comprehensively reviewing each defect then becomes the Achilles heel of the overall mask inspection process.

Traditionally, defects are reviewed manually by an operator, which makes the process error-prone especially given the low-contrast in the resolution-limited aerial images. This also limits the quality and quantity of classifications in terms of the different types of characterization and number of defects that can practically be reviewed by a person. In some ways, such manual classification limits the capability of the inspection tool itself from being setup to detect smaller defects since it generally results in many more defects that need to be then manually reviewed.

Paper 8681-109 at SPIE AL 2013 discussed an innovative approach to actinic mask defect review using computational technology, then focusing on Die-to-Die transmitted aerial and high-resolution inspections. In this approach, every defect is characterized in two different ways, viz., quantitatively in terms of its print impact on wafer, and qualitatively in terms of its nature and origin in the mask manufacturing process. The latter characterization qualifies real defect signatures, such as pin-dots or pin-holes, extrusions or intrusions, assist-feature or dummy-fill defects, write-errors or un-repairable defects, chrome-on-shifter or missing chrome-from-shifter defects, particles, etc., and also false defect signatures, such as those due to inspection tool registration or image alignment, interlace artifacts, CCD camera artifacts, optical shimmer, focus errors, etc. Such qualitative characterization of defects has enabled better inspection tool SPC and process defect control in the mask shop.

In this paper, the same computational approach to defect review has been extended to contamination and haze defect inspections, including Die-to-Die reflected, and non Die-to-Die or single-die inspections. In addition to the computational methods used for transmitted aerial images, defects detected in die-to-die reflected light mode are analyzed based on special defect and background coloring in reflected-light, and other characteristics to determine the exact type and severity of the defect. For those detected in the non Die-to-Die mode, only defect images are available from the inspection tool. Without a reference, i.e., defect-free image, it is often difficult to determine the true nature or impact of the defect in question. Using a combination of inspection-tool modeling and image inversion techniques, Luminescent's LAIPHTM system generates an accurate reference image, and then proceeds with automated defect characterization as if the images were simply from a die-to-die inspection. The disposition of contamination and haze defects this way, filters out >90% of false and nuisance defects that otherwise would have been manually reviewed or measured on AIMSTM.

Such computational defect review, unifying defect disposition across all available inspection modes, has been imperative to ensuring no yield losses due to errors in operator defect classification on one hand, and on the other, has enhanced defect characterization and detection capability of the inspection platform itself notwithstanding the number of defects detected in the process.

Keywords: 32nm and below, Computational Review, Computational Lithography, Pattern Recovery, Inverse Lithography, Actinic Inspection, Aerial Inspection, High Resolution Inspection, Contamination inspection, D2DRf, nonD2D

8880-21, Session 8

## Evaluation of dry technology for removal of pellicle glue on advanced exposed optical photomasks

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The fast pace of MOSFET scaling is accelerating the introduction of smaller technology nodes to extend CMOS beyond 20nm as required by Moore's law. CMOS scaling beyond 20nm faces many difficult challenges in many areas including the availability of defect free photomasks. Defect free mask availability has been regarded as one of the top priorities for high volume manufacturing (HVM) due to yield losses caused by surface defects. Therefore, in order to meet stringent CD, Overlay and Defect requirements for sub-20nm technology nodes, especially with different absorber materials, mask suppliers are focused on developing new cleaning technologies to deliver defect free photomasks. Critical photomasks are also restricted for use on certain scanners, and qualification of multiple mask sets for high volume manufacturing makes the challenge even greater to match overall performance. This is leaving a gap in maintaining these photomasks in a fab environment, for not only haze control but also basic functionality. The industry standard of using wet cleaning techniques (which uses aggressive chemicals, like SPM, and SC1) to re-pel photomasks in the fab can result in damage to fragile features (like.g. - scatter bars), CD changes due to material erosion, and the potential for creating defects that require other means of removal. Also, these wet cleaning methods in the fab environment can create haze. Haze can be controlled and managed by: 1. Chemical free (dry) cleaning, 2. Inline fab inspection, and 3. Managing the environment where photomasks are stored.

In this paper we will discuss a dry technique (chemical free) to remove pellicle glue from an advanced exposed optical photomask. Samsung Austin Semiconductors (SAS), jointly worked with Eco-Snow Systems (a subsidiary of RAVE N.P., Inc) to evaluate the use of a Dry Reactive Gas (DRG) technique to remove pellicle glue on an exposed photomask, and its potential impact on haze growth. This technique will significantly reduce the impact to the critical geometry in active arrays within the photomask patterns, resulting in preserving the patterning performance level required at the wafer level

The paper will discuss results and viability of this technique as used on advanced photomasks.

8880-22, Session 8

## Inline detection of Chrome degradation on binary 193nm photomasks

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193nm binary photomasks are still used in the semiconductor industry for the lithography of some critical layers for the nodes 90nm and 65nm, with high volumes and over long period. However, these 193nm binary masks can be impacted by a phenomenon of chrome oxidization [1], [2], [3, [4], leading to critical dimensions uniformity (CDU) degradation with a pronounced radial signature. If not detected early enough, this CDU degradation may cause defectivity issues and lower yield on wafers. Fortunately, a standard cleaning and repel service at the maskshop has been demonstrated as efficient to remove the grown materials and get the mask CD back on target [2],[4].Some detection methods have been already described in literature, such as wafer CD intrafield monitoring (ACLV)[2], giving reliable results but also consuming additional SEM time with less precision than direct reticle measurement.

In this paper, we propose another approach, by monitoring the CDU directly on the photomask, concurrently with defect inspection for regular requalification to production for waferfabs. For this study, we focused on a Metal layer in a 90nm technology node. Wafers have been exposed with production conditions and then measured by SEM-CD. Afterwards, this mask has been measured with a SEM-CD in maskshop and also inspected on a KLA Tencor X5.2 inspection system, with pixels 125 and 90nm, to evaluate the iCDU option [5].

iCDU was firstly developed to provide feed-forward CDU maps for scanners intrafield corrections, from arrayed dense structures on memory masks. Due to layout complexity and differing feature types, CDU monitoring on logic masks used to pose unique challenges. The selection of suitable feature types for CDU monitoring on logic masks is no longer an issue, since the transmitted intensity map gives all the needed information, as shown in this paper.

In this study, the mask was heavily degraded after more than 18,000 300mm wafers exposed and the cleaning brought it back almost to its original state after manufacture. Wafer CD, mask CD and iCDU results can be compared, before and after a standard maskshop cleaning. Measurement points have be chosen in logic areas and SRAM areas, so that their respective behaviours can be studied separately. Transmitted maps before and after cleaning were analysed in terms of CD shift and CDU degradation. The delta map shows a nice correlation with mask CD shift. iCDU demonstrated the capability to detect a reliable CD range degradation of 5nm on reticle by a comparison between a reference inspection and the current inspection. Die to die inspection mode provides also valuable data, highlighting the degraded chrome sidewalls, more in the mask centre than on the edges.

Ultimately, these results would enable to trigger the preventive cleanings rather than on predefined thresholds. The expected gains for waferfabs are cost savings (adapted cleanings frequency), increased reticle availability for production, longer reticle lifetime, no additional SEM time neither for mask nor on wafer.

8880-23, Session 9

## Comparison of CD measurements of an EUV photomask by EUV scatterometry and CD-AFM

Frank Scholze, Victor Soltwisch, Gaoliang Dai, Mark-Alexander Henn, Hermann A. Gross, Physikalisch-Technische Bundesanstalt (Germany)

We present a comparison of line shape parameters like CD and side wall angle measured on EUV photomask test structures. The structures investigated are dense and semi-dense bright and dark lines with different nominal CDs between 200 nm and 140 nm. The results show excellent linearity of the scatterometry and AFM CD values within a range of only about 1 nm and an offset of the absolute values below 3 nm.

Scatterometry is a common technique for characterizing nano-structured surfaces. Our goal is to establish scatterometry as a traceable and absolute metrological method for dimensional measurements. The properties of the object are derived from an optimization which minimizes the difference between the measured and calculated intensities. Here, a maximum likelihood estimation (MLE) method is used to reconstruct geometry profile parameters and to estimate their uncertainties from the measured scattering efficiencies. The impact of line roughness on the reconstruction results is included in the model. We performed goniometric scatterometry using monochromatized radiation having three different wavelengths in the EUV spectral range around 13.5 nm with a fixed incidence angle of 6°, which resembles the working conditions in a current EUVL-tool, using the EUV reflectometer at PTB's EUV radiometry beamline at BESSY II. CD and side wall angle were evaluated.

A Critical Dimension Atomic Force Microscope (CD-AFM) which allows direct, accurate and non-destructive measurements of nanostructures with high resolution was set up at PTB. It facilitates versatile measurements of e.g., height, CD, sidewall angle, line edge/width roughness, corner rounding, and pitch. It applies flared tips to probe steep and even undercut sidewalls and employs a new Vector-Approaching-Probing strategy which enables very low tip wear and high measurement flexibility. Its traceability is ensured by a set of calibrated step-height and lateral standards. The effective tip geometry was characterized by CD reference materials calibrated by transmission electron microscopy. Measurements were performed at 5 selected spots for each feature pattern of the mask using a "CDR-70s"-type tip (70 nm nominal width). Measurement stability and tip wear were checked during the whole measurement series, and shown to be better than 0.1 nm. The apparent middle CD was evaluated at half feature height and was corrected by the characterized effective tip geometry to obtain the specimen CD. The sidewall angle was determined from the centre part of the sidewall profile between 0.375 and 0.625 relative feature height. Feature height and line edge roughness were also measured.

The comparison of the scatterometry and AFM CD values yields a linear relation within a spread of only about 1 nm and an offset of the absolute values below 3 nm. For the side wall angle, both methods yield consistent results within a range of about 2°. This variation corresponds to real variations of the side wall angle as measured by the AFM. We will discuss ways to further improve the measurement capabilities.

The test mask was provided by the Advanced Mask Technology Center (AMTC) Dresden, a joint venture of GlobalFoundries and Toppan Photomask.

8880-24, Session 9

## Two-dimensional mask effects at the 14nm logic node

Amy E. Zweber, Anne E. McGuire, Chester Huang, Katherine Ballman, Mike S. Hibbs, Steven C. Nash, IBM Corp. (United States); Takeshi Isogawa, Yoshiyuki Negishi, Tasuku Senna, Toppan Photomasks, Inc. (United States); Tom B. Faure, Emily E. Gallagher, Jed H. Rankin, Daniel J. Dechene, Lin Hu, Mohamed Talbi, IBM Corp. (United States); Samit Barai, IBM India Private Ltd. (India); Yongan Xu, IBM Corp. (United States)

At the 14 nm logic node, significant lithographic changes relative to previous technologies are needed to resolve tight contact-level pitch requirements. At this node, both source-mask optimization and bright field attenuated phase shift masks (attnPSM) were deployed.1 Adapting to these new requirements is essential for mask makers to deliver the necessary 14 nm on-wafer lithographic results. Bright field masks return focus to negative tone resist materials to reduce write time and improve opaque main feature fidelity.2 AttnPSM processing requires thicker mask resist films than binary OMOG masks, which increases feature aspect ratios and challenges the resolution performance. Additionally, extending the application of 193 immersion lithography for further generations requires not only continued reduction of traditional sources of variation but investigation into and quantifying the impact of completely new ones. The complex patterning schemes being used now require additional scrutiny on mask two-dimensional (2D) controls. To enable accurate model accounting, one dimensional characterization of the mask is no longer sufficient; two-dimensional (2D) data is required to complete a mask model with an acceptable wafer response.1 This paper characterizes and assesses the importance of 2D mask effects on both attnPSM and OMOG masks. A methodology for characterizing corner rounding and line end shortening is presented. Optical mask 2D measurements as well as wafer simulation and wafer print results are summarized.

1 Hamieh, B., Choi, H. C., Erenturk, B., Guo, W., Hamouda A., Liu, H., McIntyre, G., Meiring, J., Moreau, D., Thomas, A., and Wei, A., "Enabling reverse tone imaging for via levels using attenuated phase shift mask and source optimization," Proc. SPIE 8683-19 (2013).

2 Zweber, A. E., Faure, T, McGuire, A., Sundberg, L. K., Sooriyakumaran, R., Sanchez, M. I., Bozano, L. D., Senna, T., Fujita, Y., Negishi, Y., Tanabe, M., Kaneko, T., "Study and comparison of negative tone resists for fabrication of bright field masks for 14 nm node," Proc. SPIE 8522-27 (2012).

8880-25, Session 9

## Measurement of EUV absorber and resist CD using spectroscopic ellipsometer

Kyung M. Lee, Malahat A. Tavassoli, Pei-Yang Yan, Intel Corp. (United States); Guojing Zhang, Intel Corp (United States)

Oblique-incidence spectroscopic ellipsometer, operating at conventional illumination wavelength (w/o the need of special low-wavelength range) was successfully used in order to measure the CD and height of Absorber structure on EUV plates, and its applicability down to <10nm pitch (1x) structure was investigated via simulations. EUV FCCD & DCCD experimental data from ellipsometry, SEM, and AFM are presented to compare precision and merit of each method.

8880-26, Session 10

## 2013 EMLC Best Paper: Experimental approach to EUV imaging enhancement by mask absorber height optimization *(Invited Paper)*

Natalia V. Davydova, Robert C. de Kruif, ASML Netherlands B.V. (Netherlands); Haiko Rolff, Advanced Mask Technology Ctr. GmbH Co. KG (Germany); Brid Connolly, Toppan Photomasks, Inc. (Germany); Eelco van Setten, Ad Lammers, Dorothe Oorschot, ASML Netherlands B.V. (Netherlands); Norihito Fukugami, Yutaka Kodera, Toppan Printing Co., Ltd. (Japan)

No Abstract Available

8880-27, Session 11

## Reflecting on inspectability and wafer printability of multiple EUV mask absorbers

Kazunori Seki, Toppan Photomasks, Inc. (United States); Karen D. Badger, Emily E. Gallagher, Gregory R. McIntyre, IBM Corp. (United States); Toshio Konishi, Toppan Photomasks, Inc. (United States); Yutaka Kodera, Satoshi Takahashi, Toppan Printing Co., Ltd. (Japan); Vincent A. Redding, KLA-Tencor Corp. (United States)

EUV is the strongest candidate for the next generation lithography. The EUV blank materials are different from the ones used on conventional optical blanks. The structure itself is more complicated than conventional optical masks since the mask is reflective and 40 bilayers of Mo/Si capped with a Ru layer create the Bragg mirror surface. The absorber materials are also newly-introduced and various types of EUV absorber stacks are evaluated in this paper. The absorber modifies image contrast and influences both the mask inspectability and the ultimate wafer resist results. To study the effect, masks were fabricated from four different film stacks on which the thickness of the low reflective and absorber layers vary. All blanks had the same Ru-capped multilayer substrate beneath the absorber stack, and the same CrN backside. Inspection contrast, defect sensitivity and inspectability were measured on a 193nm wavelength inspection tool. The focus of this paper is on mask inspection at the 193nm wavelength; however, wafer results at the 13.5 nm EUV exposure wavelength will be included to anchor the relevance of the mask inspection results.

8880-28, Session 11

## The SEMATECH high-NA actinic reticle review project (SHARP) EUV mask-imaging microscope

Kenneth A. Goldberg, Iacopo Mochi, Markus P. Benk, Arnaud P. Allezy, Michael R. Dickinson, Carl W. Cork, James B. Macdougall, Patrick P. Naulleau, Senajith B. Rekawa, Lawrence Berkeley National Lab. (United States)

We have recently commissioned the first of a new generation of high-resolution extreme ultraviolet (EUV) microscopes dedicated to current and future generations of EUV photolithography research. To achieve its high imaging resolution, coherence control, and the ability to flexibly emulate a variety of current and future EUV printing tools, the SEMATECH High-NA Actinic Reticle review Project (SHARP), features several first-of-their-kind design elements in an all-new, synchrotron-based microscope platform. SHARP is designed to produce various illumination partial coherence conditions and discrete, rotating azimuthal planes of incidence, while offering a range of illumination central ray angles (6-10°), 4x numerical apertures (NA) values from 0.25-0.625, and tunable illumination wavelength.

During its eight years of operation, SHARP's predecessor, the SEMATECH Berkeley Actinic Inspection Tool (AIT) demonstrated the essential need for high-quality EUV-wavelength imaging for mask research. Owing to the wavelength-specific reflective properties of EUV reticles, imaging with EUV light is the only faithful way to understand the physical response of defects, repairs, and pattern optical proximity corrections. For several reasons, the differences between EUV and non-EUV measurement technologies are likely to increase in future nodes.

Operating since January 2013, SHARP's performance has already exceeded that of its predecessor: the most significant way may be flux. Imaging comparison tests show that SHARP delivers nearly 150 times higher photon flux than AIT. Imaging tests with lens NA values up to 0.50 (4x) revealed that proper assessment of the imaging resolution is currently limited by the unavailability of sample masks with sub-50-nm hp features.

In SHARP, a novel, three-mirror, Fourier-synthesis illuminator converts the synchrotron's low-divergence input beam into a programmable range of incidence angles, from 1-19°, focused onto the mask. The ~1-kHz angle-scanning is powered by a 1-mm-diameter, multilayer-coated MEMS mirror that scans pupil-fill patterns during exposure. SHARP's condenser is an ellipsoidal mirror with 10x demagnification, designed to concentrate the beam onto a 5-100-µm mask region. The ellipsoidal mirror can be programmed to scan through small (500 µrad), angular range, to increase the illumination uniformity and area. SHARP's high-resolution imaging system relies on Fresnel zoneplate lenses, which serve as diffraction limited, small-field objectives, patterned using electron-beam lithography into an array of various NA values, angles of incidence, magnifications, and azimuthal angles (for emulation of lithography-tool imaging across a ring field). SHARP is also equipped with an in-situ visible-light microscope to simplify mask navigation, and a pair of photodiodes to compare the incident and reflected EUV power.

We report the results of in-progress calibration, optimization, and performance testing, including imaging resolution, aberration characterization, illumination coherence-control and uniformity, among other performance metrics. We will also discuss SHARP's mechanical design, which uses a vibration-isolated internal platform and a shared rigid frame that connects the independent mask and zoneplate stages for nm-scale stability during exposures. Specified for relevance down to 8-nm CD and beyond, we anticipate that SHARP will serve the development of EUV lithography for years to come.

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8880-30, Session 11

## EUV patterned mask inspection system using projection electron microscope technique

Hidehiro Watanabe, Ryoichi Hirano, Susumu Iida, Tsuyoshi Amano, Tsuneo Terasawa, EUVL Infrastructure Development Ctr., Inc. (Japan); Masahiro Hatakeyama, Takeshi Murakami, Shoji Yoshikawa, Kenji Terao, EBARA Corp. (Japan)

Patterned mask inspection system using the projection electron microscope (PEM) technique is explored. The capability of the defect detection required in EUV mask for half pitch (hp) 16 nm node high volume manufacturing was verified.

The sensitivity capturing less than 18 nm sized defect is required for EUV mask pattern inspection system for hp 16 nm node devices

according to the updated ITRS2012. The patterned mask inspection using electron beam probe is a candidate for 1X nm EUV mask inspection. Especially the PEM technique is recognized as an inspection technique having the advantages of high throughput as DUV inspection and of fine resolution as SEM inspection.

EIDEC is developing a novel pattern inspection system using PEM technique with EBARA CORPORATION. The electron beam for high illumination intensity is generated by an electron gun, and is then deflected by a beam separator to illuminate the surface of an EUV mask. The mask image by scattered electrons focuses on a Time Delay Integration (TDI) image sensor through the projection optics. The illuminating area is wide enough to cover the sensor area, which relaxes the limitation in resolution brought about by space charge effect, a serious issue in SEM system.

We already reported the experimental results of the image resolution and the transmittance of electron optics superior to expected designed values. In this paper, we describe the capability of defect detection using experimental results of EUV mask pattern inspection by this system. The high resolved electron image by the developing PEM optics with sophisticated image processing technique, enhancing the defect image on electron noise inherent to electron microscope, enables to detect less than 18 nm sized defects in hp 64 nm mask patterns for hp 16 nm node LSI devices. The analysis of synthesized PEM images using computer simulation of electron trajectory supports the result.

This study is supported by New Energy and Industrial Technology Development Organization (NEDO) and Ministry of Economy, Trade and Industry (METI).

8880-31, Session 12

## Defects on high-resolution negative-tone resist: “The revenge of the blobs” *(Invited Paper)*

Martha I. Sanchez, Linda K. Sundberg, Luisa D. Bozano, Ratnam Sooriyakumaran, Daniel P. Sanders, IBM Almaden Research Ctr. (United States); Tasuku Senna, Toppan Photomasks, Inc. (United States); Masahito Tanabe, Toru Komizo, Itaru Yoshida, Toppan Printing Co., Ltd. (Japan); Amy E. Zweber, IBM Corp. (United States)

Resist materials rely on solubility differences between the exposed and unexposed areas to create the desired image. For positive-tone chemically amplified resists, image contrast is accomplished by deprotecting the exposed area causing it to become more polar, and therefore, more soluble in aqueous alkaline developer. Most negative-tone resists achieve the solubility difference by cross-linking the exposed area causing it to be insoluble in developer. We have developed a new high resolution, high sensitivity negative-tone resist that relies on dissolution switching, similar to a positive-tone mechanism, but where the exposed area is insoluble in aqueous developer resulting in a negative-tone image. During mask evaluation for 14nm optical technology applications of the new resist type, 1 – 5 um size defects were found in large numbers under certain exposure conditions. This paper will describe the process and tests used to uncover the cause and the source of the defects we affectionately refer to as “blobs” and what we can do to eliminate them.

8880-32, Session 12

## Controlling the sidewall angle of advanced attenuated phase-shift photomasks for 14nm and 10nm lithography

Richard E. Wistrom, IBM Corp. (United States); Yoshifumi Sakamoto, Toppan Photomasks, Inc. (United States); Thomas B. Faure, Jeffery Panton, IBM Corp. (United States); Takeshi Isogawa, Toppan Photomasks, Inc. (United States); Anne E. McGuire, IBM Corp. (United States)

As optical lithography is extended to the 14nm and 10nm technology nodes, sidewall angle (SWA) control of photomask features becomes increasingly important. Mask SWA affects the lithographic process variation (PV) band and influences properties such as resolution and exposure latitude on wafer. The experiments to be reported here study SWA for advanced attenuated phase-shift photomasks. SWA is evaluated from three perspectives. First, the effects of local mask environment, such as etch loading and linewidth, will be tested. Second, a variety of SWA measurement methods, such as SEM cross section, 3-D SEM, and AFM, will be compared. Third, the effects of mask etch process parameters such as bias power, pressure, and etch chemistry will be studied. In addition, statistical experimental design and analysis methods will be employed to quantify the effects of MoSi etch process parameters on other mask properties such as critical dimension, linearity, and thru-pitch.

8880-33, Session 12

## Model-based etch profile simulation of advanced PSM films

Michael Grimbergen, Madhavi R. Chandrachood, Jeffrey X. Tran, Toi-Yue B. Leung, Keven Yu, Amitabh Sabharwal, Ajay Kumar, Applied Materials, Inc. (United States)

For advanced binary and PSM mask etch, final profile control is critically important for achieving desired mask specifications. As an aid to attain profile control, an etch profile simulation method has been developed. The method starts with an initial photoresist profile and incorporates etch rate and directionality information to predict the final etch profile. In this presentation, simulation results will be compared to measured etch profiles for advanced PSM substrates. The results will highlight the importance and implications of incoming resist profile and etch selectivity on final profile.

8880-34, Session 12

## Implementable and systematic mitigation of EUV phase defects

Wen Chang Hsueh, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

Phase defects in mask blanks is one of the key issues in extreme ultraviolet lithogra-phy (EUVL). If defect-free mask blanks is the only solution, it will result in very high cost and low yield of EUV masks. In this paper, we present a novel method for fabri-cating defect-free-like EUV masks by implementing several novel techniques such as smart chip-assignment, fine metrology-orientation and precise e-beam sec-ond-alignment from blank preparation to e-beam exposure. The mitigation success rate versus mask pattern density is simulated and verified by lithographic results using mitigated masks. The maximum counts of < 100-nm sized defects associated with a variety of pattern densities is shown in Table 1 below. Our methodology provides a way to achieve defect-free-like EUV mask blanks.

8880-35, Session 13

## Studying the effects of modified surface chemistry on chrome migration in binary photomasks

Christopher Kossow, Peter S. Kirlin, Michael J. Green, Photronics, Inc. (United States)

Migration of the Cr/CrxOy film in binary photomasks during use in 193nm photolithography has been observed for some time in the semiconductor industry. This phenomenon leads to a shift in the reticle critical dimensions (CDs) that worsen with increased exposure eventually resulting in wafer yield loss. This paper studies the impact of varying annealing conditions on the CrxOy species on the surface of the mask. Further, we examined the effect of a surface condition with maximized Cr2O3 content on the 193nm-induced chrome migration phenomenon. Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), and X-Ray Photoelectron Spectroscopy (XPS) were used to characterize the composition of the Cr/CrxOy film. A 193nm accelerated exposure test bench was used to induce film migration in samples of varying surface chemistry.

8880-36, Session 13

## Investigation of EUVL reticle capping layer peeling under wet cleaning

SherJang Singh, Uwe Dietze, SUSS MicroTec Inc. (United States); Arun J. Kadaksham, Mason Jang, Frank Goodwin, SEMATECH Inc. (United States)

In the absence of pellicle a EUVL reticle is expected to withstand up to 100x cleaning cycles. EUVL reticle constitutes a complex multi-layer structure with extremely sensitive materials which are prone to damage during cleaning. The 2.5 nm thick Ru capping layer exhibits multiple modes of failure under wet cleaning process. In this study we have investigated the Ru peeling effect caused by thermal radiation from In-situ UV process. Ru peeling damage from radiation is correlated to the state of Ruthenium and underlying multilayer. We demonstrate that by adjusting the radiation parameters and by optimizing the cleaning process, it is possible to delay or prevent the onset of Ruthenium peeling. Different steps of the cleaning process are also individually analyzed for possible thermal effects on the capping layer and corrective actions are therefore presented.

8880-37, Session 13

## Causes and mitigation of large killer defects in ultralow defect extreme UV mask blanks

Adrian Devasahayam, Alan Hayes, Boris Druz, Viktor Kanarov, Timothy L. Pratt, Alfred Weaver, Veeco Ion Beam Equipment Inc. (United States); Patrick A. Kearney, SEMATECH Inc. (United States); Alin O. Antohe, SEMATECH Inc. (United States) and Veeco Ion Beam Equipment Inc. (United States); Frank Goodwin, SEMATECH Inc. (United States)

Availability of a high volume supply of low defect density (LDD) reflective mask blanks is one of the critical technology gaps for commercialization of Extreme Ultraviolet Lithography. Ion Beam Deposition (IBD) systems are used in the mask blank fabrication process to deposit EUV reflective multilayers of silicon and molybdenum on polished LTEM (Low Thermal Expansion Material) substrates. For high volume manufacturing (HVM), much lower mask defect densities and better production control is required. Recently, root cause analysis of the sources of defects based on new experimental data [1], and a comprehensive strategy for defect mitigation [2], has been presented. It is concluded that a next generation IBD tool design reconfigured according to the new findings is needed. Meanwhile, the systems currently in production can and must be further improved. Present mask yield is limited by large “killer” defects, which analysis indicates originate from chamber shield surfaces bombarded by stray energetic ion and neutral atom fluxes from the ion beam [1]. Such fluxes are generated by gas scattering, beam divergence, and neutralized ions reflected from the sputtering target. In this paper, we will focus on the causes of the killer defects and correlation to the “beam overspray” fluxes. We will then describe our plans and the status of our efforts to reduce them in the existing IBD systems by ion source and other modifications. Learning from these efforts can also be used to accelerate the development of the next generation tool.

[1] V. Jindal, P. Kearney, J. Sohn, et al, “Ion beam deposition system for depositing low defect density extreme ultraviolet mask blanks, Proceedings SPIE, Vol. 8322, 83221W-1 (2012).

[2] A.V. Hayes, B. Druz, V.Kanarov, et al, “Fabrication of Ultralow Defect Extreme UV Mask Blanks: Limits to Current Deposition Technology and Strategies for a Next Generation Tool Design,” Paper to be presented at the 20th International Symposium on Photomask and NGL Mask Technology, Pacifico Yokohama, April 16-18, 2013.

8880-38, Session 14

## 1D design style implications for mask making and CEBL

Michael C. Smayling, Tela Innovations, Inc. (United States)

At advanced nodes, CMOS logic is being designed in a highly regular design style because of the resolution limitations of optical lithography equipment. Logic and memory layouts using 1D Gridded Design Rules (GDR) have been demonstrated to nodes beyond 12nm. Smaller nodes will require the same regular layout style but with multiple patterning for critical layers.

One of the significant advantages of 1D GDR is the ease of splitting layouts into lines and cuts. A line & cut approach has been used to achieve good pattern fidelity and process margin to below 12nm. Line scaling with excellent line-edge roughness (LER) has been demonstrated with self-aligned spacer processing.

This change in design style has important implications for mask making:

- The complexity of the masks will be greatly reduced from what would be required for 2D designs with very complex OPC or inverse lithography corrections.
- The number of masks will initially increase, as for conventional multiple patterning, but there are future options for mask count reduction.
- The line masks will remain simple, with little or no OPC, at pitches (1x) above 80nm. This provides an excellent opportunity for continual improvement of line CD and LER. The line pattern will be processed through a self-aligned pitch division sequence to achieve pitch division by 2 or pitch division by 4.
- The cut masks can be done with “simple OPC” as demonstrated to beyond 12nm. Multiple simple cut masks may be required at advanced nodes. “Coloring” has been demonstrated to below 12nm for two colors and to 8nm for three colors.
- Cut/hole masks will eventually be replaced by e-beam direct write using complementary e-beam lithography (CEBL). This transition is gated by the availability of multiple column e-beam systems with throughput adequate for high-volume manufacturing.

A brief description of 1D and 2D design styles will be presented, followed by examples of 1D layouts. Mask complexity for 1D layouts patterned directly will be compared to mask complexity for lines and cuts at nodes larger than 20nm. No such comparison is possible below

20nm since no single patterning approach works below ~80nm pitch using optical exposure tools.

Wafer results for line patterns with pitch division by-2 and by-4 will be presented at sub 12nm nodes. Examples of post-etch results will be presented for 1D patterns done with cut masks and compared to cuts exposed by a single-column e-beam direct write system.

8880-39, Session 14

## Charting CEBL's role in mainstream semiconductor lithography

David K. Lam, Multibeam Corp. (United States)

E-Beam direct writing (EBDW) requires no masks and affords high resolution. However, its historically slow writing speed has kept it out of high volume manufacturing (HVM). Thanks to continuing EBDW advances combined with the industry's move to the unidirectional (1D) gridded layout style, EBDW promises to cost-efficiently complement 193nm ArF immersion (193i) optical lithography in HVM.

Patterning conventional 2D random design layout with 193i lithography is a major roadblock to scaling and manufacturing advanced devices. To overcome the challenge, IC designers have increasingly adopted 1D layout with "lines and cuts" in critical layers since 2007. Leading logic and memory chipmakers have been making advanced devices with lines-and-cuts in HVM for several generations.

Patterning lines and cuts has become printing and cutting gratings. However, while 193i is excellent for printing grating, cutting these lines is a different matter. As nodes advance, optical cutting requires complex OPC, multiple patterning, and expensive cut masks. All this raises manufacturing cost – even for HVM.

The use of advanced EBDW for patterning line-cuts, working with 193i that prints the lines, was first envisioned by Intel lithography guru Yan Borodovsky in 2010 when he coined the term: "Complementary Lithography". Such complementary use of EBDW is known as Complementary E-Beam Lithography, or CEBL.

This paper will chart how CEBL can work hand-in-hand with 193i in fabricating advanced 1D-layout devices, recognizing the support infrastructure required for CEBL. The following topics will be reviewed:

• Why conventional EBDW with parallel pixel writing of 2D patterns won't work

• Why generic all-purpose EBDW systems are not well suited to perform cutting in HVM

• Where CEBL can play a key role in mainstream HVM semiconductor lithography

• How a multiple miniature-column design/architecture offers a highly cost-efficient approach to CEBL

8880-40, Session 14

## Impact of proximity model inaccuracy on patterning in electron-beam lithography

Shy-Jay Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

Electron beam lithography is a promising technology for next generation lithography. Compared to optical lithography, it has better pattern fidelity and larger process window. However, the proximity effect caused by the electron forward scattering and backscattering in the resist and the underlaying substrate materials has a severe influence on the pattern fidelity when the required critical dimensions (CD) are comparable to the electron beam blur size. Therefore, an accurate electron scattering model and a proper proximity correction play a vital role in electron beam lithography. In this paper, we describe the model accuracy of electron scattering in terms of multiple Gaussian kernels with in-house proximity error correction to reduce proximity error with much better accuracy and more self-consistency than the double Gaussian kernel on both the 5-kV and the 100-kV electron energies. The impact of various Gaussian kernels used in the proximity correction on the lineation of typical patterns is also addressed.

8880-41, Session 15

## 2013 Photomask Japan Panel Discussion Summary: Future mask patterning technologies in the next decade: searching for the best mix solution *(Invited Paper)*

Noriaki Nakayamada, NuFlare Technology, Inc. (Japan); Ichiro Kagami, Sony Semiconductor Kyushu Co., Ltd. (Japan)

This paper will give a review and summary of the key messages from the 2013 PMJ panel discussion topic : "Future mask patterning technologies in the next decade: searching for the best mix solution." The results of the special survey conducted for the panel will be reviewed along with a brief summary of each panelist's point of view.

The panel was motivated by the Best Paper Award Winner of BACUS 2012 "Future Mask Writers Requirements for the Sub 10nm Node Era" by M. Chandramouli, N. Wilcox, A. Sowers. D. Cole, and F. Abboud of Intel Corporation. The panel consisted of representatives from mask shops, mask writer manufacturers, EDA, and an industry expert on optical multi-beam technologies. The discussions were centered on the roadmap for writers as there is a need for a smooth transition from variable shaped beam (VSB) to multi-beam technologies. Other requirements such as the need for 0.01-0.05nm addressability as expressed by the survey results, and the issues surrounding Mask Data Preparation with the Writer were discussed by the panel.

Panel Moderators: Noriaki Nakayamada, NuFlare Technology, Inc. (Japan), Ichiro Kagami, Sony Semiconductor Co. (Japan)

Panelists:

Inkyun Shin, Samsung Electronics, Co., Ltd (Korea)

Chris Progler, Photronics, Inc., (USA)

Aki Fujimura, D2S, Inc. (USA)

Hans Loeschner, IMS Nanofabrication AG (Austria)

Hiroshi Matsumoto, NuFlare Technology, Inc. (Japan)

Tor Sandstrom, Micronic Mydata AB (Sweden)

8880-42, Session 16

## Mask automation: need a revolution in mask makers and equipment industry

Seong-yong Moon, Sangyong Yu, Young-Hwa Noh, Hyun-Joo Lee, Han-Ku Cho, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

As improving device integration for the next generation, high performance and cost down are also required accordingly in semiconductor business. Recently, significant efforts have been given on putting extreme ultraviolet (EUV) technology into fabrication in order to improve device integration. At the same time, 450mm wafer manufacturing environment has been considered seriously in many ways in order to boost up the productivity. Accordingly, 9-inch mask has been discussed in mask fabrication business recently to support 450mm wafer manufacturing environment successfully. Although introducing 9-inch mask can be crucial for mask industry, multi-beam technology is also expected as another influential turning point to overcome currently the most critical issue in mask industry, electron beam writing time. No matter whether 9-inch mask or multi-beam technology will be employed or not, mask quality and productivity will be the key factors to survive from the device competition.

In spite of significant efforts on manufacturing automation in mask industry, it is still far from the automation level in wafer industry. Now, mask facility automation is inevitable rather than considered as an option in order to control many parameters and specifications which are required more than the wafer industry does for higher mask manufacturing yield. With advanced mask facility automation not only optical mask but also EUV mask or 9-inch mask industry can be expected to grow up.

Recently SEMI Equipment Communications Standard II (SECS-II) protocol has been used for semiconductor manufacturing equipment. SECS-II enables the massage transmission between the equipment and host. It is an open frame communication protocol supporting real-time data acquisition and analysis with system parameters.

8880-44, Session 16

## DSA template mask determination and cut redistribution for advanced 1D gridded design

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With the feature sizes keep shrinking in the modern IC manufacturing, conventional 193nm ArF immersion optical lithography (193i) is reaching its limit and new generation of lithography device is still lagging behind. As a result, the industry has been transiting from the random 2D designs to highly regular 1D gridded designs for sub-20nm nodes and making the circuit with print-cut technology.

In this process, randomly distributed cuts are the major challenge, which may be too dense to be printed by single patterning lithography, and multiple patterning techniques or complementary lithography techniques are required for cut fabrication. Recently, the technology of block copolymer directed self-assembly (DSA) has shown its advantage in contact hole patterning. This technology can be further expanded by reversing the tune to be used in cut printing and reduce the manufacture cost. However, the features must be patterned under the guidance of specified DSA templates, and the types of feasible templates are rather limited. To organize the cuts in a 1D layout to form a valid DSA template mask, the cuts must be shifted such that the real wires are extended, while the dummy wires are shortened. In this way, the functionality of the circuits will remain, and the impact on performance will be limited.

To redistribute the cuts to generate a valid DSA template mask, we propose a graph-theoretic algorithm to shift the original cuts according to a given set of valid DSA templates and minimize the overall cut movements to limit the performance impact. This algorithm consists of two stages. In the first stage, we build a conflict graph to include a vertex for each cut in the graph. For each pair of cuts, add an edge between them if they violate DSA design rule. The weight of the edge is defined by the movement amount of the two cuts to resolve the conflict. In the second stage, we resolve the conflicts by template matching. For each connected components in the graph, we try to move the cuts to match a template with largest number of cuts. If there is no matching pattern, we bipartition the graph and perform template matching. This process continues recursively until a template is matched. Note that in the worst case, the component will be partitioned into a set of single vertices, which indicates there is no feasible cut redistribution.

This proposed algorithm is expected to construct the graph linearly to the number of cuts, thus to provide an efficient scheme for layout modification and DSA template mask determination to meet constraints from DSA process as well as the performance change on the original layout.

8880-45, Session 16

## Finishing of EUV photomask substrates by CNC precessed bonnet polisher

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The specification for “extreme ultraviolet lithography mask substrates” states that Peak-to-Valley flatness error should range between 30 nm to 100 nm over the quality area (that is, up-to 5 mm away from the substrate edges). Such low flatness error is difficult to achieve on square shaped substrates, especially with the conventional chemical / mechanical polishing equipment (CMP) typically used in industry. An innovative sub-aperture CNC polishing process is presented in this paper, which answers the need for corrective post-finishing after conventional polishing by CMP equipment.

The CNC process is based on soft bonnet tool precession, and can be summarized as follows: the position and orientation (precession angle) of a spinning, inflated, membrane-tool are actively controlled as it traverses the surface of a workpiece. The workpiece may have any general shape, including concave, flat, or convex, aspheric or free-form. While a classical polishing tool is pressurized against the surface of the part, with no attempt to control actively the Z position of the tool in a local or global coordinate frame, in the technique we describe the Z position, precession, as well as the contact-force, are actively controlled with a CNC machine tool. This process may be used with any combination of cloth and abrasives, depending on the substrate material, in order to generate a sub-aperture spot that traverses the workpiece with controllable feed rates.

The precessed bonnet polishing technique has now been applied to corrective finishing of EUV photomasks (after conventional polishing by CMP equipment). The experiments carried out so far have dealt with characterization of the achievable flatness error and surface roughness, as a function of overall process time.

Potential surface roughness performance was determined by full-factorial characterization of three of the available CNC process parameters: (1) bonnet air pressure, (2) bonnet precession angle, and (3) bonnet rotation speed. A range of process conditions was thus found to deliver surface roughness below 0.5nm rms in the 50 nm to 10 um spatial wavelengths range.

Corrective polishing experiments were subsequently carried out, using process parameters that deliver surface roughness below 0.5 nm rms whilst attaining relatively high removal rates (above 0.1 mm3/min). Interferometric measurements of the flatness error were fed into feed rate moderation software, for tool path output to a 7-axis CNC machine. Flatness error improvement was thus demonstrated from 200~300 nm P-V down to 50~100 nm P-V.

Finally, a series of experiments was carried out with varying process conditions at the edge of the photomask substrate (by reducing the sub-aperture polishing spot diameter and slowing down its relative feed rate). Analysis of data from this series of experiments provides clues of a potential ability to increase the quality area of EUV photomasks beyond the 5 mm defined in the specification.

8880-99, Session 16

## Simulation and correction of resist charging due to fogging in electron-beam lithography

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Improvements in the variation of critical dimensions (CD) and placement accuracy in electron beam lithography (EBL) are of high practical importance in the modern maskmaking industry where acceptable variations are on the one nanometer range over an entire

mask area. Primary electrons scatter in resists and substrates; they produce backscattered and secondary electrons that reach objective lens. These electrons, in turn, produce third generation electrons from the lens; they come back to the resist and provide additional exposure and charging. This fogging effects both CD variation and placement accuracy. In this paper, we present simulations of fogging at various conditions.

The Monte Carlo simulation tool CHARIOT was updated in order to enable the simulation of multiple generations of fast and slow electrons from objective lens and other objects over the substrate. The 3D simulation mesh was able to model electron scattering at a sub-nanometer scale to achieve the required accuracy, while still allowing the simulation area to be centimeters in area, combining two competing requirements.

The simulation results of charges deposited on the resist as well as the absorbed dose variations due to fogging are presented. The charge distribution due to fogging for multiple conditions of EBL system setups were simulated: beam voltage, working distance, and the diameter of the hole in the objective lens were varied. While dose variation is produced mostly by relatively high speed electrons, resist charging due to fogging is produced mainly by low voltage electrons.

The resist charging deflects electron beam from the intended landing point, this results in placement error. It is known that displacement due to charging is the major error term in the placement error. EBL systems are capable of correcting the placement error if the error map is known. Prediction of the placement error for any layout is provided by the DISPLACE software. The software takes into account EBL system setup, resist parameters, and writing order; the output is the placement error map due to charging.

8880-46, Session 17

## A novel design-based global CDU metrology for 1X nm-node logic devices

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As dimension of device shrinks to 1X nm node, an extreme control of critical dimension uniformity (CDU) of masks becomes one of key techniques for mask and wafer fabrication. For memory devices, a large number of optical techniques have been studied and applied to mask production so far. The advantages of these methods are to eliminate the sampling dependency due to their high throughput, to minimize the local CD errors due to their large field of view (FOV) and to improve the correlation with wafer infield uniformity if they have scanner-like optics.

For logic devices, however, CD-SEM has been a single solution to characterize CD performance of logic masks for a long time and simple monitoring patterns, instead of the cell patterns, have been measured to monitor the CD quality of masks. Therefore a global CDU of the mask tends to show its ambiguity because of the limited number of measurement sites and large local CD errors. An application of optical metrology for logic mask is a challenging task because patterns are more complex and random in shape and because there is no guarantee of finding patterns for CDU everywhere on the mask. CDU map still consists of the results from the indirect measurements and the traditional definition of uniformity, a statistical deviation of a typical pattern, seems to be unsuitable for logic CDU. A new definition of CDU is required in order to maximize the coverage area on a mask.

In this study, we have focused of the possibility of measuring cell patterns and of using an inspection tool with data base capability, KLA Teron617, to find the areas where the repeating patterns exist and the patterns which satisfy a certain set of condition. Then we have devised a new definition of CDU and an algorithm with which CDU maps of each type of patterns, which are intensity-based or width-based, are combined into one universal CDU map. Then we have checked the feasibility and validity of our new methodology through evaluation its fundamental performance such as accuracy, reproducibility, and correlation with other CD metrology tools with a set of logic masks.

In addition to our conclusion, the requirements for measuring completely random patterns will be discussed briefly.

8880-47, Session 17

## EUV scatterometry-based measurement method for the determination of phase roughness

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AFM-based roughness measurement reveals the topography of EUV masks, but is only sensitive to the top surface. Scatterometry provides a more accurate approach to characterize the effective phase roughness of the multilayer, and it becomes important to determine the valid metrology for roughness characterization. In this work, the AFM-measured roughness data for a set of 6 test masks were compared to the power spectral density calculated from the scatterometry measurement. Both measurements of the substrate and mask blank were provided for comparison. In addition to in-plane measurement, our scatterometer has been modified for out-of-plane scattering measurement. Preliminary results showed noticeable discrepancies between AFM- and scatterometry-measured roughnesses, and we concluded specifying tolerable roughness by AFM-based measurement is limited. In this paper, we described an EUV scatterometry-based measurement method for the determination of phase roughness with the goal of minimizing the amount of physical scattering data to be collected and rendering the method compatible with potential future standalone EUV reflectometer tools.

8880-48, Session 17

## SEM image quality enhancement technology for bright field mask

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The Bright-field mask came to be used to print a small contact hole in ArF immersion multiple patterning lithography. And there are some technical difficulties when the small floating dot is to be measured by the SEM because of the shadow issue. However, the new scan technology of Multi Vision Metrology SEM E3630 presents a solution for these difficulties. The combination of new scan technology and the other MVM-SEM functions can provide further extended application with more accurate measurement result.

8880-49, Session 17

## Direct phase-shift measurement of an EUV mask with gradient absorber thickness

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We directly extracted the phase-shift values of an EUV mask by measuring the reflectivity of the mask. The mask had gradient absorber thickness along the vertical direction. We measured the reflectivity of the open areas (Mo/Si multilayer), and the dark areas (absorber) by using the EUV reflectometer at LBNL. We also measured the diffracted 0th order light intensities of grating patterns having several sizes of lines or contact holes. The phase-shift values were derived from these data assuming an interference model of the diffracted lights.

We found that the phase-shift values oscillated depending on the absorber thickness as expected from the simulation. This is due to the standing wave effect inside the absorber. The absorber thickness having 180 degree phase-shift, which works as an embedded attenuated phase-shifting mask, was ~ 72 nm. The reflectivity of the absorber at this thickness was 1.4 % (2.4% relative to the multilayer reflectivity). We therefore expect non-negligible phase-shifting effect on wafer printing. These values of course depend on the composition of the absorber.

8880-50, Session 18

## eMET POC: performance of the proof-of-concept electron multibeam mask writer *(Invited Paper)*

Christof Klein, Hans Loeschner, Elmar Platzgummer, IMS Nanofabrication AG (Austria)

A proof-of-concept electron multi-beam mask writer (eMET POC) has been realized in 2012, which utilizes 262,144 programmable beams of 20nm beam size and 50keV beam energy to pattern 6” mask blanks [1,2,3]. The eMET POC was designed from scratch to meet the requirements of the 11-nm half-pitch node, which was demonstrated on HSQ coated mask blanks [2].

In this paper, new performance data obtained with pCAR coated mask blanks will be presented and compared to HSQ results. Furthermore, long term stability and throughput demonstration results obtained at 12.8 Gbps data rate will be discussed.

[1] Christof Klein, Hans Loeschner, and Elmar Platzgummer, J. Micro/Nanolith. MEMS MOEMS 11(3), 031402 (2012)

[2] Elmar Platzgummer, Christof Klein, and Hans Loeschner, SPIE Photomask Technology BACUS 2012, Monterey, Sept 11 - 13, 2012, Proc. SPIE 8522 (2012)

[3] Elmar Platzgummer, Christof Klein, and Hans Loeschner, SPIE Advanced Lithography – Alternative Lithographic Technologies V, Proc. SPIE 8680 (2013)

8880-51, Session 18

## Shot count reduction for non-Manhattan Geometries: concurrent optimization of data fracture and mask writer design

Russell B. Cinque, JEOL USA Inc. (United States); Tadashi Komagata, Taiichi Kiuchi, JEOL Ltd. (Japan); Paolo Petroni, Thomas Quaglio, Luc Martin, Aselta Nanographics (France)

VSB mask writers, which create patterns using a combination of rectangles and right triangles, are ill-suited to non-Manhattan geometries. This issue is particularly acute for layouts which contain a large fraction of linear, “off-angle” patterns such as photonic or DRAM designs. Unable to faithfully reproduce the “off-angle” structures, traditional VSB mask writers approximate the desired design using overlapping shots. Fidelity to the original pattern comes at a cost of increased shot count and reduced throughput.

Aselta has developed a novel fracture algorithm to dramatically reduce the shot count of such designs. Using a traditional rectangle-only VSB, the new algorithm provides more than 10% shot count reduction. When combined with a modified JBX-3200MV VSB, the shot count is reduced by a factor of 2 in average while maintaining the same level of fidelity. The data preparation software tool has also the capability of trading off a more accurate level of fidelity with an even more reduced shot count.

The paper will first describe the basic principles of the fracturing algorithm and e-beam writer hardware configuration then demonstrate the advantage of the method on a variety of patterns.

8880-52, Session 18

## Turret-type electron gun for EBM-8000

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To reduce down time associated with routine cathode replacement we developed a turret-type electron gun for our electron beam mask writer, EBM-8000. The turret-type electron gun consists of a barrel-shaped electrode (barrel) and a rotation mechanism, with 8 thermal cathodes set on the barrel. The barrel was devised so that it can be rotated from outside of the gun chamber, and each thermal cathode can in turn face the anode. This enables us to exchange cathodes without venting the gun to atmosphere, thereby reducing the downtime for cathode replacement by 80% compared to conventional single-cathode guns.

Two key elements were considered in developing the turret-type electron gun: reducing fluctuation in beam current, and eliminating discharge sources.

Reducing fluctuation in beam current is one of the most important elements because it has an impact to CD accuracy. In EBM-8000, the current fluctuation must be 0.1% (3 sigma) or less to attain the CD accuracy specification. To achieve this goal, we measured the relationship between the cathode temperature and current fluctuation at a current density of 400A/cm2, and based on this relationship, we set the cathode temperature at the lowest value that satisfies the current fluctuation specification. This procedure enabled us to meet the EBM-8000 current density and CD accuracy specifications, and simultaneously decrease the evaporation speed of the cathode material; thereby increasing the cathode life to 180 days per cathode, or 4 years per electron gun.

Special treatment to eliminate discharge sources is necessary to realize long-term stability of the electron gun. In the case of the turret-type electron gun, the surface of the barrel must be specially conditioned at assembly to eliminate any risk of discharge when the gun is in service. We devised a conditioning sequence which repeatedly increases and decreases the voltage applied to the barrel in N2 atmosphere. This conditioning sequence allowed us to dramatically decrease the

probability of discharges, allowing us to achieve long-term stability operation.

8880-53, Session 19

## EUV multilayer defect compensation (MDC): latest progress on model and compensation methods

Linyong Pang, Masaki Satake, Danping Peng, Ying Li, Peter Hu, Dongxue Chen, Vikram L. Tolani, Luminescent Technologies (United States)

According to the ITRS roadmap, mask defects are among the top technical challenges for introducing extreme ultraviolet (EUV) lithography into production. Making a multilayer defect-free extreme ultraviolet (EUV) blank is not possible today and is unlikely to happen in the next few years. This means that EUV must work with multilayer defects present on the mask. A number of methods have been proposed in the past to deal with this problem. One of the most popular takes advantage of degrees of freedom in where the pattern is located on a blank, shifting it so that multilayer defects are covered by absorber to minimize their effects on the image. This method works if the number of multilayer defects is sufficiently small and the mask pattern has large absorber regions that may be suitably placed to cover them. It is therefore best suited to sparse, dark-field patterns. The probability that a solution exists decreases as the number of multilayer defects increases, or the density of absorber in the mask pattern decreases. Whether a solution exists for a particular blank-pattern combination depends on specific coordinates of the defects and absorbers.

The method proposed originally by Luminescent is to compensate effects of multilayer defects on images by modifying the absorber patterns. The effect of a multilayer defect is to distort the images of adjacent absorber patterns. Although the defect cannot be repaired, the images may be restored to their desired targets by changing the absorber patterns. This method was introduced in our paper at BACUS 2010, which described a pixel-based compensation algorithm using a fast multilayer model. The fast model made it possible to complete the compensation calculations in seconds, instead of days or weeks required for rigorous Finite Domain Time Difference (FDTD) simulations. Our second paper at SPIE Advanced Lithography 2011, extended the results from one-dimensional to two-dimensional patterns by formulating the problem with level-set methods. Our third paper at BACUS 2011 introduced new algorithms to consider process window, and allow repair tool constraints, such as permitting etching but not deposition. The multilayer defect growth model was also enhanced so that the multilayer defect can be “inverted”, or recovered from the top layer profile using a calibrated model. Our fourth paper at BACUS 2012 introduced a calibrated multilayer defect model, and its use to reconstruct profiles of layers of the reflector stack above the defect. A new method to compensate the phase error by material deposition was also proposed. Our fifth paper at SPIE Advanced Lithography 2013, covered simulation of all options to compensate multilayer defects, including absorber modification, material deposition combined with absorber modification, and multilayer peeling combined with absorber modification. A few multilayer peeling options were discussed and simulated.

Progress in MDC is the subject of this paper. First, a multilayer growth model is calibrated using the new data collected from SEMATECH EUV masks with natural multilayer defects. Calibration input data include the multilayer defect top layer profile and the substrate profile obtained with atomic force microscopy (AFM).

The calibrated model is then applied to perform Multilayer Defect Reconstruction (MDR) and Multilayer Defect Compensation (MDC). In the MDR application, inverse methods are used to extract information about the defect from an AFM profile of the multilayer film. The recovered multilayer defect profile is fed into the MDC engine to calculate the modified absorber pattern. A fast simulator for the EUV absorber and multilayer, Defect Printability Simulator (DPS), provides good accuracy for 11nm half pitch patterns.

A new method to compensate pit defects using nanomachining to correct both phase error and transmission error is also described. Simulation studies using this new method will be presented in this paper.

8880-55, Session 19

## Using segmented models for initial mask perturbation and OPC speedup

Ayman M. Yehia Hamouda, GLOBALFOUNDRIES Inc. (United States); Mohab Anis, The American Univ. in Cairo (Egypt); Karim S. Karim, Univ. of Waterloo (Canada)

Sub-wavelength photolithography heavily depends on Optical Proximity Correction (OPC), where the pattern fidelity and CD Uniformity can never be achieved without a good OPC. The OPC runtime-resource factor has been exponentially increasing every node, where it is currently approaching a dangerous level in terms of runtime and cost as the 20nm node is approaching industrialization. A reasonable portion of the OPC computation is spent in small iterative mask perturbations trying to reach a solution state that prints closer to the OPC target, followed by the final few iterations aiming to accurately achieve printability on target with an almost zero EPE. In our work we propose replacing the first iterations of OPC with a single fast multi-model iteration that can perturb the OPC mask into a shape that is very close to its final state. This approach reduces the OPC runtime by more than 30% without affecting the final mask quality.

8880-80, Session 19

## Full-chip implant correction with wafer topography OPC modeling in 2xnm FDSOI technologies

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Ionic implantation photolithography step considered to be non critical started to be influenced by unwanted overexposure by wafer topography with technology node downscaling evolution [1], [2]. Starting from 2xnm technology nodes, implant patterns modulated on wafer by classical implant proximity effects are also influenced by wafer topography which can cause drastic pattern degradation [2], [3]. This phenomenon is expected to be attenuated by the use of anti-reflecting coating but it increases process complexity and involves cost and cycle time penalty. As a consequence, computational lithography solutions are currently under development in order to correct wafer topographical effects on mask [3]. For ionic implantation source Drain (SD) on Silicon-on-Insulator (SOI) substrate, wafer topography effects are the consequence of active silicon substrate, SOI substrate, poly patterns, STI stack, and transitions between patterned wafer stack. OPC modeling development has started with a first modeling solution available addressing SOI related effects for devices developed in FDSOI technologies [3]. As this model is expected to be used for mask correction, this modeling development has to be continued to address also stack effects related to local bulk areas within SOI substrate for devices developed in FDSOI technologies.

In this paper, wafer topography aware OPC modeling flow taking into account exhaustive stack effects identified for devices in 28nm FDSOI technology is presented. Quality check of this full chip stack aware OPC model is shown through comparison of mask computational verification and known systematic defectivity on wafer. Also, the integration of wafer topography OPC model into OPC flow for mask correction is presented with quality and run time penalty analysis.

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