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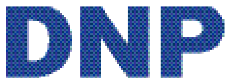
COFFEE BREAKS www.ravenano.com www.sematech.org www.microsi.com www.photomask.com	RECEPTION FOOD www.taiwanmask.com LANYARDS www.smt.zeiss.com/sms Wi-Fi www.microsi.com	TUESDAY LUNCH CO-SPONSORS  DNP America, LLC a Dai Nippon Printing company www.dnp.co.jp/eng www.kla-tencor.com WEDNESDAY BREAKFAST BREADS www.intel.com SESSION NOTEPAD www.nikonprecision.com
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Conference 8522: Photomask Technology

Tuesday - Thursday 11–13 September 2012

Part of Proceedings of SPIE Vol. 8522 Photomask Technology 2012

8522-1, Session 1

Transforming designs to chips: an end user's point-of-view on mask making *(Keynote Presentation)*

John Y. Chen, NVIDIA Corp. (United States)

The Photomask is a tool required to replicate a set of complicated IC geometries numerous times producing chips in large volume. It's arguably the most critical part in the manufacturing process because it has huge impact if it's not done right. Today, the definition of right means perfection. Whether it's data completeness or the pattern fidelity (placement and dimension), the requirement is zero flaws. This presentation will focus on the technology needs which challenge mask making capabilities including data preparation/OPC, CD & LER control, alignment and defect elimination.

As an end user, the speaker intends to discuss the impact of future lithography and mask making on the design and manufacturing of new products. He will emphasize performance, precision and perfection and the necessity of the three p's for the continuation of "Moore's Law."

8522-2, Session 2

2012 Mask Industry Assessment

Lloyd C. Litt, Matt Malloy, SEMATECH North (United States)

A survey supported by SEMATECH and administered by David Powell Consulting was sent to semiconductor industry leaders to gather information about the mask industry as an objective assessment of its overall condition. The survey was designed with the input of semiconductor company mask technologists and merchant mask suppliers. This is the eleventh consecutive year for the mask industry assessment. With ongoing industry support, the report has been used as one of the baselines to gain perspective on the technical and business status of the mask and semiconductor industries. It continues to serve as a valuable reference to identify the strengths and opportunities of the mask industry. The results will be used to guide future investments pertaining to critical path issues. This year's survey and reporting structure is similar to those of the previous years. Questions are grouped into following categories: general business profile information, data processing, yields and yield loss mechanisms, delivery times, returns, and services. Within each category are multiple questions that result in a detailed profile of both the business and technical status of the critical mask industry. This profile combined with the responses to past surveys represent a comprehensive view of changes in the industry.

8522-3, Session 2

JPM12 Best Paper: Photomask repair technology by using gas field ion sources

Fumio Aramaki, Tomokazu Kozakai, Osamu Matsuda, Osamu Takaoka, Yasuhiko Sugiyama, SII NanoTechnology Inc. (Japan); Hiroshi Oba, SII NanoTechnology Inc (Japan); Kazuo Aita, Anto Yasaka, SII NanoTechnology Inc. (Japan)

No Abstract Available

8522-4, Session 3

Improving mask CD uniformity using MB-MDP for 14nm node and beyond

Byung-Gook Kim, Jin Choi, Jissong Park, Chan-Uk Jeon, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Ingo Bork, Ryan Pearman, Sterling Watson, Aki Fujimura, D2S, Inc. (United States)

Model-Based Mask Data Preparation (MB-MDP) has been discussed in the literature for its benefits in reducing mask write times. By being model based (i.e., simulation based), overlapping shots, per-shot dose modulation, and circular and other character projection shots are enabled. This reduces variable shaped beam (VSB) shot count for complex mask shapes, and particularly ideal ILT shapes. In this paper, the authors discuss another even more important aspect of MB-MDP. MB-MDP enhances CD Uniformity (CDU) on the mask, and therefore on the wafer. Mask CDU is improved for sub-80nm features on mask through the natural increase in dose that overlapping provides, and through per-shot dose modulation. The improvement in CDU is at the cost of some write times for the less complex EUV masks with only rectangular features. But these masks do not have the basis of large write times that come from complex SRAFs. For ArF masks for the critical layers at the 14nm logic node and below, complex SRAFs are unavoidable. For these shapes, MB-MDP enhances CDU while simultaneously reducing write times. Simulated and measured comparison of conventional methodology and MB-MDP methodology are presented.

8522-5, Session 3

Impact of an etched EUV mask black border on imaging and overlay

Natalia V. Davydova, Robert C. de Kruif, Eelco van Setten, ASML Netherlands B.V. (Netherlands); Brid Connolly, Toppan Photomasks, Inc. (Germany); Norihito Fukugami, Toppan Printing Co., Ltd. (Japan); Ad Lammers, ASML Netherlands B.V. (Netherlands); Vicky Philipsen, IMEC (Belgium); John Zimmerman, Noreen Harned, ASML (United States)

There are multiple mask parameters that can be tuned to optimize the lithographic performance of the EUV photo mask [1]. One of them is the absorber height. A reduction of the absorber height allows for example a higher resolution and reduces the OPC needed for shadowing correction [1],[2],[5]. Downside of a thinner absorber is the increased reflectivity which manifests itself not only in the image field but also in the so called light shield area or image border.

The image border is a pattern free (absorber covered) area around the die on the photo mask forming the transition area between the part on the mask that is completely shielded from the exposure light by the Reticle Masking (REMA) blades and the die. The image border accommodates the finite REMA placement accuracy and the penumbra, the half shadow of the REMA blades allowing close spaced die printing on the wafer.

When printing a die at dense spacing, which is common practice in a production environment, its image border will overlap part of the neighboring die causing actinic and DUV (Out Of Band) light to expose

this area affecting the CD and contrast at the edges of the dies. This effect has been reported elsewhere. For a 44nm thick absorber we found a CD impact of 8nm [3] for 32 nm dense lines whereas for a 55nm thick absorber this effect was 4nm for 27 nm dense lines. Increasing the die spacing would prevent this unwanted exposure but results in an unacceptable loss of valuable wafer real estate thereby reducing the yield per wafer and is thus not a viable manufacturing solution.

There are other solutions. In a previous paper [3] we proposed correction by means of Optical proximity Correction (OPC) using Brion's Tachyon NXE model. An alternative is to create a so called black border: The reflectivity in the image border is reduced to a sufficient low level by, for example, increasing the absorber thickness, add a special coating or replace the absorber with a low reflective material [4]. The most radical solution is removal of the absorber and the underlying multilayer down to the low reflective substrate, so-called multilayer etching [4].

In this paper we will present the effects of such a black border created by a multilayer etch on features and their placement on the reticle and the impact on CD (27nm dense and isolated lines) and overlay on the wafer. By comparing the wafer CDU printed with and without black border we will determine how well the image border effect is mitigated by the multi layer etching.

[1] "EUVL mask performance and optimization", N.Davydova et.al. Proc. SPIE (2012)

[2] "Impact of mask absorber on EUV imaging performance", E. van Setten et.al., Proc. SPIE, Vol. 7545 (2010)

[3] "Imaging performance improvements by EUV mask stack optimization", N.Davydova et.al. Proc. SPIE (2011)

[4] "Light-shield border impact on the printability of extreme-ultraviolet mask", T.Kamo et.al., J. Micro/Nanolith. MEMS MOEMS 10 (2011)

8522-6, Session 3

An enhanced measure of mask quality using separated models

Anthony D. Adamov, Kazuyuki Hagiwara, Ingo Bork, D2S, Inc. (United States); Jin Choi, Jissong Park, Byung-Gook Kim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

Mask Error Enhancement Factor (MEEF) has been a standard measure of mask quality [BG Kim, 1995]. MEEF varies all mask dimensions by a fixed value and sees the difference in CD on the wafer. If a 1-nm increase on mask features (which are at 4x the features sizes on the wafer) results in a 1-nm increase on wafer, MEEF is 4.0. MEEF is the popular measure of sensitivity of mask CD to wafer CD. But MEEF needs to be extended for the complex mask era. With the emergence of complex masks with sub-80nm complex (non-rectangular) SRAFs, mask CDU is much more highly dependent on the shape and size of the feature. While features written on mask were orthogonal edges and wider than 100-nm, mask CDU had not been very different from one mask feature to another. Dose margin did not vary greatly from edge to edge, or shape to shape. Any detectable differences, such as from CD Split or slivers, were avoided or reduced significantly during data preparation. With sub-80nm complex SRAFs, dose margin differences are substantial, and CD Split becomes unavoidable. The new extended-MEEF is proposed by the authors in this paper. Simulation results demonstrate the difference among multiple sample data between MEEF and the extended-MEEF measures of CDU sensitivity.

8522-7, Session 3

Cold-development tool and technique for the ultimate resolution of ZEP520A to fabricate an EB master mold for NIL for 1Tbit/in2 BPM/HDD development

Hideo Kobayashi, Hiromasa Iyama, Takeshi Kagatsume, Tsuyoshi Watanabe, HOYA Corp. (Japan)

Cold-development is well-known as a resolution enhancement technique on polymer EB resists such as ZEP520A. As designing developer chemistry functioned to reduce dissolution speed for an EB resist resolution enhancement, so as cold-development works. Dip-developing with a developer solvent chilled by a refrigerator or a freezer, such a typical method had been used to carry it out in general in the past.

The above typical cold-development method, i.e. wafer immersion into a chilled developer, had several inferiorities obviously such as developer temperature instability during development process, temperature inconsistency between developer solvent and a wafer, water-condensation and pattern collapsing on drying, i.e. pulling out a wafer from the cold developer solvent.

We then tried to design and build a single wafer spin-develop tool, process sequence and recipe as well, for ZEP520A cold-development in order to solve those difficulties, and to accomplish a perfect cold-development in ambient air at a room temperature (RT). The process sequence in specific is, 1) prior to starting a cold developer solvent dispensing, firstly adjust quartz wafer temperature (WT) from the RT down to the target temperature (TT), and then 2) start dispensing a cold developer solvent chilled at the TT, next 3) start dispensing a cold rinsing solvent chilled at the TT, and next 4) start dispensing the second rising solvent at the RT until the WT passing over at least (lowest) a dew point of the ambient air, and finally 5) stop dispensing the second rinsing solvent, and start spin-drying up to finishing. We successfully built a single wafer spin-develop tool for the cold-development down to minus –10°C to deal with the above sequence automatically without the temperature instability, without the temperature inconsistency, without the wafer frosting.

By employing such a developer tool, we then tried to see effect of the cold-development for resolution enhancement on ZEP520A, and tried to quantify resolution limit by the cold-development down to minus –10°C in conjunction with varying developer chemistry. In specific, we tried to make hole patterns in hexagonal closest packing in 40nm, 35nm, 30nm, 25nm pitch, and examined holes in defect in shape, size and its distribution, by varying setting temperature from the RT to the TT in the cold-development, by varying developer chemistry from the standard ZED N-50 (n-amyl acetate, 100%) to ZMD-C (MiBK+IPA, 56%+44%) which is a rinsing solvent mixture originally. We also examined the other developer (solvent mixture) we designed MEK+FC, MiBK+FC and IPA+FC.

This paper describes cold-development tool and technique, and its results down to minus –10°C, for resist resolution enhancement on ZEP520A to fabricate 1Xnm bits (holes) in 25nm pitch to fabricate an EB master mold for Nano-Imprinting Lithography for 1Tbit/in2 bit patterned media (BPM) in HDD development and production.

Keywords: EBL, cold-development, ZEP520A, mold, BPM

8522-8, Session 3

Improvement of lithographic performance and reduction of mask cost by simple OPC

Koichiro Tsujita, Canon Inc. (Japan); Michael C. Smayling, Tela Innovations, Inc. (United States); Valery Axelrad, Sequoia Design Systems, Inc. (United States); Yuichi Gyoda, Ryo Nakayama, Canon Inc. (Japan)

These days such complex lithography solutions as inverse lithography technology and pattern splitting of 2 dimensional layouts are being introduced. However, the complexity of mask patterns leads to an increase of mask cost and reduces mask fabrication. We have developed an innovative SMO which optimizes lithographic conditions such as source and mask pattern at the same time. We can set a restriction of mask patterns in the SMO to make the mask patterns simple. Though the mask pattern is simple, since each pattern has independent optimization parameter and interaction between mask patterns and OPE by source is well balanced, the final result shows a good lithographic performance. We apply this technology to the cut pattern of 1 dimensional GDR layout of an SRAM, the array circuit, and the logic block of 20nm node and below. There the cut patterns are restricted

to be rectangles. For the cut pattern, the critical factors are as follows. Width: on-target where the cut intersects the line. Length: long enough to cover the line, short enough to not touch adjacent lines. These relaxed constraints allow the use of OPC which results in simplified patterns on the mask. The simulation work under ArF single exposure shows 16nm node of metal layer and 12nm node of gate layer can be resolved with simple rectangles. For both layers bright field exposure is used and positive and negative developments are applied for metal layer and gate layer respectively. It is also found that the simple pattern has lower MEEF than the complicated mask pattern by conventional OPC. We show the theoretical mechanism. Applying simple mask pattern and 1D GDR consisting of simple and regular layout, MEEF can be suppressed to be less than 5 even at the 16nm node. All this was confirmed experimentally. We also observed the masks of simple rectangles and complicated OPC pattern and found it was difficult to reproduce the latter pattern accurately. We could finally form the island patterns for the metal layer and cut patterns for gate layer on 25nm L/S of grid patterns through the total process of SADP, etching and so on. This is remarkable considering nodes below 16nm have been considered to be processed by NGL like EUVL.

We prepared mask data with various types of complexity of patterns in a full chip and evaluated the writing time of an up-to-date EB writer. The time depends on the shot counts and the typical shape with conventional OPC takes 4 times longer time than the rectangle. Since the cost of writing time is considered to be 20% of the entire cost, the saved cost can be 15%. Such complex pattern as that by inverse lithography takes 10 times longer time and has an impact on other technologies of inspection or process. The saved mask cost can be 30% or more. It corresponds to ~$100,000 per mask for advanced nodes.

8522-9, Session 3

A profile-aware resist model with an image location dependant threshold

Sylvain Moulis, Vincent Farys, STMicroelectronics (France); Jérôme Belledent, Romain Therese, CEA-LETI (France); Song Lan, Qian Zhao, Mu Feng, Laurent Depre, Russell J. Dover, Brion Technologies, Inc. (United States)

The pursuit of ever smaller transistors has driven technological innovations in the field of lithography, for example the resolution limitations of 193 nm wavelength lithography tools were overcome by for the introduction of immersion lithography. However, 20 nm technological node requires further new innovations in order to continue following the path of Moore's law, with EUV, e-beam and double patterning lithography as the primary candidates. As EUV and e-beam lithography are still not ready for mass production for 20 nm and not yet proven for the 14 nm node, double patterning lithography will play an important role for these nodes.

Double patterning comes in different flavour: Litho-Etch-Litho-Etch (LELE), Litho-Freeze-Litho-Etch (LFLE), and Self-Aligned-Double-Patterning (SADP). LELE and LFLE decompose the design in to two masks, each one being a part of the original design. SADP decomposes the design into two different masks: the core mask and the trim mask. The core mask lithography is used to create a mandrel around which a spacer material is then deposited, allowing the mandrel to be then etched away, just leaving the spacer material to define the pattern. The second mask, which is the trim mask, completes the original design. From a process perspective SADP is considered to be one of the most credible solutions for sub-20 nm nodes due to its better process tolerance and fewer overlay problems.

As the spacer width defines the minimum dimensions of the design, it is necessary to exert a tight control on it. The spacer material is deposited on the sides of the mandrel, and thus the side-wall-angle (SWA) of the mandrel will have a strong impact on the final width as well as on the robustness of the spacer pattern. We can decrease this impact by first etching the mandrel lithography in a hard mask and then depositing the spacer on it, but this solution adds some process steps, and therefore increases costs. It is then critical to be able to predict accurately the SWA of the mandrel resist patterns.

The SWA is pattern-dependant: it is more critical in 2D patterns containing corners, or on line-ends. A SWA model has been developed, enabling prediction of the mandrel resist profile. This allows tighter control of critical dimension (CD) by Optical Proximity Correction (OPC) for sub-20 nm technological nodes, as well as the possibility to predict resist loss which could induce a pattern failure after etch..

In this study, we propose to calibrate a SWA model based on atomic force microscope (AFM) measurements on 1D and 2D patterns. This model is based on some readily available commercial 2D resist models, on which we will apply a variable threshold as a function of resist height, to determine the resist profile. We will try different threshold functions in order to increase the model accuracy, which will be compared to a full physical model.

8522-10, Session 4

CD control with defect inspection: you can teach an old dog a new trick

Clemens S. Utzny, Albrecht Ullrich, Jan P. Heumann, Elias Mohn, Stefan Meusemann, Advanced Mask Technology Ctr. GmbH Co. KG (Germany); Rolf Seltmann, GLOBALFOUNDRIES (Germany)

Achieving the required critical dimensions (CD) with the best possible uniformity (CDU) on photo-masks has always played a pivotal role in enabling chip technology. Current control strategies are based on scanning electron microscopy (SEM) based measurements implying a sparse spatial resolution on the order of ~ 10-2 m to 10-1 m. A higher spatial resolution could be reached with an adequate measurement sampling, however the increase in the number of measurements makes this approach in the context of a productive environment unfeasible. With the advent of more powerful defect inspection tools a significantly higher spatial resolution of 10-4 m can be achieved by measuring also CD during the regular defect inspection. This method is not limited to the measurement of specific measurement features thus paving the way to a CD assessment of all electrically relevant mask patterns. Enabling such a CD measurement gives way to new realms of CD control. Deterministic short range CD effects which were previously interpreted as noise can be resolved and addressed by CD compensation methods. This in can lead to substantial improvements of the CD uniformity. Thus the defect inspection mediated CD control closes a substantial gap in the mask manufacturing process by allowing the control of short range CD effects which were up till now beyond the reach of regular CD SEM based control strategies. This increase in spatial resolution also counters the decrease in measurement precision due to the usage an optical system.

In this paper we present detailed results on a) the CD data generated during the inspection process, b) the analytical tools needed for relating this data to CD SEM measurement and c) how the CD inspection process enables new dimension of CD compensation within the mask manufacturing process. We find that the inspection based CD measurement generates typically around 500000 measurements with a homogeneous covering of the active mask area. In comparing the CD inspection results with CD SEM measurement on a single measurement point base we find that optical limitations of the inspection tool play a substantial role within the photon based inspection process. Once these shift are characterized and removed a correlation coefficient of 0.9 between these two CD measurement techniques is found. This finding agrees well with a signature based matching approach. Based on these findings we set up a dedicated pooling algorithm which performs on outlier removal for all CD inspections together with a data clustering according to feature specific tool induced shifts. This way tool induced shift effects can be removed and CD signature computation is enabled. A statistical model of the CD signatures which relates the mask design parameters on the relevant length scales to CD effects thus enabling the computation CD compensation maps. The compensation maps address the CD effects on various distinct length scales and we show that long and short range contributions to the CD variation are decreased. We find that the CD uniformity is improved by 25% using this novel CD compensation strategy.

8522-11, Session 4

Study of critical dimension uniformity (CDU) using a mask inspector

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Mask CDU map has many uses, including feed -forward to the e-beam mask writer to compensate for global process variation on the photomask and for wafer exposure systems to optimize intra-field CDU in semiconductor manufacturing. Mask CD SEMs are popularly used today to determine CD map after many process stages such as etching, developing and cleaning. However, full mask image information analysis with a mask inspector is one of potential solutions for overcoming sampling rate limitation of CD SEM measurement. By comparing the design database with the inspected dimension, the complete CDU behavior of the specific patterns can be obtained without extra work and tool time. These measurements can be mapped and averaged over various spatial lengths to determine changes in relative CD across the mask. Eventually, this methodology relies on the high stability of the optical system of the inspector. This paper studies the repeatability of the CDU map from a mask inspector and its correlation with CD SEM measurement on various pattern attributes such as feature size, tone, orientation and sampling length.

8522-13, Session 4

An impact of mask CDU and local CD variation on intra-field CDU

Junji Miyazaki, ASML Japan Co., Ltd. (Japan); Orion Mouraille, ASML Netherlands B.V. (Netherlands); Masaru Higuchi, Yosuke Kojima, Shunsuke Sato, Toppan Printing Co., Ltd. (Japan); Jo Finders, ASML Netherlands B.V. (Netherlands); Hiroaki Morimoto, Toppan Printing Co., Ltd. (Japan)

Critical dimension uniformity (CDU) control, especially intra-field CDU, is an important item for advanced lithography, and it has to be controlled very tight since it affects all the exposure fields. There are many contributors in the intra-field CDU such as mask, exposure tool, resist process and metrology. It is well known that the mask CDU influence to wafer intra-field CDU is becoming dominant because the mask error enhancement factor (MEEF) is quite high for low k1 lithography (1, 2). Also the above mentioned contributors impact the CDU by both global (field level) and local (grating level) variations. In this paper, we analyze in detail the CDU budgets where we clarify the impact of local CD variation.

Two test masks using advanced att-PSM and OMOG binary blanks were exposed on an immersion scanner at optimum illumination setting. For a couple of test features the CD values were measured at 1620 positions on the mask and wafer using a CD-SEM. The 50-nm staggered hole features using att-PSM showed a mask global CDU of 1.64 nm (3sigma) and a wafer intra-field CDU of 2.30 nm (3sigma), showing that the mask global CDU was a major part of the intra-field CDU. By applying a global mask CD correction using a MEEF of 5.11, the wafer intra-field CDU can be reduced to 0.953 nm (3sigma). We analyzed the wafer intra field CDU which is caused by the local CD variation (mask and process) and measurement noise. We could identify that a primary cause of the wafer intra field CDU after applying mask CD correction was coming from these local CD variation, which might disturbs the proper usage of dose correction of masks CD.

We'd like to demonstrate that the impact of mask local CD variation on the correction flow can be greatly reduced by applying multiple mask measurements within a grating, and hence to discuss the optimum conditions allowing for an accurate intra field CDU determination. We will also discuss how to optimize the CD sampling scheme in order to apply a dose correction on an exposure system to compensate for mask CDU.

[Reference]

(1) Jo Finders, et al, "Impact of reticle absorber on the imaging properties in ArFi lithography", EMLC 2012

(2) Yaron Cohen, et al, "PSM and Thin OMOG Reticles Aerial Imaging Metrology Comparison Study", EMLC 2012

8522-14, Session 4

Reticle CDU and wafer CDU correlation for 28nm reticle processes

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Reticle critical dimension uniformity (CDU) is one critical criterion for qualified mask layers processes. Normally, the smaller the three sigma value of reticle CDU is, the better is the reticle CDU performance. For qualification of mask processes, the mask layers to be qualified should have a comparable reticle CDU compared to the process of record (POR) mask layers. Because the reticle critical dimension (CD) measurement is based on algorithms like middle side lobe measurement, evaluation of the reticle CD-values cannot reflect aspects like reticle sidewall angle and variation in corner rounding which may be critical for 28nm technology nodes (and below). All involved tools and processes contribute to the wafer intra-field CDU (scanner, track, reticle, metrology). Normally, the reticle contribution to the wafer CDU should be as small as possible. In order to reduce the process contributions to the wafer intra-field CDU during the mask layers qualification process, the same toolset (exposure tool, metrology tool) should be applied as a POR-toolset. Out of the results of these investigations the correlation between wafer measurement to target (MTT) and reticle MTT can be obtained in order to accurately qualify the CDU performance of the mask processes.

We will demonstrate the importance for linkage between reticle MTT and wafer MTT for use of multiple mask processes and alternative materials. We will investigate the results for three processes of mask layers looking at advanced binary material from two suppliers. Objective of this article is to demonstrate the distribution between reticle MTT and wafer MTT as a qualification criterion for mask processes. The correlation between wafer CDU and reticle CDU of these mask processes are demonstrated by having performed investigations of dense features of different 28nm-technology layers (poly-layer, active-layer, and first-metal layers). Referring to the correlation between wafer and reticle MTT, the contribution of the reticle CDU to the wafer CDU can be used as an evaluation method for mask processes qualification. The dependency of the wafer intra-field MTT with respect to different reticle blank materials is also discussed.

8522-85, Session 4

Comparison of critical dimension uniformity measurements on an inspection system with measurements on a reticle SEM

John M. Whittey, KLA-Tencor Corp. (United States); Jan P. Heumann, Albrecht Ullrich, Advanced Mask Technology Ctr. GmbH Co. KG (Germany); Edgardo Garcia, Mark Wagner, KLA-Tencor Corp. (United States); Norbert J. Schmidt, KLA-Tencor Germany (Germany); Clemens S. Utzny, Stefan Meusemann, Advanced Mask Technology Ctr. GmbH Co. KG (Germany)

The spatial sampling frequency of SEM measurement systems on Photomasks is relatively sparse especially compared with 100%

inspection. By defining specific critical dimension criteria such as feature size, tone, orientation and sampling length it is possible to use the inspection process to measure critical dimensions relative to the design data base. These measurements can then be mapped and averaged over various spatial lengths to determine changes in relative critical dimension variations across the mask. This information has a variety of uses, including being fed back to the e-beam lithography systems used to generate the photomasks or fed forward to the wafer exposure systems to optimize intrafield critical dimension uniformity during semiconductor manufacturing. SEM measurement systems are used to determine feature sizes in photomask manufacturing facilities today. By comparing measurements obtained during inspection with measurements on reticle SEM, it is then possible to use results from both tools to obtain a more comprehensive understanding of critical dimension uniformity behavior across the mask. Each tool can then be used optimally. This paper compares SEM measurements on the photomask with inspection measurements on various critical dimension feature layouts.

8522-99, Session 4

CD uniformity improvement through elimination of hardware influences on post-exposure bake

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The tolerance level for CD signatures induced by any process step in the mask manufacturing process has been dramatically reduced with each technology node. Although influence from resist processes such as bake latitude has decreased to less than 1nm/°C, 0.1°C temperature non-uniformity translates into CD non-uniformity of 0.1nm or approximately 5 - 10% of the process budget. For future technology nodes, the post exposure bake process cannot exhibit any thermal imprint. The total temperature range must remain at zero throughout the entire treatment of the mask surface.

The influence of the measurement devices (wireless and wired sensor arrays) used to optimize the hotplate, on the performance of the Post Exposure Bake (PEB) process is discussed elsewhere. A zero degree total temperature range post exposure bake process for a multi-zone hotplate is proposed in this same study [1,2]. The proposed concept “mirror bake” is based on two symmetric individually wired sensor arrays, with the influencing hardware at opposite locations on the sensor array surface. Based on the individual hotplate optimization for each individual sensor array, a combined recipe for the multi-zone hotplate is calculated to compensate for the hardware influence.

In this paper the “mirror bake” concept is validated by comparing the CD uniformity data of masks manufactured with a PEB process using a single standard sensor array or masks using the “mirror bake” concept. The “mirror bake” concept achieved a CD uniformity improvement of up to 1.2nm (CD range). During this work additional hardware influences from the sensor arrays were identified.

8522-16, Session 5

Impact of EUVL mask surface roughness on an actinic blank inspection image and a wafer image

Takeshi Yamane, Tsuneo Terasawa, EUVL Infrastructure Development Ctr., Inc. (Japan)

Extreme Ultraviolet lithography (EUVL) is a promising technology for the fabrication of ULSI devices with a half-pitch of 22 nm and beyond. However, the fabrication of defect-free mask blanks, and their inspection continues to be a matter of concern. To address this issue, an actinic (at-wavelength) full-field EUVL mask blank inspection system with a dark-field imaging technique has been developed. In this technique, the light scattered from a mask blank surface reaches a CCD camera where a defect is captured as a spot signal brighter than the background level (BGL). In this system, a detection probability for a 1.2 nm-high 40 nm-wide programmed-defect was attained to be more than 99 % with an inspection time of 4.8 hours for full-field area of the mask blank. This result assures that the system could meet the demand for hp 16 nm node inspection.

The BGL is a measure of light scattered by the surface roughness of the mask blank. The average of BGL is due to the roughness with its period being shorter than the pixel size of the CCD camera on the inspection system, whereas the variation of BGL is due to the roughness where its period is longer than the pixel size, shot noise, and fluctuation of illumination intensity. In the case where a full-field area (140 mm sq.) of a mask blank is inspected, 7.84 x 1010 pixels data is collected. Due to the variation of BGL, some background signals in a full-field area may exhibit their intensities as large as a phase defect.

In this work, the background signals due to the mask surface roughness were analyzed. Images from some specific area of the mask blank were captured a number of times and accumulated. From the accumulated image, the influence of shot noise and fluctuation of the illumination intensity was filtered out. Therefore, the BGL variation of the accumulated image could be related only due to the roughness with its period longer than the pixel size. The specific area was also observed with AFM and compared with the accumulated image, followed by an analysis of the relationship between the roughness and the signal intensity of the accumulated image. Furthermore, the impact of the roughness on a wafer image was compared with that of a phase defect by using simulation. The results of this analysis will be reported.

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8522-17, Session 5

Illuminating EUVL mask defect printability

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For the next few years, the EUV Lithography (EUVL) community must learn to find mask defects using non-actinic inspection wavelengths. The non-actinic light cannot always determine the exact nature of the defect; whether it is a particle, pattern, or defect in the multilayer. It also cannot predict which defects will induce phase errors and which will induce amplitude errors on wafer. Correlating the signature of the defect as seen by a non-actinic inspection tool and on wafer resist image will inject essential knowledge into the non-actinic defect classification. This paper will explore the correlation between EUVL mask defect signatures detected (and not detected) at 193 nm inspection wavelengths and wafer-printable defects. The defects of interest will be characterized at mask level using atomic force microscopy (AFM) and critical dimension scanning microscopy (CDSEM). Simulations will be deployed to explain the signatures illuminated by both EUVL and 193nm exposures. This work addresses the gap between inspection sensitivity at non-actinic wavelengths and EUVL mask defect printability, and provide generalized understanding of how the two views differ.

8522-18, Session 5

EUV multilayer defect compensation (MDC) by absorber pattern modification: calibrating the model and validate accuracy with real data

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According to the ITRS roadmap, mask defects are among the top technical challenges to introduce extreme ultraviolet (EUV) lithography

into production. Making a multilayer defect-free extreme ultraviolet (EUV) blank is not possible today, and is unlikely to happen in the next few years. This means that EUV must work with multilayer defects present on the mask. A number of methods have been proposed in the past to deal with this problem. One of the most popular takes advantage of degrees of freedom in where the pattern is located on a blank, shifting it so that multilayer defects are covered by absorber to minimize their effects on the image. This method works if the number of multilayer defects is sufficiently small and the mask pattern has large absorber regions that may be suitably placed to cover them. It is therefore best suited to sparse, dark-field patterns. The probability that a solution exists decreases as the number of multilayer defects increases, or the density of absorber in the mask pattern decreases. Whether a solution exists for a particular blank-pattern combination depends on specific coordinates of the defects and absorbers.

The method proposed by Luminescent is to compensate effects of multilayer defects on images by modifying the absorber patterns. The effect of a multilayer defect is to distort the images of adjacent absorber patterns. Although the defect cannot be repaired, the images may be restored to their desired targets by changing the absorber patterns. This method was introduced in our paper at BACUS 2010, which described a simple pixel-based compensation algorithm using a fast multilayer model. The fast model made it possible to complete the compensation calculations in seconds, instead of days or weeks required for rigorous Finite Domain Time Difference (FDTD) simulations. Our second paper at SPIE Advanced Lithography 2011, extended the results from one-dimensional to two-dimensional patterns by formulating the problem with level-set methods. Our third paper at BACUS 2011 introduced new algorithms to consider process window, and allow repair tool constraints, such as permitting etching but not deposition. The multilayer defect growth model was also enhanced so that the multilayer defect can be "inverted", or recovered from the top layer profile using a calibrated model.

Progress in MDC is the subject of this paper. First, a multilayer growth model is calibrated using real data. A SEMATECH programmed defect mask of various dimensions prepared using e-beam patterning technology was used to calibrate the multilayer growth model. Calibration input data also included the multilayer defect top layer profile captured by Atomic force microscopy (AFM), and cross section captured by transmission electron microscopy (TEM). SEMATECH's AIT was used to image ML phase defects and compare their printability with simulation to verify the model accuracy.

The calibrated model was then applied to perform Multilayer Defect Reconstruction (MDR) and Multilayer Defect Compensation (MDC). In the MDC application, inverse methods were used to extract information about the defect from an AFM profile of the multilayer film. The recovered multilayer defect profile was fed into the MDC engine to calculate the modified absorber pattern. A fast simulator for the EUV absorber and multilayer, Defect Printability Simulator (DPS), provided good accuracy for 16nm half pitch patterns.

The modified absorber patterns were placed on the test mask, and printed to assess performance of this method. Comparison of the AIT print to DPS simulation will be shown.

8522-19, Session 5

Capability of EBeyeM for EUV mask production

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According to ITRS road map [1], sensitivity of EUV mask inspection needs to detect defect size of 20 nm in few years. EB (Electron Beam) inspection is one of the candidates to meet such severe defect requirement. EB inspection system, named EBeyeM, has been developed for EUV mask inspection. EBeyeM has high performance of sensitivity and throughput by using PEM (Projection Electron Microscope) technique and image acquisition technique to acquire image with TDI (Time Delay Integration) sensor while continuous stage moving [2].

In a previous study, we showed performance of EBeyeM whose sensitivity in particle inspection was 20-30 nm at 2 hours in 100 mm square, and that in pattern inspection was around 20 nm in a development phase [3], [4]. In a production phase, not only the sensitivity and the throughput but also stability is needed.

In this paper, as to the stability, repeatability was evaluated. Furthermore, as to the sensitivity and the throughput, the half throughput could be achieved with the almost same sensitivity as the conventional one by increasing current density in particle inspection.

From these results, we will report whether EBeyeM can use on production level.

[1] International Technology Roadmap for Semiconductors (ITRS) 2011 Edition, Lithography, List of Tables page11, table LITH6

[2] M.Miyoshi, Y.Yamazaki, T.Nagai, I.Nagahama and K.Okumura, "Development of A Projection Imaging Electron Microscope with Electrostatic Lenses", J.Vac. Sci. Technol. B17, (6), pp.2799-2802 (1999)

[3] T.Hirano, S.Yamaguchi, M.Naka, M.Itoh, M.Kadowaki, T.Koike, Y.Yamazaki, K.Terao, M.Hatakeyama, H.Sobukawa, T.Murakami, K.Tsukamoto, T.Hayashi, K.Watanabe, N.Kimura, N.Hayashi, "Development of EB Inspection System EBeyeM for EUV Mask", Proc. SPIE Vol.7823, 78232C (2010).

[4] S.Yamaguchi, M.Naka, M.Kadowaki, T.Koike, T.Hirano, M.Itoh, Y.Yamazaki, K.Terao, M.Hatakeyama, K.Watanabe, H.Sobukawa, T.Murakami, K.Tsukamoto, T.Hayashi, N.Kimura, N.Hayashi, "Performance of EBeyeM for EUV Mask Inspection", Proc. SPIE Vol.8166, 81662F (2011).

8522-20, Session 5

Electron-beam inspection of 16nm HP node EUV masks

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EUV lithography is one of the most promising solutions for 16nm HP node semiconductor device manufacturing. To manufacture the EUV masks, electron beam inspection (EBI) tool will be likely the necessary tool since optical inspection using 193nm and 199nm light are facing a limitation of resolution around 64nm EUV mask absorber pattern (16nm on wafer). Several challenges are expected to inspect these small patterns with EBI system. Firstly, required sensitivity is quite high. According to ITRS roadmap, the smallest defect size needed to detect is about 18nm for 15nm NAND Flash HP node. Secondly, small pixel size is likely required to obtain the high sensitivity. Thus, it might damage Ru capped Mo/Si multilayer due to accumulated electron beam bombardments. It also has potential of elevation of nuisance defects and reduction of throughput.

In this presentation, we share our initial inspection results for 16 nm HP node EUV mask using an EBI system eXplore 5400. We found that the EBI system has capability to capture 16 nm defects on 64nm absorber pattern EUV mask satisfying the sensitivity requirement of 15nm NAND Flash HP node inspection. Furthermore, we confirmed there is no damage to susceptible Ru capped Mo/Si multilayer. We also identified that low throughput and high nuisance defect rate are critical challenges needed to address the 16nm HP node EUV mask inspection. The high nuisance defect rate could be caused by poor LWR and stitching errors during EB writing of 64nm HP pattern. This result suggests we need further improvements of patterning processes for 16nm HP node EUV masks.

8522-21, Session 5

EUV mask inspection study for sub-20nm device

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Reflected light inspection has been used to inspect EUVL mask which consists of multi layers and metal absorber. However, sub-wavelength half pitch patterns and reflected inspection make unprecedented phenomenon like tone inversion. These lead EUV inspection more difficult in detectability and inspectability for separating out defects and falses.

In this study, we report the evaluation result of inspection dependency of illumination conditions like OAI(Off-Axis Illumination), sigma and polarization for sub-20nm EUVL PDM(programmed defect mask). With inspection of sub-20nm device mask, we finally address the inspection feasibility for sub-20nm device and the future direction of inspection technology.

8522-42, Session PS1

Study of droplet spray impact on a photomask surface

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To overcome the challenge of particle removal without pattern damage, it is important to control and optimize the physical force impact into a narrow energy distribution regime. This can be achieved by gaining in-depth knowledge into the fundamentals of physical cleaning methods as well as the process parameters affecting the performance of these systems. Droplet Spray is considered to be a gentle physical force technique. The droplet size and droplet velocity defines the kinetic energy of a droplet which transfers pressure (momentum) onto the substrate surface resulting into particle removal or pattern damage. Droplet pressure is directly influenced by gas and liquid flow rate as well as nozzle design (orifice size, etc.) and process parameters like nozzle distance and scan speed across the substrate surface. In this paper, effect of process and hardware parameters on droplet momentum transfer will be presented and related to kinetic energy as calculated from droplet velocity and size. Effect of these process parameters is studied on pattern damage and particle removal identifying a damage free surface cleaning regime.

8522-60, Session PS1

Study of the durability of the Ru-capped MoSi multilayer surface under megasonic cleaning

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Because the lack of a pellicle for EUV masks make them prone to particle contamination, EUV masks need to be cleaned frequently. Despite the relatively good resistance of the TaN absorber lines to pattern damage by megasonic cleaning, the Ru cap can be easily damaged by megasonic cleaning. In a recent study, we demonstrated that the dissolved gas type and concentration are critical factors in determining the cavitation types that eventually introduce pits on the surface of Ru-capped multilayer films. In particular, dissolved oxygen creates many more pits than dissolved CO_2 under similar conditions.

In this paper, we present the results of SEMATECH's extensive experimental studies of pit creation on Ru-capped multilayer EUV blanks by megasonics on as a function of frequency, acoustic field power, gas type, and concentration in ultra-pure water and chemicals during sonication. Pit dimensions were determined by AFM and correlated to different megasonic cleaning parameters. By correlating fluid velocity close to the surface and studying pit creation on the Ru cap by AFM, we determined the damage threshold conditions under which pit defects are created on the surface.

8522-62, Session PS2

Layout relocation considering defect inspection tolerance for EUV blank defect mitigation

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Due to the absence of defect-free blanks in extreme ultraviolet (EUV) lithography, defect mitigation is necessary before mass production. One effect way to mitigate defect impact is to cover all blank defects with absorbers of the layout, such that the defects will not be printed on wafer. Usually the EUV exposure system allows the mask to be shifted within a certain region, which leaves some freedom for the layout to be rotated and shifted on the blank. However, since the layout scale is huge and there can be billions of features on the layout, how to find the optimal orientations and locations efficiently to completely cover all defects becomes a challenging problem. On the other hand, the defect inspection tool might not be able to detect the exact sizes and locations of the defects accurately, so the inspection tolerance should also be considered during the layout relocation. Thus, among multiple optimal orientations and locations to place a layout on a blank, how to find the best one with the maximum inspection tolerance remains another problem.

In this paper, we first develop an intersection algorithm to efficiently obtain all feasible regions to place a layout on a blank. Due to the limited shifting freedom for the layout, each blank defect only impacts a certain portion of the whole layout, and the defect must be covered by the absorbers from its own impact region. In addition, the blank defects may have different sizes. In order to completely cover a defect, all absorbers within its impact region are shrunk first according to the size of the defect to form feasible regions. After that, each defect can be considered as a single point and the remaining problem is how to cover all defect points with its own feasible regions. To reduce the computational efforts for this problem, we divide each impact region into many small tiles. Instead of trying to cover all defects simultaneously, we only consider two of the defects at a time. Within a certain tile if no feasible regions can be found to cover both defects at the same time, the tile becomes redundant and not worth considering when processing the other defects in future. With more defects taken into consideration, the number of valid tiles becomes less and less, which save the computational efforts dramatically. Therefore, the runtime is super-linear to the number of defects. And the efficiency can be improved even further by sorting the impact regions first according to the number of valid tiles. In addition, if no feasible location exists, the algorithm can terminate quickly without processing all defects. Then in the next step, the obtained feasible regions are divided into overlapping rectangles that are maximal in area. By sorting the feasible rectangles, we are able to report the first n rectangular regions to place the layout on the blank with the best defect inspection tolerance.

8522-63, Session PS2

Efficient simulation of EUV multilayer defects with rigorous data base approach

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Defects below and inside multilayers of EUV masks belong to the most critical concerns for the application of EUV lithography in manufacturing processes. These defects are difficult to inspect and to repair. Moreover, they may print at different focus positions. Therefore, systematic investigations and classifications of such defects and the development of defect repair strategies are essential. This work can only be performed

with the help of simulations. In order to deal with the very specific and challenging simulation task different approaches based on fully rigorous electromagnetic field (EMF) solvers, partially rigorous EMF solvers and analytical approximation models have been presented. However, due to the high sensitivity of the simulation results on the defect parameters, the large defect parameter range, the complex structure of defective multilayers and the required accuracy the application of a fully rigorous EMF solver seems to be indispensable. One of the biggest challenges to be solved is the extensively long simulation time for the rigorous computation of EUV multilayer defects.

This paper presents the extension of the well-established rigorous EMF solver Waveguide (comparable to the RCWA approach) for the efficient simulation of structured EUV masks with multilayer defects. A typical and fully rigorous EUV multilayer defect simulation with our Waveguide solver takes several hours on a state of the art personal computer. This includes already extensive optimizations of all parts of the simulation algorithm. Such long simulation times make the systematic defect investigation and in particular the defect repair investigation very difficult. A powerful solution of the problem with the important feature to keep the fully rigorous simulation is a defect data base approach. The idea of this approach is to split-up the mask into the defective multilayer part and the absorber part. Both parts are computed rigorously using the Waveguide solver. The time consuming computations of the defective multilayer part can be performed separately and continuously for numerous systematically varied defect parameters and the results will be stored in a data base. Since the simulation time of the absorber part is usually in the range of seconds this part will be computed on demand during an investigation. This ensures the flexibility required for defect repair simulations. The coupling of the flexible on demand absorber simulation with the defect data base leads to very fast simulations with a large parameter range. The computation time of such a coupled and fully rigorous simulation of a structured EUV mask with multilayer defect is in the range of seconds up to a few minutes.

The new simulation approach will be presented in detail. Selected simulation examples of defect investigations and defect repairs demonstrate the functionality and the capability to perform fast and flexible EUV multilayer defect computations.

8522-64, Session PS2

High-brightness EUV light source for actinic mask inspection and AIMS

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Adlyte has demonstrated exceptional results including high brightness on it's EUV LPP light source. Adlyte is developing and commercializing two products to address the requirements for mask inspection and metrology. The products are low power source (LPS) and high power source (HPS) based on it's proven technology. The product platform has one main core combined with different optics to satisfy each individual application such as AIMS, ABI, and API. The current system demonstrates high brightness, which has been measured to be around 280W/mm2.sr with power at the source of 12W/2pi. The source can operate at high duty cycle, with a compact footprint and flexible architecture. In order to have the highest uptime an auto fuel-handling system has been designed in. The system has also been designed for high reliability in a high volume manufacturing environment. The fuel used to achieve the highest CE when irradiated with a high power diode pumped solid state Nd:YAG laser in the current product is high speed and frequency tin droplets. To minimize debris being detrimental to the first collector optics a state-of-the-art mitigation system has been developed and tested. In this paper we will discuss the current system performance results.

8522-65, Session PS2

Fiducial mark requirements from the viewpoints of actinic blank inspection tool for phase-defect mitigation on EUVL mask

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The requirements of Fiducial Mark (FM) on EUVL Mask were studied by experiments with EUV Actinic Blank Inspection (ABI) tool, E-Beam (EB) writer and other mask inspection tools to establish the phase defect mitigation method.

To cover the defect by absorber pattern shift with 3 sigma confidence level, the defect size and 6 sigma of total phase defect location accuracy; should be less than the pattern width. This total accuracy need to be reduced to < 20 nm (1 sigma) for next generation EUV blank inspection tools;[1].

In addition to the previous study for which FMs were etched by Focused Ion Beam (FIB) [2], we fabricated FMs by EB exposure and etching process, and inspected FMs with MIRAI EUV ABI tool. Then we estimated FM location accuracy for several line widths and depths.

And we also evaluated both of FIB and EB etched FMs with and without absorber coating on FMs by using EB writer and other mask inspection tools. Because these tools are necessary to detect amplitude defects, of which EUV ABI tool has weak detection capability, and to cover defects by absorber pattern shift. And we estimated FM location accuracy for several line widths and depths with and without absorber on these tools.

In this presentation, we will explain the experiment results of Fiducial Mark location accuracy which were fabricated by E-Beam exposure and etching process in addition to FIB etching, and inspected by MIRAI EUV ABI tool, EB tool and other mask inspection tools. And we will propose the optimum ranges of Fiducial Mark line width, depth, and fabrication method on EUVL Mask based on above results.

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[1] Pei-Yang Yan, Proc. of SPIE Vol. 7488, 748819, 2009.
[2] Tetsunori Murachi, Proc. of SPIE Vol. 8322, 832268, 2012.

8522-66, Session PS2

EUVL mask inspection at Lyman alpha

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Mask inspection is an outstanding challenge in Extreme Ultra-Violet Lithography (EUVL). The purpose of this investigation is to compare mask imaging characteristics of ArF (193nm) and KrF (248nm) inspection sources to a Lyman-alpha line of Hydrogen (121.6nm) inspection source. The Lyman-alpha source provides a raw resolution improvement of 36% compared to ArF and 51% compared to KrF sources, but the practical implementation of the Lyman-alpha source has not previously been evaluated in detail. Our comparison uses Rigorous Coupled Wave Theory (RCWT) and vector propagation through the optical system to simulate various partially coherent illumination schemes at each wavelength, using reasonably accurate mask material properties and dimensions. The entire multilayer stack and grating structure on the top surface are considered. The overall modeling is a combination of vector diffraction at the mask and vector imaging in a reflection microscopy configuration. The simulation study evaluates contrast for spatial frequencies representative of EUVL multilayer masks. Imaging and detection of defects on EUVL masks and mask blanks are also considered. One distinct advantage of the Lyman-alpha source is that the 121.6nm wavelength corresponds to an atmospheric transmission window. That is, a path length in dry air of nearly 2cm is reasonable. Therefore, a vacuum environment for mask substrate inspection is not required. One disadvantage of the Lyman-alpha source is that source brightness technology is not as mature as for ArF or KrF sources. Potential for application in approaching technology nodes is discussed.

8522-67, Session PS2

EUV mask blank defect avoidance solutions assessment

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It is anticipated that throughout the process development phase for the introduction of EUV lithography, defect free substrates won't be available - even at manufacturing stage non-repairable defects may still be present. We investigate EDA based approaches for defect avoidance such as reticle floor planning, defect avoidance by shifting the entire reticle field (pattern shift), defect avoidance through pattern shift in addition to layout classification (smart shift), and defect repair in data prior to mask write. This investigation is followed by an assessment of the complexity and impact on the mask manufacturing process of the various approaches. We then explore the results of experiments run using Mentor Graphics' software solution for EUV defect avoidance on various mask blanks, analyzing effectiveness and performance.

8522-68, Session PS2

Backside defect printability for contact layer with different reticle blank material

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Backside defects are out of focus during wafer exposure by the mask thickness and cannot be directly imaged on wafer. However, backside defects will induce transmission variation during wafer exposure. When the size of backside defect is larger than 200 microns, the shadow of such particles will locally change the illumination conditions of the mask patterns and may result in a long range critical dimension (CD) variation on wafer depending on numerical aperture (NA) and pupil shape. Backside defects will affect both wafer CD and critical dimension uniformity (CDU), especially for two-dimensional (2D) structures. This paper focuses on the printability of backside defects on contact layer using annular and quadrupole illumination mode, as well as using different reticle blank material. It also targets for gaining better understanding of critical sizes of backside defects on contact layer for different reticle blanks.

We have designed and manufactured two test reticles with repeating patterns of 28nm and 40nm technology node of contact layers. Programmed chrome defects of varying size are placed on the backside opposite to the repeating front side patterns in order to measure the spatial variation of transmission and wafer CD. The test mask was printed on a bare silicon wafer, and the printed features measured for size by spatial sampling. We have investigated two contact layers with different illumination conditions. One is advance binary with single exposure; another is phase shift mask with double exposure. Wafer CD variation for different backside defect sizes are demonstrated for the two contact layers. The wafer bright light defect inspection for backside defects will also be demonstrated.

8522-70, Session PS2

Key issues in automatic classification of defects in post-inspection review process of photomasks

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The mask inspection and defect classification is a crucial part of mask preparation technology and consumes a significant amount of mask preparation time. As the patterns on a mask become smaller and more complex, the need for a highly precise mask inspection system with high detection sensitivity becomes greater. However, due to the high sensitivity, in addition to the detection of smaller defects on finer geometries, the inspection machine could report large number of false defects. The total number of defects becomes significantly high and the manual classification of these defects, where the operator should review each of the defects and classify them, may take huge amount of time. Apart from false defects, many of the very small real defects may not print on the wafer and user needs to spend time on classifying them as well. Also, sometimes, manual classification done by different operators may not be consistent. So, need for an automatic, consistent and fast classification tool becomes more acute in more advanced nodes.

Automatic Defect Classification tool (NxADC) which is in advanced stage of development as part of NxDAT1, can automatically classify defects accurately and consistently in very less amount of time, compared to a human operator. Amongst the defects detected by the Mask Inspection System, NxADC identifies several types of false defects such as registration error, false defects due to problems with CCD, noise, etc. It is also able to automatically classify real defects such as, pin-dot, pin-hole, clear extension, multiple-edges opaque, missing chrome, chrome-over-MoSi, etc.

We faced a large set of algorithmic challenges during the course of the development of our NxADC tool. These include selecting the most efficient image alignment algorithm to detect registration errors (especially when there are sub-pixel registration errors or misalignment in repetitive patterns such as line space); differentiating noise from very small real defects, registering grey level defect images with layout data base, automatically finding out maximum critical dimension (CD) variation for defective patterns (where patterns could be Manhattan as well as all angle), etc. This paper discusses about many such key issues and suggests strategies to address some of them based upon our experience while developing the NxADC and evaluating it on production mask defects.

8522-71, Session PS2

RDMS: a Windows-based reticle defect search database with AHDC for interconnected mask and wafer fabs

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Ever imagine life without a search engine? Now imagine if there was a search engine for reticle defects that allowed you to search, trend size, and relate defects on any reticle from any inspection tool, in any of your interconnected fabs, at any time with a performance similar to a typical Google search. What would you do with it?

With EUV upon us, it is ever more critical that we be able to organize reticle inspection data in a manner that can be data mined at one's finger tips. Given the uncertainly involving EUV defect classification, it is important that the process engineers at the mask and wafer fabs have access to as much defect data as possible about a given reticle. This data must be made available on common Windows based PCs or even tablet computers.

Information is and has always been key. Information presented instantly and in an organized manner can give the user unparalleled insight into the Mask quality, process health, steps needed to improve yield and throughout time.

Presented here is a comprehensive reticle defect management system backed by a relational database architecture that can be deployed at the mask and wafer fabs in a distributed architecture. The advantage of such a system is that the defects on the mask can be tracked even after the reticle leaves the MaskShop and begins its life at the wafer fab. Not only so, the reticle defects can be tracked simultaneously across the mask and wafer fab infrastructure even when the reticle is repeatedly sent back for a reclean or to address Haze induced defect growth.

The system described here not only collects every inspection record (with images) from the most commonly used inspection tools, but it can also automatically classify defects, identify repeated defects from inspection of the same reticle as well as trend the size of all repeated defects with a few mouse clicks (or finger taps on tablet PCs). The population of inspection records in the analysis workspace could be distributed across the Maskshop and the Wafer fabs. Other features of the system include powerful search, complete reticle defect repair history and powerful metrology.

This article includes results from an automated heuristic defect classification (AHDC) algorithm for reticle inspections that mimics the classification rules. The results from AHDC are stored inside RDMS. AHDC does not require CAD data, thus it can be rapidly deployed in a high volume production environment without the need for extensive design data management. Measurement accuracy is generally much better than 1/75th the pixel size.

Various CD, residue, intensity difference, area metrics generated by the AHDC algorithm are automatically matched between defects in repeated inspections and are graphically trended. The framework presents these metrics to a technician for rapid decision making in a high volume production environment, in a concise and filtered manner, leading to faster throughput time and improved mask quality.

8522-72, Session PS2

Status of the AIMS(TM) EUV Project

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In previous conferences the status of the AIMS™ EUV project has been presented in which the basic layout scheme and preliminary design have been presented along with the targeted performance specification levels to be met. Presently the final design milestone of the project has been successfully completed and assembly of the prototype tool is underway. The final design concept will be presented along with the current status of the tool and simulated performance data.

8522-73, Session PS3

Double patterning for 20nm and beyond: design rules aware splitting

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Double patterning presents itself as one of the best candidates for pushing the limits of ArF lithography to 20nm technology node and below. It has the advantage of theoretically decreasing the minimum resolvable pitch by a factor of two, or the improvement of the process window by relaxing the lithographic conditions.

Double patterning though has its own complexities. Not only sophisticated algorithms are required to simply split the design into two exposures, but these two exposures have to comply with the design manual rules. The number and the complexity of these rules tend to increase for more compact designs in terms of minimum CD and layout topology which in turns increase the coding burden on engineers to let the splitting code be aware of such numerous rules.

In this context, we are proposing a new double patterning flow. It will be shown how the splitting can be done while taking into account numerous design rules. And finally, rules prioritization will be discussed in order to avoid conflicts between them.

8522-74, Session PS3

Placement-aware decomposition of a digital standard cells library for double-patterning lithography

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To continue scaling the circuit features down, Double Patterning (DP) technology is needed in 22nm technologies and lower. DP requires decomposing the layout into two masks. In some cases, it is not possible to decompose the layout into two masks due to the presence of mask violations after decomposition (native conflicts) which requires a re-design. This paper focuses on the placement of standard cells as part of a general framework for placement and routing for DP. Placing standard cells then trying to decompose the whole design or the whole standard cell block is very inefficient; since a native conflict inside a cell (internal conflict) requires a redesign and a native conflict on the boundary in-between two cells (boundary conflict) requires multiple iterations for placement and routing phases to get a clean decomposition. Unlike previous work that adds extra spacing between cells to avoid boundary conflicts, our target is to get a conflict-free decomposed layout through online-placement without adding extra spacing -to keep the area at a minimum- using pre-decomposed cells and considering the boundary effects of adjacent cells. This is done through two steps.

Step 1 is preparing a pre-decomposed library of standard cells to be used in the online-placement. The library contains several possible decomposition layouts (views) for each cell that contain no internal conflicts. The library also maintains a record of possible arrangements of views that can be placed adjacent to each other without causing boundary native conflicts. This step is performed only once to generate a DP version of the library. In our experiments, getting all possible views for all cells considering all possible boundary conditions was clearly a tough task if handled in a brute force approach because it needs considering a huge number of cell arrangements. A library of 100 cells would have close to a million different arrangements to be analyzed. Accordingly, we had to work first on reducing the number of cell arrangements using different reduction methods. The first reduction method is the “Correlated Boundary Reduction”, where groups of cells of correlated geometries at the boundaries are reduced to one representative cell. The second method is the “Margin Reduction”, where for each cell; based on cells margins calculations; we find all possible adjacent cells that might result in boundary conflicts; only these cells are considered in our analysis. After the reduction steps, iterations of decomposition of all resulting arrangements take place till the resulting views stabilize, and these views are all the possible views. Then, Step 2 feeds the results of step 1 to the placer to be aware of all cell views and their valid arrangements during placement.

Experimental results showed 40% reduction in the number of arrangements using the “Correlated Boundary Reduction” method, the “Margin Reduction” method drastically reduced the total number of arrangements to be analyzed to 6.4%. Finally, we were able to build a placement-aware DP-ready cell-library with an optimized number of cell views. This cell-library can be used with a DP-aware placement tool to provide a decomposed conflict-free layout.

8522-76, Session PS3

Novel customized manufacturable DFM solutions

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The paper is to provide DFM solutions on yield improvement based on foundry point of view. We have created the novel work flow to deploy the efficient yield enhancement ways in different design to silicon stage. In design environment, except for communicating with conventional design rule manual, aggressively, we may guide designer to employ the well-characterized regular logic bricks which built from process proven hotspots. Later, after design sign-off, mask preparation stage, the layout manipulation or layout retargeting are implemented to enlarge the process window when facing diversity of layout patterns in the design. At the same time, layout analysis and layout comparison, the two crucial methodologies, are used to capture all layout related detractors. The first one can identify the process sensitive hotspots, which will be highlighted and anchored as process limiters during the patterning process. Layout comparison can be used to debug the yield loss on similar process and design style, which is very efficiency way to narrow down the roadblocks of yielding. Another smart and customized solution is create the process control monitoring structures (PCM), which are extracted from previously yield ramping lessons and process hotspots. The PCMs will be dropped into scribe lane of production tapeouts and acted as pioneers of production ramp up.

All the process weakness hotspots are managed as the knowledge base, which will be continuously characterized and calibrated during the high volume manufacturing. Generally, this positive feedback loop of yield enhancement will benefit for both designer and manufacturer, especially for the cycle time of design to market and rapid ramp of product yield.

8522-77, Session PS3

Enhancement of mask process correction(MPC) through dose modulation of already geometrically corrected layout data

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Mask CD uniformity, CD linearity requirements continue to tighten along with shrinking wafer CD uniformity budget. Mask manufacturing using E-Beam at 32 nm process node and below is failing to meet these requirements due to the inherent systematic errors in the e-beam process. Electron forward scattering, backward scattering, fogging effect and beam blur are the major issues in e-beam lithography which cannot be ignored at advanced process nodes. Given a mask process model, there are multiple ways to correct and improve the CD signatures of patterned mask layout.

MPC-GC (Mask Process Correction through Geometric Correction) is a technique, which moves the edges of input shapes inwardly or outwardly to improve threshold intensity and slope at the shape boundaries. MPC-GC also adds new segments to the layout which could help in improving the fidelity between contours of printed shapes on mask with that of desired shapes. MPC-GC uses a mask process model and performs iterative simulations by moving edges or adding new segments to the layout to minimize a defined error function between simulated and desired contours.

In MPC-GC, minimization of error function is limited by the amount of allowed edge movements and the number of new segments which can be added. Ability to move segments gets restricted because of the neighboring edges. Adding new segments increases the shot count, which affects mask write time. So, the new segments cannot be added arbitrarily to improve the fidelity of simulated contour. Since, geometric correction is done under these constraints there will always be further scope to improve the intensity profile of the mask layout to achieve better fidelity.

In this paper, we discuss about an MPC flow to further enhance fidelity of the patterned shapes on the mask by adding dose correction on top of the geometric correction. In the proposed flow of MPC through Dose Correction (MPC-DC), the software can take 2 input layout data, viz. pre and post-GC corrected data. The objective would continue to be to increase fidelity of the simulated contours with respect to contours of pre-geometrically corrected data. However, the dose corrections would be made on the fractured shots of the post-geometrically corrected data.

We have developed NxMPC-DC tool as part of NxMDP(1) tool suite to achieve the above mentioned objective. If the input layout data is not fractured already, NxMPC-DC will use dose-correction friendly fracturing algorithm of NxFracture to enhance the effectiveness of subsequent dose modulation and then assign modulated dose values to the shots. NxMPC-DC would take the same mask process model as the one used for NxMPC-GC. Hence, in this proposed flow, the fidelity of the simulated contour would only improve beyond the MPC-GC corrected data as there would not be any conflict between the mask process models used for geometric and dose based corrections.

(1) NxMDP is a Mask Data Prep tool suite from SoftJin Technologies

8522-78, Session PS3

Efficient Boolean and multi-input flow techniques for advanced mask data processing

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Mask data preparation (MDP) typically involves multiple, sometimes many steps to ensure that the data is properly written on the mask. This may include multiple inputs, transformations (scaling, orientation, etc.), and processing (layer extraction, sizing, Boolean operations, data filtering). Many MDP techniques currently in practice require multiple passes through the input data and/or multiple file I/O steps to achieve these goals. This paper details an approach which efficiently process the data, resulting in minimal I/O and greatly improved turnaround times (TAT). This approach takes advanced processing algorithms and adapts them to produce efficient and reliable data flow. In tandem with this processing flow, an internal jobdeck mapping approach, transparent to the user, allows an essentially unlimited number of pattern inputs to be handled in a single pass, resulting in increased flexibility and ease of use.

Transformations and processing operations are critical to MDP. Transformations such as scaling, reverse tone and orientation, along with processing including sizing, Boolean operations and data filtering are key parts of this. These techniques are often employed in sequence and/or in parallel in a complex functional chain. While transformations typically are done “up front” when the data is input, processing is less straightforward, involving multiple reads and writes to handle the more intricate functionality and also the collection of input patterns which may be required to produce the data that comprises a single mask.

The approach detailed in this paper consists of two complementary techniques: efficient MDP flow and jobdeck mapping. Efficient MDP flow is achieved by pipelining the output of each step to the input of the subsequent step. Rather than writing the output of a particular processing step to file and then reading it in to the following step, the pipelining or chaining of the steps results in an efficient flow with minimal file I/O. As will be seen, this can result in significant improvements in TAT, depending on the configuration. While these improvements are obviously case-dependent, it will be demonstrated that for typical flows they can be large.

The efficient MDP flow is enhanced by a technique which allows in essence an unlimited number of pattern inputs by taking each transformed pattern and including it in an input jobdeck. Making use of established jobdeck handling capabilities, the user-selected input pattern/transformation combinations are mapped to an input jobdeck which is processed by the advanced flow, allowing great flexibility and user control of the process.

8522-79, Session PS3

Split-It!: From Litho Etch Litho Etch to Self-Aligned Double Patterning decomposition

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Double Patterning (DP) is still the most viable lithography option for sub-22 nodes. The two main types of DP are Litho Etch Litho Etch (LELE) and Self-Aligned Double Patterning (SADP). Of those two, SADP has the advantage of lower sensitivity to overlay error. However, the main problem of SADP is that it is too restrictive in comparison to LELE because stitches are not allowed in SADP, and a lot of pitch values are prohibited. Upon decomposing a layout that has not been designed for SADP, it is expected to find a large number of mask violations. In Spacer Is Dielectric (SID) tone of SADP, the smallest possible pitch can be achieved with layouts having spacing values equal to the width of the deposited sidewall (spacer).

One of the ways to do SADP decomposition is to use LELE decomposers while prohibiting stitches, and to generate mandrel and trim masks from LELE masks using some Boolean characterization equations. In this paper, we propose an SADP-decomposer that is based on an LELE decomposer, "Split-It!". However, the core of the LELE decomposer has been made SADP-aware. The mandrel and trim masks generator is based on Calibre SVRF (Standard Verification Rule Format) code that uses the LELE decomposer output and maps this output to the SADP masks. We focus on the SID tone and we study the effect of adding SID-awareness to the decomposition engine on the quality of the results.

Our decomposer is a graph-based decomposer. The system starts by hashing the polygons into a bucket structure that facilitates the spatial search among the layout features. The bucket structure is used to find the pairs of conflicting polygons that are separated by spacing values less than the minimum allowed. Then, the detected violations are used to construct a graph representation of the layout where a graph link between two polygons indicates a spacing violation. The graph has two types of violation links; namely, a spacer-width-spacing link and a non-spacer-width-value link. This differentiates between a violating distance of value equal to the width of the sidewall and a violating distance of a different value. The graph coloring algorithm executes in two rounds of depth-first traversal while switching colors between violating polygons such that they get assigned to opposite masks. The first round considers spacer-width-spacing links, and assigns pairs of polygons connected by this type of links to opposite masks. Then, the second round considers all links to color the remaining polygons. This way, the algorithm gives higher priority to polygons separated by sidewall width . Whereas, if the design has conflicts causing some mask violations, these conflicts will be localized at the spacing values that are not allowed in SADP and would need designer intervention or a retargeting algorithm to eliminate the conflicts.

The algorithm has been tested on the first metal layer, being the densest layer in the layout, in standard cell designs. Experimental results show that adding SID-awareness to the core of the decomposer has decreased the average number of coloring conflicts by 38%.

8522-81, Session PS4

Photomask quality evaluation using lithography simulation and precision SEM image contour data

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To evaluate photomask quality, the current method uses spatial imaging such as AIMS (optical).

This technique at 1Xnm node has a resolution limit, small defects will be difficult to extract.

To simulate the mask error-enhancement factor (MEEF) influence for aggressive OPC in 1Xnm node, wide FOV contour data and tone information are derived from high precision SEM images.

For this purpose we have developed a new contour data extraction algorithm with sub-nanometer accuracy resulting in a wide Field of View (FOV) SEM image: ($>10\mu m^2$).

In this time, we evaluate the MEEF influence of high-end photomask pattern using the wide FOV contour data of "MVM-SEM(TM) E3630" and lithography simulator "TrueMask DS(TM)" of D2S Inc.

As a result, we can detect the "invisible defect" as the MEEF influence using the wide FOV contour data and lithography simulator.

8522-82, Session PS4

Effective method for PV-Band comparison to lithography and etching process

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We developed an effective method for evaluating the correlation of shape of litho and etching pattern. The purpose of this method makes the relations of the shape after that is the etching pattern an index in wafer same as a pattern shape on wafer made by a lithography process.

Therefore, this method measures the characteristic of the shape of the wafer pattern by the lithography process and can predict the hotspot pattern shape by the etching process.

Thereby, although it was formerly only management of Hotspot in Litho, the influence on a problem peculiar to etching can also be estimated beforehand. We developed the technique of analyzing distribution of shape edge performance as the shape management technique. In this study, we conducted experiments for correlation method of the pattern (Measurement Based Contouring) as two-dimensional litho and etch evaluation technique. That is, observation of the identical position of a litho and etch was considered. It is possible to analyze variability of the edge of the same position with high precision.

In study, it reports on the outcome of the experiment for effectiveness and the accuracy of this method.

In other words, I calculate the shape of the lithography pattern corresponding to each exposure parameter and distance of contour of the etching pattern two-dimensionally. And, as a result, I evaluate width to be provided.Therefore, the production of the semiconductor considers not only the optimization of conventional Litho but also the performance by the etching, and general monitoring is possible by using the method.

8522-83, Session PS4

Grayscale and colorscale microstructures formed by layered distributing microdrops over polymer film for photomask utilized in single mask photolithography

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Abstract Grayscale and colorscale microstructures are formed through layered distributing microdrops over polymer film for construction soft photomask utilized in single mask photolithography in ultraviolet (UV) range, which demonstrate a modulated UV-light penetrating behavior through changing the distributing density of basic grayscale or colorscale microstructure shaped over polymer film used. A model to describe the penetrating behaviors of UV-light over polymer film covered by a large number of basic grayscale or colorscale microstructure constructed, for instance, typical square and other microstructures shaped by partially overlapping several squares, is set up. Several key factors, which will influence the surface character and the quality of acquired functioned microstructures in photoresist and further substrate

such as diffractive or refractive microlenses using soft photomask achieved according to the approach introduced by us, are discussed carefully. The optical penetrating characteristics of the fabricated grayscale and colorscale film structures are obtained experimentally. The measurement results are basically consistent with theoretical prediction.

Keywords Grayscale microstructure, colorscale microstructure, UV-light penetrating characteristics, microlenses

1.Introduction

Recently, with the rapid development of the micro-fabrication technique of micro-optical devices and miniaturized optical systems with the feature size of micrometer or even small to nanometer, micro-optical structures, for instance, typical refractive and diffractive microlenses and micro-mirrors for main applications in optical communication, MOEMS, optical integration, military and biomedical imaging, wavefront detection, optical display, and optical data storage, etc., are finding increasingly widespread applications. So far, many methods to fabricate high quality microlenses with binary or continuous profiles, for example, photo-sensitive or thermal-sensitive shaping, hot- or UV-embossing, injection mounding, molding or casting, combination UV-photolithography with thermally reflowing, holographic exposure, sol-gel process, sputteringly etching or milling by ion beam, ion exchanging, X-ray or high energy beam lithography, micro-contact printing, directly writing by modulated lasers or e-beam, diamond turning, chemical or electrochemical process, and micro-structural formation by filling preshaped concave template with desired optical materials, etc., have already been extensively employed. Generally, the technique involving the conventional ultraviolet photolithography for prototyping photoresist microlenses leading to substrate microstructures needed, which defines the critical feature size and the layout of three-dimensional patterned structures, should be close to the demands of commercial mass production because of a longtime and relatively mature development of integrated microelectronic industry. However, for numerous applications of microlenses, the requirements including further simplifying technological flow, reducing production cost, shortening preparing and performing time, promoting fabricating precision, improving optical performance, forming feature microstructures over the curved surface of substrate treated, and having better compatibility with standard integrated circuit technology, etc., have continuously motivated investigators to explore more simple and reliable means.

Current researches show that the grayscale photomask techniques based on different working principles are inherent of very high resolution, and suitable to fabricate many kinds of micro-optics structures such as microlens, waveguide, and fine grating, etc[1-6]. So far many grayscale formation approaches including the micromirror projection display, the high energy beam sensitive glass photomask, the halftone photomask, the modulated scanning laser beam or e-beam method, the ion exchange processing, etc., have been developed. But mapping the layout of functional microstructures in photomask is usually a nonintuitive, complicated, time consuming, and expensive process.

The method based on microdrop distribution controlled by computer shows some attractive and competitive features compared to grayscale techniques mentioned above, such as low computational and fabricating cost, rapid arrangement of grayscale or colorscale microstructures, and allows for a more easily and rapidly understanding of designing requirements and parameter selection, because of the rapid advance of micro-jetting technology with precisely positioning function. The approach, which utilizes the grayscale or colorscale microstructures introduced in this paper, has a fine positioning and aligning accuracy in implementing pattern transferring, and then the pattern shaping errors can be remarkably decreased, and thus relatively complex micro-structures can be fabricated through common and inexpensive photolithographic facilities, so as to offer a potential of meeting the demands as above. In Sec. II, a grayscale model is established for describing the penetrating behaviors of UV-light in photolithography operation. In Sec. III, the colorscale technique for photomask is shown, which is similar to grayscale case. Finally, a brief summary is given.

2.Figures

Fig.1.Cross-sectional profile character of grayscale pattern
Fig.2.Schematic of photolithography for typical diffractive and correspondent to cylindrical structure refractive photoresist microlens patterns fabricated by grayscale technology investigated by us.
Fig.3.Transmitting characteristics of UV-light over film wafers
Fig.7.Dependence relations of the UV-light transmitting power with grayscale microstructures introduced. over film wafer on color ranging from 0 to 255 at the brightness of 150

3.Summary

By orderly distributing basic grayscale or colorscale microstructures introduced by us over polymer film for soft photomask utilized in single-mask photolithography, the pattern structures with multiple phase levels or smooth surface profile, which corresponds to the diffractive or refractive microlenses, respectively, can be obtained easily. According to the theoretical model and experimental relations between the transmitting power of UV-light and color with different brightness, the pattern structures with circle or non-circle (envelope) profile can be formed. It can be expect that the grayscale and colorscale technique based on microdrop jetting principle will play an important role in the mass production of many micro-optical structures.

4.References

[1] Thomas Dillon, Anita Sure, Janusz Murakowski, and Dennis Prather, “Continuous-tone grayscale mask fabrication using high-energy-beam-sensitive glass”, J. Microlith. Microfab. Microsyst. 3, 550-554(2004).

[2] Brian Morgan, Christopher M. Waits, John Krizmanic, and Reza Ghodssi, “Development of a Deep Silicon Phase Fresnel Lens Using Gray-Scale Lithography and Deep Reactive Ion Etching”, JOURNAL OF MICROELECTROMECHANICAL SYSTEMS 13, 113-120(2004).

[3] Glenn H. Chapman1, Yuqiang Tu, Chinheng Choo, Jun Wang, David K. Poon, and Marian Chang, “Laser-induced Oxidation of Metallic Thin Films as a Method for Creating Grayscale Photomasks”, Proc. SPIE 6153, 61534G(2006).

[4] Zhaolin Lu and Dennis W. Prather, “Total internal reflection-evanescent coupler for fiber-to-waveguide integration of planar optoelectric devices”, OPTICS LETTERS 29, 1748-1750(2004).

[5] Jeremy D. Rogers, Tomasz S. Tkaczyk, and Michael R. Descour, “Removal of ghost images by using tilted element optical systems with polynomial surfaces for aberration compensation”, OPTICS LETTERS 31, 504-506(2006).

[6] Jeremy D. Rogers, Ari H. O. Kärkkäinen, Tomasz Tkaczyk, Juha T. Rantala, and Michael R. Descour, “Realization of refractive microoptics through grayscale lithographic patterning of photosensitive hybrid glass”, OPTICS EXPRESS 12, 1294-1303 (2004).

8522-84, Session PS4

Correcting image placement errors using registration control (RegC®) technology in the photomask periphery

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The ITRS roadmap specifies wafer overlay control as one of the major tasks for the sub 40 nm nodes in addition to CD control and defect control. Wafer overlay is strongly dependent on mask image placement error (registration errors or Reg errors) 1. The specifications for registration or mask placement accuracy are significantly tighter in some of the double patterning techniques (DPT). This puts a heavy challenge on mask manufacturers (mask shops) to comply with advanced node registration specifications. The conventional methods of feeding back the systematic registration error to the E-beam writer and re-writing the mask are becoming difficult, expensive and not sufficient for the advanced nodes especially for double pattering technologies.

In this paper we present test done utilizing the Carl Zeiss SMS recently developed technology called RegC®. Six production masks were measured on a standard registration metrology tool and the registration errors were calculated and plotted. A specially developed algorithm and the RegC® wizard (dedicated software) were used to compute a correction lateral strain field that would minimize the registration errors. This strain field was then implemented in the photomask bulk material using an ultra short pulse laser based system. Finally the post process registration error maps were measured and the resulting residual registration error field with and without scale and orthogonal errors removal was calculated.

Results: This work demonstrate a robust process flow in the mask shop which leads up to 32% registration 3sigma improvement, bringing some out of specifications masks into specifications, utilizing the RegC® process in the photomask periphery while leaving the exposure field optically unaffected.

Conclusions: It was proven that a registration correction strain field can be computed using the RegC® special algorithm with very high prediction capabilities of the post process residual registration error. It was demonstrated that a laser based correction method can be used to effectively reduce the registration error in the mask with no effect on any other mask properties and hence bring an out of specification mask into specification.

Key words: Image Placement, Registration, Wafer Overlay, Photomask, Laser, RegC®, RegC Wizard.

8522-86, Session PS5

Study for compensation of unexpected image placement error caused by variable shape beam mask writer deflector

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The Electron Optical System (EOS) is designed for the electron beam machine employing a vector scanned variable shaped beam (VSB) with the deflector. Most VSB systems utilize multi stage deflection architecture to obtain a high precision and a high-speed deflection at the same time. Many companies use the VSB mask writer and they have a lot of experiences about Image Placement (IP) error suffering from contaminated EOS deflector. And also most of VSB mask writer users are having already this error.

In order to use old VSB mask writer, we introduce the method how to compensate unexpected IP error from VSB mask writer. There are two methods to improve this error due to contaminated deflector. The one is the usage of 2nd stage grid correction in addition to the original stage grid. And the other is the usage of uncontaminated area in the deflector. According to the results of this paper, 30% of IP error can be reduced by 2nd stage grid correction and the change of deflection area in deflector. It is the effective method to reduce the deflector error at the VSB mask writer. And it can be the one of the solution for the long-term production of Photomask.

8522-87, Session PS5

Proximity effect correction optimizing image quality and writing time for an electron multi-beam mask writer

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Electron multi-beam mask writers address the challenge of long mask write times for increasingly complex masks. The writing speed of the multi-beam mask writer under consideration here depends on the maximum dose required for exposing the patterns. We present a proximity effect correction scheme that improves image quality (compared to a dose-only correction) and allows for a maximum dose limit. The scheme combines dose and shape correction to reduce line end shortening and improve image slopes by an overdose technique. Pattern homogeneity is improved by normal and inverted dummy patterns at a sufficient distance from feature edges. The improved pattern homogeneity reduces the required maximum dose. Further compensation strategies allow for a fixed maximum dose limit, albeit reducing image slope at some places in case the fixed maximum dose too aggressive. We test this scheme with and without maximum dose limit, and compare the achieved image quality against that for a dose-only correction. The results of this simulation study are verified by comparing top down SEM images of resist structures from exposures using the different corrections.

8522-88, Session PS5

Evaluation of CP shape correction for e-beam writing

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Character projection (CP) exposure reduces shot count of e-beam exposure by printing complex patterns in one e-beam shot. However, there is a deformation issue that must be addressed. The designed patterns on the CP stencil do not print faithfully on the substrate, particularly at the 1X dimensions of an advanced node.

The deformation of CP printing is decomposed into some elements: for example, CP stencil manufacturing error, proximity effect and the element which is caused by beam blur of the e-beam writer.

The element caused by beam blur can be predicted by measuring the total beam blur obtained from CD-dose curves. Therefore, based on the prediction, it is expected that intended patterns can be exposed by applying the correction to the CP stencil beforehand. Using both the deformations of standard cell exposed pattern and the measured beam blur, we confirmed that the standard cell patterns can be corrected by the shape modulation of patterns on the CP stencil.

Procedure used for the experiment is as follows:

(1) Standard cell patterns of 22nm node for direct write of wafer were exposed by one CP shot.

(2) Space collapse between exposed patterns, line end shortenings, corner rounding and effect of CP opening ratio were measured to obtain the correction parameters.

(3) The beam blur was calculated by CD-Dose curve obtained by line and space pattern exposure.

(4) Corrected CP stencil of standard cell was manufactured with applying shape modulation based on the result of (2) and (3).

(5) With using the corrected CP stencil, standard cell patterns were exposed by one CP shot.

We confirmed that our shape correction method is the appropriate solution for correcting the deformation issue of CP printing.

In this evaluation, because the relation between the fidelity of CP stencil and the beam blur was clarified, the required beam blur for the finer node patterns was revealed not only by the simple line and space patterns but also by measuring the deformations of the complex standard cell patterns. In addition, we simulated the optical system to realize the required beam blur. As a result, a small spherical aberration was found. We also report on this result.

Acknowledgement:

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8522-89, Session PS5

An 8192-channel grating light valve modulator for direct-write ultraviolet lithography

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Direct-write lithography holds the potential of revolutionizing micro-fabrication since it allows direct transmission of image data into the media, eliminating the time and cost of mask fabrication and maintenance. We have developed an 8192-channel direct-write spatial light modulator based on Grating Light Valve (GLV) technology. This diffractive linear pixel array operates at UV wavelengths from 350-450nm. It is a monolithically integrated device in which the silicon-nitride based GLV MEMS and the CMOS drive electronics are fabricated together on the same chip. The array operates with a refresh frequency of 250 kHz (4us), facilitating pixel transmission rates over 2 giga-pixels/s. Each channel driver supports 10-bit amplitude and 8-bit pulse edge timing control within the column period. When combined with 355nm illumination and 10:1 reduction optics, 1.5um minimum features can be printed with a placement resolution of 0.5um in both axes. In this paper, we will briefly review the operating principle, development highlights, system results and future applications of this novel direct-write modulator.

8522-90, Session PS6

Determining printability of reticle defects exposed under advanced SMO/ILT free-form scanner illumination sources

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ABSTRACT

In order to keep pace with ever shrinking features using 193nm lithography, the semiconductor industry is incorporating Source Mask Optimization (SMO) and Inverse Lithography Technology (ILT). These technologies often result in exotic customized scanner illumination sources as seen in Figure 1. Simulation shows that defect printability can be dramatically affected by changes in the illumination settings. This creates a challenge since only the latest model scanner emulator tools are capable of producing free form sources. In this study, we propose a new method of determining the printability of reticle defects using advanced Computational Inspection and Metrology algorithms to simulate scanner aerial images from reticle SEM images. This new approach is capable of simulating all free form illumination sources and is able to create reference aerial images from either defect free SEM images or directly from the mask design GDS. SEM images from a programmed defect test reticle are simulated using this new method under different illumination sources. The same defects are imaged with AIMS with the same illumination conditions as in simulation. The resulting data will be presented and compared showing the contrasts and correlation of the two methods.

Keywords: defect disposition, printability, simulation, scanner emulation

8522-91, Session PS6

Resist model validity regarding source variation in SMO

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Source Mask Optimization (SMO) is an advanced resolution enhancement technique with the goal of extending optical lithography lifetime by enabling low k1 imaging [1,2]. On that purpose, an appropriate source and mask duo can be optimized for a given design. SMO can yield freeform sources that can be realized to a good accuracy with optical systems such as the FlexRay [3].

Such optimization process is done through optical simulation to determine the source and the mask shape. Therefore, as a unique source shape is obtained, a unique optical model is generated. However, this optical model is not suffusing to predict the resist compортment, and a resist model has to be had to the optical model. Such model is generally calibrated once for a given source and corresponding wafer measurements.

However, SMO will yield different sources for different design layout, which could be similar or totally different. With the existing flow, a new optical model is generated for each source. But resist model remains unchanged due to unavailability of corresponding wafer data.

In this paper, we will study the validity of the resist model calibrated for a given source with respect to other sources. Both freeform and parametric sources will be presented and compared. The main goal of such study is to confirm if different sources can be used with the same resist model.

[1]. Alan E. Rosenbluth, et al. Optimum mask and source patterns to print a given shape. SPIE Vol. 4346, 2001, pp 486-502.

[2]. Alan E. Rosenbluth et al. Intensive optimization of masks and sources for 22nm lithography SPIE Vol. 7274, 727409 (2009)

[3]. Stephen Hsu et al. Source-mask co-optimization: optimize design for imaging and impact of source complexity on lithography performance. Proceedings of the SPIE, Volume 7520, pp. 75200D-75200D-11 (2009).

8522-93, Session PS7

Model-based fracturing with shot overlap for edge-based OPC layouts

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Resolution enhancement techniques such as Optical Proximity Correction (OPC) have enabled the semiconductor manufacturing industry to continuously shrink the critical dimension of integrated circuits. This results in increasingly complex masks and processing techniques leading to excessively long mask write times. In previous work, we proposed a model based fracturing algorithm allowing for shot overlap aimed at layouts resulting from pixel based OPC. In doing so, we minimize mask write time by directly determining the shot location, size and dosage from the curvilinear OPC mask.

In this work we propose a model-based fracturing algorithm for rectilinear masks, such as those resulting from edge-based OPC. Our approach is to determine the shot information based on the mask manufacturing model, allow for shots to be overlapped, thus decreasing shot count and mask write times. Our proposed method differs from current model-based techniques in a number of ways: (a) we allow for shot overlap; (b) we assume the input layout to be rectilinear resulting from edge based OPC, rather than curvilinear resulting from pixel based OPC with SRAFs; (c) it aims for zero edge approximation error between the resist contour and the desired mask.

Our proposed approach transforms the fracturing problem to covering polygons with overlapping shots. While there are polynomial time algorithms for solving the polygon partition problem, covering a polygon with overlapping rectangles is known to be an NP-complete problem. We propose a two-step greedy approach to find the best fracturing in situations where shot overlap is allowed. In the first step we heuristically cover the polygon with overlapping rectangles. While the covering problem is NP-complete, we have empirically found that this heuristic rectangle covering with overlap outperforms the optimal polygon partition without overlap in terms of rectangle count. This cover corresponds to an initial guess at shot placement. From there we incorporate the forward scatting and resist model to determine the shot dosage. First, we sample the mask contour and compute the influence of each shot onto the sampled points of the contour. To do so, we set up a least squares problem that seeks to minimize the mask error at the sampled points. In solving this convex least squares problem we determine the best dose for all of the placed shots. Next, we heuristically

update the locations of the edges for each shot by computing the edge placement error between the simulated and desired contours. Afterwards the shot dosage is recomputed with the updated shot locations to generate a more accurate shot placement and description.

We provide simulation results comparing the shot count and approximation error between our proposed approach and that of commercially available fracturing packages for a number of layouts. In addition, we compare the resulting shot count from our algorithm with that of the optimal partitioning of the polygon input into non-overlapping shots. We find that our algorithm is able to outperform commercially available software by 10% and is able to outperform the theoretic best polygon partition, that does not allow overlap, by 5%.

8522-94, Session PS7

Direct dose map synthesis for raster-based multiple electron-beam systems

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Abstract:

Multi-beam maskless lithography has been gaining momentum in the recent years. The delay, infrastructure problems, and high cost of EUV have increased the interest in alternative next-generation lithography techniques. Some regard maskless as technically and economically superior, and a more scalable solution, not only for prototyping, but also for high-volume manufacturing.

In this paper, we address the correction of proximity effects of maskless lithography. They comprise several components: Long range effects from electron backscattering, and short range effects such as beam blur, forward scattering, resist effects, etc. As feature sizes shrink, the complex short range effects increasingly cause poor patterning fidelity and aggressive e-beam proximity correction (EPC) is needed to correct for these errors. Traditional correction strategies target variable shaped beam (VSB) tools that provide capabilities to modulate the dose of individual shots. With limitations of dose-based correction, the strategy moved from pure dose correction to address long range effects into geometric and hybrid correction, increasingly employing correction approaches and platforms as they are used in optical lithography. These strategies are, however, still rooted in traditional geometric approaches. They fail to take full advantage of the raster-addressability of the multi-beam tools that employ thousands of controllable electron beams operating in parallel for the exposure. The raster-addressability of the exposure map enables innovation in the pattern synthesis for proximity correction. In this paper, we present a novel way to correct the proximity effects in e-beam patterning with pixel-based inverse algorithms.

The inverse correction framework we employ in the present paper is pixel-based and therefore matches the capabilities of the multi-beam tools. The proximity correction problem can be characterized as an inverse imaging problem, similar to the one in mask synthesis in optical lithography. The goal is to find a rasterized dose map, which meets the required contour matching criteria along with other desirable characteristics. Note that by directly synthesizing a pixel-based dose map, the separation between dose and geometric correction as it is known from VSB tools is removed. This provides an additional freedom in searching the entire available solution space in order to find an optimal solution.

An added advantage of the inverse formulation is to allow propagation of relevant e-beam specific properties in our synthesized dose map via regularization, or a Bayesian based a priori. To that effect, we introduce and discuss an energy minimization term, which aims to reduce the total energy of the dose map, a desirable property to minimize adverse e-beam patterning effects such as beam distortion, heating and charging effects. This results in underexposure of the center of fat features, an e-beam specific feature, which is also seen in dose-based approaches and rule-based approaches. We also discuss process window enhancement terms in our cost for improving the ILS of the e-beam aerial image.

We show simulation results for 15nm maskless lithography targeted at 5keV systems as the one developed by Mapper. We conclude by providing an outlook to account for the long range backscattering effects found in higher energy e-beam systems, and approaches towards speeding up inverse methodology for full-chip applications.

8522-95, Session PS7

Application of KrF (248nm) Alt-PSM (strong-shift) technology for special patterning requirements in MEMS applications

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Alternating Phase-Shift Mask (Alt-PSM) technology was proposed over 30 years by Dr. Levenson as a way to improve the performances of optical lithography (1,2). In the alt-PSM lithography, patterns of positive resist are created by the electrical field cancellation at the boundaries between 0o and 180o phase regions. As a result, we can achieve resist pattern line-width much less than the exposure wavelength even with small exposure NA (Numerical Apertures). In addition, the lack of zero-diffraction order in Alt-PSM lithography greatly enhances the exposure depth-of-focus and allows us to obtain small features with high aspect ratio in a highly topographic surface. Due to the pattern complexity in the IC (Integrated Circuit) design and the requirement of a trim mask to remove patterns formed in the un-wanted phase-edge regions, alt-PSM technology found very limited application in today's high volume IC manufacturing industry, where the lithography technologies are developed towards the continuous reduction of exposure wavelengths and the double, and triple patterning processes in a highly planar silicon surface. On the other hand, the MEMS (Micro-Electro-Mechanical systems) industry provides a unique opportunity to integrate the alt-PSM lithography into the device fabrication process. For example, the fabrication of magnetic writer heads used in the HDD (hard disk drive) industry requires a few photo-layers to pattern deep ultra-small line-width patterns with high aspect ratio and over a highly topographic surface. In addition, the high cost-of-ownership and limited critical layers make the ArF scanner introduction hard to be justified economically at the current generation of products. Based on these considerations, we selected the alt-PSM technology using our existing KrF process to accomplish photo-process requirement.

In this paper, we will discuss the application of Alt-PAM lithography in one of the critical layers in our MEMS process. We will discuss the design of the matrix mask to evaluate the feasibility of using Alt-PSM and the related patterning results. The printing results of the matrix mask demonstrated that we can achieve sub-150nm line over a sloped surface on 0.75-microns photo-resist with a KrF scanner. The FE (focus-exposure) matrix data indicated that the alt-PSM technology provides us with the adequate photo-process windows to meet the device fabrication requirement. As part of alt-PSM process, we will also discuss the selection of phase-shift areas and the associated trim mask design and the effectiveness of the OPC design..

Key word: Alt-PSM, MEMS, KrF patterning, Focus-Exposure Windows

Reference:

1. M.D. Levenson, et. Al, " Improving resolution in photolithography with a phase shifting mask," IEEE Trans. Electron Dev. ED-29 (12), pp. 1828-36 (1982)
2. Levinson, Harry (2004). Principles of Lithography (2nd edition ed.). SPIE-The International Society for Optical Engineering. ISBN 0-8194-5660-8.

8522-96, Session PS7

Impact of EUV photomask line-edge roughness on wafer prints

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The line-edge roughness (LER) of a photomask image has a measurable impact on the corresponding printed wafer LER. This impact increases as wafer exposures move from 193nm DUV to 13.5nm EUV wavelengths since the imaging tool is a low-pass filter with EUV passing more spatial frequencies. Even the high frequency mask LER may impact the wafer image by lowering its image log-slope (ILS). Studying the magnitude and frequency content of mask LER is a first step to reducing the wafer LER. The next step is to determine which components of mask LER actually transfer to the wafer LER. Order is imposed on this study by fabricating programmed LER patterns on an EUV mask to introduce controlled variations in LER spatial frequency and magnitude. More specifically, line-width roughness (LWR), LER and power spectral density (PSD) are extracted from 64nm and 90nm pitch lines on a programmed LER EUV photomask. The same mask is exposed on the ASML EUV Alpha Demo Tool (ADT) at Albany NanoTech. Standard wafer resist processes are deployed and the dose and focus are varied during exposure. Wafer LER, LWR and PSD are extracted and correlated back to the base mask patterns revealing an empirical LER transfer function (LTF) and PSD cutoff frequency. Exploration of the ILS, resist blur and speckle contributions to LER will be discussed. Finally, the study is extended to 45nm pitch lines by deploying a pupil filter on the ADT to explore the effect on LER as the feature sizes shrink.

8522-105, Session PS7

Dry etching technologies for reflective multilayers

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We have developed a highly integrated methodology for patterning Extreme Ultraviolet (EUV) mask, which has been highlighted for the lithography technique at the 14nm half-pitch generation and beyond.

The EUV mask is characterized as a reflective-type mask which is completely different compared with conventional transparent-type of photo mask. And it requires not only patterning of absorber layer without damaging the underlying multi reflective layers (40 Si/Mo layers) but also etching multi reflective layers. In this case, the dry etch process has generally faced technical challenges such as the difficulties in CD control, etch damage to quartz substrate and low selectivity to the mask resist.

Shibaura Mechatronics ARESTM mask etch system and its optimized etch process has already achieved the maximal etch performance at patterning two-layered absorber. And in this study, our process technologies of multi reflective layers will be evaluated by means of optimal combination of process gases and our optimized plasma produced by certain source power and bias power. A variety of experiments were conducted and results will be discussed in this study. Present status of the development and evaluation results of the system will be shown on our poster session.

8522-97, Session PS8

Reticle and wafer CD variation for different dummy pattern

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Dummy pattern fill to a layout for the purpose of raising the density of specific regions. Proximity effect of electron beam exposure, develop and etch performance of reticle show typical process effects, driven by pattern densities. Although the reticle processes are set up to compensate the influence of the pattern density, the reticle CD can vary with dummy pattern. When the isolated features become the nested features after the insertion of dummy pattern, the reticle CD variation is even larger because nested features exacerbate the proximity effect of electron beam. Another reason is that the reticle etch ratio as well as develop dynamics are also slightly dependent on the local density of pattern. With different dummy pattern around the main feature, the final reticle CD will be changed. Wafer CD of main feature is also depended on the surround patterns which will induce different boundary condition for wafer exposure.

We have investigated three reticles for 28nm first-metal layer; two of them are the same reticle advance binary blank material manufactured with comparable reticle process. The third uses the different reticle blank material with relative thin thickness of the absorber layer which is also made with a comparable reticle process. The optical proximity correct (OPC) test patterns are designed with two different dummy patterns. The CD differences of the three reticles will be demonstrated for different dummy pattern and will be discussed individually. All three reticles have been exposed and the wafer critical dimension trough pitch (CDTP) and linearity performance is demonstrated; also the line-end performance for two dimensional (2D) structures is shown for the three reticles. The wafer CD difference for CDTP, linearity and 2D structures is also discussed, respectively.

8522-98, Session PS8

Bimetallic grayscale photomasks for micro-optics fabrication using dual-wavelength laser writing techniques

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Microfabrication of high resolution micro-optics devices requires better than 1/8th wavelength (~60 nm) in both vertical and horizontal surface precision. Critical to this is the creation of grayscale masks with near 256 gray level resolution to create sufficient vertical precision in the photoresist. Grayscale bimetallic photomasks are bi-layer thermal resists consisting of two thin layers of Bi-on-Indium or Tin-on-Indium that can reach this precision. When written with a focused laser spot these films become controllably transparent by accurately varying laser power producing a thermally created bimetallic metal oxide whose optical density changes almost linearly in most regions from ~3 OD (unexposed) to <0.22OD (fully exposed). Previously, a direct-write raster-scan photomask system with a multi-line CW Argon-ion laser was used with feedback-controlled Gaussian beam to achieve 256-level grayscale masks. With the Gaussian laser spot, the feedback system was effective such that the average gray-level error reduced from ±4.2 gray-levels in an open-loop approach to ±0.3 gray-levels in a closed-loop approach. Test masks showed that remaining gray-level errors were due to the Gaussian beam profile which creates a thermal profile across the writing spot, translating into variations in gray levels. To correct this a beam shaper was used to change the laser spot to a flat-top beam. Raster-scanning the mask using the flat-top beam helps further reduced the gray-level errors. Preliminary results show that the flat-top beam reduces gray-level fluctuations, and lines can be written with less overlapped area helping to have higher resolution masks. Lateral precision of the pattern is set by the focused spot resolution as the bimetallic resists have been shown to produce at least 45 nm lines structures. The multi-line Argon laser enables the separation of a controllable system by dual wavelength separation from a single stabilized laser source. A stabilizer is targeted at keeping the Argon laser source power within 0.1% during the writing processes. Using the single 488nm (blue-green) line creates gives better control of beam shape in the modulated laser beam writing the pattern. At the same time a lower power stable 457nm blue-violet line is separated from the same laser an introduce in the beam path through the focused optics to characterize the grayscale pattern

both during the writing process (for feedback control of the bimetallic oxidation) and post writing mask metrology. Sensors below the mask plate spectrally separate the 457nm line enabling the high accuracy measurements. The mask Optical Density measurements are thus not affected by the modulation of the writing beam and done at a wavelength that has optical transmission levels near that of the bimetallic material at the photolithographic exposure system wavelengths. One target application is the creation of a Gabor superlens which requires multiple layers of aligned microlenses arrays and aperture produce through microfabrication. The microlens arrays must have lenses whose optical shape varies from lenslet to lenslet across an entire patterned surface of cm size. Laser direct written grayscale masks enable relatively low cost, rapid turn around mask production needed for creating such structures with microfabrication processes.

8522-100, Session PS8

Photomask etch: addressing the resist challenges for advanced phase-shift and binary photomask

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In order to successfully achieve the goals of the 16nm technology node on photomasks, one has to be able to write features down to 40 nm, develop, etch and be able to transfer them on to wafers. The aspect ratios for these features create resolution challenges during the direct write (charging issues) and wet develop processes for photomasks. The photomask industry is addressing this challenge by adopting ultra-thin resists. From a mask etch perspective, need for improved resist selectivity and an in-situ resist thickness monitoring becomes critical. During mask etch, we use optical emission spectroscopy and transmission methods to monitor film removal. In this paper, we will outline a novel approach to dynamically monitor resist removal rates for ultra-thin resists. Data will be presented on various binary and phase-shift film stacks, with final resist thickness targets in the range 400-600A.

8522-101, Session PS9

Process variation aware inverse mask optimization

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In post-optical lithography, printing sub-wavelength features is way beyond the Rayleigh diffraction limit and increasing the need of Resolution Enhancement techniques (RETs). In the near past, optical proximity correction (OPC) incorporating sub-resolution assist features (SRAFs) are extensively used in the semiconductor industry to improve the pattern fidelity and reduce the process variations, which pushes the limits of optical lithography for many generations in order to stay on the pace of Moore's Law. Unfortunately, the diffraction effects of light become more and more influential as critical dimension still shrinking. Thus pattern fidelity becomes highly sensitive to the process variations in the low k1 regimes. Therefore, such two techniques are of no avail. To overcome the two problems, Inverse lithography (IL) becomes a promising candidate which uses pixelated mask to obtain the more degrees of freedom than previous techniques in solution space. IL calculates the optimal masks by minimizing the designed cost functions incorporating the forward and backward algorithms. Various lithography conditions and requirements can be joined into the cost functions with adequately mathematically modeling. Hence the optimal mask can ensure the most important dual goal of optical lithographers. Recent researches propose many kinds of optimization algorithms, cost function designs, and hardware verifications. In this work, we present a process condition-aware gradient-based optimization approach which optimizes the pixelated mask not only at the perfect process condition but also other process conditions simultaneously. Our goal is to maximize the exposure-defocus (E-D) process window (PW). The images of the optimal masks at the perfect process condition will lose some pattern fidelity as other process conditions are jointly considered. However such tradeoff is in the realities of the situation. Thus balancing the pattern fidelity through the whole working range is the name of the game in our work. The gradients of the cost functions under different process conditions are derived. The gradients will be updated once process condition changing during computer practice. Hence the corrected patterns will be generated and placed automatically. By the way, the computational complexity of above gradients is usually high. Because of sampling many process conditions, the optimizations are always time-consuming. In order to address the above issue, adopting alternative gradient approaches will make our optimization efficient. In this case, some of the gradients out of the perfect process condition will be approximated. The approximated gradients can also have promising patterns but efficient. The results show that the process windows are enlarged by our proposed algorithm, and the speed is increasing. The images formed by final optimal masks are degraded at the perfect process condition, but hold acceptable pattern fidelity over the broad working range.

8522-102, Session PS9

Hotspot classification based on higher-order local autocorrelation

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Hotspot classification is an important step of wafer verification process. Under possible center-shifting condition, conventional hotspot classification using pattern similarity based on overlapping area calculated by overlaying two hotspot patterns directly is not suitable. This paper proposes a hotspot classification method based on higher-order local autocorrelation (HLAC). Firstly, we extract the features of the hotspot patterns using HLAC method. Secondly, the principal component analysis (PCA) is performed on the features for dimension reduction. Thirdly, the simplified low dimensional vector features of the hotspot patterns are used in the pre-clustering step. Finally, detailed clustering using pattern similarity calculated by discrete 2-d correlation is carried out. Because the HLAC based features are shifting-invariant, the center-shifting problem caused by the defect location inaccuracy can be overcome during the pre-clustering process. Experiment results show that the proposed method can classify hotspots under center-shifting condition effectively and speed up the classification process greatly

8522-103, Session PS9

Proximity effect correction parameters for patterning of EUV reticles with Gaussian electron-beam lithography

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Proximity Effect Correction (PEC) parameters for Electron Beam Lithography (EBL) are of critical importance for Critical Dimension (CD) uniformity and pattern fidelity in the manufacture of Extreme Ultraviolet Lithography (EUV) reticles[1]. The values of these parameters are well known for simple substrates, such as silicon wafers, but complex substrates such as EUV blanks, composed of several layers of materials (quartz, molybdenum, silicon and ruthenium) present a challenge[2,3]. The authors present a method for determining the PEC parameters for arbitrary substrates including silicon wafers, binary chrome reticles for 193nm optical lithography, and EUV reticles using a VB300 Gaussian EBL writer and patterns conducive to CDSEM metrology. The authors demonstrate the ability to utilize the parameters determined using this method to attain less than 3nm three-sigma CD uniformity across the pattern. The results of this empirical approach are compared to the results of Monte Carlo simulation to determine which layers in the EUV

stack have the most impact on the optimal PEC parameters obtained.

The proximity effect in EBL is composed of two components. The first is due to interaction of the electron beam with the substrate, where electrons backscatter and emerge from the substrate to pass through the resist again at a distance up to several tens of microns from the incident beam. The extra dose that the resist receives accumulates as the desired pattern is written, and has the effect of creating a background dose, lowering the dose to size for dense features, while sparse features remain comparatively unaffected. The character of the backscatter dose is generally approximated as a Gaussian with the parameters β and η describing the range (full width half maximum) and intensity (relative to the incident beam intensity). The second component of the proximity effect is due to the forward scattering of the beam as it passes through the resist. This is a short range effect on the order of nanometers that leads to line broadening with a pronounced effect in thick resists, and is ignored in this study.

The adverse effect of the proximity effect can be clearly seen in Figure 1 (a), (b) and (c) where the center of 100nm, 110nm and 120nm half pitch gratings are severely overdosed, while the edges receive a lower dose when the grating is exposed with a single, uniform incident dose. This is due to the difference in exposed area density at the center of the gratings (surrounded by exposed area), and at the edge (bordered by unexposed area). In this study 100nm half pitch gratings, 100µm on each side, with CDSEM targets spaced at intervals from center to edge are patterned on several substrate types (Figure 2). The patterns are proximity effect corrected for an array of β and η values using CATS software from Synopsys, and each target in the array is measured using a CDSEM to search the β and η, parameter space to find those values which yield the best CD uniformity across the grating, from center to edge as illustrated in Figures 3 and 4. Figure 1 (d), (e), (f) show gratings with the same half-pitches after correction using the optimal PEC parameters for the EUV substrate.

The method is applied to a variety of substrates including silicon wafers, 193nm reticle substrates and EUV reticle substrates. The PEC parameters are determined for accelerating voltages of 100keV (typically used for direct write in the College of Nanoscale Science and Engineering (CNSE) VB300 system) and 50keV (typically used in industrial mask manufacture). The results of these experiments are then compared to results derived from Monte Carlo simulations to determine the materials in the EUV reticle stack which most affect the PEC parameters.

8522-104, Session PS9

Particle transport in plasma systems for development of extreme-ultraviolet lithography mask blanks

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Extreme ultraviolet lithography (EUVL) is the leading next generation lithography technology to succeed optical lithography beyond the 22 nm technology node. Reducing defects on extreme ultraviolet (EUV) masks is one of the most critical issues to be addressed for commercialization of EUV lithography. The EUV mask blanks are deposited by ion beam deposition system where particle generated during the deposition process and within system are major sources of defects. Transport of sputtered particle or material in an ion-beam sputtering deposition system is a very complex electrostatic problem to devise mitigating solutions. The trajectory of these particles or atoms is affected by the ambient plasma density and temperature, the time dependent charge on the particles or atoms, and the potential drop between target and substrate, among other effects. In order to better understand contamination of surrounding components and ways to control the transport of material, we employ numerical simulation of a typical ion-beam sputtering system. We use the plasma simulation framework VORPAL, developed by Tech-X Corporation and CU Boulder, for studying these effects. In this poster, we will present initial simulation results of the transport of sputtered material in a parallel plate geometry for particle size on the order of 10-100 nm, plasma density of roughly 10^{12} cm^{-3} and applied voltage on the order of 100V. In particular, we address the effects of the plasma sheath at the target and substrate. The transport study of particles in similar plasma systems is highly important and beneficial but not limited to development of EUV mask blanks.

8522-106, Session PS9

Nanoparticle detection limits of TNOs RapidNano: modeling and experimental results

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Particles on EUV reticles are widely recognized as a major risk for printed defects. Due to the absence of a pellicle any particle on the reticle is projected in focus at the wafer. Defect-free IC-production demands the absence of particles larger than a quarter of the critical dimension on the reticle. Hence, every piece of equipment in the reticle handling chain shall be qualified on particle cleanliness. To this end TNO has developed the RapidNano, a particle scanner based on dark field microscopy. The RapidNano can detect very low numbers of added particles in equipment cleanliness qualification tests.

This paper describes a model for the scattering of light from a clean reflective surface having finite roughness, as well as from particles on such surfaces. The detection probability of PSL or Aluminum nanoparticles on AlCo, CrN and Silicon substrates can be calculated. The model predictions for the detection limit of nanoparticles are in excellent agreement with the experimental observations. Today's RapidNano detects 60 nm PSL spheres with a detection probability of 95% on an XXX-flat Silicon wafer. The model can be used to forecast on the detection limit of the next-generation RapidNano's, who are currently under development.

8522-22, Session 6

The e-beam resist test facility: performance testing and benchmarking of e-beam resists for advanced mask writers *(Invited Paper)*

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With each new generation of e-beam mask writer comes the ability to write leading edge photomasks with improved patterning performance and increased throughput. However, these cutting-edge e-beam tools are often used with older generation resists, preventing the end-user from taking full advantage of the tool's potential. The generation gap between tool and resist will become even more apparent with the commercialization of multi-beam mask writers which are expected to be available for production use in 2015. The mask industry needs resists capable of meeting the resolution, roughness, and sensitivity requirements of these advanced tools and applications.

The E-beam Resist Test Facility (ERTF) has been established to fill the need for consortium based testing of e-beam resists for mask writing applications on advanced mask writers out to the 11nm half-pitch node. SEMATECH and the College of Nanoscale Science and Engineer (CNSE) established the ERTF in early 2012 to test e-beam resist samples from commercial suppliers against the required performance metrics for each application at the target node. The ERTF makes use of the process and metrology infrastructure available at CNSE, including a Vistec VB300 Vectorscan e-beam tool adjusted to operate at 50kv. Resists are pre-screened on 300mm Si wafers through the CNSE wafer line with additional optimization cycles for promising materials. The best

performing resists are then tested on EUV and/or ArF mask blanks to gauge performance on the intended substrates. All results are added to the resist benchmarking database for trend analysis and identification of the best resists for each application.

An overview of the ERTF, and the key metrics, is provided. Tools, baseline processes, and operation strategy details are discussed, and resist testing and benchmarking results are shown. A gap analysis comparing the champion results to the required metrics for each application is presented. The long-term outlook for the ERTF and plans to expand the facility to include resist testing for e-beam direct write lithography are also discussed.

8522-23, Session 6

Conductive layer for charge dissipation during electron-beam exposures

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Electron beam resists develop a surface potential during exposure, which can lead to image placement errors of up to several nanometers [1] and account for poor CD uniformity and image quality. To address this problem, we have formulated a conductive polymer that can be coated onto the resist. Our conductive discharge layer (CDL) is water-soluble and it is easily removed during the processing steps.

Having established that our material has a low enough resistance for full charge dissipation, we have carried out extensive tests to evaluate the impact of the layer on lithographic performance. We will report these findings, which include measurements of the effect of CDL application on resist resolution, contrast, speed, and roughness of the resist on both wafer and on mask.

Keywords:Conductive discharge layer, image placement errors, E-beam lithography, chemically amplified resists, line edge roughness.

[1] K.D. Cummings, J. Vac. Sci. Technol. B (6) 1990, pg. 1786

8522-24, Session 6

Mask characterization for CDU budget breakdown in advanced EUV lithography

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As the ITRS Critical Dimension Uniformity (CDU) specification shrinks, semiconductor companies still need to keep a higher yield of good wafers per day and high performance (and hence market value) of finished products. This can not be achieved without continuous analysis and improvement of on-product CDU as one of the main drivers for process control and optimization with better understanding of main contributors from the litho cluster: mask, process, metrology and scanner.

In this paper we will demonstrate a study of mask CDU characterization and its impact on CDU Budget Breakdown (CDU BB) performed for an advanced EUV lithography with 1D and 2D feature cases.

We will show that this CDU contributor is one of the main differentiators between well-known ArFi and new EUV CDU budgeting principles. We found that reticle contribution to intrafield CDU should be characterized in a specific way: mask absorber thickness fingerprints play a role comparable with reticle CDU in the total reticle part of the CDU budget. Wafer CD fingerprints, introduced by this contributor, may or may not compensate variations of mask CD's and hence influence on total mask impact on intrafield CDU at the wafer level. This will be shown on 1D and 2D feature examples in this paper.

Mask stack reflectivity variations should be taken into account: these fingerprints have visible impact on intrafield CDs at the wafer level and should be considered as another contributor to the reticle part of EUV CDU budget.

We observed also MEEF-through-field fingerprints in the studied EUV cases. Variations of MEEF may also play a role for the total intrafield CDU and may be taken into account for EUV Lithography. We characterized MEEF-through-field for the reviewed features, the results to be discussed in our paper, but further analysis of this phenomenon is required.

This comprehensive approach to mask part of EUV CDU characterization defines delivery of accurate and integral CDU Budget Breakdown per product/process and Litho tool.

Better understanding of CDU budget for advanced EUVL nodes achieved by Samsung and ASML helps to extend limits of Moore's Law and to deliver successful implementation of smaller, faster and smarter chips in semiconductor industry.

8522-25, Session 6

Process challenges in advanced photomask etch processes

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As feature size decreases in photomask patterning processes, plasma etch processes have become more challenging to control pattern resolution, error budget, and defectivity. In this paper, we will address key plasma etch challenges during high resolution patterning development and manufacturing. Several performance metrics including resolution, reliability, and defectivity will be discussed to assess the etch challenges.

Critical Dimension (CD) resolution has always been a key challenge, especially for phase shift mask technology. Traditional chlorine-based etch chemistry in Cr absorbers has shown micro-loading effect which results in significant linearity degradation as aspect ratio increases. For recent years, several approaches were studied to address the linearity issue in photomask etch community. In addition to unit process improvement on resist and etch processes, new integration approach with hardmasks can enable to improve the resolution. We will discuss some resolution enhancement options in next generation mask technology. Plasma-induced charging issue has become another challenge. In general, plasma electrons can act as localized charging source on the substrates due to their isotropic nature. Irregular electrostatic charging can distort the trajectory of charged plasma particles on etching surface so that patterning performance can be significantly affected by surface condition. This type of the issue has been reported and studied extensively in Si-wafer processing for a couple of decades. As pattern size decreases in photomasks, the issues can deteriorate the process window. Some process metrics will be discussed to address the charging issue in plasma etch.

In photomask manufacturing, there are several critical factors to determine photomask quality. Process reliability in plasma etch can determine overall photomask quality metrics such as CD and phase. To improve manufacturing yield, it is so crucial to keep all process parameters reliable. Advanced process control technique can be a potential option to contain intrinsic process variability issue. Another key challenge in manufacturing is defect control. Any large defects induced by plasma process can directly impact the production yield and turn-around time. Furthermore, the defect size control becomes more critical as the minimum feature size is scaled down. We will discuss some options to improve the defectivity during plasma processes.

8522-26, Session 6

Advanced photomask fabrication process to increase pattern reliability for sub-20nm node

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As technical advances continue, the pattern size of semiconductor circuit has been shrunk. So the field of the photomask needs the processing more strictly. It is critical to the photomask which contained considerably shrank circuit and ultra high density pattern for sub-20 nm tech device, although a small defect is negligible in the conventional process. Even if some defect can be repaired, it is not satisfied with a strict pattern specification. Stricter fabrication process and pattern specification increase the manufacture cost. Furthermore, EUV photomask manufacture cost is several times expensive than the conventional photomask. Therefore the effort to decrease defects is important for the photomask fabrication process. In addition, when defects are occurred, it is obviously important that the repaired patterns have better pattern reliability. In this paper, we studied about advanced processes that control and remove hard defects minutely on ArF attenuated phaseshift mask. This study was accomplished for 4 areas. First of all, we developed advanced Mosi etch process. Defects occurred under this etch process are not fatal. The thickness of hard defects were controlled thinner under this etch process compared with conventional etch process. Secondly, we studied cleaning process that has good performance on Cr : MoSi surface and a poor hydrophilic contrast to control side effect by etch process. Thirdly, we made inspection technique for detecting thin thickness hard defects. Lastly, we researched a repair technology that is effective in hard defects of thin thickness. The performance of the repaired pattern was verified by AIMS. In this study, it is researched that control shape, properties of defects to prepare a reliable repair and improved repaired photomask pattern reliability by 30% over.

8522-27, Session 6

Study and comparison of negative tone resists for fabrication of bright field masks for 14nm node

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In order to meet the challenging patterning requirements of the 14 nm node, the semiconductor industry has implemented use of negative tone develop (NTD) and other tone inversion techniques on wafer to enable use of bright field masks which provide a better lithography process window. Due to e-beam write time and mask pattern fidelity requirements, the increased use of bright field masks means that mask makers must focus on improving the performance of their negative tone chemically amplified resist (NCAR) processes. In addition, the move to heavy use of bright field masks is introducing new challenges for mask makers. Bright field masks for 14 nm critical layers are required to have opaque sub-resolution assist features (SRAFs) as small as 50 nm while at the same time having across mask critical dimension (CD) uniformity of less than 2 nm (3 sigma) to meet the 2014 ITRS targets. Achieving these specifications is particularly difficult for bright field contact and via level masks.

This paper will survey the performance requirements for NCAR resists for building 14 nm critical level masks. As part of this survey, the results of current commercially available and development NCAR resists will be compared. The study will focus on key elements of the resist process pertaining to line edge roughness, pattern fidelity, minimum feature size, and critical dimension control through density with differences in resist type, sensitivity, and thickness. In addition, use of a novel flow cell test apparatus for detailed study of the develop loading performance of the NCAR resists will be described. Data showing the current capability of these NCAR materials as well as remaining 14 nm node performance gaps and issues will be presented.

8522-28, Session 7

Novel DPT methodology co-optimized with design rules for sub-20nm device

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Even though the extreme resolution enhancement technics such as off-axis illumination and computational lithography have been used to achieve enough process window and CD uniformity, we are facing severe limitation for sub-20nm node patterning because Extreme Ultra Violet (EUV) lithography is not ready due to technical challenges and low throughput. As an alternative solution, Double Patterning Technology (DPT) becomes the essential patterning scheme for sub-20nm technology node. DPT requires complex design rules because DTP rules need to consider layout decomposability into two masks. In order to keep design rule simplicity and achieve better designability, we propose two layout decomposition methodologies in this paper; 1) Mandrel generation for better uniformity, 2) Contact patterning to improve scalability.

FinFET becomes main stream of sub-20nm technology device architecture because the device reduces short-channel effects without highly doped channel/body which is not preferred due to severe dopant fluctuation. However, FinFET has high sensitive impact on variation of fin patterning. Therefore, we propose new DPT methodology to minimize CD variation of mandrels for fin patterning with SADP. For example, Fig. 1 illustrates different methods of mandrel generation with SADP. Since even number of mandrels for active fins as shown in Fig. 1(a) provide better symmetry for lithography and Reactive Ion Etch (RIE), mandrel generation in Fig. 1(a) can improve CD uniformity during fin patterning with SADP compared to the mandrel in Fig. 1(b).

Contact patterning of MOL has historically been one of the most challenging modules for sub-20nm technology. We studied DPT methodology optimization with given design rule set for local interconnect and contact layers. DPT methodology of Middle of Line (MOL) includes not only technical decomposition methodology but also DPT co-optimized colorless design rule. In order to achieve desired design scaling for sub-20nm technology node, we propose the chip-level decomposition methodology which can reduce extra space to prevent odd-cycle patterns at standard cell boundary. In addition, we developed colorless design rules to obtain proper scalability under the various special structures for gate contacting. Source Mask Optimization (SMO) for contact patterning was used to enhance resolution. With the approaches, we develop design flow to optimize design by implementing DPT compliance checking according to both colorless design rules and chip-level decomposition method. Co-optimizated design rules considering design, decomposition and process requirement enable us to obtain about 3% scaling benefits by comparison with normal DPT flow.

8522-29, Session 7

Mask design automation: an integrated approach

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Mask Design, or the process of assembling, arranging and configuring the pattern data required to make a photomask, has many characteristics that make it appropriate for automation, including a high order of complexity, many steps in the process flow, many parameters to define, and multiple flow variants. Traditionally Mask Design has been performed in several discrete steps, each having its own set of

tools, processes, data formats, and parameter sets. These include, for example, Boolean layer extraction, fill pattern generation, biasing, Optical Process Compensation (OPC), frame generation (assembling the patterns relevant to reticle and wafer alignment, automated bar code identification, masking/taping borders, process control monitors and test patterns); fracture (transforming design data formats into mask write tool formats); jobdeck generation (creating the mask write tool instruction set); and Mask Rule Checking (MRC). These separate and often non-compatible process flows make integration challenging. Additionally, the frame generation process typically has evolved in complexity ad hoc and is often not performed in a systematic manner that makes it easily adaptable to automation.

In this paper we describe a process-of-record driven approach to Mask Design automation. A hierarchical methodology is described that solves the frame generation problem universally, and treats the mask layout as a unified hierarchical structure. This automation provides a framework for combining multiple EDA tools into seamless, integrated, flexible process flows capable of processing OASIS and GDSII files through DRC, Boolean derivations, dummy fill generation, OPC application, frame generation, MRC, as well as other data manipulations, to produce inspection-ready jobdecks and pattern files, metrology guides, and reports required for mask manufacturing.

8522-30, Session 7

Generating well-behaved OASIS files for mask data processing

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Since the introduction of OASIS 1.0, the OASIS file format has gradually become adopted across the semiconductor manufacturing industry for advanced technology nodes. The OASIS standard provides a wide range of compaction and compression options. However, within this range of possible options, choices made during file creation can create significantly different OASIS files for the same design data. These differences can result in inefficiencies in mask data processing. This paper starts by pointing out some common problems with existing OASIS file generation and the corresponding issues that these problems create in subsequent processing. We then present some strategies and methodologies on generating well-behaved OASIS files. These strategies yield reductions in overall turn-around-time. We conclude with some comments on the OASIS standard for the future.

We begin by establishing the benefits of certain modal options of the OASIS format. In particular we wish to prove that if a file is in strict mode and both the S_CELL_OFFSET and S_BOUNDING_BOX properties are present for each cell within the file, then such a file is intrinsically faster to process. To test this hypothesis, we will generate post-OPC data files that contain the above characteristics. These files will then be taken through the mask preparation process without taking advantage of these modal options. This represents the processing time for the files that lack these modal options. The mask preparation process will then be repeated, this time taking advantage of the modal options, establishing the speed-up in processing due to the use of the OASIS modal options.

Our second goal is to establish the importance of data locality in an OASIS file. In this context, data locality refers to the correlation between data in the spatial domain (the geometry itself) and its storage domain (the file-offset of the geometry). Good data locality implies that data that is nearby geometrically are also nearby within the file. We intend to take a set of post-OPC designs and generate two sets of files, one with good data locality and one with poor data locality. These two file sets will then be taken through the same exact mask preparation process with the processing times recorded. The result will establish that OASIS files with good data locality can be processed much faster than those with poor locality.

Finally, we recommend the future OASIS standard add a multi-file variant. This is of particular importance as, without an established OASIS multi-file variant, processing time is wasted partitioning a single monolithic OASIS file into smaller pieces to facilitate distributed processing. Processing time is also wasted re-assembling the results back into a single monolithic OASIS file. We will provide data on the cost of partitioning and re-assembling to support our suggestion for the addition of a multi-file variant to the OASIS standard.

8522-31, Session 7

Novel routing layer trim/cut reduction in SADP SID process

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With the current VLSI technology node shrinking to 20nm, 193 nm immersion (193i) lithography with single exposure has reached its resolution limit, and double patterning technology has been widely applied in metal layer fabrication. Self-aligned double patterning (SADP) is a promising double patterning technology for the routing layer fabrication due to its overlay-tolerant capability. As most of the routing wires in one interconnect layer are unidirectional, it is also trivial to have the routing layer decomposed by simply assigning every other routing track cores (core tracks) and all the other tracks space (space tracks). For the wrong way wires, the requirement of even-jog is necessary. Besides the separations by jogs in the SADP process, the rest of the tip-tip and tip-line gaps have to be achieved by trim. For logic circuit design, the cut patterns are randomly distributed on every track across the layout, which can be very dense due to the small pitch size. It could be possible that routing layer is indecomposable because of the too dense cuts. Therefore, how to reduce the cut number in the trim mask to make the decomposition feasible becomes a critical question to further push SADP process for the future technology node.

In this paper, we propose a novel routing layer trim/cut reduction strategy for SADP SID process to largely reduce the density of the cut patterns (50% reduction on average), while keeping the original design unchanged. In the first step of core assignment, instead of simply assigning each core track to be a continuous single core, we use the discontinuous cores on one core track and let gaps between core wires defined by the spacers surrounding the cores. Since spacers of two adjacent core wires will merge together to form a single gap, two adjacent space tracks will still be completely separated from each other. In the second step of cut pattern fabrication, since a large amount of cuts on the core tracks have already been generated, the trim mask only needs to cut on the space tracks, and hence the density of cut patterns is largely reduced.

We can have obvious benefit from this approach. First, no extra process step is necessary, but the density of cuts on the trim mask can be largely reduced. Second, no complex decomposition algorithm is needed and the whole process can be implemented straightforwardly. Third, the approach has tremendous help on reducing the cut mask number once the wire pitch continuous to shrink, which will largely reduce the fabrication cost and increase the potential throughput.

8522-32, Session 7

Automatic marking by use of MRCC and range pattern matching for advanced MDP

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One step in MDP is the process of marking CD features via the jobdeck. These marks are usually further translated into specially formatted files used by optical metrology tools or CD SEM. There are various practices currently in use to accomplish the marking process, e.g.: by eye with a point and click GUI, by script using a list of known coordinates, by searching for a coordinate within a very limited neighborhood of a suspect coordinate, etc. However, all of these methods suffer from various shortcomings. They require extensive user intervention, or not

all or enough marking places are found, or the coordinates that are supposed to be known are slightly off and cause mark placement scripts to fail, and so on.

This paper details an approach using CATS MRCC-RPM, where a new pattern matching functionality is used to find locations suitable for mark placements. The location coordinates thus found are then passed to well known mark placing functionality to then place the marks.

Finding coordinates in a jobdeck to place marks is fundamental in MDP. Marks are placed on coordinates where a particular feature of interest needs to be measured. Therefore, every feature of interest needs to be somehow described. Given a description, locations in the jobdeck that fit the description need to be found, and a mark placed at each such coordinate.

In this approach, the way used to describe features of interest is by pattern definitions. A pattern consists of a description of figures, plus possible constraints such as distance ranges, boundary conditions, don't care regions, etc. Every feature of interest may be described by one or more such pattern definitions. Therefore, a feature of interest can be described by a set of patterns, also known as a pattern library, and the same is true of a group of features of interest.

The question then becomes: how can a pattern that describes a feature of interest be created? In a jobdeck, at least one location of a feature of interest is well known. Given the bounding box of one feature of interest, an exact pattern that describes it can be generated using CATS MRCC. Once an exact pattern is generated, range constraints can be added to describe possible variations of the pattern, if so required.

In such a way, a pattern library can be created, which is then passed to the CATS MRCC-RPM match algorithm, which in turn outputs all match locations, as well as match orientation, within the jobdeck. The match output is then fed to mark placement features to finally place the marks, giving full automation to mark placement.

8522-33, Session 8

Choosing the data flow paradigm for EUV mask process corrections

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When compared to conventional chrome absorber masks, electron beam patterning of EUV masks requires additional corrections to account for electron backscattering from the mirror and tantalum (Ta) based absorber layers. Current e-beam systems cannot correct for these additional backscattering effects with in-tool proximity effect correction (PEC) algorithms. Hence new methods of correction are needed, which require an implementation of the correction into the mask writer data prior to exposure.

Where these corrections should be performed in the data flow between mask user and mask supplier, and who should calibrate and maintain the corrections is not clear. We report on the attempt to calibrate a correction for EUV masks using actual CD data, and an e-beam backscattering model. The resulting Point Spread Function (PSF) is used to simulate and predict the measured CD data. Results show significant discrepancies between the scattering simulation and measured CDs, termed "process effects", as well as difficulties in calibrating this simulation experimentally, both of which lead to sources of error.

We present possible origins, magnitudes and variability of these error sources, along with other variations in this correction. We conclude by recommending an appropriate data flow for this simulation as well as correction calibration and maintenance responsibilities.

8522-34, Session 8

Bridging the gaps between aerial image inspection/review systems and actual ILT/SMO scanner performance using computational inspection and metrology technologies

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Computational techniques have been playing an increasingly important role in furthering resolution of optical lithography. Advanced Computational Lithography Technologies, such as Inverse Lithography Technology (ILT) and Source Mask Optimization (SMO), are enabling the printing of the most challenging layers, such as contact and metal, for the 20nm node and beyond.

In order to deploy SMO/ILT into production, improvements and upgrades of mask infrastructure are required, including mask writing, inspection, defect review, and repair. For example, AIMS(™) tools have often been used as the standard for assessing mask defect printability, because they emulate scanner optics and are able to produce a roughly linear correlation between aerial-image CD and wafer CD after resist develop. However, this correlation is far from linear in sub-32nm technology nodes, and is especially problematic for SMO/ILT masks used in 2X and lower nodes. This is partly because the current AIMS tool cannot accurately capture complex free-form illuminators and the resulting mask-3D effects. Another problem is the inherent non-linearity of the wafer resist and MEEF factors in specific geometries such as tight pitches, line-ends, etc.

Similar challenges are encountered during aerial-image based mask inspections. Aerial image based mask inspection is supposed to emulate aerial images of scanner, so "what you see on mask inspection is what you get on scanner"; however, similar challenges exist as for AIMS. First, inspection optics produce highly magnified images on CCD arrays, instead of 4:1 reduction images typical for scanners, so image contrast is significantly different, as indicated by standard vector optics. Second, it is difficult to replicate free form illuminators used with scanners, at least not in a timely fashion. Third, the resist effects are not considered.

In this paper, we will discuss these challenges in detail and present results from a newly developed suite of applications designed to bridge these gaps using Advanced Computational Lithography and Inspection Technologies.

First a uniform Computational Inspection and Metrology flow and frame are presented that work for imaging tools in inspection and metrology/review. Basically, the imaging tool's optics will be modeled mathematically. By solving the inverse problem, the mask pattern (including defects) will be recovered from its images. The images could be single or multiple, captured at different conditions, such as defocus, transmitted or reflected mode. After the mask pattern with the defect is recovered, a simulation using the scanner optics yields the aerial image. The real free-form source can be used, and a resist model can be applied to predict the printed pattern accurately.

This flow had been previously applied to high resolution mask inspection system in the Litho Plane Review (LPR). In this paper the application is expanded to AIMS - using AIMS to predict aerial images for free form sources. AIMS data collected under different sources will be presented to validate accuracy of the method.

8522-35, Session 8

Wafer stack impact on OPC/LMC models for 28nm and below

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At the 28 nm technology node and below optical proximity correction (OPC) needs to take in to account light scattering effects from prior layers. The impact of prior layers on the current layer lithography needs to be considered particularly when there is no anti-reflective coating present in the exposed resist areas, which is typical for implant layers.

A new model form has been developed by Brion to address the stack behavior during model calibration. This model can then be used in verification (using Tachyon LMC)and eventually during model based OPC to increase the accuracy of mask correction and verification.

This paper discusses an exploration of this new model form using extended customer measurements (including SEM). Data to date shows good correction and prediction on 1D structures, however there is still some room for improvement for 2D patterns which will be address in the next model generation.

8522-36, Session 8

The impact of the simulation model on SMO results

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Simultaneous source-mask optimization (SMO) has demonstrated significant improvements compared to sequential optimization schemes of the source and the mask, respectively. However, as long as the underlying simulation model does not realistically reflect the printing on wafer the predicted improvements might not be experimentally observable. It is even much more challenging than for classical OPC to prepare and to employ a predictive model for SMO because the model is required to conserve its predictive power not only under nominal conditions and for a given source but through process conditions and across variable source shapes. In this paper we investigate the impact of the simulation model on the SMO results. We compare different degrees of model rigor, ranging from a simple 2D aerial image model, blurred aerial images in 2D and 3D and a physical resist model including explicit simulations for the process steps of Post-Exposure-Bake and Development. By extending the approach described in Ref.1 for incorporating a rigorous simulation model into SMO, we study the impact of the simulation model on the resulting source shape. Additionally, we use the physical resist model as a reference simulation model to assess the potential loss of lithographic process stability due to the usage of simplified models within SMO.

Ref.1: T. Mülders et al., Source-mask optimization incorporating a physical resist model and manufacturability constraints, Proceedings of SPIE 8326, 83260G (2012)

8522-37, Session 8

Advanced module for model parameter extraction using global optimization and sensitivity analysis for electron-beam proximity effect correction

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In Electron Proximity Effect Correction, the quality of a correction is highly dependent on the quality of the model. Therefore it is of primary importance to have a reliable methodology to extract the parameters and assess the quality of a model. Among others the model describes how the energy of the electrons spreads out in the target material (via the Point Spread Function) as well as the influence of the resist process. There are different models available in the literature, as well as several different approaches to obtain the appropriate value for their parameters [1~4]. However, those techniques are usually limited for a certain PSF model, have some restriction in terms of complexity, or require a prohibitive number of measurements.

In this work, we propose a straightforward approach to obtain the value of parameters of a PSF. The methodology is general enough to be applied for more sophisticated models as well. It focused on improving the three steps of model calibration procedure: First, it is using a good set of calibration patterns. Secondly, it secures the optimization step and avoids to get attracted by a local optimum. And finally the developed method provides an improved analysis of the calibration step, which will allow quantifying the quality of model as well as enabling a comparison of different models. Figure 1 illustrates the schematics of one of the test calibration patterns were used in this development.

The use of sensitivity analysis techniques affords an optimal set for the calibration measurement. The most sensitive patterns are selected in order to get the lower uncertainty on the extracted model parameters. The quality of the fit is assured by a Efficient Global Optimization algorithm (EGO)[5]. This approach evade that the search may stall at a local optimum, enabling the parameters obtained for the PSF model do correspond to the global optimum. One of the original aspects of the proposed implementation of global optimizer is the use of a kriging meta-model[6].

The efficiency of suggested method is demonstrated using both simulation and experimental data on several substrate/resist stacks. Moreover, the impact of model quality on the quality of correction will be assessed. Figure 2 depicts the results obtained on a subset of the calibration patterns, which the one that shown in figure 1.

Besides providing the PSF parameter values, the proposed module also delivers two other reports, one indicating the sensitivity of each model parameter in relation to the measurements applied and other indicating the final overall quality of the fitting result. Both evaluations are based in algorithms of global sensitivity analysis[7~9]. Moreover, this result is able to use for evaluating the benefit of increasing the complexity of model, for example working with quadruple Gaussians distributions instead of triple one in PSF.

8522-38, Session 9

Zeta potential evaluation for enhancing sub-20nm node photomask cleaning
(Invited Paper)

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As semiconductor manufacturing advances to sub-20-nm nodes, the tiny particle specification (size < 50 nm) on photomasks is getting more and more stringent. Photomask cleanliness seriously impacts manufacturing cycle time and productivity. This is a serious challenge in the development of for sub-20-nm node mask cleaning process. Several cleaning processes, including chemical and physical forces, are widely used in mask cleaning. In this study, we focus on chemical force by zeta potential (ZP). The ZP indicates the degree of repulsion between the particles and mask surface (mostly quartz). In the nano-scale, stronger repulsion means the easier to remove the particle from mask surface. By controlling ZP of different chemicals from –10 mV to –150 mV in the cleaning process, the particles removal efficiency (PRE) is further improved about 10% especially for smaller-size particles. The ZP measurement methodology for different cleaning chemicals on quartz surface is also carried out. This index is helpful in evaluating the performance of new chemicals for mask cleaning. To enhance

photomask cleaning for sub-20-nm nodes, it's necessary to increase the chemical force because the physical force has been constrained by pattern damages. Moreover, the much smaller assistant feature will be used to gain more lithography process window such as negative tone developing (NTD) process. How to choose the suitable cleaning process for next generation mask making becomes very critical and important.

8522-39, Session 9

Effect of radiation exposure on the surface adhesion at Ru-capped MoSi multilayer blanks

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Although ruthenium is suitable for capping MoSi multilayer mirrors, its stability during different processing conditions poses challenges. The different types, wavelengths, and intensities of radiation used during application and characterization processes on ruthenium-capped MoSi multilayer blanks affect their surface defectivity and EUV reflectivity by altering their material composition, surface energy, surface morphology, and surface defect properties. Better understanding of the evolution of defects on the ruthenium surface throughout different processing steps, including exposure to radiation, is essential to successfully managing surface defects and improving the stability of ruthenium-capped MoSi multilayer blanks.

We have shown previously that the physical and chemical composition, surface defectivity, and EUV reflectivity of the ruthenium capping layer and first few bilayers of the multilayer exhibit changes under optical radiation exposure. Depending on the power and the wavelength of this radiation, the changes may either be thermal or chemical resulting in intermixing of the multilayers, formation of silicide, and modifications to the different oxide phases. Since these alterations occur close to the surface, the particle adhesion properties of ruthenium-capped MoSi multilayer blank surfaces are likewise affected.

This study investigates the effects of radiation on the surface adhesion properties of ruthenium-capped MoSi multilayer blanks. To this end, radiation exposure experiments were performed using optical and e-beam irradiation of the blank surfaces. The optical radiation wavelength was varied from UV to NIR, spanning a wide spectral range (λ= 13.5 nm, 173 nm, 266 nm, 532 nm, 1064 nm), while for electron irradiation, the incident e-beam energy and dose were varied. The effects of radiation exposure on particle adhesion, surface contact angle, surface defectivity, and EUV reflectivity changes after multiple cleaning cycles are presented.

8522-40, Session 9

The plasma etching methods for minimizing mask CD variation by cleaning process

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There has been a growing demand for more precise Mask CD MTT (critical dimension mean to target) control by shrinking the semiconductor device. Generally, The CD MTT is determined by patterning process. But, additional CD MTT variation often occurs by cleaning process after patterning process. As a result, it is important to preserve the CD MTT for minimizing CD variation by cleaning process. The cleaning process of photomask is becoming more critical for 32nm node and below because the size of defect and SRAF pattern is in the same range. In order to achieve high first cleaning pass yields, intensive cleaning method depending on media not physical force is still essential to photomask manufacturing and these cleaning process bring about considerable CD MTT change. Therefore, it is necessary to keep the durability of MoSi material by the new surface treatment method.

In this study, we presented the plasma etching technique for Cr strip etch in the 2nd process of the attenuated HTPSM for minimizing CD variation by cleaning process. Diverse dry etching processes are investigated to improve the durability of the MoSi patterns. In order to evaluate the surface modification of the MoSi film, surface compositions are analyzed by XPS (x-ray photoelectron spectroscopy). The variation of CD MTT and optical properties are also evaluated by CD SEM and n&k analyzer, respectively. The difference of CD shift between initial measurement and 2nd measurement after cleaning process depends on plasma etching methods. Consequently, the increase of MoO_3 that is less soluble than MoO_2 leads to preserve CD MTT by cleaning chemicals. We also evaluate the variation of CD and optical properties by the conditions of cleaning process after Cr strip etch in 2nd process. Finally, The CD variation is dramatically reduced through the combination of Cr strip etch and cleaning process.

8522-41, Session 9

Preparation of substrates for EUV blanks using an etch clean process to meet HVM challenges

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Achieving mask blanks with defectivity less than 0.03 defects/cm^2 at 30 nm SiO_2 equivalent and above is one of the key goals for accomplishing high volume manufacturing capability for EUV lithography. Defect free blanks for lithography start from defect free substrates. Currently, defects on both LTEM and quartz substrates are dominated by pits, scratches, particles and residues left by the polishing processes used to achieve the roughness and flatness specifications of the substrates. Normally, such defects are extremely difficult to be removed and particles often leave pits as they are removed by cleaning. Standard cleaning processes relying on megasonic cavitations for particle removal are insufficient for removing such defects from substrates. It is well known that hydrofluoric acid is an etchant of fused silica (quartz) and buffered HF in different concentrations has been used in the past for cleaning quartz and silicon substrates. Ideally, an etch clean process should not increase the roughness of the substrate while cleaning. However, in the process of etching and removing the defects, the roughness of the substrates is invariably increased which is undesirable. The rate of roughness change is directly dependent on the concentration and time of exposure, which also affects the etch rate and defect removal rate.

In this paper we report that a post polishing etch clean process has been developed for ULE and quartz substrates which meet the defectivity, roughness and flatness specifications for EUV blanks. We also examine the effects of substrate roughness on blank roughness, and inspection capability of substrates and blanks at different roughness levels using a defect inspection tool capable of inspecting defects down to 35 nm SiO_2 equivalent size. Defect smoothing using etch clean processes have been proposed and demonstrated in the past using an anisotropic etch mechanism. This study focuses on complete removal of defects from EUV substrates, and therefore smoothing is not an issue. Multilayer blank deposition process is known to decorate defects on substrates. We use this as a technique to identify any defects that might be left on the substrate surface after etch cleaning. In most cases, we find that the substrates have low defectivity and do not affect the EUV requirements. We demonstrate that the etch clean process can be used to increase the yield of high quality ULE substrates to meet the high volume production requirements of euv masks.

8522-43, Session 9

A new approach in dry technology for non-degrading optical and EUV mask cleaning

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Currently within the photomask industry, there are several challenges for

cleaning masks in order to meet the specifications for advanced node optical masks and Extreme Ultra Violet (EUV) technology. Growth of photo-induced carbon contamination on masks and EUV optics within the vacuum chamber of EUV exposure tools is one example. These are in addition to the conventional defects on optical and EUV masks that include organic and inorganic contamination from mask processing. For optical masks, the re-pelliclization process requires the removal of the pellicle adhesive track, which generally requires an aggressive wet clean that may drastically degrade the mask optical properties. Therefore, a more effective non-damaging combination of cleaning techniques is highly desirable for removal of organic and inorganic defects comprising particle contaminants, contamination adders from process tools, chemical residues, glue residue, carbon contamination, photoresist, haze defects, etc.

The Eco-Snow Systems group of RAVE N.P., Inc. has developed a new combined cleaning technique that satisfies the above-mentioned requirements: 1) it is a dry technique and does not require the aggressive wet chemistries that degrade the mask, 2) it operates at atmospheric pressure and therefore avoids expensive and complicated equipment associated with vacuum systems, 3) it utilizes ultra-clean reactants and does not deposit reaction byproduct adders, 4) it can be used locally for site specific cleaning without exposing the rest of the mask or can be used to clean the entire mask, 5) it is flexible and removes organic as well as inorganic particulates and film contaminations, and 6) it complements current techniques utilized for cleaning of advanced masks such as reduced chemistry wet cleans.

In this paper, we shall present examples demonstrating the capability of this technique for critical removal of carbon contamination as well as pellicle glue residues.

8522-61, Session 9

Controlling MegaSonic performance by optimizing cleaning media's physical and gaseous properties

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As the feature size of the mask shrinks, the feature becomes more fragile and the potential for physical force damage during cleaning increases. At the same time, increased feature density of the mask makes it difficult to remove particles from congested trenches without physical force cleaning. Acoustic energy has the ability to suppress the hydrodynamic boundary layer thereby transferring the physical force impact closer to particle trapped in the deep trenches of the mask. MegaSonic, which employs acoustic energy, is a preferred physical force cleaning technology for advanced masks. However MegaSonic can be extremely aggressive if the energy distribution is not contained within the narrowest process window available. In this paper, liquid media properties and its effect in controlling MegaSonic energy is evaluated. A chemistry is identified which provides favorable gaseous properties for controlling MegaSonic cavitation. The effect of this chemistry is characterized by measuring acoustic energy and Sonoluminscense. The phenomenon is further verified with pattern damage studies.

8522-44, Session 10

The significance of rigorous electromagnetic field simulation on mask development for 20nm optical lithography technology

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According to Moore's Law, the feature size of transistors is continuously shrinking. When the feature size is close to or smaller than the wavelength of 193 nm, the thick mask effects caused by the light scattering inside a mask stack become significant. Thus, for 20 nm optical lithography technology, the difference between a commonly-used thin mask electromagnetic field (EMF) calculation, well-known as the Kirchhoff approach, and experimental results can no longer be neglected. In order to explore the factors introduced by the mask stack, a rigorous EMF simulator has to be used; and unlike with the Kirchhoff approach, the physical parameters of the mask stack are also required to consider, including thickness, index of refraction, and the side wall profile.

A thinner mask stack is expected to reduce the thick mask effects, but the composition of the absorber must also be considered. Three different mask absorbers, which are referred to as mask A, B and C, are used to explore the impact of thickness on the lithography performance for 20 nm technology. The total stack thickness of mask A, B and C is approximately 50 nm, 50 nm and 70 nm, respectively. Each stack consists of different materials of absorber and anti-reflection coatings (ARC). Their thickness ratios are also varied. A Finite-Difference Time-Domain (FDTD) method is used as a rigorous simulator. Both 1D line/space and 2D contact patterns from 20 nm optical lithography are tested. Mask A and B are compared to investigate the effect of different indices of refraction, which contribute to the image log slope (ILS), mask error enhancement factor (MEEF), best focus (BF) shift and other lithographic data, directly affecting the process variation band (PV Band). Due to the large thickness, mask C demonstrates a change in the OPC EMF bias through various patterns, which is not easily worked out within thin the mask OPC recipe.

The mask side wall profiles could also have the potential to change the PV Band, which is not predictable using a thin mask calculation. The study of side wall angle effects starts with the calculation of a usual PV Band, including mask CD change, dose change and defocus. Light scattering inside the mask stack is calculated based on the side wall profile, and it is found that the phase of the light varies after propagation through the mask stack. This phenomenon results in the BF shift and leads to a CD impact caused by defocus. Besides the tradition PV Band, the mask side wall angle is a variable added into the process variation settings in this paper. The deviation of the new PV Band result from that of the traditional one shows a significant impact due to the side wall profile.

8522-45, Session 10

The new test pattern selection method for OPC model calibration, based on the process of clustering in a hybrid space

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Model-based Optical Proximity Correction (MB-OPC) is widely used in advanced lithography processes, particularly for the production of critical mask layers. The OPC model contains an empirical part, which must be calibrated using careful measurements of test patterns at the wafer level. As a result, the success of the entire OPC model largely depends on a precise test pattern selection method.

This paper focuses on how to automatically select the 'basis' geometries from a huge collection of test patterns. This refers to the selected patterns, which similarly represent the optical behavior of most non-selected patterns. The approach described in this paper employs an analysis of the sensitivities of image parameters in regard to changes in test pattern geometrical parameters. Consider test pattern M, and the corresponding biased pattern M+dM, the sensitivity is defined as (A(M+dM)-A(M))/dM, where A could be any of the following: a simulated critical dimension, an area enclosed by simulated contour, a contrast, an image slope, minimum/maximum intensity. These sensitivities are combined into one row of sensitivity matrix S, where the number of rows

equals P - the total number of test patterns. The normalized columns of matrix S span the sensitivity space.

Additionally to the sensitivity matrix S, we join the image parameter matrix IPS, which has P rows, and each row contains an image slope, and minimum/maximum intensities. The columns of the resulting block-diagonal matrix H = diag(S,IPS) span so-called hybrid space. The reason we add the image parameter space to the sensitivity space S, is to improve the robustness of subsequent empirical OPC model. Indeed, sometimes the collection of test patterns can be mapped into a significantly smaller sensitivity space, therefore to be sure that the selected geometries have enough variety in image parameters we add IPS.

Then, in order to select the representative patterns in the hybrid space we employ a centroid-based clustering method. The patterns that have similar sensitivities and at the same time similar image parameters are collected within one cluster. Then centroids of the clusters are chosen as representatives. The patterns that correspond to these representatives construct the pool of selected test patterns.

This approach is applied to an example system in order to investigate the minimum size of a sampling set, so that the resulting calibrated model has the error comparable to that of the model built with a lager sampling set. In addition, the proposed method selects the calibration patterns that produces a model with a lower prediction error compare to the conventional algorithm of image parameter space coverage. Moreover, in the presented method we calculate the image parameters only twice - for initial and biased test patterns, whereas in the other methods, that consider sensitivities of image parameters in regard to changes of model parameter, we need to calculate image parameters as many times as the number of model parameters.

8522-46, Session 10

OPC and verification for LELE double patterning

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LELE double patterning technology is being deployed for 20nm production. With the use of two separate litho-etch steps in the lithography of one layer, LELE doubles the pitch achievable in the traditional single litho-etch step.

However, as wavelength of the light used in each litho-etch step is as before, the need for OPC remains, and is even more critical. With LELE, new OPC requirements emerge — the need to ensure sufficient overlap and the need to prevent the bridging between between the mask images from the two separate litho-etch steps. These requirements necessitate the process of tandem OPC for the two masks, as each one needs to be informed of the correction that is being done to its twin. In this paper, we will present an overview of the tandem OPC, the mechanisms that allow communication between the two mask OPCs to maintain/achieve good overlaps/spacings where needed and still correcting for overall image quality, and the possibilities that are opened up by the nature of LELE in that LELE OPC has more freedom in recognizing that the fidelity aspect of the OPC problem is with respect to the final image of the layer.

With LELE, the need for OPC verification is even more prominent due to mask overlay errors which, while contained in a small radius, can be in an arbitrary direction. As a result of high frequency information loss during each litho-etch step, the image after each processing step is rounded. Such rounding increases the risk of pinching, and can introduce sharp angles which are susceptible to electro-migration.

In this paper, we will also present our approach which has the observation that when two points on a contour boundary are sufficiently far away from a mask stitching area the smallest possible distance between them can be computed with just a few shift directions — for points originating from the same mask, they are not susceptible to mask shift effect; for points from different masks the smallest possible distance is the distance between the points at the nominal mask positions minus the maximum possible shift value. Computation for the minimum possible distance between points lying inside mask stitching areas is much more complicated. But with these more complex computations contained within the stitching area and non-stitch area computation sped up by the aforementioned observation, a full-chip solution becomes practical.

In the end, our paper concludes with examples and experimental results.

8522-47, Session 10

Source mask target optimization flow

Clovis Alleaume, Emek Yesilada, Vincent Farys, STMicroelectronics (France)

It's been several technological nodes now that lithographers use the same 193nm wavelength in order to realize smaller and smaller features. In order to extend the lifetime of 193nm lithography, innovated techniques have been implemented. Source Mask Optimization is one of them, and consists in using a dedicated optical source associate with a specific layout in order to print aggressive features with a better patterning fidelity.

Retargeting is widely use during optical proximity correction to enlarge process window. Such retargeting is usually done trough geometrical rules, and is called rule based retargeting. Retargeting has a strong impact on the Source Mask Optimization technique, both on the source shape and the OPC result.

Traditional SMO flow uses a fixed lithography target. However, modifying this target during SMO flow adds another degree of optimization and can result in a different source that can provide better process window than traditional method. We developed therefore a model base retargeting within SMO flow in order to optimize the target iteratively along with the source.

In this paper, this new flow will be presented showing the impact of model based retargeting on SMO. Process window simulation along with 1D and 2D structures will be studied.

8522-48, Session 11

Photomask film degradation effects in the wafer fab: How to detect and monitor over time

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As a result of repeated cleanings and exposure effects such as chrome migration or MoSi oxidation some photomasks in the semiconductor fabs exhibit changes in critical dimension uniformity (CDU) over time. Detecting these effects in a timely manner allows for better risk management and process control in manufacturing. By monitoring changes in film reflectance intensity due to the various degradation mechanisms it is possible to predict when they may begin to influence across chip line width variations (ACLV). By accurately predicting the magnitude of these changes it is possible for semiconductor manufacturers to replace the photomasks before they have an impact on yields. This paper looks at changes in reflected intensity as a result of the degradation of the photomask film and how to monitor and map these changes as part of the normal reticle inspection process.

8522-49, Session 11

Reticle storage in mini-environment with extreme clean dry air

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Haze formation on the patterned metal surface of reticles is a known problem for IC manufacturers that can impact device yield and increase operational costs due to the need for more frequent cleaning of the reticles. Storage of reticles in an ultraclean environment can reduce haze formation and reduce operational costs.

We examined the contamination levels of a new type of reticle stocker that stores reticles in microenvironments which are continuously purged with extreme clean dry air (XCDA). Each microenvironment consists of twelve vertically stacked reticle storage slots which can be opened at any slot. The design of the microenvironment includes an XCDA supply that provides a homogeneous horizontal flow of XCDA between the reticles.

Figure 1. Reduction of contamination levels inside the storage microenvironment as a function of XCDA flow rate.

As shown in Fig. 1, continuous XCDA purge reduces the contaminant levels inside the microenvironment. The amount of reduction depends on the XCDA purge flow rate and the chemical species. Volatile organic substances can be reduced by more than two orders of magnitude. Humidity is reduced less because the plastic material of the storage microenvironment incorporates water in its matrix and can release moisture to the extremely dry atmosphere. Chemical filters applied to mini- or microenvironments typically reduce the contaminant levels only by 95-99% and do not reduce the humidity.

To pick and place reticles, the reticle storage microenvironment must be opened. The transient contaminant levels inside the empty microenvironment show an increase at the moment when the microenvironment is opened. Under the given conditions, the microenvironment returns to equilibrium levels with a time constant of 105 seconds (see Fig. 2). Similar dynamic response was measured for IPA and acetone.

Figure 2. Transient humidity when the storage microenvironment was opened for reticle handling.

The impact of handling on reticles stored inside the microenvironment was found to depend on several factors. When the microenvironment is filled with reticles, the horizontal XCDA flow purges a smaller volume of air and therefore re-establishes the equilibrium condition more quickly than in an empty microenvironment. The recovery time constant of a filled microenvironment was measured as only 20 seconds compared with 105 seconds for an empty microenvironment. Reticles below and above the opened slot were found to act as “shield” for the rest of the microenvironment and reduce the impact of opening the microenvironment. Moreover, the impact depends on the distance between the storage position and the opened slot: the larger the distance the smaller the impact. The last two factors

reduced the peak value in the transient humidity measurements to one third when the microenvironment was opened 5 slots away from the storage slot.

GLOBALFOUNDRIES Fab 1 used the results of these studies to optimize the parameter settings for its reticle storage. The reticles are stored in microenvironments which utilize extremely low contaminant levels. Based on the current utilization profile of the reticle stocker, the storage microenvironments are opened for approximately 0.01% of the time the reticles are stored in the stocker. Even in the short opening times the contamination levels do not exceed the ITRS requirements for reticle storage (see ITRS 2011, YE3 limits for reticle pod interior, supporting ≤28 nm technology nodes).

8522-50, Session 11

Haze management with aerial mask inspection: case study

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Haze monitoring is one of the main challenges in semiconductor manufacturing. In most cases the efficient way to manage haze in the fab is by means of mask inspection. In many cases the mask inspection is complemented by wafer inspection to compensate for mask inspection sample rate and possible mask inspection miss (e.g. defects at high MEEF locations). Although the use of mask inspection for haze monitoring is essentially a standard in the industry, the methodology differs between fabs. At one end are foundries where mask lifetime does not play a significant role and the cost of a printing defect is very high. At the other end are memory fabs where mask lifetime is a significant factor and the cost of a printing haze defect is less than in foundries. The logic fabs are somewhere in between. This paper we present a case study of haze monitoring by an Aerial mask inspection tool (Applied Materials Aera3) done at a memory fab. We describe the methodology characteristic of memory fabs and demonstrate the Aera3 early haze warning advantages on production data. These advantages include, simple tuning, fast TPT and printability assessment capability. Having these advantages, wafer print for the purpose of WI and printability assessment by SEM review can be avoided shortening the cycle time for decision and reducing costs.

At the end we’ll demonstrate on the data how the methodology would look like for different semiconductor manufacturing cost functions.

8522-51, Session 12

Proposal to extend the loading effect correction in EBM-8000

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Continuous shrinkage of the pattern size in semiconductor manufacturing demands further improvement of CD uniformity (CDU) for photomasks and mask writers. To satisfy demands on CDU by ITRS, we released last year the EB mask writer EBM-8000, designed for mask production of 22nm half-pitch generation and for mask development of 16nm half-pitch generation. Specification of EBM-8000 on local CDU is 1.3 nm for clear line’s three sigma.

Mask process for patterning, applied after writing photomasks, is one factor responsible for CDU. Loading effect occurs at resist development or etching light shielding layer, such as Cr or opaque MoSi film. This effect deviates CD depending on the position of the mask or pattern density, degrading global CDU.

Loading effect correction (LEC) can predict the CD change expected in subsequent mask processes, and compensate for that CD change from loading effect induced by the processes. Our EBM series are equipped with the LEC function using the dose modulation method, which modulates proximity effect correction (PEC) parameters, namely base dose and backscattering ratio, according to the required CD correction. This LEC method can change pattern size to compensate the loading CD bias and preserve the accuracy of PEC. Thus, LEC function can control pattern CD depending on global pattern density and the position on mask, while PEC is accurate at every position on the mask. This function is suitable for etch loading effect correction. Additional dose modulation can be applied by user-defined positional dose map to correct positional deviation of threshold dose for resist development.

As global CDU requirement gets tighter, it becomes more important to correct the secondary component of loading effect observable after LEC eliminates the primary component. In this paper, we propose a dose composition method to extend LEC function in EBM-8000, to realize a LEC function that can treat plural loading effects.

In our new design, the dose composition method can accept sets of LEC exposure dose. Each set of LEC exposure dose, needed to treat each loading effect, is calculated in the EBM using a corresponding set of parameters and positional maps supplied by the user. The calculated sets of LEC exposure dose is then performed a composition calculation, using uniquely-defined relation between amount of dose modulation and resultant CD change. Here, the relation is assumed to hold at every position on mask and not subjective to loading effect. Using this relation, sets of LEC dose maps are then converted to sets of LEC CD change maps for three local pattern densities, for instance, 0 %, 50 %,

and 100%. The sum of sets of LEC CD maps are obtained for each local pattern density to define a set of a base dose map and a back scattering ratio map used for writing.

We verified through simulations using the threshold dose model that our new method was sufficiently accurate. Composition of sets of LEC dose for development and etch loading was successful. This paper describes the model, the correction procedure, and possible applications of the method.

8522-52, Session 12

Printing results of a proof-of-concept 50keV electron multi-beam mask exposure tool (eMET POC)

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Printing results as achieved with a proof-of-concept 50keV electron multi-beam mask exposure tool (eMET POC) will be reported.

The eMET POC consists of a column with 200x reduction optics. Inserted into the column is a CMOS addressable (max. 12.8 Gbps) blanking device, providing 256k (k=1024) programmable beams within 82µm x 82µm beam array fields. Multi-beam exposures are done on 6" mask blanks moved at constant speed with a high precision (1nm 1sigma) laser-interferometer controlled stage in stripes of 82 µm width (2µm overlap between adjacent stripes).

Detailed evaluation results with respect to resolution, CDU, linearity, distortion control and stability, as well as OPC and ILT exposure capabilities will be presented.

8522-53, Session 12

Shape-dependent dose margin correction using model-based mask data preparation

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Dose Margin has always been known to be a critical factor in mask making. This paper describes why the issue is far more critical than ever before with the 20-nm logic node and beyond using ArF Immersion lithography. We present a solution to the problem, demonstrated by simulation and test printing results.

The mask shapes are increasingly complex and small. Width of sub-resolution assist feature (SRAFs) are well below 80-nm, and the shapes drawn on the masks are increasingly non-orthogonal. Both of these factors contribute to dose margin being shape dependent. Previously, when the desired contour on mask was axis-parallel, and therefore written with the edge of the variable shaped beam (VSB) electron beam shots, and when the shapes were over 100-nm in width, the dose margin was relatively constant across shapes. The dose margin issue therefore was mostly about controlling it across all shapes. Now, because the widths of the shapes are approaching the forward blur of the electron beam shots, and because the desired contour edge is not always written by a VSB edge, dose margin is significantly variable from shape to shape.

Model-Based Mask Data Preparation (MB-MDP) had been presented [references] to show shot count improvements for these complex masks. This paper describes MB-MDP improved the Dose margin. The improvement predicted with theoretical simulation with D2S is confirmed by the results of real mask written by JBX-3200 (JEOL) with HOYA.

8522-54, Session 12

Reflective electron-beam lithography performance for the 10nm logic node

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Maskless electron beam lithography can potentially extend semiconductor manufacturing to the 10 nm Logic (16 nm half pitch (HP)) technology node and beyond. KLA-Tencor is developing Reflective Electron Beam Lithography (REBL) targeting high-volume 10nm L (16 HP) production. This paper reviews progress in the development of the REBL system towards its goal of 100 wph throughput for High Volume Lithography (HVL) at these advanced nodes.

Previously, KLA-Tencor reported on the development of a Reflective Electron Beam Lithography (REBL) tool for maskless lithography at and below the 10 nm logic (16 nm HP) technology node. Since that time, the REBL team and its partners (TSMC, IMEC) have made good progress towards developing the REBL system and Digital Pattern Generator (DPG) for direct write lithography. Traditionally, e-beam direct write lithography has been too slow for most lithography applications. E-beam direct write lithography has been used for mask writing rather than wafer processing since the maximum blur requirements limit column beam current - which drives e-beam throughput. To print small features and a fine pitch with an e-beam tool requires a sacrifice in processing time unless one significantly increases the total number of beams on a single writing tool.

We will share concepts for position control during write time on a multi column e-beam system and a novel approach for reducing the minimum spot size to support the 10 nm L (16 HP) node overlay and resolution requirements. This paper will present simulation results as well as data obtained using a lithography demonstration platform.

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8522-55, Session 12

Future mask writers requirements for the sub-10nm node era

Mahesh Chandramouli, Nathan E. Wilcox, Andrew T. Sowers, Damon M. Cole, Frank E. Abboud, Intel Corp. (United States)

No Abstract Available

8522-56, Session 13

EUVL mask repair: expanding options with nanomachining *(Invited Paper)*

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Mask defectivity is often sited as a barrier to EUVL manufacturing, falling just behind low source power. Mask defectivity is a combination of intrinsic blank defects, defects introduced during the mask fabrication and defects introduced during the use of the mask in the EUV exposure tool. This paper works towards minimizing the printing impact of blank defects so that the final EUVL mask can achieve a lower defectivity. Multilayer defects can be created by a step or scratch as shallow as 1nm in the substrate. These small defects create coherent disruptions in the

multilayer that can generate significant variations in mask reflectivity and induce clearly-defined, printable defects. If the optical properties of the defect can be well understood, nanomachining repair processes can be deployed to fix these defects. The purpose of this work is to develop new nanomachining repair processes and approaches that can repair complex EUVL mask defects by targeted removal of the EUVL mask materials. The first phase of this work uses nanomachining to create artificial phase defects of different types and sizes for both printability evaluation and benchmarking with simulation. Once the printability of various nanomachined structures is understood, the second phase of the work aims to optimize the process to repair real EUVL mask defects with surrounding absorber patterns. Options for repairing random natural multilayer defects using nanomachining will be summarized.

8522-57, Session 13

E-beam based mask repair as door opener for defect free EUV masks

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For photomask production mask repair has become a fundamental part of the production process. The transition from 193 nm to EUV has dramatic challenges especially for performing successful mask repair. Since the EUV-photomask is used as mirror and no longer as transmissive device the severity of different defect types has changed significantly. Furthermore the EUV-photomask material stack is much more complex than the conventional 193nm photomask. As a consequence repair capability is required for defects in the absorber layer and for defects in the mirror. This expands the field of critical defect types even further and requires not only repair capability for smaller defects but also for new material stacks and multilayer defects.

One of the most promising concepts for EUV photomask defect repair is focused electron beam induced processing. This technology employs a high resolution electron beam to induce a local chemical reaction on the EUV mask surface. A suitable precursor gas is dispensed through a nozzle in close vicinity to the incident beam. Depending on the precursor chemistry, a reaction is induced by the electrons, leading to either a deposition caused by fragmentation of precursor molecules or to a reaction between the adsorbed molecules and the substrate material, resulting in volatile products and thus etching of the substrate material. The reaction is confined to the area exposed by the electron beam, so this technique allows high resolution nanostructuring.

From a repair point of view a EUV mask can be separated into 3 layers: The absorber, the capping layer and the multilayer. Different as for 193 nm photomasks defects can propagate through these layers, which makes the detection and the repair complex or impossible if conventional methods are used. In this presentation we will give a brief introduction into ebeam based mask repair. An overview of different defect types show that from a repair point of view all defects condense into two defect types. One is a defect in the absorber itself, which is almost impossible to repair if 193nm repair technology is applied because of parasitic degradation and collateral damage of the capping layer if 193nm repair technology is applied. The second type distorts the mirror quality which has two delicate implications. First the defect is almost invisible in SEM review and second the defects origin is below the complete stack which requires a complete new repair strategy.

In this presentation we will give an overview of key features of our e-beam based repair tool, discuss EUV repair requirements and demonstrate current repair performance. It will be demonstrated, by which methods the smooth multilayer defects can be visualized and located. Furthermore a new repair strategy will be introduced and demonstrated on real defects. The repairs will be verified by wafer prints.

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Applying computational inspection and metrology technologies to mask repair: post repair simulation (PRS)

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Computational techniques have been playing an increasingly important role in furthering resolution of optical lithography. Advanced Computational Lithography technologies, such as Inverse Lithography Technology (ILT) and Source Mask Optimization (SMO), are enabling the printing of the most challenging layers, such as contact and metal, for the 20nm node and beyond. Now such techniques are expanded into inspection and metrology with many new applications in mask houses and wafer fabs enabling process advancement, improving throughput of tools, and eliminating operator errors. One area of these applications is mask repair.

Mask patterns are becoming more complicated and less intuitive due to more aggressive OPC created by Computational Lithography techniques such as ILT and SMO. It is now more difficult for operators to know what the true mask patterns are supposed to look like and trying to find reference images on the mask can add extensive cycle time. This challenge is overcome by incorporating a Reference Pattern Generator (RPG) which automatically generates reference SEM images from the mask design GDS, as discussed in our prior publication [1]. The current mask repair flow also can involve looping through repair tool and AIMSTM review tool - repair tool repairs mask defect and then repaired defect is verified by AIMS to confirm the aerial image is within the spec. As the semiconductor industry marches down to smaller technology nodes, looping through these tools numerous times is occurring more and more often increasing cycle time and mask costs. Another difficulty is that repair success rate is not hundred percent, some defects repaired do not pass the AIMS check; therefore, have to be reloaded back onto repair tool to perform another round of repair. Adding more loops through the repair and AIMS check significant increases the turn-around and reduces the effective capacity of the entire repair area. Ideally, the mask should not be removed from repair tool until all defects are repaired successfully.

Post Repair Simulation (PRS) was developed to meet this goal. PRS takes the SEM image of the repaired site and then simulates the aerial image using the exact scanner optical and illumination conditions (including free form sources). If the CD on the aerial image does not meet spec, the defect has to be repaired again until it does. By doing so, the chance having a repaired defect not meeting the AIMS spec is dramatically reduced or eliminated. Therefore, the repair turn-around time is greatly reduced improving mask cycle time while effectively increasing the overall throughput of the repair and AIMS tools. Since the image obtained on the repair tool is a SEM image, it cannot be used in lithography simulation directly. There are many technical challenges that have to be overcome in order to make such a flow work.

In this paper, we will discuss these challenges in detail and present results demonstrating the accuracy and benefits of PRS. Results on both programmed defects and real defects from product masks will be presented. The repair cycle time changes and effective tool capacity gains before and after using PRS will also be shown.

Reference:

[1] Pang, L., et al, “Computational lithography and inspection (CLI) and its applications in mask inspection, metrology, review, and repair”, Proc. SPIE 7823, 78232H (2010)

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Computational defect review for actinic mask inspections

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ABSTRACT

As optical lithography continues to extend into low-k1 regime, resolution of mask patterns continues to diminish. The limitation of 1.35 NA posed by water-based lithography has led to the application of various resolution enhancement techniques (RET), for example, use of strong phase-shifting masks, aggressive OPC and sub-resolution assist features, customized illuminators, etc. The adoption of these RET techniques combined with the requirements to detect even smaller defects on masks due to increasing MEEF, poses considerable challenges for a mask inspection engineer. Inspecting masks under their actinic-aerial image conditions would detect defects that are more likely to print under those exposure conditions. However, this also makes reviewing such defects in their low-contrast aerial images very challenging. On the other hand, inspecting masks under higher resolution (HiRes) inspection optics would allow for better viewing of defects post-inspection. However, such inspections generally would also detect many more defects, including printable and nuisance, thereby making it difficult to judge which are of real concern for printability on wafer. Often, an inspection engineer may choose to use Aerial and/or HiRes inspection modes depending on the specific device-layer characteristics of the mask. Hence, a comprehensive approach is needed in handling defects both post-aerial and post-HiRes inspections.

In this paper, we propose the use of a novel computational approach to reviewing defects post actinic-inspections. For aerial-images, this involves first determining whether the defect is real or nuisance or false based on user-specified print CD error criteria. The defect print criteria can be different at different critical locations within the same image, enabled by use of Luminescent's image-based topology markers. Real and nuisance defects are then characterized based on their type and origin, for example, isolated pin-dot or pin-hole, extrusion or intrusion, assist-feature or dummy-fill defect, write-error or un-repairable defect, chrome-on-shifter or missing chrome-from-shifter defect, particle, etc. False defects are also characterized based on their origin, for example, those due to tool registration or image alignment, tap, CCD camera blemish, optical shimmer, focus, etc. issues. Visual or manual-operator classifications of these defects in the low-contrast aerial-images is error-prone, and very laborious and time-consuming.

For HiRes images, the same computational classification scheme is applied. The key difference here is that wafer printability of defects detected in HiRes mode is computed under Aerial-image conditions using Luminescent's Lithographic Plane Review (LPR) product. In this approach, HiRes images are first inverted to mask-plane where the defective and reference mask patterns are recovered from the inspection images, and then forward-simulated to appropriate aerial-image exposure conditions. The simulated aerial defect and reference images are analyzed in the same comprehensive scheme as aerial images from the inspection tool.

This computational approach to defect review post actinic mask-inspection is imperative to ensuring no yield losses due to errors in operator defect classification on one hand, and on the other, furthering the detection capability or sensitivity of the inspection platform itself not withstanding the number of defects detected in the process.

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