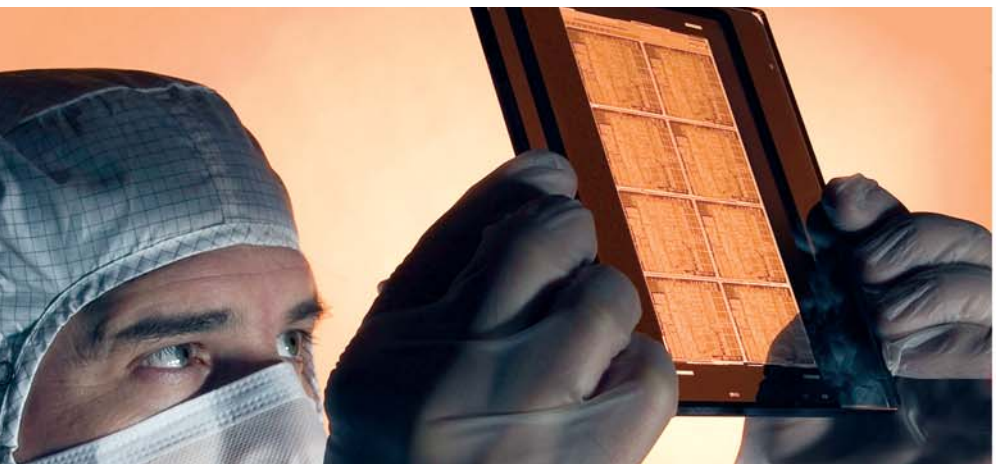
SPIE Photomask Technology

Technical Program

Conferences and Courses: 14 – 17 September 2009
Exhibition: 15 – 16 September 2009

Monterey Marriott and Monterey Conference Center
Monterey, California, USA



BACUS

The international technical group of SPIE dedicated to the advancement of photomask technology.

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Connecting minds. Advancing light.

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Welcome to Photomask 2009!

On behalf of the event sponsor, SPIE, BACUS, and the Program Committee, we would like to welcome you to "The 29th Annual SPIE/BACUS Photomask Symposium" — the premier worldwide technical conference and exhibition for the photomask industry. This year's conference will give you the chance to engage with the most up-to-date research on emerging and on-going issues facing the photomask industry in advanced lithography and their manufacturing and data solutions. New at this year's conference are four sessions related to nano-imprint and patterned media technology. This is a new growth opportunity for the photomask industry in the coming years with a new and different set of challenges.

The conference will open Tuesday morning with the keynote presentation given by Dr. Michael R. Polcari, the President and CEO of SEMATECH Inc., who will certainly have some significant industry insight, so you won't want to miss his keynote!

This year, the conference received over 140 abstracts. The conference will run Tuesday through Thursday morning, followed by the Special Session Thursday afternoon. Tuesday and Wednesday we will be running full parallel sessions.

On Tuesday and Wednesday the international exhibition will be open. Please stop in and see what's new from the folks that are really the backbone of the photomask industry. Without their active participation and support it would be very difficult to manufacture a photomask.

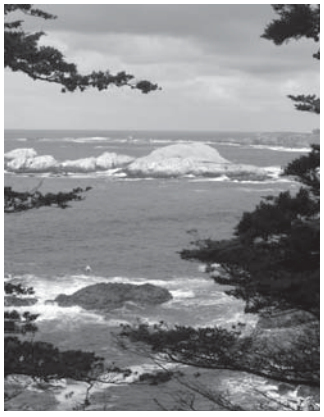
The conference will conclude Thursday, with the always popular Special Session as a timely one-stop overview of the key issues facing the industry. This year's special session will take a fresh look at "Commodity or Technology? Sub-20nm Mask Making at Yet another Crossroad." It will follow the previous years' format by addressing the hottest technical issues, development barriers, and potential roadblocks in the form of lively debate.

This should be another great week for exciting technical exchanges, many opportunities to meet with old colleagues and make new ones, fundamental and advanced courses from industry leaders, and the largest photomask exhibition in the world.

Welcome to beautiful Monterey on the ocean!

Larry S. Zurbrick
Agilent Technologies, Inc. (United States)
2009 Conference Chair

M. Warren Montgomery
College of NanoScale Science and Engineering (CNSE) and SEMATECH Inc. (United States)
2009 Conference Cochair



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Contents

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SPIE would like to express its deepest appreciation to the program chairs, conference chairs, cochairs, program committees, and session chairs who have so generously given of their time and advice to make this symposium possible. The symposium, like our other conferences and activities, would not be possible without the dedicated contribution of our participants and members.

This program is based on commitments received up to the time of publication and is subject to change without notice.

Left cover image: Courtesy of AMTC.

Keynote Presentation

Dr. Michael Polcari,
President and CEO,
SEMATECH Inc.

Global Collaboration in Semiconductors and Strategies for the Mask Industry

Room: Steinbeck Forum • Tuesday 8:10 to 8:50 am

Dr. Michael R. Polcari has served as SEMATECH's president and CEO since 2003. He is responsible for leading the consortium's advanced technology R&D programs in lithography, front end processes, interconnect, and metrology. Dr. Polcari has also overseen the launch of two SEMATECH subsidiaries—ATDF, as a leading R&D processing and prototyping center, and the International SEMATECH Manufacturing Initiative (ISMI), which has added seven members during his tenure.

Exhibition/Poster Reception

Monterey Conference Center, Serra Grand Ballroom

Tuesday 15 September . . . . . 6:30 to 8:00 pm

Poster Reception Beer/Wine Sponsored by

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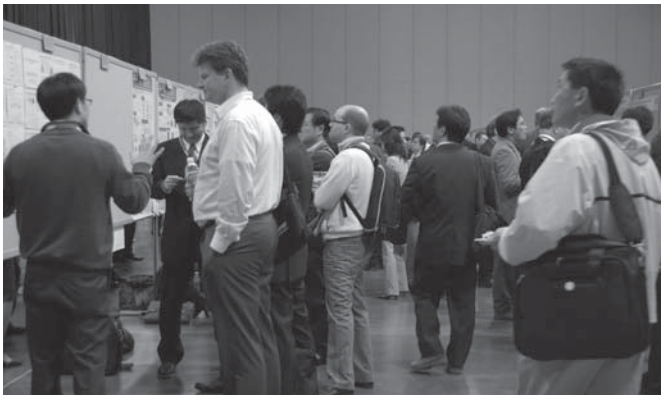
Symposium attendees and guests are invited to attend an Exhibition/Poster Reception on Tuesday evening in the Serra Grand Ballroom. The reception provides an opportunity for attendees to meet colleagues, network, view poster papers, and visit the exhibit booths. Refreshments will be served. Attendees are requested to wear their conference registration badges.



Poster Viewing

Monterey Conference Center, Serra Grand Ballroom

Tuesday 15 September . . . . . 6:30 to 8:00 pm
Wednesday 16 September . . . . . 10:00 am to 3:00 pm

Poster authors may set up their poster papers between 10:00 am and 4:00 pm on Tuesday and will leave them up until Wednesday afternoon. Authors will be present during the Poster Reception 6:30 to 8:00 pm Tuesday to answer questions and provide in-depth discussion regarding their papers. Any papers not removed by Wednesday at 3:00 pm will be considered unwanted and will be discarded. SPIE assumes no responsibility for papers left up after Wednesday at 3:00 pm.

Don't Miss the Photomask Reception

Wednesday 16 September
6:30 to 8:30 pm

San Carlos Ballroom
Marriott Hotel

Join your colleagues and friends at the annual Photomask Reception. This year's event focuses on good food, beverages, and plenty of time to socialize or talk business with fellow conference attendees. Awards and other presentations will be included in the evening.

Admission is included with your paid registration. Guest tickets may be purchased at the cashier (we highly recommend purchasing in advance to assure your reservation).

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Special Session on Commodity or Technology? Sub-20nm Mask Making at Yet Another Crossroad

Special Session and Lunch Sponsored by APPLIED MATERIALS®

Steinbeck Forum

Thursday 17 September, 1:10 to 4:30 pm

Panel Moderators: **M. Warren Montgomery,** College of NanoScale Science and Engineering (CNSE) and SEMATECH Inc.; **Wolfgang Staud,** Applied Materials, Inc.

Panelists include: **Bruno M. LaFontaine,** GLOBALFOUNDRIES Inc.; **Mark Wagner,** Applied Materials, Inc.; **Chiang Y. Yang,** Intel Corp.; **Franklin D. Kalk,** Toppan Photomasks, Inc.; **Greg P. Hughes**, SEMATECH North; **Brian J. Grenon,** Grenon Consulting Inc.; **Naoya Hayashi,** Dai Nippon Printing Co., Ltd. (Japan); **Thomas R. Albrecht,** Hitachi Global Storage Technologies, Inc.

The mask making industry once again finds itself torn between two very diverging technologies: for the first time in this conference we have a full day program of topics from the Patterned Media [Hard Disk Drive] Industry.

If maskshops want to participate in this growing market, it will require some very special tooling [rotary e-beams, optical and EB inspection, EB metrology, scatterometry, NIL, NIL coating, etch, deposition, and potentially CMP] - and all of this for a process that needs to be as cost sensitive as possible, since cost per disk is in the $1<$2 range. Not to mention the cost of change over for very special form factors.

On the other side are the almost urgent and heavy capital investment requirements for EUV tooling. Some of the same equipment, especially optical and EB inspection, blank and pattern inspection - actinic preferred, and the massive handling issues due to a non-existent pellicle.

As an alternate solution, NIL is also being investigated by IC manufacturers for a possible entry into the 1x nodes. Needless to say that SMO, ILT and DPT and SBPD are still the mainstay solutions, and also have their very specific requirements.

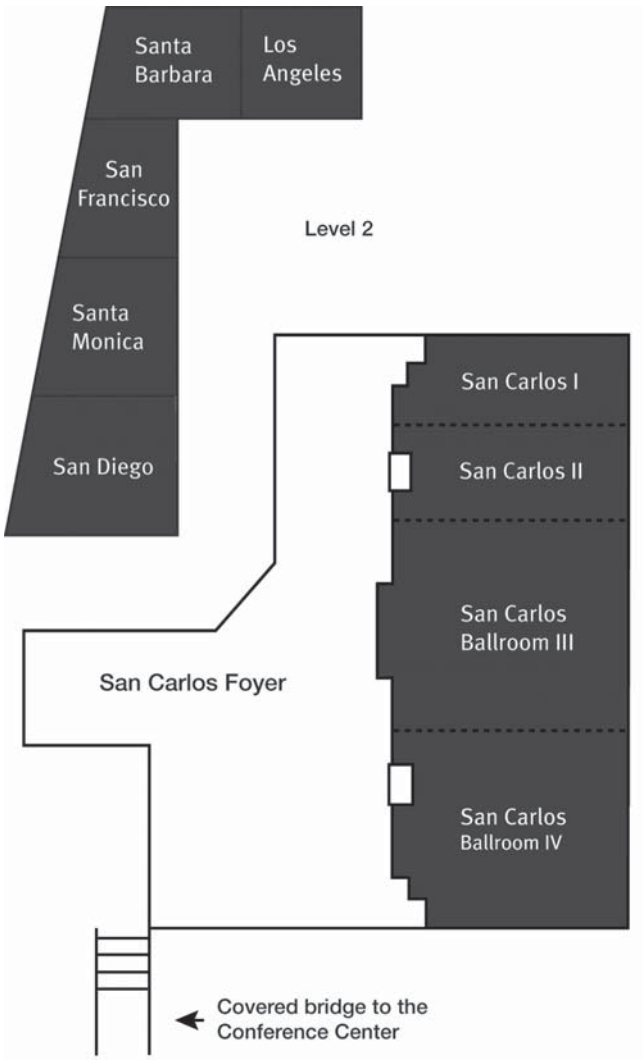
Captive mask shops face the challenge of having to gear up for both, or even all three, or stretch new or existing equipment across multiple technologies. Merchant shops, much the same, also need to decide to engage, and potentially set up dedicated production lines.

The various approaches are diametrically opposed. On one side is highest end users that can absorb the cost of advanced masks and EUV, on the other end extremely cost consciences commodity players, that need masks/templates on the fast and cheap, and can live with certain defect levels.

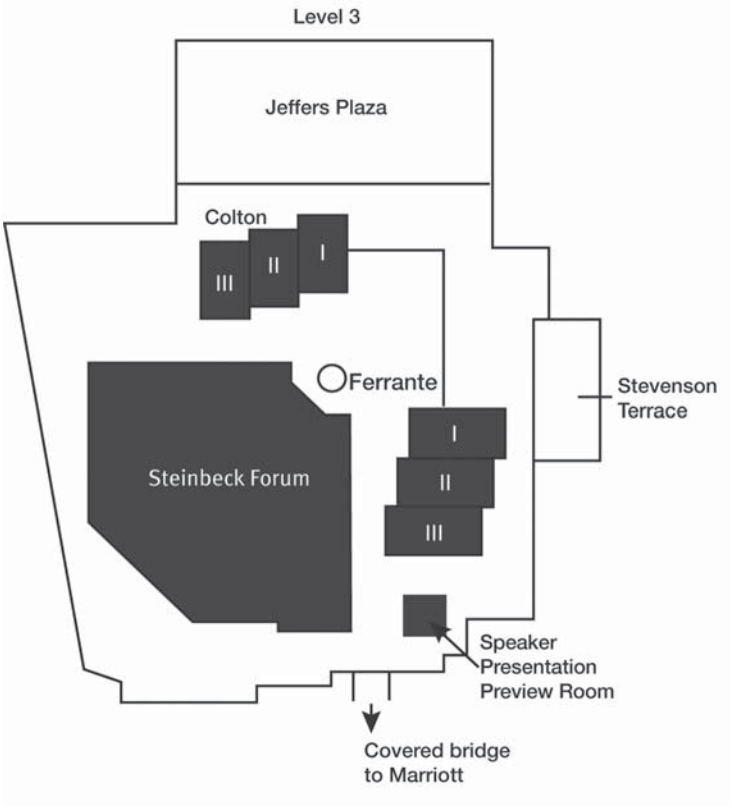
Your moderators, Warren and Wolf, will make an attempt to 'pitch' these two extremes against each other, and see which side the equipment suppliers will fall on. We are hoping for a very lively discussion, and will solicit questions and discussions from the audience [prior write-in questions allowed].

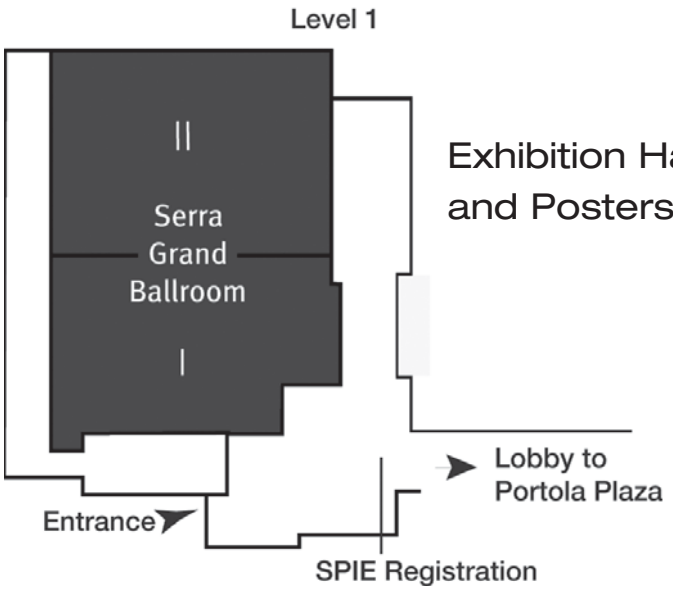
Floorplans

Marriott Floorplan



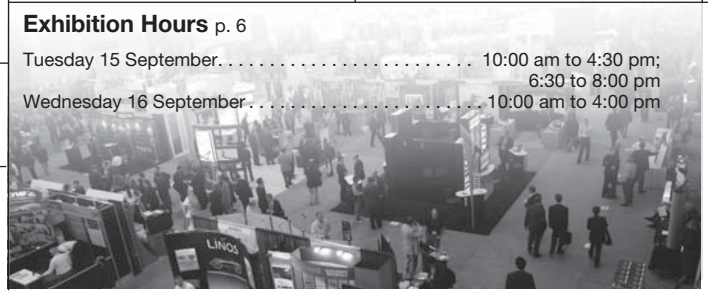
Monterey Conference Center Floorplan





Exhibition Hall and Posters

Monday 14 September	Tuesday 15 September	Wednesday 16 September	Thursday 17 September
Courses	**Conference**		
SC942 **Design-Technology CoOptimization to Combat Escalating Manufacturability and Design Challenges** *(Liebmann, Rovner)*, p. 18	**Photomask Technology Sessions** p. 11		
	Poster Viewing Hours 6:30 to 8:00 pm	10:00 am to 3:00 pm	**Special Session on Commodity or Technology? Sub-20nm Mask Making at Yet Another Crossroad**, 1:10 to 4:30 pm, p. 3
SC724 **Optical Lithography Extension: New Resolution Enhancement Techniques and Design for Manufacturing (***Pierrat)*, p. 18	**Exhibition/Poster Reception** *Serra Grand Ballroom* 6:30 to 8:00 pm, p. 3	**Photomask Reception** *Marriott Hotel, San Carlos Ballroom* 6:30 to 8:30 pm, p. 5	
SC579 **Photomask Fabrication and Technology Basics** (*Duff*), p. 18	**Exhibition Hours** p. 6 Tuesday 15 September . . . . . 10:00 am to 4:30 pm; 6:30 to 8:00 pm Wednesday 16 September . . . . . 10:00 am to 4:00 pm		



SPIE Photomask Technology

Exhibition Guide

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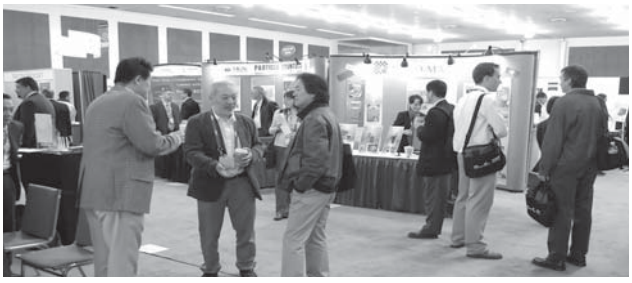
Make time for the Exhibition


Moving Technology to Market™

Exhibition: 15-16 September 2009
Monterey Conference Center, Serra Grand Ballroom
Monterey, California, USA

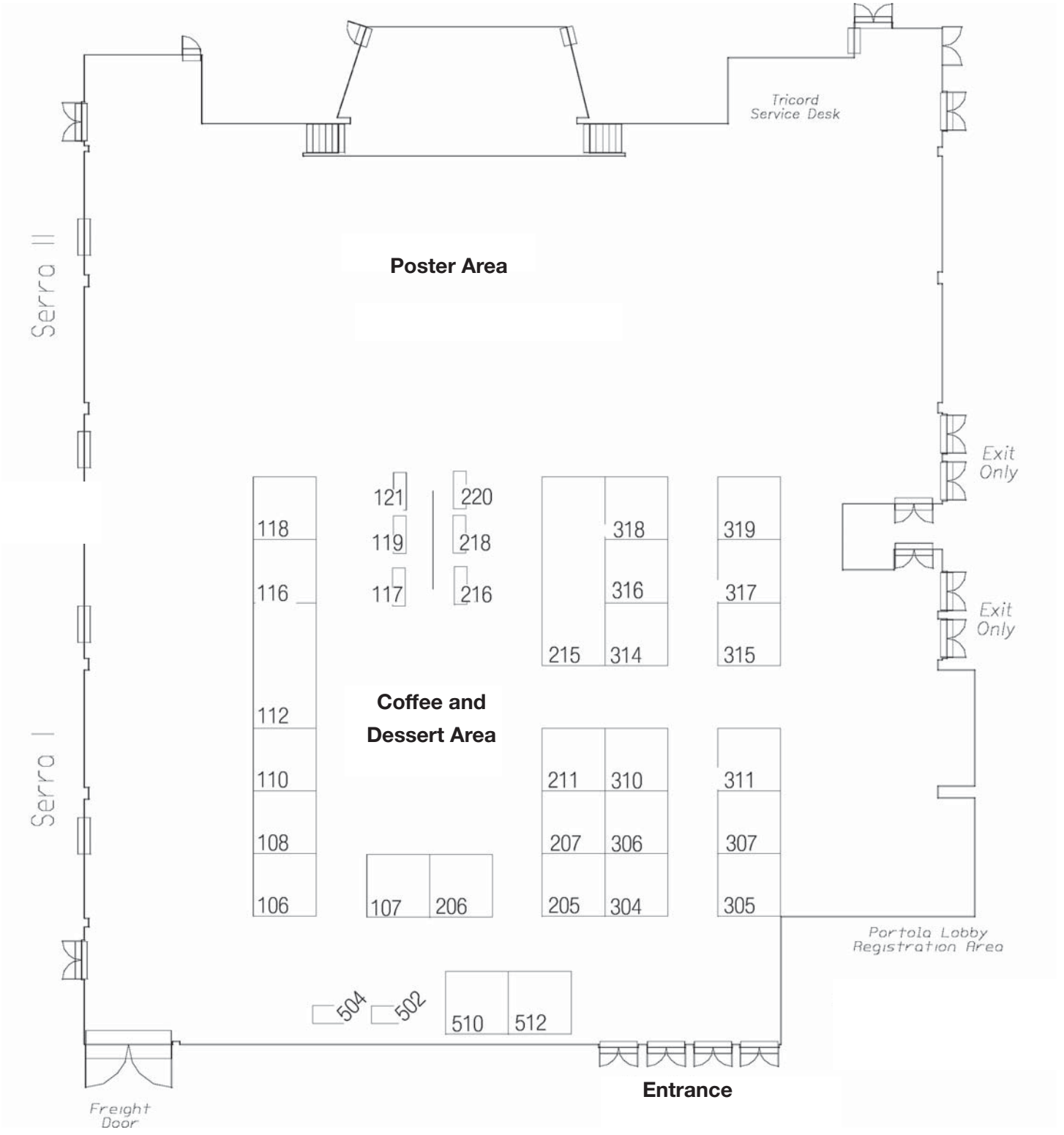
Tuesday 15 September . . . . . 10:00 am to 4:30 pm; 6:30 to 8:00 pm

Wednesday 16 September . . . . . .10:00 am to 4:00 pm

Exhibitor Listing *(as of August 14, 2009)*

Applied Materials. . . . . #215
Carl Zeiss SMT . . . . . #108
Corning Inc. . . . . #311
Gudeng Precision Industrial Co., Ltd. . . . . #306
Hitachi High Technologies America, Inc. . . . . #118
Inko Industrial Corp. . . . . #504
KLA-Tencor . . . . . #304
KM ACT Corporation. . . . . #314
Mentor Graphics . . . . . #211
Micro Lithography Inc. . . . . #116
Micronic Laser Systems AB. . . . . #512
Mitsui Chemicals America, Inc. . . . . #220
n&k Technology, Inc. . . . . #206
Nippon Control System Corp. . . . . #315
OMG-Cyantek . . . . . #216
Park Systems, Inc. . . . . #310
Plasma-Therm LLC . . . . . #205
Pozzetta Products, Inc. . . . . #112
Semiconductor International Magazine . . . . . #218
Shin-Etsu MicroSi, Inc. . . . . #305
Sigmameltec Ltd. . . . . #307
SII NanoTechnology . . . . . #207
SoftJin Technologies Private Ltd. . . . . #110
Solid State Technology . . . . . #502
Synopsys, Inc. . . . . #107
XEI Scientific, Inc. . . . . #119
XYALIS. . . . . #510

Serra Grand Ballroom



Thursday Lunch/Special Session Sponsor

Applied Materials #215

3050 Bowers Ave M/S 1901, Santa Clara , CA, 95054-3299
408/727-5555; fax 408/748-9943
www.appliedmaterials.com

Applied Materials, Inc. is the global leader in nanomanufacturing technology solutions with a broad portfolio of innovative equipment, service and software products for the fabrication of semiconductor chips, flat panel displays, solar photovoltaic cells, flexible electronics and energy efficient glass. At Applied Materials, we apply nanomanufacturing technology to improve the way people live.

Exhibition Hall Wi-Fi Sponsor

Carl Zeiss SMT #108

Carl Zeiss Promenade 10, Jena, Germany, 07745
49 3641 642563; fax 49 3641 642938
info-sms@smt.zeiss.com; www.smt.zeiss.com

New Product: Next Generation AIMS offering advanced repair verification for all litho techniques at 32nm node.

Carl Zeiss SMT is a leading global supplier of both metrology and manufacturing equipment for the semiconductor industry. Core expertise in light and electron optics, complemented by a revolutionary femto-second laser technology form the foundation of a product portfolio comprising metrology, qualification, repair/tuning and monitoring of lithographic photomasks. Our advanced mask solutions empower our customers to develop and manufacture zero defect photomasks realizing highest yields. Contact: Jim Polcyn, Director Sales US/SMS Products, polcyn@smt.zeiss.com; Nadine Schuetze, Marketing Manager, n.schuetze@smt.zeiss.com.

Corning Inc. #311

SPIE Corporate Member

1 Riverfront Plz, Corning, NY, 14831
607/974-9000; fax 607/974-8177
dayjl@corning.com; www.corning.com

New Product: The Tropel® UltraFlat™ 200 measures surface flatness of photomasks with six nanometer uncertainty.

Corning Tropel is a leading manufacturer of non-contact metrology instrumentation designed specifically for the photomask industry. These products measure photomasks and photoblanks at every stage of the manufacturing process, including, substrate polishing, coating, patterning and the mounting of pellicles. Stress software can compare pre and post processing measurement data to analyze the effects of film stress and other mechanically induced deformation. Contact: Chris Lee, Product Manager, leeca@corning.com; Susan Fabi, Commercial Manager, fabise@corning.com.

Gudeng Precision Industrial Co., Ltd. #306

SPIE Corporate Member

No 428 Bade St, Shulin City, Taipei, Taiwan, 23857
886 2 2680 0980; fax 886 2 2680 0960
sales@gudeng.com; www.gudeng.com

Founded in 1998, Gudeng Precision Industrial Co., Ltd. assists clients to enhance its yields and reduce cost after transfer to semiconductor front-end manufacture equipment technology. Our products are mask pick, mask case, wafer cassette, Reticle SMIF pod, mask cleaner, CDA/ N2 Purge Station & cabinet and mask cleaning services. Also Gudeng provides the usage of ultra clean mask shipping/ store/ cleaning equip by Lithography manufacture under 90 nm. Any questions, contact Parson Hsieh parsonhsieh@gudeng.com

Hitachi High Technologies America, Inc. #118

SPIE Corporate Member

5100 Franklin Dr, Pleasanton, CA, 94588
925/218-2800; fax 925/218-3230
www.hitachi-hta.com

Hitachi High Technologies Corporation introduces advanced metrology systems for photomasks: CG4500 enabling the high-precision measurement of next generation photomask; Design Gauge enabling various effective measurement functionalities based on design data. Contact: Lorena Page, Applications Department Manager, lorena.page@hitachi-hta.com.

Inko Industrial Corp. #504

695 Vaqueros Ave, Sunnyvale, CA, 94085
408/830-1041 ; fax 408/830-1058
sales@pellicle-inko.com; www.pellicle-inko.com

New Product: ArF 193nm DUV pellicle with minimized outgas.

INKO, a U.S. based pellicle manufacturer, with a complete line of pellicles for applications ranging from ASIC designs to high volume memory production. We make pellicles for broadband to I/G line to 248nm KrF and 193nm Arf DUV lithography. Contact: Joe Mac, Sales and Customer Services, joemac@pellicle-inko.com; Sherry Chi, Marketing, sherry@pellicle-inko.com.

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KLA-Tencor #304

SPIE Corporate Member

1 Technology Dr, Milpitas, CA, 95035
408/875-3000
info@kla-tencor.com; www.kla-tencor.com

KLA-Tencor Corporation (NASDAQ: KLAC) is a leading provider of process control and yield management solutions, including reticle inspection and metrology equipment. Additional information may be found at www.kla-tencor.com.

KM ACT Corporation #314

2340 W Braker Ln Ste A, Austin , TX, 78758
512/490-6554; fax 512/490-6558
chegeman@km-usa.com; www.woojinact.com

Lanyards/Tuesday Morning Coffee Break Sponsor

Mentor Graphics #211

SPIE Corporate Member

8005 SW Boeckman Rd, Wilsonville, OR, 97070-7777
503/685-7000; fax 503/685-1543
www.mentor.com

Mentor Graphics is a world leader in EDA and IC manufacturing software. The Calibre product line provides flexible, comprehensive solutions for computational lithography and mask data preparation. Mentor OPC products offer dense simulation with co-processor acceleration using the Cell Broadband Engine™ for unprecedented accuracy, speed and low cost of ownership. Calibre also models lithographic process variability in devices and interconnects, enabling layout enhancements to ensure higher yield. Contact: Steffen Schulze, MDP Product Marketing Director, steffen_schulze@mentor.com.

General Refreshment Sponsor

Micro Lithography Inc. #116

1257 Elko Dr, Sunnyvale, CA, 94089-2211
408/747-1769; fax 408/747-1978
www.mliusa.com

New Product: New ArF-193nm pellicle for high NA 32nm lithography is available.

MLI is featuring pellicles formulated to yield high rates of transmission and long lifetimes for UV exposure. Our complete line of pellicle films ranges from broadband, g-/i-line to DUV (KrF-248nm and ArF-193nm). MLI's DUV pellicles have the lowest outgassing materials available in the market today. Contact: Diana Tjin, Sales Administrative Manager, diana.tjin@mliusa.com.

Micronic Laser Systems AB #512

Box 3141, Taby, Sweden, 183 03
46 8638 5200; fax 46 8638 5290
info@micronic.se; www.micronic.se

Micronic Laser Systems AB is a Swedish technology company providing laser pattern generators for the production of photomasks. Micronic's systems are used by the world's leading electronics companies in the manufacture of television and computer displays, semiconductor circuits and semiconductor packaging components. Contact: info@micronic.se.

Mitsui Chemicals America, Inc. #220

2099 Gateway Pl Ste 260, San Jose, CA, 95110
408/487-22891; fax 408/453-0684
www.mitsuichemicals.com

Since 1986, Mitsui has been the leader in providing pellicles to the semiconductor industry. ISO 9001 certified full-automated plant produces Mitsui Pellicle with more than 99% of transmission, excellent uniformity and superb longevity. The non-dust structure based on 17 years accumulated expertise and rigorous selection of the materials contributes to maximum production yields at your fab. by eliminating pellicle related particle generations. Contact: Masanari Kitajima, General Manager m.kitajima@mitsuichem.com.

n&k Technology, Inc. #206

80 Las Colinas Lane, San Jose, CA, 95119
408/513-3800; fax 408/513-3850
sales@nandk.com; www.nandk.com

n&k Technology, Inc., of San Jose, California, manufactures advanced metrology tools for semiconductor, photomask, flat panel display. The company's high resolution optical metrology systems are used for film thickness, n and k, phase shift, trench depth, CD and profile measurements. n&k Technology systems, ranging from table-top to fully automated, are field-proven, production-worthy, fast, accurate, and non-destructive. Contact: Allan Deyto, Regional Account Manager, adeyto@nandk.com.

Nippon Control System Corp. #315

150 Mathilda Pl Ste 204, Sunnyvale, CA, 94086
408/737-0338
ncs-patacon@nippon-control-system.co.jp;
www.nippon-control-system.co.jp

New Product: NDE is now officially available. NDE is next generation MDP system from NCS.

Nippon Control System is a software company which has provided MDP system called PATACON for 20 years. The headquarters is in Japan. There is also a local branch office in the US. Contact: Shu Ohara, US Branch Manager, oohara@nippon-control-system.co.jp.

OMG-Cyantek #216

SPIE Corporate Member

3055 Osgood Ct, Fremont, CA, 94539
510/651-3341; fax 510/651-3398
www.cyantek.com

OMG - Cyantek is the leading supplier to photo mask manufactures around the globe. We provide a full line of developers, metal etchants, organic and aqueous based resist strippers, specialty cleaners and customized blends for mask manufacturing technologies. Our products are used on chrome, iron oxide and silicon dioxide, along with other specialized substrates. Other electronic technologies such as FPD, IC and thin film processes also utilize many of our products in their critical processes. Contact: Dale Deg, Sales & Marketing Manager, dale.deg@omgi.com.

Park Systems, Inc. #310

3010 Olcott St, Santa Clara, CA, 95054
408/986-1110; fax 408/986-1199
info@parkafm.com; www.parkafm.com

Park Systems serves its customers with a complete range of Atomic Force Microscopes (AFM) solutions for the most demanding imaging and measurements needs in research and industry. Park Systems' AFM solutions are derived from our continuous innovation in AFM technology over 20 years, combined with our strength to form a successful partnership with customers. Contact: Sung Park, VP of Sales & GM, sung@parkafm.com; Albert Wang, Director of Technical Sales, albert@parkafm.com.

Plasma-Therm LLC #205

10050 16th St N, St. Petersburg, FL, 33716
727/577-4999
www.plasmatherm.com

New Product: Mask Etcher V is Plasma-Therm's latest equipment for advanced Photomask etching at 32nm and below.

Plasma-Therm LLC., designs, manufactures, sells and supports plasma etch and plasma enhanced chemical vapor deposition (PECVD) equipment to semiconductor device manufacturers. These systems are used in applications ranging from leading edge R&D to high volume production. Our served markets include Photomask Etching, Wireless communication, MEMS, Nanotechnology, Data Storage, Solar Cells and LED/Photonics Processing. Contact: Emmanuel Rausa, Director-Technical Marketing, emmanuel.rausa@plasmatherm.com; Edward Ostan, Exec VP Sales and Marketing, ed.ostan@plasmatherm.com.

Pozzetta Products, Inc. #112

3121 S Platte River Dr, Englewood, CO, 80110
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artemis@pozzetta.com; www.pozzetta.com

Companies around the world trust Pozzetta to create secure environments for the handling, storage, and transport of photomasks, reticles, and wafers. Pozzetta will protect your valuable products from particles, ESD damage, outgassed components, and high costs. Contact: Artemis Vasiliades, Account Executive, artemis@pozzetta.com.

Promotional Partner

Semiconductor International Magazine #218

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Semiconductor International is the world's leading trade publication serving the semiconductor manufacturing industry. The print and digital editions reach over 37,000 qualified buyers of semiconductor manufacturing equipment and materials around the world, more than any other publication in the industry. Additional products include Semiconductor Packaging, Online Buyers Guide, SI Product Showcase, SI Japan, SI China, e-newsletters and the industry's leading website, www.semiconductor.net. Contact: Laura Peters, Editor-in-Chief, lpeters@reedbusiness.com.

Shin-Etsu MicroSi, Inc. #305

10028 S 51st St, Phoenix, AZ, 85044-5203
480/893-8898; fax 408/893-8637
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Shin-Etsu, the world's No. 1 supplier of semiconductor silicon wafers and a leading supplier of essential electronic materials. Shin-Etsu's product portfolio includes, photomask blanks, EB resists, pellicles, synthetic quartz, semiconductor advanced resists along with numerous specialized thermal interface materials. Contact: Edwin Nichols, Marketing Manager, enichols@microsi.com; info@microsi.com.

Sigmameltec Ltd. #307

SPIE Corporate Member

3-37-7 Shimoasao Asao-ku, Kawasaki, Japan, 215-0022
81 44 987 9381; fax 81 44 987 1417

New Product: Introducing the MRC8000 Final Clean and Resist Strip System designed for cleaning 22nm photomasks.

For over 30 years, Sigmameltec has been providing its photomask customers with cutting edge toolsets for the production of the most advanced masks. Specializing in customized mask processing tools, Sigmameltec is the global leader in wet processing for the mask industry. Contact: Mike McAvoy, General Manager - International Sales, mike.mcavoy@sigmameltec.com.

SII NanoTechnology #207

RBM Tsukiji Bldg, Shintomi 2-15-5 Chuo-ku, Tokyo, Japan, 104-0041
408/497-4498
www.siint.com

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2900 Gordon Ave Ste 100-11, Santa Clara, CA, 95051
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Conference 7488

Tuesday-Thursday 15-17 September 2009 • Proceedings of SPIE Vol. 7488

Photomask Technology

Conference Chair: **Larry S. Zurbrick,** Agilent Technologies, Inc.

Conference Co-Chair: **M. Warren Montgomery,** College of NanoScale Science and Engineering (CNSE) and SEMATECH Inc.

Program Committee: **Frank Abboud,** Intel Corp.; **Kiho Baik,** Luminescent Technologies, Inc.; **Artur P. Balasinski,** Cypress Semiconductor Corp.; **Uwe F.W. Behringer,** UBC Microelectronics (Germany); **Ronald R. Bozak,** RAVE LLC; **William H. Broadbent,** KLA-Tencor Corp.; **Peter D. Buck,** Toppan Photomasks, Inc.; **Han-Ku Cho,** SAMSUNG Electronics Co., Ltd. (Korea, Republic of); **Frank A. Driessen,** Takumi Technology B.V. (Netherlands); **Roxann L. Engelstad,** Univ. of Wisconsin, Madison; **Emily E. Gallagher,** IBM Corp.; **Brian J. Grenon,** Grenon Consulting, Inc.; **Naoya Hayashi,** Dai Nippon Printing Co., Ltd. (Japan); **Mark T. Jee,** HOYA Corp. USA; **Rik M. Jonckheere,** IMEC (Belgium); **Bryan S. Kasprowicz,** Photronics, Inc.; **Kurt R. Kimmel,** Advanced Mask Technology Ctr. GmbH & Co. KG (Germany); **Chin-Hsiang Lin,** Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); **Wilhelm Maurer,** Infineon Technologies AG (Germany); **Thomas H. Newman,** Micronic Laser Systems Inc.; **Hiroshi Nozue,** NuFlare Technology, Inc. (Japan); **James E. Potzick,** National Institute of Standards and Technology; **Emmanuel Rausa,** Plasma-Therm LLC; **Frank M. Schellenberg,** Mentor Graphics Corp.; **Thomas Scherübl,** Carl Zeiss SMS GmbH (Germany); **Robert J. Socha,** ASML MaskTools Inc.; **Christopher A. Spence,** GLOBALFOUNDRIES Inc.; **Wolfgang Staud,** Applied Materials, Inc.; **Jacek K. Tyminski,** Nikon Precision Inc.; **J. Tracy Weed,** Synopsys, Inc.; **John M. Whittey,** KLA-Tencor Corp.

Tuesday 15 September

Room: Steinbeck Forum . . . . . Tues. 8:00 to 8:10 am

Opening Remarks

Session Chairs: **Larry S. Zurbrick,** Agilent Technologies, Inc.; **M. Warren Montgomery,** College of NanoScale Science and Engineering (CNSE) and SEMATECH Inc.

SESSION 1

Room: Steinbeck Forum . . . . . Tues. 8:10 to 10:10 am

Invited Session

Session Chairs: **Larry S. Zurbrick,** Agilent Technologies, Inc.; **M. Warren Montgomery,** College of NanoScale Science and Engineering (CNSE) and SEMATECH Inc.

8:10 am: **Global Collaboration in Semiconductors and Strategies for the Mask Industry (Keynote Presentation)** *(Presentation Only)*, Michael R. Polcari, SEMATECH Inc. (United States) . . . . . [7488-01]

8:50 am: **Mask Industry Assessment: 2009**, Gregory P. Hughes, Henry K. Yun, SEMATECH North (United States) . . . . . [7488-02]

9:10 am: **EMLC09 Best Paper: MAPPER: high-throughput maskless lithography** *(Presentation Only)*, V. Kuiper, Bert J. Kampherbeek, Marek Wieland, Guido de Boer, Gerard F. ten Berge, J. Boers, Remco J. A. Jager, Ton van de Peut, Jerry J. M. Peijster, Erwin Slot, Stijn W. H. K. Steenbrink, Tijs F. Teepen, Alexander van Veen, MAPPER Lithography (Netherlands) . . . . . [7488-03]

9:30 am: **JPM09 Panel Overview**, Kokoro Kato, Seiko Instruments Inc. (Japan) . . . . . [7488-04]

9:50 am: **JPM09 Best Paper: Comparison of lithographic performance between MoSi binary mask and MoSi attenuated PSM** *(Presentation Only)*, Mitsuharu Yamana, Toppan Printing Co., Ltd. (Japan); Matt J. Lamantia, Toppan Photomasks, Inc. (United States); Tatsuya Nagatomo, Yoji Tonooka, Toppan Printing Co., Ltd. (Japan) . . . . . [7488-05]

Coffee Break . . . . . 10:10 to 10:40 am

Tuesday 15 September *(continued)*

Sessions 2-3-4 run concurrently with sessions 5-6-7-8.

SESSION 2

Room: Steinbeck Forum . . . . . .Tues. 10:40 am to 12:20 pm

Defect Inspection and Disposition

Session Chairs: **William H. Broadbent,** KLA-Tencor Corp.; **Wolfgang Staud,** Applied Materials, Inc.

10:40 am: **SMO photomask inspection in the lithographic plane**, Emily E. Gallagher, Karen D. Badger, IBM Corp. (United States); Yutaka Kodera, Toppan Photomasks, Inc. (United States); Jaione Tirapu-Azpiroz, Kafai Lai, Scott D. Halle, Gregory R. McIntyre, IBM Corp. (United States); Mark J. Wihl, Shaoyun Chen, Ge Cong, Ann Wieczorek, Aditya Dayal, KLA-Tencor Corp. (United States) . . . . . [7488-06]

11:00 am: **Field results from die-to-model application for mask inspection**, Jun Kim, Intel Corp. (United States); Lev Faivishevsky, Shmoolik Mangan, Applied Materials (Israel); Wei-Guo Lei, Joan McCall, Suheil Zaatri, Michael Penn, Rajesh Nagpal, Intel Corp. (United States) . . . . . [7488-07]

11:20 am: **Mask defect auto-disposition using aerial image-based analyzer**, Jin-Hyung Park, Wonil Cho, Wook Chang, Dong-Hoon Chung, Chan Uk Jeon, Han-ku Cho, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Vikram L. Tolani, Luminescent Technologies, Inc. (United States) . . . [7488-08]

11:40 am: **Defect printability analysis by lithographic simulation from high-resolution mask images**, Guangqing Chen, Brion Technologies, Inc. (United States) . . . . . [7488-09]

12:00 pm: **Printability verification function of mask inspection system**, Hideo Tsuchiya, Masaki Yamabe, Masakazu Tokita, Kenichi Takahara, Association of Super-Advanced Electronics Technologies (Japan); Kinya Usuda, NuFlare Technology, Inc. (Japan); Fumio Ozaki, Nobutaka Kikuiri, Advanced Mask Inspection Technology, Inc. (Japan) . . . . . [7488-104]

Lunch/Exhibition Break . . . . . 12:20 to 1:40 pm

SESSION 3

Room: Steinbeck Forum . . . . . .Tues. 1:40 to 3:40 pm

Defect Inspection and Repair

Session Chairs: **John M. Whittey,** KLA-Tencor Corp.; **Ronald R. Bozak,** RAVE LLC

1:40 pm: **Using metrology capabilities of mask inspection equipment for optimizing total lithography performance**, Shuichi Tamamushi, Noriyuki Takamatsu, NuFlare Technology, Inc. (Japan) . . . . . [7488-11]

2:00 pm: **High-MEEF reticle inspection strategy**, Anna Tchikoulaeva, AMD Saxony LLC & Co. KG (Germany); Remo Kirsch, AMD Fab36 LLC & Co. KG (Germany); Stephanie Winkelmeier, Advanced Mask Technology Ctr. GmbH & Co. KG (Germany) . . . . . [7488-12]

2:20 pm: **New database mode inspection capabilities for advanced reticles**, Arosha W. Goonesekera, Phillip Lim, Bo Mu, Aditya Dayal, KLA-Tencor Corp. (United States) . . . . . [7488-13]

2:40 pm: **Simulation-based mask defect repair verification and disposition**, Eric G. C. Guo, Cathy Liu, Skin Zhang, Sandy Qian, Semiconductor Manufacturing International Corp. (China); Guojie Cheng, Liang Zhou, Ling Li, Anchor Semiconductor, Inc. (China); Ye Chen, Ching-Yun Hsiang, Anchor Semiconductor, Inc. (United States); Gary Zhang, Anchor Semiconductor, Inc. (China); Bo Su, Anchor Semiconductor, Inc. (United States) . . . . . [7488-14]

3:00 pm: **Challenging defect repair techniques for maximizing mask repair yield**, Anthony D. Garetto, Carl Zeiss SMT Inc. (United States); Jens Oster, NaWoTec GmbH (Germany); Markus Waiblinger, Carl Zeiss SMS GmbH (Germany); Klaus Edinger, NaWoTec GmbH (Germany) . . . . . [7488-15]

3:20 pm: **Expanding the lithography process window (PW) with CDC technology**, Sz-Huei Wang, Chung-Ming Kuo, Yu-Wan Chen, Powerchip Semiconductor Corp. (Taiwan); Guy Ben-Zvi, Pixer Technology Ltd. (Israel) and Carl Zeiss SMS GmbH (Germany); Erez Graitzer, Avi Cohen, Pixer Technology Ltd. (Israel) . . . . . [7488-16]

Coffee Break . . . . . 3:40 to 4:10 pm

SESSION 5

Room: Ferrante . . . . . .Tues. 10:40 am to 12:00 pm

Nano-Imprint and Patterned Media Technology I

Session Chairs: **Dan Gentry,** Xyratex International Inc.; **Brian J. Grenon,** Grenon Consulting, Inc.

10:40 am: **Lithographic patterning of magnetic recording media**, Thomas R. Albrecht, Hitachi Global Storage Technologies, Inc. (United States)[7488-23]

11:00 am: **Nano-imprint lithography: enabling technology for discrete track recording (DTR) media and beyond**, Peter R. Goglia, Dan Gentry, Xyratex International Inc. (United States) . . . . . [7488-24]

11:20 am: **High-precision and low-cost lithography for patterned media**, David S. Kuo, Kim Y. Lee, Henry Yang, Yautzong E. Hsu, Hongying Wang, Zhaoning Yu, Wei Hu, Justin J. Hwu, Gene Gauzner, Koichi Wago, Dieter Weller, Seagate Technology LLC (United States) . . . . . [7488-25]

11:40 am: **Discrete track media: media manufacturing perspective**, Tsutomu T. Yamashita, Western Digital Corp. (United States). . . . . [7488-26]

Lunch/Exhibition Break . . . . . 12:00 to 1:20 pm

SESSION 6

Room: Ferrante . . . . . .Tues. 1:20 to 3:00 pm

Nano-Imprint and Patterned Media Technology II

Session Chairs: **Peter R. Goglia,** Xyratex International Inc.; **Ronald J. Miller,** EV Group Inc.

1:20 pm: **Study of program defects of 22-nm nano-imprint template with an advanced e-beam inspection system**, Takaaki Hiraka, Naoya Hayashi, Jun Mizuochi, Yuko Nakanishi, Satoshi Yusa, Shiho Sasaki, Masaaki Kurihara, Dai Nippon Printing Co., Ltd. (Japan); Nobuhito Toyama, Dai Nippon Printing Co. America, Inc. (United States); Yasutaka Morikawa, Hiroshi Mohri, Dai Nippon Printing Co., Ltd. (Japan); Hong Xiao, Chiyan Kuan, Jack Y. Jau, Hermes Microvision, Inc. (United States) . . . . . [7488-27]

1:40 pm: **A cost of ownership model for imprint lithography templates for HDD applications**, Brian J. Grenon, Grenon Consulting, Inc. (United States) . . . . . [7488-28]

2:00 pm: **High-resolution e-beam repair for nano-imprint templates**, Marcus Pritschow, Institut für Mikroelektronik Stuttgart (Germany); Harald Dobberstein, Klaus Edinger, Carl Zeiss SMS GmbH (Germany); Mathias Irmscher, Institut für Mikroelektronik Stuttgart (Germany); Douglas J. Resnick, Kosta Selinidis, Ecron Thompson, Molecular Imprints, Inc. (United States); Markus Waiblinger, Carl Zeiss SMS GmbH (Germany) . . . . . [7488-29]

2:20 pm: **Duplicated quartz template for 2.5-inch discrete track media**, Noriko Yamashita, Tadashi Oomatsu, Satoshi Wakamatsu, Katsuhiro Nishimaki, Toshihiro Usa, Kazuyuki Usuki, FUJIFILM Corp. (Japan) . [7488-30]

2:40 pm: **Requirements in mold manufacturing for pattern media**, Babak Heidari, OBDUCAT AB (Sweden) . . . . . [7488-31]

SESSION 7

Room: Ferrante . . . . . .Tues. 3:00 to 3:40 pm

Source-Mask Optimization

Session Chair: **Artur P. Balasinski,** Cypress Semiconductor Corp.

3:00 pm: **Source-mask co-optimization (SMO) using level set methods**, Vikram L. Tolani, Peter Hu, Danping Peng, Tom Cecil, Robert Sinn, Linyong Pang, Bob E. Gleason, Luminescent Technologies, Inc. (United States) . . . . . [7488-32]

3:20 pm: **Sampling design for the joint source-mask optimization**, Yuri Granik, J. Andres Torres, Mentor Graphics Corp. (United States) . . . [7488-33]

Coffee Break . . . . . 3:40 to 4:10 pm

Tuesday 15 September *(continued)*

Sessions 2-3-4 run concurrently with sessions 5-6-7-8.

SESSION 4

Room: Steinbeck Forum . . . . . .Tues. 4:10 to 6:10 pm

Mask Films, Process Control, and Equipment

Session Chairs: **Emily E. Gallagher,** IBM Corp.;
Peter D. Buck, Toppan Photomasks, Inc.

4:10 pm: **Post-exposure bake tuning for 32-nm photomasks**, Amy E. Zweber, IBM Corp. (United States); Toru Komizo, Toppan Photomasks, Inc. (United States); James P. Levin, John Whang, IBM Corp. (United States); Satoru Nemoto, Shinpei Kondo, Toppan Photomasks, Inc. (United States) . . . . . [7488-17]

4:30 pm: **Reduction of local CD-linewidth variations in resist develop through acoustic streaming**, Gaston Lee, HamaTech APE GmbH & Co. KG (Taiwan); Peter Dress, HamaTech APE GmbH & Co. KG (Germany); Ssuwei Chen, Uwe U. Dietze, Hamatech USA Inc. (United States). . . . . [7488-18]

4:50 pm: **Plasma characterization of Tetra III Cr etch system**, Michael Grimbergen, Keven Yu, Toi-Yue Leung, Madhavi Chandrachood, Alan Ouye, Saravjeet Singh, Ibrahim M. Ibrahim, Ajay Kumar, Applied Materials, Inc. (United States). . . . . [7488-19]

5:10 pm: **Behavior of the molybdenum silicide thin film by 193-nm exposure**, Sin-Ju Yang, Kee-Soo Nam, S&S TECH (Korea, Republic of); Han-Sun Cha, Jin-Ho Ahn, Hanyang Univ. (Korea, Republic of). . . . . [7488-20]

5:30 pm: **Mask performance improvement with mapping**, Jan Hendrik Peters, Clemens S. Utzny, Eric Cotte, Advanced Mask Technology Ctr. (Germany) . . . . . [7488-21]

5:50 pm: **Enhanced laser writing techniques for bimetallic grayscale photomasks**, Glenn H. Chapman, James M. Dykes, Simon Fraser Univ. (Canada) . . . . . [7488-22]

SESSION 8

Room: Ferrante . . . . . .Tues. 4:10 to 6:10 pm

RET and OPC/ORC

Session Chairs: **Steffen F. Schulze,** Mentor Graphics Corp.;
Christopher A. Spence, GLOBALFOUNDRIES Inc.

4:10 pm: **Study of litho-friendly layout design by source mask optimization using inverse lithography technology**, Hyo Chan Kim, Sungsoo Suh, Young-Chang Kim, Sung-Woo Lee, SukJoo Lee, Seong-Woon Choi, Chan-Hoon Park, Joo-Tae Moon, SAMSUNG Electronics Co., Ltd. (Korea, Republic of) [7488-34]

4:30 pm: **Subresolution assist features placement using cost-function-reduction method**, Jinyu Zhang, Tsinghua Univ. (China); Min-Chun Tsai, Brion Technologies, Inc. (United States); Wei Xiong, Yan Wang, Zhiping Yu, Tsinghua Univ. (China) . . . . . [7488-35]

4:50 pm: **Inverse lithography (ILT) mask manufacturability for fullchip DRAM production**, Kiho Baik, Vikram L. Tolani, Guangming Xiao, Dong H. Son, David H. Kim, Bob E. Gleason, Luminescent Technologies, Inc. (United States); Byung-Gook Kim, Sungsoo Suh, SAMSUNG Electronics Co., Ltd. (Korea, Republic of). . . . . [7488-95]

5:10 pm: **SRAF enhancement using inverse lithography for 32-nm hole patterning and beyond**, Vincent Farys, Frederic Robert, STMicroelectronics (France); Fahd Chaoui, Jorge Entradas, Olivier R. Toublan, Mentor Graphics (Ireland) Ltd. (France); Yorick Trouiller, Lab. d'Electronique de Technologie de l'Information (France). . . . . [7488-37]

5:30 pm: **Model-based assist feature placement for 32-nm and 22-nm technology nodes using inverse mask technology**, Amyn A. Poonawala, Benjamin D. Painter, Chip Kerchner, Synopsys, Inc. (United States) . [7488-38]

5:50 pm: **Model-based assist features,** Bayram Yenikaya, Apo Sezginer, Cadence Design Systems, Inc. (United States). . . . . [7488-39]

POSTERS - TUESDAY

Monterey Conference Center, Serra Grand Ballroom

Tuesday 15 September, 6:30 to 8:00 pm

Session Chairs: **Wilhelm Maurer,** Infineon Technologies AG (Germany); **Larry S. Zurbrick,** Agilent Technologies, Inc.

EXHIBITION/POSTER RECEPTION

Monterey Conference Center, Serra Grand Ballroom

Tuesday 15 September, 6:30 to 8:00 pm

Symposium attendees and guests are invited to attend an Exhibition/Poster Reception on Tuesday evening in the Serra Grand Ballroom. The reception provides an opportunity for attendees to meet colleagues, network, and view poster papers. Refreshments will be served. Attendees are requested to wear their conference registration badges.

POSTER VIEWING

Tuesday 15 September, 6:30 to 8:00 pm • Wednesday 16 September, 10:00 am to 3:00 pm

Poster authors may set up their poster papers between 10:00 am and 4:00 pm on Tuesday and will leave them up until Wednesday afternoon. Authors must be present during the Poster Reception 6:30 to 8:00 pm Tuesday to answer questions and provide in-depth discussion regarding their papers. Any posters not removed by Wednesday at 3:00 pm will be considered unwanted and will be discarded. SPIE assumes no responsibility for papers left up after Wednesday at 3:00 pm.

Cleaning/Contamination/Haze

Back-glass cleaning: reducing repelliclization costs by focused action, Francesca Perissinotti, Luca Sartelli, Hiroyuki Miyashita, DNP Photomask Europe (Italy); Ming-Chien Chiu, Yu-Chang Liu, Hung-Chieh Chung, Gudeng Precision Industrial Co., Ltd. (Taiwan); Frank Sundermann, Stuart Gough, Sonia Tourniol, Felix Dufaye, STMicroelectronics (France) . . . . . [7488-96]

EUV Mask

Feasibility study of the complex approach to flare, shadowing, optical, and process corrections for EUVL MDP, Peter Nikolsky, Natalia Davydova, Paul J. van Adrichem, ASML Netherlands B.V. (Netherlands); Jiong Jiang, Huayu Liu, Brion Technologies, Inc. (United States) . . . . . [7488-89]

Novel EUV mask inspection tool with 199-nm laser source and high-resolution optics, Nobutaka Kikuiri, Ryoichi Hirano, Masatoshi Hirono, Advanced Mask Inspection Technology, Inc. (Japan); Kinya Usuda, Hideaki Hashimoto, Kenichi Takahara, Nuflare Technology, Inc. (Japan); Hiroyuki Shigemura, Osamu Suga, Tsuyoshi Amano, Semiconductor Leading Edge Technologies, Inc. (Japan). . . . . [7488-98]

Inspection and Repair

Automated wafer defect analysis using high-resolution reticle inspection data, Bryan W. Reese, Poh-Boon Yong, KLA-Tencor Corp. (United States) . . . . . [7488-100]

Aerial plane inspection for advanced photomask defect detection, Trent A. Hutchinson, KLA-Tencor Texas (United States); William J. Huang, Song Pang, KLA-Tencor Corp. (United States). . . . . [7488-101]

AIMS™ mask qualification for 32-nm node, Rigo Richter, Holger Seitz, Thomas Thaler, Ulrich Stroessner, Thomas Scherübl, Carl Zeiss SMS GmbH (Germany) . . . . . [7488-102]

Inspection of complex OPC patterns for 4x node and beyond, Sang Hoon Han, Wonil Cho, Won Sun Kim, Dong-Hoon Chung, Chan Uk Jeon, Han-ku Cho, SAMSUNG Electronics Co., Ltd. (Korea, Republic of). . . . . [7488-103]

Theoretical foundations of die-to-model inspection, Lev Faivishevsky, Sergey Khristo, Ishai Schwarzband, Shmoolik Mangan, Applied Materials (Israel) . . . . . [7488-106]

POSTERS - TUESDAY *(continued)*

Session Chairs: **Wilhelm Maurer,** Infineon Technologies AG (Germany); **Larry S. Zurbrick,** Agilent Technologies, Inc.

New analysis tools and processes for mask repair verification and defect disposition based on AIMS™ images, Eric R. Poortinga, Carl Zeiss SMT Inc. (United States); Thomas Scheruebl, Rigo Richter, Carl Zeiss SMS GmbH (Germany) . . . . . [7488-107]

New tools to enable photomask repair to the 32-nm node, Ronald R. Bozak, Ken Roessler, Bernie Arruza, Dennis Hogle, Roy L. White, Tod E. Robinson, Michael D. Archuletta, David A. Lee, RAVE LLC (United States) . . . . . [7488-146]

Mask Data Preparation

Reducing the shot counts of mask writing with OPC by extracting repeating patterns, Masahiro Shoji, Nippon Control System Corp. (Japan); Tadao Inoue, SII Nanotechnology Inc. (Japan); Masaki Yamabe, Association of Super-Advanced Electronics Technologies (Japan) . . . . . [7488-108]

Improving the quality of fractured mask data through in-place optimization of the fracturing solution, D. S. S. Bhardwaj, Nageswara Rao, Archana Rajagopalan, Nitin Bhat, Ravi R. Pai, SoftJin Technologies Pvt. Ltd. (India) . . . . . [7488-109]

Economic assessment of lithography strategies for the 22-nm technology node, Tejas Jhaveri, Andrzej J. Strojwas, Carnegie Mellon Univ. (United States); Larry Pileggi, Vyacheslav Rovner, PDF Solutions, Inc. (United States) and Carnegie Mellon Univ. (United States) . . . . . [7488-144]

Mask Process Control/Equipment

Improved particle control by adopting advanced ceramic materials in dry etcher for defect reduction, Dong-Soo Min, Guen-Ho Hwang, PKL Co., Ltd. (Korea, Republic of) . . . . . [7488-111]

Mask Substrate/Blank/Films

The study of the birefringence as PSM materials for immersion lithography, Ju-Hyun Kang, S&S TECH (Korea, Republic of); Han-Sun Cha, Hanyang Univ. (Korea, Republic of); Sin-Ju Yang, S&S TECH (Korea, Republic of); Jin-Ho Ahn, Hanyang Univ. (Korea, Republic of); Kee-Soo Nam, S&S TECH (Korea, Republic of) . . . . . [7488-112]

Metrology

A study of contour image comparison measurement for photomask patterns in 32-nm beyond, Isao Yonekura, Hidemitsu Hakii, Masaru Higuchi, Keishi Tanaka, Toppan Printing Co., Ltd. (Japan); Yoshiaki Ogiso, Toshihide Oba, Toshimichi Iwai, Jun Matsumoto, Takayuki Nakamura, Advantest Corp. (Japan) . . . . . [7488-113]

Noble approach for mask-wafer measurement by design-based metrology integration system, Tatsuya Maeda, Ryoichi Matsuoka, Hitachi High-Technologies Corp. (Japan); Katsuya Hayano, Dai Nippon Printing Co., Ltd. (Japan) . . . . . [7488-114]

Corner rounding analysis of reticle, optical, and resist contributions, Yunfei Deng, Jongwook Kye, Thomas I. Wallow, Harry J. Levinson, GLOBALFOUNDRIES Inc. (United States) . . . . . [7488-115]

OPC

Investigation of subresolution assist feature process window, Mingjing Tian, Zhi Gang Yang, Semiconductor Manufacturing International Corp. (China) . . . . . [7488-36]

Adaptive OPC approach based on image simulation, Qingwei Liu, Semiconductor Manufacturing International Corp. (China); Liguo Zhang, Mentor Graphics Shanghai Electronic Technology Co. (China) . . . . [7488-116]

Introducing process variability score for process window OPC optimization, Moutaz Fakhry, Mentor Graphics Corp. (United States); Hesham Maaty, Mentor Graphics Corp. (Egypt); Ahmed M. Seoud, Mentor Graphics Corp. (United States) . . . . . [7488-117]

Patterning of 90-nm node flash contact hole with assist feature using KrF, Yeonah Shim, Sungho Jun, Jae-hyun Kang, Jaeyoung Choi, Kwangseon Choi IV, Jaewon Han, Dongbu HiTek Co., Ltd. (Korea, Republic of) . . . . . [7488-118]

On comparing conventional and electrically driven OPC techniques, Puneet Gupta, Dominic Reinhard, Univ. of California, Los Angeles (United States) . . . . . [7488-119]

OPC model calibration and parameter optimization for 3D complex patterns using scatterometry data, Oleg Kritsun, GLOBALFOUNDRIES Inc. (United States); Aasutosh Dave, Mentor Graphics Corp. (United States); Yunfei Deng, GLOBALFOUNDRIES Inc. (United States); Jie Li, Jiangtao Hu, Nanometrics Inc. (United States). . . . . [7488-120]

OPC model space approach to in-line process monitoring structures, Romuald Sabatier, STMicroelectronics (France) and Institut Fresnel (France); Antonio Di Giacomo, STMicroelectronics (France); Caroline Fossati, Salah Bourennane, Institut Fresnel (France) . . . . . [7488-121]

Practical application of OPC in electrical circuits, Martin McCallum, Nikon Precision Europe GmbH (United Kingdom); Stewart Smith, Andreas Tsiamis, Anthony J. Walton, J. Tom Stevenson, The Univ. of Edinburgh (United Kingdom); Andrew C. Hourd, Univ. of Dundee (United Kingdom). . . [7488-122]

Pattern Generation/Equipment

Three-dimensional Si aperture plates combined with programmable blanking plates for multibeam mask writing, Florian Letzkus, Mathias Irmscher, Michael Jurisch, Institut für Mikroelektronik Stuttgart (Germany); Elmar Platzgummer, Christof Klein, Hans Loeschner, IMS Nanofabrication AG (Austria) . . . . . [7488-123]

Simulation and Modeling

Examination about observation of the identical position of a mask and silicon, Ryoichi Matsuoka, Hiroaki Mito, Yoshihiro Ota, Hitachi High Technologies Corp. (Japan); Yasutaka Toyoda, Hitachi, Ltd. (Japan) . . . . . [7488-124]

Revisit to aberration: a simulation study of lens aberration-induced overlay misalignment and its experimental validation, Hoyeon Kim, Sung-Woo Lee, Byeong-Cheol Lee, Sanghwa Lee, Kyoungyong Cho, Seong-Woon Choi, Chan-Hoon Park, SAMSUNG Electronics Co., Ltd. (Korea, Republic of) . . . . . [7488-125]

Wafer topography proximity effect modeling and correct for the implant layer, Hua Song, James P. Shiely, Synopsys, Inc. (United States) . . [7488-126]

Fast and accurate computation of partially coherent imaging by stacked pupil shift operator, Yaogang Lian, Xin Zhou, Luminescent Technologies, Inc. (United States) . . . . . [7488-128]

Extensions of boundary layer modeling of photomask topography effects to fast-CAD via pattern matching, Marshal A. Miller, Andrew R. Neureuther, Univ. of California, Berkeley (United States) . . . . . [7488-130]

Calibration of lithography and etch models using SEM images, Kostyantyn Chuyeshov, Jesus Carrero, Apo Sezginer, Vishnu G. Kamat, Cadence Design Systems, Inc. (United States) . . . . . [7488-133]

Predictive modeling for EBPC in EBDW, Rainer Zimmermann, Martin Schulz, Wolfgang Hoppe, Hans-Jürgen Stock, Wolfgang Demmerle, Synopsys GmbH (Germany); Alex Zepka, Synopsys, Inc. (United States); Serdar Manakli, Laurent Pain, Lab. d'Electronique de Technologie de l'Information (France) . . . . . [7488-135]

Effective methodology to make DFM guide line, Jaeyoung Choi, Yeonah Shim, Kyunghee Yun, Kwangseon Choi IV, Jaewon Han, Dongbu HiTek Co., Ltd. (Korea, Republic of) . . . . . [7488-136]

pRSM: models for model-based litho-hotspot repair algorithms, Marko Chew, Toshikazu Endo, Yue Yang, Mentor Graphics Corp. (United States) . . . . . [7488-137]

Effect of SRAF placement on process window for technology nodes that uses variable etch bias, Ahmed M. Seoud, Mentor Graphics Corp. (United States) . . . . . [7488-138]

FPGA as the programable tool for yield improvement, Tho L. La, Xilinx, Inc. (United States); Charles Chen, Xilinx, Inc. (Taiwan); M. H. Wang, Chih-Chung Huang, Ching-Tsai Chang, Hornjaan Lin, Yming Tseng, Ian Tseng, You R. Wu, Shih Chieh Lo, Sam C. Y. Lin, United Microelectronics Corp. (Taiwan) . . . . . [7488-141]

Model-based lints for litho-hotspots repair, Yue Yang, Marko Chew, Toshikazu Endo, Mark Simmons, Mentor Graphics Corp. (United States) . . . . . [7488-142]

What is a good empirical model for OPC?, Eldar Khaliullin, Yaogang Lian, Mark Davey, Xin Zhou, Luminescent Technologies, Inc. (United States) . . . . . [7488-143]

Wednesday 16 September

Sessions 9-10-11-12-13 run concurrently with sessions 14-15-16-17-18.

SESSION 9

Room: Steinbeck Forum . . . . . Wed. 8:00 to 10:00 am

EUV Mask Substrates and Processing

Session Chairs: **Archita Sengupta,** Intel Corp.; **Han-Ku Cho,** SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

8:00 am: **Correlation of overlay performance and reticle substrate nonflatness effects in EUV lithography**, Sudharshanan Raghunathan, John G. Hartley, Univ. at Albany (United States); Jaewoong Sohn, Kevin Orvek, Sematech North (United States) . . . . . [7488-40]

8:20 am: **Etch process development of different blank structure for EUV mask production**, Yong-Dae Kim, Hynix Semiconductor Inc. (Korea, Republic of) . . . . . [7488-41]

8:40 am: **Thin absorber EUVL mask with light-shield border for full-field scanner**, Takashi Kamo, Toshihiko Tanaka, Osamu Suga, Semiconductor Leading Edge Technologies, Inc. (Japan) . . . . . [7488-42]

9:00 am: **EUVL ML mask-blank fiducial mark application for ML defect mitigation**, Pei-Yang Yan, Intel Corp. (United States) . . . . . [7488-43]

9:20 am: **Optimized mask structure for the reduction of shadow effect on 22-nm node**, Eun-Jin Kim, Hyunsu Kim, InWook Cho, Hanyang Univ. (Korea, Republic of); Seong-Sue Kim, Han-Ku Cho, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Ilsin An, Hye-Keun Oh, Hanyang Univ. (Korea, Republic of) . . . . . [7488-44]

9:40 am: **Actinic EUVL mask-blank inspection capability with time-delay integration mode**, Takeshi Yamane, Teruo Iwasaki, Toshihiko Tanaka, Tsuneo Terasawa, Osamu Suga, Semiconductor Leading Edge Technologies, Inc. (Japan). . . . . [7488-45]

Coffee Break . . . . . 10:00 to 10:30 am

SESSION 10

Room: Steinbeck Forum . . . . . Wed. 10:30 am to 12:10 pm

Patterning Technology and Tools

Session Chairs: **Thomas H. Newman,** Micronic Laser Systems Inc.; **Hiroshi Nozue,** NuFlare Technology, Inc. (Japan)

10:30 am: **Development of multiple-pass exposure in electron-beam direct-write lithography for sub-32-nm nodes**, Luc Martin, Serdar Manakli, Béatrice Icard, Jonathan Pradelles, Lab. d'Electronique de Technologie de l'Information (France); Régis Orobtchouk, Alain Poncet, Institut National des Sciences Appliquées de Lyon (France); Laurent Pain, Lab. d'Electronique de Technologie de l'Information (France) . . . . . [7488-46]

10:50 am: **Charged particle multibeam lithography evaluations for sub-16-nm hp mask node fabrication**, Elmar Platzgummer, Hans Loeschner, IMS Nanofabrication AG (Austria); Joerg Butschke, Holger Sailer, Mathias Irmscher, Institut für Mikroelektronik Stuttgart (Germany) . . . . . [7488-47]

11:10 am: **Electron-beam mask writer EBM-7000 for Hp 32-nm generation**, Takashi Kamikubo, Kenji Ohtoshi, Noriaki Nakayamada, Rieko Nishimura, Hitoshi Sunaoshi, NuFlare Technology, Inc. (Japan); Kiminobu Akeno, Soichiro Mitsui, Toshiba Corp. (Japan); Yuichi Tachikawa, Hideo Inoue, Susumu Oogi, Hitoshi Higurashi, Akinori Mine, Takiji Ishimura, Seiichi Tsuchiya, Yoshitada Gomi, Hideki Matsui, Shuichi Tamamushi, NuFlare Technology, Inc. (Japan). . . . . [7488-48]

11:30 am: **Exposure results with four-column cells in multicolumn EB exposure system**, Akio Yamada, Hiroshi Yasuda, Advantest Corp. (Japan); Masaki Yamabe, Association of Super-Advanced Electronics Technologies (Japan). . . . . [7488-49]

11:50 am: **Enabling photomask technology for large and small displays**, Tor Sandstrom, Micronic Laser Systems AB (Sweden). . . . . [7488-50]

Lunch/Exhibition Break . . . . . 12:10 to 1:40 pm

SESSION 14

Room: Ferrante . . . . . Wed. 8:20 to 10:00 am

Nano-Imprint and Patterned Media Technology III

Session Chairs: **Naoya Hayashi,** Dai Nippon Printing Co., Ltd. (Japan); **Tsutomu T. Yamashita,** Western Digital Corp.

8:20 am: **6-inch circle template fabrication for patterned media using a conventional resist and new chemically amplified resists**, Morihisa Hoga, Masaharu Fukuda, Tsuyoshi Chiba, Mikio Ishikawa, Naoko Kuwahara, Kimio Itoh, Masaaki Kurihara, Dai Nippon Printing Co., Ltd. (Japan); Nobuhito Toyama, Dai Nippon Printing Co. America, Inc. (United States); Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan) . . . . . [7488-64]

8:40 am: **A new x-ray metrology for characterizing a shape of nanostructure of patterned media**, Kazuhiko Omote, Yoshiyasu Ito, Kiyoshi Ogata, Rigaku Corp. (Japan); Yuichi Kokaku, Hitachi, Ltd. (Japan) . . [7488-65]

9:00 am: **Polymeric soft stamps for patterned media applications**, Ronald J. Miller, Jr., EV Group Inc. (Austria); Paul Lindner, Gerald Kreindl, Markus Wimplinger, Thomas Glinsner, Michael Kast, Dominik Treiblmayr, EV Group E. Thallner GmbH (Austria) . . . . . [7488-66]

9:20 am: **Inspection for nano-imprint lithography at 32-nm with an advanced e-beam inspection system**, Hong Xiao, Hermes Microvision, Inc. (United States). . . . . [7488-67]

9:40 am: **SEM CD metrology on nanoimprint template: an analytical SEM approach**, Justin J. Hwu, Seagate Technology LLC (United States); Sergey Babin, Abeam Technologies (United States). . . . . [7488-68]

Coffee Break . . . . . 10:00 to 10:30 am

SESSION 15

Room: Ferrante . . . . . Wed. 10:30 to 11:50 am

Nano-Imprint and Patterned Media Technology IV

Session Chairs: **Dan Gentry,** Xyratex International Inc.; **Dieter Weller,** Seagate Technology LLC

10:30 am: **Optical metrology for template and disk patterned imprints**, Roman Sappey, Arthur Jenkins, Sri Venkataram, KLA-Tencor Corp. (United States) . . . . . [7488-69]

10:50 am: **Mold fabrication for discrete track recording media**, Hiroshi Yamashita, Hideo Kobayashi, Takashi Sato, Osamu Nagarekawa, HOYA Corp. (Japan). . . . . [7488-70]

11:10 am: **A nondestructive metrology solution for detailed measurements of imprint templates and media**, Jeffrey W. Roberts, Linlin Hu, n&k Technology, Inc. (United States); Torbjorn Eriksson, Kristian Thulin, Obducat Technologies AB (Sweden); Babak Heidari, OBDUCAT AB (Sweden) [7488-71]

11:30 am: **High-volume step and flash imprint lithography for patterned media**, Douglas J. Resnick, Cynthia Brooks, Gerard M. Schmid, Michael L. Miller, Dwayne L. LaBrake, S. V. Sreenivasan, Molecular Imprints, Inc. (United States) . . . . . [7488-72]

Lunch/Exhibition Break . . . . . 11:50 am to 1:20 pm

SESSION 16

Room: Ferrante . . . . . Wed. 1:20 to 2:00 pm

Mask Business

Session Chairs: **Uwe F.W. Behringer,** UBC Microelectronics (Germany); **Brian J. Grenon,** Grenon Consulting, Inc.

1:20 pm: **Fabless but not fab-careless**, Toshiyuki Hisamura, Xin Wu, Soumya Banerjee, Xilinx, Inc. (United States) . . . . . [7488-73]

1:40 pm: **A universal mask management relational database**, Philippe Morey-Chaisemartin, XYALIS (France) . . . . . [7488-74]

Wednesday 16 September

Sessions 9-10-11-12-13 run concurrently with sessions 14-15-16-17-18 (continued).

SESSION 11

Room: Steinbeck Forum . . . . . Wed. 1:40 to 3:00 pm

Metrology I

Session Chairs: **Thomas Scheruebl,** Carl Zeiss SMS GmbH (Germany); **Jacek K. Tyminski,** Nikon Precision Inc.

1:40 pm: **Results of an international photomask linewidth comparison of NIST and PTB**, Harald Bosse, Wolfgang Hässler-Grohne, Bernd Bodermann, Detlef Bergmann, Egbert Buhr, Physikalisch-Technische Bundesanstalt (Germany); James E. Potzick, Richard Quintanilha, Ronald G. Dixson, Michael T. Stocker, National Institute of Standards and Technology (United States) . . . . . [7488-51]

2:00 pm: **Measurement sampling frequency impact on determining magnitude of pattern placement errors on photomasks**, John M. Whittey, Frank Laske, KLA-Tencor Corp. (United States); Neil Berglund, Mike Takac, NorthWest Technology Group (United States); Seurien Chou, Synopsys, Inc. (United States); Klaus-Dieter Roeth, KLA-Tencor Corp. (United States) . . . . . [7488-52]

2:20 pm: **An 193-nm optical CD metrology tool for the 32-nm node**, Zhi Li, Frank Pilarski, Detlef Bergmann, Bernd Bodermann, Physikalisch-Technische Bundesanstalt (Germany) . . . . . [7488-53]

2:40 pm: **How much is enough? an analysis of CD measurement amount for mask characterization**, Albrecht Ullrich, Jan Richter, Advanced Mask Technology Ctr. GmbH Co. KG (Germany) . . . . . [7488-54]

Coffee Break . . . . . 3:00 to 3:30 pm

SESSION 12

Room: Steinbeck Forum . . . . . Wed. 3:30 to 5:30 pm

Metrology II

Session Chairs: **James E. Potzick,** National Institute of Standards and Technology; **John M. Whittey,** KLA-Tencor Corp.

3:30 pm: **Photomask metrology using a 193-nm scatterfield microscope**, Richard Quintanilha, National Institute of Standards and Technology (United States); Yeung Joon Sohn, KT Consulting Inc. (United States) and National Institute of Standards and Technology (United States); Lowell P. Howard, Precera, Inc. (United States) and National Institute of Standards and Technology (United States); Michael T. Stocker, Richard M. Silver, James E. Potzick, National Institute of Standards and Technology (United States) . . . . . [7488-55]

3:50 pm: **Experimental test results of pattern placement metrology on photomasks with laser illumination source designed to address double-patterning lithography challenges**, Klaus-Dieter Roeth, Frank Laske, Dieter K. Adam, Michael Heiden, Lidia Parisoli, Slawomir Czerkas, John M. Whittey, KLA-Tencor GmbH (Germany). . . . . [7488-56]

4:10 pm: **In-die metrology on photomasks for low-k1 lithography**, Thomas Scheruebl, Dirk Beyer, Ute Buttgereit, Carl Zeiss SMS GmbH (Germany) . . . . . [7488-57]

4:30 pm: **Critical dimension uniformity using reticle inspection tool**, Venugopal Vellanki, KLA-Tencor Corp. (United States). . . . . [7488-58]

4:50 pm: **IntenCD technology for fast and accurate scanner performance: determination**, Ilan Englard, Applied Materials BV (Netherlands); Jo M. Finders, Ingrid M. Janssen, Frank Duray, Marcel Demarteau, Ono Wissmans, Jacques A. Waelpoel, ASML Netherlands B.V. (Netherlands); Shmoolik Mangan, Michael Ben Yishai, Yaron Cohen, Yair Elblinger, Neil Berns, Applied Materials (Israel) . . . . . [7488-59]

5:10 pm: **New AFM solution for photomask metrology**, Yueming Hua, Sung Park, Ryan Yoo, Sang-il Park, Park Systems Inc. (United States). . . . [7488-60]

SESSION 13

Room: Steinbeck Forum . . . . . Wed. 5:30 to 5:50 pm

Mask Cleaning and Maintenance

Session Chairs: **Bryan S. Kasprowicz,** Photronics, Inc.; **Brian J. Grenon,** Grenon Consulting, Inc.

5:30 pm: **Advances in CO_2 cryogenic aerosol technology for photomask post AFM repair**, Charles W. Bowers, Ivin Varghese, Mehdi Balooch, Werner V. Brandt, Eco-Snow Systems, Inc. (United States) . . . . . [7488-62]

SESSION 17

Room: Ferrante . . . . . Wed. 2:00 to 3:20 pm

Mask Data Preparation

Session Chairs: **Frank Abboud,** Intel Corp.; **Christopher A. Spence,** GLOBALFOUNDRIES Inc.

2:00 pm: **Deployment of OASIS.MASK (P44) as direct input for mask inspection of advanced photomasks**, Tsafi Lapidot, Khen Ofek, Aviram Tam, Mark Wagner, Applied Materials, Inc. (Israel); Suheil Zaatri, Yan Liu, Michael Asturias, Joan McCall, Wei-Guo J. Lei, Intel Corp. (United States); Minyoung Park, Amanda M. Bowhill, Emile Sahouria, Steffen F. Schulze, Mentor Graphics Corp. (United States). . . . . [7488-75]

2:20 pm: **Mask data prioritization based on design intent-II**, Masakazu Endo, Kokoro Kato, Tadao Inoue, Masaki Yamabe, Association of Super-Advanced Electronics Technologies (Japan). . . . . [7488-76]

2:40 pm: **Favorable hierarchy detection through Lempel-Ziv coding-based algorithm to aid hierarchical fracturing in mask data preparation**, D. S. S. Bhardwaj, Nilanjan Ghosh, Nageswara Rao, Ravi R. Pai, SoftJin Technologies Pvt. Ltd. (India) . . . . . [7488-77]

3:00 pm: **Latest results and computing performance of the ePLACE data preparation tool**, Juergen Gramss, Ulf Weidenmueller, Vistec Electron Beam GmbH (Germany); Reinhard R. Galler, EQUIcon Software GmbH Jena (Germany); Volker Neick, Arnd Stoeckel, Vistec Electron Beam GmbH (Germany); Detlef Melzer, Martin Suelzle, EQUIcon Software GmbH Jena (Germany); Joerg Butschke, Institut für Mikroelektronik Stuttgart (Germany); Ulrich Baetz, Fraunhofer-Institut für Photonische Mikrosysteme (Germany) . . . . . [7488-79]

Coffee Break . . . . . 3:20 to 3:50 pm

SESSION 18

Room: Ferrante . . . . . Wed. 3:50 to 5:50 pm

Simulation and Modeling

Session Chairs: **J. Tracy Weed,** Synopsys, Inc.; **Kiho Baik,** Luminescent Technologies, Inc.

3:50 pm: **Impact of mask roughness on resist line-edge roughness**, Chris A. Mack, Lithoguru.com (United States) . . . . . [7488-80]

4:10 pm: **Full-chip mask process verification: sequential verification of e-beam, short-range etch, and long-range mask process effects**, Ali Mokhberi, Changsheng Ying, Cadence Design Systems, Inc. (United States) . . . . . [7488-81]

4:30 pm: **Challenges for the 28-nm half node: is the optical shrink dead?**, J. Andres Torres, Fedor G. Pikus, Oberdan W. Otto, Mentor Graphics Corp. (United States). . . . . [7488-82]

4:50 pm: **Reduced basis method for computational lithography**, Jan Pomplun, Konrad-Zuse-Zentrum für Informationstechnik Berlin (Germany); Lin W. Zschiedrich, Sven Burger, JCMwave GmbH (Germany); Frank Schmidt, Konrad-Zuse-Zentrum für Informationstechnik Berlin (Germany). . . . [7488-83]

5:10 pm: **Efficient analysis of three-dimensional EUV mask-induced imaging artifacts using the waveguide decomposition method**, Feng Shao, Peter Evanschitzky, Tim Fühner, Andreas Erdmann, Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany) . . . . . [7488-84]

5:30 pm: **Isotropic treatment of EMF effects in advanced photomasks**, Jaione Tirapu-Azpiroz, Alan E. Rosenbluth, Ioana C. Graur, IBM Corp. (United States) . . . . . [7488-85]

Thursday 17 September

SESSION 19

Room: Steinbeck Forum . . . . . Thurs. 8:20 to 9:00 am

EUV Mask Contamination and Cleaning

Session Chairs: **Jan Hendrik Peters,** Advanced Mask Technology Ctr. GmbH Co. KG (Germany); **Naoya Hayashi,** Dai Nippon Printing Co., Ltd. (Japan)

8:20 am: **Impact of carbon contamination on EUV masks**, Yu-Jen Fan, Leonid Yankulin, Univ. at Albany (United States); Andrea F. Wüest, Francis Goodwin, Sungmin Huh, SEMATECH North (United States); Patrick P. Naulleau, Kenneth A. Goldberg, Lawrence Berkeley National Lab. (United States); Gregory P. Denbeaux, Univ. at Albany (United States). . . . . [7488-86]

8:40 am: **Critical issues and progress in EUV mask cleaning**, Takeya Shimomura, Dai Nippon Printing Co. America, Inc. (United States); Ted Liang, Intel Corp. (United States) . . . . . [7488-87]

SESSION 20

Room: Steinbeck Forum . . . . . Thurs. 9:00 to 10:00 am

EUV Mask Data Preparation and Inspection

Session Chairs: **Naoya Hayashi,** Dai Nippon Printing Co., Ltd. (Japan); **Jan Hendrik Peters,** Advanced Mask Technology Ctr. GmbH Co. KG (Germany)

9:00 am: **Modeling of EUV lithography**, Eric Hendrickx, Gian F. Lorusso, IMEC (Belgium); Eelco Van Setten, ASML Netherlands B.V. (Netherlands); Steven G. Hansen, ASML US, Inc. (United States); Martin Lowisch, Carl Zeiss SMT AG (Germany); Jiong Jiang, Wei Liu, Luoqi Chen, Brion Technologies, Inc. (United States) . . . . . [7488-99]

9:20 am: **Investigation of buried EUV mask defect printability using actinic inspection and fast simulation**, Christopher H. Clifford, Sandy Wiraatmadja, Tina T. Chan, Andrew R. Neureuther, Univ. of California, Berkeley (United States) . . . . . [7488-90]

9:40 am: **Study of EUVL mask pattern defect inspection using 199-nm inspection tool with superresolution method**, Hiroyuki Shigemura, Tsuyoshi Amano, Osamu Suga, Yukiyasu Arisawa, Semiconductor Leading Edge Technologies, Inc. (Japan); Ryoichi Hirano, Masatoshi Hirono, Nobutaka Kikuiri, Advanced Mask Inspection Technology, Inc. (Japan); Hideaki Hashimoto, Kenichi Takahara, NuFlare Technology, Inc. (Japan) . . . . . [7488-91]

Coffee Break . . . . . 10:00 to 10:30 am

SESSION 21

Room: Steinbeck Forum . . . . . Thurs. 10:30 to 11:30 am

DPL Implementation and RET Manufacturability

Session Chairs: **Frank A. Driessen,** Takumi Technology B.V. (Netherlands); **Robert J. Socha,** ASML MaskTools Inc.

10:30 am: **Single-mask double-patterning lithography**, Rani S. Ghaida, George Torres, Puneet Gupta, Univ. of California, Los Angeles (United States) . . . . . [7488-92]

10:50 am: **Resolving contacts conflicts for double-patterning split**, Nassima Zeggaoui, Vincent Farys, Emek Yesilada, Frederic Robert, Yorick Trouiller, STMicroelectronics (France) . . . . . [7488-93]

11:10 am: **Geometric distribution of full-chip DPT coloring**, Levi D. Barnes, Yong Li, Steve Biederman, Christopher M. Cork, Alexander Miloslavsky, Benjamin D. Painter, Synopsys, Inc. (United States). . . . . [7488-94]

Lunch Break . . . . . 11:30 am to 1:10 pm

SESSION 22

Room: Steinbeck Forum. . . . . Thurs. 1:10 to 4:30 pm

Special Session on Commodity or Technology? Sub-20nm Mask Making at Yet Another Crossroad

Special Session and Lunch Sponsored by

Panel Moderators: **M. Warren Montgomery,** College of NanoScale Science and Engineering (CNSE) and SEMATECH Inc.; **Wolfgang Staud,** Applied Materials, Inc.

Panelists include: **Bruno M. LaFontaine,** GLOBALFOUNDRIES Inc.; **Mark Wagner,** Applied Materials, Inc.; **Chiang Y. Yang,** Intel Corp.; **Franklin D. Kalk,** Toppan Photomasks, Inc.; **Greg P. Hughes,** SEMATECH North; **Brian J. Grenon,** Grenon Consulting Inc.; **Naoya Hayashi,** Dai Nippon Printing Co., Ltd. (Japan); **Thomas R. Albrecht,** Hitachi Global Storage Technologies, Inc.

The mask making industry once again finds itself torn between two very diverging technologies: for the first time in this conference we have a full day program of topics from the Patterned Media [Hard Disk Drive] Industry.

If maskshops want to participate in this growing market, it will require some very special tooling [rotary e-beams, optical and EB inspection, EB metrology, scatterometry, NIL, NIL coating, etch, deposition, and potentially CMP]- and all of this for a process that needs to be as cost sensitive as possible, since cost per disk is in the $1<$2 range. Not to mention the cost of change over for very special form factors.

On the other side are the almost urgent and heavy capital investment requirements for EUV tooling. Some of the same equipment, especially optical and EB inspection, blank and pattern inspection - actinic preferred, and the massive handling issues due to a non-existent pellicle.

As an alternate solution, NIL is also being investigated by IC manufacturers for a possible entry into the 1x nodes. Needless to say that SMO, ILT and DPT and SBPD are still the mainstay solutions, and also have their very specific requirements.

Captive mask shops face the challenge of having to gear up for both, or even all three, or stretch new or existing equipment across multiple technologies. Merchant shops, much the same, also need to decide to engage, and potentially set up dedicated production lines.

The various approaches are diametrically opposed. On one side is highest end users that can absorb the cost of advanced masks and EUV, on the other end extremely cost consciences commodity players, that need masks/templates on the fast and cheap, and can live with certain defect levels.

Your moderators, Warren and Wolf, will make an attempt to 'pitch' these two extremes against each other, and see which side the equipment suppliers will fall on. We are hoping for a very lively discussion, and will solicit questions and discussions from the audience [prior write-in questions allowed].

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SC724

(Pierrat), **Monday 8:30 am to 12:30 pm, $310 / $370**

Photomask Fabrication and Technology Basics

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29th Annual Symposium

SPIE Photomask Technology

Final Summary Digest

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Conference 7488:

Photomask Technology 2009

Please refer to paper/poster numbers when referencing Final Summaries. Paper titles may vary between the Program and the final summaries because of print dates.

The manuscripts will be included, in full, in the Proceedings of SPIE Volume 7488.

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SPIE

Conference 7488: Photomask Technology

Tuesday-Thursday 15-17 September 2009 • *Part of Proceedings of SPIE Vol. 7488 Photomask Technology 2009*

SPIE Photomask Technology

7488-01, Session 1

Global Collaboration in Semiconductors and Strategies for the Mask Industry (Keynote Presentation)

M. R. Polcari, SEMATECH Inc. (United States)

No abstract available

7488-02, Session 1

Mask Industry Assessment: 2009

G. P. Hughes, H. K. Yun, SEMATECH North (United States)

Microelectronics industry leaders routinely name the cost and cycle time of mask technology and mask supply as top critical issues. A survey was created with support from SEMATECH and administered by David Powell Consulting to gather information about the mask industry as an objective assessment of its overall condition. The survey is designed with the input of semiconductor company mask technologists and merchant mask suppliers. This year's assessment is the eighth in the current series of annual reports. With ongoing industry support, the report can be used as a baseline to gain perspective on the technical and business status of the mask and microelectronics industries. The report will continue to serve as a valuable reference to identify the strengths and opportunities of the mask industry. The results will be used to guide future investments pertaining to critical path issues. This year's survey is basically the same as the 2005 through 2008 surveys. Questions are grouped into categories: General Business Profile Information, Data Processing, Yields and Yield Loss Mechanisms, Delivery Times, Returns, and Services. Within each category is a multitude of questions that create a detailed profile of both the business and technical status of the critical mask industry. This in combination with the past surveys represents a comprehensive view of changes in the industry.

7488-03, Session 1

EMLC09 Best Paper: MAPPER: high-throughput maskless lithography

V. Kuiper, B. J. Kampherbeek, M. Wieland, G. de Boer, G. F. ten Berge, J. Boers, R. J. A. Jager, T. van de Peut, J. J. M. Peijster, E. Slot, S. W. H. K. Steenbrink, T. F. Teepen, A. van Veen, MAPPER Lithography (Netherlands)

Maskless electron beam lithography, or electron beam direct write, has been around for a long time in the semiconductor industry and was pioneered from the mid-1960s onwards. This technique has been used for mask writing applications as well as device engineering and in some cases chip manufacturing. However because of its relatively low throughput compared to optical lithography, electron beam lithography has never been the mainstream lithography technology. To extend optical lithography double patterning, as a bridging technology, and EUV lithography are currently explored. Irrespective of the technical viability of both approaches, one thing seems clear. They will be expensive [1].

MAPPER Lithography is developing a maskless lithography technology based on massively-parallel electron-beam writing with high speed optical data transport for switching the electron beams. In this way optical columns can be made with a throughput of 10-20 wafers per hour. By clustering several of these columns together high throughputs can be realized in a small footprint. This enables a highly cost-competitive alternative to double patterning and EUV alternatives. In 2007 MAPPER obtained its Proof of Lithography milestone by exposing in its Demonstrator 45 nm half pitch structures with 110 electron beams in parallel, where all the beams where individually switched on and off [2].

In 2008 MAPPER has taken a next step in its development by building several tools. A new platform has been designed and built which contains a 300 mm wafer stage, a wafer handler and an electron beam column with 110 parallel electron beams. This manuscript describes the first patterning results with this 300 mm platform.

7488-04, Session 1

JPM09 Panel Overview

K. Kato, Seiko Instruments Inc. (Japan)

No abstract available

7488-05, Session 1

JPM09 Best Paper: Comparison of lithographic performance between MoSi binary mask and MoSi attenuated PSM

M. Yamana, Toppan Printing Co., Ltd. (Japan); M. J. Lamantia, Toppan Photomasks, Inc. (United States); T. Nagatomo, Y. Tonooka, Toppan Printing Co., Ltd. (Japan)

No abstract available

7488-06, Session 2

SMO photomask inspection in the lithographic plane

E. E. Gallagher, K. D. Badger, IBM Corp. (United States); Y. Kodera, Toppan Photomasks, Inc. (United States); J. Tirapu-Azpiroz, K. Lai, S. D. Halle, G. R. McIntyre, IBM Corp. (United States); M. J. Wihl, S. Chen, G. Cong, A. Wieczorek, A. Dayal, KLA-Tencor Corp. (United States)

Source Mask Optimization (SMO) describes the co-optimization of the illumination source and mask pattern in the frequency domain. While some restrictions for manufacturable sources and masks are included in the process, the resulting photomasks do not resemble the initial designs. Some common features of SMO masks are that the line edges are heavily fragmented, the minimum design features are small and there is no one-to-one correspondence between design and mask features. When it is not possible to link a single mask feature directly to its resist counterpart, traditional concepts of mask defects no longer apply and photomask inspection emerges as a significant challenge.

Aerial Plane Inspection (API) and Wafer Plane Inspection (WPI) are two lithographic inspection modes that move the detection of defects to the lithographic plane. API and LPI can be deployed to study the lithographic impact of SMO mask defects. This paper briefly reviews the API and WPI technologies and explores their applicability to 22nm designs by presenting SMO mask inspection results. These results are compared to simulated and wafer print expectations.

7488-07, Session 2

Field results from die-to-model application for mask inspection

L. Faivishevsky, S. Mangan, Applied Materials (Israel)

Die-to-Model (D2M) inspection is an innovative approach to running inspection based on a mask design layout data. The Aera2 D2M concept takes inspection from the traditional domain of mask pattern to the preferred domain of the wafer aerial image. To achieve this, D2M transforms the mask layout database into a resist plane aerial image, which in turn is compared to the aerial image of the mask, captured by the Aera2 optics.

D2M detection algorithm works similarly to an Aerial D2D (die-to-die) inspection, but instead of comparing a die to another die it is compared to the aerial image model. D2M is used whenever D2D inspection is not practical (e.g., single die) or when a validation of mask conformity to design is needed, i.e., for printed pattern fidelity. D2M is of particular importance for inspection of logic single die masks, where no simplifying assumption of pattern periodicity may be done. The application can tailor the sensitivity to meet the needs at different locations, such as device area, scribe lines and periphery.

In this paper we present field testing results of the D2M mask inspection application at mask shops. We describe the methodology of using D2M, and review the practical aspects of the D2M mask inspection.

7488-08, Session 2

Mask defect auto-disposition using aerial image-based analyzer

J. Park, W. Cho, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

At the most advanced technology nodes, such as 3Xnm and 2Xnm, aggressive OPC and Sub-Resolution Assist Features (SRAFs) are required. However, their use results in significantly increased mask complexity and MEEF (Mask Error Enhancement Factor), making mask defect disposition based on high-resolution mask image more challenging than ever. Therefore, aerial image or wafer plane image based mask disposition becomes essential. As the first step to mitigate such difficulties, new mask inspection technologies that rely on hardware emulation and software simulation to obtain aerial image at the wafer plane have been developed; however, automatic mask disposition based on aerial image is still problematic because aerial image does not give the final resist CD or contour, which are commonly used in lithography verification on post-OPC masks.

An automated mask defect dispositioning system works in both aerial image-to-aerial image and aerial image-to-database modes, and can operate on aerial images from both AIMSTM and aerial-image-based inline mask inspection tools. The disposition criteria are primarily based on wafer-plane CD variance. The system also connects to a post-OPC lithography verification tool that can provide gauges and CD specs or generate its own gauges and CD specs based on defect location and litho printing requirements, which are then used in the mask defect disposition.

7488-09, Session 2

Defect printability analysis by lithographic simulation from high-resolution mask images

G. Chen, Brion Technologies, Inc. (United States)

High resolution photomask inspection has been a critical tool in the lithographic manufacturing process. However, with advances of low-k1 lithography and aggressive OPC masks, it is increasingly difficult to judge the printability of defects detected by traditional high resolution photomask inspection. By simulating aerial images and resist contours from high resolution mask images, it is possible to separate lithographically-significant mask defects from those that are not.

We have developed this functionality, Mask-LMC, with mask images from a sub-200nm wavelength mask inspection system. Both die-to-die and die-to-database inspection modes are supported and both transmitted and reflected images are utilized. The first step of the process is to recover the patterns on the mask from high resolution T and R images by de-convolving inspection optical effects. This step uses a mask reconstruction model, which is based on rigorous Hopkins-modeling of the inspection optics, and is pre-determined before the full mask inspection. After mask reconstruction, wafer scanner optics and wafer resist simulations are performed on the reconstructed mask, with a wafer lithography model. This step leverages Brion's industry-proven, hardware-accelerated LMC (Lithography Manufacturability Check) technology. Existing litho process models that are in use for Brion's OPC+ and verification products may be used for this simulation. In the final step, special detectors are used to compare simulation results on the reference and defect dice. We have developed detectors for contact CD, contact area, line and space CD, and edge placement errors. We have tested Mask-LMC on several 45nm- and 32nm-node test masks and production masks. The simulated defect CD have been compared against AIMS measurements and found to be accurate.

In summary, working together with a high resolution mask inspection system, Mask-LMC is a valuable tool for finding wafer printing defects on advanced photomasks.

7488-104, Session 2

Printability verification function of mask inspection system

H. Tsuchiya, M. Yamabe, M. Tokita, K. Takahara, Association of Super-Advanced Electronics Technologies (Japan); K. Usuda, NuFlare Technology, Inc. (Japan); F. Ozaki, N. Kikuiri, Advanced Mask Inspection Technology, Inc. (Japan)

In the effort to continuously utilize ArF lithography deriving maximum performance, various schemes such as OPC and SRAF are added to a mask. As the demand for forming a minute pattern on the mask has been so strong as to push to the limit of pattern forming precision, the dimension of pattern defect and that of pattern edge roughness have become almost the same.

In addition to the conventional demand for high sensitivity with which the mask inspection system detects the minute size defects, capability to extract true defects from wide variety of patterns that should not be counted as defects (pseudo/nuisance defects) has been demanded. It is particularly necessary to ascertain suppression of MEEF expansion incurred by such effects as combinations of pattern edge roughness of a main pattern and defects of SRAF.

To deal with the situation, a new method to detect defects using simulated wafer aerial images or wafer resist images is being developed. For that purpose, getting precise mask images and high-speed-and-high-accuracy calculation technical capabilities are indispensable.

Association of Super-Advanced Electronics Technologies (ASET), Japan, started a 4-year project to reduce the mask manufacturing cost and turn-around-time (TAT) by optimizing integration of mask data processing (MDP), mask writing, and mask inspection since 2006, with a support from the New Energy and Industrial Technology Development Organization (NEDO), Japan. A printability verification function is one of the themes and ASET has been evaluating Brion's Lithography Manufacturability Check (LMC) technology as a candidate to be used for that function.

For getting precise mask images, NuFlare technology, Inc. (NFT) has been developing NPI-5000 PLUS mask inspection systems which is able to obtain precise mask images using 198.5 nm in transmission and reflection

modes simultaneously. The 198.5 nm wavelength has a feature very close to that of the scanner (193nm). For high-speed-and-high-accuracy calculation, Brion technologies has been developing computational lithography technology which can estimate precise mask pattern shapes from real mask images and simulate precise lithography process. NFT and Brion are jointly developing mask image based printability verification function combining their respective technologies and the result of ASET research.

This report describes the defect detection results and introduces the developed mask inspection system with the printability verification function.

7488-11, Session 3

Using metrology capabilities of mask inspection equipment for optimizing total lithography performance

S. Tamamushi, N. Takamatsu, NuFlare Technology, Inc. (Japan)

The demand for aggressive image placement accuracy and the CD uniformity for each generation is being increasingly accelerated by DPT deployment.

Both IP and CDU required for 32nm hp generation is 0.9nm as shown in ITRS road map.

It is getting evident that the error factors exist in the areas other than mask writer because IP accuracy and the CD uniformity of mask writer have been remarkably improved for each generation.

It is feasible to correct those errors with mask writer if the error factors are reproducible, and the natures of them are not pattern dependent.

It is also feasible to correct them with the mask writer when there is a clear rule even if they are pattern dependent, like resist charging effect.

Thus, it is not possible to correct them with writer when the rule is not clear or there is no reproducibility.

The method of the correction with the scanner is in effect devised by obtaining the CD and IP maps of the each mask after the mask pattern is drawn by DPT in practical use.

We are developing a technology that generates CD and the IP maps for each mask from the image data of inspection equipment with the ultimate goal of “in-die overlay improvement” optimizing Scanner as well as Writer performances.

Laser interferometer installed in the scanner of our inspection equipment has the same degree of accuracy as the metrology device.

The location information with high accuracy can be added to the image data by acquiring the signal of the image sensor synchronizing with the clock generated from this laser interferometer.

We evaluated the positional measurement function by using NPI systems with the evaluation mask, we report on the result and our assessment.

7488-12, Session 3

High-MEEF reticle inspection strategy

A. Tchikoulaeva, AMD Saxony LLC & Co. KG (Germany); R. Kirsch, AMD Fab36 LLC & Co. KG (Germany); S. Winkelmeier, Advanced Mask Technology Ctr. GmbH & Co. KG (Germany)

Reticle defectivity has been a widely discussed topic in the last few years primarily due to ongoing haze issues but also because of the increasing number of the qualification methods available in the fab. Mask shops are taking a closer look at the alternatives to the direct reticle inspection [1], making a step towards wafer inspection as a valid option for reticle qualification.

High MEEF patterns represent the most interesting and challenging case study due to potentially comparable sensitivity performance of the wafer inspection and reticle inspection tools as reported in [2]. A reticle with programmed defects in different environments was used to define detection limits, capture rates and noise levels for both direct reticle inspection and the inspection of the wafer print. Reticle inspection was performed using KLA587 tool. For the inspection of the wafer prints two most advanced DUV inspection tools were used. Defect sizes were defined on the reticle and on the wafer using SEM CD tools. These data were complemented by AIMS measurement which is the only available defect disposition tool at the mask shop today. Correlation between actual wafer CD and AIMS deviations was examined.

The focus of this study was to identify gaps and opportunities existing in the reticle qualification chain starting with the outgoing qualification at the mask shop and continuing during the reticle lifetime in the fab. Results and conclusions of this investigation will be presented and discussed in conjunction with the prospects and possible modifications of pursued approach for 45nm and the future nodes.

[1] K.Kimmel et al. “Optimal Mask Characterization by Surrogate Wafer Print (SWaP) Method”, Proc. of SPIE BACUS 2008, to be published.

[2] A. Poock et al. “Wafer fab mask qualification techniques and limitations”, Proc. of SPIE BACUS 2006, vol. 6349.

7488-13, Session 3

New database mode inspection capabilities for advanced reticles

A. W. Goonesekera, P. Lim, B. Mu, A. Dayal, KLA-Tencor Corp. (United States)

Semiconductor device fabricating technologies are rapidly advancing towards 32nm node and beyond. Reticles at these device nodes are designed with tight critical dimension (CD) specifications and sub-resolution features. Inspection tools capable of detecting both pattern and contamination defect types are critical for high yield of devices at these design nodes. To meet this challenge, KLA-Tencor has developed dual mode database (DB) inspection capability on the new TeraScanXR reticle inspection tool at high throughput and sensitivity. The new concurrent transmitted and reflected database inspection algorithm (UXRdbTR) provides capability to find pattern and contamination defects in a single pass at substantially improved speed. The wafer plane inspection algorithm (WPIdbTR) provides capability to capture defects that only have printability impact at equally high throughput. Additionally, most recently developed Aerial plane database inspection algorithm (APIdbTR) provides the capability to capture defects that have a potential to print on the wafer. All three database inspection modes are available at 72 nm and 90 nm pixel views. Inspection results with the UXRdbTR algorithm demonstrate improved sensitivity and good inspectability at throughput up to 4 times faster than TeraScanHR system inspection. This paper will focus on inspection results from a variety of advanced reticles inspections covering the 32nm and 45nm nodes.

7488-14, Session 3

Simulation-based mask defect repair verification and disposition

E. G. C. Guo, C. Liu, S. Zhang, S. Qian, Semiconductor Manufacturing International Corp. (China); G. Cheng, L. Zhou, L. Li, Anchor Semiconductor, Inc. (China); Y. Chen, C. Hsiang, Anchor Semiconductor, Inc. (United States); G. Zhang, Anchor Semiconductor, Inc. (China); B. Su, Anchor Semiconductor, Inc. (United States)

As the industry moves towards 45nm and 32nm technology nodes, the mask inspection, with increased sensitivity and shrinking critical defect size, catches more and more nuisance and false defects. Increased defect counts pose great challenges in the post inspection defect

classification and disposition: which defect is real defect, and among the real defects, which defect should be repaired and how to verify the post-repair defects.

In this paper, we report a methodology using SEM mask defect images, as well as optical inspection mask defects images (only for verification of phase and transmission related defects) in defect verification and disposition, in particular, in post repair defect verification to address one of the challenges.

We will demonstrate the flow using 45nm programmed mask defects. First, 20 types of defects, which include typical mask defects, as well as some typical defects in real circuit environments, were designed with up to 30 different sizes for each type. The SEM image was taken for each programmed defect after the test mask was made. Selected defects were repaired after SEM images and wafer printing as defect printability reference.

A software tool is used to extract edges of the SEM images and converted extracted edges into polygons in GDS format. Then, the converted polygons from the SEM images were filled with the correct tone to form mask patterns and were merged back into the original design GDS. The purpose of the merge is for contour simulation, since normally the SEM images cover only small area (~1 m) and accurate simulation requires including larger area of optical proximity effect. With lithography process model, the resist contour of area of interest (AOI-the area surrounding a mask defect) can be simulated. If such complicated model is not available, a simple optical model can be used to get aerial image intensity of AOI. With build-in contour analysis functions, the software can easily compare the contour (or intensity) differences between real mask (with defect) and ideal mask (without defect). With user provided judging criteria, software can be easily disposition the defect based on contour comparison. In addition, process sensitivity properties, like MEEF and NILS, can be ready to obtain in the AOI with a lithography model, which will make mask defect disposition criteria more intelligent.

7488-15, Session 3

Challenging defect repair techniques for maximizing mask repair yield

A. D. Garetto, Carl Zeiss SMT Inc. (United States); J. Oster, NaWoTec GmbH (Germany); M. Waiblinger, Carl Zeiss SMS GmbH (Germany); K. Edinger, NaWoTec GmbH (Germany)

It is critical in today's economic climate to improve mask yield as material, processes and tools are more time and cost involved than ever. The driving force behind this increase in cost is not only due to the push towards smaller features, but also the need for the mask house to maximize overall mask yield. One way to directly improve mask yield is to increase the range of mask defects that can be repaired and the effectiveness with which these defects can be repaired. This increases the defect repair yield which in turn contributes to the overall mask yield.

The Carl Zeiss MeRiT MG 45 is the most comprehensive and versatile repair tool available for production. With the ability to repair both clear and opaque defects tool transfer and setup time is saved for masks with multiple defect types. Without the necessity for multiple repair tools, the cost of ownership is also reduced. The MeRiT MG 45 has the capability to return to a repair site multiple times without degradation of the optical properties. This allows human errors to be corrected and challenging repairs to be conservatively approached increasing overall mask house productivity.

An example of a 248 nm 6% double bridge defect is used to demonstrate the ability to return to a repair. The clear regions on a double bridge were purposely etched too wide leaving the opaque lines thin. AIMS™ data was obtained and the defect was returned to the MeRiT MG 45 in order to widen the lines with a deposition. AIMS™ data was again acquired and intensity profiles for the etch step and the subsequent deposition step compared. The double bridge is obvious after the etching step with the center line printing 27.6% undersized at focus. The neighboring clear spaces and opaque lines are also affected and the results are quantitatively summarized. After the deposition the repair is indistinguishable from the neighboring lines and spaces and the center line is less than 1% difference in CD at focus.

The ability to perform multiple repair attempts with the MeRiT MG 45 without degrading the optical properties of the neighboring area has been demonstrated. This technique has been successfully applied to production masks at customer sites allowing the MeRiT MG 45 to increase defect repair yield saving time and money.

7488-16, Session 3

Expanding the lithography process window (PW) with CDC technology

S. Wang, C. Kuo, Y. Chen, Powerchip Semiconductor Corp. (Taiwan); G. Ben-Zvi, Pixer Technology Ltd. (Israel) and Carl Zeiss SMS GmbH (Germany); E. Graitzer, A. Cohen, Pixer Technology Ltd. (Israel)

The continuous shrinking of the semiconductor device nodes requires tough specs of CD uniformity which result in narrowing of the lithography process window. Finding methods for expanding the process window will enable to continue manufacturing at least one more generation using the existing litho equipment.

In this paper we will demonstrate a way to expand the lithograph process window by using the Carl Zeiss CD control (CDC) Technology.

A production memory product in PSC fab P1/2 showed reduced yield due to reduced process window in Poly layer. A close investigation in the fab showed CD non uniformity of 3.95nm 3S and 6.5nm Range in this layer.

A CDC process to improve the CDU was applied by the Carl Zeiss CDC200 tool.

Post CDC results show that CDU 3S has reduced to 1.94nm (53% improvement) and 3.7 nm Range (43% improvement).

Further assessment of this layer process window showed an increase of DOF from 0.15 um pre CDC to 0.3 um post CDC and exposure latitude increase from 18.7% pre to 26.7% post CDC.

To summarize our findings, applying the CDC process to the problematic layers allowed to increase the PW in both DOF and exposure latitude by improving the CDU of the layer. This resulted in better yield of this product.

7488-17, Session 4

Post-exposure bake tuning for 32-nm photomasks

A. E. Zweber, IBM Corp. (United States); T. Komizo, Toppan Photomasks, Inc. (United States); J. P. Levin, J. Whang, IBM Corp. (United States); S. Nemoto, S. Kondo, Toppan Photomasks, Inc. (United States)

In optimizing E-beam resist process conditions for photomask lithography, the primary performance measurements for optimization are resolution, critical dimension uniformity (CDU), line edge roughness (LER), through-pitch, and linearity. Optimization of the process can involve many variables including e-beam writer, resist type, bake condition, develop condition, and etch condition. Through technology nodes, one parameter that has consistently shown a critical impact on these factors is the post exposure bake (PEB) condition. With 32nm e-beam resist technologies having reduced temperature sensitivity, this paper investigates the current impact of PEB conditions.

The purpose of the PEB is to activate internal chemical reactions and to enable photoacid diffusion within the photoresist film rendering contrast between the exposed and unexposed regions. The PEB temperature, duration, and environment can influence the outcome of the chemical

reaction and the acid diffusion. The PEB temperature must at a minimum be high enough to reach the reaction activation energy. The PEB duration specifically for mask materials must be long enough for the mask to reach the steady state temperature. Finally, the PEB environment should have controlled surrounding flow to improve uniformities. This paper will study the influence of PEB temperature, duration and environment on 32 nm positive and negative tone resists by reporting and analyzing the primary performance measurements: resolution, resist feature profiles, though-pitch, linearity, global CDU, and LER. The resolution will be determined with top-down SEM imaging and scatterometry, while the resist profiles will be examined with scatterometry and cross-section SEM imaging. The resist profiles will illustrate PEB impacts on secondary profile features, such as resist footing and t-topping, where the secondary profile features will be related to resist CD measurements and transfer during etch to the final performance measurements. The global CDU and feature LER will be resolved on a low density patterned mask using an 11x11 array of lines and spaces with isolated and nested proximities, where through-pitch and linearity are measured on the same mask in resist and post etch. The PEB assessment will be summarized with emphasis on the relationship of PEB temperature, duration, and environmental interaction and dependencies between the positive and negative tone resists.

7488-18, Session 4

Reduction of local CD-linewidth variations in resist develop through acoustic streaming

G. Lee, HamaTech APE GmbH & Co. KG (Taiwan); P. Dress, HamaTech APE GmbH & Co. KG (Germany); S. Chen, U. U. Dietze, Hamatech USA Inc. (United States)

According to the ITRS roadmap for lithography (2008 edition), the CD uniformity requirement of optical masks beyond 32nm HP is less than 1.5nm (3 sigma). Especially for double patterning lithography, not only the global uniformity but also the local uniformity is of very high concern. Therefore it is imperative that the develop process will yield CD-linewidth control independent of pattern sizes or pattern loading, following precisely those pattern size image correction strategies applied during mask writing (e.g. proximity and fogging correction). Conventional methods of resist develop cannot meet such requirement without negative side affects (e.g. increased dark loss, pattern collapse, global CD-uniformity degradation and/or defect issues). The ASonic® nozzle developed by HamaTech APE combines the very favorable dark loss, defect and global CD-linewidth control benefits of a fast and uniform low impact initial develop dispense (surface wetting), with an enhanced developer agitation through acoustic streaming, which provides improved local CD-control independent of pattern size and loading.

The principle functionality of the ASonic® nozzle is described. Developing loading effect is examined with various conditions and CD linearity, proximity and CD uniformity are also verified.

7488-19, Session 4

Plasma characterization of Tetra III Cr etch system

M. Grimbergen, K. Yu, T. Leung, M. Chandrachood, A. Ouye, S. Singh, I. M. Ibrahim, A. Kumar, Applied Materials, Inc. (United States)

This paper describes plasma characterization results obtained using the Langmuir probe, emission spectroscopy and OnWaferTM temperature sensor array. The data sheds light on electron temperature, electron density, ion density and with actinometry we can estimate the concentrations of species in the plasma. The plasma optical spatial uniformity can be monitored using new endpoint optical ports near the mask. Spatial uniformity optical emission data will be presented to highlight the changes observed with the new configuration.

In a typical inductively-coupled plasma (ICP) chamber both ions and neutral radicals are created. In a chlorine-oxygen plasma, both ions and neutrals participate in chrome etching, but the ions attack the photoresist (PR) masking layer, reducing the selectivity. By introducing a uniquely designed third electrode, the ion flux to the masking layer can be reduced. With reduced flow of ions, the Cr etch rate is reduced, but the PR etch rate is reduced even further. This has the benefit of increasing the selectivity and improving etch bias. In addition, the etch uniformity is notably improved.

7488-20, Session 4

Behavior of the molybdenum silicide thin film by 193-nm exposure

S. Yang, K. Nam, S&S TECH (Korea, Republic of); H. Cha, J. Ahn, Hanyang Univ. (Korea, Republic of)

In order to embody high resolution at 32 nm and below, molybdenum silicide (MoSi) phase shift mask (PSM) is essential which is beneficial when using this material in the ArF lithography process, generally. But some problems reported from for the variation of PSM characteristics which are transmittance variation and chemical durability. This characteristics change became an issue for the yield drop of the semiconductor device manufacturing. So we study the behavior of the MoSi PSM thin film in the view point of the ArF laser exposure in this paper.

Firstly, the problems of the MoSi thin film by the 193 nm exposure are observed. From the result, 0.52 % of the transmittance changed by the 193 nm irradiation with 10 kJ of energy. Accordingly, MoSi thin film characteristic is degraded by the ArF laser irradiation. The reason for the transmittance degradation by irradiation for the MoSi thin film is analyzed. And we find that the oxygen is activated by the ArF laser and this activated oxygen is penetrated to the MoSi thin film. So the transmittance is increased by the penetrated oxygen. And then we investigate the improvement scheme for the MoSi thin film's irradiation characteristic. Firstly, the composition of the thin film is changed by the reactive gas ratio change, new reactive gas application in the sputtering process. Also, the new transition metal is added to the MoSi thin film like transition metal. And then, modified MoSi thin film's exposure characteristic is evaluated by the transmittance and chemical durability for the H2SO4 and SC-1 after 193 nm laser irradiation. Consequently, modification of the composition for the MoSi thin film by the reactive gas and transition metal helps for the improvement of the irradiation characteristic for the MoSi thin film.

7488-21, Session 4

Mask performance improvement with mapping

J. H. Peters, C. S. Utzny, E. Cotte, Advanced Mask Technology Ctr. (Germany)

Current high-end chips require an extremely precise fabrication of lithographic masks. Some of the most critical parameters are the placement of structures on the masks as well as their dimensional tolerances. Improving these two key parameters has always been one of the central objectives of the Advanced Mask Technology Center (AMTC). To this end, the AMTC has complemented its process development by a set of enhancement schemes which are used to compensate residual process signatures. In this paper, improvements achieved in the area of CD uniformity (CDU) and pattern placement are shown. The correction schemes take first principle considerations as well as empirical findings into account. Based on this, a set of design and process parameters is used to determine the spatial corrections which will optimize mask quality parameters. This enables the AMTC to tailor the writing parameters to the needs of each mask design. Latest results for the 32nm technology show that values as low as 5nm 3-sigma registration and 3nm 3-sigma CDU can be reached at the same time.

7488-22, Session 4

Enhanced laser writing techniques for bimetallic grayscale photomasks

G. H. Chapman, J. M. Dykes, Simon Fraser Univ. (Canada)

Under laser exposure bimetallic thin films of Bi/In and Sn/In oxidize becoming transparent. By controlling the laser power, direct-write binary and grayscale photomasks have been produced with the mask's transparency (optical density, OD), ranging between ~3.0 (unexposed) to <0.22 OD (fully exposed). Precise 3D micro-optics require both high vertical accuracy, graylevels over large OD changes, and precise lateral pattern creation. To achieve this result, an OD measurement system has been developed that provides real-time OD measurements while the masks are being written. Raster-scanning pattern lines using different amounts of overlap, the OD system can determine the effective laser beam spot-size and identify the optimal line-spacing for Bi/In and Sn/In films. The effective spot-size of the laser is ~60% larger for Sn/In relative to Bi/In, likely due to Sn/In's higher thermal conductivity. For mask-writing, the optimal line spacing is dependent upon the laser beam's power distribution profile and heavily influences the writing time of the mask. Using a line-spacing 3-5 times smaller than the effective spot-size, variations in the patterned mask caused by a Gaussian-distributed beam were found to be minimized at the cost of increasing the writing time of the mask by the same factor. Beam-shaping the laser to have a more uniform top-hat distribution allows a line-spacing 1-2 times smaller than the effective spot-size to be used.

With the development of the real-time power and OD measurement system, adjustments are made to an originally open-loop mask-writing system allowing the measurements to control the laser's writing intensity while patterning the mask. Comparing v-groove patterns written on Bi/In and Sn/In films, closed-loop system designs using pre- and post-scanning or on-the-fly OD measurements are examined to determine which approach provides the best accuracy, repeatability and grayscale range, while still keeping the mask-writing time reasonable.

With the development of the closed-loop design, mask patterns consisting of v-grooves, staircases, and micro-lens patterns were produced and measured using three bimetallic film mask-writing systems. First, an open-loop system that does not use any power or OD measurements for controlling the laser. Second, a power-calibrated system where the laser power settings are verified at the end of each patterned line. Lastly, a closed-loop system where the OD of the mask is measured and used to control the laser while it is patterning. Once written, OD scans of the masks determine each system's grayscale accuracy, repeatability, and range. Furthermore, the time taken to produce each of the masks is also measured; identifying each system's effective mask-writing speed. The open-loop mask-writing system is shown to operate the fastest, with the ability to produce up to 64-level grayscale masks, but suffers from issues regarding repeatability with different films. The power-calibrated and closed-loop systems demonstrate superior repeatability but operate at a slower rate due to the added measurement time and reduced writing-velocity, respectively. An added benefit for the closed-loop system is that variations in the OD of the as-deposited film are corrected for and effectively removed by the system allowing for the production of 256-level grayscale masks.

7488-23, Session 5

Lithographic patterning of magnetic recording media

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As the magnetic recording industry approaches a data density of 1 Tbit per square inch, extending the use of conventional continuous granular media has become increasingly difficult due to thermal stability limitations. Lithographically patterned media promises a route to significantly higher densities and has emerged as a front runner to replace conventional media. There are two versions of patterned media: 1) discrete track media (DTM), in which granular media is patterned into individual tracks separated by nonmagnetic material, and 2) bit patterned media (BPM), in which a magnetic film is patterned into single-bit islands. While DTM is simpler to fabricate and integrate, BPM offers more potential density gain. Patterning of BPM requires nm-scale features to be defined over full-disk areas at very high volume and low cost. These requirements have driven the choice of nanoimprint lithography as the only viable option. Master patterns for creating imprint templates are generated by e-beam lithography, and, in the case of BPM, block copolymer self-assembly. Use of these technologies marks a significant departure from the semiconductor industry lithography roadmap; the magnetic recording industry will drive the introduction of these new lithographic methods.

7488-24, Session 5

Nano-imprint lithography: enabling technology for discrete track recording (DTR) media and beyond

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The hard drive business has been fueled by areal density growth for over 40 years. Many technology transitions have occurred within that time that has enabled density growth as high as 100% per year. The fundamentals of recording physics predict that another key technology transition is required to continue that growth. PMR writers with Tunneling GMR readers on continuous media have limited areal density growth potential. Current view is this limit is less than 800 Gb/in2. DTR media promises a boost in areal density ... but how much ... and at what cost? Beyond DTR, bit patterned media (BPM) and energy assisted recording offer further opportunities for density growth. These also require investment in lithographic definition of disk features to be viable. Nano-Imprint Lithography using e-beam masters is being staged to provide the capability for DTR and BPM media track and bit definition. This session is aimed at clarifying the motivation for DTR media and exploring the impact of lithographically defined tracks on the manufacturing of disks.

7488-25, Session 5

High-precision and low-cost lithography for patterned media

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The Magnetic recording industry continues to meet the challenges for areal density growth by innovation. Patterned media is one of the potential paths to extend this growth beyond perpendicular recording. For patterned media to be viable, it is critical to meet stringent lithography requirements and at the same time achieve low cost. Critical dimensions (< 20 nm) and pattern placement accuracies (<5% of bit size) across the full surface of a disk require precision rotating stage electron beam writing, to avoid down-track stitching errors. One particular challenge is beam placement control and stability over long writing times of several days. To achieve low-cost, nano-imprint lithography is essential as it allows leveraging one single master recording into millions of disks through multiple template replicas (100 - 1000) and disk imprints (1000-10000).

We will demonstrate a technique for template replication via nano-imprint lithography. For media fabrication, a key requirement for nano-imprint lithography is to imprint on both sides of the media with high throughput. This is accomplished with a double-sided imprint tool. With high-precision and low cost lithography, patterned media could become the next paradigm in magnetic recording technology.

7488-26, Session 5

Discrete track media: media manufacturing perspective

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Hard Disk Drive (HDD) Industry is considering the use of discrete track recording (DTR) technology to achieve higher recording density for future generations of HDDs. There are numerous challenges to manufacturing discrete track media in a manner that is consistent with the cost-of-ownership model required for the HDD industry. A general overview of the manufacturing steps required for making the DTR media will be presented, and focus will be put on two key technology components for DTR media manufacturing, which are e-beam lithography, and nano-imprint lithography (NIL). These two technologies which have their roots in semiconductor processing, have very different requirements placed on them when applied to hard disk manufacturing. Those differences will be outlined with emphasis on technical requirements and cost-of-ownership model that they must follow in order to be successfully applied to DTR technology.

7488-27, Session 6

Study of program defects of 22-nm nano-imprint template with an advanced e-beam inspection system

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Nanoimprint lithography (NIL) is a candidate of alternative, low cost of ownership lithography solution for deep nano-meter device manufacturing[12]. For the NIL template pattern making, we have been developing the processes with 100keV SB EB writer and 50keV VSB EB writer to achieve the fine resolution of near 20nm[1-7]. However, inspection of nanoimprint template posed a big challenge to inspection system due to the small geometry, 1x comparing to 4x of Optical mask and EUV mask. Previous studies of nanoimprint template inspection were performed indirectly on a stamped wafer and/or on a round quartz wafer[13]. Electron beam inspection (EBI) systems have been widely used in semiconductor fabs in nanometer technology nodes. Most commonly EBI applications are electrical defects, or voltage contrast (VC) defects detection and monitoring.[8] - [11].

In this study, we used a mask EBI system developed by Hermes Microvision, Inc. to directly inspect a NIL template with line/space and hole patterns half pitched from 22nm to 90nm and with program defects sized from 4nm to 92nm. We inspected the template at two template manufacturing steps: after quartz etch with chromium (Cr) hard mask and after the Cr hard mask has been removed. Capability of inspection with 10nm pixel size has been demonstrated and capability of capturing program defects sized 12nm and smaller has been shown. This study proved the feasibility of EBI as inspection solution of nanoimprint template for 22nmHP and beyond.

7488-28, Session 6

A cost of ownership model for imprint lithography templates for HDD applications

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Cost of ownership projections have often been used to determine the potential costs associated with the introduction of novel lithography applications. While they are often controversial and their accuracy or usefulness are a function of the validity of the assumptions used to build the model; they provide insight to the real technical issues as well as the critical areas that required the most financial and technical resources for success and profitability. This paper will provide a first look at the key technical and financial challenges of using imprint technology the fabrication of hard disk drives. The focus will be on the template cost of ownership, pattern generation time, inspection and repair and yield.

7488-29, Session 6

High-resolution e-beam repair for nano-imprint templates

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UV nanoimprint lithography (UV-NIL) is a high-throughput and cost-effective patterning technique for complex nano-scale features and is considered a candidate for the 22nm node and beyond. Using state-of-the-art variable shaped beam (VSB) pattern generators and commercially available resists templates with full-field flash gate layers have already been demonstrated. The results approached the specifications for the 32nm node requests in terms of resolution, line edge roughness, placement and uniformity [1]. Recent improvements of template patterning using a VSB tool even showed the capability towards full-field templates for device manufacturing below 32nm half-pitch [2].

In UV-NIL high-resolution template patterns are replicated into a monomer layer deposited on a substrate. Pattern defects resulting from e-beam patterning and subsequent pattern transfer processes significantly contribute to imprint defectivity [3]. Thus inspection and repair are two essential components of the template fabrication chain. E-beam repair with its advantages of precise beam placement using fine resolution images and damage free repair by e-beam induced chemical reactions is a promising repair technology for high-resolution imprint templates. Recently, we demonstrated gas assisted e-beam repair of UV-NIL templates by applying recipes specifically tailored for NIL repair requirements [4].

In this work an e-beam repair test stand with improved beam and stage stability has been used. We investigated the repeatability of 3D pattern reconstruction with main focus on the height control of the deposition and etch processes. Additionally, we examined the resolution capability of the improved hardware on selected programmed defects in order to address possible requirements for imprint repair tools of future generation nodes. Repairs of programmed defects with different types and sizes were made to a fused silica mask of the 65mm form factor and repair results were analyzed by SEM inspection. Imprints were performed to examine the stability of the repaired defects.

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7488-30, Session 6

Duplicated quartz template for 2.5-inch discrete track media

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Nano Imprint Lithography (NIL) process has been proposed as a method of making a Discrete Track Media (DTM) for the next generation HDD. The fabrication of the patterned template is one of the key elements in NIL processes. Most of the past reports have discussed the performance of DTM template with narrow band lithography patterns and there were few reports on the full-surface patterned templates.

In this paper, the quartz template patterned for 2.5 inch full surface DTM is discussed. A full surface (R=14-31mm) patterned Si master with Track Pitch (TP) 125nm was fabricated for 2.5 inch Discrete Track Media (DTM) using R-theta Electron Beam (EB) writing and Reactive Ion Etching (RIE). The pattern was successfully transferred from a Si master to quartz templates by the UV-NIL process without hard mask. The shape of the quartz template pattern was rectangular and the taper angle of the pattern is approximately 75 degree. The pattern height of the quartz template was approximately 60nm with 48 nm of the line width of half pattern height. The pattern height of the quartz template fabricated in this process is very uniform over the full surface and the measured at each 4 points of the inner and outer diameter area was less than 1.5nm.

The UV-NIL process described in this report does not use any hard mask layers (such as Cr) on the quartz wafer. The UV-NIL resist was directly coated on the quartz wafer, and the resist was patterned by UV-NIL process. The advantage of this process is the elimination of the coating, etching and removal of the hard mask layer. On the other hand, this process requires the UV-NIL resist with high etching resistance and the UV-NIL resist synthesized the monomer structures were newly developed for this purpose. The quartz template with TP of 120nm and pattern height of 60nm was successfully fabricated using the UV-NIL resist with etching selectivity of 2.5. The fabricated pattern had the rectangular shape and good pattern height uniformity, while the pattern fabricated with UV-NIL resist of etching selectivity of 1.6 was below 60 nm in the pattern height and the pattern shape was triangular. We have succeeded to obtain the quartz template over full surface by using the new resist with etching selectivity of 2.5.

The DTM templates pattern with higher density was investigated. The quartz template with TP 75nm was fabricated with the combination of the UV-NIL resist usage and an improved RIE coition. The pattern height of 60nm with approximately 35 nm of the line width of half pattern height was fabricated on the quartz templates. The shape of the quartz template pattern was rectangular and the taper angle of the pattern is approximately 80 degree.

7488-31, Session 6

Requirements in mold manufacturing for pattern media

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Obducat is supplier of lithography solutions for manufacturing and replication of advanced micro- and nano- scale structures.

We provide viable and cost-effective lithography solutions that will give a competitive edge to our customers, enabling them to deliver break-through applications and achieve improved profitability and success. Obducat is the first company to commercialize Nanoimprint Lithography (NIL) and Electron Beam Recorder (EBR). Today Obducat is the market leader with the largest installed base worldwide of NIL.

The increased requirement for a higher storage capacity in hard drives generates a need for a new manufacturing technology that enables sub 30 nm feature sizes. Current magnetic media technology is facing difficulties to continue to higher surface densities due to the super-paramagnetic limitations. By using isolated magnetic domains to store the data makes it possible to overcome these limitations. The Discrete Track Recording (DTR) approach is expected to enable storage densities well beyond 1 Tbits/in2.

Manufacturing of Pattern Media will require direct-write lithography system capable of creating a master mold, which can be used in replication on final media by Nano imprint lithography (NIL). The imprint process replicates the original pattern exceptionally cost efficient, making mass production of magnetic media possible. However, realization of pattern media offers challenges.

This talk discusses the requirements for mold/stamp fabrication and qualification methods to be used for high-volume DTR replication with NIL. It will also clarify the challenges and solutions that involve both Electron Beam Recording, imprint lithography and their implications on the downstream processes in HDD media manufacturing.

7488-32, Session 7

Source-mask co-optimization (SMO) using level set methods

V. L. Tolani, P. Hu, D. Peng, T. Cecil, R. Sinn, L. Pang, B. E. Gleason, Luminescent Technologies, Inc. (United States)

Masks computed by use of Inverse Lithography Technology (ILT) are being increasingly used in 32nm and below nodes for their significantly improved litho performance even beyond model-based OPC. This technique poses the design of photomasks as an inverse problem and then solves for the optimal photomask using rigorous mathematical approach. One such approach is the level set based method wherein a level set function m(x,y) represents the contour of the mask. The zero level set m(x,y)=0 then represents the actual mask at a given instance. The same level-set approach has now been extended to determine the most optimized source (p,q) for a given target.

Optimizing a source based on target information alone could be misleading since the target does not have, for example, assist features that would otherwise improve printability of isolated or semi-isolated features in random logic or SRAM patterns. Co-optimizing the mask with the source enables the source to evolve where the mask otherwise would not be able to contribute, for example in tight and forbidden pitches.

Using Level Set Methods, co-optimizing the source and mask for a given target is a natural extension of optimizing the mask alone in ILT. The same cost function, say maximizing DOF, which is used to compute the ILT mask can be used for the source as well. This approach enables accurate and fast computation of the optimized source and mask for given set of patterns and could also utilize running on a distributed computing environment.

7488-33, Session 7

Sampling design for the joint source-mask optimization

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In comparison to the mask optimization problems of traditional OPC or inverse lithography, the source-mask optimization (SMO) introduces additional 100 to 1000 source variables. This limits the total area under consideration to hundreds of square microns, which cannot possibly cover the whole chip.

The design must be sampled in a clever manner to account for difficult to print and repeated regions. We compare various design sampling strategies which are capable of capturing all essential proximity situations.

7488-34, Session 8

Study of litho-friendly layout design by source mask optimization using inverse lithography technology

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Source and Mask co-Optimization (SMO) plays an increasingly important role in the RET required to continue shrinking designs in the low-k1 lithography regime. It is essential to obtain an acceptable process window (PW). In memory device, the critical layers which include dense patterns with minimum pitch determine the process margin dominantly. Therefore, the layout design should be optimized in terms of SMO so as to maximize whole PW. In this paper, the layout for lithography-friendly design may be searched by SMO method which Inverse Lithography Technology (ILT) provides. For the smart searching, the dimensions of pattern topology are parameterized with minimum design constraints. The maximized PW is obtained at each parameterized layout. Consequently, the final dimension may be determined by the comparison of each maximized PW. The optimized design corresponding to SMO results should be verified by the wafer printing test. As further works, the optimal cell design can be employed in terms of lithography process.

7488-35, Session 8

Subresolution assist features placement using cost-function-reduction method

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Inverse lithography technique (ILT) has been proposed as an option for Resolution Enhancement Technology (RET) to cope with the severe optical distortions in sub-wavelength lithography. However, the existing optimized mask usually is always too complex for mask manufacturing and inspection. Although Optical Proximity Correction (OPC) is one of the most important techniques widely used, the current methodologies of sub-resolution assist features (SRAFs) placement can be rather primitive and extremely pattern-dependent. Recently, a few works use ILT to create SRAFs automatically for model-based OPC optimization. In this paper, we use a newly proposed ILT algorithm-Cost-function-Reduction method (CFRM) to create SRAFs. CFRM is proved to be much effective and efficient than gradient-based algorithm and traditional simulated annealing method. We improve CFRM to be an initial condition independent algorithm (ICIA) by tuning running parameters of CFRM. Starting from random generated initial patterns, the optimized final mask patterns are quite similar and are almost determined by first a few iterations. Mathematically, CFRM can be considered as a rough but efficient implementation of densification and dynamic canonical descent (DCD) proposed by K. Bousson which has been proved to be effective in finding global minimum. Based on these stated properties, a fast and effective SRAF algorithm is proposed to handle SRAF placement. This method can be applied to various mask technologies (binary, APSM, 6%EPSM, 18%EPSM and strong APSM) and partial-coherence image model.

7488-37, Session 8

SRAF enhancement using inverse lithography for 32-nm hole patterning and beyond

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At 32 nm node and beyond, one of the most critical processes is the holes patterning due to the Depth of Focus (DOF) that becomes rapidly limited. Thus the use of Sub Resolution Assist Features (SRAF) becomes mandatory to keep DOF to a sufficient level through pitch.

SRAF are generally generated using Rule Based OPC with a different cleaning step to avoid risk of SRAF printing or conflict with main feature. One of the key challenges of using such a technique is the ability of placing SRAF in random holes features. The rule based approach cannot treat all the configurations resulting in non-optimal SRAF placement for certain main feature. On the other hand, Inverse Lithography has shown the ability of generating SRAF at the ideal size and position (theoretically) and interest of this technique has been proven experimentally. Nevertheless, this kind of technique is not yet ready for maskshop due to MRC limitation caused by the pixilated SRAF output, and the important mask writing time due to the shotcount.

In this paper we propose to make a comparison of the two approaches on random 2D features. We will see that Inverse Lithography permits to keep a sufficient DOF on 2D features configurations where Rule based appears to be limited. Simulated and experimental results will be presented comparing Rule based, Ideal and MRC constraints SRAF as well as Runtime performance on hole patterning using such techniques.

7488-38, Session 8

Model-based assist feature placement for 32-nm and 22-nm technology nodes using inverse mask technology

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Inverse lithography has been long known to provide a true mathematical solution to the mask design problem. In this work, we derive the mathematical inversion of a partially coherent optical imaging system under several candidate cost functions like aerial image fidelity, contour fidelity, process window maximization, and ILS maximization. The work builds on the inverse imaging approach outlined in [1] which used a simplified coherent illumination model. Here, we extend the idea to more realistic imaging conditions including off-axis illumination, resist stack effects, polarization, vector imaging, and variable threshold resist models. Our treatment can handle both conventional as well as pixilated source shapes, which are gaining much popularity for the upcoming 22nm nodes. The inverse mask technology (IMT) framework is implemented in Proteus, and is vastly optimized for speed and efficiency.

The latter half of our paper focuses exclusively on the application of the inverse lithography framework to model-based assist-feature placement. Our suggested work-flow (see [2]) does an IMT-based MBAF placement followed by an integrated OPC and AF printability step. In this work, we explore the effect of higher order kernels on the inverse mask field for conventional, parametric, and pixilized source shapes. We also study the effect of these kernels on the final AF placement as well as the focus and exposure latitudes. The proposed AF placement framework is extended to both contact and line space type patterns. Finally, we report our results on the process window improvements using inverse-AF at 32 and 22nm technology nodes.

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7488-39, Session 8

Model-based assist features

B. Yenikaya, A. Sezginer, Cadence Design Systems, Inc. (United States)

We present a model-based method of generating and optimizing sub-resolution assist features. Assist feature generation is based on a focus sensitivity map derived from a cost function that minimizes the variations in the printed pattern with respect to focus change. We also demonstrate a method to generate mask-friendly SRAF polygons from the focus sensitivity map. After model-based placement, assist features and the main polygons are optimized together by moving their edge segments. The goals of the optimization are:

1.The printed pattern matches the target layout at best focus;

2.Variations in the printed pattern with respect to focus change are minimal;

3.Assist features or side lobes do not print; and

4.Mask polygons obeys manufacturability rules.

The image is calculated on a 2-D grid when enforcing the condition that assist features and side-lobes do not print.

This approach is significantly faster than inverse lithography solutions and suitable for full chip optimization. We demonstrate superior process window for contact layer at 45 nm node and below.

7488-95, Session 8

Inverse lithography (ILT) mask manufacturability for fullchip DRAM production

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Improvements in resolution of exposure systems have not kept pace with increasing density of semiconductor products. Alternatives such as EUV or high-index optical materials have not developed at the pace originally forecasted, so for the next few years we must rely on 193 nm systems using water immersion. In order to keep shrinking circuits using equipment with the same basic resolution, lithographers have turned to options such as double-patterning, and have moved beyond model-based OPC in the search for optimal mask patterns. Inverse Lithography Technology (ILT) is becoming one of the strong candidates for 32nm and below low-k1 lithography regime. It enables computation of optimum mask patterns to minimize deviations of images from their targets not only at nominal but also over a range of process variations, such as dose, defocus, and mask CD errors.

The computation of ILT mask usually starts with the calculation of an optimized contoured mask which if simply manhattanized (converted to XY segments) could seem to be very complicated. In a prior publication [1], it has been shown that the Inverse Synthesizer (IS) product has the capability to adjust for mask complexity to make it more manufacturable while maintaining the significant litho gains of nearly ideal ILT mask. Further improvements will be made to realize manufacturability of these masks at fullchip levels. This includes enhancements to mask fracturing and jog-alignment algorithms, write-time improvements, creating new and simpler MRC rules, hard and soft-defect inspection setups, high pattern fidelity and production-worthy defect and throughput performance demonstrated by the mask shop. Overall, these improvements are projected to make fullchip ILT masks more manufacturable for routine production.

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7488-96, Poster Session

Back-glass cleaning: reducing repelliclization costs by focused action

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With the optimization of sulfate-free cleaning the issue of haze under pellicle was almost eliminated. In consequence, current reasons for mask repelliclization needs are moving from pattern issues to more gross problems on back glass. Moreover, the longer life of photomasks allows a new problem to appear as growing defects on back glass, commonly ascribed to environmental conditions at user's site. The commonality of these problems is being independent on mask complexity and substrate. In order to avoid the criticalities of pellicle removal and cleaning treatment as well as the cost of necessary inspection after new pellicle application, the best solution is cleaning only the backside of the mask, provided that integrity of pellicle and pattern on front side are preserved

In this article we present the results obtained by the use of the Mask cleaner DE050019 - on several cases.

The efficiency of the treatment was assessed in terms if removal capability on different kinds of contaminations, either from use or mask aging. Pattern inspections were conducted in order to assess ESD robustness. Ionic resides were checked by IC aimed to compare with standard cleanings.

This methodology demonstrated to be capable of maintaining a Particle Removal Efficiency>97% on all kinds of contaminations, without any damage to pellicle or harm to patterns, still maintaining residual ions at the same level as after cleaning by standard tools.

7488-89, Poster Session

Feasibility study of the complex approach to flare, shadowing, optical, and process corrections for EUVL MDP

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The switch from 193i to EUV Photolithography will bring some fundamental changes in exposure. The flare levels of an EUV machine are significantly higher compared with standard 193i machines. Moreover shadow effects on the reticle are not equivalent to 193i. It is inevitable that these fundamentals require modifications in the Optical Proximity Correction (OPC) and Mask Data Preparation (MDP) flows.

In this paper in collaboration with ASML Brion the critical enabling steps of the Mask Data Preparation (MDP) for EUVL, Flare, Shadowing and Optical and Process Corrections (OPC), are investigated.

We measured the needs of the EUV MDP flow against the capabilities of a state-of-the art OPC flow built for 193i. Adaptations are being made to implement features which are currently not available in a 193i based flow.

We present a feasibility study of the Model Based approach to the EUV OPC on a wide selection of clips and full-mask designs. Also we demonstrate simulations and verification of the EUV modeling capabilities for the Tachyon software with various flare range and levels.

Distortions such as mask shadowing and proximity effects were characterized. We also evaluated the accuracy of the EUV OPC modeling and expected OPC corrections on the reviewed selection of clips as a substantial part of the overall CDU budget.

Finally an overall EUV OPC flow as a manufacturable solution based on the advanced Tachyon software and ASML's knowledge of Photolithography was discussed.

7488-98, Poster Session

Novel EUV mask inspection tool with 199-nm laser source and high-resolution optics

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A novel EUV mask inspection tool with 199nm laser source and super-resolution image detection optics has been developed. The usage of ArF immersion lithography for hp 32nm node and beyond leads to the increase of mask error enhancement factor in the exposure process. This makes preferable the inspection wavelength to be consistent with that of lithography tool. NPI-5000PLUS, which is a photo-mask inspection tool using 199nm wavelength, was already developed by Advanced Mask Inspection Technology (AMIT) and produced by Nuflare Technology (NFT). This system has ability corresponding to hp 32nm node photo mask inspection.

Developed EUV mask inspection tool is based on proven platform NPI-5000PLUS, and can implement Die-to-Die inspection and Die-to-Database inspection with 50nm pixel size optics. In order to implement EUV mask inspection with only a short time for mask set-up, reflected illumination type alignment optics to guide alignment mark and adjust mask coordinate with visible illumination light are equipped. Moreover, to inspect EUV masks for hp32nm and beyond, the image detection optics with super-resolution method and the lower noise image acquisition system are incorporated in this tool. We adopted novel polarized illumination technique for image contrast enhancement. To modify the illumination condition, illumination control optics are inserted at the illumination optical pupil position. Image contrast enhancement was confirmed by experiments using several kinds of EUV mask, whose absorber structures were different, and these phenomena are consistent with simulation results.

Currently, this inspection tool has two illumination fields on mask, as well as NPI-5000PLUS. One is for transmitted illumination field and the other is for reflected illumination one. This platform has capability by switching each field illumination to transmitted and reflected, then applying polarization control optics to the system. To provide appropriate and effective super-resolution potential to the inspection machine, illumination type and pupil control are adjusted, the most qualified defect detection sensitivity can be achieved.

This study is supported by New Energy and Industrial Technology Development Organization (NEDO).

7488-100, Poster Session

Automated wafer defect analysis using high-resolution reticle inspection data

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Most semiconductor fabs implement a reticle inspection strategy to prevent wafer yield loss caused by mask defects. However, in the event a reticle defect causes a repeating wafer defect signature, identifying the 'problem layer' can be very time consuming. In some extreme cases, the manufacturing line may shut down for extended periods until root cause is identified.

This paper examines a software solution from KLA-Tencor that automatically searches high-resolution reticle inspection data of each mask used to produce the affected wafer. As a result, the specific reticle layer and exact printing defect are quickly isolated from all candidate layers and graphically presented for root cause confirmation. The outcome is an automated process that either confirms, or eliminates, reticle quality as the source of yield-limiting wafer defect performance: all in a fraction of the time typically needed to solve this type of problem.

By stacking layers of high-resolution reticle inspection data, marginally printing defects from entire mask sets are included in the search process. These defects must also be considered since they can produce 'soft' repeating wafer defect signatures due to occasional, yet normal, varying lithographic focus and exposure conditions. In addition, this paper looks at reticle trend analysis features the Klarity software solution offers to further optimize wafer yield and enhance reticle re-qual programs for any technology node.

7488-101, Poster Session

Aerial plane inspection for advanced photomask defect detection

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A new methodology - Aerial Plane Inspection (API) - has been developed to inspect advanced photomasks used for the 45 nm node and beyond. Utilizing images from a high resolution mask inspection system, mask image is recovered from a combining of the transmitted and reflected images, then a transformation is performed to replicate the aerial image planes produced in a photolithography exposure system. These aerial images are used to compare adjacent die in a Die-Die inspection mode in order to find critical defects in the photomask. The mask recovery process and modeling of the aerial plane image allows flexibility to simulate a wide range of lithographic exposure systems, including immersion lithography. Any source shape, Sigma, and numerical aperture (NA) can be used at all common lithographic wavelengths. Sensitivity of the inspection can be fully adjusted to match photomask specifications for CD control, line-end shortening, OPC features, and for small and large defective areas. An additional adaptive sensitivity option can be utilized to automatically adjust sensitivity as a function of MEEF.

Using the Aerial Plane Inspection to compare pattern images has the benefit of filtering out non-printing defects, while detecting very small printing defects. In addition, defects that are not printing at ideal exposure condition, but may be reducing the lithographic process window, can also be detected. Performing defect detection at the aerial image plane is more tolerant to small Optical Proximity Correction (OPC) sub-resolution assist features (SRAFs) that are difficult to inspect at the reticle image plane.

7488-102, Poster Session

AIMS™ mask qualification for 32-nm node

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Moving forward to 32nm node and below optical lithography using 193nm is faced with complex requirements to be solved. Mask makers are forced to address both Double Patterning Techniques and Computational Lithography approaches such as Source Mask Optimizations and Inverse Lithography. Additionally, lithography at low k1 values increases the challenges for mask repair as well as for repair verification and review by AIMS™. Higher CD repeatability, more flexibility in the illumination patterns as well as significantly improved image performance must be added when developing the next generation mask qualification equipment. This paper reports latest measurement results verifying the appropriateness of the latest member of AIMS™ measurement tools - the AIMS™ 32-193i.

We analyze CD repeatability measurements on various patterns (lines/spaces, contact holes) with and without programmed defects. The influence of the improved optical performance and newly introduced interferometer stage will be verified. This paper highlights both the new Double Patterning functionality emulating double patterning processes and the influence of its critical parameters such as overlay errors and resist impact. Beneficial advanced illumination schemes emulating scanner illumination document the AIMS™ 32-193i to meet mask maker community's requirements for the 32nm node.

7488-103, Poster Session

Inspection of complex OPC patterns for 4x node and beyond

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OPC (Optical Proximity Correction) technique is inevitable and getting more complex to resolve finer features on wafer with existing optical lithography technology. Because of not only smaller main features but also these aggressive SRAF (Sub Resolution Assist Features) on reticle, reticle inspection process is getting more difficult. Some SRAF generated with special model-based OPC tools are so sophisticated that we can hardly imagine final patterns on wafer simply by seeing patterns on reticle. These model-based OPCs consist of many kinds of assist features since they are designed differently according to various target features on wafer and lithographic conditions, even though there are sustained efforts to simplify and improve the pattern shapes and arrays with MRC techniques. Consequently, inspecting this sort of extremely complex SRAF causes too many false alarms or/and nuisance defects, which makes reticle inspection process a burden in entire reticle fabrication process. To reduce the number of false alarms, inspection engineers should desensitize the inspection threshold reluctantly, but desensitizing always embraces the possibility of missing defects printable on wafer.

To overcome this dilemma, several advanced approaches have been developed, such as, TLD (Thin Line Desense), LPI (Lithographic Plane Inspection), and Aerial Image Based Inspection. We compare and analyze the functionalities of enhanced inspection methods with complex OPCed features for 4x nodes and beyond.

7488-106, Poster Session

Theoretical foundations of die-to-model inspection

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Die-to-Model (D2M) inspection is an innovative approach to running inspection based on a mask design layout data. The Aera2 D2M concept takes inspection from the traditional domain of mask pattern to the preferred domain of the wafer aerial image. To achieve this, D2M transforms the mask layout database into a resist plane aerial image, which in turn is compared to the aerial image of the mask, captured by the Aera2 optics.

The aerial model calculation starts from the mask layout database (GDS file), then a mask patterning model (writer and etch) is applied to produce the mask transmission model. The core step of converting the mask into aerial image model is based on Hopkins model of light diffraction. The implementation takes the coherent decomposition approach, where the partial coherent optics system is described by a set of filters. The filters, usually dubbed as kernels, represent eigenfunctions of the optical imaging system. The model-learning process learns the minimal set of kernels and their coefficients (eigenvalues), to produce a compact representation of partial coherent optics on the inspection system. During inspection, these kernels provide a highly efficient method to apply the optics model on the mask model, to finally create the aerial image of the mask in real time.

D2M detection algorithm works similarly to an Aerial D2D (die-to-die) inspection, but instead of comparing a die to another die it is compared to the aerial image model. D2M is used whenever D2D inspection is not practical (e.g., single die) or when a validation of mask conformity to design is needed, i.e., for printed pattern fidelity. D2M is of particular importance for inspection of logic single die masks, where no simplifying assumption of pattern periodicity may be done. The application can tailor the sensitivity to meet the needs at different locations, such as device area, scribe lines and periphery.

In the present paper we review the theoretical foundations of the D2M inspection.

7488-107, Poster Session

New analysis tools and processes for mask repair verification and defect disposition based on AIMS™ images

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Using AIMS™ to qualify repairs of defects on photomasks is an industry standard. AIMS™ images match the lithographic imaging performance without the need for wafer prints. Utilization of this capability by photomask manufacturers has risen due to the increased complexity of layouts incorporating RET and phase shift technologies. Tighter specifications by end-users have pushed AIMS™ analysis to now include CD performance results in addition to the traditional intensity performance results.

Discussed is a new Repair Verification system for automated analysis of AIMS™ images. Newly designed user interfaces and algorithms guide users through predefined analysis routines as to minimize errors. There are two main routines discussed, one allowing multiple reference sites along with a test/defect site within a single image of repeating features. The second routine compares a test/defect measurement image with a reference measurement image. Three evaluation methods possible with the compared images are discussed in the context of providing thorough analysis capability.

This paper highlights new functionality for AIMS™ analysis. Using structured analysis processes and innovative analysis tools leads to a highly efficient and more reliable result reporting of repair verification analysis.

7488-108, Poster Session

Reducing the shot counts of mask writing with OPC by extracting repeating patterns

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Since May 2006, the Mask Design, Drawing, and Inspection Technology Research Department (Mask D2I) at the Association of Super-Advanced Electronics Technologies (ASET) has been researching and developing for the mask manufacturing cost and TAT by concurrent optimization of MDP, mask writing, and mask inspection. As part of the project, we devised the method of the extraction of repeating patterns from mask data after OPC and use as Character Projection (CP) for reducing the shot counts during the electron beam writing, and we developed the extraction tool and evaluated it by using actual device production data obtained from the member companies of MaskD2I. In this paper, we will address the verification results of the extraction tool and introduce the result of the extraction from several masks and the result of the simulation that considers the influence of PEC aiming at practical use.

7488-109, Poster Session

Improving the quality of fractured mask data through in-place optimization of the fracturing solution

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Due to poorly optimized fracturing strategies, the Quality of Results (QoR) of fractured data generated through Mask Data Preparation (MDP) may be sub-optimal or non-uniform. It is also frequently observed that different instances of similar polygons might get fractured differently, especially if

they have different orientations. This may result into poor CD uniformity. For some instances of the polygons a better fracturing solution may be possible compared to the one present in the fractured mask data.

In this paper, we present the idea of (in-place) substitution of the fracturing solution of some of the badly or non-uniformly fractured instances of polygons by a better fracturing solution. This In-Place Optimization (IPO) strategy does not modify the fracturing data of polygons which might have already acceptable fracturing solutions. Hence, rather than carrying out complete re-fracturing, the QoR of fractured data can be improved in-place through applying patches to the hotspots of badly or non-uniformly fractured polygons. Polygons could be categorized as badly or non-uniformly fractured based on the values of various quality metrics - such as number of shots, number of sliver shots, total shoreline sliver length, CD uniformity, splitting of slanted edges, etc. Apart from this an optimally fractured solution of a polygon ideally suitable for critical regions may not necessarily be needed if the polygon is located in the not-so-critical regions. In the proposed IPO scheme, the criterion for ranking the QoR of a fractured solution of a polygon can be given as an external parameter. The IPO technique identifies all instances of such badly fractured polygons which have their ranks below some user specified threshold value and replaces their fracturing solutions with better fracturing solutions. The better fracturing solution could be the one which might already be present in some other fractured instance of the same polygon (possibly with a different orientation) within the fractured data or it could be generated through instantiating a separate polygon-level fracturing algorithm. The proposed IPO scheme allows internal substitution (where the solution exists already in the fractured data) as well as external substitution (where the fracturing solution is generated externally through a separate fracturing algorithm). Since this IPO technique modifies the fractured mask data, it is mandatory to have a stringent built-in validation scheme that verifies that the modified data is geometrically equivalent to the original data. Firstly, the proposed validation scheme verifies that the substituted fractured data is geometrically equivalent to the originally fractured data without introducing any overlaps of trapezoids in fractured data. Secondly, it verifies that fracturing of the polygons which originally had acceptable fracturing solutions has not been altered. The paper gives detailed results of observed QoR improvement when such IPO of fracturing was employed on several test cases.

7488-144, Poster Session

Economic assessment of lithography strategies for the 22-nm technology node

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The unavailability of extreme ultra violet lithography (EUVL) for mass production of the 22nm technology node has created a significant void for mainstream lithography solutions. To fill this void, alternate lithography solutions that were earlier deemed to be technically and economically infeasible, such as double patterning technologies (DPT), massively parallel direct write e-beam (MEBM) and Interference assisted lithography (Intf), have to now be aggressively developed and adopted to ensure the timely deployment of the 22nm technology node. While several studies have been undertaken to estimate the lithography process costs for volume production with the aforementioned technologies, these studies have provided only a partial analysis since they have not taken into account the impact on design density and product yield.

In this paper we propose to use the cost-per-good-die metric in order to capture process costs as well as yield and design density. We have developed a framework that estimates the lithography cost-per-good-die for SRAM arrays and have applied it to evaluate the economical feasibility of the various lithography strategies under consideration for the 22nm technology node. Specifically, we compare the cost-per-good-die for different 32MB SRAM arrays, each optimized for a different lithography choice. Our analysis shows that the selection of the best lithography strategy is both layout and volume specific. The use of MEBM solutions is recommended for Contact and Via layers, the use of Intf is recommended for dense layers such as Poly and Metals, and the use of more expensive DPT or MEBM is recommended for Active layer where restrictions necessary to enable interference based lithography cause a significant area penalty. In summary, we find that a “mix & match” strategy is ideally suited for the 22nm technology node, with Interference followed by MEBM applied for low-to-medium volume products, and high volume products (exceeding 7 million dies) implemented by Interference followed by the traditional optical lithography to acheive the lowest lithography cost-per-good-die.

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7488-111, Poster Session

Improved particle control by adopting advanced ceramic materials in dry etcher for defect reduction

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As integration of circuits increases, required feature size becomes smaller and smaller. Defect control become tighter due to decrease of defect size that affects the image printed on the wafer and increase of possibility to be killer defect like 2-faced bridge defect. Therefore, particles sources from all processes should be controlled extremely.

Especially for dry etching process, Alumina ceramics have been widely used for plasma resistance materials such as electrode covering plate and insulator. However, they also can be etched under CF4 plasma condition, even small amounts. It has been reported in several literatures that non-volatile byproduct from the etched ceramics can be particle source to be killer defect. Therefore, Selection of ceramics materials must be important for particle control in dry etch process.

In this paper, Etch resistance difference was studied for alumina and yttria ceramics with various density and surface roughness. Ceramics surface change after plasma treatment was observed and particles generated by plasma were done by EDS analysis for particle source tracking. Particle and defect control performance were also evaluated by replacing existing alumina parts in dry etcher with the material with best performance.

7488-112, Poster Session

The study of the birefringence as PSM materials for immersion lithography

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According to semiconductor technology roadmap, the immersion lithography emerges for the 32 nm and below technology. Therefore the immersion lithography requires new process parameters such as high refractive index fluid, stepper, resist and birefringence. So a lot of working for those items has been studied and the component and material of phase shift mask (PSM) have become more important. The birefringence of PSM thin film is an essential issue for development of advanced technology, especially. Accordingly, we study the birefringence with thin film characteristics.

Having a transmittance of 6% at 193 nm, four different kinds of thin films have been prepared by DC magnetron sputter. In this paper, we have measured the birefringence by a polarized microscopy and the results of measuring the birefringence got from 4.0 x 10-4 nm to 1.2 x 10-4 nm. And then the effects on birefringence with reactive gas ratio and deposition methods (atomic layer deposition (ALD), chemical vapor deposition (CVD), long through sputtering (LTS) and ion beam deposition (IBD)) are investigated. As a result, the birefringence value is changed by residual stress and stoichiometric reaction in thin film. And, we find out that we can control the birefringence by the tuning of thin film properties.

7488-113, Poster Session

A study of contour image comparison measurement for photomask patterns in 32-nm beyond

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As photomask patterns become smaller and more complex, it is difficult to characterize the pattern feature by only one-dimensional Critical Dimension (CD). Photomask patterns are getting more complex in 32-nm beyond especially for aggressive Optical Proximity Correction (OPC) and Source Mask Optimization (SMO). The feature of these patterns cannot be characterized by conventional measuring methods, because they are no longer simple one-dimensional patterns. In addition small size defects become problematic because the defects cannot be distinguished by SEM in review process. Such problem happens easily in the repeated patterns field. A method of contour image comparison measurement is very effective to solve these issues. It extracts the contour from SEM images; measurement object and reference are superimposed. The difference of feature is measured by CD and Area. Contour image comparison measurement system was developed by utilizing MaskEXPRESSTM that is software for mask feature analysis.

In this paper, the function of the system will be explained and the result will be discussed in terms of measurement accuracy and using programmed defects mask.

7488-114, Poster Session

Noble approach for mask-wafer measurement by design-based metrology integration system

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OPC (Optical Proximity Correction) technique is getting more complicated towards 32 nm technology node and beyond, i.e. from moderate OPC to aggressive OPC. Also, various types of phase shift mask have been introduced, and their manufacturing process is complicated. In order to shorten TAT (Turn around time), mask design technique needs be considered in addition to lithography technique.

Furthermore, the lens aberration of the exposure system is getting smaller, so its current performance is very close to the ideal. On the other hand, when down sizing of device feature size reaches the 32nm technology node, cases begin to be reported where the feature dimension is not matched between a mask pattern and the corresponding printed pattern. Therefore, it is indispensable to understand the pattern size correlation between a mask and the corresponding printed wafer in order to improve the processing accuracy and the quality in the situation where the device size is so small that the low k1 lithography is widely used in production.

One of the approaches to improve the estimated accuracy of lithography is the use of contour data extracted from mask SEM image in addition to the application of a mask model.

This paper describes a newly developed integration system that aims to solve the issues above, and its applications. This is a system that integrates mask CD-SEM (Critical Dimension-Scanning Electron Microscope) CG4500, wafer CD-SEM CG4000, OPC evaluation system DesignGauge, all manufactured by Hitachi High-Technologies.

The measurement accuracy improvement was examined by executing a mask-wafer same point measurement, i.e. measurement of the corresponding points, with same measurement algorithm utilizing the new system. First, we prepared a mask and wafers for 50nm line. Then, we measured mask patterns and verified the validity based on the measurement value, the image, the measurement parameter and the coordinates. Then a job file was formulated for a wafer CD-SEM using the new system so as to measure the corresponding patterns that were exposed using the mask. In addition, the average CD measurement was tried in order to improve the capability.

Furthermore, in order to estimate the pattern shape with high accuracy, a contour was calculated from a mask SEM image, and the result was used with the design data in a litho simulation. This realizes a verification that includes mask fabrication error.

This system is expected to be beneficial for both mask makers and device makers.

7488-115, Poster Session

Corner rounding analysis of reticle, optical, and resist contributions

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It is known that corners in the design layouts are printed rounded due to finite resolution of optics system in lithography. The resulted corner rounding in printed wafer contours has shown effects in device performance [1]. There has been theoretical analysis on corner rounding [2], which showed corner rounding radius scales linearly with wavelength/NA and resist diffusion. With the fast progress of optical lithography, the corner rounding improves over the time. In sub-wavelength optical lithography, the use of optical proximity correction could improve imaging fidelity [3] and reduce corner rounding radius close to its theoretical limit due to optical and resist resolution. But now optical lithography faces the physical limitation in terms of wavelength and numerical aperture (NA) scaling, the reduction of corner rounding radius is also facing a limit. The improvement of resist resolution provides only a little improvement on corner rounding radius due to the optical resolution limit as shown in Figure 2. In EUV Lithography, optical resolution is greatly improved, and thus resist blur effects dominate corner rounding. The contribution from mask corner rounding will also be discussed in additional to contributions from optics and resist.

Figure 1 shows the curve fitting procedure to obtain corner rounding radius and corner pullback for simulated rounded image contours. Figure 2 shows calculated corner rounding radius through resist blur for both NA = 1.35 optical lithography and NA = 0.25 EUV lithography cases.

7488-36, Poster Session

Investigation of subresolution assist feature process window

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As CD linearity issue exists in small feature sizes at the advanced technology nodes pattern process, it can be found that after process sub-resolution assist feature (SRAF) size deviates from its target, pattern collapse or missing while main feature size is on target. Optimizing process CD linearity is a direct approach to solve the problem. But it is also necessary to investigate the SRAF process window. And adding proper

bias to the writing data is an alternative way.

In this paper, several groups of designed test patterns with SRAF size matrixes are used to explore their process window on PSM blank. The SRAF length and width sizes and length-width ratio have a number of variations. The whole test patterns are exposed with different writing conditions and their process performances are investigated and compared. Test SRAF matrixes process windows are investigated on both resist layer and final MoSi layer. The resist layer process boundaries are roughly estimated by SEM image visual observation from the smallest sizes to the larger sizes. But on the MoSi layer the test matrixes are inspected on the KLA tools with both Die-to-Die and Die-to-Database method to verify the final process boundaries. The SRAF length-width ratio combination to the process performance is also investigated in the experiment.

The process CD biases for the test pattern length/width combination respectively are measured so that such database can be used for defining better writing biases. The results of the investigation also enable us to improve SRAF process window.

7488-116, Poster Session

Adaptive OPC approach based on image simulation

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The implement of the immersion micro-lithography pushes the resolution limitation of the 193nm light source. And the brand-new lithography tool makes many optical effects, which can be ignored at dry exposure technology node, now have significant impact on the pattern transmission process from design to silicon. All these effects are now inducing great challenge to the Optical proximity correction technology. More and more sophisticated correction technologies are employed now to promise the pattern fidelity during the lithography process. But due to the complexity of the modern design, the most headache challenge that facing the OPC engineer is the fragmentation and correction control recipe development. To provide a control recipe that can cover most kinds of design layout is now a difficulty job. In the work, we will demonstrate our study of an adaptive OPC approach that is based on image simulation, which can shorten the recipe development time effectively.

7488-117, Poster Session

Introducing process variability score for process window OPC optimization

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As the IC Industry moves towards 32nm technology node and below, it becomes important to study the impact of process window variations on yield. PVBands is a technique to express process parameter variations such as dose, focus, mask size, etc. However, PVbands width alone is insufficient as a quantitative measure for judging the PVband performance, as it does not take into consideration how far away the contours are from the target.

In this paper, a novel mathematical formulation has been developed to better judge the PVBands performance. It expresses the PVBand width and symmetry with respect to the target through a single score. This score can be used in OPC (Optical Proximity Correction) iterations instead of working with the nominal EPE (Edge Placement Error). Not only does this approach provide a better measure of the PVBands performance through the value of the score, but it also presents a straightforward method for PWOPC optimization by using the PV Score directly in the iterations.

7488-118, Poster Session

Patterning of 90-nm node flash contact hole with assist feature using KrF

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The sub-90nm technology node, patterning of contact hole using KrF lithography system is one of the most challenging tasks. Contact hole patterning at KrF lithography system can be printed using Off-Axis Illumination(OAI) such as Quasar or Quadrupole. However this condition usually offer poor image contrast and poor Depth Of Focus(DOF), especially isolated contact hole. Sub-resolution assist feature(SRAF) can be used to improve the image contrast and DOF for isolated contact hole. With the SRAF, intensity profile of the isolated feature will be modified to dense-like one and, as a result, focus response of the isolated feature can be improved to dense feature level. The insertion of SRAF in a contact design is mostly done using rule based scripting. The configuration of SRAF that distance of assist feature to main feature, size and number of assist feature was adjusted by simulation tool first. However in case of random contact hole, rule-based SRAF placement is almost impossible task. We have used an inverse lithography technique to treat random contact hole.

In this paper we prove the impact of SRAF configuration both on pattern profile and process margin. We also show that the experimental data can easily be predicted by calibrating aerial image simulation results. As a conclusion, we suggest methodology to set up optimum SRAF configuration with rule and inverse lithography technology.

7488-119, Poster Session

On comparing conventional and electrically driven OPC techniques

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This paper compares the expected runtime, mask complexity and electrical accuracy of solutions produced by conventional Shape Driven Proximity Correction (SDOPC) and Electrically Driven Optical Proximity Correction (EDOPC). When electrical objectives are used over geometrical objectives, electrical accuracy increases [1, 2]. This can result in a smaller fragmentation and/or larger OPC step size used for EDOPC for an equivalent current accuracy resulting in improvement in OPC runtime and reduced mask complexity. Even with same fragmentation scheme for both EDOPC and SDOPC, EDOPC can accept a significantly larger number of solutions, leading to a shorter algorithm runtime.

Consider a simple gate represented by the overlap of the poly and active layers. The geometry of the layout is shown in Figure 1. The overlap is fragmented into N edges and each edge is allowed to be shifted in steps of S inward in a range of R. This geometry results in roughly (R/S + 1)^N possible layouts produced by edge-based OPC. After lithography, each contour is sliced into constant length segments and checked for correctness. A contour is accepted by SDOPC if every slice has bounded Edge Placement Errors (EPEs). For EDOPC the current of each slice in a contour is summed together and the resulting total current must be within current boundaries [5]. Since EDOPC is concerned with (roughly) minimizing error in weighted harmonic mean (i.e., total current metric) of the EPEs rather than maximum EPE, it will have a much larger set of acceptable solutions. Note that all shape-acceptable solutions and electrically acceptable but the converse is not true.

To examine the OPC results experimentally, all possible layout solutions are generated and run through a lithography simulator in 65nm technology. EDOPC achieves a better current accuracy that SDOPC. Moreover, both experiments and mathematical models show that EDOPC has a larger number of accepted solutions (5X to 1000X) in this simple test case indicating that well-implemented EDOPC algorithms should converge much faster to an acceptable OPC solution than SDOPC. Our results

suggest that a move to electrical objectives and constraints can make OPC orders of magnitude faster and more electrically accurate.

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7488-120, Poster Session

OPC model calibration and parameter optimization for 3D complex patterns using scatterometry data

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In previous work we developed the methodology of using scatterometry data for OPC model calibration and verification. The scatterometry results were compared with the CDSEM results and very good correlation with BCD data was observed.

The precise characterization of complex 3D features represents a significant challenge for the lithography OPC process. The main difficulty lies in transferring sufficient information about three-dimensional features into the OPC model building process. Current advances in scatterometry modeling software allow measuring more complex structures and obtain accurate information on parameters such as tip-to-tip distances and shapes. In this work we will report on OPC model calibration and verification for complex 3D patterns. In the case of SRAM patterns we will discuss the specific feature parameter optimization through process window. In addition we will also review scatterometry metrology trade offs for such complex 3D patterns measurements.

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7488-121, Poster Session

OPC model space approach to in-line process monitoring structures

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With shrinking technology nodes and increasing geometries criticity, it has become more and more difficult to conceive fast and accurate in-line check to insure process quality for each lithography level. Time and costs limit metrology options.

A commonly accepted solution consists in some CD measurement on high contrast structure for each critical level. However, the RET complexity of current layouts makes this solution no longer fully reliable and allows non-conform materials to pass through the check. The idea behind this article (patent pending) is to add a second verification by creating a set of small structures layouted to cover specific coordinates in the model parameters space. Extrapolated model parameters allow to layout geometries encircling the OPC space region occupied by the production device. Those structures shall bridge or pinch for litho or process deviations before any detectable impact on the most sensitive shapes present in the product. Total size of few square microns is required to stay within a single SEM picture at defect-detecting magnification. The use of image processing based on pattern recognition on SEM pictures to assess their sensitivity to process variations permits a fast analysis.

As a matter of fact, this approach will allow getting reliability by watching the whole model space and economic compatibility as the procedure is fast and cost-effective.

7488-122, Poster Session

Practical application of OPC in electrical circuits

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Today's Optical Proximity Correction (OPC) is becoming increasingly complex and requires that we use smaller and smaller grid sizes to produce the fine patterns required. These small grids lead to very high overheads in data handling and, more importantly, for the tools that will write and inspect the mask, making the mask extremely expensive. For line patterns, typically using Scattering Bar (SB) OPC, this leads to small line type features, but for two dimensional structures, such as corners, we have very complex structures using either additive or subtractive OPC features to produce the desired shape. However, what is not clear is whether these structures need to be so perfect for the electrical task they are required to perform. In this work we have created a number of corner type electrical test structures and applied different degrees of OPC to both the outer and inner corners of the structures. These features have then been printed on doped polysilicon wafers and the wafers then etched and electrically tested. Images of the etched features were also captured and electrical performance of these simulated. Correlation between the measured and simulated results help to confirm that the electrical effect of OPC on the outer corner is minimal, whereas the inner corner shape has a great effect upon corner rounding and as such a great effect upon the current flow path. The data suggests that OPC on the outside corner has little effect upon a simple circuit performance, but care should be taken with OPC on inner corners.

7488-123, Poster Session

Three-dimensional Si aperture plates combined with programmable blanking plates for multibeam mask writing

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Multi-beam lithography is considered a promising fabrication technology for future node mask making. Due to rising design complexity and therefore increasing pattern writing times the multi-beam approach has distinguished throughput advantages compared to state of the art variable shaped beam pattern generators.

A key component of a projection multi-beam writing tool is the

programmable blanking plate for generating the desired pattern geometry on the mask substrate.

In our case a highly parallel charged particle beam illuminates a Si aperture plate which shapes and generates many thousand individual spot beams. These beams pass through a blanking plate with integrated CMOS electronics for de-multiplexing the writing data. The blanking plate is equipped with blanking and ground electrodes placed around the apertures switching the beams 'on' or 'off', dependent on the desired pattern. The beam array is demagnified by a 200x reduction optics and the exposure of the mask substrate is done in stripes by a continuous moving stage [1].

Cross talk between adjacent beams in the blanking plate has to be avoided to ensure adequate pattern fidelity and line edge roughness on the mask substrate. One solution is the insertion of a 3D Si aperture plate in proximity to the blanking plate shielding the blanking electrodes from each other during operation.

We developed and characterized a new process flow for the fabrication of these 3D Si aperture plates for the case of 43 thousand beams in parallel and will present and discuss the cross talk results for blanking plates combined with standard 2D and new 3D Si aperture plates.

7488-124, Poster Session

Examination about observation of the identical position of a mask and silicon

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We have developed a highly integrated method of mask and silicon metrology.

The aim of this integration is evaluating the performance of the silicon corresponding to Hotspot on a mask.

The method adopts a metrology management system based on DBM (Design Based Metrology).

This is the high accurate contouring created by an edge detection algorithm used in mask CD-SEM and silicon CD-SEM.

Currently, as semiconductor manufacture moves towards even smaller feature size, this necessitates more aggressive optical proximity correction (OPC) to drive the super-resolution technology (RET).

In other words, there is a trade-off between highly precise RET and mask manufacture, and this has a big impact on the semiconductor market that centers on the mask business.

As an optimal solution to these issues, we provide a DFM solution that extracts 2-dimensional data for a more realistic and error-free simulation by reproducing accurately the contour of the actual mask, in addition to the simulation results from the mask data.

On the other hand, there is roughness in the silicon form made from a mass-production line.

Moreover, there is variation in the silicon form.

For this reason, quantification of silicon form is important, in order to estimate the performance of a pattern.

In order to quantify, the same form is equalized in two dimensions. And the method of evaluating based on the form is popular.

In this study, we conducted experiments for averaging method of the pattern (Measurement Based Contouring) as two-dimensional mask and silicon evaluation technique.

That is, observation of the identical position of a mask and a silicon was considered.

The result proved its detection accuracy and reliability of variability on two-dimensional pattern (mask and silicon) and is adaptable to following fields of mask quality management.

- Discrimination of nuisance defects for fine pattern.

- Determination of two-dimensional variability of pattern.

- Verification of the performance of the pattern of various kinds of Hotspots.

In this report, we introduce the experimental results and the application.

We expect that the mask measurement and the shape control on mask production will make a huge contribution to mask yield-enhancement and that the DFM solution for mask quality control process will become much more important technology than ever. It is very important to observe the form of the same location of Design, Mask, and Silicon in such a viewpoint.

7488-125, Poster Session

Revisit to aberration: a simulation study of lens aberration-induced overlay misalignment and its experimental validation

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For the miniaturization of integrated circuits (IC), a patterning with small CD and small overlay (O/L) is highly required. To exceed the physical limits (NA,) for smaller patterning, a double patterning technology (DPT) was introduced. However, DPT made the specification of overlay much tighter (for example less than 6nm O/L is required for 32nm DPT). O/L misalignment (M/A) is induced from numerous sources including metrology error and stage control error, and aberration in projection optics. In the past, the contribution from aberration in projection optics was negligible among the sources. However, as design rule become smaller, aberration induced O/L M/A is evaluated to take considerable portion in the overlay budget. This paper focuses on projection optics induced O/L issues. We presents a simulation analysis of M/A between contact hole (C/H) pattern and line & space (L/S) pattern at 65nm node based on the aberration data from actual lithography tool to single out the main source of O/L M/A. In addition, experimental results of the O/L measurements in cell area and key area with lens heating (LH) correction are provided for validation purpose. The study shows that the aberration in projection optics can induce considerable M/A and the conventional overlay keys do not represent this M/A properly. Among the Zernike fringe polynomials, the third-order portion (D3) in Z2 (tilt) is found to be the critical source of misalignment. This portion of the aberration is resulted from the LH and can be corrected. However, this correction method needs improvements because its controllability over LH is not enough for the complete correction of LH induced M/A. Besides D3, Z10 (3-Foil) are found to be the major sources for pattern shift in C/H patterns, and Z7 and Z14 (Coma x) are found for L/S patterns. These aberrations can induce M/A approximately 4nm. The variation of aberration across the slit is validated to make M/A up to approximately 1nm between C/H and L/S. These M/As can be added up because these results only consider in-shot pattern shift, not relative O/L M/A from shot to shot. These results show that a tighter specification control in projection optics, such as separation Coma X and 3-foil as an individual specification from lens aberration specification, is highly desirable for the successful switchover to smaller design rules using DPT.

7488-126, Poster Session

Wafer topography proximity effect modeling and correct for the implant layer

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Photolithography on reflective surfaces with topography can cause additional exposure in some areas in the photo resist, resulting in undesired critical dimension (CD) variations in the printed patterns. Using bottom anti-reflective coatings (BARCs) will reduce the severity of the problem. However that's not a preferred solution in some situations due to added process complexity. This is the case for implant layer patterning.

This topography proximity effect (TPE) in implant layer patterning has

been ignored in the mask synthesis flow for the 45nm and larger nodes due to its relatively small impact to the CDs and the implant layer is one of the so-called noncritical layers. When the device critical length reaches 32nm and lower, the variations on the implant layer caused by underlying topography becomes more and more an issue and need to be addressed in the mask synthesis flow. In order to do that, simulation with non-planar stack is required. The available tools for photolithography simulation with wafer topography, such as Synopsys Sentaurus Lithography, adopt a rigorous approach based on the Maxwell equations, and hence unfit for full chip optical proximity correction (OPC) due to their long runtimes. A fast method for TPE simulation is needed to make wafer topography proximity correction (TPC) feasible.

In this paper, we propose an approximate method that captures TPE reasonably well. It enables fast model calibration and full chip implant layer mask correction, and fits in the current OPC flows easily. We validate the method's accuracy by comparing its simulation results with those produced by Sentaurus Lithography. We also show how it helps implant layer mask synthesis that takes TPE from previous layers, such as the shallow trench isolation (STI) and gate layers, into consideration.

7488-128, Poster Session

Fast and accurate computation of partially coherent imaging by stacked pupil shift operator

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In this paper, the stacked pupil shift operator approach first introduced by Yamazoe cite{Yamazoe08} has been further developed and implemented for fast and accurate lithography simulation. The stacked pupil shift operator $mathcal{P}$ is a singular matrix obtained by stacking pupil functions that are shifted according to the illumination condition. The transmission cross coefficient (TCC) matrix can then be constructed in an elegant fashion as $mathrm{TCC} = mathcal{P}^{dagger}mathcal{P}$. The new development presented in this paper utilizes a matrix multiplication technique to speed up the computation of TCC matrix by tenfolds on average. This enables fast and accurate generation of TCC kernels for complicated illumination source shapes where a large number of source points are required to obtain good accuracy. The singular-value-decomposition (SVD) is applied to the TCC matrix instead of the stacked pupil shift operator $mathcal{P}$ so that mask and resist proximity effects can easily be included in the effective TCC kernels.

7488-129, Poster Session

Etch bias modeling and retargeting flow

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In this paper we present a physics-based variable bias model (VBM) designed to capture microloading effect and aperture effect in the etch process. In the process proximity compensation (PPC) methodology, it is desired to have sequential litho and etch models, especially for a process with large variable etch biases. VBM can be calibrated independently of the litho model, using After Development Inspection (ADI) and After Etching Inspection (AEI) SEM measurements. If desired, VBM can also be calibrated in a lumped fashion with the litho model. During the retargeting step, etch bias is applied to the design pattern and each edge is moved by a variable bias amount. We also present considerations of model calibration flow and retargeting flow. Various strategies are compared and model fitting results are presented.

7488-130, Poster Session

Extensions of boundary layer modeling of photomask topography effects to fast-CAD via pattern matching

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The accuracy and speed with which through-focus mask edge effects can be assessed in early stages of physical design are assessed through comparing results from Pattern Matching with boundary layers with those from rigorous mask and image simulation. For high NA immersion lithography, phase errors in the field transmission are introduced through edge interaction at the photomask creating distortion in both real and imaginary field transmission. Attenuating, alternating, and tritone PSMs allow for better imaging performance, but bring with them complications arising from the mask stacks. Boundary layer modeling has emerged as a candidate for modeling these electromagnetic field (EMF) effects in photomask transmission. Methods for calculating boundary layer contributions from 1D grating structures for attenuating and alternating phase-shifting masks (PSM) was reported [1,2] with an observed quadrature effect equivalent to a clear field width of 0.1 to 0.4 wavelength per edge [1]. Boundary layers are useful primarily because they can be treated as additional mask layers and optimized using OPC and similar thin mask modeling. Pattern Matching [3,4,5] uses aberration specific targets to assess the susceptibility of patterns to standard aberrations, of which focus is primary concern.

This study examines the accuracy and speed of first-cut accurate Patterning Matching in predicting on wafer CD change through focus for lithography scenarios for the 45, 32 and 22 nm generations. Boundary layers for various mask types are applied to typical test patterns in Cadence and Pattern Matching with off-axis illumination and defocus conditions are used to estimate intensity changes attributable to mask edge effects. Layouts identified by Pattern Matching to have significant intensity changes through focus are then systematically investigated through near field and image simulation with Panoramic Technologies. Of key interest are line-ends in logic and jogs in SRAM cells.

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7488-133, Poster Session

Calibration of lithography and etch models using SEM images

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Model-based Process Proximity Correction (PPC) models and corrects optical, resist and etch proximity effects. Its performance is directly related to the model accuracy, thus it is important to have a model that closely describes both the lithography and etch processes. Traditionally, model calibration was performed using 1D CD-SEM measurements of simple line

and space structures. As layout dimensions continued to shrink, it became obvious that relying on 1D data was not enough for building an accurate model. In order to improve the predictability of the model for arbitrary two-dimensional layouts, model calibration engines were extended to handle cut-line CD-SEM measurements of 2D layout clips. However this approach still suffers from inability to fully capture the corner rounding effects of the process.

New generation of measurement tools makes it possible to collect resist (DI) and post-etch (FI) SEM images, which contain more information than conventional CD measurements. We present a new model calibration method which simultaneously fits multiple SEM images or a combination of SEM images and 1D CD-SEM measurements. The images are preprocessed to extract the contours and to compensate for metrology and process variability and SEM alignment errors. The contour extraction algorithm estimates the data reliability and identifies and removes the outliers. The extracted DI and FI contours are then used to calibrate optical/resist and etch models.

First, the lithography model is calibrated using the DI data (DI contours and possibly CD-SEM measurements), then the etch model is calibrated from FI data in a similar manner. Optimization algorithms with specialized cost functions drive the calibration. Line-end and curvature information contained in the SEM images is used effectively; outliers are discarded based on statistical considerations. The result of this methodology is a more reliable and accurate model. The presented calibration strategy is especially useful when 1D data is not available or is unreliable, as in the case of contact layers, for instance.

7488-135, Poster Session

Predictive modeling for EBPC in EBDW

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We present a methodology to apply e-beam proximity correction (EBPC) to e-beam direct write (EBDW) wafer manufacturing processes. The methodology as shown in this paper is in principal equivalent to the concept which is used for optical wafer manufacturing processes, and can basically also be applied to other techniques like for example EUV.

As known from optical and shown here for e-beam application, a complete tool platform for test pattern generation, model fitting, correction, and verification are mandatory for successful application of the proposed methodology. This platform covers all steps from the generation of a test pattern (TP) for (experimental or virtual) measurement data creation, over e-beam model fitting, proximity effect correction (PEC), and verification of the results using a rigorous e-beam simulator.

Process data can then either be obtained by manufacturing and measuring the test patterns, or using a predictive simulator using physical models for exposure, resist processing, development and metrology. In absence of production-ready tools for multi-e-beam wafer processing, simulation provides us the capability of understanding the effects as well as building and verifying correction strategies at an early stage and ready them for deployment as tools become manufacturing ready. Simulation also provides the capability of separating various effects and accurately assessing the impact of variability of each one.

This flow is demonstrated for the cases of low (5 keV) and high (50 keV) electron energies. For both cases, standalone dose correction and geometric correction is applied to a TP including line/space and line end structures. Whereas dose correction is a state-of-the-art way used in Mask Error Correction (MEC), which - however - is in our case applied on 1x wafer scale, we also show that geometric (shape) correction can be performed on the basis of standard modeling and proximity correction tools as used for the optical case.

Since the proximity range (PR) for low energies is comparable to that in the optical case, we can show that geometric model-based correction is preferred for low electron energies. For high electron energies, standard OPC-like correction with its 1µm ambit cannot cover the proximity effects caused by long range (LR) electron scattering. Two concepts to take LR effects into account are shortly discussed, namely combining the geometric correction with dose correction, or extending the geometric correction to larger ambits, based on corresponding complement of the SR model by a LR model, a method similar to that currently considered for the optical case (flare effect).

Finally, analysis of the correction results is used to discuss PEC strategies for low and high electron energies, with respect to short range (SR) and LR effects. Application of best strategies to both cases is our focus for future work.

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7488-136, Poster Session

Effective methodology to make DFM guide line

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Design For Manufacturing (DFM) has become an important focusing part in the semiconductor industry as the feature size on the chip goes down below the 0.13um technology. Lots of DFM related ideas have been come up, tried, and adopted for wider process window and higher device performance. As the minimum features are getting shrunk, the design rules also become more complicated, but still not good enough to describe the certain pattern that imposes narrow process window or even failure of device. Thus, these process hot spot patterns become to identify, correct, or remove at the design step. One of the efforts is to support a DFM guide line to the designer or add to conventional DRC rules. However it is very difficult to make DFM guideline because we detect the hot spot pattern and confirm if these patterns is real hot spot or not.

In this study, we developed effective methodology how to make DFM guide line. Firstly we use the software, called nanoscope to detect hot spots on post OPC layouts and then make this detected hot spot pattern to test patterns that it can check electrical performance and then we compared with electrical performance according to split condition. It is confirmed this method is very effective to make DFM guide line below the 0.13um technology.

7488-137, Poster Session

pRSM: models for model-based litho-hotspot repair algorithms

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A straight-forward method of computing repair hints for litho hotspot could involve multiple steps such as modifying a layout clip to reflect changes for a potential repair, applying full RET/OPC treatment to the layout clip, and performing a litho simulation to compute new contours. Although accurate, this method is not practical due to the computational costs involved especially if such a flow is going to be embedded into P&R tools. A more elegant solution is to build a sufficiently accurate model to estimate contour changes as a function of design layout changes. Such a model would have to capture the interaction of design layout and post tape-out operations such as RET/OPC when predicting the eventual printed contours. A litho hotspot repair hint algorithm could then utilize such contour models to compute litho hotspot repair hints. The key is to create both the contour models and error bound estimates for such contour models.

In our approach, we have developed a modeling methodology based on Response Surface Model(RSM) which captures in sufficient accuracy the

complex interaction between design layout and post tapeout operations. Our approach, which call pRSM (Partition RSM), doesn't require overly complex model forms in order to capture the design layout to contour mapping. Instead, we create a family of models along with error bound estimate models which we call local truncation error(LTE). The LTE function allows the client of the pRSM model to monitor dynamically the error bounds and adjust its algorithms appropriately. Examples of how a pRSM client application could use the LTE information range from dynamically adjusting the derating of a contour model's predicted value to swapping to a different pRSM model.

In our pRSM modeling methodology, we first classify design layout configurations into a small number of partitions, build a RSM model and error LTE model for each partition. The layout configuration partitioning approach results in higher quality model fits for given model form. In this paper we describe our pRSM methodology consisting of the criteria to slice layout configurations into different partitions and LTE model forms. We also present results illustrating the advantages of our pRSM methodology over that of traditional RSM approaches and describe briefly a model calibration environment used to generate pRSM models.

7488-138, Poster Session

Effect of SRAF placement on process window for technology nodes that uses variable etch bias

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Process window boundary for 45nm node and below become very close, which makes small shift in SRAF placement affects the immunity to process variations for certain critical pitches and 2d structures.

During correction flow (OPC), the litho target (resist target) is generated from the original design target (etch target) during an etch simulation. This etch simulation uses a variable etch model that apply variable biases to etch target fragments and generates the litho target (resist target).

SRAF design and optimization is sometimes designed in an early phase of the process characterization, before etch model calibration. In that case, SRAF placement is based on original design target (etch target).

After building and calibrating the etch model, it is possible to generate the resist target by simulating the original design target (etch target) using an etch simulation and output a new litho target (resist target).

Placing SRAF based on resist target will certainly produce different immunity to process window variation for certain patterns. On the other hand, placing SRAF based on resist target could be a challenge because all 1d edges of resist target are divided into fragments with different etch bias.

This work studies what is the optimum approach for SRAF placement for technology nodes that uses an etch model during correction flow. the different SRAF placements that are based whether on original design target or based on generated litho target (resist target) are compared and suggestions are being made to ensure the optimum process window immunity for critical patterns.

7488-141, Poster Session

FPGA as the programable tool for yield improvement

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One of the biggest technology challenges at 65nm node is high static power consumption. Static power consumption is largely a result of transistor sub-threshold (source-to-drain) leakage and gate leakage. Poly gate Critical Dimension (CD) has been correlated to transistor sub-threshold leakage and leakage variation; thus, tighter CD control can reduce leakage variation and help to enlarge yield and performance window.

The need to have tight control of CD variation is even more critical for larger die size where one die can occupy the entire reticle field. FPGA flexible programmability feature requires large die size. At same time, such FPGA unique programmability feature can be utilized to study intra-field CD process variation. Based on this process variation information, DoseMapper - a patented technique by ASML - can be used to optimize process parameters to reduce intra-field variation.

By programming FPGA into many local Built-in-Self-Test (BIST) patterns, with each pattern output being a Tilo propagation delay, intra-field Tilo delay can be profiled. Sub-threshold leakage cannot be profiled directly for intra-field; however, majority of leakage current correlates to Tilo delay which can be used to profile the intra-field CD variation and served as guidance for DoseMapper optimization.

In this paper, FPGA programmability is utilized to optimize intra-field process variation in order to maximize 65nm technology yield and performance window. Split results showed that the intra-field CD variation can be reduced by half and subsequently improved yield significantly.

7488-142, Poster Session

Model-based lints for litho-hotspots repair

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A repair for a litho hotspot requires both an identification of specific design layout edges and a set of specifications of how edge modifications to resolve the hotspot. All litho hotspot detection tools can generate a hotspot marker indicating the layout edges directly involved with a hotspot. Identifying the layout edges touching such a litho hotspot marker as primary repair hint candidates is a straight-forward process which can be easily compiled into a set of rules. The challenge is to identify secondary repair hints which involving layout edges not directly adjacency to the hotspot markers. The brute force approach of creating layout variants with potential repair changes followed by a full RET treatment and litho simulations to obtain the new contours is too computational intensive to be practical.

We propose an approach using approximate contour models to estimate the effect on the contour due to design layout modifications. Our work builds upon a modeling methodology called Partition RSM (pRSM) which is builds on standard Response Surface Models(RSM). Our pRSM model methodology contains estimates of contour changes as a function of layout changes as well as error bound estimates of the contour models itself. More details of our pRSM modeling methodology is described elsewhere.

In this paper we present details and results from an implementation of a model based hint(MBH) engine which utilizes our approach. Our hint engine uses pRSM models both to identify the neighborhood shapes and to compute the shape changes amount to resolve a hotspot. The key advantage of pRSM models is that the litho hotspot repair hint engine can utilize the error bound estimates both to guard-band the contour estimate from the pRSM model and to switch to different pRSM. Guard banding is technique to inject more conservatism into the hint engine as to avoid "bad" or ineffective hints. We also describe other features in our MBH engine which allows the specification of both design specific and design rule considerations to constrain the type and number of litho repair hints.

7488-143, Poster Session

What is a good empirical model for OPC?

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An accurate process model is of utmost importance to optical proximity correction (OPC). There are many parameters and methodologies in constructing and calibrating a model. We set out to define the practical guidelines in determining the quality of an OPC model, so that we know where to turn and when to stop in the hunt for a good model. The guidelines are framed in Fisher theory of estimation, especially its criteria for estimator performance: consistency, sufficiency, and efficiency.

7488-40, Session 9

Correlation of overlay performance and reticle substrate nonflatness effects in EUV lithography

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It has been shown previously that reticle non-flatness results in image placement errors[1]. When multiple device levels are printed using EUV lithography, substrates of different shapes can lead to what we refer to as reticle matching overlay (RMO) errors. This is analogous to matched machine overlay (MMO) in which the stage and lens distortion signatures on multiple exposure tools do not match perfectly, resulting in overlay errors. For multiple reticle overlay, two reticles used on the same tool with the same chucking system can yield relatively large overlay errors if the substrate shapes are different enough. In this paper, we will discuss experiments in which multiple substrates (20 in total) from multiple vendors are compared for substrate shape mismatches. The flatness measurements are performed on a Zygo phase shifting interferometer at the Mask Blank Development Center (MBDC) in Albany. The substrate is held in a vertical mount to reduce gravity-induced substrate sag during the measurements. IP errors resulting from this non-flatness have two separate components: (1)Substrate thickness variations leading to IP errors due to variations in the Z-height of the reticle top surface and (2) In-plane distortion (IPD) induced IP errors resulting from chucking non-flat substrates on a flat chuck. Typically IP error due to IPD is calculated with the help of finite element modeling (FEM) or analytical methods. In this study, the IPE due to IPD is calculated using analytical methods detailed elsewhere[2]. A simple analytical model provides enough accuracy in IP error due to IPD to perform reticle shape matching. The total error is the sum of IPE due to IPD and IPE due to Z-height variation. We present an analysis of all 20 blanks for the best and worst overlay signatures when used for printing multiple device levels. A comprehensive analysis of scanner correctable and non-correctable errors for different substrate shapes will also be presented. Non-flatness specifications for EUV blanks will be reviewed based on these reticle matching results. As an example, two relatively non-flat substrates may be adequate if the final IP error signatures for these substrates match under EUV exposure.

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7488-41, Session 9

Etch process development of different blank structure for EUV mask production

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As Extreme Ultraviolet Lithography (EUVL) is the favorite next generation lithography candidate for IC device manufacturing with feature sizes beyond 32nm, the etch process of the EUV mask become more essential in enabling the overall success of EUV lithography and the requirement on critical dimension (CD) and side wall profile of EUV mask control becomes ever stringent. Therefore, for satisfying the tight CD uniformity and linearity requirements listed in the SIA roadmap, it is necessary to optimize the etching processes for gaining proper selectivities between absorber, buffer and capping layers and adequate profile and low etch bias.

In this paper, we use two type blank masks of different stacks. The purpose of this study is to understand the etch characteristics for patterning Ta-based EUV mask, which will enable us to determine robust process condition in terms of CD performance and profile control. The etch process of Ta-based EUV mask is investigated with inductively coupled plasma (ICP) of fluorine-containing and chlorine-containing gas chemistries.

7488-42, Session 9

Thin absorber EUVL mask with light-shield border for full-field scanner

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Extreme Ultraviolet lithography (EUVL) is one of the most promising lithography to attain ULSI devices with 32nm half-pitch (hp) and beyond. Mask plays a key role in lithography and should be regarded as an integral part of a lithographic system. One of the requirements for EUVL mask is high lithographic performance, such as high image contrast, low shadowing effect owing to reflective mask and oblique illumination. In the previous papers, we demonstrated that shadowing effect could be reduced without loss of printability performance by applying thinner LR-TaBN absorber. When the thinner absorber mask is practically applied to actual EUVL for ULSI chip production, it is inevitable to introduce EUV light shield area into mask-frame region which suppresses leakage of the EUV light from adjacent exposure shots. We also proposed and fabricated two thinner absorber masks with EUV light shield areas. One is stacked absorber type of light shield area structure and the other is multilayer etching type. For both types of masks, we demonstrated high performances at light shield areas by employing a Small Field Exposure Tool (SFET).

From the view point of mask process flexibility for higher mask CD accuracy, we believe that the multilayer etching type of light shield structure is more promising than the stacked absorber type. It is, however, worried about some stress changes caused by multilayer etching. In this paper, we evaluate the thinner absorber EUVL mask with the multilayer etching type of light shield structure by focusing mainly on mask substrate flatness and position accuracy.

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7488-43, Session 9

EUVL ML mask-blank fiducial mark application for ML defect mitigation

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Fabricating defect-free extreme ultraviolet lithography (EUVL) multi-layer (ML) mask blanks presents a big challenge in EUVL technology. ML defect sources primarily come from substrate defects and ML deposition adders. Defect reduction, therefore, needs to address many development aspects, such as substrate material, substrate polishing, substrate cleaning, blank handling, and ML deposition. High investment cost and potential low blank yield can quickly drive up EUVL cost of ownership. However, allowing a few defects on the ML blank can improve the blank yield drastically. Utilizing such defect-blanks through defect mitigation schemes has been proposed. It includes directly repairing small ML phase and amplitude defects, mask absorber pattern proximity repair, and using absorber pattern to cover the ML defects. It includes directly repairing small ML phase and amplitude defects, repairing mask absorber pattern to compensate the effect of an adjacent ML defect, and using absorber pattern to cover the ML defects. In each case, the ML defects will first need to be identified and located during the ML blank defect inspection. To precisely locate the ML defects

on the blank, fiducial marks on the ML blank are needed for mask alignment and defect location identification.

In this paper, we will present the details of a ML defect mitigation process flow, i.e., using absorber pattern to cover the ML defects, and the corresponding experimental validation of this mitigation flow. We will also discuss the fiducial marking scheme, its application in the defect mitigation flow, the error budget of ML defect mitigation, such as defect position measurement error, fiducial mask position error, e-beam alignment errors, etc.,

7488-44, Session 9

Optimized mask structure for the reduction of shadow effect on 22-nm node

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Extreme ultra-violet lithography (EUVL) was believed to be one of the strong candidates for the patterning of 22 nm node and below. The EUV light shining 6 degrees oblique incidence to the mask, do not get the desired critical dimension (CD) because the shadow effect influences to the pattern. Thus, many researchers studied the mask modification for reducing the shadow effect such as the phase-shift mask (PSM) or the sidewall angle decreased mask.

In this paper, a new etched multilayer binary mask is suggested for reduction of shadow effect on 22 nm node. First, we compare the designed new etched multilayer binary mask with the binary mask that the absorber part was replaced with other material instead of multilayer. The reduction of the shadow effect on this new structure will be reported. Second, the influence of the various materials of the absorber in etched PSM mask is studied and most effective material for the 22 nm patterning is sought. We used the horizontal-vertical bias as a metric for the new mask structure. Through this study, our suggested new etched multilayer binary mask has a good aerial image and shows better contrast compared to the binary mask. Thus, we can minimize the shadow effect in EUV with a new mask structure.

7488-45, Session 9

Actinic EUVL mask-blank inspection capability with time-delay integration mode

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Extreme Ultraviolet lithography (EUVL) is a promising technology for ULSI devices with a half pitch of 32 nm and below. However, the fabrication of defect-free mask blanks and their inspection continue to be a matter of concern for the implementation of EUVL. A multilayer phase defect is initiated by some kind of disorder in the multilayer that is generated during the multilayer film growth if a particle or a pit happens to reside on a quartz substrate surface. Because this kind of defect is hardly noticeable on the mask blank surface with a conventional inspection system, an actinic (at wavelength) defect inspection technique is being pursued.

To address this issue we have developed an actinic full-field EUVL mask blank inspection system to detect multilayer phase defect by employing a dark field imaging technique. Based on our estimation of impact of a phase defect on a wafer for 22 and 32 nm HP devices, we maintain that our target of inspection sensitivity was to capture a phase defect caused by a 1.5 nm-high and 40 nm-wide protrusion on a multilayer surface. In this system the light scattered from the mask blank surface propagating in a direction between the inner and outer NAs of a Schwarzschild optics reaches a CCD camera where a defect is captured as a spot signal brighter than the background intensity of the surrounding area. The mask blank stage of the system scans the full field of a mask blank to capture images with time delay integration (TDI) method. With the obtained images, the system can detect a defect as a spot signal brighter than a pre-determined threshold. The threshold was determined to be far larger than variation of the background intensity so that the system cannot detect the variation as a defect, referred as 'false defect detection'. Using this threshold, programmed phase defects on a mask blank were observed with stage scanning. The result was that the system detected 1.5 nm-high and 60 nm-wide defect with few false defect detections in the case of 1mm/s scan velocity. This scan velocity indicates that the inspection time is 10 hours per mask.

To maintain the defect sensitivity, stability of defect signals plays a key role because the signal intensity of such a small defect is weak. For this work, several mask blanks were inspected at full-filed area with the actinic inspection system where the parameters for stable full-filed inspection, stability of the defect signal intensity for example, were evaluated. Furthermore, the latest status of the inspection system will be reported.

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7488-46, Session 10

Development of multiple-pass exposure in electron-beam direct-write lithography for sub-32-nm nodes

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Electron beam direct write (EBDW) lithography has been successfully integrated in the ASIC manufacturing industry to sustain optical lithography for prototyping applications, low volume production and for the development of the next technological nodes. As microelectronics is now moving towards the 32nm node and beyond, new patterning techniques are required to reach such resolutions. With the multi beam solution, electron beam lithography is an interesting technique to meet the requirements of sub-32nm nodes. However the standard proximity effects correction methods based on dose modulation are not sufficient to provide the required patterning accuracy and dimensions control. A new writing strategy is needed to push the resolution capabilities of electron beam lithography. In a previous paper a new writing strategy based on multiple pass exposure has been introduced to pattern critical dense lines. It consists in adding small electron Resolution Improvement Features (eRIF) on top of the nominal lines. The eRIF and the lines are exposed in two successive passes with complementary doses. Compared to the standard exposure, this solution increases the amplitude of the dose profile. This helps to enlarge the energy latitude and to reduce the line edge roughness. It was also shown that the energy latitude and the line edge roughness can be tuned by adjusting the size and the dose of the eRIF.

This paper will deal with the application of the multiple pass exposure technique to the sub-32nm nodes. A detailed analysis will be done to optimize this new approach. To do so the gains obtained with the multiple pass exposure in term of energy latitude, line edge roughness and dose to size will be studied. First investigations show that the dose, the size and also the placement of the eRIF have a huge impact on the energy latitude and the dose to size. In this paper we will analyse in detail the influence of the design of the eRIF for the sub-32nm nodes. The best conditions in term of dose, size and placement of the eRIF will be used to establish design rules for the multiple pass exposure. Finally we will study the impact of the multiple pass exposure strategy on the throughput of EBDW lithography. It will be shown that a trade off has to be found between the writing speed and the improvement of the energy latitude and the line edge roughness.

7488-47, Session 10

Charged particle multibeam lithography evaluations for sub-16-nm hp mask node fabrication

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A detailed evaluation study will be presented with respect to the suitability of projection electron and ion multi-beam lithography [1] for the fabrication of leading-edge complex masks.

The presentation will include recent results as obtained with electron and ion multi-beam proof-of-concept systems with 200x reduction projection optics where patterns are generated on substrates using a programmable aperture plate system with integrated CMOS electronics generating several thousand of well defined beams in parallel.

A comparison of electron and ion projection multi-beam writing will be provided, in particular with respect to the suitability to expose non-chemically amplified resist (non-CAR) materials.

The extendibility of projection multi-beam technologies for 16nm, 11nm and 8nm hp mask nodes will be discussed.

[1] E. Platzgummer et al., Proc. SPIE Vol. 7122 and BACUS Newsletter Feb2009.

7488-48, Session 10

Electron-beam mask writer EBM-7000 for Hp 32-nm generation

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Semiconductor scaling is expected to soon reach hp 32nm generation, while limitation is already in our view. Then, such various lithography candidates as double patterning, EUV, imprint, complicated mask, source optimization are being pursued. As any of the lithography methodologies requires aggressively high accuracy with fine resolution without incurring unreasonably long write time even for the substantially high shot counts, a new tool is demanded.

Thus, NuFlare Technology Inc. has developed an electron beam mask writer, EBM-7000 on a new platform to cope with the situation. Electron optics system is designed to have low aberrations with high current density of 200 A/cm2. As presented at last BACUS2008, it has pattern resolution of about 30 nm for 1:1 lines and spaces.

In addition, stage and digital-analog converter (DAC) for deflectors have also been improved. The stage is more simplified than that used for previous EBM writers and designed with higher stiffness to reduce mechanical noise, distortion and external contribution factors. DAC is also designed to reduce electronic noise. As a result, image placement accuracy has been substantially improved as to achieve a few nm with our test pattern. Similar figure of overlay accuracy between 2 masks is also obtained.

Local CD uniformity (LCDU) performance is virtually same as the one for EBM-6000 because shot noise effect, in which the statistical distribution of electrons in resist induces line edge roughness and eventually degrades LCDU, is the dominant error source. LCDU in 3 obtained with PRL009 resist (FUJIFILM Electronic Materials Co,, Ltd.) is 1-1.5 nm. For global CD uniformity (GCDU), process stability is becoming more and more influential. The error estimations of GCDU will have to be discussed separately.

In the area of data path, block size which is to define a unit size of data processing in data divisions or expansion to make shaped shots of the EB writer is designed to be variable to efficiently handle any scale volume data. The block size can be selected to optimum size depending on data volume. The data in each block is processed with PC cluster system in parallel. Thus, the data processing speed of 500MB/s, fast enough to bury the process time within exposure time for hp32nm generation, is achieved.

In this paper, system configuration of EBM-7000 with accuracy data obtained is presented.

7488-49, Session 10

Exposure results with four-column cells in multicolumn EB exposure system

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In the Mask Writing Equipment Technology Research Laboratory of ASET MASK-D2I project, we have assembled an e-beam multi-column-cell (MCC) exposure system made up of four column cells for the proof-of-concept (POC) of MCC with character projection (CP) technology.

We have evaluated the variations in beam position and current density in one column cell caused by deflections in other columns. We could conclude that there is no impact from deflections in other column cells in the POC system. So we could calibrate individually the beam path in each column cell without any influences from other column cells. The calibration could minimize the current density deviations of the beams to select CP patterns down to within 0.2 %.

We are exposing various patterns to evaluate exposure accuracy of the POC system. We measured stitching accuracy between deflection fields in each column cell, and are investigating to improve the accuracy in each column cell. We also started an evaluation of the stitching between patterns exposed with different column cells in the POC system. Our system can measure landing positions of beams in each column cell with a mark detection method of the same mark on a common stage. Furthermore, the stage position for each column cell is measured with an interferometer referring to the corresponding column cell position. In the conference, we will show exposure patterns and will discuss evaluation results of exposure accuracy of the four-column-cell system.

7488-50, Session 10

Enabling photomask technology for large and small displays

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The commercial availability of large LCD panels at attractive prices depends on efficient production with 1X projection of large photomasks onto huge glass substrates, each one of them holding several display screens. The size of a pixel is typically 200 x 65 microns and the pixel transistor has a gate length of five microns. Compared to semiconductor dimensions this seems like easy lithography. The reality is that, due to the gray-scaling in the display, the varying viewing angles and the surprising discrimination or errors by the human eye, errors in mask and process must be controlled with utmost precision. Relative CD errors must be maintained to within sub-percent levels and the registration tolerance is of the order of 10^-7. Furthermore, subresolution mask features and multilayer masks are increasingly brought into use, forcing mask makers to advance their technology continuously. The success of LCD screens and the ever-improving image quality demonstrates how successful the industry has been in improving litho quality and at the same time lowering the cost per unit area.

The future holds new challenges with 3D displays, OLEDs and active electronics on the glass - or the plastic foil! In order to succeed these display technologies must advance the image quality further, while

accommodating new elements like more complex circuitry and lenticular screens. The learning that has taken place for large LCDs must also be used for the production of small displays for personal display devices, digital cameras and electronic books. Mask makers will have to provide both larger and smaller masks with still better fidelity, higher resolution, better quality control and new features, and equipment makers need to support this in an economic and timely fashion.

7488-51, Session 11

Results of an international photomask linewidth comparison of NIST and PTB

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In a contribution at the BACUS conference 2008 the approach to a bilateral photomask linewidth comparison of NIST and PTB, the mask standards used and the measurement and analysis methods applied at both institutes were presented [1]. In the follow-up contribution of this year the main focus will be on the presentation and discussion of the status of the comparison measurement results and their implications for CD control in photomask manufacturing.

The mask standards used for the bilateral comparison between NIST and PTB are a NIST SRM 2059 mask standard [2] and a mask standard of PTB design [3] which was manufactured and made available for the bilateral comparison by the Advanced Mask Technology Center (AMTC) in Dresden.

The linewidth or CD measurements on the photomask standards have been carried out by a combination of different techniques, namely CD-AFM and UV transmission optical microscopy at NIST and CD-SEM and UV optical transmission microscopy, supported by additional AFM characterizations, at PTB. The smallest line feature sizes present on the mask standards are nominally 250 nm on the NIST SRM 2059 mask standard and nominally 40 nm on the mask standard of the PTB design. We are going to measure and compare the results down to the nominal 100 nm line features on this mask.

The definition of the measurands will be clearly stated and defined, as e.g. width of the line at 50% of the line feature height. For every measurement method applied, a suitable model for determination of the measurand from the microscope image has to be applied. For each of the linewidth measurement results the associated measurement uncertainty values will be specified according to accepted international guidelines [4]. This paper will present and discuss the comparison measurement results in view of the associated measurement uncertainty values.

The support of the international mask comparison by the AMTC and by the NIST Office of Microelectronic Programs is gratefully acknowledged.

[1] Potzick, J.; Dixson, R.; Quintanilha, R.; Stocker, M.; Vladar, A.; Buhr, E.; Häßler-Grohne, W.; Bodermann, B.; Frase, C.-G.; Bosse, H.: International photomask linewidth comparison by NIST and PTB; SPIE Conference on Photomask Technology 2008, Monterey, 06-10, October, 2008; Proceedings of SPIE on CD-ROM 7122 (2008),

[2] NIST SRM 2059 is available from the Office of Standard Reference Materials, NIST, EM 205, Gaithersburg, MD 20899. Voice 301-975-6776, FAX 301-948-3730.

[3] Richter, J., et al: “Calibration of CD mask standards for the 65 nm mode: CoG and MoSi”, EMLC 2007, 23rd European Mask and Lithography Conference EMLC, Proc. SPIE: 6533, (2007), 65330S-1 - 65330S-10.

[4] Guide to the expression of uncertainty in measurement, ISO, 1995, 110 p., ISBN 92-67-10188-9.

7488-52, Session 11

Measurement sampling frequency impact on determining magnitude of pattern placement errors on photomasks

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Current methodologies for determining pattern placement errors on production masks is based primarily on limited sample sizes and Gaussian statistics. This methodology and accepted practice may not be indicative of the true nature of pattern placement errors actually occurring on the photomasks. Pattern placement errors can originate from a variety of sources on e-beam generated photomasks. Random shot placement errors, localized charging, global charging, and writing strategies may all have an impact on overall pattern placement errors. It is suspected that the pattern placement errors on the photomasks are not distributed in a Gaussian manner, but are in fact a function of various frequency sensitivities. This paper investigates different measurement sampling frequency strategies on a leading edge poly layer to determine what level or amount of measurements are necessary to more accurately determine the probabilities of the true placement errors on the photomask, and what frequency components may or may not be included in the errors.

7488-53, Session 11

An 193-nm optical CD metrology tool for the 32-nm node

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A novel optical critical dimension (CD) metrology tool equipped with a 193 nm laser source and high numerical aperture objectives (NA=0.9) is under development at the Physikalisch-Technische Bundesanstalt (PTB)), the National Metrology Institute of Germany. The tool is designed for characterization of photomasks up to 6-inch and offers ‘at-wavelength’ measurement for current and future 193 nm lithography.

A pulsed 193 nm ArF excimer laser (Coherent OPTexPro-T) is used as the light source in the system. The DUV laser beam is then delivered to the microscope body by means of a multi-mode optical fiber, reducing potential negative influence of laser acoustical noise and vibrations. Furthermore, by carefully choosing the fiber coupling method and the multi-mode fiber length, highly incoherent laser light could be obtained directly after the fiber. An experimental investigation of the actual quality of the incoherent light with the ‘double-slit’ method has verified the validity of the concept.

The illumination and imaging system of the 193 nm DUV microscope will provide various imaging capabilities ranging from ordinary bright-field to special structured illumination schemes, which help to further enhance the flexibility and performance of the microscope.

Traceability of the characterization results to the SI unit ‘meter’ will be accomplished by means of laser interferometry. A differential laser interferometer (Renishaw RLD) with sub-nanometer resolution is employed to measure in-situ the relative displacement of the structures under test within the object plane of the microscope. The mechanical set-up of the metrology tool has been designed with the help of finite element analysis to realize a positioning stability in the nanometer range.

This newly developed microscope will enable linewidth measurements of micro- and nanostructures with an unsurpassed measurement uncertainty of down to 10 nm (95 % confidence interval). Due to its higher resolution and lower uncertainty, the DUV microscope will be even applicable and suitable for the 32 nm technology currently in development.

7488-54, Session 11

How much is enough? an analysis of CD measurement amount for mask characterization

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The demands on CD (critical dimension) metrology amount in terms of both reproducibility and measurement uncertainty steadily increase from node to node. Different mask characterization requirements have to be addressed like very small features, unevenly distributed features, contacts, semi-dense structures to name only a few. Usually this enhanced need is met by an increasing number of CD measurements, where the new CD requirements are added to the well established CD characterization recipe. This leads straight forwardly to prolonged cycle times and highly complex evaluation routines. At the same time mask processes are continuously improved to become more stable. The enhanced stability offers potential to actually reduce the number of measurements. Thus, in this work we will start to address the fundamental question of how many CD measurements are needed for mask characterization for a given confidence level.: We used analysis of variances (ANOVA) to distinguish various contributors like mask making process, measurement tool stability and measurement methodology. These contributions have been investigated for classical photomask CD specifications e.g. mean to target, CD uniformity, target offset tolerance and x-y bias. We found depending on specification that the importance of the contributors interchanges. Interestingly, not only short and long-term metrology contributions are dominant. Also the number of measurements and their special distribution on the mask layout (sampling methodology) can be the most important part of the variance. The knowledge of contributions can be used to optimize the sampling plan.: As a major finding, we conclude that there is potential to reduce a significant amount of measurements without loosing confidence at all. Here, full sampling in x AND y as well as full sampling for different features can be shortened substantially almost up to 50%.

7488-55, Session 12

Photomask metrology using a 193-nm scatterfield microscope

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The current binary photomask linewidth Standard Reference Material (SRM) supplied by the National Institute of Standards and Technology (NIST), SRM 2059, is the fifth generation of such standards for mask metrology. The calibration of this mask has been historically carried out using an in-house NIST ultra-violet transmission microscope and more recently in combination with a Atomic Force Microscope (AFM).

Recently, a new optical reflection scatterfield microscope has been developed at NIST for critical dimension (CD) and overlay metrology purposes. Scatterfield microscopy is a set of optical techniques we have been developing over the last several years that rely on illumination and collection optics engineering. These techniques rely on structured illumination for static imaging or scanned illumination applied in a high magnification scatterometry platform with a sufficiently large Conjugate Back Focal Plane (CBFP) (transmission or reflection). Our new scatterfield reflection microscope, which uses 193 nm excimer laser light in various sophisticated configurations, has been constructed to allow measurement of both the image plane and the Fourier plane using full-field and angle-resolved illumination. By reducing the wavelength compared to many current metrology tools that work in the visible and near ultra-violet light range, we have made substantial improvements in image resolution and commensurate gains in sensitivity to geometrical parameters.

In the proposed paper, the 193 nm scatterfield reflection microscope and the UV transmission microscope are used in full-field mode and angular mode by engineering their CBFP to enable angle-resolved scatterometer measurements with an illumination NA range from 0.08 to 0.70 and 0.0 to 0.60 respectively. Experimental results obtained on SRM mask features (isolated lines) for different polarization states of the illumination will be presented and discussed. Results will also be compared between measurements performed on our optical microscopes and the CD AFM. Finally, we will evaluate assumptions of the modeling and uncertainties and we will present future improvements.

7488-56, Session 12

Experimental test results of pattern placement metrology on photomasks with laser illumination source designed to address double-patterning lithography challenges

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The Double Patterning Lithography (DPL) Technique for wafer exposures is placing greater demand on the requirements for pattern placement accuracy on photomasks. The distortion influence of the pellicle on plate bending is also a factor especially when the pellicle distortions are not repeatable substrate to substrate. The combination of increased demand for greater accuracy and the influence of pellicle distortions are key factors in the need for high resolution through pellicle in-die measurements on actual device features. A key enabler of this capability is measurement resolution. Measurement resolution is typically defined by the Rayleigh equation of lambda divided by the numerical aperture of the lens in the optical system. Utilization of continuous wave lasers offers advantages such as narrow bandwidth over pulsed lasers. This allows for the design and manufacture of high numerical aperture long working distance lenses. Resolution of features for pattern placement measurements is not as rigorous as measurement for critical dimensions as features are typically defined by the center points of two edges in both the X axis direction and the Y axis direction. This paper reports on the initial experimental results of 266 nm continuous wave laser illumination on features of various sizes using unique measurement algorithms developed specifically for pattern placement measurements.

7488-57, Session 12

In-die metrology on photomasks for low-k1 lithography

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New lithography techniques like Double Patterning, Computational Lithography and Source Mask Optimization will be used to drive immersion lithography to its limits. This results in several challenges for the mask maker. The extremely high MEEF values amplify small process variations on the mask features on the wafer. Complex mask features using sophisticated OPC and assist features as well as double patterning tightens the registration and CDU specification at the same time. Especially, overlay and registration become critical and must be ensured on every die. In-die registration and CD metrology on arbitrary features is required to measure mask performance precisely.

These requirements have driven the development of new mask metrology tools at Carl Zeiss, especially for CD and registration.

In this paper an overview about several in-die metrology techniques will be given. Applications of in-die CD measurements using the Zeiss WLCD tool as well as in-die registration measurements using the Zeiss Prove tool will be shown and discussed.

7488-58, Session 12

Critical dimension uniformity using reticle inspection tool

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The Critical Dimension Uniformity (CDU) specification on photomask is getting increasingly tighter which each successive node. The ITRS roadmap for optical masks indicates that the CDU (3 sigma) for dense lines for binary or attenuated phase shift mask is 3.4nm for 45nm half-pitch (45HP) node and will go down to 2.4nm for 32HP node. The current capability of mask shop processes results in CDU variation across the photomask of a similar magnitude.

Hence, we are entering in a phase where the mask CDU specification is approaching the limit of the capability of the current Process of Record (POR). Mask shops have started exploring more active mechanisms to improve the CDU of the mask. A typical application is in feeding back the CDU data to adjust the mask writer dose and compensate for non-uniformity in the CDs, resulting in improved quality of subsequent masks. For this purpose mask makers need a dense measurement of CDs across the reticle in a short time. A dense mask CDU map can also be fed-forward to the lithography scanner tools to adjust the dose across the exposure field and improve the printed wafer CDU.

Mask makers are currently using the CD-SEM tool for data collection. While the resolution of SEM data ensures its position as the industry standard, an output map of CDU from a reticle inspection tool has the advantage of denser sampling over larger areas on the mask. High NA reticle inspection systems scan the entire reticle at high throughput, and are ideally suited for collecting CDU data on a dense grid.

In this paper, we describe the basic theory of a new, reticle inspection-based CDU tool and results on advanced memory masks. We discuss applications of CDU maps for optimizing the mask manufacturing process.

7488-59, Session 12

IntenCD technology for fast and accurate scanner performance: determination

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Scanner performance is measured against its illumination, optical and mechanical elements contributions to the final printed errors on wafers. Isolation of those combined scanner errors from other sources is a challenging task since the total error budget of the lithography process consists of many dynamic varying sources, such as wafer pre imaging of planarity and stack properties.

The mask is conceived as part of the scanner optics and integral to the imaging process. Therefore mask errors contribution to the overall error budget becomes crucial for any advance litho process evaluation.

Discrete mask measurement techniques are currently being used to create across-mask CDU maps. By subtracting these maps from their final wafer measurement CDU map counterparts, it is possible to assess the real scanner induced printed errors, with certain limitations. The current discrete measurement methods are time consuming and some overlook mask based effects other than line width variations, such as transmission and phase variations, all of which influence the final printed CD variability.

In this paper we present a novel methodology, which takes advantage of the recently introduced Applied Materials Aera2 mask inspection tool with IntenCD technology. Scanning the mask at high speed, the IntenCD aerial imaging based maps offer full mask coverage and accurate assessment of all masks induced source of errors simultaneously, making it ideal for mask and scanner qualifications.

7488-60, Session 12

New AFM solution for photomask metrology

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With the continuous feature size reduction in photolithography process, the features on photomask will soon shrink to below 100 nm. Also because the use of phase shift mask, the depth control of the features on photomask now become also very important. All these challenge the current photomask inspection and metrology tools. AFM is a very promising nano-metrology tool. It has very high resolution, and it can be operated in air. Also the measurement with AFM is non-destructive, and has no material bias. It is believed that AFM will play an important role in Critical Dimension (CD) and photomask metrology.

The first generation AFM based on piezoelectric tube scanners has high spatial resolution and performs well in qualitative measurements. However, it suffers from poor repeatability and accuracy due to the background curvature and crosstalk between the x-y-z axes, making it inadequate for quantitative metrology.

Here we introduce our new XE-AFM using decoupled XY and Z scanner. This new AFM structure gives our AFM some unique advantages in nano-metrology. The decoupled XY and Z scanner configuration eliminates the crosstalk between all three scan directions. We use flexure scanner for scanning in XY direction. Because of the inherent structure, the flexure scanner can only move in X and Y direction. This gives an ultra flat scan surface. The movement in X and Y are also independent, so XY scanner can be made highly orthogonal. Z scanner uses a dedicated stacked piezo ceramic, which can generate very strong force. With the innovative design, the Z scanner also has very small mass loading, so the Z scanner has much higher band width and response much faster than conventional tube scanner. Because of this, our AFM can do true non-contact mode in air, and this minimizes the tip wearing. All these are very important for reliable and repeatable high precision metrology.

7488-62, Session 13

Advances in CO_2 cryogenic aerosol technology for photomask post AFM repair

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As the mask technology matures, critical printing features and sub-resolution assist features (SRAF) shrink below 80 nm, forcing critical cleaning processes to face significant challenges. These challenges include use of new materials, oxidation, chemical contamination sensitivity, proportionally decreasing printable defect size, and a requirement for a damage-free clean. CO2 cryogenic aerosol cleaning has, for many years, shown potential to offer a wide process window for AFM repair. Previously, the feasibility of CO2 cryogenic aerosol in post AFM repair photomask cleaning was demonstrated. Until recently, CO2 purity and delivery hardware issues resulted in residue adder contamination and SRAF damage below 150 nm critical feature size. Some key desirable properties of CO2 cryogenic aerosol cleaning are the non-oxidizing and non-etching properties when compared to conventional chemical wet clean processes with or without megasonics. In this paper, recent advancements of CO2 cryogenic aerosol cleaning technology are presented, highlighting improvements in the areas of particle adder reduction, electrostatic

discharge (ESD) mitigation, and lowering the critical feature size without damage.

Key aspects of successful CO2 cryogenic aerosol cleaning include the spray nozzle design, CO2 liquid purity, and system design. The design of the nozzle directly controls the size, flux, and velocity of the CO2 snow particles. Methodology and measurements of the solid CO2 particle size and velocity distributions will be presented, and their responses to various control parameters will be discussed. Adder control can be achieved only through use of highly purified CO2 and careful materials selection. Recent advances in CO2 purity will be discussed and data shown. The mask cleaning efficiency by CO2 cryogenic aerosol and damage control is essentially an optimization of the momentum of the solid CO2 particles and elimination of adders. Data on CO2 tribocharge mitigation, the main cause of ESD, will be presented and application to current technology nodes discussed. The previous damage threshold of 150 nm SRAF structures has been reduced to 70nm and data will be shown indicating 60 nm is possible in the near future.

7488-63, Session 14

Developing inspection strategies for nano-imprint lithography

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Reticles used in optical lithography typically contain primary features four to five times larger than their resulting wafer images. Even within these relatively large mask patterns, one primary inspection challenge is to discriminate between randomly occurring defects and intentional RET (Reticle Enhancement Technique) structures such as OPC (Optical Proximity Correction) or SRAF (Sub Resolution Assist Features) of similar size and shape.

Containing nearly the opposite set of characteristics are NIL (NanoImprint Lithography) reticles. Since NIL pattern transfer is achieved by physically contacting a UV curable resist, these mask patterns are free from RET structures which greatly simplifies the detection of pattern and contamination defects. However, such defects lie within 1x primary patterns that far exceed minimum feature size requirements of most traditional reticle inspection systems. Finally, NIL reticles contain only etched quartz features since no chrome or phase shift materials are needed to produce contrasting optical images for this unique lithographic application.

This paper examines some of the NIL inspection challenges and results obtained by using existing production systems designed for traditional optical lithography photomasks. As NIL lithography continues to gain popularity, understanding the pattern and contamination defect requirements and current capabilities is an area of interest to the semiconductor, and alternative, business segments.

7488-64, Session 14

6-inch circle template fabrication for patterned media using a conventional resist and new chemically amplified resists

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Nanoimprint lithography (NIL) is one of the promising candidates for a method of fabricating a patterned media for next generation hard disk drives. The pitch, characterizing the feature size on the media, will become 70-90 nm for discrete-track media in 2010 and 25 nm for bit-patterned media in 2012. Template is the key issue in NIL and two kinds master template fabrication processes have been developed at DNP by using of a 100kV spot beam eb-writer.

Quartz wafer process with a conventional e-beam resist

The template fabrication process, which uses high-resolution conventional resist, for patterned media is almost the same as those for semiconductors except dry-etching process. The 6-inch quartz wafer was etched in the photo-mask tool on a special tray which was made from carving the 6025 substrate. We will report the results of our quartz-etching process. 48nm pitch patterns were resolved in a 2.5-inch diameter circle.

Silicone wafer process with new chemically amplified resist

Conventional e-beam resist has high resolution performance but has a problem of low throughput because of its low sensitivity when it is used at a high acceleration voltage of 100 kV. Therefore, we have examined silicone wafer process with new chemically amplified resist developed in pursuit of high resolution instead of high sensitivity. The reasons to select si-wafer are good etching capability and less quenching at interface. It can be use as maser template for replica quartz template. Target specifications are two times or higher sensitivity than ZEP-resist and a 50 nm pitch or finer resolution. We evaluated a new high-resolution CAR developed by TOKYO OHKA KOGYO Co., LTD. The new CAR patterns were resolved down to at 48 nm pitch, but were collapsed even at 64 nm pitch. To prevent collapse, we tried to optimize baking conditions and to examine primers as promoters of the adhesion between the resist patterns and the substrate surface. And then resist patterns were achieved down to at 48 nm pitch. We will report the results of the performance of the new CAR and fabrication approach of the si-template with the use of the new CAR.

7488-65, Session 14

A new x-ray metrology for characterizing a shape of nanostructure of patterned media

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The use of patterned media is extensively studied in order to overcome superparamagnetic problem and to increase the areal density of magnetic disk drives. In patterned media, the magnetic layer is created as an ordered array of data tracks or isolated bits. The size and the shape of those tracks or bits are directly related with signal intensity and noise of the media, and they are expected to be highly controlled for better read/write performance. However it poses serious challenges for metrology tools to characterize the crucial structure of those patterns with only few-tens of nanometer or smaller dimensions.

In the above situation, we have been trying to develop a new nanoscale metrology by employing x-ray scattering technique. Traditionally, x-ray scattering (diffraction) is used for determining an atomic scale structure of materials. In addition, it is also useful for determine secondary structure of nanometer scale such as segregation of metallic alloys, nanoperticels, nanopores [1], and so on by using so called small angle x-ray scattering (SAXS). When x-rays irradiate surface of substrate on which periodic tracks or islands are fabricated, diffraction peaks come from the periodic structure may be observed. We have already confirmed that the structure of surface gratings with several hundred nanometer pitch could be characterized by means of a grazing incidence ultra-small angle scattering (GI-USAXS) system [2]. We have observed a lot of diffraction peaks from periodicity of the gratings and average pitch of the grating could be determined in very high accuracy based on the known wavelength of Cu K 1 radiation (= 0.154093 nm). Furthermore, we have successfully determined line width and side wall angle by taking into account intensity ratio of the each diffraction and decay late of higher-order diffraction.

We have characterized fabricated patterns having about 100 nm pitch of circular discrete track on 2.5-inch disc by using the present GI-USAXS system. Even though the track line is curved, more than tenth order diffraction peaks were observed and could be estimated line width of the track line. The results are in good agreement with that of scanning electron microscopy. Moreover, the height of tracks is also be measured by the detector scanning along normal to the surface direction. It is difficult to observe height of such a nanostructure nondestructively except x-ray method. We will also show obtained cross-section structures of the track in the presentation.

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[2] Y. Ito, et al., Jan. J. of Appl. Phys. 46, L773 (2007).

7488-66, Session 14

Polymeric soft stamps for patterned media applications

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The move to full-field imprinting is a necessary step for cost-effective manufacturing for applications such as patterned media that require high throughput. Full-field imprinting is typically realized by the fabrication of a "working" stamp using a hard stamp as the master template. This working stamp can then be used in a full-field imprinting process commonly termed as "soft UV-NIL".

Full-field imprint requires the ability to conform to the TTV of the imprinted substrate while maintaining the fidelity of the desired features. A low surface energy, to facilitate the de-embossing process, is also required. Typically, working stamps fall into two groups: soft, polymeric stamps and hard stamps. Both types face issues in their fabrication and the imprint process making their transition to high volume manufacturing environments challenging. Soft working stamps are typically made from Polydimethylsiloxane (PDMS) as this material provides a low surface energy and good conformal qualities. But PDMS is not practical for patterned media imprinting due to the fact that it requires a long, thermal cure under pressure and can have issues with maintaining pattern fidelity at small feature sizes [1].

Hard and flexible working stamps can be used to achieve high pattern fidelity. These stamps are typically made of thinned, flexible glass with the master stamp pattern transferred into the imprinting surface through an imprint and etch process [2]. While this method allows for fine feature sizes (sub-50 nm) to be transferred to an imprint resist with good fidelity, these stamps have several issues that make them undesirable for manufacturing applications. Firstly, their fabrication typically requires costly and time consuming imprinting and etch steps. Secondly, an anti-stiction layer needs to be applied and monitored during processing which adds additional equipment and process steps. Finally, the thickness of these substrates makes them delicate and difficult to handle.

In this paper, we will show results from polymeric "working" stamps fabricated with a novel set of materials and with demonstrated resolution of </= 50 nm over a large area. These materials are either currently commercially available or in pilot production stage. They provide the benefits of high resolution, low cost-of-ownership and simple fabrication when compared with competing solutions. The working stamp can be made directly from the master - eliminating the need for imprinting and etching. Also, one can fabricate sub-masters from the original working stamp using the same class of materials - providing greater flexibility for the master fabrication. The working stamp (and sub-masters) can be fabricated very quickly (a matter of minutes) using only a standard mask aligner as the materials only require UV curing. The stamps have shown the ability to handle multiple imprints. Finally, these materials do not require anti-stiction coatings.

[1] U. Plachetka, et. al., "Comparison of multilayer stamp concepts in UV-NIL" Microelectronic Engineering 83 (2006) 944-947.

[2] Xiaomin Yang, et. al., Toward 1 Tdot/in.2 nanoimprint lithography for magnetic bit-patterned media: Opportunities and challenges, J. Vac. Sci. Technol. B, 26 (6), 2008, 2604 - 2610.

7488-67, Session 14

Inspection for nano-imprint lithography at 32-nm with an advanced e-beam inspection system

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Ultra violet nano imprint lithography (NIL) is one of the candidates of alternative lithography solution for deep nanometer integrated circuit (IC) manufacturing. [1] Defect inspection solution for both the imprint mask and NIL printed wafers is one of major challenges of the NIL development because the small feature size.

In this study, a 32nm programmed defect imprint mask was fabricated and the patterns were transferred to the wafer with the step and flash imprint lithography process developed by Molecular Imprints, Inc. [2] NIL resist patterns on the wafer surface consisted of a static random access memory (SRAM) Metal 1 (M1) cell, dense lines, and dense arrays of pillars. Sizes of the programmed defects ranged from 4 nm to 48 nm with increments of 4 nm. [3]

We used eScan®315, an electron beam inspection (EBI) system developed by Hermes Microvision, Inc to capture the programmed defects in resist patterns. Different from the common EBI applications of voltage contrast (VC) defects capturing [4], [5], [6], [7] and photolithography process window qualification of contact mask, [8] this study required highest resolution of the EBI tool to catch the tiny physical defects. EBI with 10nm pixel size has been demonstrated and capability of capturing program defects sized 8nm has been proven. This study demonstrated the feasibility of EBI as the NIL defect inspection solution of 32nm and beyond.

7488-68, Session 14

SEM CD metrology on nanoimprint template: an analytical SEM approach

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CD metrology is the most needed feedback in nanofabrication and automatic CDSEM-based methods are by far the industrial standard due to its well-established methodology and ease in measurement setup and measurement flexibility. The CD measurements from SEMs consist of two steps, the first being the pixel based electron emission signal intensity profile generation and the second being the algorithm treatment on the generated intensity profile for the dimension determination. However, CDSEM metrology involves uncertainty of the measurement in the second step, because the SEM signal formation is an extremely complex process depending on the pattern geometry, materials, detector setup, and beam voltage. Analytical SEMs are even less optimized for the task of quantitative metrology, especially at the CD ranging below 100 nm.

In this work, we used an analytical SEM for CD metrology applications on quartz nanoimprint template. The machine was tuned and beam characterization was done first to find the best condition for consistent manual operation using BEAMETR beam measurement pattern and software. The optimized beam condition set was then used for image collection on a 60 nm pitch pattern quartz template and the measurements were done using threshold method. In order to discuss the profile effect on the scan signal and the resulting influence on CD measurements, we used CHARIOT simulation software for simulated intensity profile. Sidewall angle, feature profile rounding, and feature height were the major parameters of consideration in simulation. The optimized beam condition was then used as input for the simulated intensity profile. The intensity profile went through measurement algorithm treatment and the sensitivity and the measurement limitation from the parameter varied were discussed. The methodology for minimizing CD algorithm error on profile influence was also discussed.

7488-69, Session 15

Optical metrology for template and disk patterned imprints

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Driven by ever-growing storage areal density needs, the hard-disk drive (HDD) industry is transitioning to patterned magnetic media. This will be the first time that the HDD media industry will use lithography processes that require critical dimension (CD) control. Thanks to nano-imprint technology, the CDs will be smaller than the most advanced semiconductor design rules. Of particular interest for pre-etch templates and disks are resist lateral and vertical CDs, resist residual layer thickness (RLT) and resist side-wall angle (SWA). For post-etch (final) templates and disks, the dimensions of interest are lateral and vertical CDs and side-wall angle (SWA). After introducing the industry's need for accurate and precise metrology, we will present detailed physical arguments and results (simulations and measurements) to illustrate why a spectroscopic ellipsometry based scatterometry technique meets the requirements of discrete track and bit-patterned media roadmaps. Using a Xenon arc lamp with 240nm-900nm spectral range, the diffraction effects on the periodical patterns yield sufficient reflected intensity and polarization variations, to accurately determine the imprinted profiles, for CDs as low as 10nm. Model based sensitivity analysis, and experimental correlations to cross-section SEM images will be discussed for both template and disk imprints, each at pre- and post-etch process steps.

7488-70, Session 15

Mold fabrication for discrete track recording media

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Electron-beam (EB) lithography is a key technology for fabricating a nanoimprint master mold for discrete track recording media (DTR). Not only high resolution and accuracy but also high throughput is required in terms of manufacturing cost. We have already reported 120-nm track pitch (TP) full field (2.5") mold fabrication and have completed that of 90-nm TP, recently. In this paper, we will show some patterning results for 60-nm TP or smaller and also discuss feasibility of EB lithography for bit-patterned media (BPM).

7488-71, Session 15

A nondestructive metrology solution for detailed measurements of imprint templates and media

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This study investigates a non-destructive optical metrology technique, adapted from OCD (Optical Critical Dimension) metrology designed for photomask devices, that furnishes a measurement solution for hard disk drive discrete track recording (DTR) and bit patterned media (BPM) templates and imprints. CD-SEM and AFM measurements can provide only limited information, and cross section SEM measurements are destructive. Because the measurement data must have sensitivity to repeated structures on either transparent or opaque substrates, the optical metrology system described in this study, relies on simultaneous measurement of polarized Reflectance (Rs and Rp) and polarized Transmittance (Ts and Tp), covering a wide wavelength range, from 190 - 1000nm. The quantities "Rs and Rp, Ts and Tp" represent two polarizations of reflectance and transmittance. The transmittance data, Ts and Tp, is particularly important for templates where reflectance is typically less than 3%, and transmittance is of the order of 95%, providing significant sensitivity to parameters of interest. The measured Rs and Rp, Ts and Tp data is analyzed using Rigorous Coupled-Wave Analysis in conjunction with the Forouhi-Bloomer dispersion equations for optical properties (n and k).

A significant difference between the hard disk and photomask samples is the orientation of trenches in patterned samples. Trenches in photomasks are normally periodic line gratings which are orientated along the x or y axes. DTR structures in hard disk drives consist of concentric circles around the disk center. For this reason, the optical metrology system described in this study is given an R- stage. Any position on the disk can be measured by rotating the disk relative to the optical system and changing the radius. In this way, the angle and polarization of incident light is consistent from point to point, without operator alignment errors, and matches the orientation expected for data analysis.

From the measurement and analysis of Rs and Rp, Ts and Tp, feature height, feature width and side-wall angle of DTR and BPM templates and imprints, as well as residual layer thickness of imprints, are accurately determined. Uniformity maps of the measured parameters can be produced in a fraction of a minute, and the ability to quickly obtain detailed structure dimensions at multiple points provides new and valuable information to hard disk drive manufacturers. Simulations of theoretical Rs and Rp, Ts and Tp relating to next generation structures are performed for DTR and BPM templates and imprints, and it is demonstrated that the optical metrology system has the capability to measure future products.

7488-72, Session 15

High-volume step and flash imprint lithography for patterned media

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The Step and Flash Imprint Lithography (S-FIL®)1 process uses drop dispensing of UV curable resists for high resolution patterning. Several applications, including patterned media, are better, and more economically served by a full substrate patterning process since the alignment requirements are minimal. Patterned media is particularly challenging because of the aggressive feature sizes necessary to achieve storage densities required for manufacturing beyond the current technology of perpendicular recording. In this paper, the ability to fabricate Master Templates, Replicate Masters and create Working Templates, and print disks is demonstrated.

The process starts with the fabrication of a Master Template. An example of this process, for 25nm bit patterns, is shown in Figure 1. A high resolution electron beam resist, such as PMMA or ZEP520A is used to define the bit array. Since the pattern is radially symmetric, a rotary stage e-beam tool is required. A chromium lift-off process, followed by a glass etch is used to form the patterns in the template (See Fig 1a and 1b). The Master Template is then replicated by imprinting onto a blank fused silica wafer using an Imprio 11002, a fully automated full disk/wafer imprint system (Figure 1c). After transferring the pattern into the substrate, the Replicate Template can then be used to print on disks to create the patterned media. A final template layout is shown in Figure 2. Depicted along with the patterned media are marks designed to align both the template and the disk.

It is anticipated that bit patterned media will be required for very high density hard drives (~ 1Tb/in2). It is possible, however, that an interim solution such as discrete track media will be adopted for earlier insertion. Discrete track media consists of an array of concentric lines (or tracks), with half pitches on the order of 50nm and below. The formation of the tracks is challenging because of the line densities required over substantial distances.

Pictured in Figure 3 are top-down and cross sectional images of the imprinted tracks at a half pitch of 50nm (See Figures 3a and 3b). Also

shown (Figure 3c) are servo-like patterns that are interspersed between the tracks. This paper will cover the details of both the Master Template fabrication process and the Replicate Template process. Details of the imprint process will also be described. Finally, the prospects for printing smaller bit arrays and finer track pitches will also be discussed.

7488-73, Session 16

Fabless but not fab-careless

T. Hisamura, X. Wu, S. Banerjee, Xilinx, Inc. (United States)

There are two different foundry-fabless working models in the aspect of mask, some foundries have in-house mask facility while others contract with merchant mask vendors. Significant progress has been made in both kinds of situations. Xilinx as one of the pioneers of fabless semiconductor companies has been working very closely with both merchant mask vendors and mask facilities of foundries in past many years, contributed well in above mentioned progress in both technology and services.

Our involvement in manufacturing is driven by the following three elements:

The first element is to understand the new fabrication and mask technologies and then find a suitable design / layout style to better utilize these new technologies and avoid potential risks. Because Xilinx has always been involved in early stage of advanced technology nodes, this early understanding and adoption is especially important.

The second element is time to market. Reduction in mask and wafer manufacturing cycle-time can ensure faster time to market.

The third element is quality. Commitment to quality is our highest priority for our customers. We have enough visibility on any manufacturing issues affecting the device functionality. Good correlation has often been observed between FPGA speed uniformity and the poly mask Critical Dimension (CD) uniformity performance. To achieve FPGA speed uniformity requirement, the manufacturing process as well as the mask and wafer CD uniformity has to be monitored.

Xilinx works closely with our wafer foundry and mask supplier to improve productivity and the yield from initial development stage of mask making operations. As an example, defect density reduction is one of the biggest challenges for mask supplier in development stage to meet the yield target satisfying the mask cost and mask turn-around-time (TAT) requirement. Historically, masks were considered to be defect free but at these advanced process nodes, that assumption no longer holds true. There is a need to be flexible enough on unrepairable defect for advanced masks but also a need for efficient risk management system on mask defect waivers. Mask defects are often waived in low design criticality area in favor of scrapping the mask and delaying the mask and wafer schedule.

Xilinx's involvement in mask manufacturing has contributed significantly to our success in past many technology nodes and will continue.

7488-74, Session 16

A universal mask management relational database

P. Morey-Chaisemartin, XYALIS (France)

With the emergence of submicron technologies new product development costs have soared to reach an average of $15M. This includes all direct and indirect costs from specification to the start of volume production. At 65nm a single mask set costs more than $1M. As statistically final silicon needs at least one rework on metal layers, we can roughly estimate that mask budget is at least 10% of the chip development.

It is then obvious that IDM companies as well as fabless design centers must take special care for mask management. Any mistake during all mask data preparation and ordering process has a dramatic impact on cost and schedule. Improving data exchange between mask data preparation teams and mask shops by using the SEMI-P10 standard has been a great step, but building an internal mask data preparation database to warrant a safe traceability of all masks still remains a challenge.

Most major IDM companies have already developed some mask management solution, but often incomplete and not fully integrated. Smaller companies, which still represent 25% of the mask business, do not have the time and bandwidth to develop a robust mask management solution.

Statistics on mask supply chain show that we are facing the classical Pareto rule: 80% of the problems will be related to 20% of the masks.

Additionally, very few in-house solutions allow back tracking of mask making problems discovered by the mask shop during writing or more often inspection of the masks, though the tracking and analysis of such data would lead to a better design process, aware of the challenges of mask fabrication.

We have developed a relational database, which manages all the data related to mask data preparation during the entire life of the project. This database is not only dedicated to mask ordering, it also includes feedbacks on mask manufacturing from the mask shop and on silicon manufacturing from the production line making mask traceability possible.

Such a universal mask management database offers large semiconductor companies as well as small players in the business an operational solution for their mask management, which warrants interoperability between all mask suppliers.

This paper describes the miscellaneous information related to mask ordering and tracking, which need to be managed as well as all the relations between these data. In order to make this information shareable by everybody, a clear definition of what is behind each keyword is given.

The relation between the data stored in the universal management database and the SEMI-P10 standard is also explained. Finally the focus is made on the formalization of the data returned by the mask shops and its impact on design and yield improvement.

This development has been partially sponsored by a European research project (Crystal) and made in collaboration with IDM companies, EDA companies and Mask Shops.

7488-75, Session 17

Deployment of OASIS.MASK (P44) as direct input for mask inspection of advanced photomasks

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With each new process technology node chip designs increase in complexity and size leading to a steady increase in data volumes and mask data prep flows require more compute resources to maintain the desired turn around time (TAT) at a low cost. The effect is aggravated by the fact that a mask house operates a variety of equipment for mask writing, inspection and metrology - all of which until now require their specific data formatting. An industry initiative sponsored by SEMI has established new public formats OASIS (P39) for general layouts and OASIS.MASK (P44) for mask manufacturing equipment that allow for the smallest possible representation of data for various applications. The paper will review a mask data preparation process for mask inspection that is based on the OASIS formats and reads OASIS.MASK files directly in real time into the machine. An implementation based on standard parallelized compute hardware will be described and characterized demonstrating throughputs required for 45nm and 32nm technology nodes. An inspection test case will be reviewed.

7488-76, Session 17

Mask data prioritization based on design intent

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Mask D2I/ASET has been working to reduce TAT for mask writing and inspection. We have been developing a data flow for mask manufacturing in which we refer design intent information in order to reduce TAT of mask manufacturing processes. We convert design level information "Design Intent (DI)" into priority information of mask manufacturing data "Mask Data Rank (MDR)" so that we can identify the importance of reticle patterns from the view point of design side. As a result, we can reduce mask writing and mask inspection time justifiably. Our target is to build efficient data flow converting DI to MDR.

Automatic DI creation flows from EDA tools and an automatic MDR creation flow from the created DI were already established. We extracted design intents (Litho hotspot area, Shield net, Gate channel area, Timing critical net, Dummy metal fill, Power ground net, etc.) from database in EDA tools automatically, and converted them into MDR. By using this flow, we already showed TAT reduction in mask writing and mask inspection for only limited number of design data. In this presentation, we will show TAT reduction results for actual device design data, and we will discuss issues and their solutions.

7488-77, Session 17

Favorable hierarchy detection through Lempel-Ziv coding-based algorithm to aid hierarchical fracturing in mask data preparation

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Fracturing process in Mask Data Preparation (MDP) is a compute intensive and time consuming process. The input to fracturing could be design layout data in GDSII or OASIS format, or in intermediate mask data formats (like MEBES or OASIS.MASK). In case of re-fracturing, the input to the fracturing algorithm could even be in machine-specific mask formats. Most fracturing algorithms are designed to exploit available hierarchy in input data to improve the turn-around-time as well as to reduce the size of mask data. However, in practice, it is found that even if the input data is hierarchical, it may not be favorable for fracturing if there are too many interactions between the different nodes (or cells) of the hierarchy. Usually, if polygons belonging to different cells in the hierarchy overlap with each other, the hierarchy is considered not-too-favorable for hierarchical fracturing. These scenarios are very frequently encountered in system LSI designs where quite complex hierarchies are very common. In such cases, the fracturing algorithm must resolve the overlaps between polygons before fracturing, which in turn results into less amount of effective hierarchy. Apart from this, the aggressive OPC steps are also known to reduce the hierarchy of the original layout data to a large extent.

In this paper, we present a technique where input design layout with not-too-favorable hierarchy or almost flat mask data can be converted into favorable hierarchical data. This will speed up the fracturing or re-fracturing steps and also minimize the output fractured data size. In general, because of inherent regularity in most designs, the layout contains large number of repetitive patterns of polygons. In this proposed technique, we find such repeating polygonal patterns and generate a favorable multilevel hierarchy. Firstly, the overlaps among the polygons in the input data are resolved, followed by identification of polygonal patterns that repeat in different locations. For finding such repetitions, we use a modified version of Lempel-Ziv (LZ) coding algorithm which was originally devised for compressing character strings. We apply the modified LZ algorithm on the signatures of polygons in the geometrical data. All polygons located within a neighborhood of interest are selected in each step and passed to a modified LZ filter. The LZ filter maintains a look-up table of recurring multi-polygonal patterns. The filter is similarly applied on all candidate neighborhoods in the layout. The implication of this is that the LZ look-up table records the sets of multi-polygonal patterns that repeat a large number of times. From such sets of polygonal patterns, a favorable multi-level hierarchy is generated. The characteristic of such a multi-level favorable hierarchy is that the polygons do not overlap with each other even though the bounding boxes of cells containing these polygons could overlap with each other. Apart from the obvious benefits of reducing fracturing time through hierarchical fracturing, such a favorable hierarchy allows considerable reduction in fractured data size as most mask data formats allow two-levels of hierarchy. The paper describes experimental results of favorable hierarchy detection on a number of test cases.

7488-79, Session 17

Latest results and computing performance of the ePLACE data preparation tool

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At the EMLC 2009 in Dresden the data preparation package ePlace was presented for the first time. This package has been used for quite different applications covering mask write, direct write and special applications. In this paper we will disclose results achieved when using the ePlace package for processing of layout data of immediate interest. During the evaluation phase of the new solution we could benefit from broad the experience we collected over many years with the fracture performance of the MGS software which is one core element of today's ePlace package.

A key interest of this paper is the investigation of the scalability of computing solutions as a cost-effective approach when processing huge data volumes with the new solution. This is reflected against current state-of-the-art data processing tasks as part of both mask and direct write applications.

Furthermore, we evaluated visualising and simulation possibilities of the ePlace package with respect to its application on latest layouts, or as required, in various applications.

The improved performance of the data preparation package including its adaptation to new e-beam lithography options, as, for instance, the incorporation of the cell projection capability, will be also described.

As an example the matching of the data path with the Vistec SB3055 will be discussed. Processing of DFEB data (including cell contents) and their conversion to real run-time data is reported. The advantages of the parallel use of standard shape beam und cell projection technologies are highlighted focussing on latest writing time yields achieved when applying the CP feature.

7488-80, Session 18

Impact of mask roughness on resist line-edge roughness

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Masks are typically specified based on mean and uniformity of critical dimensions over a range of feature types of nominal sizes. Thanks to growing values of the mask error enhancement factor (MEEF), CD specifications on the mask have been shrinking at a faster rate than the nominal wafer CD. Lately, another important lithographic metric has begun

to affect the way mask specifications are being approached: resist line-edge roughness (LER). As the importance of LER to wafer lithography grows, concern about the transfer of roughness from the mask to the wafer has also grown. Early experimental studies [1] showed that the frequency filtering affect of projection imaging significantly attenuated the impact of mask roughness. A theoretical study [2] defined the LER transfer function (LTF) from mask to wafer in the frequency domain. The relationship between the LTF and the MEEF has also been discussed [3]. However, the combination of shrinking specifications, increased resolving capability of lithographic imaging tools, and increased importance of wafer LER has meant that mask roughness can no longer be thought of as an insignificant contributor to wafer LER.

In this paper, a simplified version of the LTF will be derived, relating the frequency dependence of the LER transfer from mask to wafer to both the MEF and the imaging tool resolution. With this simplified LTF in hand, a rational method for specifying photomask roughness will be proposed.

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7488-81, Session 18

Full-chip mask process verification: sequential verification of e-beam, short-range etch, and long-range mask process effects

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Mask process compensation (MPC) is quickly gaining acceptance and being deployed at mask-shops at advanced technology nodes. Similar to OPC where design polygons are compensated to account for wafer lithography effects, MPC compensates the post-OPC data to account for systematic mask process effects including but not limited to e-beam, resist and etch effects. Again similar to OPC-verification, there is then a need to verify the MPC correction and find potential mask-process hot-spots. The mask process verification (MPV) scheme uses a sequential approach in performing the verification. Therefore three models are required: ultra-short range e-beam model, short-range etch model, and a long range model to account for effects such as fogging and etch macro-loading. The e-beam resist and short range etch models are calibrated using DI & FI contour measurements of mask test-patterns; the long range model is calibrated using CD-SEM FI measurements. The models are then used sequentially to simulate the mask process; first, a dense resist image is computed and a resist contour is extracted by applying a threshold. To obtain the etch contours, the etch model is applied to the simulated resist contours. Finally, if required, at each target point the simulation result is adjusted using the long-range model. The simulation result is then compared to target polygons and violations are recorded for review. In order to make reviewing process easier, violations are categorized based on target shape (e.g. line-end, corner, wide-line, narrow line etc); since target polygons are post-OPC data and can include many jogs, a ‘cleaned-up’ version of the target-polygon is used for classification. Furthermore, a pattern-matching algorithm is used to eliminate violations on repeated patterns and present the user with only unique violations. This combination of classification and pattern matching can significantly reduce the number of violations that need to be reviewed. Finally, the turn-around time (TAT) of verification tool is very important; verification is usually run in parallel with fracture, and the overall cycle time can potentially gate the release of data to e-beam writer. We present example TAT numbers and analyze the impact of various components of the flow on TAT.

7488-82, Session 18

Challenges for the 28-nm half node: is the optical shrink dead?

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A half-node process has been routinely used to deliver incremental improvements in process control and hardware availability in order to continue Moore’s Law. Traditionally, due to the imaging requirements, parameters such as numerical aperture and partial coherence were not set to their maximum resolution settings, thus leaving room in hardware and RET recipes to accommodate incremental imaging requirements. However, as hardware availability and computational lithography methods are stressed to the maximum of their capabilities to deliver the next technology nodes, it is worth asking the question if such optical shrinks continue to be viable moving forward. Already 28nm layouts scaled down from the original 32nm layouts are starting to show signs of configuration limitations dictated by the available imaging hardware.

In this paper we show that two-dimensional features determine the feasibility of migrating successfully to the next half-node even when one-dimensional metrics suggest that such migration should be possible. While it has been proposed that methodologies that are based on fabrics can guarantee composability and are intrinsically easier to migrate to smaller nodes, such approaches are mostly valid for processes in which the frequency distribution of the object to be imaged remains compatible with the hardware and RET of choice. This paper suggests that the distribution and extent of the layout fabric discontinuities present one of the major hurdles to composability. In other words, it is not only necessary to determine the best pitch and width of the underlying fabric, it becomes crucial to determine the distribution of the discontinuities present in the layout to build discrete devices.

Given that the feasibility of a half-node process is determined mostly by its ability to achieve denser patterns without non-trivial layout modifications, in this paper we show that it is important to start looking at the explicit layout configuration aspects that determine layout printability. We have selected a collection of typical 32nm layouts, as well as traditional layout configurations, and have determined their intrinsic failure conditions for a given process. For a given layout, different geometric parameters are varied in order to determine how incompatible certain layout variations are with respect to its patterning process.

The results indicate that for a well padded 32nm process it may still be possible to perform an optical 28nm shrink with only a minimum of manual intervention, assuming that certain layout configurations are removed or carefully monitored during production. However, the nature of the analysis suggest that moving forward to 22nm and in the absence of higher-resolution hardware (i.e. EUV) optical shrinks that require little or no layout modifications to the desired patterns to be printed may no longer be possible.

7488-83, Session 18

Reduced basis method for computational lithography

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The importance of numerical simulations for design, optimization and metrology of photomasks has grown rapidly over the last years due to the ongoing miniaturization of integrated curcuits.

A bottleneck for these many-query and real-time applications are long computational times for rigorous simulations of the near field in the photomask. Usually the same basic layout has to be simulated multiple times for different values of geometrical parameters, e.g. line width, absorber edge angle, etc.

The reduced basis method can be applied to this task. The solution process is decomposed into an expensive offline and a cheap online step. In the offline step the reduced basis is built self-adaptively by solving the underlying model rigorously several times. The full model is then projected onto the reduced basis. In the online step the assembled reduced system can be solved in the order of seconds basically independent on the size of the original problem. Error estimators assure the reliability of the reduced basis solutions.

Since the reduced basis method computes accurate approximations to the rigorous solutions the underlying solver for the offline construction of the reduced basis has to provide high quality solutions. We use the finite element solver JCMsuite for this task.

In our contribution we explain the basics of the reduced basis method and apply it to 2D and 3D simulation of photomasks. We demonstrate that highly accurate results can be computed in short times allowing e.g. for online simulations in metrology applications.

7488-84, Session 18

Efficient analysis of three-dimensional EUV mask-induced imaging artifacts using the waveguide decomposition method

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Several imaging artifacts induced by EUV masks such as feature orientation dependent placement errors and a global shift of the best focus are already well known to lithographers and can be easily compensated. However, other advanced aberration-like artifacts like feature orientation/ tone dependent focus shifts and tilt of the process window (similar to spherical aberration) are much more difficult to compensate. A previous study [1] employed a Zernike analysis of the mask-induced phase effects to understand the corresponding effects for line/space patterns. This paper extends this approach to investigate the observed effects for contact holes and more complex 3D layouts using the Waveguide decomposition method as an efficient electromagnetic field (EMF) solver.

The Waveguide decomposition method has been demonstrated [2] to be a fast and efficient rigorous EMF solver to compute the light diffraction from 3D masks. This method is adapted to Manhattan type mask layouts with feature edges along the x- and y-axis only. It decouples the diffraction effects along x and y and produces a two-dimensional diffraction spectrum by superposition of the separate x- and y-diffraction spectra. The phases of the diffraction orders correspond to a phase deformation of the farfield at the entrance pupil of the imaging system. A Zernike fit is applied to analyze the phase information and to understand the phase-induced aberration-like effects on the imaging. At first, a 32nm semi-dense contact array is investigated to verify the validity of the decomposition method. The lithographic imaging results and Zernike coefficients are computed using the Waveguide decomposition method and the benchmarked full Waveguide method, respectively. A comparison of the results is shown. Good agreement of the cross section at best focus is observed. The process windows show the same asymmetry and best focus shift. The simulation time of mask diffraction using the full Waveguide method is 1.5 hour on a standard PC, while the Waveguide decomposition method significantly speeds up the same simulation to 2 seconds with sufficient accuracy.

Subsequently, the mask induced phase effects on lithographic results versus different mask stack and illumination parameters are computed. The phase effects are then analyzed by fitting the phase with Zernike coefficients. The correlation between the behavior of Zernike coefficients and that of lithographic imaging results versus the selected parameters is demonstrated. The accordance suggests that the application of the Zernike analysis of the mask diffraction phase helps to understand the relevant effects and their impact on imaging artifacts. Major mask/illumination parameters with the most pronounced impact on the lithographic results are identified. Finally, the developed simulation approach is applied to more complex layouts like long contacts, different line end configurations, and elbow structures. From the analysis of these results in terms of overlapping process windows and other criteria, conclusions with respect to necessary OPC strategies and mask fabrication options will be drawn.

7488-85, Session 18

Isotropic treatment of EMF effects in advanced photomasks

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Classical methods for modeling electromagnetic scattering from the topography of lithographic reticles must place a high premium on fast computation, and toward that end they apply pre-stored perturbations (e.g. the so-called boundary layers) to feature edges in order to approximate the impact of finite-thickness mask films. Though approximate, these methods involve E&M calculations with vector fields, and so employ edge-field corrections that are different for edges oriented parallel to the vector field compared to the edge-fields for perpendicularly oriented edges; as a result these methods entail a requirement for two separate aerial image simulations with orthogonal polarizations to represent unpolarized illumination. This imposes a minimum 2X runtime penalty relative to baseline thin-mask (TMA) simulations, since the known method for combining the effect of both polarizations into one single set of imaging TCCs applies only to thin-mask calculations. More severe performance penalties are common in so-called sparse imaging methodologies when topographic effects are included, since the separated treatment of feature edges and the internal area of the features can increase the number of memory lookups required.

In this paper an isotropic field perturbation approach is evaluated, in which an isotropic edge field correction, common to all edge orientations, mimics the effect of the true parallel and perpendicular edge field perturbations when the mask is illuminated with unpolarized light, as well as in certain cases of polarized illumination. The isofield is not an ad hoc empirical correction but rather an accurate approximation in the limit of modest departures from scalar TMA. More specifically, we show that the isofield model accounts for vector imaging effects with full accuracy in the TMA terms, and in an approximate way in the electromagnetic edge-field terms that becomes accurate when the polarization dependence of the TMA terms is small. We will show with comparison to electromagnetic simulations across various structure types as well as comparison against wafer linewidth measurements that the accuracy loss relative to classic polarized EMF correction approach is within a small percentage on mask blanks where the electromagnetic edge field perturbation terms are small relative to the TMA term. Methodology to extend these models into the subwavelength diffraction regime will be discussed as well as practical techniques suggested by the isofield for mitigating the impact of topography.

7488-86, Session 19

Impact of carbon contamination on EUV masks

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Impact of carbon contamination on patterned extreme ultraviolet (EUV) masks is a significant issue due to lowered throughput and potential effects

on imaging performance. In this work, a series of carbon contamination experiments was performed intentionally on a patterned EUV mask with the EUV Microscope for Mask Imaging and Contamination Study (MiMICS) at Albany.

The mask was then inspected using a photoemission sensor installed on the SEMATECH Berkeley Microfield-Exposure tool (MET) to determine the reflectivity loss due to the carbon contamination. The density of carbon used for this work is 1.5 g/cm3, and the carbon thickness is approximately 25 nm for 8 hours exposure in MiMICS tool.

A reticle scanning electron microscope (SEM) was also used to inspect the mask and provide a top-down view measurement. A larger CD was observed after the mask was contaminated.

The image printing was carried out using the SEMATECH Berkeley MET, and the exposed wafers were then analyzed using a SEM and the SuMMIT software. To study the impact of carbon contamination on imaging performance, CD was measured at the best focus as a function of dose and exposure time.

In addition, the mask was analyzed using the SEMATECH Berkeley Actinic-Inspection tool (AIT) to record the intensity profile as aerial images from selected regions of the EUV mask. In order to determine the effect of carbon contamination on the absorbing features, we analyzed the process window and contrast curve, as well as the normalized image log-slope (NILS) and line width roughness (LWR) on the contaminated EUV mask based on the ThroughFocus software.

Another tool we used for the direct measurement is an atomic force microscope located in Albany. We measured the surface roughness of the clean multilayer and the contaminated region on the mask. A larger RMS roughness was measured from the carbon film deposited on the absorbing features. Cross-sectional and 3D surface plots were showed as well.

To understand the contamination topography, simulations were performed based on the calculated aerial images and resist parameters. We started the model by assuming the actual topography was deposited either directly or conformal, and more accurate control of the sidewall was applied to determine the ratio that was best matched to the experimental data. After this, a CD compensation was conducted to understand the differential thickness of carbon contamination on the sidewall due to the shadowing effect.

With the knowledge of the topography, simulations were used to predict the limitations of allowed carbon thickness with optical correction.

7488-87, Session 19

Critical issues and progress in EUV mask cleaning

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The readiness of the defect free mask supply is one of the top challenges for the implementation of extreme ultraviolet lithography (EUVL) to high volume manufacturing of semiconductor devices for the 22 nm node and beyond. Surface cleaning plays a crucial role not only in fabrication of defect free masks with high-yield in the mask shop but also in maintaining mask cleanliness during mask usage in the wafer fab. However, EUV mask cleaning faces unique challenges as a result of the use of new types of materials and reflective mask structure employed for the EUV mask, and the more frequent cleaning needed due to the lack of pelicle protection.

Systematic investigations have been carried out to determine the basic capability and fundamental issues of current and speculative techniques for EUV mask cleaning. We identified that the small particulates (the so-called adders) left on the surface from the wet cleaning process was our primary issue for extending the current cleaning process to meet EUV requirements [1]. To address this challenge, the effects of various cleaning processes and chemistries were assessed and we successfully achieved zero cleaning adders and 100% particle removal efficiency on EUV mask blanks. These data were obtained using the Lasertec M1350 which has 80nm standard SiO2 particle equivalent sensitivity. This year, we have started the evaluation of cleaning efficiency using the new inspection tool, the Lasertec M7360 which has 50nm standard SiO2 particle equivalent sensitivity on the EUV mask blanks. This high sensitivity inspection tool enabled us to recognize further challenges on the cleaning of much smaller particles, not visible with the M1350.

In this paper, we will present our latest results about cleaning efficiency of smaller particles using the M7360 and adder analysis and reduction. We will also discuss the cleaning of masks contaminated by particles from shipping and handling and during processing in an EUVL exposure tool.

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7488-90, Session 20

Investigation of buried EUV mask defect printability using actinic inspection and fast simulation

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The printability of buried EUV defects near absorber features will be studied using aerial images from the Actinic Inspection Tool (AIT) at Lawrence Berkeley National Laboratory (LBNL) [1] and the fast EUV simulation program RADICAL (Rapid Absorber Defect Simulation for Advanced Lithography) [2].

The AIT is a direct CCD actinic (EUV-wavelength) EUV mask inspection tool. It employs a bending magnet at the Advanced Light Source synchrotron at Lawrence Berkeley National Laboratory as its source and uses a Fresnel zone plate lens to project a high-magnification image with numerical aperture values that emulate current EUVL printing tools. Bitmap aerial images recorded by the AIT are suitable for direct comparison with bitmaps from simulation.

The RADICAL simulator used in this study is a full 3D EUV mask simulator designed to predict the aerial image from an EUV mask with a buried defect and absorber features. It can simulate a defective mask geometry three orders of magnitude faster than a finite difference time domain (FDTD) simulator. The mask used in this study is a programmed defect EUV mask in which 48nm high posts on a substrate are over-coated with a multilayer. The over-coating produced defects with about a 60 nm FWHM diameter and heights ranging up to 8nm [3].

A good match has been shown previously between these two tools [4]. This paper will build on that investigation by comparing the printability of defects with various sizes and locations through focus. All comparisons will be done for defects near 250nm lines on the mask with a nearly coherent illumination because that is what is available on the AIT. However, when EUV lithography is introduced, it will print features much smaller than 250nm mask scale. Unfortunately, current EUV mask making and imaging systems are not adequate for experimental investigation of defects near such small features. For these cases, RADICAL will be used alone to predict the effects of buried EUV mask defects imaged in a production EUV scanner. Defect printability will be investigated as a function of defect size, position and focus for the smaller absorber lines critical to 22nm and 16nm node imaging.

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7488-91, Session 20

Study of EUVL mask pattern defect inspection using 199-nm inspection tool with superresolution method

H. Shigemura, T. Amano, O. Suga, Y. Arisawa, Semiconductor Leading Edge Technologies, Inc. (Japan); R. Hirano, M. Hirono, N. Kikuiri, Advanced Mask Inspection Technology, Inc. (Japan); H. Hashimoto, K. Takahara, NuFlare Technology, Inc. (Japan)

Extreme ultraviolet lithography (EUVL) with 13.5-nm exposure wavelength is a promising candidate for the next-generation lithography because of its excellent resolution for 32-nm half pitch (hp) node device and beyond. With high resolution imaging from EUVL there also come some technical challenges. From the standpoint of EUVL it is necessary to fabricate defect-free mask by eliminating phase defects, pattern defects, and contaminations. As the feature sizes on the mask are shrinking, it is important to improve the pattern defect detection performance. EUVL mask pattern defect inspection is possible only by using reflective light. But with reflective light the image contrasts tend to diminish. There are two key issues with EUVL mask pattern defect inspection: one is the improvement of contrast since it is important to be able to see the base pattern of mask, and the other is the improvement of response signal from mask pattern defects. A higher signal to noise ratio will allow higher defect detectability. At Selete (Semiconductor Leading Edge Technologies, Inc.), a feasibility study was conducted for EUVL mask pattern defect inspection using a current DUV mask inspection tool with 199-nm wavelength illumination optics. Based on this work a new EUVL mask inspection tool with low system noise (optical and mechanical) is being built by NFT (NuFlare Technology, Inc.) and AMiT (Advanced Mask Inspection Technology, Inc.). In this tool, a switching mechanism between p-polarized illumination and circularly-polarized illumination has been incorporated.

By using this tool, we evaluated the image contrast and the capability of detecting defects on the EUVL masks. The test mask includes a defect sensitivity evaluation pattern and contrast evaluation pattern. The base patterns are 128nm half pitch, and 108nm half pitch, and 88nm half pitch line and space. And we used two types of test masks with different absorber materials. One is LR-TaBN which has 19% reflectivity at 199-nm wavelength. The other is LR-TaSi which has 5% reflectivity at 199-nm wavelength.

In this paper, we report our experiment results into the impact of EUVL mask absorber structure and inspection system optics on mask defect detection sensitivity.

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7488-99, Session 20

Modeling of EUV lithography

E. Hendrickx, G. F. Lorusso, IMEC (Belgium); E. Van Setten, ASML Netherlands B.V. (Netherlands); S. G. Hansen, ASML US, Inc. (United States); M. Lowisch, Carl Zeiss SMT AG (Germany); J. Jiang, W. Liu, L. Chen, Brion Technologies, Inc. (United States)

One of the main experimental setups for EUV lithography is the ASML EUV Alpha-Demo Tool (ADT), which allows for the first full-field EUV exposures at a wavelength of 13.5nm and a numerical aperture of 0.25. Good CD uniformity has been seen for a number of features, ranging from 40nm LS down to 30nm LS (<3nm 3sigma). The experimental data that are collected from wafers exposed on this tool, allow for accurate model calibration and an identification of possible lithographic errors seen across the exposure field. The current work focuses on how various factors, such as reticle CD, slit intensity uniformity, focus, shadowing and flare impact CD across the field and how these effects can be properly modeled.

As a first aspect of the modeling, we have calibrated a full resist model to process window data. The full resist model is then used in a combination with experimental measurements of reticle CD, slit intensity uniformity, focal plane behavior, and EUV thick mask effects to model the evolution of wafer CD across the exposure field. The modeled evolution of CD across the exposure field was found to be a good match to the experimentally seen evolution of CD across the field, and confirms that the 4 factors mentioned above are main contributions to the CD uniformity across the field.

As a second topic, we have measured the CD on wafer of vertical lines at different flare levels and model the evolution of wafer CD through flare, reticle CD, and pitch using Brion's Tachyon OPC engine. The modeling first requires the generation of a flare map using long-range kernels to model the EUV specific long-range flare. The accuracy of the flare map can be established independently from the CD measurements, by using the traditional disappearing pad test for flare determination (Kirk test). The flare map is then used as background intensity in the calibration of the traditional optical models with short-range kernels. For a structure set of 1000 features and over a flare range of 8%, an rms fit value of <1nm was obtained.

This modeling work enables a better understanding of the errors contributing to CD variation across the field for EUV technology. A first experimental assessment was made of the EUV specific parameters, such as flare and shadowing, and the impact of these parameters is compared versus the traditional lithographic error contributors, such as dose and focus.

7488-92, Session 21

Single-mask double-patterning lithography

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For reviewers: extended abstract with sample results available at http://www.ee.ucla.edu/~rani/BACUS09-Ghaida-Gupta.pdf

This paper introduces shift-trim double patterning lithography (ST-DPL), a cost-effective method for implementing double-patterning with a single photomask (especially at polysilicon layer). The mask is re-used for the second exposure by applying a translational mask-shift. Extra printed features are then removed using a non-critical trim exposure. ST-DPL can be implemented using LELE and LLE with little modifications to the processes as demonstrated in Figure 1. For the same mask to be used for both patterns at poly layer, few design rule restrictions are necessary: (1) some values of gate pitch are prohibited: gate pitch is either X (amount of shift) or greater or equal to X0, where X0 is the minimum gate pitch of single patterning; (2) in light of (1), minimum gate spacing is equal to contacted-gate spacing; (3) number of horizontal tracks available for poly routing depends on the repeatable shape of the critical mask (we limit it to at most three).

Some repeatable critical mask shapes are used. Each shape contains a vertical line to print gates and possibly horizontal lines to print field poly. Shapes with limited horizontal lines impose restrictions on poly routing and may prohibit the usage of landing pads for contacts. However, these shapes can achieve much better resolution since the mask is more regular.

The feasibility of ST-DPL is demonstrated on actual standard cells. ST-DPL steps applied to 4-input OAI standard-cell are illustrated. For this example, there are two layout options for allowing ST-DPL. In the first option, just 2% area overhead is introduced and one redundant diffusion-contact is removed from the circuit. In the second option, 9% area overhead is introduced and no changes are made to the layout topology. ST-DPL application for such cells is straightforward and introduces no area overhead.

ST-DPL's use of a single critical mask cuts mask-cost to nearly half of this cost in standard DPL.

Since in ST-DPL the same mask is used for both exposures, mask CD variation, which is the second most important contributor to the overall CD

variation, no longer affects the difference between the two distributions and the bimodal problem is alleviated.

Mask loading and unloading between both exposures is not necessary in ST-DPL. As a result, overlay from reticle metrology error, which is caused by reticle mounting/heating and particle contamination of the reticle alignment marks, is eliminated in ST-DPL. In addition, the time saved on loading/unloading procedure leads to enhancement of critical scanners throughput.

Negative LLE process that avoids removing the wafer from the exposure tool chuck between the two lithography-steps was shown to be viable in previous work. In case such process is used with ST-DPL, the second exposure can be performed after a blind shift without any alignment. This practically eliminates any overlay error between the two patterns and, also, saves alignment time.

7488-93, Session 21

Resolving contacts conflicts for double-patterning split

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Double patterning (DP) is one of the main enabling technologies for extending photolithography beyond 45 nm technology node [1]. The key idea of DP is to make dense features possible by splitting a design into two masks, typically marked by two colors in order to increase pitch size and improve depth of focus (DOF) for each exposure mask. Geometrical pitch split is the core of DP [2].

In this work we focus more specifically on the splitting of contact pattern layer. If the contact spacing is less than the minimum colouring space then the features must be assigned opposite colors corresponding to different exposures. However, for certain contact pattern configurations for which features are separated by less than the minimum coloring space different colors cannot be assigned and are flagged as color conflicts.

Some of these contact color conflicts can be resolved by model-based methods; while the un-resolvable ones known as native conflicts (NC) [3] such as triangle or square placement from contact spacing, can only be resolved by changing the design. With the help of design for manufacturing (DFM), the NC can be eliminated in order to obtain 100% of split success on tested layouts. However the state of the art DFM redesign solution is highly expensive in terms of resources and time.

In this paper we propose a method for contact color conflicts treatment that helps to improve DP-NC designs in an optimal way. It is based on the latest RET in optical lithography such as source and mask optimization (SMO) [4] and inverse lithography technology (ILT) [5].

Results will be presented which demonstrate the ability of this method to solve the most critical split contact conflicts in DP for advanced node.

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7488-94, Session 21

Geometric distribution of full-chip DPT coloring

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Decomposition of an input pattern in preparation for a double patterning process is an inherently global problem in which the influence of a local decomposition decision can be felt across an entire pattern. In spite of this, a large portion of the work can be massively distributed. We will discuss the advantages of geometric distribution for polygon operations with limited range of influence. Further, we have found that even the naturally global “coloring” step can, in large part, be handled in a geometrically local manner. In some practical cases, up to 85% of the work can be distributed geometrically. We will describe the methods for partitioning the problem into local pieces and will present scaling data up to 100s of CPUs. Some of these methods of geometric distribution result in superior output symmetry and hierarchic preservation, reducing output file size. Data on these topics will also be presented.

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Thursday 17 September . . . . . .8:00 am to 10:30 am

Exhibition Hours
Monterey Conference Center – Serra Grand Ballroom

Tuesday 15 September . . 10:00 am to 4:30 pm; 6:30 pm to 8:00 pm
Wednesday 16 September . . . . . 10:00 am to 4:00 pm

Exhibition admission is included in your registration fees.

SPIE Membership
SPIE Members receive 15% off conference and course registration fees.

Student Members
Save 50% on Course Registration. Proof of full-time student status is required. Student ID number or proof of student status required with your registration. Offer applies to undergraduate/graduate students who are enrolled full time and have not yet received their Ph.D.

Press Representatives
Media/Press - For credentialed press and media representatives, please email contact information, title and organization to media@spie.org.

Special Events

Exhibition Poster Reception
Monterey Conference Center, Serra Grand Ballroom

Tuesday 15 September. . . . . 6:30 to 8:00 pm

Beer/Wine Sponsored by SYNOPSYS

Symposium attendees and guests are invited to attend an Exhibition/Poster Reception on Tuesday evening in the Serra Grand Ballroom. The reception provides an opportunity for attendees to meet colleagues, network, and view poster papers. Refreshments will be served. Attendees are requested to wear their conference registration badges.

Poster Viewing
Tuesday 15 September . . . . . 6:30 to 8:00 pm
Wednesday 16 September . . . . . 10:00 am to 3:00 pm

Poster authors may set up their poster papers between 10:00 am and 4:00 pm on Tuesday and will leave them up until Wednesday afternoon. Authors will be present during the Poster Reception 6:30 to 8:00 pm Tuesday to answer questions and provide in-depth discussion regarding their papers. Any papers not removed by Wednesday at 3:00 pm will be considered unwanted and will be discarded. SPIE assumes no responsibility for papers left up after Wednesday at 3:00 pm.

Photomask Reception
Monterey Marriott, San Carlos Ballroom

Wednesday 16 September . . . . . 6:30 to 8:30 pm

Sponsored by
KLA-Tencor Accelerating Yield · SYNOPSYS · TAIWAN MASK CORP

Beer/Wine Sponsored by HOYA

Don't miss it! Make plans to join your colleagues and friends at the annual Photomask Reception. This year's event focuses on good food, beverages, and plenty of time to socialize or talk business with fellow conference attendees. Awards and other presentations will be included in the evening. Admission is included with your paid registration. Guest tickets may be purchased with your pre-registration or onsite (we highly recommend purchasing in advance to assure your reservation).

Food & Beverage Services

Breakfast Breads
Monterey Conference Center, Steinbeck Lobby

Complimentary breakfast breads will be served from 7:30 to 8:30 am, Tuesday through Thursday, for symposium attendees in the Steinbeck Lobby.

Coffee Breaks
Complimentary coffee will be served at the following times and locations. Please check the individual technical conference listings for exact times and locations.

Monterey Conference Center, Serra Grand Ballroom
Tuesday 15 September . . . . . .10:10 to 10:40 am; 3:40 to 4:10 pm
Wednesday 16 September . . . . .10:00 to 10:30 am; 3:00 to 3:30 pm

Monterey Conference Center, Steinbeck Lobby
Thursday 17 September . . . . . .10:00 to 10:30 am; 3:00 to 3:30 pm

SPIE-Hosted Lunches
Monterey Marriott, San Carlos Ballroom

Hosted lunches will be served at the following times:

Tuesday through Thursday . . . . . .Noon to 1:00 pm

Please check the individual technical conference listings for exact times.

Complimentary tickets for these lunches are included for full conference registrants. Exhibitors and students may purchase tickets in the SPIE Registration Desk in the Portola Lobby.

Desserts
Dessert will be served during coffee breaks on Tuesday and Wednesday in the Exhibition Hall. A complimentary ticket for dessert will be included in attendee and exhibitor registration packets.

Attendee Services

Cashier

SPIE cashier can assist with registration payments, adding a course, receipts, and badge corrections.

Internet Services

Internet Pavilion

Monterey Conference Center, Steinbeck Lobby

Sponsored by JEOL

Tuesday and Wednesday . . . . . 7:30 am to 6:00 pm

Thursday . . . . . 8:00 to 10:30 am

SPIE will have a complimentary Internet Pavilion Tuesday through Thursday, 15-17 September, where attendees can use provided workstations or hook up their laptop to an Ethernet connection to access the Internet.

Wireless Internet Service

Monterey Conference Center, Exhibition Hall

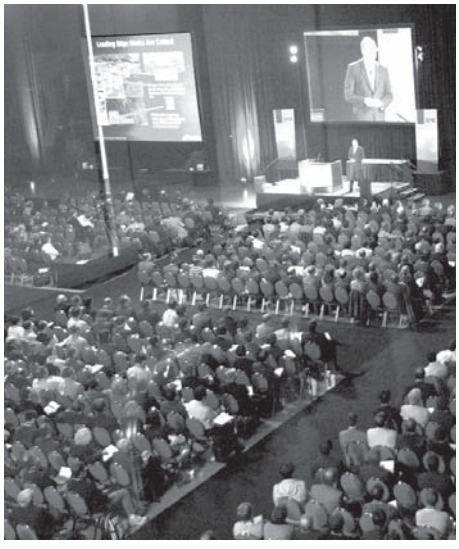
Sponsored by ZEISS

Open during Exhibition Hours

Complimentary wireless access is available in the Exhibition Hall, Serra Ballroom. Wi-Fi access instructions are available in the Exhibition Hall and at the SPIE Registration Desk. SPIE recommends that you properly secure your computer before accessing the public wireless network. Failure to do so may allow unauthorized access to your laptop as well as potentially introduce viruses to your computer and/or presentation.

Hotel Service Internet

Each hotel room is equipped with data ports for hook-up to high speed Internet service for $12.95 for 24 hours.



Business Services

Business Center

At the Monterey Marriott, attendees may use their hotel room key to access the onsite Business Center which offers use of a free online computer. Copy and fax machines are available at the front desk. Copies are free for the first 20 copies, 10 cents per page after. The fax machine is $1.00 per page for domestic usage and $3.00 per page for international usage.

Each hotel room is equipped with data ports for hook-up to high-speed Internet service for $12.95 for 24 hours.

Offsite Business Center

Fedex Kinkos is located at 799 Lighthouse Ave., Ste. A, Monterey, California, 93940, Phone: 800 463 3339. It is 1.3 miles from the Monterey Marriott (approx. 5 minutes driving time). Go north on Calle Principal, left onto Del Monte Ave., right onto Pacific St., right onto ramp to merge onto Lighthouse Ave.

Message Center

The SPIE Message Center telephone number is 831 646 5312. Ask for SPIE/BACUS Registration Desk. Messages will be taken during registration hours Monday through Thursday, 14-17 September. Please check at the SPIE Registration Desk if you expect a message.

Speaker Presentation Preview Room

Monterey Conference Center, Sloat Room

Open during Registration Hours

Each conference room will have a computer workstation, LCD projector, screen, lapel microphone, and laser pointer. All presenters are encouraged to visit the Speaker Presentation Preview Room to confirm display compatibility of their presentation, whether using a memory device or laptop, with the audiovisual equipment supplied in the conference rooms.

Speakers, who have requested equipment prior to the request deadline, are asked to report to the SPIE Registration Desk to confirm their requested equipment.

Course Materials Desk

Located at the SPIE Registration Desk. Open during Registration hours.

If you have registered to attend a course, you will obtain your badge, course notes, and the class location during the Registration process.

Marketplace and Souvenirs

The SPIE Marketplace is your source for the latest SPIE Press books, Proceedings, and Educational and Professional Development materials. To purchase any Marketplace materials or become an SPIE Member, please ask at the Photomask Registration Desk.

Child Care Services

The Monterey Marriott suggests the following child care service companies in Monterey:

Parents Time Out, Phone: 831 375 9269

Corporate Kids Events, Inc & VIP Babysitting Services, Phone: 800 838 2787, www.corporatekidsevents.com, Email garen@corporatekidsevents.com

SPIE does not imply an endorsement or recommendation of this service. It is provided on an “information only” basis for your further analysis and decision. Other services may be available.

Policies

Refund Policy

There is a $40 service charge for processing refunds. Requests for registration refunds must be received no later 3 September 2009. All registration fees will be forfeited after this date.

Membership dues are not refundable. SPIE Digital Library subscriptions are not refundable.

Audio, Video, Digital Recording Policy

Meeting Rooms and Poster Sessions

For copyright reasons, recordings of any kind are strictly prohibited without prior written consent of the presenter in any conference session, course or of posters presented. Each presenter being taped must file a signed written consent form. Individuals not complying with this policy will be asked to leave a given session and asked to surrender their film or recording media. Consent forms are available at the SPIE Registration Desk.

Exhibition Hall

For security and courtesy reasons, photographing or videotaping individual booths and displays in the Exhibit Hall is allowed ONLY with explicit permission from onsite company representatives. Individuals not complying with this policy will be asked to surrender their film and to leave the exhibit hall.

Laser Pointer Safety Information

SPIE supplies tested and safety approved laser pointers for all conference meeting rooms, and for course rooms if instructors request one. For safety reasons, SPIE requests that presenters use our provided laser pointers available in each meeting room.

Underage Persons on Exhibition Floor

For safety and insurance reasons, no persons under the age of 16 will be allowed in the exhibition area during move-in and move-out. During open exhibition hours, only children over the age of 12 accompanied by an adult will be allowed in the exhibition area.

Unauthorized Solicitation

Any manufacturer or supplier who is not an exhibitor and is observed to be soliciting business in the aisles, or in another company's booth, will be asked to leave immediately. Unauthorized solicitation in the Exhibit Hall is prohibited.

Unsecured Items

Personal belongings such as briefcases, backpacks, coats, book bags, etc., should not be left unattended in meeting rooms or public areas. These items will be subject to removal by security upon discovery.

Parking

Parking at the Monterey Marriott Hotel

Valet only is available at $19 overnight (subject to change). No self parking available. Short term parking, 4 hrs or less, is $11.

Parking at the Monterey Conference Center

Public parking is available in the East Garage, two blocks down from the hotel. Drive down Franklin Street (one-way), turn left on Washington Street, and turn left into the parking garage. You can also enter the parking garage turning left on Del Monte Street or left on Tyler Street (both one way streets). To park, pay the flat rate per day of $7, payable in exact change as there is no attendant on duty to make change. MasterCard or Visa is also accepted. No in/out privileges. City Parking Lots (831-646-3953) http://www.monterey.org/parking/

Parking is also available in the West Garage across from the East Garage, which has an attendant on duty, open 24 hours with in/out privileges. Drive down Washington Street; go left on Del Monte Street and left on Tyler. The lower level has a time limit maximum of 90 minutes and parking in this lower level is free. The upper level charges $.50 per 20 minutes and $10 max per day, with the first hour free. They accept cash or American Express, MasterCard or Visa, and the attendant will make change.

Additional Conference Center Parking at the Portola Plaza Hotel Lot

Conference Center guests can park at the Portola Plaza Hotel for $2 for the 1st hour, $1 each additional half hour, maximum $18, 24 hrs. payable with cash or credit cards (no checks). There is an attendant onsite. Portola Plaza Hotel phone number is 831 649 4511. The hotel is directly across from the Marriott, and both are connected to the Monterey Conference Center by a footbridge.

All parking rates are subject to change without notice.

Car Rental

Hertz Car Rental has been selected as the official car rental agency for this Symposium. To reserve a car, identify yourself as a Photomask Conference attendee using the Hertz Meeting Code CV# 029B0012.

* In the United States call +1 800 654 2240
* Book online www.hertz.com

About Monterey

Monterey Marriott Hotel
350 Calle Principal
Monterey, CA 93940

The Monterey Marriott Hotel is located with in easy walking distance of the Monterey Bay Aquarium, Fisherman's Wharf, Cannery Row and fabulous shopping. The hotel features an outdoor pool, day spa, fitness center, and nearby golf, tennis and beaches. Your hotel concierge will be happy to arrange everything from car rentals to a golf outing.

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Volume	Title	Price
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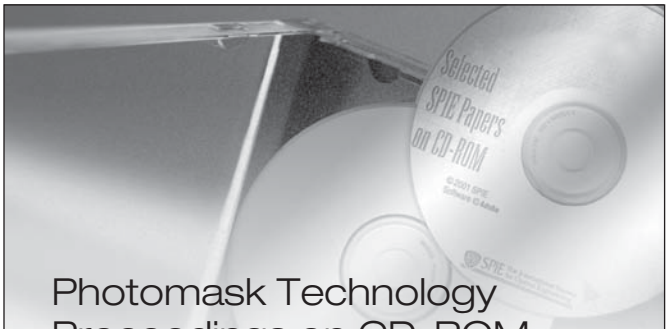

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