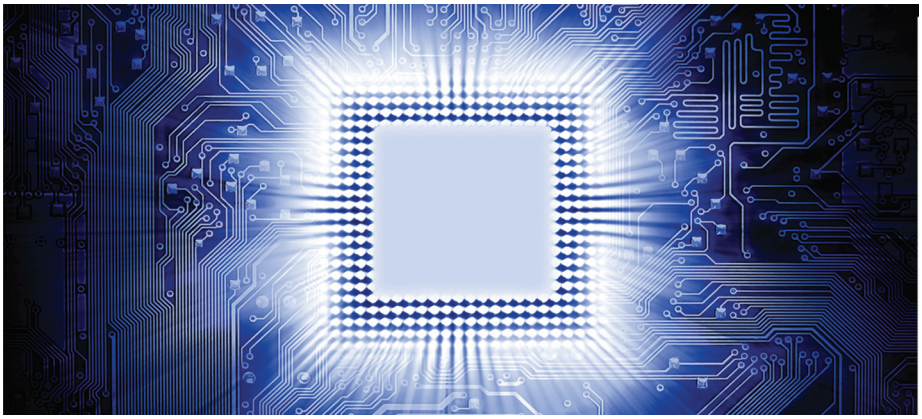
Abstract Summaries

SPIE Lithography Asia Taiwan

Conference and Exhibition: 18–19 November 2009
Sheraton Taipei Hotel
Taipei, Taiwan



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Conference 7520: SPIE Lithography Asia - Taiwan

Wednesday-Thursday 18-19 November 2009 • Part of Proceedings of SPIE Vol. 7520 Lithography Asia 2009

7520-01, Session 1: Plenary Session

An outlook on future silicon industry

K. Kim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

Since the invention of integrated circuit(IC), the semiconductor industry has grown at an unprecedented pace. This growth has been fueled by an exploding customer demand for products utilizing semiconductor chips. In the past the main semiconductor growth engine was the PC market, since the late 1990s the mobile era has been another growth engine with a vast assortment of now familiar products, such as mobile phones, digital cameras and MP3 music players and so on.

In spite of recent years' global economic recession and the nature of ebb and tide of semiconductor market, especially memory market, it is generally agreed that the semiconductor industry will continue to expand due to continued steady growth of the mobile, digital consumer and entertainment markets.

The advances in silicon technology have been the backbone of tremendous previous growth. And, in fact, it has repeatedly been shown that the number of transistors integrated into silicon chips has indeed doubled every 18 months, which is called Moore's law. Enormous computing power and huge memory capacity which Moore's law brings in actually make modern Internet world possible. As silicon technology enters into nano scale dimension, further improved capabilities of integrated circuits can bring great opportunities to silicon industry by merging with the adjacent related technologies such as health-bio, nano, and robotics and etc. These technologies will be the new growth engines for silicon industry, at the same time silicon technology will also provide many benefits to these industries.

Despite these bright prospects, there is growing concerns about whether silicon technology can continue to keep pace with demand when the silicon technology enters into the "deep nano-scale" dimension. This is because there would be ultimate limits to transistor scaling, and narrowing margins in manufacturing due to ever-increasing fabrication costs tied to technical complexities. Though most experts believe that silicon technology will maintain its leadership beyond 10 nm, however it is certainly true that a number of fundamental and application-specific obstacles will not readily permit to further shrinkage. A common example is the inevitable occurrence of variations due to rough line edges and surfaces when pattern sizes approach atomic scales.

It is therefore the primary aim of this paper to investigate various possible paths to overcome these obstacles and ultimately, to continue to grow silicon industry far beyond nanometer regime.

7520-02, Session 1: Plenary Session

3D integration opportunities, issues, and solutions: a designer's perspective

C. Wu, Industrial Technology Research Institute (Taiwan)

As the development cost of a typical system-on-chip (SOC) using state-of-the-art technology soars, more and more people turn to three-dimensional (3D) integration for possible alternatives that provide better or equal performance with lower cost. Stacking dies using the Through-Silicon-Via (TSV) technology has been considered one of the most promising solutions to extending the life of Moore's law in semiconductor industry, but of course there are problems to be solved before the infrastructure can be set up to support the industry for manufacturing TSV-based 3D integrated devices. In this talk we will discuss the opportunities, design and manufacturing issues, and possible solutions for 3D integrated devices, from a designer's perspective.

7520-03, Session 1: Plenary Session

Rivalry and complementary of photon and electron beams

B. J. Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

Not long after the photon beam was used to delineate circuit patterns in resist, e-beam was called for duty due to the concern of photons running out of resolution. The e-beam counterpart of proximity printing, projection printing, and direct writing quickly took shape as early as 1975. The race was on. Optical projection printing, taking advantage of a high degree of parallelism, excelled in throughput and economy for wafer patterning. However, electrons can be quickly deflected to directly write patterns. It took over mask writing. Rivalry turned into complementary for decades.

Recently e-beam has a new opportunity to beat photon beam at its own game of parallelism and eliminate the problems associated with masks altogether. This presentation compares optical and e-beam imaging technically, economically, and historically, pointing to the rewards and challenges for each technology to succeed.

7520-04, Session 1: Plenary Session

Mask technology and timing for IC and LCD applications

C. J. Progler, Photronics, Inc. (United States)

An understanding of the complex interaction between mask making processes and component fabrication has taken center stage as mask suppliers confront a wide array of lithography integration scenarios, cost containment initiatives and cycle time demands. This talk will highlight progress and challenges in mask manufacturing for high end IC and LCD applications from current state of the art to future industry needs. We will discuss both common aspects and application specific differences for mask technology used in IC and TFT LCD fabrication with emphasis on how the mask ties into the final application. Finally, consideration for the evolving business model of commercial mask making will be discussed including potential alternatives to the status quo.

7520-05, Session 2

EUV litho status at SELETE

O. Suga, Semiconductor Leading Edge Technologies, Inc. (Japan)

No abstract available

7520-06, Session 2

High power LPP EUV source system development status

B. S. Lin, Cymer Southeast Asia, Ltd. (Taiwan); N. R. Farrar, D. Brandt, Cymer Inc. (United States)

Extreme ultraviolet (EUV) technology has been recognized as the major lithography technology for 22 nm HP and beyond to fulfill Moore's Law: circuit dimensions shrink 70% every 2~3 years in order to achieve cost down and obtain greater functionality per unit area. EUV source power is one of the key factors to determine the degree of cost-down efficiency compared to the other lithography technologies, like double patterning. Only when EUV power can achieve to a certain level, the cost of EUV lithography under high volume manufacturing (HVM) can become much more competitive than that of double patterning techniques. In this paper, the performance of the first production Cymer high power laser produced plasma (LPP) EUV source

integrated with a 5 sr multi-layer mirror (MLM) collector and fully integrated debris mitigation will be shown. The latest results on power generation, stable and efficient collection, and clean transmission of EUV light through the intermediate focus will be presented. The lifetime of the MLM collector is a critical parameter in the development of extreme ultraviolet LPP lithography sources. Debris mitigation techniques are used to inhibit reflectivity degradation from deposition of target material, sputtering of the multilayer coating, and implantation of incident particles, which can reduce the efficiency of the MLM collector during exposure. The far field images of MLM collector are recorded by intermediate focus metrology with CCD camera to determine the reflectivity status of the MLM collector during exposure. The results of these debris mitigation techniques are compared through multiple-hour EUV exposure. Intermediate focus protection is essential to keep contamination from passing through to the illumination optics. Testing shows cleanliness at the source-scanner interface acceptable to the limit of detection.

7520-07, Session 2

EUVL: towards implementation in production

H. Meiling, C. Wagner, ASML Netherlands B.V. (Netherlands); N. Harned, ASML Wilton (United States); A. C. Chen, P. K. Cheang, ASML Taiwan Ltd. (Taiwan)

Cost, cost, cost: that is what it is - ultimately - all about. Single exposure lithography is the most cost effective means of achieving critical level exposures, and extreme ultraviolet lithography (EUVL) is the only technology that will enable this for </= 27nm production. ASML is actively engaged in the development of a multi-generation production EUVL system platform that builds on TWINSCAN™ technology and the designs and experience gained from the Alpha Demo Tools (ADTs). The ADTs are full field step-and-scan exposure systems for EUVL and are being used at two research centers for EUVL process development by more than 10 of the major semiconductor chip makers, along with all major suppliers of masks and resist. Recently, succesfull implementation of EUVL for the contact hole and metal1 layer was demonstrated in the world's smallest (0.099 um2) electrically functional 22nm CMOS SRAM device [1].

We will highlight the key features of the system description for the production platform, including the manufacturing status of projection lens, illuminator optics, and source. Experimental results from ADT showing the progress in imaging and resist work will be covered as well - a snapshot of imaging data can be seen in the figure below.

We will share our vision on the extendability of EUVL by discussing our system implementation roadmap. We will explain our approach for multiple tool generations on a single platform, highlighting the ways to support the technology nodes from 27nm half-pitch with a 0.25NA lens going down to below 16nm with a 0.32NA lens.

[1] IMEC press release, 28 April 2009 (http://www2.imec.be/imec_com/imec-22nm-sram-cells-with-euv.php?year=2009&month=04).

7520-08, Session 2

Imaging performance of production-worthy multiple-E-beam maskless lithography

T. Fang, S. Lin, J. Chen, S. Chang, F. Krecinic, B. J. Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

E-beam maskless lithography is a potential solution for 32nm half-pitch (HP) node and beyond. The major concern to implement it for mass production is whether its throughput can be enhanced to a production-worthy level. Without violating the law of physics using unrealistic e-beam current, parallelisms in the writing beams and data path are the only possible solutions to achieve such high productivity. It has been proposed to achieve throughput greater than 10 wafers per hour (WPH) from a single column with >10,000 e beams writing in parallel, or even greater than 100 WPH by further clustering multiple columns within a certain tool footprint. The MAPPER concept contains an CMOS-MEMS blanker array supported by a high-speed optical data-path architecture to simultaneously control more than ten thousand e beams writing in parallel, switching on and off independently.

The MAPPER Pre-Alpha Tool with a 110-beam 5-keV column and a 300-mm wafer stage has been built and is ready for imaging test. In this paper, the resist imaging results of 110-beam parallel raster-scan writing for 32-nm logic circuit layout with e-beam proximity correction on 300-mm wafer is shown. The challenges of implementing multiple e-beam direct writing in mass production environment, including illumination, focusing, and CD uniformity, are discussed. Demonstration is planned on the feasibility of correcting the beam-to-beam CD deviation by applying various writing schemes to each individual beam according to the actually measured beam current and beam size.

7520-09, Session 2

Advances in maskless and mask-based optical lithography on plastic flexible substrates

I. Barbu, M. G. Ivan, P. Giesen, TNO Science and Industry (Netherlands); M. J. E. Van de Moosdijk, ASML Netherlands B.V. (Netherlands); E. R. Meinders, TNO Science and Industry (Netherlands)

Plastic electronics is an emerging industry with huge potential growth in the future, which will likely have a great impact on our everyday life. New technologies spanning potential application fields are currently under development. These include OLED large-area displays, urban commercial signage, and flexible e-paper. Successful development of any of these products at a reasonable cost depends on process parameters, materials, and equipment. Optical lithography is the most promising candidate for patterning thin film transistors on plastic substrates. Manufacturing transistors on flexible substrates is not straightforward and involves a number of challenges, like foil handling, lithography process and control of in-plane foil deformation. The temporary fixation of a flexible substrate on a rigid carrier appeared to provide excellent surface flatness and dimensional stability. In previous work, we have reported the patterning of submicron transistors with overlay accuracies better than 0.3 micron with this technology [1]. Active control of in-plane deformations becomes essential in case of pattern transfer on large-area flexible substrates. In this paper, we focus on the development of a robust process for large-area patterning of metal circuits on plastic foils with maskless and mask-based optical lithography.

A systematic investigation of the substrate influence on the final resist profiles is presented for three DNQ-based, positive-tone photoresists. Because different applications may require different flexible substrates, two plastic foils were investigated: poly(ethylenenaphthalate) (PEN) and poly(ethyleneterephthalate) (PET). They are characterized by different glass transition temperatures and different thermo-mechanical properties which impact their suitability for the targeted end application. To ensure the dimensional stability of the foils during processing, the flexible substrates were temporarily laminated onto rigid substrates (6-inch Si wafers) by an in-house developed method [2, 3]. Influence of foil roughness on the quality of resist profiles and metal patterns was investigated, and substrates with and without planarization layers were employed. The results obtained with flexible substrates were benchmarked against results obtained with silicon and gold-coated silicon substrates.

We compare three different imaging techniques: one-to-one proximity printing (Karl Suss MA8 mask aligner), reduction projection lithography (ASML PAS 5500/100D stepper) and optical maskless lithography (Holst Centre research tool). Optical maskless lithography is a relatively new optical imaging technique, in which the reticle-related constraints are overcome by the usage of pixel grid imaging, where the projected image is formed by an array of beamlets which are selectively turned on/off by a computer controlled spatial light modulator [4]. The resist profiles and metal lines were characterized with optical microscopy, scanning electron microscopy, and atomic force microscopy.

[1] M. Péter, F. Furthner, T.C.T. Geuns, B. van der Putten, W. de Laat, G.H. Gelinck, E.R. Meinders, Advances in lithographic patterning of micron-sized features on flexible substrates, Proceedings OSC 2008.

[2] Maria Peter, Francois Furthner, Jochem Deen, Wim J.M. de Laat, Erwin M. Meinders, "Lithographic patterning of metals on flexible plastic foils", Thin Solid Films, 517, 3081-3086, (2009).

[3] M. Péter, W. de Laat, P. T. M. Giesen, C.-Q. Gui, E. R. Meinders, Patterning Submicron Features on Flexible Plastic Substrates by Optical Lithography, Mater. Res. Soc. Symp. 2008, Proc. 1030, 1030-G04-04.

[4] Pease, F. R., "Maskless Lithography", Microelectronic Engineering, 78-79, 381, 2005.

7520-11, Session 3

Source-mask selection using computational lithography: further investigation incorporating rigorous resist models

M. D. Smith, S. H. Kapasi, S. A. Robertson, J. J. Biafore, KLA-Tencor Texas (United States)

Recent publications have emphasized the criticality of computational lithography in source-mask selection for 32 and 22 nm technology nodes. Lithographers often select the illuminator geometries based on analyzing aerial images for a limited set of structures using computational lithography tools. Last year, Biafore, et al demonstrated the divergence between aerial image models and resist models in computational lithography. In a follow-up study , it was illustrated that optimal illuminator is different when selected based on resist model in contrast to aerial image model. In the study, optimal source shapes were evaluated for 1D logic patterns using aerial image model and two distinct commercial resist models. Physics based lumped parameter resist model (LPM) was used. Accurately calibrated full physical models are portable across imaging conditions compared to the lumped models. This study will be an extension of previous work. Full physical resist models (FPM) with calibrated resist parameters will be used in selecting optimum illumination geometries for 1D logic and memory patterns. Additionally, optimal source geometries for critical 2D patterns (Line-ends) will also be evaluated using different models. Several imaging parameters - like Numerical Aperture (NA), source geometries (Annular, Quadrupole, etc.), illumination configurations for different sizes and pitches will be explored in the study. Our goal is to compare and analyze the optimal source-shapes across various imaging conditions. In the end, the optimal source-mask solution for given set of designs based on all the models will be recommended.

7520-12, Session 3

Feasibility studies of source and mask optimization

T. Nakashima, T. Matsuyama, Nikon Corp. (Japan)

Resolution of optical lithography is defined by exposure light wavelength, projection lens NA and k1 factor. Exposure tools are, historically, developed to reduce exposure light wavelength, to increase projection lens NA, and to reduce k1 factor. Reducing exposure light wavelength is achieved by changing the light source, i.e., i-line of Hg lamp (365 nm) to KrF excimer laser (248 nm) and ArF excimer laser (193 nm). The next source wavelength is considered to be EUV (13 nm). Exposure projection lens NA was gradually increased through 0.78, 0.85, 0.92 by continuous development of optical design and manufacturing technologies. The limitation of projection lens NA was considered to be 1.0, but immersion lithography tools extend the limitation to 1.43 (refractive index of water at 193 nm).

Reducing k1 factor also improves the fine resolution of optical lithography. Off axis illumination (OAI), such as annular, quadrupole, and dipole illumination, and mask enhancement technologies, such as attenuating phase shift masks (PSM) and alternating PSM have been introduced to reduce the k1 factor. The physical limit of the k1 factor is 0.25, but litho-etch-litho-etch double patterning or using non-linear reaction material enables k1 < 0.25 lithography.

In such low-k1 lithography, the fidelity of other patterns not at the resolution limit, such as other linewidths, other pitches, line-ends, corners, and T-shaped patterns may limit the lithography process. For example, the most suitable illumination shape to resolve fine pitch lines and spaces is a leaf-shape dipole, but this illumination is problematic for 2x pitch patterns, perpendicular patterns, and line-ends. In order to expose both resolution limit line and space patterns and the other patterns simultaneously, complex illumination shape and mask design are required. The source and mask optimization (SMO) technique will resolve such complex issues.

In general, SMO uses the process window area as the merit function, and searches a combination of illumination shape and mask patterns to maximize focus margin and dose latitude. But in the actual lithography process, we need to consider other error factors, such as mask writing error, projection lens aberration, illumination optics influence, customized illumination optics manufacturing error, and reticle and wafer stage vibration error.

We have evaluated a prototype SMO software, optimizing illumination shape and mask for extracted patterns from GDS files. This software can analyze several mask pattern CDs and target fidelity. In this paper, we will report the sensitivity of the SMO solution relative to potential error factors, and try to find more robust solutions. Furthermore, we will discuss the manufacturing issues of customized illumination optics for the SMO solution, for example, concentrated illumination in a very small area of the pupil, manufacturability of very complex illumination shapes, and durability of optical elements.

7520-13, Session 3

Source-mask optimization: impact of source and mask complexity on lithography performance

S. D. Hsu, Brion Technologies, Inc. (United States)

The co-optimization of the source and mask patterns is vital to future advanced ArF technology node development. In this work, we systematically study the impact of source and mask complexity on designs with different k1 and pitch distribution. Using the source mask optimization co-optimization method, a design pattern with a range of pitch distribution and a SRAM pattern are investigated. k1 for these designs is varied from 0.5 to 0.28. For these two cases, we study the impact of the complexity of the source and mask on the co-optimization result. On the source side we vary the source from traditional DOE advince freeform DOE that subjected to ASML scanner specific constraints. On the mask side, we control the mask complexity by enforcing the assist feature geometry and varying the mask manufacture rule check (MRC). We report the process window comparison with different source and mask complexity through a range of k1 value.

7520-32, Session 3

Regularization of inverse photomask synthesis to enhance manufacturability

N. Jia, E. Y. Lam, The Univ. of Hong Kong (Hong Kong, China); A. K. K. Wong, Consultant (United States)

Photomask design can be formulated as an inverse imaging problem. Although such inverse lithography is considered superior to other model-based OPC approaches in delivering better on-wafer pattern fidelity, the lack of a good mathematical description of constraints, particularly robustness against process variation and mask manufacturability, hinders its adoption in industrial use.

In this paper, we focus on mask manufacturability. Inverse lithography has the ability to generate "unintuitive" mask patterns, which are non-obvious and difficult to predict. However, they often contain curvilinear image contours and irregular shapes, which add heavy computation load on segmentation and data preparation, and cost more mask-writing time. To deal with this problem, we apply manufacturability constraints on the mask design to mandate more regular mask shapes without serious pattern fidelity loss.

We formulate the mask design as a pixel-based inverse image synthesis problem. An optimization framework, using gradient descent, iteratively modifies the mask image to generate on-wafer pattern close to the target pattern. In previous work, total variation (TV) has been used for regularization and it is shown to regulate the mask shape effectively and can minimize the isolated pixels and far-away assist features. However, TV is not very effective in regulating the mask shape to be rectangular, but allows some diagonal lines to exist. Here, we propose modifications to control mask shapes bet-

ter. In addition to applying TV regularizations on the whole mask image, we also use it on the edges of the mask image. The rationale is that as we force the curves of edges to be more vertical or horizontal (which give small TV values), the shape of the mask becomes more rectilinear.

The algorithm proceeds as follows. First, two edge images are calculated by the first-order difference along x- and y-axis respectively. Then, along the orthogonal directions, a 1-D TV of each edge image is calculated.

The edge constraint used in the optimization process is the summation of the TV values from these two edge images. Simulation shows the TV regularization on both edge and image could shape the mask pattern to be more rectangular. We thus can argue that this is a useful constraint in applying inverse lithography to enhance mask manufacturability.

7520-14, Session 4

The LER/LWR metrology challenge for advance process control through 3D-AFM and CD-SEM

J. Foucher, P. Faurie, CEA-LETI (France)

The continuous shrinkage in dimensions of microelectronic devices as reaches such level, with typical gate length in advance R&D of less than 20nm combine with the introduction of new architecture (FinFET, Double gate...) and new materials (porous interconnect material, 193 immersion resist, metal gate material, high k materials...), that new process parameters have to be well understood and well monitored to guarantee sufficient production yield in a near future. Among these parameters, there are the critical dimensions (CD) associated to the sidewall angle (SWA) values, the line edge roughness (LER) and the line width roughness (LWR).

Thus, a new metrology challenge has appeared recently and consists in measuring “accurately” the fabricated patterns on wafers in addition to measure the patterns on a repeatable way. Therefore, a great effort has to be done on existing techniques like CD-SEM, Scatterometry and 3D-AFM in order to develop them following the two previous criteria: repeatability and accuracy in order to get the lowest TMU (Total measurement uncertainties) values.

In this paper, we will compare the 3D-AFM and CD-SEM techniques as a mean to measure LER and LWR on various materials (silicon, 193 resist, E-Beam resist). Indeed, depending on the material type, the interaction between the electron beam and the material or between the AFM tip and the material can vary a lot and subsequently can generate measurements bias. The first results tend to show that depending on CD-SEM conditions (magnification, number of acquisition frames) the final outputs can vary on a large range and therefore show that accuracy in such measurements are really not obvious to obtain. On the basis of results obtain on various materials that present standard sidewall roughness or predefined sidewall roughness and with different software analysis, we will show the limit of each technique and will propose different ways to improve them in order to fulfil advance roadmap requirements for the development of the next IC generation.

7520-15, Session 4

Optimization of overlay correction methods and monitoring scheme for double patterning technology

T. Chiou, ASML Taiwan Ltd. (Taiwan); C. Huang, C. Chue, Nanya Technology Corp. (Taiwan); J. Lee, A. C. Chen, ASML Taiwan Ltd. (Taiwan); C. Shih, Nanya Technology Corp. (Taiwan)

Double patterning technology (DPT) is capable of extending usability of the immersion ArF systems for 32nm half-pitch and below. However, overlay error between the two patterning steps will directly contributes to critical dimension (CD) variation in a litho-etch-litho-etch process [1,2]. When CD uniformity budget becomes tighter and tighter in the coming technology nodes, overlay error needs to be well controlled to enable the DPT. For example, the 32nm DPT requires overlay performance smaller than 3nm for a single critical layer. However, the most advanced scanners today are able to provide a 3-4nm dedicated chuck overlay accuracy (single machine usage with chuck dedication, so dual chuck usage for optimum overlay at full productivity) [3]. Clearly not yet sufficient to meet 3nm on product overlay requirement and not leaving much room for process/production environment contributions. Various overlay correction schemes are then crucial to help achieve the tight target.

In general measured overlay errors are decomposed into linear and higher-order terms as well as residue. The linear terms and some of the higher-order terms (also known as correctables) can be corrected by today’s scanners. Several overlay correction schemes have been developed to suppress overlay errors coming from the exposure system or various processes [4]. For instance, a linear model is applied to correct intra- and inter-field overlay errors. The non-linear errors can be further corrected with higher-order process correction (HOPC) technique. Furthermore, overlay errors in each individual field can be corrected separately (correction per exposure, CPE). Similarly, correction of higher-order terms in a field (i.e., intra-field high-order process correction, iHOPC) is also applicable to correct more overlay errors.

To well present overlay performance and correct the errors through modeling later on, sufficient overlay markers that are distributed evenly across an exposure field are required. Consequently, the intra-field overlay errors can be corrected accordingly. For the inter-field correction, in principle a model that covers overlay errors in all exposure fields is preferred to appropriately reflect overlay variation across the wafer. However, the metrology time will be an issue for the increased number of measured markers. For example, Fig. 1 shows that the total measurement time is increased dramatically when increasing the number of sampling fields. Note that in this case only 5 markers were selected within a field. If the number of field markers increases, not only metrology time raises significantly, but also distribution of the markers plays important role in overlay modeling accuracy. An example of field-marker accuracy through sampling scheme is shown in Fig. 2. One can see that a 9-marker sampling with proper marker distribution is able to improve overlay by nearly 2nm (18%). These two examples indicate that optimizations of marker sampling within a field and field sampling on a wafer are needed to take care of both model accuracy and throughput. In this paper, we develop automatic sampling approaches for all overlay correction schemes to increase model accuracy for DPT. Meanwhile the metrology time is considered in the optimization loop. Furthermore, when applying the methodology to monitor on-production overlay, the overlay performance can be handled efficiently to meet the overlay requirement of the 32nm DPT production.

7520-16, Session 4

Optical critical dimension measurements for patterned media with 10s nm feature size

Y. Liu, Nanometrics Inc. (United States) and Seagate Technology LLC (United States); M. Tabet, J. Hu, Nanometrics Inc. (United States); Z. Yu, W. Hu, S. Zhu, J. J. Hwu, S. Lee, Seagate Technology LLC (United States)

Data storage density of hard disk drives has increased 8 orders of magnitude in the last 50 years. To keep increasing the recording density, there is a need to make the small bits thermally stable. While it seems the strongly coupled, high Ku magnetic materials are needed, the recording head may lose its ability to write on the highly coupled recording layer. In order to overcome the writability issue, patterned media has been proposed as the bits of patterned media are magnetically separated from each other.

Patterned media manufacturing presents a number of metrology challenges, such as the charging issues of quartz template for e-beam based metrology, the difficulty to reach the small trench bottom (56nm pitch or less) for AFM, and UV imprint resist shrinkage to e-beam and VUV light. For the first time, OCD technique, which has relatively recently been shown to yield very accurate information on the critical dimensions, wall-angles and detailed wall shape of grating structures in semiconductor industry, is introduced for patterned media applications.

This talk presents the successful OCD applications, which use spectro-

scopic, specular reflected light measurements (ellipsometry-SE) of grating structures and the analysis using Rigorous Coupled-Wave Analysis (RCWA), to extract accurate grating profile for Quartz template and UV imprint resist structures with the pitch as small as 56nm. The OCD measured grating profiles match the cross-section SEM imaging scans perfectly, and the correlation between OCD and AFM for the remaining layer thickness (RLT) of UV imprint resist is linear with R^2 > 0.99. The OCD results show that it is the leading candidate to overcome these challenges for patterned media metrology.

7520-17, Session 4

Ultra-sensitive optical metrology for hard disk DTR and BPM imprints

L. Hu, J. W. Roberts, I. Bloomer, n&k Technology, Inc. (United States); Y. Liu, S. Lee, Seagate Technology (United States)

With pitches in the double-digit nanometer range and depths in the single-digit nanometer range, superior sensitivity is a necessary metrology requirement for measuring hard disk drive discrete track recording (DTR) and bit patterned media (BPM) imprints. This presentation describes an ultra-sensitive metrology system, adapted from semiconductor scatterometry, which furnishes a non-destructive optical measurement solution for DTR and BPM imprint media.

The optical metrology system introduced in this talk relies on the measurement of polarized reflectance (Rs and Rp). The quantities “Rs and Rp” represent two polarization states of reflectance. The optical design is based on reflective optics with no beam splitters or refractive lenses, to produce optimized signal-to-noise of the polarized reflectance (Rs and Rp) data over the entire measured wavelength range, from 190 - 1000nm. Classical reflectometry incorporates one or more beam-splitters, as well as refractive optical components, resulting in less than optimum signal-to-noise, particularly in the deep UV wavelength regime (190 to 350nm).

The measured Rs and Rp data is analyzed using valid physical models: Rigorous Coupled-Wave Analysis (RCWA) in conjunction with the Forouhi-Bloomer dispersion equations for optical properties, n and k.

We will present depth, CD, and side-wall angle measurement results, obtained from using this ultra-sensitive polarized reflectance system. The measured samples have a pitch of 100nm, and different thicknesses of DLC coating, with etch depths ranging from 5nm to 15nm. It will be shown that the measured Rs and Rp data of these samples differ by no more than one per cent, and that the differences mainly occur in the deep UV wavelength range, from approximately 190 to 350 nm.

7520-18, Session 4

After development inspection (ADI) studies of photo resist defectivity of an advanced memory device

H. Kim, B. Lee, Samsung Electronics Co., Ltd (Korea, Republic of); H. Xiao, Hermes Microvision, Inc. (United States)

Electron beam inspection (EBI) system is known for its high sensitivity and has been widely deployed in the fabs mostly for after etch inspection (AEI) and post chemical mechanical polishing (CMP) of conducting layer (polysilicon, tungsten or copper) applications. For technology nodes with larger feature geometry, most killer physical defects can be captured with optical defect inspection systems, thus the main applications of EBI system are focused on capturing electrical defects using the voltage contrast (VC) between normal structures and defective structures. Defects at ADI are physical defects and were mostly inspected with optical systems. For device with larger feature size, tiny defects of photo resist (PR) that are invisible to optical inspection system usually can be removed by PR trimming before the main etch process sequence, thus they won’t cause yield loss. When critical dimension (CD) shrinks to 3Xnm, techniques, such as double patterning, have to be employed and unit memory cell size is reduced from 8F2 to 6F2 and further to 4F2. The process window of PR trimming becomes very small. Small PR defects that cannot be captured by optical systems may not be killer defects in current generation, but will become killer defects in the near future. Therefore, study of EBI applications on PR patterns becomes necessary.

In this study, a PR wafer with focus exposure matrix was inspected with both an advanced optical system and an advanced EBI system, and the inspection results were carefully examined. We found that EBI can capture most killer defects that optical system captured. It can also capture certain critical defects that are very insensitive to optical system, such as nano-bridges.

7520-90, Session 4

Challenges in development and construction of stand alone inspection, metrology, and calibration tools for EUV lithographic application

R. C. Perera, EUV Technology (United States)

Extreme Ultraviolet (EUV) Lithography is currently viewed as the most promising approach for reaching the 22 nanometer node in the manufacture of silicon devices. One of the principal challenges in the ongoing EUVL research effort is the development of necessary at wavelength metrology tools.

EUV Technology manufactures custom R&D instrumentation for the utilization and analysis of short wavelength electromagnetic radiation - soft x-rays and extreme ultraviolet (EUV). Our company has pioneered the development of several of stand alone inspection, metrology and calibration tools for EUV lithographic applications that can be operated in a clean room environment on the floor of a fab. An overview of necessary metrology tools for EUV Lithography will be presented and the challenges in developing these tools in order to support the successful implementation of EUV Lithography for the 22nm node will be discussed.

7520-19, Session 5

Image reversal trilayer using a positive-tone 193nm resist

D. J. Abdallah, D. Lee, M. Neisser, R. R. Dammel, AZ Electronic Materials USA Corp. (United States)

Imaging sparsely separated small recessed-images such as isolated trenches and contact holes has become increasingly difficult. Image Reversal Trilayer (IRT) approach attempts to alleviate this by reversing the tone of a bright field positive photoresist image that has a larger lithographic process window. In addition, IRT provides a solution to the decreasing photoresist budgets and antireflection issues associated with high NA imaging by incorporation of a thick optically tuned carbon hard mask. By placing the silicon hard mask over a photoresist image many of the problems associated with imaging on SiHM with standard trilayer processing can be avoided as well.

Feasibility of this image reversal trilayer process was previously demonstrated by patterning of trenches and contact holes in a carbon hard mask from line and pillar photoresist images, respectively. Improvements have been made in both the SiHM and CHM. The 2nd generation siloxane type SiHM does not require resist freezing and has a higher Si content and the polysilazanes type, which has shown to also incorporate an inherent shrink capability which extends the resolution of small recess structures, was modified so that the shrink can be controlled through resin modifications as opposed to the etch process. This paper describes the lithography, pattern transfer process and 2nd generation hard mask materials developed for the IRT processing. Particular emphasis will focus on pattern density effects which is applicable to any top-coating image reversal process.

7520-20, Session 5

Resist freeze double patterning on spin-on trilayer materials

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Many approaches to double patterning have been devised, of which most have been designed to reduce the number of process steps. The resist freeze process is one such technique that eliminates the first etch step from the standard litho-etch litho-etch (LELE) process. The resist freeze material chemically modifies the patterned photoresist, as well as potentially the layer beneath, which may result in a performance change at the second lithography step. In this paper, we present the results of resist freeze double patterning on standard trilayer stacks consisting of a silicon hardmask on top of a carbon underlayer. Comparison of pattern profiles of first and second lithography steps will be made, and the effects of formulation modifications of the silicon hardmasks will be examined. Also, the contribution of the carbon underlayer to lithography performance will be investigated.

7520-21, Session 5

Latest developments in photosensitive DBARCs

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Anti-reflective coatings (ARC) have become integral part of lithography to control CD. AZ is a pioneer in developing both top (TARC) and bottom anti-reflective coatings (BARC). Developable anti-reflective coatings (DBARC) are emerging materials technology. The biggest advantage of DBARC is it eliminates the need of plasma etch thus avoiding any concerns of damage to plasma sensitive layers during implantation. In addition, DBARCs also help in addressing scum related defect issues. There are two types of DBARCs: photosensitive and non-photosensitive. Photosensitive DBARCs offer better resolution performance as the develop mechanism is anisotropic. Therefore, it is also more robust, capable of providing better resolution performance needed for less than 3X nodes. This paper provides general chemical concept, mechanism and performance of photosensitive DBARCs applicable for 248 and 193 nm exposures. We show how adjusting the photosensitivity of DBARC enables matching to different resists. Technical factors in resist that affect ability to match DBARC to resist are discussed. Examples including 130nm L/S KrF exposures, 80 nm L/S dry ArF exposures and 45nm L/S immersion ArF Exposures.

7520-23, Session 5

High Si content anti-reflective coatings and their extension to a UV freeze dual patterning process

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The work will be present in two parts. The first part discusses Honeywell's high Si content bottom anti-reflective coating (SiBARC) material UVAS. UVAS was designed for use in a multi-layer patterning scheme such as tri-layer patterning, however may be used in a single layer patterning applications as well. UVAS polymer platforms for ArF, KrF and EUV patterning have been developed. UVAS is a monomer based siloxane polymer chemistry and, as such, has the freedom to be tuned and adapted to suit the particular need of the patterning requirement. Simulations are used to determine the optimum thickness and optical properties for UVAS to achieve the minimum substrate reflectance required to meet the local patterning requirement. Most up-to-date photoresist patterning and integration data will be presented.

In the second part of the presentation we will discuss the extension of UVAS into a freeze based dual ArF patterning process. As IC manufactures explore different paths to meet the resolution requirements for next generation technology, patterning schemes which utilize a dual patterning process are under extensive evaluation or in some cases already be in use. One dual patterning process being investigated uses a 172nm UV cure to render the first photoresist pattern immiscible to the casting solvent and developer solution used to define the second photoresist pattern. This work investigates and compares the use of a SiBARC and an organic BARC for the patterning of the first photoresist features and how the film properties of the respective BARC films are altered by the UV cure. It is important that the thickness and optical properties of the BARC film be unaffected by the UV cure as this same film is reused for reflectivity control during the patterning of the second photoresist pattern.

We will present the change in thickness and optical properties of the UVAS-A SiBARC film versus 172nm UV cure dose, and how these modifications impact the lithographic process margin for patterning line-space photoresist features. Patterning results will be presented for both interleaved (pitch split) and cross-grid dual patterned photoresist features. An extensive discussion of the UV cure freeze process to construct 60nm contact holes with dry lithography using a cross-grid dual patterning process will be made.

7520-22, Poster Session

Synthesis and imaging study of a series of novel photoactive polymers with diazoketo groups in their side chains

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A kind of Photoactive polymer with Diazoketo Groups in its side chains has been reported in SPIE and other related papers, and this photoactive polymer can be used in deep UV non-CARs(non-chemically amplified resists) system. Based on the work above, a series of novel photoactive monomers with substituent like phenyl, p-methylphenyl, p-methoxyphenyl, p-dimethylamidophenyl on the end of the molecule are designed and synthesized. By changing their substituents , the maximum-absorption wavelength of the photoactive monomers has been moved to 356nm, and it still has a comparatively large absorption at 365nm (I-line). A series of photoactive polymers have been obtained by polymerizing the monomer with methyl methacrylate and hydroxy ethyl acrylate together. Upon irradiaton in the waveleng of 365nm, the diazoketo groups wich are in the side chains of the photoavtive polymers undergo the wolff rearrangment, affording ketens that react with water to provide base-soluble photoproducts. Applying this kind of photoactive polymers to non-CARs, a positive image can be obtained. The photoinduced reaction of the photoactive polymes is showed below. This kind of photoactive polymers have great value in I-line non-CARs, TFT-LCD and IC discrete devices processing. And the anti-dry etching ability is enhanced by the introduction of the benzene ring.

7520-31, Poster Session

Improvement on post-OPC verification efficiency for contact/via coverage check by final CD biasing of metal lines and considering their location on the metal layout

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As IC design complexity keeps increasing, it is more and more difficult to ensure the pattern transfer after optical proximity correction (OPC) due to the continuous reduction of layout dimensions and lithographic limitation by k1 factor. To guarantee the imaging fidelity, resolution enhancement technologies (RET) such as off-axis illumination (OAI), different types of phase shift masks and OPC technique have been developed. In case of model-based OPC, to cross-confirm the contour image versus target layout, post-OPC verification solutions continuously keep developed - contour generation

method and matching it to target structure, method for filtering and sorting the patterns to eliminate false errors and duplicate patterns. The way to detect only real errors by excluding false errors is the most important thing for accurate and fast verification process - to save not only reviewing time and engineer resource, but also hole wafer process time and so on. In general case of post-OPC verification for metal-contact/via coverage check, verification solution outputs huge of errors due to borderless design, so it is too difficult to review all points of them. It should make OPC engineer to miss the real defect, and may it cause the delay time to market, at least.

In this paper, we studied method for increasing efficiency of post-OPC verification, especially for the case of contact/via coverage check. For metal layers, final CD after etch process shows various CD bias, which depends on distance with neighbor patterns, so it is more reasonable that consider final metal shape to confirm the contact/via corverage. Through the optimization of biasing rule for different pitches and shapes of metal lines, we could get more accurate and efficient verification results and decrease the time for review to find real errors. In this paper, the suggestion in order to increase efficiency of OPC verification process by using simple biasing rule to metal layout instead of etch model application is presented.

7520-62, Poster Session

Metrology accuracy effect on process overlay performance

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Required overlay target has been getting tighter and tighter as design rules shrinks down continuously. It has been developed not only advanced tools but also various RETs (Resolution Enhancement Technology) to extend the resolution limits of lithography. However Overlay performance is completely yet dependent on exposure tool, though various methods have been investigated to improve the overlay performance.

We investigate the impact of overlay reading metrology on process overlay controllability. Generally, overlay reading accuracy is directly involved in process overlay by root-square-sum with other factors, such as exposure tool capability and process factors. Overlay performance has not been much affected by metrology accuracy. As the design rule shrinks down, overlay metrology accuracy becomes one of the critical issues in order to improve process overlay performance. In addition, overlay metrology can influence on overlay control in more complicated manners. Usually batch wafers are exposed with pre-decided align parameter based on measured overlay. Therefore final overlay also relies on the reliability of overlay metrology during sample.

In this study, we investigate the relation between TMU (Total Measurement Uncertainty) and real process overlay experimentally, for two types of overlay metrology systems, IBO & DBO. DBO (Diffraction-based overlay) has shown better TMU than IBO, so expected to be better metrology solution in view of accurate measurement. Overlay data from correction by each DBO and IBO (Image-based overlay) method will be compared with TMU of them.

7520-63, Poster Session

Hot spot management through design based metrology

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Recently several Design Based Metrologies (DBMs) are introduced and being in use for wafer verification. The major applications of DBM are OPC accuracy improvement, DFM feed-back through Process Window Qualification (PWQ) and advanced process control. In general, however, the amount of output data from DBM is normally so large that it is very hard to handle the data for valuable feed-back. In case of PWQ, more than thousands of hot spots are detected on a single chip at the edge of process window. So, it takes much time and labor to review and analyze all the hot spots detected at PWQ. Design-related systematic defects, however, will be found repeatedly and if they can be classified into groups, it would be possible to save a lot of time for the analysis.

7520-65, Poster Session

40nm mesh patterning using negative tone development process

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The semiconductor industry faces a change of reducing wavelength in order to achieve higher lithographic resolution. It is the general consensus that EUV lithography will not be ready for the 32 nm node and probably also not for the 22 nm node. Water-based 193 nm immersion lithography is the only option for the next nodes; however, its resolution limit at a maximum practical NA of 1.35 is around 50nm for contact hole pattern. In this situation, double patterning has emerged as the semiconductor industry's chosen method to continue shrinking feature sizes.

Chip manufacturers begin to focus on crossing lines to make contact hole patterns, so-called mesh patterning process. Mesh patterning processes include capping freezing, thermal curing, UV curing, negative-tone resist and negative-tone development, etc depending on the freezing method of first photoresist patterns.

Among these processes, negative-tone development has been proposed as a potential cost-effective double patterning technique, even though it has still challenges that must be overcome and understood in order to make it a manufacturing solution.

In this paper, we will demonstrate the potential and challenges of the negative-tone development process targeting 40nm contact hole patterns.

7520-66, Poster Session

Immersion and dry lithography monitoring for flash memories (after develop inspection and photo cell monitor) using a darkfield imaging inspector with advanced binning technology

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After-development inspection (ADI) and photo-cell monitoring (PM) are part of a comprehensive lithography process monitoring strategy. ADI is performed on product wafers after resist coat, exposure and development. PM is done on test wafers and monitors track and scanner performance. Capturing defects in the litho cell rather than at later process steps shortens the cycle time and allows for wafer re-work, reducing overall cost and improving yield.

Low contrast defects of interest (DOI) and multiple noise sources make litho inspection challenging. Broadband brightfield inspectors with selectable illumination bands and optical apertures provide the highest sensitivity to litho DOI.1 However, a darkfield imaging inspector with advanced binning capabilities has proven to provide a high-throughput option for litho defect monitoring.2

This paper describes a methodology that has been developed and implemented in production for monitoring litho layers. On a darkfield imaging inspector, a very high sensitivity inspection is used in conjunction with the advanced defect binning to detect pattern issues and other DOI and remove nuisance defects.

Starting with 65nm flash ADI, this methodology enabled the separation and tracking of 'color variation' defects that correlate directly to CD varia-

tions caused by an out-of-focus situation. An extensive study using a set of wafers exposed at different focus offsets demonstrated the capability of the darkfield imaging inspector to effectively detect and separate random defects from systematic 'color variation' defects related to focus excursions. The defect data correlated well with geometric variations in the critical dimensions of printed features as verified by spectroscopic CD measurements. Production data validated the use of the darkfield imaging inspector for high-throughput monitoring at ADI. This unique inspection capability proved effective at detecting excursions and alerting engineers to out-of-focus conditions, reducing the time required for scanner re-qualification and preventing yield-limiting defects from printing on production wafers.

For 65nm and 45nm immersion lithography PM, this methodology produced sensitivity to random defects at a lower cost-of-ownership. Based on an extensive study that compared relative capture of critical immersion defects (figure 2), the darkfield imaging inspector was implemented as tool-of-record for immersion lithography daily photo-cell monitoring. Production defect density trend data demonstrated capture of several excursions - each well-correlated to an increase in defectivity for a defect bin that related to a specific immersion-litho defect type.

Keywords: ADI, PM, CD variations, lithography, immersion lithography, defectivity, darkfield inspection, process monitoring

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7520-67, Poster Session

Control of CD errors and hotspots by using a design based verification system

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The shrink of device node to raise the integration is important for the raising of cost performance on memory device. Targeting the feature CD (Critical Dimension) and defect control to achieve a large process margin with high product yield become a essential management point under the node shrink, thus sufficient works have been progressed on the product level. In this work, control of the CD errors and hotspots will be discussed by using a verification system with an image verifier algorithm between design layout and wafer images. The NGR2100TM was utilized for a verification system. The verification works for the CD distributions and defect status are implemented on 4x nm DRAM memory.

It was able to confirm the CD distributions of targeting degree in fullchip regions. Using the measured CD data, the database processes were performed by analyzing the differences of target to real CD values. The database file is composed of gathering which has large error characteristics of CD data. The information of gathering data is used for the target correction based on the OPC (Optical Proximity Correction) procedure. The simplest way to compensate the CD errors caused by proximity is to have certain geometries on the mask resized so that all features print at the required dimensions on the wafers. Consequently, mask revision is processed through the confirming of final process condition using the optimized corrected values. The revised mask is subsequently examined under the same verifier condition compare to the previous test. Although the degree of distribution improvement is different related to the design target value, additional improvement is possible by re-analysis and optimization for the considering the etch load effect.

Detection of systematic hotspot was also evaluated using NGR system. First of all, fullchip simulation was performed under dose and defocus split conditions. The extracted defects from the simulation vary as the result of OPC accuracy and optimization. The weak points as defect are recalculated by pattern analyzer tool. The tool offers a defect grouping function for the specified layout size, thus it can be utilized as a sampling process in fullchip verification. Sampling points induced by the recalculation lead a strict process margin by measuring a PWQ (Process Window Qualification) wafer. Then, unpredictable-critical hotspots are verified through the fullchip measurement in margin boundary chip, thus they can be minimized by control of the defect origination.

7520-68, Poster Session

Bottom-anti-reflective coatings (BARC) for LFLE double patterning process

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Double patterning process using ArF lithography has been developed as one of the most promising candidate for hp32 and beyond, however complicated process flow and cost of ownership are the critical issue for this process. LELE (Litho-Etch-Litho-Etch) is the one of the standard process, but in order to reduce the process and cost, LFLE (Litho-Freezing-Litho-Etch) and LLE (Litho-Litho-Etch) process have been investigated as the alternative process. In these processes, Organic Bottom-Anti-Reflective coating (BARC) is used 2 times with same film in both 1st Litho and 2nd Lithography process. In 2nd Lithography process, resist pattern will be print at space area where exposed and developed in 1st lithography process. Therefore, organic BARC needs to have process stability in Photo and development step to keep good litho performance between 1st and 2nd lithography in LFLE / LLE process.

This paper describes the process impact of 1st exposure and development for organic BARC, and the LFLE / LLE performance with optimized organic BARC will be discussed.

7520-69, Poster Session

Silicon-based molecular resists for ArF lithography

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Molecular resists have drawn attention for fine patterning as they exhibit single molecular weight which is beneficial for LER/LWR control. The main problem of the molecular resists has been the resistibility to the etching process. The etch resistance have usually been improved by introducing rigid phenyl moieties to the resist, but this method is not compatible with ArF laser. To inherit the advantages of the molecular resist and increase the etch resistance, silicon-based molecular resist has been designed and synthesized for the multilayer photolithography process. For the exact control of the molecular weight, highly defined silicon backbone was needed. Thus, POSS® (Polyhedral oligomeric silsesquioxane) structure was chosen as the main silicon frame. Introduction of the acid labile group on the highly defined POSS gave silicon based molecular resist with high silicon loading up to 23%. Previously reported POSS-based resists have used a hydrosilylation reaction which gives a mixture of products. Application of a different reaction scheme has allowed us to synthesize POSS-based molecular resists with exact single molecular weights. The rigid structure of POSS is also thought to be advantageous for the increase of the etch resistance and physical properties. One of the disadvantages of the reported POSS-based photoresists was the low glass transition temperature, which is not compatible with current lithography processes. The other problem is the extremely high hydrophobicity of the POSS structure which does not allow the conventional washing process with a TMAH solution. Thus we focused on the side chain variation of the POSS structure to circumvent these problems. For the thermal stability, alkyl side chains have been changed to cyclic alkyl moieties. The synthesized molecular resists have proven their thermal stability up to 210 °C with neither melting point nor glass transition temperature observed on TGA analyses. With suitable side chains and introduction of the ether moieties, the surface property has been controlled to be comparable to that of the commercial silicon resists. The contact angle of the deionized water on the resist-coated wafer showed 68°, which is similar to that of the commercial silicon resist. The lithographic results with ArF laser will also be reported.

7520-70, Poster Session

Mesh patterning process for 40nm contact hole

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Double patterning with 193nm immersion lithography is generally recognized as a candidate for 40nm contact hole imaging techniques. However, the cost of double patterning should be much higher than single patterning lithography. Therefore most of chip manufacturers desire more simplified process. LLE (Litho-Litho-Etch) could be a better candidate than LELE (Litho-Etch-Litho-Etch) because of its simplicity.

In order to simplify the double patterning process, we have been investigating LLE process without freezing process. If freezing process is unnecessary, neither of freezing material nor additional coating nozzle is needed. Recently LLE process without any freezing materials has been investigated and successfully established to realize double patterning process.

In order to make 40nm contact hole patterns, mesh patterning process using crossing line patterns has a big advantage in terns of aerial image contrast against single patterning.

In this paper, we will present the feasibility test results of mesh patterning process without freezing materials for 40nm contact hole application.

7520-71, Poster Session

40nm mesh patterning using capping freezing process

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One of the most difficult layers to pattern with a usable process window is a contact level. As the industry moves towards 40nm node and beyond, the challenges associated with printing contact holes with a manufacturable process window have become increasingly difficult. Current high NA exposure tools such as 1.35NA, designed for 193nm lithography, are capable of printing 50nm contact holes at most.

In order to shrink contact hole patterns, there were a variety of processes such as a resist reflow, RELACS, SAFIRE and so on. However, we are no longer able to make use of these processes for 40nm contact hole patterning as we need to shrink not only hole diameter but pattern pitch.

In this paper, we will demonstrate the patterning performance of capping freezing process which is one of the mesh patterning techniques.

7520-72, Poster Session

Synthesis of ArF photoresist by reversible addition-fragmentation chain transfer (RAFT) polymerization with three methacrylate monomers

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ArF immersion lithography is a predominant technology to get fine patterns less than 100nm. And the synthesis of superior ArF photoresist is an essential factor for developing ArF lithography technology. Almost ArF immersion photoresist are prepared by free radical polymerization of some methacrylate monomers with lithography functionalities such as solubility change, resist, adhesion property, and so on. Because of easiness to polymerization and ambient polymerization condition, free radical polymerization is applied to produce various commercial polymers. However, free radical polymerization has poor reaction control ability to produce sophisticated, well-defined polymers. Also the polymer from free radical polymerization has high molecular weight distribution (PDI), more than (at least) 1.5. When applied to a copolymerization system, free radical polymerization yields polymer chains with different monomer composition. For low PDI and controlled composition polymer, controlled/living radical polymerization (CRP) can be applied. Three well-known controlled/living polymerization, atom transfer radical polymerization (ATRP), stable free radical polymerization (SFRP), and reversible addition-fragmentation chain transfer (RAFT) polymerization can produce a polymer with well defined structure, designed molecular weight, and low PDI. However, for lithography photoresist material, reversible addition-fragmentation transfer (RAFT) polymerization is the most appropriate method among these controlled/living radical polymerization methods, because of absence of metal catalyst, and adaptability to various monomers.

Because of superior polymerization ability, controlled/living radical polymerization has been applied to produce lithography photoresist, but detailed reaction information has not been announced. Just simple studies such as the relation of PDI and molecular weight on patterns were done. However, Kinetic study on reversible addition fragmentation chain transfer process of copolymerization system is important because the ratio of monomers in a polymer chain affects the property of the polymer. Also difference of polymerization process of free radical polymerization and controlled/living radical polymerization makes it more important; In case of free radical polymerization, a chain is produced in seconds, but in case of controlled/living radical polymerization, every chain is initiated and grows simultaneously. When they applied to copolymerization, the product from different methods has different monomer composition and physical properties. And this is a crucial factor on pattern property.

In this study, ArF photoresist composed of three different methacrylate monomers with different functions respectively was synthesized via reversible addition fragmentation chain transfer polymerization using 2-cyanopropyl dithionaphthalene (CPDN) as a chain transfer agent (CTA). The conversion of each monomer was measured by proton nuclear magnetic resonance (1H-NMR), and molecular weight and molecular weight distribution of polymer were checked by gel permeation chromatography (GPC). The effects of several factors including the initial ratio of monomers and the ratio of chain transfer agent to the amount of monomers or initiator on kinetics of monomers were checked. Also kinetics of each monomer in homopolymerization was checked and compared with that of copolymerization system.

7520-73, Poster Session

Overlay Improvement by ASML HOWA 5th Alignment Strategy

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In this study, we demonstrated the achievement of moderating the poor overlay at wafer edge area by using a high order wafer alignment strategy.

The mechanism is to use non-linear correction methods with high order models (up to 5th order), with support by the function High Order Wafer Alignment (known as HOWA) in scanner. Instead of linear model for the 6 overlay parameters which come from average result, HOWA alignment strategy can do high order fitting through the wafer to get more accurate overlay parameters which represent the local wafer grid distortion better. As a result, the overlay improvement for wafer edge is achieved. Moreover, since alignment is a wafer dependent correction, with HOWA the wafer to wafer overlay variation can be improved dynamically as well. In addition, the effects of different mark quantity and sampling distribution from HOWA are also introduced in this paper.

7520-74, Poster Session

Characterize the 65nm through pitch behaviors for scanner parameters by CD SEM and Scatterometry metrologies

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The through pitch behaviors or optical proximity curves are one of the most important benchmarks to evaluate the performance of lithographic process [1, 2]. In this study, the exposure settings are perturbed on one scanner intentionally to emulate the Optical Proximity Effect (OPE) through pitch matching for multiple scanners. Two processes are applied on the same scanner (TWINSCAN XT1700i), one is the reference process with the nominal exposure condition; the other is the perturbed process with some scanner parameters slightly changed from the reference process.

The sensitivity of the printed features to each scanner parameter that is adjusted is determined by exposing wafers with the minimum or maximum value of each parameter within the linear sensitivity range. Five adjustable scanner parameters are investigated in this study: dose, focus scan range, NA, _ringwidth, _center of the illumination pupil. Proxi65 reticle, the test reticle, contains the pitches with a variety of biases sufficient for selecting the target CD and can be used for exposing patterns for both SEM and OCD (Optical CD).

For the exposures, the illumination setting is an NA=1.1 annular source shape with inner/outer sigma 0.6/0.8 and x+y polarized light. The minimum and maximum pitches of the 1D line/space pattern are 130 and 500nm, respectively. Wafer CD is targeted at 66nm with mask CD 66nm, no assist feature is added for the isolated pitches. 18 pitches are selected for generating the OPE curve and they are the most sensitive ones to this illumination setting.

Two different kinds of metrology tools are used to measure the printed features; one is the CD SEM, the other is scatterometry. MCD (middle CD) measured by scatterometry is compared to the CD SEM data for the OPE curve. A very consistent offset between two metrologies is presented through the pitches; the range of the offset is about 4.5, and the R-squared value is greater than 0.98 for point to point of CD SEM versus MCD correlation. As a result of the metrology data, we have concluded that the OCD data are as reliable as the measurements by CD SEM.

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7520-75, Poster Session

Litho scenario solutions for FinFET SRAM 22nm node

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For the development of the most cost effective lithographic solutions for the 22nm node, the most likely lithographic process and relevant requirements (CDU, overlay, CoO) according to the respective technology roadmaps need to be identified. To this end, use cases being most representative for logic device are selected. Imaging solution scenarios for single exposure (SE), double exposure (DE), and double patterning (DPT), are proposed per critical layers. The respective process capability is predicted under ideal and realistic conditions. Emphasis is laid on source mask optimization (SMO) with standard DOE, customized multipole DOE and freeform DOE in order to identify the limits of each litho technology and therefore to anticipate the insertion point of EUV lithography.

SRAMs (Static Random Access Memory) are circuit components in most system-level, large scale integrated circuits such as microprocessors. Smaller SRAM cells can help providing faster processors that consume less power. For our study, 22nm logic FinFET (Fin Field Effect Transistor) SRAM is selected as the use case because FinFET SRAM cells are considered to be a potential successor to conventional planar transistors for 22nm node chips and allow cell size reduction without deteriorating SRAM stability. Here we focus on the back-end layers of FinFET SRAM, including metal, via and contact.

In a first step we report on the litho solutions performed under ideal scanner conditions with ASML Brion TachyonTM SMO product, which co-optimizes a pixilated freeform source and a continuous transmission gray tone mask based on merit functions of edge placement error. Per scenario, these simulations result in a set of preferred litho solutions with respective source and mask. These solutions have to conform to an imaging metric characterized by MEEF and common PW based on typical fab requirements.

In a second step the previously generated solutions are evaluated for CDU analysis using real scanner error budget. The purpose is to predict the CDU performance of scanner, process and reticle in order to identify the major contributors for every scenario solution. Finally the feasibility of proposed solutions will be verified for some selected scenarios by exposure and CD-SEM metrology and an analysis of lithographic limit for every scenario will be reported.

7520-76, Poster Session

Implementation of new recticle inspection strategy for mask quality control in memory fab

J. Cheng, KLA-Tencor Corp. (Taiwan)

This paper discusses a strategy of mask qualification inspection in an advanced memory fab. Progressive defects continue to be the major cause of mask degradation due to intensified exposure and environment control issues. Direct reticle inspection has been widely implemented in wafer fabs to provide early warning of haze defects before they reach critical levels. However, IQC of mask should be considered as well in the advanced fabs to reduce the risk before being exposed. Reticle inspection systems are increasingly challenged by aggressive sub-resolution assist feature (SRAF) and high requirement to detect printable defects. Previously StarLight2 was used as re-qual strategy for the whole mask inspection. Later developed Stralight2+ has better defect model capability and defect detection. In this paper, we will study the integrated inspection mode: Die-to-Die (D2D) on main pattern area and Stralight2+ on scribes and frames area to establish a new mask inspection strategy in memory fab. The StarLight2+ will address inspectablity challenge on aggressive SRAF and provide the early warming for crystal growth type defect on the scribe lines. D2D can act as guard in main feature during IQC and Re-qual.

7520-77, Poster Session

Programmable mask desgin of bendable LCD display

H. Huang, National Chiao-Tung University (Taiwan)

The color TFT-LCD has changed the habits of people watching TV, using computers, education, meeting and so on. The bendable TFT-LCD, which is different from traditional TFT-LCD, is more light and easy to carry. Students can carry their paper-like LCD to school and put them in their bag. People can also read daily newspaper from their package.

This study numerically analyes how a programmable mask is fabricated by using the biomolecule array technology. Particularly, how a TFT-LCD type programmable mask with an electrical signal applied can selectively transmit incident light. Besides, the biomolecule array having high density

was fabricated by selectively illuminated the ultraviolet light to a sample substrate.

7520-78, Poster Session

Fabrication of diamond and diamond-like carbon molds for nano-imprinting lithography

J. W. Yu, C. Cheng, National Cheng Kung Univ. (Taiwan); Y. Guo, Toppan CFI (Taiwan) Co., Ltd. (Taiwan); F. C. Hong, National Cheng Kung Univ. (Taiwan)

Micro- and nano-scale molds were fabricated using nanocrystalline diamond (nano-diamond) and diamond-like carbon (DLC) films for imprinting lithography. Patterning was first transferred to the resist on nano-diamond and DLC thin films by photolithography and imprint lithography methods, and then deep etching with inductively-coupled plasma reactive ion etching (ICP-RIE) was applied to transfer patterns to nano-diamond and DLC films for the fabrication of diamond molds. Nano-diamond films of about 1.5um in thickness were deposited on silicon substrates by hot filament chemical vapor deposition (HFCVD) by controlling CH4/H2 ratios and substrate temperatures. Thick diamond-like carbon films containing silicon oxide nanoparticles were deposited on silicon substrates by PECVD using gaseous HMDSO (Hexamethyldisiloxane) reactants to release the film stress. E-beam writer was used to pattern the resist on the Cr film-covered thick DLC film. By using ICP-RIE, Cr film was first patterned with the patterned e-beam resist as the etching mask, and then DLC thick film was etched to form nanoimprint mold using the patterned Cr as the etching mask. High fidelity nano patterns were transferred with nano-imprinting lithography using the nano-diamond and DLC molds. Good mold releasing behavior and high mold strength were observed for the nanocrystalline diamond and DLC molds due to their highly hydrophobic surface and high toughness, respectively. Further details will be described in this paper.

7520-79, Poster Session

Critical dimension reconstruction of metrology test structures with programmed line edge roughness by scatterometry

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As semiconductor manufacturing technology advances to sub-45-nm nodes and the critical dimension (CD) continues to shrink, the need for dimensional accuracy grows more critical. Line edge roughness (LER), fluctuations in the line edge of lithographic structures, can be a significant fraction of the feature dimensions and it will limit circuit performance in the next generation technology nodes. Scatterometry as a non-destructive and cost effective optical metrology for next generation technology has been applied to periodic fine line-space structures to determine geometric parameters such as CD, side-wall angle and height. Since SEM is not capable of measuring LER at the bottom and AFM capability is limited in dense structures, the requirement for a reliable LER measurement is in demand. Therefore, we investigated the LER influence on scatterometry applications. The metrology test structures with programmed LER are fabricated by e-beam lithography to verify and improve the scatterometry models. CD and LER are reconstructed by using the diffraction pupil images of scatterometry measurements.

The metrology test structures were exposed on resist ZEP-520A using an Elionix ELS-7000 100-kV e-beam direct-write machine. The test structures are with CD between 30 and 120 nm, the pitch of 200 nm and 600 nm, and thickness of 40 nm and 100 nm. We also have fabricated programmed LER structures with CD between 80 and 120 nm, pitch of 200 nm, and thickness of 100 nm. Complete diffraction pupil images of these periodic gratings are captured for CD reconstruction. The diffraction pupil images are measured with TE and TM polarization light. Seven wavelengths of 425, 450, 500, 550, 650 and 700 nm are available for measurement. With proper modeling of the given features, Maxwell equations are solved numerically to reconstruct the CD profile based on the measured pupil images. CD and side-wall angle can be obtained from the reconstructed profile. In addition to the regular grating patterns, specially designed gratings with programmed LER are considered as well. CD profile models for various designed LER patterns will be created and investigated in this study.

7520-80, Poster Session

Study of OPC accuracy by illumination source types

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The challenge for the upcoming full-chip CD uniformity (CDU) control under 3Xnm nodes is unprecedented with expected specifications in semiconductor manufacturing. To achieve these requirements, OPC models not only must be accurate for full chip process but also be developed in advance. For that reason, robust OPC using real lithographic terms was proposed. Real lithographic systems have deviations from ideal behavior in the process, illumination, projection and mechanical systems as well as in metrology. The deviations from the ideal are small but non-negligible. In case of OPC model accuracy, There are multiple sources of residual errors in the model, and model inaccuracies are only one of several factors which contribute to errors in the final wafer image. One significant class of modeling error is related to how the illumination source is used. This topic has been researched extensively in recent years.

For this study we assess accuracy of optical model for robust OPC using ideal and actual illumination sources, and test conditions are below.

1) We examined the difference of pupil types to output model respectively.

2) A parameterized test pattern layout was used by 1D test pattern types that have various lines and spaces.

3) All models were calculated in automation method so as to exclude the dependency of user skills.

4) OPC accuracies were examined by gate layer patterns on full chip level.

The study is performed for 5X~4Xnm nodes lithographic processes. The main focus of the study was on usability of model that is made by measured source data in semiconductor manufacturing. Results clearly showed that actual source for optical model have merits and demerits.

7520-81, Poster Session

Expanding The lithography process window (PW) with CDC technology

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Semiconductor device nodes are continuing to shrink and require strict specs of CD uniformity resulting in a narrowing of the lithography process window. In order to continue using the current litho equipment for at least one more generation, methods must be found to expand the process window.

This paper will demonstrate a way of expanding the lithograph process window by using the Carl Zeiss CD Control (CDC) Technology.

Reduced yield was evident in a production memory product in PSC fab P1/2 due to reduced process window in Poly layer. CD non uniformity of 3.95nm 3S and 6.5nm range in this layer was found after close examination in the fab.

A Carl Zeiss CDC200 tool was used to apply the CDC process to improve the CDU.

It was evident in the post CDC results that the CDU 3S was reduced to 1.94nm (53% improvement) and 3.7 nm Range (43% improvement).

Additional verification of this layer's process window showed an increase of DOF from 0.15 um pre CDC to 0.3 um post CDC and an exposure latitude

increase from 18.7% pre to 26.7% post CDC.

To summarize our findings, application of the CDC process to the problematic layers allowed to increase the PW in both DOF and exposure latitude by improving the CDU of the layer, thereby substantially increasing the yield of this product.

7520-82, Poster Session

Fulfilling a comparably optical performance of sub-60nm half-pitch pattern using an optimization of advanced diffractive optical element and mask transmittance

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Decreasing the cost of production is the first priority in memory introductory. Engineers are chasing this goal and requested to approach it. It is also a necessity of reducing red ink during the great depression in particular. According to the custom, the promptest and the most effective method is increasing the yield on a wafer.

In DRAM industry, making use of immersion tool is a direct means if a producer wants to arrive at mass production of sub-60 nm generation node without fierce fluctuation. However, here is a question. Up to the present, an immersion tool is still a huge investment for the majority of memory manufacturers. Moreover, it would be a hardship to attain the adequate equipment, which is manipulated in a scale of mass production, for them in such a slump.

Therefore, the focus of lithographic study has been buried in how process engineers print out sub-60 nm patterns by conventional ArF tool. Double patterning is a highly potential technique for this thorny circumstance no matter what kinds of camps they are; Litho-Etch-Litho-Etch or Litho-Litho-Etch. But they would be confronted by new challenges, such as pattern overlay, instability in novel process, and so on.

Based on the above, we should survey other alternatives simultaneously on the basis of bringing about only a minuscule process variation and equipment on hand.

To do so, we concentrate on single exposure and a combination of high transmittance mask (high T mask) and advanced diffractive optical element (DOE) in 54nm half-pitch. Under a concern of the mask 3D effect, we evaluate the optical performance in a transmittance range from 6 to 30 percent and between convectional (dipole-40, NA0.93, 0ut/ in=0.97/0.82) and advanced illuminations (dipole-20, NA0.93, 0ut/ in=0.97/0.85) by lithographic simulator. Next, a series of fine tune of mask pattern sizing are verified to correspond to real condition on resist patterning. Additionally, MEEF is also put into investigation for a precise judgment.

As anticipated, a possible candidate is discovered in the optimization study between mask transmittance and advanced DOE. Meanwhile, we establish this persuasive evaluation procedure.

Importantly, this simulation assessment, from a perspective of limited investment, proposes a promising resolution of production cost and process dilemma. We also attempt to draw a conclusion to when the occasion for application of high transmittance mask is. Both of them can provide a valuable reference for research and practice.

7520-83, Poster Session

Green binary and phase shifting mask

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SixNy/Ni thin film green mask blanks were developed , and are now going into be used to replace general Chromium film used for binary mask as well as to replace Molydium silicide embedded material for AttPSM for i-line (365nm), KrF(248nm), ArF (193 nm) and Contact/Proximity lithography. A bilayer structure of a 5nm thick opaque, conductive nickel layer and a SixNy layer is proposed for binary and phase-shifting mask. With the good controlling of plasma CVD of SixNy under silane (50 sccm), ammonia (5 sccm) and nitrogen (100 sccm), the pressure is 250 m Torr. and rf frequency 13.65 MHZ and power 50W. SixNy has enough deposition latitude to meet the requirements as an embedded layer for required phase shift 180 degree, and the T% in 193, 248 and 365 nm can be adjusted between 2% to 20% for binary and phase shifting mask usage. Ni can be deposited by e-gun, its sheet resistance Rs, is less than 0.8 kΩ/square. Jeol e-beam system and i-line stepper are used to evaluate these thin film green mask blanks, feature size less than 200nm can be printed. Transmission and reflection spectra of various SixNy/Ni layers are inspected by using UV spectrometer, Optical constants of the SixNy/Ni film are measured by n & k meter and Durability against photomask cleaning is controlled by pinhole inspection using particle counter. Detail applications of these green thin film for Binary and Phase shifting mask will be presented in the conference.

7520-84, Poster Session

Development of high n organic BARC for 193nm immersion photolithography

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193nm immersion photolithography enables high resolution photoresist pattern printing, which is necessary for 45nm node and beyond integrated circuit (IC) chip fabrications. In general, thin photoresist film is needed for high resolution resist pattern generations. However, on the other hand, plasma etching pattern transfer process requires as much as possible resist film thickness for good pattern transfer fidelity. To balance those conflicting requirements, several different patterning resist schemes were suggested and developed in past a couple of decades such as top surface imaging, bilayer and trilayer resist schemes. Mainly due to good resist compatibility and flexibility for reflective control, organic bottom antireflective coating (oBARC) is widely used in advanced IC manufacturing processes and likely its use will be continued for future generations such as 3x and 2x nm node chip fabrications. To minimize resist film thickness loss during oBARC layer plasma etch opening, high etch rate oBARC was developed and is widely employed in IC industry. Another approach to tackle on this conflict is to use thinner BARC. Under same set of resist patterning conditions including illumination condition and substrate stack, thinner BARC film thickness with same level of reflectivity control requires BARC with higher refractive index. High refractive index such as larger than 1.95 is very challenging for synthetic organic polymers. In this publication, physical characteristics of high n polymers, simulation results involving in using high n BARC and characterizations of oBARC developed based on high n platform polymers such as immersion resist compatibility, outgassing and etch performances will be presented.

7520-85, Poster Session

A novel single-component chemically amplified positive DUV photoresist derived from PHS

J. Liu, L. Wang, Beijing Normal Univ. (China)

Poor compatibility in two-component or three-component resist between the PAGs and the polymer matrix could cause acid diffusion and non-uniform deprotection reaction and some other problems.Single-component resist system, which are constructed by the polymers consisting of two major functional components, photoacid-generating unit and the acid-labile unit,will improved the performance of resist material. In this paper, poly (p-hydroxylstyrene) was used as raw material and a novel polymer was synthesized with sulfonuium triflate group attached on part of the benzene rings by chemical reactions and the hydroxy groups partly protected by t-BOC, which can be used as a kind of single-component CA positive photoresist. The PHS derived polymer can be dissolved in common solvents. The thermal stability, UV absorption, photolysis property, acidolysis of the polymer were investigated.The lithographic performance of the polymer as single-component positive DUV photoresist was evaluated.

7520-86, Poster Session

Abbe-PCA-SMO: microlithography simultaneous mask and mask optimization using Abbe-PCA

C. C. Chen, National Taiwan Univ. (Taiwan); L. S. Melvin III, Synopsys Inc.

With the growing need for high quality optical proximity correction (OPC) for deep-sub-wavelength microlithography. Not only the mask shape need to be complexly altered such as scattering bar, or phase shift mask, the light source shape, polarity, and intensity also acted as another optimization variable.

It is easy to see that the first difficulty of developing complicate simultaneous source mask optimization (SMO) algorithm is the kernel generation time. It is well-known that the well-known Hopkin's method is suitable for compact kernel generation. However, the runtime could be huge if frequent source modification is need. On the other hand, Abbe's method can easily adopt the SMO task, however, the kernels are not compact.

Last year, we proposed Abbe-PCA algorithm which generates as compact kernels as Hopkin's method and as fast as Abbe's method. Abbe-PCA perform Principle Component Analysis to the E-field instead of I-field which is much smaller and easier task. Combing with analytical decomposition algorithm. Abbe-PCA is very efficient and accurate. Since Abbe-PCA evolved from Abbe's method, it can serve as good candidate for SMO task.

In this paper, we will present that Abbe-PCA can perform efficient SMO with great accuracy. Couple with advanced adjoint optimization method. Abbe-PCA-SMO is hundred time faster than the Hopkin's method. Extensive experimental results demonstrate the efficiency and accuracy of this method, Abbe-PCA-SMO.

7520-87, Poster Session

Subwavelength plasmonic photonics for photolithography beyond the diffraction limit

K. Chen, National Cheng Kung Univ. (Taiwan)

The diffraction limit sets a minimum value on the product of the line width and the angular divergence of light. As limited by the diffraction, photolithography becomes the key issue preventing the semiconductor industry from progressing according to Moore's Law. Besides to employ a shorter wavelength, one solution is to make three dimensional circuits that require the through-silicon vias (TSV) with high-aspect-ratio holes/lines. But, the light divergence and thus the depth of focus in conventional photolithography becomes the problem. Here, we propose possible subwavelength plasmonic photonic solutions related to both line width and divergence limitations. We note that the wave function within a subwavelength metallic slit whose width is smaller than half the wavelength is not considered in conventional optics or quantum theories. Thus, while we still obey the fundamental wave concept, we demonstrate, with both FDTD simulation and experimental NSOM measurement, that by utilizing a new setup of a metallic subwavelength aperture as the lens to preserve, generate and squeeze the sub-limit wave functions an incident light can be focused in the intermediate zone to a single-line width with its value smaller than the diffraction limit of half the wavelength. The fields focused by the lens with the focusing aperture beyond (FAB; i.e., "fabulous") this limited line width are verified to be radiative with a momentum capable of propagating toward the far zone as concerned by the limit and in sharp contrast to the evanescent near-field that cannot freely propagate in free space. Thus, the working distance with this sub-limit light focusing can be longer. On the other hand, with a different structure and physics mechanism, our simulations have produced 2-D super-collimated (i.e., divergent-less) light beams in free space which beats the divergence aspect of the diffraction limit. The preliminary NSOM measured result agrees with that from our FDTD simulation. We find that the wave fields can also propagate and the field amplitude remains constant for more than fifteen wavelengths while its width is only about two wavelengths. Also, we have built an exposure machine; the widths of the exposed patterns for different distances between the structure and the photo-resist remain almost same. As feasible fourth generation photolithography solutions, higher resolution, simplicity and lower-cost are three notable anticipated features in these two breakthroughs. Both focused aperture printing and direct writing are possible. The practical issues of the working distance and the depth of focus can be solved according to the ITRS roadmap.

7520-88, Poster Session

Heat conduction considering heat loss to photoresist on top of wafer during post exposure bake

M. Jung, S. Kim, D. W. Kim, H. Oh, Hanyang Univ. (Korea, Republic of)

Post exposure bake (PEB) process among the lithography steps is important for making good patterns when the chemically amplified resist is used. During PEB, the de-protection reaction and acid diffusion are determined by bake temperature and time. One of the key factors that determines the de-protection and acid diffusion is the initial temperature rising inside the photoresist. The time delay between the temperature rising from the room temperature to the pre-set bake temperature is the main cause of line width variation. It is very important to control 1~2 nm line width variation for patterns of 32 nm and below. This variation mainly comes from PEB temperature and time of the resist on top of the multi-stacking silicon wafer on hot plate. In order to predict the accurate PEB temperature and time applied to the resist, we studied heat transfer from hot plate to the resist on top of the silicon wafer. We calculated boundary temperature values of each layer and compared the change of temperature caused by different kinds and thicknesses of sublayers including antireflection coating and resist. Heat loss to the environment is also included to solve real heat conduction problem. We also found that the resultant line width is changed by small temperature variation, stack thickness or layer numbers.

7520-89, Poster Session

FAST-LH: a manufacturing-environmental friendly method of lens heating monitoring

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Lens heating (LH) monitoring is crucial for photolithography process control; ineffective lens heating compensation will cause severe focus and image drift on photoresist pattern. Conventional/standard lens heat-test recommended by equipment vendor normally requires long measuring time which is not manufacturing-environmental friendly, and it is designed more to equipment perspective.

A fast and accurate method of lens heating monitoring (FAST-LH) is discussed in this paper. Focus drift induced by lens heating is measured using both conventional and FAST-LH; result comparison shows strong correlation of focus drift with the new measuring method. Detailed methodology for the lens heating monitoring is studied; a fine tuned new measuring method is proven to be not only fast but also accurate to monitor lens heating LC compensation rate. Compared to the conventional method, FAST-LH could reflect better the actual focus drift under manufacturing environment. Due to the limitation of transforming the FAST-LH to equipment LH compensation settings, the FAST-LH is implemented for periodic monitoring and feedback; whereas the conventional method is used during compensation/corrective action.

7520-91, Poster Session

Preliminary design of a two-dimensional electron beam position monitor system for multiple-electron-beam-direct-write lithography

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Multiple-electron-beam lithography is one of the promising candidates for next-generation lithography because of its high resolution and ability of maskless operation. In order to achieve the throughput requirement for high-volume manufacturing, miniaturized electro-optics elements are utilized in order to drive massively parallel beams simultaneously. Electron beam drift problems can become quite serious in multiple-beam systems. Periodic recalibration with reference markers on the wafer has been utilized in single-beam systems to achieve beam placement accuracy. This technique becomes impractical with multiple beams. In this work, architecture of a two dimensional beam position monitor system for multiple-electron-beam lithography is proposed. It consists of an array of miniaturized electron detectors placed above the wafer to detect backscattered electrons. The relation between beam drift and distribution of backscattered-electron trajectories is simulated by an in-house Monte Carlo electron-scattering simulator. Simulation results indicate that electron beam drift can be effectively estimated from detector array output signals.

7520-92, Poster Session

Influence on digital photolithography intensity by collimated Gaussian beam

N. Luo, Y. Gao, S. He, Y. Rao, Nanchang HangKong Univ. (China)

Recently, digital lithography technology based on Digital Light Processing (DLP) has caused the extensive attention. Generally, digital lithography system includes light source, beam expansion and collimation system, Spatial Light Modulator (SLM), projection lens and substrate platform. Beam expansion and collimation is the key technology, which directly affects the imaging and lithography quality. If the laser with short wavelength is used as light source, the emergent beam after phase transform by lens group is still of Gaussian distribution. The spatial self-transform characteristics of Gaussian beam ensure the stability of its spatial propagation. However, it necessarily causes great difficulty in collimation. The beam can't be completely collimated by any optical system and has the residual Gaussian attribute. In order to analyze the influence of residual Gaussian attribute on intensity distribution of digital lithography system, we simulate the diffractive field distribution behind the beam expansion and collimation system.

The wave propagation in digital lithography system satisfies the diffraction of paraxial optical system. Thus, Collins integral is used to demonstrate the diffractive field distribution behind beam expansion and collimation system. The optical field of beam with Gaussian attribute passing through 2-D sinusoidal grating is analyzed. Finally, the step depth error of binary element is evaluated under illumination of Gaussian beam. And the optimization design of optical path is proposed.

If the axisymmetric paraxial optical system exists between diffraction plane and observation plane, it can be expressed by ABCD matrix. The beam collimation system mostly adopts reversed telescope system. Firstly, we calculate the matrix elements ABCD of the reversed telescope system. According to Collins formula, the relation between output optical field and incident field can be achieved. Then the intensity distribution behind beam expansion and collimation system can be simulated. Considering the characteristic of light source in DMD-lithography system, we achieve and simulate the complex amplitude distribution of base mode Gaussian beam passing through the beam expansion and collimation system. Taking example for 2-D grating, we simulate the modulation characteristic of beam with Gaussian attribute passing through 2-D grating. The simulation result shows that the intensity in the central area is obviously higher than that in the surrounding area, which will causes the peeling thickness of photoresist in the central is greater than that in the surrounding area. For binary step-type elements, the relation between intensity and step depth error is investigated and simulated furtherly. The step depth error is an exponential function of intensity. The maximum depth error between the center and the edge approximates to 38.5nm, which is equal to 10.97% of the theoretical depth. Thereby, the influence of residual Gaussian attribute on digital lithography system should be considered.

Simulative and experimental results show that the beam from expansion and collimation system still has residual Gaussian attribute. During exposure, some step depth error is introduced, which will affect the fabrication quality of elements. Therefore, we add fly's eye or integral lens behind beam expansion and collimation system to obtain higher light energy utilization and greater uniform illuminating area.

7520-93, Poster Session

Research on DMD-based gray-scale exposure model

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Digital lithography technology based on digital micromirror device (DMD) has caused the extensive attention recently. DMD is one of the reflective spatial light modulators (SLMs), which has inherent advantages such as high resolution, high brightness, high contrast and quick response. DMD digital lithography technique belongs to the parallel direct writing based on surface exposure. Hence, it promotes the fabrication speed of micro-optical element (MOE) mask. In the DMD-lithography system, the gray-scale pattern controlled by computer turns into the form of binary digits by video card, then they are output to DMD chip. The different gray scale results in the different deflection frequency of each micromirror, and accordingly the reflection flux of each micromirror is different. Therefore, the variable exposure can be obtained on the photoresist. The DMD reflectivity of each gray scale and the sensitive characteristic of photoresist decide on the fabrication quality of mask.

In this paper, based on DMD-lithography system, the mapping relation between gray scale an photoresist relief has been investigated. The DMD gray-scale exposure model has been established.

To obtain the DMD reflectivity of different gray scale, the change of step length is taken 10 from 0 to 255. After data fitting, we achieve the relation between gray scale and DMD reflectivity. Testing curve shows the light modulation of DMD is nonlinear from 0 to 255. However, the testing curve shows local linearization as well. The modulation of DMD is approximately linear from 40 to 130 and from 160 to 230. When designing the gray-scale mask, we should choose the gray scales in the same linear region to satisfy the requirement of multi-step relief.

Considering the light transmission in the DMD-lithography system and the development process, we set up the gray-scale exposure model. After being modulated by DMD, the reflection with mask information passes through the reduction projection system and images on the photoresist. After development, the photoresist relief can be formed. By comprehensively considering the influence of all parts on lithography, Equation (1) is deduced, which demonstrates the exposure distribution on photoresist can be transformed into relief structure after development.

$$d=a0*a1*a2*a3*Ce*I0*R*t*T/B/B \quad (1)$$

a0 represents the influence of reduction projection system on imaging intensity, a1 is a constant in relation to photoresist type and a2 is the exposure constant. Ce denotes the concentration of developer and a3 is a constant in relation to development. I0 represents the intensity of light source. R is the DMD reflectivity. t and T denote the exposure and developing time respectively. B is the transverse magnification of reduction projection system. According to Equation (1), we calculate the gray scales of 4-step grating, 4-step FZP, 8-step grating and 8-step FZP respectively.

The better experimental results are achieved when all the process parameters are reasonably controlled. Experimental results show that the exposure model is reasonable and correct. The establishment of exposure model has reference value for the precise control on gray scale in the DMD-lithography system.

7520-94, Poster Session

Calixarene-based molecular resists containing a PAG functionality for EUV lithography

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EUV lithography is thought to be a leading candidate for the pattern size of sub 30 nm. However, the stronger and shorter light sources like EUV have a big drawback to have very low output. In addition, as pattern size gets smaller, it is hard to get low enough LER at the line space pattern especially due to the distribution and the diffusion of PAG, which causes the image blur and limits the resolution of the resist.

We have designed and synthesized some novel calixarene-based molecular resists containing a photoacid generator (PAG) functionality to alleviate those sensitivity and LER problems in EUV lithography. Molecular resists have been investigated for fine patterning as they have a single molecular weight, which is useful for the LER/LWR control. PAG-bound polymer resists have been used for the higher PAG loading and the more uniform distribution of PAG to enhance the photosensitivity and to control the diffusion of photo-generated acids. Calixarene derivatives have been employed as chemically amplified molecular resists with a t-Boc protection of the phenolic hydroxyl groups in EUV lithography. As the -molecular orbital of the benzene ring is known to have a sensitizing effect, the calixarene-based molecular resists are predicted to be sensitive to EUV. The protecting groups of phenols in calixarenes can serve double purposes not only as acid-labile protecting groups but also as photo-labile protecting groups that produce acid after EUV exposure. Acid-labile protecting groups like acetal or tertiary ester functional group also can be introduced as a subunit of the molecular resists. Calixarene derivatives have at least 4 phenolic hydroxyl groups, thus it can have at least 4 PAG functionalities per a molecule to generate 4 equivalents of acid at once. The large size of the counter anion of the generated acid can control the LER to reduce diffusion length. Alternatively, the phenolic sulfonate derivatives have been introduced as a novel PAG, which could be cleaved with EUV to generate sulfinic acid and the sensitivity is acceptable. Although the fully protected calixarenes have a problem of solubility in the casting solvent, it could be solved with proper functionalization of the calixarene derivatives. The properties and lithography results of the prepared calixarene-based molecular resists containing a PAG functionality will be presented here.

7520-95, Poster Session

Improvement of KrF contact layer by inverse lithography technology with assist feature

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We discussed to KrF process extension for 90 nm technology node. The continuous shrinkage of critical dimensions on sub 130 nm devices becomes a key point to improve process margin with pattern resolution problem for lithography. Recently, according to development demand of high density and high integration device, it is tendency that the shrink rate of design rule is gradually accelerated. It is difficult to develop with image contrast problem around k1=0.25 which is a theoretical process limit region. We need to technology development which is available to having resolution for sub 90nm line and space by using KrF lithography not by using ArF lithography.

In generally, KrF have not been used in nano-process such as 90nm technology. In this study, however, we can apply the KrF in 90nm technology by means of minimizing the error range in the nano-process, optimizing assist feature, and extending the process margin. This Application of KrF in 90nm technology results in elimination of additional investment for development of 90nm technology.

In this paper we prove the impact of SRAF configuration both on pattern profile and process margin. We also show that the experimental data can easily be predicted by calibrating aerial image simulation results. As a conclusion, we suggest methodology to set up optimum SRAF configuration with rule and inverse lithography technology

7520-96, Poster Session

Generation and characterization of spatially distributed laser produced plasma extreme ultraviolet

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Two and three dot laser produced plasma extreme ultraviolet (LPP EUV) sources have been generated by using diffractive optical elements (DOE) on a slab tin target. A DOE could have better than 90% diffraction efficiency and better then 100 MW power handling capability would be the most suitable element for this task. A 1064 nm wavelength 15 ns FWHM pulse width Nd:YAG laser was used to excite the plasma. After passing through the DOE, the laser beams were focused onto the target by a pair of lens. The resulting spot radius was estimated 8.2 um on the target. The maximum pulse energy available on the target was 360 mJ. The EUV generated from the plasma was imaged by an 122 um imaging slit of a Jenoptic tool wheel. The one dimensional image of the LPP EUV together with its spectrum was recorded by an absolutely calibrated Jenoptic 0.25 m EUV spectrograph in a 45 degree geometry. The recorded 1D spatial distribution and EUV spectra demonstrate the feasibility of the EUV patterning by the novel optical method. The characteristics and potential application are investigated.

7520-97, Poster Session

The effect of the laser interference lithography patterns when substrate tilted

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The effect of the tilted substrate on the lithography patterns in maskless Laser Interference Lithography (MLIL) was numerically and experimentally studied. The two-beam interference lithography experiments are studied and the results are in good agreement with the numerical simulations. Research shows that the period of interference patterns becomes larger with increasing tilt angles of the substrate. It also showed that there has no evident change when the rotational angle no more than 3 degree in our experiment. The final results have certain significance for MLIL and fabrication of integrate circuit.

7520-98, Poster Session

Benefits from run to run CD control by using iODP for sampling rate reduction

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In order to improve production quality in semiconductor manufacture, the lithography process run to run (R2R) control is a principle solution for smaller critical dimension (CD) and faster throughput time of lithography process. A R2R moving average controller had been developed to improve process capacity (Cpk) of CD but CD-SEM measurement sampling rate and feedback time will be main factors to affect the controller efficiency. Moreover, higher measurement sampling rate which makes longer cycle time and requests more tool capacity is a difficult choice for high volume production. The iODP (integrated Optical Digital Profilometry) of Timbre Technologies, Inc. provides a solution for lower CD-SEM measurement sampling rate and meets the requirements for CD control in lithography applications simultaneously. Moreover, the measurement results direct from process tools can be utilized for R2R control to reduce feedback time and solve higher sampling request problem. Consequently, lower CD-SEM measurement sampling rate doesn't make the CD Cpk decline when iODP is adopted for CD control.

In this paper, we studied several control schemes of The DT (Deep Trench) structures from the 70nm node process with simulation in order find the best control methodology with moving average controller for high CD sampling

rate. The schemes are: (1) traditional full usage of CD-SEM measurement data; (2) full usage of iODP measurement data; and (3) usage of both of CD-SEM and iODP measurement data with different weightings. The LSQ method is adopted to find the optimal weight of specific interval. However, the optimal weight must be tuned carefully with different time intervals, otherwise, the CD variation could be increased because the difference between actual and optimal exposure doses makes CD off target. Besides, the reasonable filter interval for iODP measurement data is ±1.5nm for 70nm DT structure which is a reasonable matching specification for iODP matching to CD-SEM .

Unsurprisingly, the simulated CD Cpk purely from CD-SEM measurement data is perfectly matching to the real performance. However, the Cpk drops nearly 5% if the CD control is fully using the measurement data comparing to simulation result from pure CD-SEM measurement data. Moreover, the ideal doses simulated from pure SEM and iODP measurement data are identical which means the best simulated weightings of CD-SEM and iODP data should be capable to refer. Therefore, the sampling/hold weight compensator is chosen for the simulation of the third scheme. The result shows CD Cpk is in proportional to the weighting of CD-SEM data. The CD Cpk declines when the weighting of CD-SEM data is decreased. Nevertheless, the CD Cpk can kept at a certain level even the CD-SEM measurement sampling rate is less than 50% with the optimal CD-SEM data weighting of 0.3 or below.

7520-99, Poster Session

Determination of Gaussian beam and raster scan parameters in electron-beam-direct-write lithography considering device patterning and performance variability

H. Ng, C. Liu, H. Chen, K. Tsai, National Taiwan Univ. (Taiwan)

Low-energy electron beam lithography (LEEBL) is a promising patterning solution for the 22-nm half-pitch node and beyond due to its high resolution, low substrate damage, and increased resist sensitivities. In order to achieve throughout required for high-volume manufacturing, writing parameters such as probe size, pixel size, electron dosage, proximity correction scheme, and number of beams need to be carefully selected in a Gaussian-beam-raster-scan system. In high-throughput LEEBL, line edge roughness (LER) caused by shot noise becomes a critical issue for both device patterning and device performance variability. To characterize these effects, stochastic MOSFET gate patterning with LEEBL is constructed by overlapping energy distributions from an in-house electron scattering Monte Carlo simulation program with various writing parameters. Assoicated resist development profiles are based on Gaussaian functions for acid diffusion. Device performance variability such as I-V curve and noise margin variations of patterned devices with non-rectangular gates is predicted by incorporating a gate slicing technique and Predictive Technology Models. An iterative parameter optimization procedure is proposed to help provide initial guidelines and specifications for design and operation of multiple-electron-beam-direct-write systems.

7520-100, Poster Session

Study of photon-counting detection and imaging

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Photon-counting detection and imaging is a powerful tool for detection of weak intensities of light. A photon-counting detection and imaging experimental setup was designed and built in this study. Its structure and working principle are introduced in details. Weak photon irradiated on the avalanche photodiode (APD) which work on Geiger mode is collected by high speed data collection card continuously and processed with personal computer software. Finally, the photo-counting pulse image is acquired by this system. The expermental setup was useful tool for very faint luminescence detecting and imaging study.

7520-101, Poster Session

Evaluation of 172-nm wavelength as a possible candidate for 22 nm and below

J. You, E. Kim, H. Oh, Hanyang Univ. (Korea, Republic of)

The lithography industry has been working to extend 193 nm immersion with double patterning and complex computational lithographic techniques for 32 nm and below. Also extreme ultraviolet lithography (EUV) are used to make the 22 nm half-pitch and below. However, technical challenges remain to be addressed, as well as the high cost of the manufacturing tool. There was a report that a new wavelength, 172 or 175 nm, can be used for next generation lithography system. 172 nm lithography, although, has higher absorbance than 193 nm, it has much higher transmission than 157 nm in high refractive index liquid. Compared with 193 nm immersion lithography that has the resolution limit of 35.7 nm by using maximum numerical aperture (NA) of 1.35, 172 nm immersion lithography can be used for possible resolution limit of 27.4 nm by using maximum NA of 1.57. In this paper, we evaluated the 172 nm immersion lithography using commercial lithography simulation for 28 nm node by single exposure. We also checked the patterning possibility of 22 and 16 nm node by using 172 nm and double patterning because a totally new wavelength should show the possible extension to multiple generations.

7520-102, Poster Session

The effect of UPW quality on photolithography defect

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Photolithography resist process consists of priming, resist coating, post-apply bake, exposure, post-exposure bake develop, and post bake; advanced RETs and immersion photolithography has more critical resist process steps. Materials used in the resist process require the utmost in cleanliness, especially coating & develop process. In photolithography, De-Ionized Water (DIW) or Ultra Pure Water (UPW) is used during resist developing process as the pre-wet and rinsing material. UPW is supplied by a centralized auto supply system in a semiconductor fabrication; the UPW is controlled for temperature, pH, resistivity, TOC, ions, and etc.

State of the art semiconductor design continues to shrink; defect control becomes essential for high yields in semiconductor fabrication. In this paper, effect of UPW quality on resist process defect is revealed. Low resistivity DIW used in resist developing process generates residue defects, which created killing block etch defect after the subsequent etching process. Different measurements for DIW quality are demonstrated; water pH, conductivity, and Total Organic Carbon (TOC) in this case reflected the quality issue of UPW. Detail study on the residue defect and the cause-and-effect with UPW's quality is shown and discussed; the hypothesis is explained with experimental results. High quality UPW is required to eliminate the residue defect, hence minimal defective wafer is obtained. Additionally, optimized resist developing process to improve process robustness is also important.

7520-103, Poster Session

Controlled acetone vapor environment for the elimination of dry photoresist droplets in spray coating

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Photoresist deposition for lithography is difficult to perform on three-dimensional surfaces using the conventional spin coating method. In spin coating, the dynamic fluid effect and centrifugal force from spinning causes uneven distribution of the photoresist, particularly at the convex, edges and corners of the trenches. This results in undesirable thickness variation of the deposited photoresist. Spray coating is a replacement technique that eliminates this problem by producing micro-resist droplets that adhere firmly to the deposition location; thus, spray coating with optimal parameters

from designed experiment is a suitable method for photoresist deposition on structures with high aspect ratio. By using proper nitrogen flow rate to spread out AZ4999 resist to be micro-droplet in the same time with proper traveling nozzle speed, good resist coverage over all surfaces can perform. However, a drawback of spray coating is that a small amount of photoresist may prematurely dry, forming droplets on the even surface of the properly-deposited photoresist. Due to the added thickness from the droplets, the resulting air bearing surface (ABS pattern) contains localized defects/deformations. This work shows that these droplets can be easily removed by exposure to an acetone vapor environment. By utilizing a carefully controlled acetone environment chamber, the droplets are diluted with minimal effects on the thickness of the underlying photoresist layer. And also surface topography of resist was improved.

7520-106, Poster Session

Relaxation properties of dielectric dipoles of photo resist materials

H. Sasazaki, A. Kawai, Nagaoka University of Technology (Japan)

Relaxation properties of dielectric dipoles such as dielectric frequency dispersion, relaxation time, which should be optimized in structural material designing, are characterized. Relaxation times of dielectric dipoles of photo resist materials are characterized by Cole-Cole plot, which is employed to determine a dielectric relaxation time of dipole moment in polymer structure, based on traditional capacitance method in frequency range of 10mHz to 5MHz. The relaxation time of dry film resist (DFR) can be determined to be 12.1s. The validity of dielectric properties of DFR film as a structural material is discussed.

7520-107, Poster Session

Spontaneous deformation of resist micro pattern due to van der Waals interaction

A. Kawai, T. Yamaji, Nagaoka University of Technology (Japan)

Atomic force microscopy (AFM) is a versatile and powerful method that uses sharp tips to image, measure and manipulate matter at surface with atomic resolution. The van der Waals attractive force on a resist sheet was measured by the AFM system. The maximum value of the attractive force is about 180nN, which is enugh to deform the micro resist pattern spontaneously. The simple FEM model of the resist pattern was deformed by the van der Waals force at 180nN. This result enables to discuss the possibility of the pattern design in order to prevent the spontaneous deformation of resist micro pattern.

7520-108, Poster Session

Micro bubble removal from micro pattern structure under alternating electric field

H. Sasazaki, A. Kawai, Nagaoka University of Technology (Japan)

By the control of surface energy balance, it is well-known that micro bubbles can be trapped at a micro pattern structure formed by lithography. The removal and adhesion of micro bubbles from patterns can be controlled precisely. In this study, we confirmed that micro bubbles can move to a plus electrode applying direct electric field. In this regard, by applying alternating electric field to micro bubbles, we try to remove micro bubbles from micro pattern structure. Particularly, we focus on elastic property of micro bubbles under alternating electric field. This study will provide effective information to the application of electronic devices to liquid control technology.

7520-109, Poster Session

Computer-Aided-Design of two electrostatic lenses column by mixing dynamic programming and AI technique

F. A. Ali, Basra Univ. (Iraq)

This paper have shown a computer aided design (CAD) by using the optimization methods for the ion optical system developed, by mixing the dynamic programming procedure and artificial intelligence technique. CADION ANALYZER has been designed as an expert system, written in Java expert system shell (JESS) and Visual Basic .Net for optimizing and analyzing calculation processes for two electrostatic lenses column. By using such rule based engine, the optimized axial potential distributions for electrostatic fields undergo the constraints have been used in the two - lens optical column setup.

7520-110, Poster Session

Predictive model based pitch splitting

P. J. LaCour, A. D. Dave, D. Chou, A. V. Trichkov, Mentor Graphics Corp. (United States)

Double patterning is one of the main enabling technologies for expanding lithography beyond 45nm technology node. Geometric pitch split and litho friendly design is the core of double patterning. There has been lot of development recently in area of DP to minimize split errors and hot spots. In this paper we demonstrate one such application of predictive modeling to detect hot spots. The matrix for pitch splitting is developed at higher resolution wavelengths in design stage and the decomposed results are evaluated with different source types. This type of predictive model confronts hot spot information and un-resolvable pitches in design stage and assists in developing restricted design rules for litho friendly design.

7520-111, Poster Session

Design and characterization of 1.10m InGaAs-GaAs VECSEL

M. Nazari, Islamic Azad University,Varamin-Pishva Branch,Tehran (Iran, Islamic Republic of)

A comprehensive design method for an unconventional type of strained semiconductor quantum well lasers is applied to design multiple quantum well InGaAs-GaAs 1.050 m VECSEL for communication systems. The vertical external cavity surface emitting laser is a diode pumped solid state laser with a semiconductor quantum well gain medium, and it has become the focus of much attention in recent years. The method includes electromagnetic waveguide theory. The resulting laser has a 50 perpendicular far-field beam divergence.

An advanced structure of VECSEL laser diodes has been designed using the simulation software.Simulation results suggest that the thicknesses of layers should be changed in order to give low loss, narrow far-field divergence angle and high confinement factor.The aim of our study was two folds: (1) to provide the comprehensive analysis and calculations to design a VECSEL laser. In the simulations, the thicknesses of mirror layers, oxide layers and cavity layers are varied in order to observe variations of far-field divergence and the total confinement factor as functions of layer thicknesses. Comparison among loss, narrow far-field divergence and high confinement factor are made to optimize layer thicknesses,(2) the widths are designed to maintain single lateral mode and low loss .

7520-112, Poster Session

Durability of self-standing resist sheet composed with micro holes

A. Takano, A. Kawai, Nagaoka University of Technology (Japan)

MEMS (Micro Electro Mechanical systems) technology has been widely employed for micro device fabrication. Polymer materials, such as photoresist resin, have been focused as permanent structural materials used for MEMS. It is required that the permanent structural materials are durable to employ to micro device component. We demonstrate that the mechanical strength of self-standing resist film is enhanced by forming hexagonal hole array. The destruction strength of the resist film is analyzed by peel destruction test. As a result, the enhancement of the self-standing resist film with patterning can be obtained.

7520-113, Poster Session

PH control of water flowing in micro structure by local electrical field method

A. Takano, A. Kawai, Nagaoka University of Technology (Japan)

We have tried to control pH value of water by local electrolysis. In a macro system using a glass beaker and Al electrodes, the water pH can be changed from 7.3 to 8.6. We have fabricated a local pH control system constructed with a photoresist channel network and integrated electrodes. In this system, the electrodes are set locally at the micro network and are applied electrical field. It is effective to control the water pH in the micro channel network. We believe that this study can contribute to bio-electronics, medical and agriculture fields.

7520-114, Poster Session

Micro bubble condensation in micro channel controlled by local electrical field method

S. Ohata, A. Kawai, Nagaoka University of Technology (Japan)

Micro bubbles in several tens micrometer diameter can act as effective structural elements of micro devices. In this study, the micro device employing the bubble motion is developed. It has been experimentally revealed that bubble motion in micro channel is trapped at the channel branches. The local electrodes are set at a part of micro channel in order to control the bubble motion. Negatively charged bubble surface is received a certain force due to Coulomb's effect. This study will provide effective information to bioscience, medical science and agriculture engineering.

7520-115, Poster Session

In-situ monitoring and control of photoresist parameters during thermal processing in the lithography sequence

A. Tay, National Univ. of Singapore (Singapore)

The rapid transition to smaller microelectronic feature sizes involves the introduction of new lithography technologies, new photoresist materials, and tighter processes specifications. This transition has become increasingly difficult and costly. The application of advanced computational and control methodologies have seen increasing utilization in recent years to improve yields, throughput, and, in some cases, to enable the actual process to print smaller devices [1]. In this work, we demonstrate with the use of innovative technologies, control and signal processing techniques; and integrated metrology to improve the performance of the various photoresist processing steps in the lithography sequence.

We first demonstrate the integration of a single spectrometer to measure the photoresist thickness contour on the wafer during the spin-coating step or edge-bead removal step. We note that existing approaches in monitoring of photoresist thickness are for the cases of non-rotating wafers. Our proposed approach also does not require extra processing steps compared to off-line tools which require the wafer to be moved from the processing equipment to the metrology tool. The experimental results are compared with an off-line ellipsometer is less than 1% in terms of the worst-case error.

Next, any non-uniformity in resist thickness as well as the resist absorption coefficient can be compensated during the subsequent baking steps. Variation in photoresist extinction coefficient has a direct impact on the exposure dose required for exposing the substrate. An array of spectrometers is used to extract various photoresist properties such as resist thickness and absorption coefficient. Resist thickness and absorption coefficient may be estimated from the reflectance signals of a multi-wavelength spectrometer using a thin film optical model. When light is focused onto the resist film, phase difference between the incident and reflected light creates interference effects within the resist. The various resist parameters can then be extracted from the reflectance signals via optimization algorithms. In-situ measurement of wafer temperature is achieved using proximity pins with embedded temperature sensors which the wafer sits on. In-situ estimation of wafer temperature can also be achieved by monitoring the bake-plate temperature profiles and system identification techniques [2]. The wafer temperature and photoresist parameters can thus be controlled in real-time. Figure 1 shows the experimental setup for the proposed integrated system. Detailed modeling, analysis based on first principle heat transfer principles and experimental implementation demonstrate the feasibility of the proposed approach.

References

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7520-116, Poster Session

Improving 1D optical proximity effect matching for 45nm node by scatterometry metrology

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The optical proximity effect (OPE), the feature distortion due to the location of its neighbors, is one of the major concerns of today's lithography process engineers. The fingerprint of the OPE is required to develop an optical proximity correction (OPC) model for each process node. Typically the OPC model is developed based on experimental information on one specific scanner. The OPC model should work equally well on other scanners of the same type (here two TWINSCAN XT:1700i scanners) and on other tool types. However, small differences in optical and mechanical scanner properties, e.g. the illumination pupil, can lead to a different critical dimension (CD) characteristic for a given OPC model. In a fab with a population of scanners it is beneficial for optimum scanner utilization, productivity, and costs to match the OPE of this population. To optimize this match, we use a technique employing the methodology of the ASML/BRION "Pattern Matcher basic" imaging product. This product is designed to improve the OPE match based on measured "on-product" structures or structures on a test reticle.

For feedback of the printed CD, a fast and accurate metrology tool is needed. The solution is found in scatterometry metrology as it offers an improved metrology throughput as well as improved repeatability compared to CD-SEM. For the dense pitches we find a typical repeatability of 0.2nm for the scatterometer. The method additionally delivers stack parameters describing the cross-section of printed features (e.g. resist thickness, BARC height, Side Wall Angle (SWA)). The linear variation of the SWA with focus in a wide range allows monitoring this parameter. Scatterometry enables faster feed-back of these parameters due to measurement times of typically 1-2 sec/feature compared to 3-4 sec/feature for the CD-SEM. This

is especially advantageous when a large number of different features e.g. 1-dimensional line/spaces thru pitch are used to characterize the OPE of the lithography tool.

For OPE matching the adjustable scanner parameters investigated here are dose, focus scan range, NA, and _ringwidth, _center of the illumination pupil. The sensitivity of the CD, for these adjustable scanner parameters is determined by exposing wafers with a test reticle. It contains a wide range of 1D test structures that can be selected to resemble typical structures on products. This is followed by CD-SEM and scatterometry measurements of the resist patterns.

We show that the sensitivities and the effect of scanner tuning can be described more accurately by scatterometry measurements using an identical number of printed features as for CD-SEM metrology. This can be used to further reduce the number of measured features and by that reduce the scatterometry metrology time. The RMS deviation between the measured and the predicted tuning effect determined by scatterometry is smaller than for CD-SEM allowing setting tighter matching targets.

The RMS of the mismatch between the scanners is reduced by optimizing the setting of the adjustable scanner parameters using the sensitivities determined previously. Scatterometry and SEM metrology lead to similar scanner adjustments. Due to the reduction of the metrology contribution the residual RMS mismatch is 0.2nm for the thru pitch curves measured by scatterometry versus 0.4nm for the CD-SEM as shown in the figure.

7520-117, Poster Session

Novel assist feature design to improve depth of focus in low k1 EUV lithography

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With the expected continued progress of microelectronics scaling, low k1 lithography may be required even with EUV lithography. One of important techniques of low k1 lithography, the off axis illumination (OAI) in combination with sub-resolution assist features (SRAF) on reticles has been used extensively in optical lithography. Use of assist features combined with off axis illumination typically requires extremely small pattern sizes.

In a low k1 region of around 0.4, assist features will help DOF of isolated and semi-isolated lines. Since EUVL process operates at a relatively higher k1 value than that for the optical lithography, the assist feature size needed is relatively smaller. In addition, with the mask shadowing effect of EUVL, all horizontal lines should be biased thinner by several nano-meters, and similarly horizontal assist features will need to do the same. Fabricating such narrow features on masks is a mask fabrication challenge, and could potnetially limit the application of SRAF in EUVL when applying EUVL at low k1.

A novel approach in creating assist features with similar widths as the main critical dimension features has been identified and will be presented in this paper. This approach uses the technique of controlled reflectance of the mask rather than feature size reduction to achieve SRAF printing. As a result, the mask making could be easier, thus enabling a future low k1 of EUVL .

7520-118, Poster Session

Performance of our recently delivered EUV resist outgassing and reticle contamination tool model number EUV-RER1314

J. H. Underwood, D. C. Houser, A. T. Latzke, R. C. C. Perera, EUV Technology (United States)

One of the principal challenges in the ongoing EUVL research effort is the development of a suitable EUV-sensitive resist. In addition to high sensitivity, there is stringent limit to the amount of contaminants that the resist can outgas during wafer exposure. We have successfully developed a EUV Resist Outgassing and Reticle Contamination Tool to evaluate the candidate EUV resists. The 13.5 nm light is collected and deliver 60 mW/cm*2 to a small spot on a 300mm diameter wafer coated with the resist. The wafer is loaded onto an x-y stage in the exposure chamber through a load lock. By translating the wafer the complete wafer can be exposed and the evolved gases measured with a residual gas analyzer (RGA). At the same time a part of the focused beam is split off and focused on a witness sample that can be removed to evaluate the degradation of the optics. Finally, the combination of the x-y wafer motion with a shutter to control exposure times allows the experimenter to obtain “dose snake” and thereby to measure the “dose-to-clear” of a candidate resist. Performance of our commercially available resist outgassing tool that has been fully operational for about 9 months with very good up time will be presented.

7520-119, Poster Session

Dissolved gas quantification and bubble formation in liquid chemical dispense

G. Tom, W. Liu, ATMI, Inc. (United States)

Gas dissolved in liquids such as photoresist comes out of solution as bubbles after the liquid experiences a pressure drop in a dispense train and may cause on-wafer defects. Reservoirs in the dispense train can assist in removing bubbles but are incapable of removing dissolved gas. This study demonstrates the importance of maintaining the amount of dissolved gas in a liquid below a critical value to reduce bubbles generated after a pressure drop in the dispense train occurs. The methodology to quantify dissolved gas during liquid dispense cycle using gas chromatography is discussed. The amount of dissolved gas is correlated to the amount of bubbles downstream of a pressure drop. This study also analyzes sources of bubbles in the dispense train and techniques to mediate the sources.

7520-24, Session 6

EUV lithography development progress at IMEC

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EUV lithography is currently the leading candidate for future device manufacturing nodes. Recently its feasibility to produce 22nm node devices was shown, and pre-production tools are expected to be delivered in 2010. With the ASML EUV alpha demo tool (ADT), IMEC is studying the critical issues in various areas of the development of EUV lithography such as resists, optics contamination, reticle defectivity, imaging, exposure tool and device integration. This paper will give an overview of the development progress in all of these areas and the remaining challenges towards a mature technology for volume manufacturing will be highlighted.

7520-25, Session 6

High brightness NGL multiplexed EUV light source for EUV interferometer, metrology and inspection

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The top challenges to EUVL deployment of extreme ultra-violet lithography (EUVL) at 13.5 nm wavelength are the availability of a powerful and reliable light source in 2% bandwidth around 13.5nm spectral wavelength and the associated optics to collect the EUV photons, the so called SoCoMo (source

collector module). To support pilot line operation and EUVL transition into manufacturing, a commercial EUV aerial imaging microscope (AIM) will be required for patterned mask defect review. The EUV source for the AIM tool is very different compared with the HVM Litho source with substantially higher brightness, higher irradiance (power density) and much smaller etendue to match the projection magnification and illumination field size. The self-absorption and etendue constraints limit the usable power of a conventional single unit EUV source. The detailed parametric scans show that a single source unit cannot meet the requirements of the Litho tool with high efficiency and is not sufficient for critical metrology applications, given the limiting etendue of the optics. Previous papers have identified that the required irradiance can be achieved by spatial multiplexing, using multiple sources. For a fixed resulting etendue, the EUV power from optimal plasma of a multiplexed source (re-packing radiators from single into multiple separated micro volumes) is shown to increase with the number of units.

NANO-UV is delivering a new generation of EUV light source with an intrinsic photon collector, the i-SoCoMo concept, where an impulse micro discharge plasma source is integrated to a photon collector based on an active plasma structure. Extensive numerical modeling has been carried out to address fundamental issues in EUV plasma sources and to optimize the performance of the source. The plasma parameters providing high in-band emission for minimum energy input are in a very narrow range of values. Detailed parametric scans have provided basic numbers to select the optimal regime for tin and xenon based source operation. In particular, it has been found that highly ionized xenon plasma in the presence of fast electrons demonstrates a unique feature that has not been identified previously. The in-band emission near 13.5 nm from Xe XX and Xe XXII ions produced in the plasma by fast electrons may exceed that one from Xe XI ions of conventional xenon based EUV source. We present here experimental results from CYCLOPS , a commercial unit incorporating the i-SoCoMo technology. This source is based on a nanosecond, ultra fast micro-plasma capillary discharge with an in-built plasma structure (PlasmaLens) for photon collection and projection. The micro-plasma pulsed discharge and PlasmaLens structure are induced by an intense electron beam generated due to the transient hollow cathode effect. At the same time the beam fast electrons shift the ionization equilibrium to higher ionization degrees providing higher in-band emission intensity. The CYCLOPS source, working at multi-kHz regime in a mixture of He:Ar:Xe, possesses exceptional brightness without the use of external physical optics, and delivers more than 1016 photons/cm2/s to a mm2 spot over 60 cm away from the source at the EUV band, with an etendue below 10-4 mm2.sr. It is proposed that such a source could form the basic building block for an ideal EUV metrology source. The special coherence of the source allows the EUV interferometer for metrology and for resist inspection to be made.

Higher irradiance for aereal imaging requirements can be obtained by spatial and temporal multiplexing of multiple sources, due to the very low etendue and compact form factor of each i-SoCoMo unit. Characteristics of the CYCLOPS source used for metrology purposes are presented together with early experiences of operating 12 separate sources in a multiplexed configuration, the HYDRA(TM)-12 design.

7520-26, Session 6

Chromophore-less photoacid generator for EUV resists

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Recent advances in EUVL lithography is mainly centered on improving the RLS trade-off by employing new resist platforms, bulkier photo-acid generators (PAGs), EUV sensitizers etc. Among the several new kinds of PAGs proposed till date, the focus of development was mainly on the acid strength, compatibility with resin etc., whilst always retaining the mono, Di or tri phenyl chromophore of the PAG. Tagawa et al proposed that in the case of EUVL resists, PAGs are mainly activated by multiple secondary electrons generated by scattering of EUV photon by resist elements. [1-3] Therefore, the role played by traditional chromophore in mono-, di- or tri-phenyl groups in the PAG is in principle redundant for use in EUVL resist. Additionally, the poor resist performance related to shelf-life, post-coating delay and post-exposure delays is directly related with the photosensitivity of the chromophore in the PAG. Also, phase-segregation of PAG, an inherent measure of incompatibility with resin is also due to the structure of PAG. Therefore, from the above perspective and other reasons, chromophore-less PAG is highly desirable. Herein we report on the use of chromophore-less PAG for the patterning of EUVL resists. Resist performance using model acrylate and PHS based resist was studied. Resist contrast for each resist formulation was measured. The patterned resists were characterized using SEM. Thermal stability of the PAG was compared with model chromophore containing PAG.

7520-27, Session 6

Utilizing model-based optical proximity correction to compensate for EUV shadowing effects with improved pattern transfer fidelity and process windows

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Extreme ultraviolet (EUV) lithography is one of the promising candidates for device manufacturing with features smaller than 22 nm. Unlike traditional optical projection systems, EUV light needs to rely on reflective optics and masks with an oblique incidence of 6 for image formation in photoresist. The consequence of using a reflective projection system can result in horizontal-vertical (H-V) bias and pattern shift, which are generally referred as shadowing. Approaches proposed to mitigate this effect include changing mask topography, modifying aberrations in projection system, and biasing features along the azimuth angle, which are all rule-based. Our study shows that this effect can be substantially compensated by model-based optical proximity correction (OPC). This study investigates performance characteristics on the integration of in-house OPC algorithms and rigorous topography simulation, with and without the initial conditions of shadow compensation. OPC not only increases pattern transfer fidelity but also improves process windows significantly. Our results are more robust than the traditional shadow compensation techniques, in terms of geometric printability under process variations.

7520-28, Session 6

Comparison of simulation and wafer results for shadowing and flare effect on EUV alpha demo tool

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The move to reduction in geometries, while allowing higher performance, is driving semiconductor lithography industries to its limit. Up to 40nm nodes, current lithography method (immersion) satisfied patterning performance required to produce high performance, compact semiconductor device. Due to patterning limitation of current method, sub 40nm device require breakthrough in lithography technology. But “Sub 40nm wall” is crumbling even faster than predicted as double patterning technology and spacer patterning technology begin to emerge from many of the industries top research centers. But due to limitation set by current lithography tool, “The wall” might not crumble enough. There for EUVL(Extreme Ultra Violet Lithography) is emerging as the key enabler in preceding the current lithography method and many successful result have been reported from industries top research centers. EUVL development is premature for high production and one of the major issues introduced by development of EUVL is high level of flare and shadowing introduced by the system. Our previous paper showed that effect of shadowing and flare degrades the aerial images and introduce unbalanced Critical Dimension Uniformity(CDU). Therefore flare and shadowing correction is very crucial and prior to correction, prediction of shadowing and flare effect is inevitable in order to acquire high resolution wafer result in EUVL technology.

In this study, in order to accurately predict the shadowing and flare effect of EUVL, we compared and analyzed the wafer and simulation result of the shadowing and flare effect of the EUV alpha demo tool at IMEC. Flare

distribution of the EUV Alpha Demo tool was measured and was used in simulation tool to simulate several test case wafer result. Also, shadowing effect of the in-house created mask was measured and compared with simulation result to match the predictability of the simulation tool. Wafer result to simulation showed errRMS range within 3nm from 3 flare test environment and 2nm for shadowing test environment. Using the wafer and simulation result, correction method of both flare and shadowing effect will be discussed.

7520-10, Session 7

Source mask optimization (SMO) at full chip scale using inverse lithography technology (ILT) based on level set methods

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For semiconductor manufacturers moving toward advanced technology nodes -32nm, 22nm and below - lithography presents the greatest challenge, because it is fundamentally constrained by basic principles of optical physics. For years, source optimization and mask pattern correction have been conducted as two separate RET steps. For source optimization, the source was optimized based on fixed mask patterns; in other words, OPC and SRAFs were not considered in source optimization. Recently many different approaches of Source Mask Optimization (SMO) were developed for the lithography development stage. The next important step would be extending SMO, in particularly, the mask optimization in SMO, into full chip.

The Level Set Method, invented by Professor Stan Osher (Luminescent's co-founder) and James Sethian in 1980s, has been applied in many engineering fields, and is regarded as one of the most efficient mathematical methods for solving problems involving dynamic change of 2D patterns with topology changes. Level Set Method based Inverse Lithography Technology (ILT) was developed by Luminescent Technoliges, Inc. about 6 years ago to address the mask optimization efficiency and complexity. Now the same mathematical framework is applied to source optimization and source mask optimization. With this the consistent result and performance are guaranteed between the SMO in lithography development stage and full chip mask optimization in the OPC stage.

The enabling technology in Level Set Method based ILT is the level set representation of the design, mask, wafer patterns and scanner source. Representing the 2D design pattern, mask pattern, and wafer pattern by level sets is the most mathematically efficient way to represent 2D patterns, and gives the mask pattern practically infinite degree of freedom to change shapes during optimization (i.e., mask pattern OPC). It also solves the discontinuity problem in the mathematical formation when Sub-Resolution Assist Features (SRAF) are added into the mask patterns to enable printing of wafer patterns with better CD uniformity and larger process margin. Representing the scanner source as level set enables a free-form and gray scale representation of the scanner source, and enables the source to change shape, size, and even topologies during the optimization. Another huge benefit of level set representation is that it provides a mathematical closed form expression for the derivative of the function, which significantly improves the speed of any optimization by obviating numerical gradient calculation.

In this paper a number of memory and logic device results at the 32nm node and below are presented which demonstrate the benefits of this level set method based SMO and its extendibility to full chip designs.

7520-29, Session 7

Development of hybrid MRC with new MRC parameter for the aggressive assist feature generation and ILT

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The 1st one is obviously shown in figure 1 that the MBAF generation was limited by MRC. [1][2] Figure 1(a) shows the MBAF result for different MRC conditions and the aggressiveness is very dependent on MRC. It is also shown that the depth of focus gets worse as larger MRC was applied in figure 1(b) and (c). In this article, firstly, we have been concerned about the coverage of the current baseline MRC constraints. We represent the experimental result to find the optimal value of the new MRC parameter for several types of mask and suggest the area as New MRC constraint that can better reflect the characteristics of the mask process than general baseline MRC as shown in figure 2. Furthermore, we have shown that the aggressiveness of the mask optimization and process window can be improved by comparison between the ILT result with baseline MRC and new MRC.

The 2nd issue is the mask proximity effect on not only the assist feature but also the main feature. For the 3X nm node DRAM and FLASH device, when the minimum feature size of the OPC result of the main feature gets almost close to MRC limitation, even confirmed by MRC, the mask proximity effect is very critical and significant to the wafer result. It means that the above limitation was too loose for the main feature to be in the tolerance. Therefore, we have studied on the effect of the mask CD variation for both of the assist and main feature by making the test mask for the 3X nm node DRAM contact layers. We found out the fact that the assist feature is about two times more tolerant of the mask CD variation than the main feature. It is shown in figure 3 that the mask CD tolerance of the assist feature should be within about ±10% when the upper and lower limitation of the main feature's wafer CD variation is ±3%. In this paper, therefore, we suggest the hybrid MRC that the size of the main feature and assist feature is respectively restricted by different MRC limitation. We have evaluated the new and baseline MRC limitation for each tolerance as above with consideration of mask CD tolerance and the mask inspection.

By the use of the hybrid MRC with new MRC parameter, we can optimize the mask more aggressively and improve process window. Now we are trying to implement these MRC scheme into the current OPC, MRC engine and the mask data processing tools. After that, the flexible MRC correction in the OPC may be possible and we can achieve the more optimized mask result.

7520-59, Session 7

Fast converging inverse lithography algorithm incorporating pixel inversion and image gradient descent methods

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Semiconductor fabrication is the cornerstone of the current IC (Integrated Circuit) industry. With advances in microlithography now pushing towards nano-scale features, the problem of how to print circuit layouts on wafers has become more intricate and convoluted. Optical Proximity Correction (OPC) is a resolution enhancement technique that modifies layout designs in order to minimize their distortion when transferred to silicon. A good OPC implementation may prove sufficient for a given process technology, precluding the need for a more expensive alternative, like Double Patterning, Alternating Phase Shift Mask (AltPSM), Immersion Lithography and so on. Evidently, OPC has clear advantages in efficiency and manufacturing cost.

Segment-based OPC has been the general industry approach and has proven successful through many CMOS generations. Because it only modifies existing edges in the layout, segment-based OPC has the advantage of being easy to implement, particularly in iterative algorithms. However, as the Critical Dimension (CD) becomes ever smaller, this type edge-only compensation is not expressive enough to exploit the full range of possible mask corrections. Therefore, Inverse Lithography Technology (ILT) has been proposed as an alternative due to its more relaxed constraints and full-mask approach. However, ILT is faced with several problems, including bad convergence and the existence of local minima. To get rid of these issues, many approaches have been proposed, like pixel-flipping, gradient strategies and so on. Still, ILT needs to be further developed to become the next-generation OPC.

In this paper, we propose an ILT algorithm that employs a gradient descent method to improve convergence and reduce the Edge Placement Error (EPE). Figures 1 and 2 below exemplify the usage models of our approach. If the features are large enough, like the 200nm via in Fig. 1, the corrected mask can be calculated directly by our descent method. However, for smaller

features, like the 100nm via in Fig. 2, an initial approximation is needed for the descent method to quickly converge to the desired solution. In order to obtain the initial guess, we use the pixel-inversion ILT algorithm that we presented in [1-2]. The main advantage of this combined approach is that the pixel-inversion algorithm does not need to be fine-tuned; as can be seen in Fig. 2(b) a rough approximation is sufficient for our descent method to further enhance the correction and minimize the EPE. The end result is a more automated approach that can be used in a wider variety of layouts.

7520-61, Session 7

Using transmission line theory to calculate equivalent refractive index of EUV mask multilayer structures for efficient scattering simulation by finite-difference time-domain method

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The Finite-Difference Time-Domain (FDTD) method is used to study scattering effects of EUV mask. It requires a significant amount of memory and computation time since a very fine grid size is needed for simulation in multilayer structures. We use transmission line theory to calculate equivalent refraction indexes for EUV mask multilayer, to approximate the multilayer as one layer of bulk artificial material. The reflectivities for the small-angle incidence EUV light in the bulk artificial material and EUV mask multilayer are calculated by FDTD method, and the results show good comparison. The ideal Fresnel's equation is used to evaluate the numerical errors for FDTD method in these cases. Using the equivalent refractive index artificial material for EUV mask multilayer can reduce the memory usage and computation cost in FDTD method with tolerable numerical errors, and this method can accelerate the simulation for EUV mask design.

7520-33, Session 8

Performance of a programmable illuminator for generation of freeform sources on high NA immersion systems

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Besides wavelength of the radiation and Numerical Aperture (NA) of the projection lens, the illumination source shape is one of the most important resolution enabling tools for the lithographer. After the introduction of off-axis illumination in the nineties and the more recent introduction of polarized illumination, freeform illumination is the next step in illumination technology.

Freeform sources can increase the process window for complex structures in combination with an optimized mask. The drive to print closer to the theoretical limit of k1 = 0.25 increases the pressure on tool builders to deliver these freeform sources. Lower k1 makes lithography more complex putting more pressure on the development time of a new process to still deliver the new products in time. This requires quick access to new source shapes for both development tools and production tools.

Source tuning is also a powerful knob to match the proximity effect of a litho tool to that of a reference tool used to determine the proximity correction on the reticles. This tuning can turn a simple annular into a freeform source.

In this paper the principle and performance of a fully programmable illuminator for a high NA immersion system is described. Sources can be generated on demand, by manipulating an array of mirrors in stead of the traditional way of inserting optical elements and changing lens positions.

Measured sources generated with this new type of illumination system will be shown and compared to the target sources generated by source mask optimization software. Comparison between measured and target source will be done both in parameters of a pupil fit model and by simulated imaging impact.

7520-34, Session 8

Latest results from the Nikon NSR-S620 double patterning immersion scanner

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Immersion lithography is now well established as the leading edge technology for 40-45 nm device volume manufacturing. An extension of immersion, double patterning (DP), is the leading contender for manufacturing of 32 nm devices. For DP, substantial improvement in overlay accuracy is required to meet the CDU requirements for the 32 nm node, and substantial increase in throughput is required to meet the cost requirements. To meet these challenges, Nikon introduced the NSR-S620. The S620 incorporates Local Fill Technology and the Tandem Stage from the existing, single exposure immersion tool, and also includes new technology to improve throughput and overlay accuracy. This presentation will discuss these technological improvements and show the latest technical results.

One of the innovations of the platform is a new method of wafer alignment and surface mapping called Stream Alignment (Fig. 1). Stream Alignment is enabled by a new multiple-point alignment system using microscopes and a wide auto focus mapping system comprising multiple sensors. With this method, the time between the end of one exposure and the beginning of the next is reduced to about one third of the previous model, the NSR-S610C. Accuracy is improved because many more alignment points are available.

In addition, higher acceleration and faster scan velocity of the wafer and reticle stages of the platform also increase throughput. These throughput improvements are realized by optimal vibration dynamics design, advanced Local Fill Nozzle, and advanced control techniques. The S620 main body, including the projection lens, is isolated using Skyhook Technology, first introduced on the NSR-SF150 and SF155 i-line steppers, and the proven, low-vibration reticle stage is now mechanically isolated from the main body. This vibration free platform maximizes the imaging performance of the projection lens. Advanced control techniques are used to improve synchronization performance at high speed scan. The synchronization accuracy during scanning will be presented to show the vibration level. In addition, we will also show the immersion performance at the maximum scan velocity.

Another innovation is a new hybrid metrology system called Bird's Eye Control (Fig. 2). This solution addresses the well known interferometer measurement error caused by air fluctuation, which has been the dominant error factor in the overlay budget. This metrology system uses added encoders which are not disturbed by the air fluctuations. S620 provides higher throughput with better accuracy with the new alignment technology and control technique described above, while overcoming the issue of air fluctuations faced by the current model.

With these improvements, the S620 can address the overlay and throughput requirements of double patterning.

7520-35, Session 8

Focus budget breakdown of 4x nm DRAM process in volume manufacturing

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Although hyper NA immersion tools have been successful in providing tighter CD control and larger process margins than dry tools, state-of-the-art device with lower k1 value requires much tighter process margin. Even with 1.35 NA immersion tools, some critical layers are showing actual DOF (Depth of Focus) range less than 100nm. It means that both tool performance and layer-specific processes should be controlled and maintained much tighter

in volume manufacturing.

In this work, focus budget breakdown will be addressed for two critical layers of 4x nm DRAM process using 1.35 NA immersion tools (ASML 1900i). The objective is to determine contributions of all possible factors to total focus variation, and then to find methods to improve the on-product focus controllability in terms of both tool and process. The bottom-up analysis method is used to determine total focus variation, where all tests are correspond directly with each budget contributor and can be summed up to determine total focus variation.

Focus contributors can be divided into two categories; machine-dependent factors and process-dependent terms. Machine-dependent factors are directly related to the focus controllability of a immersion scanner itself, and include projection optics, reticle control, setup accuracy, and focus uniformity. Process-dependent factors are related to various process conditions, and include reticle and wafer flatness, product topography, product design, illumination modes and FEM accuracy.

The statistical sum of all factors can be compared to the DOF requirements for each layer, and key budget contributors can be determined. Some improvements will be implemented and verified on the product level.

7520-36, Session 8

Mueller matrix polarimetry for immersion lithography tools with a polarization monitoring system at the wafer plane

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It will be required for more accurate lithography simulation of complicated mask patterns then ever, under hyper-NA (numerical aperture) projection lens and aggressive small-aperture polarized-light illumination, to construct two systems of polarimetry; one is polarimetry for illumination, and the other is Mueller matrix polarimetry for projection lenses. The former polarimetry already reported by the authors is necessary for us to appreciate what the true polarization state of illumination is. The polarimeter mask described in the report can determine the Stokes parameters of illumination. On the other hand, the main subject of this paper is the latter polarimetry. Mueller matrix is the translation matrix of the input Stokes parameters to the output Stokes parameters. With the full elements in the Mueller matrix of a projection lens, the Stokes parameters of a light at the wafer plane can be easily and accurately predicted from the Stokes parameters of every illumination condition. The dual rotating-retarder polarimetry has been used for determining a full Mueller matirix of a sample for many years. However, this method cannot be entirely carried out for lithography tools. This paper proposed a new method of Mueller matrix polarimetry and a monitor mask used for 193-nm immersion lithography tools with a polarization monitor at the wafer plane.

7520-37, Session 8

Flexible 60-90W ArF light source for double patterning immersion lithography in high volume manufacturing

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As ArF immersion lithography is extended to meet the demands of 32nm and below, the requirements from the light source have become progressively more stringent, in the areas of performance and operating cost. The ability to extend deep ultraviolet (DUV) lithography into the 32 and sub-32nm domain has more recently relied on improvements in source-mask optimization (SMO), double patterning (DP) and complex, pixellated illumination patterns. The scanner light source has been driven to more stable optical performance (energy, wavelength and bandwidth) as well as improved beam stability (pointing, divergence, symmetry and polarization) for these resolution enhancement technologies (RET) to be successful. Additionally, some of the aforementioned technologies can be further optimized with a flexible light source that is able to produce varying power levels to suit the specific application or layer in a cost-effective manner. In the area of operating costs, DP lithography has introduced a significant cost penalty in pursuing 32 and sub-32nm patterns, as those critical layers impose a significant throughput impact for the litho cell. Scanner designers have pushed on all fronts to enhance throughput, including stage speed increases and scan slit window reductions that demand increased power levels from the light source. In this paper, we will discuss how the latest-generation lithography light source from Cymer, the XLR 600ix (announced in February 2009), has addressed these performance constraints while driving the operating costs down over time. Historically, the light source was limited to a narrow range of operating power, while improvements in optical performance were extracted. This led to the use of filters on the scanner to modulate light source power as needed, effectively 'throwing away' light. The wide power range of the XLR 600ix, from 60 to 90W, enables optimum power selection without waste. At the same time, significant performance improvements have been introduced on the XLR 600ix that reduce dose, wavelength and bandwidth variability, using sophisticated controls systems, enabling improved CD uniformity and depth of focus control, while operating at higher scanner throughputs. The XLR 600ix includes technological improvements to extend parts lifetime and reliability, as well as operational improvements that deliver predictable costs via the OnPulse program. This paper will illustrate extremely stable light source performance over extended life in the areas of dose, wavelength, bandwidth and beam stability while operating at a high power, 90W regime. Some of the challenges that have been overcome to deliver this capability will be presented, such as advances in optical materials and coatings for improved lifetime and beam stability characteristics.

7520-38, Session 9

Mask defect specification in the spacer patterning process by using a fail-bit-map analysis

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The spacer patterning process is one of the strongest candidate double-pattering technologies (DPT) for fabricating semiconductor devices using ultra-low-k1 lithography. For device fabrication, defect control of the mask is important. We already showed that the mask defect printability to the wafer in the spacer process was different from that in the conventional single-patterning process, and that the acceptable mask defect size for the spacer patterning process was considered to be relaxed (55-60nm) from that for the single patterning process (< 40nm) [1]. In the above study, the acceptable mask defect size was estimated only from the wafer defect size, however, the acceptable size was not verified by checking the device performance.

In this study, the acceptable mask defect size in the spacer patterning process was investigated using a gate-level device mask that contains several programmed defects at the cell. The device performance was investigated using a fail-bit-map analysis [2]. The defects are of several sizes and of two types, namely, opaque and clear. Firstly, the exposure and development of the wafers were performed using the above-mentioned mask, an immersion type ArF scanner, and a conventional resist process, i.e., the sequence of a resist / a bottom anti-reflective coating / a hard mask. After the development, the hard mask was etched off. After the etching, the spacer pattern was fabricated. Finally, by using the spacer pattern as an etching mask, the gate pattern was fabricated. The printability of the mask defect to the wafer was investigated using a CD-SEM after the development and after the gate fabrication. The device performance was investigated using the fail-bit-map analysis of the cells which contained the programmed defects.

The SEM measurements showed that the mask defects were transferred to the gate pattern for both opaque and clear defects. When the defect size was small, the bit cell (which contained the programmed defect) worked correctly. However, when the defect size was large, the bit cell fails. The probability of the fail of the cells increased as increasing the defect size. The acceptable mask defect size will be discussed from the fail probability.

[1] S. Miyoshi et al., Proc. SPIE 7122 (2008) p.71220P 1-8.

[2] S. Yamaguchi et al., Proc. SPIE 4889 (2002) p.826-835.

7520-39, Session 9

Analyzing electrostatic induced damage risk to reticles with an in-situ e-reticle system

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Electrostatic induced damage from electric field migration of chrome (EFM) and electrostatic discharge (ESD) has become a growing concern among reticle makers and end-users. Electrostatic induced damage to reticles has been observed across the many environments to which a reticle is subjected, from reticle manufacturing, shipping and handling, to inspection, storage and UV-exposures. It has been estimated that about half of the reticles sent for repair have some form of electrostatic induced damages [SPIE Advanced Lithography, 28 Feb 2008, Ref 6922-73]. The yield loss due to such defects on reticles is likely quite considerable. With the industry moving towards ever smaller technology nodes, the impact from such defects is expected to continue to grow. However, engineers are still blind as to where and when the damage may happen. This is largely due to the lack of an in-situ electrostatic measurement system which “sees” and “interacts with” the external electric field as a real reticle does. Sebald [Proc. SPIE Vol. 7122] introduced the E-Reticle system, a test device, which has electrostatic field sensors, a data storage component and a real time clock, all embedded within a conventional six inch quartz reticle. The chrome side of the E-Reticle has one guard ring and 4 square chrome pads. These five chrome segments are insulated from each other by the quartz glass. Under each pad, inside the reticle housing, there is a fast-response voltage sensor, which senses the potential difference between the guard ring and the pad. The measured data are time-stamped and stored in a flash memory unit in the reticle. The collected data can be wirelessly downloaded from the E-Reticle to a computer and analyzed with the Data Analysis software. The event synchronization function in the analysis software can match the events / operations in a text-based machine event log with the collected data, enabling a detailed electrostatic risk analysis against time and location. This function will enable engineers to accurately locate when and where electrostatic induced damage may happen. This paper first presents a new version of the E-Reticle with the capability of working both in a mask manufacturing environment and in a scanner litho-system. It is equipped with the scanner alignment marks for Canon, Nikon and ASML. The paper then investigates the electric field conditions in a variety of processes and environments. The E-Reticle was used to assess the damage risks in cold DI water rinse / spin dry in a mask cleaning system. Test results indicate that a reticle may see electric potential difference increase when cold DI rinse starts. Spin dry ramp may also cause the accumulation of electric potential difference. The system was also utilized to examine the influence of UV exposures on a reticle in a UV cleaning process. Electric potential readings show that UV exposures can raise the potential differences between separated chrome patterns, hence increasing the probability of electrostatic induced damage from the EFM defect mechanism. Finite element modeling was employed to understand the electric field distribution and field strength at points of interest.

7520-40, Session 9

In-die actinic metrology on photomasks for low k1 lithography

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New lithography techniques like Double Patterning, Computational Lithography and Source Mask Optimization will be used to drive immersion lithography at 193nm to its limits. The photomask will become more and more a critical optical element in the scanner beam path. Precise image transfer of the circuit features into the resist will be key for the mask manufacture and its qualification. The extremely high MEEF values in low k1 lithography dramatically amplify small process variations on the mask features to the wafer print. Complex mask features using sophisticated OPC and assist features require mask metrology under scanner conditions which measures the optical performance of the mask. Double patterning technology tightens the registration and CDU specification of the patterns at the same time. Especially, overlay becomes more and more critical and must be ensured on every die. In-die registration and CD metrology on arbitrary features at scanner wavelength can measure the mask performance precisely and ensure correct print results and high yield in the wafer fab. Moreover even a complete set of phase shift measurements, CD and registration measurements in the die features can help to ensure that mask manufacture and its qualification provide indeed the largest process window for wafer printing. It is key for higher yield and better performance.

In this paper an overview about several actinic in-die metrology techniques will be given. Focus will be on application of in-die CD measurements using the Zeiss WLCD tool as well as in-die registration measurements using the Zeiss Prove tool will be shown and discussed.

7520-41, Session 9

Revisiting adoption of high-transmission PSM: pros, cons and path forward

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High transmission attenuated phase shift masks (HTPSM) have been successfully applied in volume manufacturing for certain memory devices1. Moreover, numerous studies have shown the potential benefits of HTPSM for specific lithography applications2, 3. In this paper, the potential for extending HTPSM to other applications, such logic and analog devices, is revisited with emphasis on understanding manufacturing versus performance tradeoffs as compared to other mask based resolution enhancement approaches. Since the successful implementation of HTPSM depends heavily on illumination source layout and optical proximity correction, simple comparisons using regular line space patterns are shown to be inadequate for understanding the benefits of HTPSM usage. By considering mask and exposure system variations, such as focus/dose, mask critical dimension, phase, and transmission, the overall process window can be enhanced when HTPSM is combined with optimized OPC and source illumination. Therefore, HTPSM may be a viable and lower cost alternative to other complex RET approaches. For immersion lithography, HTPSM may minimize the impact from mask topography if the HTPSM absorber layer thickness is less than the thickness of traditional 6% PSM. Toward this, we review blank options for HTPSM that can minimize scattering effects in high NA lithography.

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7520-42, Session 9

Back side photomask haze revisited

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Back side haze on photomasks has been previously reported and continues to present problems in many fabs throughout the industry. While some process changes have resulted in the reduction in both the occurrences and rate at which back side haze form; proper handling and storage of reticles remains paramount in protecting all surfaces on the reticle from haze formation. We will describe again the basic mechanisms for the haze formation and how proper storage can result in the significantly reducing the risk of haze formation during storage and use in the fab.

There is an increasing trend in the semiconductor fab to classify all contamination on the reticle as haze. In this paper we will provide data that differentiates haze from the more common particle contamination on reticles.

Improving yields and reticle life by haze mitigation will not prevent particle contamination, two distinct approaches are required. Reticle storage and reduction of air-borne molecular will increase reticle usage without haze formation. Proper handling and particle control are required to prevent particle deposition.

7520-43, Session 10

In-shot overlay matching without pattern dependency using alignment and overlay metrology marks

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Recently pattern overlay accuracy becomes more and more important because of the small pitch patterning. Immersion technology made us be able to using hyper NA beyond 1.0 and this technology provided a lot of possibility to make a very small patterns. But there was no significant technical jump for overlay. Therefore chip makers started to compensate non-linear systematic overlay errors. For example, high order inter-field overlay correction is used to improve overlay performance between the tool to tool matching. Now chip makers try to compensate in-shot overlay. Scanner vendors provide intra-field matching options such as iHOPC(intra-field high order process correction - ASML) and SDM (Super Distortion Matching - Nikon) those are the method to match in-shot overlay easily. However there are a lot of arguments what the correct way is to measure the in-shot overlay and how we can feedback those measured data to APC system. Especially for the distortion measurement of scanner, we have different data from the mass production trend of distortion.

In this study, the pattern dependency and another cause of in-shot overlay error will be defined. This will provide a clue to solve difference between the mass production in-shot overlay trend and machine distortion data. The final goal of this study is providing the way to monitor the in-shot overlay correctly and feed-back to APC system.

7520-44, Session 10

A sophisticated metrology solution for advanced lithography: addressing the most stringent needs of today as well as future lithography

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Advanced lithography is becoming increasingly demanding when speed and sophistication in communication between litho and metrology (feed-back control) are most crucial. Overall requirements are so extreme that all measures must be taken in order to meet them. This is directly driving the metrology resolution, precision and matching needs in to deep sub-nanometer level.

Keeping the above in mind, a new scatterometry-based platform is under development at ASML. Authors have already published results of a thorough investigation of this promising new metrology technique (SPIE Asia 2008, SPIE Microlithography 2009) which showed excellent results on resolution, precision and matching for overlay, as well as basic and advanced capabilities for CD.

In this technical presentation the authors will report the newest results from this ASML platform. One of the goals of the new work in this presentation is to report overlay-results comparison between programmed overlay values (programmed on the scanner) and measured overlay by this new technology. Results from standard-size targets as well as small, process-robust overlay target results are reported. This report also aims to highlight the effectiveness of back-end (BEOL) layer overlay measurement capabilities where a good measurement was challenging with existing solutions. A complete front-end (FEOL) and back-end (BEOL) layer measurement strategy that minimizes the scribe-line consumption will be discussed. Finally, fab application and integration of this new technology will be discussed along with some early results from focus-dose control activity.

7520-45, Session 10

Scatterometry Measurement of Asymmetric Gratings

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Scatterometry has been used extensively for the characterization of critical dimensions (CD) and detailed side-wall profiles of periodic structures in semiconductor fabrication processes. It is demonstrated that scatterometry can provide accurate and high-precision measurement for 2D and 3D structures used in integrated circuits. Various experimental configurations, e.g., normal incident broadband reflectance spectroscopy, spectroscopic ellipsometry, and angular scatterometry measurement, have been developed to collect light signals diffracted from periodic structures. So far majority of the measurements are applied for symmetric gratings. In most cases devices are designed to be symmetric although errors could occur during fabrication processing and result in undesired asymmetry. The problem with asymmetric lines lies in the lack of capability to distinguish between left and right asymmetries with conventional optical scatterometry techniques.

In this work we investigate the capability of measuring grating asymmetry using three scatterometry configurations, i.e., normal incident broadband reflectometry, spectroscopic ellipsometry (SE), and generalized ellipsometry Mueller matrix measurement. The selection of these configurations covers different angles of incidence and azimuth angles. Two different samples, an imprint patterning disk and a spacer double patterning wafer, are used for the study. For patterning disk by imprint lithography, when the template is separated from the disk, sometimes the relief image on disk has asymmetrical profile, and cross-section SEM reveals that the asymmetrical resist line is typically tilted towards the outer diameter direction. For spacer double patterning, the asymmetry is introduced by the imbalance of spacer and sacrificial grating CD controls so that the final line features are placed with an overlay error.

The results show that non-normal alignment configurations have good sensitivity for measuring and distinguishing left and right asymmetry, and can therefore be used for monitoring processes, such as lithography and etch processing, for which symmetric structures are desired.

7520-46, Session 10

Systematic defect management by design aware inspection

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Based on three years of field engagement at IDM, memory and foundry fabs, we identified top defect challenges faced by fabs developing devices for the 32/28nm technology node. We surveyed systematic defects caused by process variation and interaction among design, process and OPC, and compiled the results of the meta-analysis. The survey results, supported by previously published works, showed that several types of systematic defects were prevalent at these leading-edge nodes. Because systematic defects must be identified early in process development and ramp to reduce development cost, our focus in this paper was to assess novel design-aware defect management techniques for detecting and identifying systematic defects.

Approach

To accomplish comprehensive design-aware defect management, we explored two major components: 1) Use of design layout data (e.g. GDS or OASIS file) to inspect critical areas identified by both simulation and empirical data gathering during process development, and 2) Identification of systematic pattern failures and random particles through defect binning by design and functional areas.

Deployment

Design-aware defect inspection can be used in many applications. In this work we discuss the following case studies:

1) Use of design information to identify systematic defects due to design-process interaction. Weak pattern can fail in a spatially random distribution across die and wafer. These failures are not just due to reticle or design issues but can occur due to design-process interaction. Such failures can be identified by the use of design-based grouping.

2) Efficiency in inspection care-area generation. A typical SOC device can contain thousands of scattered SRAM areas. The time it takes for an engineer to find them and group them into a single care area while setting up an inspection recipe is often time- or cost-prohibitive. By using design information these areas can be automatically identified, and a customized inspection recipe, enabling optimal sensitivity in each area of the die, can be built within the time allotted by the fab. Results from tests of this concept in one fab are given in.

3) Use of marginal pattern information. Marginal patterns are difficult to process but can be a good source of information for monitoring lithography tools. By evaluating the spatial signature of weak patterns using a pattern library, litho tool condition can be monitored. Similarly process split or mask revision can be analyzed quickly by using a pattern library that contains marginal pattern.

Summary

Three use cases have shown that, with the increase in systematic defects at the 32/28nm nodes, it is now valuable to integrate design data into the fab environment. In the first case study, introduction of design information helped identify weak pattern distributed randomly across the wafer. In the second case study, use of design information increased productivity in inspection recipe setup through accurate care-area definition and by permitting off-line setup. In the third case study, design information enabled engineers to make best use of marginal pattern data to monitor their litho tools. Both design-based setup and design-based binning strategies proved valuable.

All necessary technologies are available today to support these novel design-based strategies for management of systematic defects.

7520-47, Session 10

EUV mask pattern inspection with an advanced electron beam inspection system

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EUV mask defectivity is one of the most challenging road blocks for applications of the EUV lithography in sub-32nm technology node integrated circuit manufacturing. There are two major defect types of EUV mask: multi layer (ML) phase defects and pattern defects.

ML phase defects are mainly caused by the decoration of defects on substrate during ML deposition. Even a few nanometer height differences on the ML could cause the printable phase defect because of the short wavelength of 13.5 nm in EUV lithography. The ML phase defects are mainly inspected using confocal microscope with ultraviolet (UV) and deep UV (DUV) wavelength. [1], [2] Recently, actinic inspection of ML phase defects with EUV wavelength was also reported. [3]

EUV mask pattern defects are formed during absorber layer patterning process. Most pattern defect inspections are performed using optical inspection system with DUV wavelength. [4], [5], [6] In this study, an electron beam inspection (EBI) system developed by Hermes Microvision, Inc. (HMI) has been used to inspect an advanced EUV mask with 32nm half-pitch (HP) node patterns included programmed defects.

Comprehensive studies on inspection sensitivity and inspectability such as throughput and nuisance defects for EUV mask with the EBI system were conducted. We found the EBI has potential capability to inspect the 32nm HP node EUV mask. In the conference, we will elaborate on details of not only inspection sensitivity of various programmed defect categories but also throughput assessments with various inspection conditions. We will also discuss material dependencies of absorber layer, buffer layer and capping layer on the inspection sensitivity.

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7520-48, Session 11

Implementation of double patterning processes toward 22nm node

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The Numerical aperture(NA) has been significantly improved to 1.35 by the introduction of water base immersion 193nm exposure tool, however, realistic minimum feature size is still limited to 40nm, even with the help of robust RETs.

Double patterning processes are technique that may be adopted for fabricating etching mask patterns for the 32nm node, and possible also for the 22nm node. Although several double patterning processes have been introduced such as LELE,LLE and self-aligned spacer process, LELE LLE may still have disadvantage for over lay accuracy. The self-aligned spacer process has drawn much attention as an effective means of enabling the formation of repetitive patterns easily.

In this paper, the demonstration results to fabricate quite fine pattern by double patterning techniques would be introduced, and the process property of several DP would be compared.

7520-49, Session 11

Development of silicon glass for etch reverse layer (SiGERL) materials and BARCs for double patterning process

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Materials and process related with double patterning by using 193nm immersion lithography has been developed for the 32/22 nm node device generations.

The following process is examined as a fine hole pattern making method. At first, the pillar pattern obtained by the X-Y double line dipole exposure. Secondly, the reverse material is applied on pillar pattern and the subsequent process (dry etching or development) converts pillar pattern into hole pattern. We examined the reverse process and materials which is Silicon Glass for Etch Reverse Layer (SiGERL). And also we investigated organic Bottom-Anti-Reflective coating (BARC) which is adequately-considered for reflectivity control, lithography and etching process.

7520-50, Session 11

Advanced patterning solutions based on double exposure: double patterning and beyond

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We developed two different pattern curing techniques to stabilize first lithography (L1) patterns for the single-etch double patterning process. The first method uses a surface curing agent (SCA) that is coated on top of the patterned surface to form a protective coating layer during the curing bake process. The second method uses a thermal cure resist (TCR) that is a special 193nm photoresist with a crosslinkable functional group to form an insoluble network upon heating at higher temperature.

It was found that the surface curing process with SCA often results in the CD growth with L1 patterns after double patterning. This is mostly likely due to the "positive" interaction between L1 resist and the resist used in the second lithography (L2). This "positive" interaction between L1 and L2 resists were reduced when a post-curing bake (PCB) process was introduced just before the L2 resist coating. L1 CD was precisely controllable during the double patterning process with PCB and by changing PCB temperature, CD change of 0.3nm/°C was observed in the temperature ranging from 120 ~ 150°C.

It was also found that the resist curing process with TCR often results in the CD loss with L1 patterns after double patterning. This is probably due to the loss of a leaving group in the L1 resist patterns during the L2 process. Even though the L1 patterns can be cured to form 3D network, it's inevitable to avoid the deprotection reaction within the L1 patterns during the L2 process where L1 patterns are exposed and baked again. In order to minimize the CD loss with TCR, we developed a double patterning primer (DPP) which enhances "positive" interaction between L1 and L2 patterns. While CD loss of 5~6nm is observed without DPP treatment, 10~12nm CD growth was observed with DPP treatment. The L1 CD after double patterning was precisely controllable by post-priming bake process with the rate of 0.3nm/°C in the temperature ranging from 120 ~ 150°C.

Taking advantage of the CD growth with DPP treatment, we also developed a new shrink process calld "Shirink Process Assisted by Double Exposure" (SPADE). Contact hole CD was reduced by 10~30nm after SPADE and excellent through pitch performance was observed. SPADE can also improve LER/LWR when used in the formaiton of smaller trenches. In this paper, we will describe the use of DPP in the advanced patterning schemes to print smaller features that are not available by the regular single patterning process.

7520-51, Session 11

Litho-freeze-litho-etch (LFLE) enabling dual wafer flow coat/develop process and freeze CD tuning bake for >200wph immersion ArF photolithography double patterning

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Wafer flow through photolithography resist processing equipment, also known as coat/develop track systems (track), has to-date been via a single path between the FOUP stage wafer indexer and in-line exposure tool system (scanner). A system's mechanical throughput has been governed by a throughput-limiting, bottleneck wafer transfer robot (wafer handling unit) running a defined cycle-time (speed) and number of moves for a given wafer process flow. This single path wafer flow approach has run into several technical barriers as coat/develop track system throughput exceeds 200 wafers per hour (wph). Adding on-top of this the track system must also support multi-step coat and develop processes to enable Litho-Freeze-Litho-Etch (LFLE) flows at high-throughput to be a cost-effective 22nm photolithography solution. Many have claimed that the LFLE process steps are too many and wafer flow in pre-existing coat/develop track systems are impractical to support >200wph double patterning photolithography. Separately, while freeze materials improvements are being made, it is also recognized the coat/develop track process influences CD mean matching and plays a significant role in achieving pattern #1 to pattern #2 CD uniformity consistency in LFLE process.

The new SOKUDO DUO track concept incorporates a dual-path wafer flow to reduce the burden on the wafer handling unit and enables high-throughput coat/develop/bake processing. Various double patterning process flows previously reported by JSR Micro, TOK, and FujiFilm were modeled on the SOKUDO DUO system and confirmed to be able to process LFLE photolithography wafers at greater than 200wph capability (single pass). As part of coat/develop track LFLE process development it was confirmed that Biased Hot Plates (BHP) with "cdTune" is effective in optimizing within wafer CD uniformity results and influences mean CD matching between line #1 and line #2 patterns. LFLE process coat, develop and bake process results are outlined for Sokudo RF3S immersion lithocell in-line with ASML XT:1900Fi system in operation at IMEC, Belgium.

7520-52, Session 12

Inorganic negative tone resists for 193nm photolithography

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We achieved the preparation of nanostructures based on negative tone inorganic resist by DUV lithography (193 nm).

It entails the preparation of a complex of a transition metal by reaction between the metal and the suitable ligand. The reaction was carried out in a solvent. Then, a partial hydrolysis of the complex allows forming metal alkoxides inorganic chains by condensation with good film-forming and photopatterning properties. This step corresponds to the synthesis of multifunctional oligomers that can be crosslinked by DUV irradiation.

We obtained well-defined patterns exhibiting low rugosity for CD down to 75 nm. The sensitivity of the resin at 193 nm is in the order of magnitude of typical chemically amplified resists. DUV interferometry was used for nanopatterning.

The main interest of this resist is that after irradiation, the material is mainly inorganic. It can even be totally mineralized through a subsequent pyrolysis procedure.

The process is compatible with a wide range of chemicals (ZrO2, TiO2, ...). We are targeting applications in microelectronics, optics, photonics, photocatalysis, photovoltaic...

7520-53, Session 12

Low temperature plasma enhanced atomic layer deposition (PEALD TM) silicon oxide enables direct spacer defined double patterning (SDDP)

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Among the different double patterning techniques, Spacer Defined Double Patterning (SDDP) gains a lot of attention and is especially adapted for the patterning of repeating structures, and thus for NAND flash, but also DRAM and even logic's SRAM. The memory market is especially cost-driven, and is consequently in quest of simple and cost-effective solutions.

The spacer deposition used to double the pattern frequency in SDDP is typically performed with a CVD-type process. The process temperature is too high to be photoresist-compatible, so an additional sacrificial pattern is needed to define the spacers. This hardmask is often composed of a multi-stack, and the additional deposition and patterning of layers increase the cost and complexity of this approach. Furthermore, the well-known limita-

tions of CVD processes with respect to conformality, within wafer uniformity and loading effect negatively impact the performance and scalability of this integration scheme.

Plasma Enhanced Atomic Layer Deposition technology (PEALD TM) is particularly appropriate to overcome those drawbacks and improve the control of the spacers' critical dimension (CD). This process has inherently a perfect conformality, an excellent uniformity, and no loading effect. Besides, PEALD SiO2 shows a high throughput at very low temperature. Thanks to the expected photoresist-compatibility, the spacers can be directly deposited onto the photoresist/BARC lines. The so-called "direct SDDP" process scheme (Figure 1) does not require an additional hardmask deposition and patterning, contrary to the standard SDDP approach.

In the present work, photoresist lines have been patterned on 300 mm wafers by an immersion ArF scanner (NA=1.2). Figure 2 highlights the very good conformality and compatibility of the PEALD SiO2 with the photoresist and BARC (deposited on a silicon substrate in this case): no detrimental impact is observed by X-SEM after the deposition, despite the use of a plasma. The full process flow described in Figure 1 has been optimized, including lithography, deposition and etch, and will be discussed in this paper. Polysilicon lines have been successfully patterned (Figure 3), and CD-SEM measurements are displayed in Table 1. The CD of line 1 and line 2, resulting from the PEALD SiO2 spacers, are identical within the SEM accuracy: 37.29 nm and 37.35 nm. Furthermore, their 3 CD-uniformity and Line Width Roughness are very good, respectively less than 1.5 nm and less than 2.0 nm. It highlights the improvements provided by the PEALD technology. Data collection on multiple wafers is currently being performed.

A successful direct SDDP integration has been reported for 32 nm half-pitch polysilicon lines. This approach, enabled by the PEALD technology, reduces cost and complexity of SDDP. The inherent advantages of this process (perfect conformality, excellent uniformity, no loading effect, low temperature process capability, high throughput) make it particularly suitable for scalability towards the 2X and 1X nodes.

7520-54, Session 12

Filtration condition study for enhanced microbridge reduction

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As lithographic pattern CDs continue to shrink, so does the tolerance for the size of photoresist defects, such as agglomerated microbridge precursors. Greater demands will certainly be placed on the cleanliness of next-generation lithography process fluids. Filtration products built around Nylon 6,6 membrane technology have demonstrated effectiveness in reducing microbridge defects within UV-sensitive photoresists.[1-4] Recent work revealed that adsorption of gel-like precursors onto Nylon 6,6 membrane media was the primary mechanism driving microbridge defect reduction.[5] In the present work, the effects of fluid flow characteristics on defect reduction using a point-of-use Nylon 6,6 filtration product are explored.

Within the photoresist solution, microbridge precursors are thought to exist as a gel-like substance. Formation of microbridge precursors can be encouraged by spiking an ArF photoresist polymer solution with metal ions, which act as quasi-nucleation sites around which the nearly insoluble resist polymer components may aggregate.[5] Since this gel-like substance includes metal, the presence of defect precursors can be quantified using inductive coupled plasma-mass spectrometry (ICP-MS).

The Pall Asymmetric P-Nylon Filter Assembly was tested using Mg-spiked photoresist polymer solution. Flow rate, filtration pressure, and membrane volume (Thickness × Area) were varied.

Evaluation results are expressed as gel removal efficiency vs. contact time (Figure 1). The dependence of gel removal efficiency, which directly correlates with measured Mg concentration, on contact time varies strongly with filtration pressure. At a high-pressure condition (0.2 MPa), gel removal efficiency shows a strong positive correlation with contact time. This is a typical phenomenon observed in adsorption processes. This result is supported by a previous observation that Nylon 6,6, compared to HDPE, is more effective in microbridge reduction at point-of-use filtration, mainly due to adsorption that is driven by electrostatic attraction to polar peptide bonds on Nylon 6,6. At low pressure, (<0.06 MPa), gel removal efficiency is independent of contact time. Moreover, removal efficiency is consistently greater than at high pressure. Previous work by Sumiya and Numaguchi suggests a physical model underlying the observed results.[6] Increased pressure drives gel aggregates to permeate the filter media depth. Conversely, at lower pressure, gels interact primarily with the filter media surface. This is confirmed by SEM observation and described by a pore plugging model. Thus, at a high-pressure condition, gels are adsorbed to a greater extent at sites throughout the membrane depth. This leads to less interaction between gels and filter media (as gels are transported through the media depth), less adsorption, and ultimately, complete gel permeation into the filtrate, which is manifested as decreased removal efficiency. At a low-pressure condition, there is less upstream force to drive gels into the filter media depth. Thus, gels adsorb primarily onto the filter media surface, leading to a weaker dependence of removal efficiency on contact time. Furthermore, less penetration of gels through the membrane thickness leads to greater removal efficiency.

In conclusion, lower filtration pressure and longer contact time were found to enhance the removal of gel-like microbridge defect precursors during point-of-use filtration of photoresist polymer solution. The impact of filtration pressure on gel removal dependency on contact time strongly suggests that electrostatic adsorption of gels to polar Nylon 6,6 functionalities is the dominant mechanism of microbridge defect precursor filtration. These findings will be very useful both in optimizing filter operating procedures and in the development of next-generation filtration products, ultimately contributing toward reduced defectivity and increased yield within next-generation lithography processes.

7520-55, Session 12

Possible line edge roughness reduction by anisotropic molecular resist

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Extreme ultra-violet (EUV) lithography technology is being developed for the patterning sub-32nm node. Line edge roughness (LER) is the one of the important issues together with the resist performance like resolution and sensitivity. There are some novel resists for EUV lithography that can be used for obtaining the target resolution and sensitivity, while the line edge roughness do not reached the target values in most resist yet. In order to reduce the LER, the molecular resist has been widely studied due to their small size compared to the conventional polymer resist. There is another approach to reduce the LER by reducing the acid diffusion length, but it is not easy to reduce down the acid diffusion length. We tried a new approach to reduce down the LER by changing the shape or structure of the molecular resist. A new molecular resist shape that shows the anisotropic structure is tried to see the LER and whether this anisotropic resist can be used for LER reduction. We studied the reduction of LER versus the resist thickness, illumination type, and acid diffusion. We also evaluated the protection group concentration ratio dependency to the LER.

7520-56, Session 12

A proven methodology for detecting photo-resist residue and for qualifying photo-resist material by measuring fluorescence using SP2 bare wafer inspection and SURFmonitor

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During the chip making process, complete removal of photo-resist after the expose & develop step, before the etch step is very critical. It has been established that unwanted photo-resist residue can cause catastrophic failure due to blocked etch resulting in significant yield loss. These photo-resist residues can be due to process tool issues and/or subtle differences in photo-resist

composition. Most of the current metrology & analytical methods do not provide enough sensitivity to detect small amounts of photo-resist residue on the wafer or differentiate between good & bad batches of photo-resist. Using the novel method described in this study, the SP2 & SURFmonitor solution has demonstrated excellent sensitivity in detecting small amounts of photo-resist residue. In addition, this method provides a simple and easy way to qualify a batch of photo-resist for production use.

This method takes advantage of the fact that photo-resist residue, which is organic in nature, will fluoresce. By scanning wafers after the expose & develop step using the SP2 (UV wavelength) unpatterned defect inspection tool equipped with SURFmonitor, it is possible to generate a full-wafer fluorescence SURFimage. This SURFimage was shown to clearly indicate the regions of the wafer that have photo-resist residues. Further, this image can be used in conjunction with the grid analysis or zonal analysis to produce a simple SPC chart for process monitoring, which can be easily implemented in a production fab. Alternatively, the same analysis can be used to qualify photo-resist for production usage.

7520-30, Session 13

Pattern prediction in EUV resists

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Accurate and flexible simulation methods may be used to further a researcher's understanding of how complex resist effects may influence the patterning of critical structures. In data of EUV resists, we have observed that, while base lithographic responses such as the exposure latitude of trench CD are about equal among samples of interest, corner rounding and the end-of-trench show much variability. The reason is unclear but may be related to the EUV exposure mechanism. At lambda = 13.5 nm, the acid generation mechanism is similar to CA e-beam resists: acid generators are hypothesized to be activated by secondary electrons yielded by ionization of the resist matrix upon absorption of high-energy EUV photons. Although the inelastic mean-free path of secondary electrons with kinetic energy 20 eV is less than 1 nm, the thermalization distance can reach ca. 5 nm, suggesting that electrons may activate acid generators some distance from the absorption site. It is hypothesized that, depending upon the properties of a given EUV resist system, the initial condition of the exposed image-in-resist (the acid shot noise image) may differ from sample to sample, modifying some downstream behavior such as corner-rounding and the end-of-trench. In this work, we attempt to gain insight into the causes of the observed differences between several EUV resists through the use of stochastic resist modeling and inductive reasoning. The model's parameterized fit to experimental data from several resists irradiated EUV will be shown and discussed. Resist pattern prediction of both 1D and 2D structures exposed with a well-characterized EUV mask will be discussed.

7520-57, Session 13

Validation of the predictive power of a calibrated physical stochastic resist model

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Virtually all lithography simulation used in the semiconductor industry relies on the continuum, or mean-field, approximation. Such models assume that the exposing illumination can be treated as a series of interfering plane waves and that the distribution of chemical components within the photoresist (PAG, photo-acid, quencher etc) is completely homogeneous and can vary continuously. Although this approach ignores statistical effects, due to the quantization of light into photons and the fact that resist components are discrete molecules, it has been used successfully for decades to predict core lithographic behaviors. However, as lithography approaches its fundamental physical limits, phenomena driven by quantized statistical processes, such as line-edge roughness, contact hole circularity and CD distribution, are becoming increasingly important. If virtual lithography is to help address these new industry challenges, then simulation tools need to, at least partially, transition from their current deterministic domain into a probabilistic one.

Earlier this year, a stochastic exposure and resist model was proposed [1], the model accurately described some basic, experimentally observed, lithographic behaviors, specifically mean CD and 3sigma LWR through exposure dose (i.e. exposure latitude) for one photoresist irradiated at two different exposure wavelengths (ArF and EUV).

In this work, the same model is calibrated to a comprehensive experimental data set for a commercially available immersion ArF photoresist, EPIC2013 (Dow Advanced Materials). The experimental data comprise of full FEM data for multiple feature pitches. At each point in the FEM, mean CD and LWR statistics are available and repeat matrices were run on separate wafers.

The dataset allows more extensive testing of the models ability to describe complex lithographic behaviors such as Bossung curve shape, proximity effects and LWR (including its power spectrum response).

Finally, the predictive power of the calibrated model is tested by comparing simulation results to experimental CD variance data for various 1D and 2D mask patterns under scanner optical settings (NA and source-shape) which differ from those used for model parameter calibration.

[1] Biafore et al., "Statistical simulation of resist at EUV and ArF', SPIE Vol. 7273, 727343, 2009.

7520-58, Session 13

Hierarchical mask assignment for double patterning lithography

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Double patterning with ArF water-based immersion systems has emerged as a strong candidate to first extend lithography to 32nm and below.

Concurrent with the advancements in double patterning process, there has been active research in decomposing a design into two masks suitable for manufacturing with double patterning. As geometries across the chip can potentially involve in the same conflict, decomposition for double patterning has been recognized as unbounded.

We will show in this paper that the unbounded nature of a potential conflict drawing in geometries from across the chip, however, poses little obstacle to efficient conflict visualization or mask assignment. Hierarchy already present in design offers different levels of abstraction for conflicts spanning across various levels of the hierarchy. And pseudo hierarchy from tiles of the flattened design are even more amenable in that they are already positioned with respect to the flat view, and overlap only marginally when they do.

While there have been generous research literature in the mask assignment problem with respect to geometries within cell or flat view of a design, details have been sketchy with respect to how hierarchy is addressed or any special handling needed for peculiar complexities arising from hierarchy. What has not been pointed out is the subtle but significant distinction that hierarchical processing adds one more dimension to the optimization problem at hand. For every step of a hierarchy processing, how it resolves its hierarchy peculiar concerns directly impacts its output hierarchy and the efficiency of processing steps that follow. In this paper, we limit our focus to the presentation of the hierarchical mask assignment algorithm which tackles the coloring aspect of the double patterning technology. We will illustrate the specific concerns arising due to the additional optimization dimension posed by hierarchical processing, and present an algorithm that address them sufficiently.

7520-60, Session 13

Model-based scanner tuning for process optimization

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Given the continually decreasing k1 factor and process latitude in advanced technology nodes, it is increasingly important to understand and control the variables which impact imaging behavior in the lithography process. In this joint work between TSMC and ASML, we use model-based simulations to characterize and predict imaging effects of these variables, and to fine-tune the scanner settings based on such information, in order to achieve optimal printing results on a per-reticle basis. The scanner modeling makes use of detailed scanner characteristics as well as wafer CD measurements for accurate model construction. Simulations based on the calibrated model are subsequently used to predict the wafer impact of changes in tunable scanner parameters for all critical patterns in the product. The critical patterns can be identified beforehand, either experimentally on wafer or on mask or through model simulations. A set of optimized scanner variable offsets, known as a “scanner tuning recipe” is generated to improve the imaging behavior for the critical patterns. We have demonstrated the capability of this methodology for multiple use cases with selected ASML scanners and TSMC processes, and will share the achieved improvements on defect reduction and yield improvements.