

Technical Program

SPIE *Advanced*
Lithography

25 February–2 March 2007

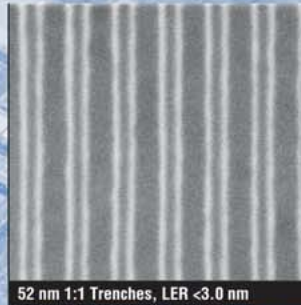
*San Jose Convention Center and San Jose Marriott
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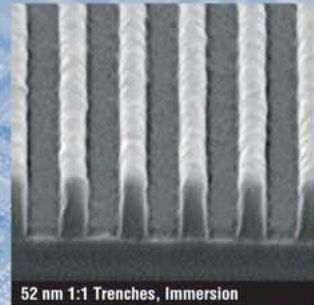
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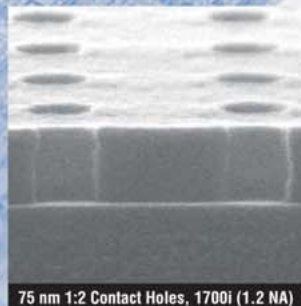
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52 nm 1:1 Trenches, LER <3.0 nm



52 nm 1:1 Trenches, Immersion



75 nm 1:2 Contact Holes, 1700i (1.2 NA)



Innovations in ArF Lithography::: In an industry that depends on innovation and leaps in technology, you should be able to depend on your materials supplier to provide leading-edge products. At Rohm and Haas Electronic Materials, we deliver all the lithography materials you need for memory and logic applications, backed by science, engineering and quality. Here are some of our latest innovations in ArF lithography:

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SPIE *Advanced* Lithography

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Technical Program

SPIE *Advanced* Lithography

Conferences • Courses • Exhibition

25 February–2 March 2007 San Jose Convention Center and San Jose Marriott • San Jose, California USA

Sponsored by:

SPIE

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Solid State Technology



Microlithography World, a Solid State Technology publication, is published in cooperation with SPIE and BACUS.

Welcome!

The SPIE Advanced Lithography Symposium is an annual international forum bringing practitioners of micro- and nanolithography together in a stimulating, informative, and interactive environment. The Symposium is fully committed to support your interests whether you work in semiconductor production lines, pilot lines, or research laboratories. It succeeds because the programs are tailored to professionals like you: those using technologies for today's production or developing it for production in the near future. Moreover, the numerous short courses offered at Advanced Lithography 2007 are taught by individuals who are active in the field and recognized for their theoretical knowledge and practical experience.

We're excited to offer this opportunity to learn about the latest state-of-the-art applications and techniques, as well as emerging issues with the new challenges of alternative technologies. This wide range of topics becomes all the more important as optical lithography, historically the dominant patterning technology, faces new and tough challenges in providing the patterning solutions for leading-edge semiconductor manufacturing.

Welcome to San Jose for our 32nd year!



Roxann L. Engelstad
Univ. of Wisconsin/Madison
2007 Symposium Chair



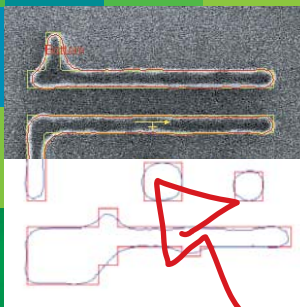
Christopher J. Progler
Photronics Inc.
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the need for

SPEED

from litho development to production

VeritySEM™ with OPC Check™



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BOOTH 703

- CD-SEM Metrology
- OPC Qualification
- CVD/PVD Hardmask
- Wafer and Mask Etch



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VeritySEM and OPC Check are part of Applied's Resolution initiative—a commitment to cut the time and cost of resolving yield-limiting defects. Visit Booth 703 and learn more about Applied's unique portfolio of Litho-Enabling Solutions, from advanced patterning films and pattern transfer to metrology, OPC design qualification—each technology carefully engineered to ease next-generation lithography requirements and optimize results.

See more at www.appliedmaterials.com/resolution

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General Refreshments

Canon U.S.A., Inc.
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Special Events and Conference Daily Overview

Monday	Tuesday	Wednesday	Thursday	Friday
Special Events				
<p><i>Plenary Presentation:</i> Nanoscale Patterning Challenges for CMOS Density Scaling, Johannes M.C. (Hans) Stork, 8:15 to 9:00 am, p. 6</p>	<p><i>Conference 6520 Panel Discussion:</i> Virtual Lithography: The Next Generation?, 6:40 to 8:10 pm, p. 9</p>	<p><i>Joint Sessions with Conferences 6517 and 6519:</i> EUV Resists 6:30 to 8:50 pm, p. 10</p>	<p><i>Conference 6521 Panel Discussion:</i> Design for Manufacturability: Open Mic Night, 7:30 to 9:00 pm, p. 10</p>	<p><i>Conference 6520:</i> Best Student Paper Award, 10:25 to 10:35 am, p. 11</p>
<p><i>Plenary Presentation:</i> Collaborative Innovation: IBM's Immersion Lithography Strategy for 65 nm and 45 nm Half-pitch Nodes & Beyond, George A. Gomba, 9:00 to 9:45 am, p. 7</p>	<p><i>Nanotechnology in Microlithography Panel Discussion on:</i> Metrology & Materials for Nanoimprint Lithography: Needs and Prospects, 7:00 to 9:00 pm, p. 10</p>	<p><i>Joint Sessions with Conferences 6520 and 6521:</i> Computational Lithography, 6:20 to 8:00 pm, p. 10</p>	<p><i>NIST Workshop:</i> Critical Dimension Standards: The Past, Present, and Future, 7:00 to 9:00 pm, p. 11</p>	
<p><i>Plenary Presentation:</i> Lithography Beyond 32 nm: A Role for Imprint?, Mark Melliar-Smith, 9:45 to 10:30 am, p. 7</p>	<p>Women in Optics Lunch, noon to 1:00 pm, p. 9</p>	<p><i>Conference 6518 Panel Discussion:</i> New Frontiers in Overlay Metrology, 8:00 to 9:30 pm, p. 10</p>	<p>Poster Reception, (Conf. 6517, 6520, 6521), 5:30 to 8:00 pm, p. 9</p>	
<p><i>Conference 6518:</i> 2006 Best Paper Announcement, 11:00 to 11:20 am, p. 9</p>	<p>EXHIBITION, p. 14 10:00 am to 5:00 pm 10:00 am to 4:00 pm</p>			
<p>BACUS and Photolithography Technical Groups Panel Discussion, 7:30 to 9:00 pm, DPT: Twice the Pain for Twice the Gain!, p. 9</p>				
<p>Poster Reception, (Conf. 6518, 6519), 5:30 to 8:00 pm, p. 9</p>				
Conferences				
Conf. 6518 Metrology, Inspection, and Process Control for Microlithography XXI (<i>Archie</i>) p. 20				
Conf. 6519 Advances in Resist Materials and Processing Technology XXIV (<i>Lin</i>) p. 26				
	Conf. 6517 Emerging Lithographic Technologies XI (<i>Lercel</i>) p. 33			
	Conf. 6520 Optical Microlithography XX (<i>Flagello</i>) p. 40			
			Conf. 6521 Design for Manufacturability through Design-Process Integration (<i>Wong</i>) p. 48	
<p>New Courses at Advanced Lithography 2007</p> <p><i>Don't miss these cutting-edge additions to this year's Professional Development program.</i></p> <ul style="list-style-type: none"> • Recent Advances in Electron Beam Lithography • Introduction to Scatterometry Metrology: Theory and Application • IP Issues in Advanced Lithography and Semiconductor Manufacturing • Lithography Integration for Semiconductor Back-End-Of-The-Line (BEOL) • Lithography Friendly Design and Beyond—A Broader Review of DfM <p>Register at the SPIE Cashier!</p>				

Welcome Announcements and Plenary Presentations

Convention Center Hall 3



A full house last year at the plenary presentation!

Welcome Announcements and Introduction of New SPIE Fellows

Monday 8:00 to 8:15 am

Symposium Chair: **Roxann L. Engelstad**, Univ. of Wisconsin/Madison

Frits Zernike and the Advances in Optical Microlithography 4th Frits Zernike Award for Microlithography

Presented by: **Roxann L. Engelstad**, Univ. of Wisconsin/Madison

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Plenary Presentations

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Nanoscale Patterning Challenges for CMOS Density Scaling

Monday 8:15 to 9:00 am



Johannes M.C. (Hans) Stork, Senior Vice President and Chief Technology Officer, Texas Instruments Inc.

Continuous improvements in optical lithography have been a primary factor in enabling the economic benefits of geometric scaling. In fact, density scaling has long been synonymous with cost scaling. However, the complexity of sub-wavelength patterning has led to significant cost increases in scanners, pattern generation, mask and resist processing, and etching. In addition, since pattern

fidelity depends on surrounding features in the immediate proximity, local variations have approached and now may exceed the level of global variations. These effects impose the use of additional statistical simulation to more accurately predict behavior across a die, and wafer, lot and fab, respectively. The cost, therefore, of improving density has reached far beyond the fab and is a major factor in the design of a product. We will examine the trade offs between continued density and performance scaling and cost improvements going forward, especially for 45/32nm CMOS low power products that integrate logic, memory and RF/analog for fully contained systems on a chip.

Dr. Hans Stork is currently Senior Vice President and Chief Technology Officer of Texas Instruments. As Director of the Silicon Technology Development organization, his primary responsibilities are the development of advanced CMOS, packaging and mixed signal process technologies.

Dr. Stork started his professional career in 1982 at IBM's T. J. Watson Research Center, investigating advanced bipolar technology and circuits. Hans became manager of the Bipolar Devices group, and from 1992 to 1994 assumed responsibility for the Exploratory Device and Technology programs at IBM Research. In 1994, Dr. Stork joined Hewlett-Packard and held the position of Director of the ULSI Research Lab between 1995 and 1999. From 1999 to 2001, Dr. Stork was Director of the Internet Systems and Storage Lab at HP Laboratories in Palo Alto, CA. In 2001, he took a position as Vice President and Director of Silicon Technology Research at TI.

Hans received two Outstanding Technical Achievement Awards from IBM. He has written or co-authored nearly 100 cited papers and holds eleven US patents. He was elected IEEE Fellow in 1994 for his contributions to SiGe devices and technology, and has served on numerous IEEE program committees. Hans was EDS editor of the Circuits and Devices magazine from 1993 to 1995, and was on the technical program committee of the Symposium on Low Power Electronics in 1995 and 1996. He also serves on the Board of Directors for SEMATECH (since 2002) and for the Semiconductor Research Corporation (since 1999). He has been a member of the SIA Technology Strategy Committee since 1999.

Dr. Stork was born in Soest, The Netherlands, and received the Ingenieur degree in Electrical Engineering from Delft University and holds a PhD from Stanford University.

Collaborative Innovation: IBM's Immersion Lithography Strategy for 65 nm and 45 nm Half-pitch Nodes & Beyond

Monday 9:00 to 9:45 am



George A. Gomba, IBM Distinguished Engineer and Director of Lithography Technology Development, IBM Corp.

Any successful lithography strategy requires the comprehensive integration of a vast array of technology elements crossing numerous scientific and engineering disciplines. A fundamental understanding of the components (imaging systems and optics, optical proximity correction (OPC), resolution enhancement techniques (RETs), photomasks, materials and processes), their interactions with each

other and with circuit design is essential to deliver a manufacturable patterning solution. IBM addresses this challenge using a collaborative innovation strategy that incorporates our internal R&D and manufacturing teams along with our technology development partners and strategic relationships with lithography-component suppliers. This approach has set the stage for IBM's implementation of immersion lithography for the 65 nm and 45 nm half-pitch nodes. Beyond this, the 32 nm half-pitch node presents unprecedented challenges; chief among them is a lack of availability of a manufacturing tooling solution to meet two-year technology cycles. This paper details the key challenges associated with the introduction of immersion as a manufacturing technology, IBM's solutions to these challenges and the outlook for future lithography nodes.

IBM's leadership in immersion hyper-NA lithography is a result of early imaging and materials investigations using interference lithography, joint development of the first immersion scanners and topcoats, the first demonstration of yielding microprocessors employing immersion and is demonstrated in the implementation a comprehensive integrated solution for 65 nm half-pitch manufacturing. Critical challenges included early recognition of defectivity formation mechanisms and prevention, the impact of water evaporation on overlay performance, and solutions that address reflectivity control and deviations from Kirchhoff approximations for the hyper-NA afforded by immersion. Compounding these challenges was the introduction of hyper-NA imaging tooling late in the development cycle. This disconnect was addressed by a computational lithography solution, which included extensive simulation that incorporated all the requisite hyper-NA effects and the pioneering use of predictive extrapolated OPC models.

Water immersion provided an increase of ~40% in NA for the 65 nm half-pitch node and allowed for direct migration of the previous node's RET solutions. The full extension of water immersion to 1.35 NA will only afford an additional 12.5% increase in NA for the 45 nm half-pitch node. This has driven a strategy for the development of significantly more aggressive RET solutions that require a co-optimization with circuit design. The approach entails rigorous process window simulations and strikes an appropriate balance between design restrictions and process complexity, such as double exposure techniques.

It is clear that the magnitude of the technological hurdles will continue to increase and new paradigms are required to successfully clear them. Along these lines, IBM is also developing leading edge technologies for rigorous EMF simulations, applications of global source mask optimization and process-window aware OPC methodologies. IBM is well positioned to address the massive computing power required to reap the benefits of these approaches. As a prelude, our recent results using deep computing will be presented.

With all the technical and schedule challenges facing alternative imaging tooling solutions, the collaborative innovation strategy of IBM and our partners is poised to take advantage of all the capabilities of water immersion lithography to provide manufacturing solutions for the 65 nm and 45 nm half-pitch nodes and beyond.

Mr. George A. Gomba is currently the Director of Lithography Technology Development for the IBM Systems and Technology Group. In this role, he is responsible for the research and development of next generation lithography

elements for advanced patterning solutions essential to the innovative integration of IBM's semiconductor process technology. Since 1989 he has held a variety of technical and managerial positions and was appointed IBM Distinguished Engineer in June 2002.

Mr. Gomba has provided industry direction in lithography research, serving as chairman of the Semiconductor Research Corporation Lithography Sciences Technical Advisory Board, co-chairman of the Semiconductor Industrial Associates Lithography Technical Working Group, and participant in numerous SEMATECH technical advisory groups.

Before joining the IBM Corporation, Mr. Gomba had nine years of experience in optical and systems engineering with the Perkin-Elmer Corporation, developing imaging and alignment systems and pioneering the first-of-a-kind deep ultraviolet step-and-scan lithography technology for the semiconductor tooling industry. Mr. Gomba holds a BS degree in Optical Engineering from the University of Rochester.

Lithography Beyond 32 nm: A Role for Imprint?

Monday 9:45 to 10:30 am



Mark Melliar-Smith, CEO, Molecular Imprints, Inc.

Imprint lithography has been used since the application of the Chinese wax seal to authenticate official documents. In the past century the resolution of the technology has been driven through commercial applications such as vinyl records, CDs and more recently by high definition DVDs. In the past decade high resolution imprinting has extended the resolution down to sub 10nm features and this fact

coupled with the low cost of the tool make it attractive as an alternative to other lithographic technologies.

More recently the evolution of imprint lithography from thermal imprinting to UV cured materials, has allowed the technology to operate at room temperature (allowing tight overlay) and low material viscosities (important for high throughput), opening up the potential for CMOS applications. This paper will discuss recent progress in align/overlay, throughput, defect density, materials and the availability of sub 20nm 1x templates, along with tool developments that make the technology a viable option for advanced CMOS beyond 32nm HP design nodes.

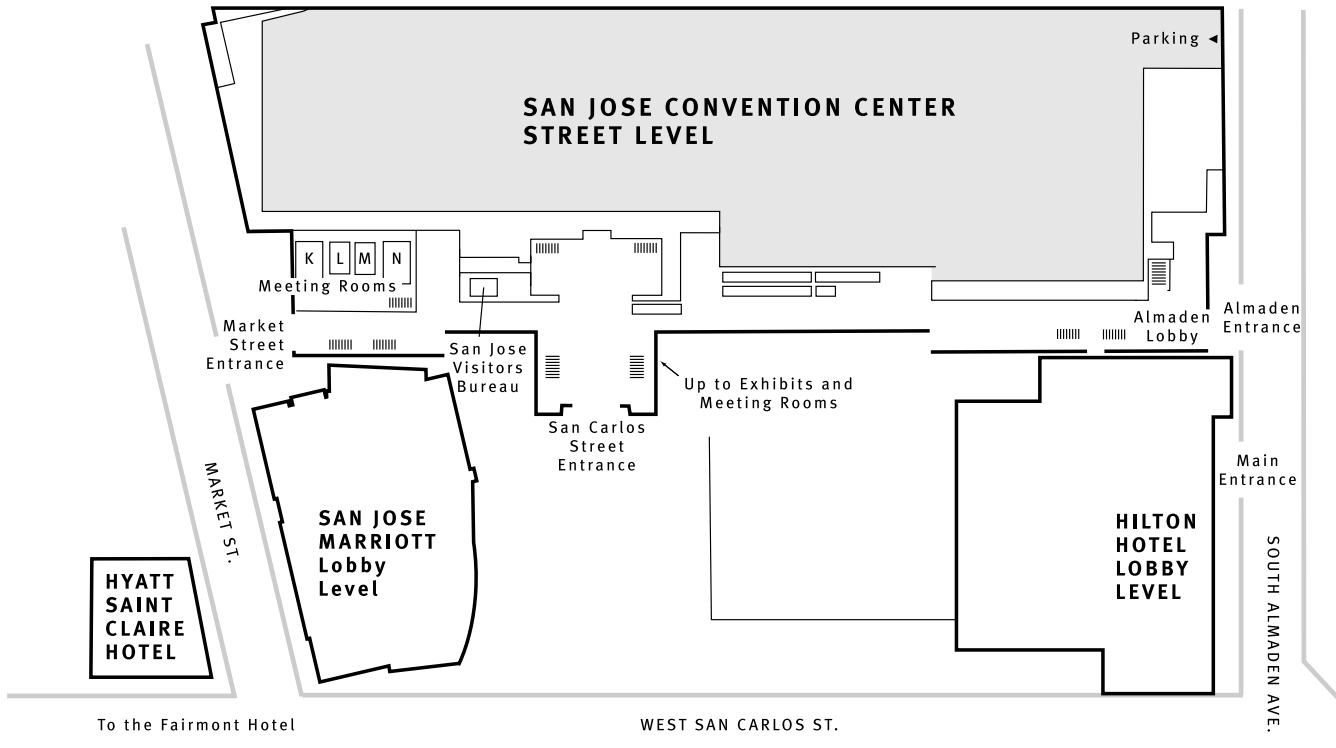
In addition, imprint lithography is being developed for other large electronic markets such as bit patterned media (BPM) for disk drives and photonic crystals to increase the brightness and efficiency of LEDs used for solid state lighting, applications likely to go into production ahead of sub 32nm CMOS. Since overlay requirements are significantly less, whole wafer (as opposed to step and repeat) imprinting is used for these applications, and the presentation will discuss the similarities (sub 25nm features), and differences with CMOS imprint technology.

Finally the paper will discuss some of the recent research work being done on devices where the ultimate resolution of imprint below 10nm is being utilized to probe the limits of electronic devices.

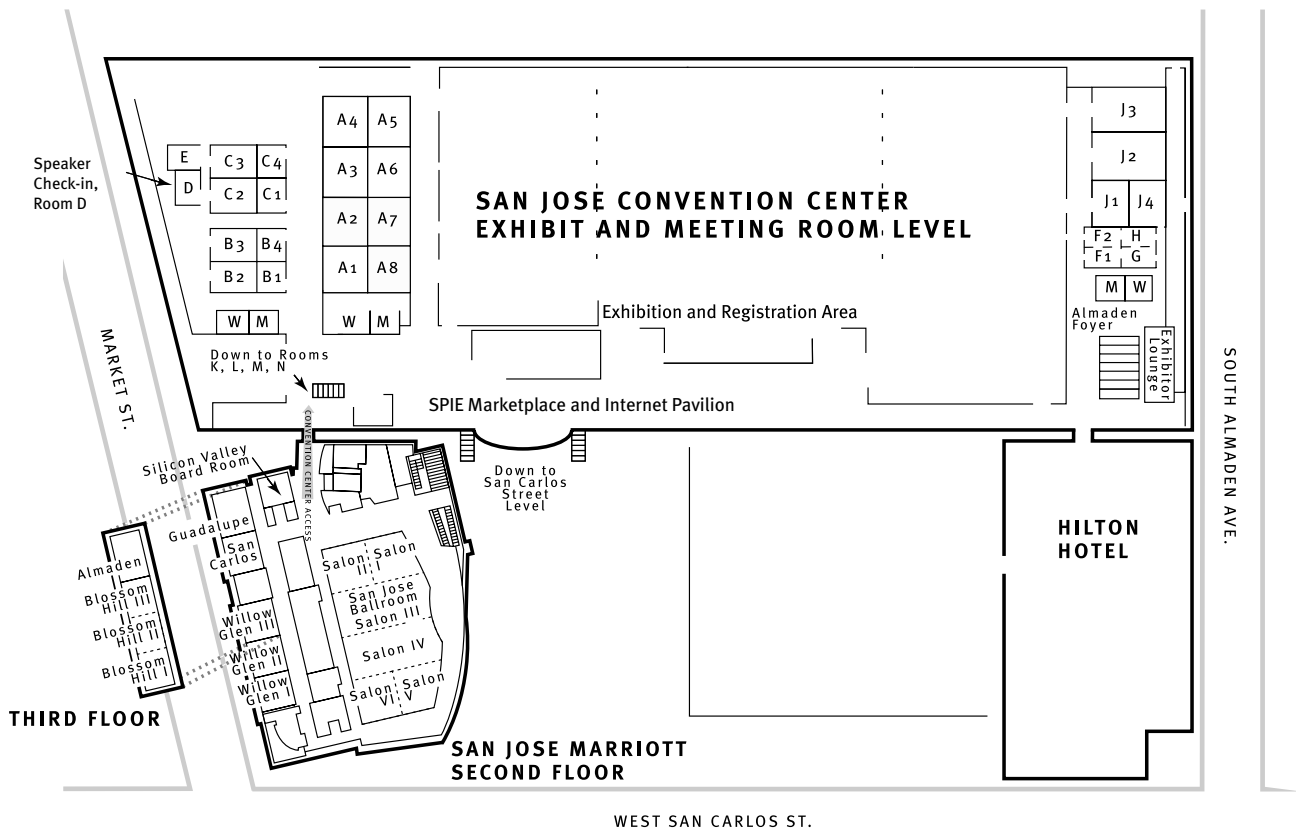
Dr. Mark Melliar-Smith is the Chief Executive Officer for Molecular Imprints, a start-up company in Austin, Texas, which develops and manufactures imprint lithography tools. Prior to joining Molecular Imprints, Mark was a Venture Partner with Austin Ventures (2002-2003), a venture capital firm located in Austin, Texas. From 1997 to 2001, he was President and CEO of SEMATECH, and from 1990 through 1996 he was the Chief Technical Officer for Lucent Technologies Microelectronics (the forerunner of Agere Systems). During his thirty-five year career, Mark has held a wide variety of technical and management positions in R&D, manufacturing and business management, including Executive Director of the Bell Laboratories Photonics and Integrated Circuit Division and VP and General Manager of the AT&T Lightwave Business Unit. He serves on the Board of Directors for Power-One (Camarillo, CA), Technitrol (Philadelphia, PA), MetroSol (Austin, TX) and Molecular Imprints. Dr. Melliar-Smith received his BS and PhD degrees in Chemistry from Southampton University and his MBA degree from Rockhurst College.

Coffee Break 10:30 to 11:00 am

San Jose Convention Center and Marriott Hotel Floorplans



Second Floor



Street Level

Conference 6518

2006 Best Paper Announcement for Metrology, Inspection, and Process Control for Microlithography

Convention Center J2

Monday 26 February 11:00 to 11:20 am

BACUS and Photolithography Technical Groups Panel Discussion

DPT: Twice the Pain for Twice the Gain!

Convention Center C1

Monday 26 February 7:30 to 9:00 pm

Moderators: **Paul Luehrmann**, ASML; **Artur Balasinski**, Cypress Semiconductor

Panelists: **Peter D. Buck**, Toppan Photomasks, Inc.; **Kevin D. Lucas**, Synopsys, Inc.; **Apo Sezginer**, Invarium, Inc.; **Tuan Pham**, SanDisk, Inc.; **Robert J. Socha**, ASML Mask Tools Inc.

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This panel of leading lithography industry experts will provide a lively discussion with respect to their opinions on both the readiness and challenges facing the mask industry under the pretext of utilizing multiple exposures to achieve sub 32nm imaging. The panelists, both lithographers and mask technologists, will provide their potentially dissenting views on just how far 193nm immersion can enable a viable lithography solution.

About BACUS

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology and Management Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management. BACUS also offers videotape subscriptions of its monthly meetings and regularly sponsors panel discussions and events to foster both personal and business relationships within the industry.

About Photolithography

The primary focus of this group is on photolithography used in the manufacture of devices, tape/disk heads, LCDs, sensors, and other technologies. The group holds joint monthly meetings with the BACUS(Photomask) in the San Francisco Bay Area on topics in photolithography technology. Topics that have been discussed at past meetings include half-micron photolithography, a top anti-reflective coating process, and advances in deep UV resist materials, metrology, and overlay. Future meetings will cover process control in semiconductor manufacturing, advanced topics in develop end point detection, depth of focus issues, modeling, dry developable resist systems, and many other fascinating and relevant subjects.

As semiconductor microelectronic devices continue their progress toward finer and finer geometries, optical microlithography not only stubbornly refuses to die, it continues to dominate comfortably alternative technologies.

Poster Receptions

Convention Center Hall 3

Monday 26 February 5:30 to 8:00 pm
(Conf. 6518, 6519)

H'ors D'oeuvres sponsored by



Beer and Wine sponsored by



Thursday 1 March 5:30 to 8:00 pm
(Conf. 6517, 6520, 6521)

Beer and Wine Sponsored by



Conference attendees are invited to the poster sessions and receptions. Authors of poster papers will be present and at their posters during these sessions to answer questions and provide in-depth discussion concerning their posters. Attendees and authors are required to wear their conference registration badges to the poster sessions.

For the poster session on Monday 26 February, poster authors can set up their posters after 10:30 am. For the Thursday poster session, the author can set-up after 9:00 am. Poster supplies (push-pins) will be available. Poster can be previewed during the day before the formal poster sessions begin at 5:30 pm.

Authors must remove their posters at the conclusion of the poster reception for that day. It is the authors' responsibility to remove their posters. Posters not removed will be considered unwanted and will be discarded. SPIE assumes no responsibility for posters left up after the end of each night's poster reception.

Conference 6520 Panel Discussion

Virtual Lithography: The Next Generation?

Convention Center A2

Tuesday 27 February 6:40 to 8:10 pm

Chairs: **Mircea V. Dusa**, ASML MaskTools Inc.; **Nigel R. Farrar**, Cymer, Inc.

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We have entered a new era in lithography. Traditional developments based on "what will be the next exposure tool" is about to become more complicated with the introduction of ultra-high NA immersion, potential use of frequency-doubling patterning techniques and indeed EUV. The long-established hardware approach is transformed through the addition of an increasingly strong soft content which modifies the center of gravity of lithography development towards a math-driven activity where optimization and metrology add to modeling and simulation as key to achieve practical manufacturing at and below 32nm. Complex algorithms become the common denominator and the drivers of the growing math-driven lithography.

They are present in all aspects of lithography, from design-based metrology algorithms to modeling, simulation, scanner and process optimization to determine realistic litho-aware design rules.

Will next generation lithography becoming a virtual lithography?

Our panel will explore the needs for advanced lithography developments and introduction into manufacturing from the perspective of a math-driven virtual algorithms compliant to next generation lithography. Participants include experts from semiconductor industry and universities.

Women in Optics Lunch

Tuesday Noon to 1:00 pm



Join us for an opportunity to network with other professionals at this lunch hosted by Roxann Engelstad, 2007 Symposium Chair. Register at the SPIE Cashier on-site by 3:00 pm Monday; location information provided upon sign-up.



Special Events

Nanotechnology in Microlithography Panel Discussion on

Metrology & Materials for Nanoimprint Lithography: Needs and Prospects

Convention Center C1

Tuesday 27 February 7:00 to 9:00 pm

Chairs: Michael T. Postek, Christopher L. Soles, National Institute of Standards and Technology

Sponsored by 

Nanoimprint is rapidly emerging as a patterning technique with enormous potential for not just the semiconductor industry, but also a range of technologies. The technique has the potential to couple the patterning resolution of e-beam lithography with the high-throughput of a stamping process, all in a low cost tool. However, there are several aspects of the nanoimprint process that differ significantly from state of the art optical lithography and these differences come with unique metrology challenges. Furthermore, the potential of a step-like jump in the patterning resolution offered by nanoimprint threatens to exacerbate many of the metrology challenges presently facing optical lithography. For nanoimprint lithography to emerge as an economically viable technology, the supporting metrology infrastructure must be developed. In this workshop our panel of experts will discuss these metrology needs, review the progress in addressing these challenges, and highlight areas that require further development. Audience participation in shaping these objectives will be encouraged.

About Nanotechnology

Nanotechnology is a strongly multidisciplinary area, and brings together the community of scientists and technologists working at the frontiers of nanoscience and nanotechnology. Basic and applied scientific as well as technological issues are of interest in the context of optics, electrical engineering, and materials science. The scope includes, but is not limited to, the following areas: nanoscale function and properties • nanoparticles, nanotubes, nanofilms and nanodeposits • nanomolecular and biomolecular materials; nanofabrication, characterization and metrology • control of nanoscale optical, mechanical, and electronic processes • transport and interaction in nanostructures • nanodevices, nanosensors and their applications; quantum wells, wires and dots • noise, dissipation and information transfer in nanoelectronic devices • molecular motors and nanomachines • ion pumps and ion channels • fluctuation-induced transport • quantum computing processes and devices photoactive arrays, materials and devices • nanophotonics; quantum and nonlinear optics in nanostructures • near-field optics, microscopy and associated technologies • colloidal systems, smart and self-assembled materials • environmental nanoparticles and aerosols • biomaterials and biophotonics.

Joint Sessions with Conferences 6520 and 6521

Computational Lithography

Convention Center A2

Wednesday 28 February 6:20 to 8:00 pm

Chairs: Alfred K. K. Wong, Magma Design Automation; Donis G. Flagello, ASML US, Inc.

The drive to push optical lithography beyond traditional limits is forcing the use of extremely aggressive OPC in conjunction with using DFM. In addition, various effects, such as mask topography need to be included in the correction solution furthering the complexity. The fundamental consequence is the increase in prominence of various computational issues associated with solutions for imaging correction. This joint session puts together various papers that highlight the issues associated with computational lithography.

Joint Sessions with Conferences 6517 and 6519

EUV Resists

Marriott San Jose Salon III

Wednesday 28 February 6:30 to 8:30 pm

EUV resists have been identified as one of the major challenges for the introduction of EUV lithography. In addition to the challenges facing resist resolution and line edge roughness, improved photospeed is required because of the limited output of EUV sources. Simultaneously meeting all three of these requirements will be challenging because of inherent shot noise limits. Therefore, new resist platforms may be required. This joint session provides a forum to discuss new developments in EUV resists and the prospects for availability of materials to support the introduction of EUV lithography.

Conference 6518 Panel Discussion

New Frontiers in Overlay Metrology

Convention Center C1

Wednesday 28 February 8:00 to 9:30 pm

Moderators: Timothy A. Brunner, IBM Thomas J. Watson Research Ctr.; Harry J. Levinson, Advanced Micro Devices, Inc.

Sponsored by 

We have entered a new era in overlay. Overlay measurements are about to become substantially further complicated with the introduction of double patterning techniques. In-chip overlay will need to be measured routinely in development and possibly in manufacturing. Target design directly affects overlay tool performance and the ability to accurately monitor overlay. New target designs are significantly more complicated from an optics and measurement perspective. Arrayed target designs, device size targets, in chip overlay, and dummy fill surrounded targets all introduce critical performance challenges. There is substantially reduced collaboration as a result of the trend to proprietary target designs. Do we need a new technology to achieve the advanced overlay requirements or an industry wide collaboration and standardization to move in a more unified direction?

The participants include experts from government laboratories and the semiconductor industry.

Student Lunch with the Experts – A Networking Event

Wednesday 28 February 12:30 to 1:30 pm

Seating is Limited, Tickets Required

Enjoy a casual meal and lively discussion with optics/lithography experts at this complimentary event. Hosted by SPIE Student Services this event will feature experts willing to share their accumulated wisdom on career paths within the optics and photonics industry. Take advantage of this opportunity to network with some of the best and brightest in the field including:

Dr. Ralph Dammel, AZ Electronic Materials USA Corp.

Dr. Harry Levinson, Advanced Micro Devices Inc.

Dr. Burn Lin, Taiwan Semiconductor Manufacturing Co Ltd

Dr. Qinghuang Lin, IBM Corp.

Dr. Michael Postek, NIST

...and more!

Students receive one complimentary ticket with registration.

Conference 6521 Panel Discussion

Design for Manufacturability: Open Mic Night

Convention Center C1

Thursday 1 March 7:30 to 9:00 pm

Moderator: Juan Antonio Carballo, IBM Corp.

Sponsored by 

Do you think DFM is “hot” but don’t know what it actually means? Do you think DFM is just old wine in new bottles? Do you think your 2 minute take on DFM is more interesting than all those formal papers? Then come to the Open Mic Panel on DFM, armed with your questions, ideas, and good humor. Transparencies, markers, and libations will be provided.

New Event!

NIST Workshop Critical Dimension Standards: The Past, Present, and Future

Convention Center B1

Thursday 1 March 7:00 to 9:00 pm

Moderator: **Ronald Dixson**, NIST—Precision Engineering Division

Linewidth or critical dimension (CD) has been an important measurand in semiconductor manufacturing metrology almost from the beginning. In the early days, though, it was sufficient to use metrology tools having an accurate scale calibration without sophisticated treatment of the edge detection. Consequently, the primary standards requirement was for traceable pitch standards.

As feature sizes became ever smaller, however, the unique edge-definition uncertainties involved in CD metrology became increasingly important—eventually necessitating the development of independent linewidth standards. Yet the problem of linewidth calibration is uniquely resistant to a universally applicable solution.

There have, however, been some notable successes for specific applications. In both the United States and Europe, National Metrology Institutes such as NIST (in the US) and PTB (in Germany) have developed photomask linewidth standards for optical metrology. The foundations of the NIST work were laid down in 80s by the late Diana Nyssonnen - who was a prominent member of the SPIE lithometrology community.

More recently, NIST - in close collaboration with SEMATECH and VLSI Standards - responded to the need for better linewidth standards by developing a specimen suitable for CD-AFM tip width calibration with 1 nm standard uncertainty. The samples were known as single crystal critical dimension reference materials (SCCDRM) and were distributed to SEMATECH member companies in late 2004.

At about the same time VLSI Standards introduced the NanoCDTM which is currently the only linewidth standard available commercially from the private sector. The NanoCDTM samples are also suitable for CD-AFM tip width calibration with comparable uncertainty to the SCCDRMs.

In close partnership with SEMATECH and VLSI Standards, NIST is continuing to push the boundaries of CD calibration and standards development. A “next generation” SCCDRM thrust was launched by NIST in 2005 with the goal of improving the technology and the user-friendliness of the samples.

Even more recently, NIST and VLSI Standards began working together on comparison studies of the SCCDRM and NanoCDTM technology. This work will provide a valuable scientific mutual validation on the results and might eventually lead to formal NIST accreditation of the NanoCDTM specimens.

In this workshop, we will review the scope and history of linewidth calibration standards, with an emphasis on work at NIST. The status and plans for the SCCDRM “next generation” will be reviewed - with ample opportunity for audience participation. The development and application of the NanoCDTM will be also discussed in presentations by both VLSI Standards and NIST.

Conference 6520: Best Student Paper Award

Convention Center A2

Friday 2 March 10:25 to 10:35 am

Sponsored by 

The Cymer Scientific Leadership Award for Best Student Paper, a monetary award to help support students engaged in research activities in optical microlithography, will be awarded this year again at the Optical Lithography conference. Student authors and student co-authors are eligible only. A panel of experts will be invited by the chair of the conference to serve as judges. The paper (oral or poster) demonstrating scientific excellence in presentation, quality and importance to the lithography community will be selected as the winner of this award.

Exhibitor Spotlights

Convention Center, Exhibition Hall 1, back of Aisle 200.

Tuesday

12:30 pm

The Benefits of AutoCal and AutoCD on PEB Profile and Critical DI CD's

Andrew Beers, OnWafer Technologies

Utilizing Gen4 BakeTemp SensorWafer and SmartFou-eZ Hardware we will demonstrate the ease and ability of OnWafers AutoCal and AutoCD software suite in improving Post Exposure Bake (PEB) Temperature Profile and Optimizing After Develop Inspect Critical Dimensions.

1:30 pm

Improved Yield Through Improved Leveling and Teaching

Dennis Bonciolini, CyberOptics Semiconductor

CyberOptics Semiconductor will discuss how wireless and wafer-like precision measurement devices (WaferSense™), for sensing, reporting and recording inclination or capable of target acquisition (utilizing machine vision technology) can improve tool performance to enhance yields in lithography areas.

2:30 pm

“EastaPure” Electronic Chemicals, Be Sure It’s Pure

Mike Quillen, Eastman Chemical Company

Stemming from its experience in high purity products Eastman is developing a next generation product used in the removal of contaminants in surface sensitive processes.

Wednesday

10:30 am

Nanoimprint solutions from Nanonex

Larry Koecher, Nanonex Corp.

Nanonex Corporation, the world leader in nanoimprint lithography, will discuss its current product offerings and solutions.

11:30 am

Wafer Based Metrology for Lithography Tools

Mei Sun, PhD, SensArray Corp.

Mei Sun will show several different configurations of instrumented wafers that can be used to characterize exposure systems, resist processing tracks, and etch patterning tools.

12:30 pm

Raith’s New Lithography Systems

George Lanzarotta, Raith USA, Inc.

Descriptions of Raith’s new lithography systems will be presented. Our new system components and improved specifications make for more complete nanotechnology workstations.

Course Daily Overview

Sunday	Monday	Tuesday	Wednesday	Thursday
Emerging Lithographic Technologies				
<p>SC100 Introduction to Electron-Beam Lithography (<i>McCord</i>) 8:30 am to 12:30 pm, \$280 / \$325</p> <p>SC101 Introduction to Microlithography: Theory, Materials, and Processing (<i>Bowden, Thompson, Willson</i>) 8:30 am to 5:30 pm, \$530 / \$615</p> <p>SC830 Recent Advances in Electron Beam Lithography (<i>Pfeiffer</i>) 1:30 to 5:30 pm, \$280 / \$325 NEW!</p> <p>SC622 Nano-Scale Patterning with Imprint Lithography (<i>Sreenivasan, Willson, Resnick</i>) 6:00 to 10:00 pm, \$280 / \$325</p>				
Metrology, Inspection, and Process Control				
<p>SC105 CD Metrology and Image Formation in the Scanning Electron Microscope (SEM) (<i>Wells, Postek</i>) 8:30 am to 5:30 pm, \$460/\$545</p> <p>SC705 Instruments and Methodologies for Accurate Metrology and Fleet Matching (<i>Archie, Banke</i>) 8:30 am to 5:30 pm, \$460 / \$545</p> <p>SC101 Introduction to Microlithography: Theory, Materials, and Processing (<i>Bowden, Thompson, Willson</i>) 8:30 am to 5:30 pm, \$530 / \$615</p> <p>SC831 Introduction to Scatterometry Metrology: Theory and Application (<i>Bao, Barry</i>) 1:30 to 5:30 pm, \$280 / \$325 NEW!</p>			<p>Register at the SPIE Cashier!</p>	
Resist Technology and Processing				
<p>SC101 Introduction to Microlithography: Theory, Materials, and Processing (<i>Bowden, Thompson, Willson</i>) 8:30 am to 5:30 pm, \$530 / \$615</p> <p>SC780 Tracks 101: Microlithography Coat and Develop Basics (<i>Daggett, Williams</i>) 8:30 am to 5:30 pm, \$460 / \$545</p> <p>SC355 Fundamentals of Photochemical Contamination Control for Lithographic Tools (<i>Kunz</i>) 6:00 to 10:00 pm, \$280 / \$325</p> <p>SC833 Lithography Integration for Semiconductor Back-End-Of-The-Line (BEOL), (<i>Lin</i>) 8:30 am to 12:30 pm, \$280 / \$325</p>			<p>SC103 Resists for Deep UV Lithography (<i>Willson</i>) 8:30 am to 5:30 pm, \$460 / \$545</p> <p>SC616 Practical Photoresist Processing (<i>Dammel</i>) 1:30 to 5:30 pm, \$280 / \$325</p>	
The Business Side				
		<p>SC832 IP Issues in Advanced Lithography and Semiconductor Manufacturing (<i>Gortych</i>) 1:30 to 5:30 pm, \$280 / \$325 NEW!</p>		

Optical Microlithography

SC120 193-nm Photoresist Materials (Dammel) 8:30 am to 12:30 pm, \$280 / \$325

SC540 Applying Optical Proximity Correction and Design for Manufacturability to Product Designs (Capodiceci, Lucas) 8:30 am to 5:30 pm, \$460 / \$545

SC707 Basics of Optical Imaging in Microlithography: A Hands-on Approach (Milster, Flagello, Brooker) 8:30 am to 12:30 pm, \$280 / \$325

SC105 CD Metrology and Image Formation in the Scanning Electron Microscope (SEM) (Wells, Postek) 8:30 am to 5:30 pm, \$460 / \$545

SC705 Instruments and Methodologies for Accurate Metrology and Fleet Matching (Archie, Banke) 8:30 am to 5:30 pm, \$460 / \$545

SC101 Introduction to Microlithography: Theory, Materials, and Processing (Bowden, Thompson, Willson) 8:30 am to 5:30 pm, \$530 / \$615

SC116 Lithographic Optimization: A Theoretical Approach (Mack) 8:30 am to 5:30 pm, \$460 / \$545

SC117 The Fundamental Limits of Optical Lithography (Smith) 8:30 am to 12:30 pm, \$395 / \$440

SC706 Imaging and Optics Fundamentals in Microlithography (Flagello) 1:30 to 5:30 pm, \$280 / \$325

SC124 Pushing the Limits: Optical Enhancement, Polarization, and Immersion Lithography (Smith) 1:30 to 5:30 pm, \$280 / \$325

SC355 Fundamentals of Photochemical Contamination Control for Lithographic Tools (Kunz) 6:00 to 10:00 pm, \$280 / \$325

SC102 Optical Lithography Modeling (Neureuther, Smith) 6:00 to 10:00 pm, \$315 / \$360

SC833 Lithography Integration for Semiconductor Back-End-Of-The-Line (BEOL), (Lin) 8:30 am to 12:30 pm, \$280 / \$325

SC779 Polarization for Lithographers (Kye, McIntyre) 8:30 am to 12:30 pm, \$280 / \$325

SC579 Photomask Fabrication and Technology Basics (Duff) 8:30 am to 5:30 pm, \$460 / \$545

SC834 Lithography Friendly Design and Beyond - A Broader Review of DfM (Liebmann, Mansfield, Wong) 8:30 am to 5:30 pm, \$460 / \$545

NEW!

SC118 Anti-Reflective Coatings: Theory and Practice (Dammel) 8:30 am to 12:30 pm, \$280 / \$325

New Courses at Advanced Lithography 2007

Don't miss these cutting-edge additions to this year's Professional Development program.

- Recent Advances in Electron Beam Lithography
- Introduction to Scatterometry Metrology: Theory and Application
- IP Issues in Advanced Lithography and Semiconductor Manufacturing
- Lithography Integration for Semiconductor Back-End-Of-The-Line (BEOL)
- Lithography Friendly Design and Beyond— A Broader Review of DfM

Register at the SPIE Cashier!

Design for Manufacturing

SC540 Applying Optical Proximity Correction and Design for Manufacturability to Product Designs (Capodiceci, Lucas) 8:30 am to 5:30 pm, \$460 / \$545

SC105 CD Metrology and Image Formation in the Scanning Electron Microscope (SEM) (Wells, Postek) 8:30 am to 5:30 pm, \$460 / \$545

SC705 Instruments and Methodologies for Accurate Metrology and Fleet Matching (Archie, Banke) 8:30 am to 5:30 pm, \$460 / \$545

SC778 Introduction to Advanced Process Control (APC) for Semiconductor Manufacturing (Misra) 8:30 am to 5:30 pm, \$460 / \$545

SC116 Lithographic Optimization: A Theoretical Approach (Mack) 8:30 am to 5:30 pm, \$460 / \$545

SC833 Lithography Integration for Semiconductor Back-End-Of-The-Line (BEOL), (Lin) 8:30 am to 12:30 pm, \$280 / \$325

NEW!

SC505 Data to Silicon: Understanding the Fundamentals of MDP, Frame Generation, RET and DFM (Morse) 8:30 am to 5:30 pm, \$460 / \$545

SC834 Lithography Friendly Design and Beyond - A Broader Review of DfM (Liebmann, Mansfield, Wong) 8:30 am to 5:30 pm, \$460 / \$545

NEW!

SC708 Impact Of Variability On VLSI Circuits (Puri, Gupta) 1:30 to 5:30 pm, \$280 / \$325

Dont miss the exhibition!

SPIE *Advanced* Lithography

San Jose Convention Center, Exhibit Halls 1 & 2

Tuesday, 27 February . . . 10:00 am to 5:00 pm

Wednesday, 28 February 10:00 am to 4:00 pm

Abeam Technologies	Intel Corp.
Aerotech, Inc.	International Radiation Detectors, Inc.
Air Products and Chemicals, Inc.	Invarium Inc.
Anchor Semiconductor Inc.	J.A. Woollam Co.
Applied Materials, Inc.	JCMwave GmbH
ASML US, Inc.	JSR Micro, Inc.
ATMI, Inc.	King Industries Inc.
AZ Electronic Materials USA Corp.	KLA-Tencor Corp.
Benchmark Technologies	Laser Focus World
Braggong Oy	Lasertec USA Inc.
Brewer Science, Inc.	LINOS Photonics, Inc.
Brion Technologies, Inc.	Media Lario Technologies
Cadence Design Systems, Inc.	Mentor Graphics Corp.
Carl Zeiss SMT Inc.	Mercury Computer Systems, Inc.
Corning Inc.	MetroBoost
CUNO Inc.	Metrosol, Inc.
CVI Laser, LLC	Micro Lithography, Inc.
Cyantek Corp.	MicroChem Corp.
CyberOptics Semiconductor	Microlithography World
Cymer, Inc.	Micronic Laser Systems AB
Digital Optics Corp.	Mitsui Chemicals America, Inc.
DNS Electronics, LLC	Molecular Imprints, Inc.
Donaldson Co., Inc.	n&k Technology, Inc.
Dongjin Semichem Co., Ltd.	Nanometrics Inc.
Eastman Chemical Co.	Nanonex Corp.
Energetiq Technology, Inc.	National Institute of Standards and Technology
Entegris, Inc.	New Focus, Inc.
EV Group Inc.	Nikon Precision Inc.
Foothill Instruments, LLC	OBDUCAT AB
FUJIFILM Electronic Materials U.S.A., Inc.	Olympus Surgical & Industrial America Inc.
Gigaphoton Inc.	OnWafer Technologies, Inc.
Gudeng Precision Industrial Co., Ltd.	ORC Manufacturing Co., Ltd.
Hakuto Co., Ltd.	Osram Sylvania Products, Inc.
Halocarbon Product Corp.	Pall Corp.
Hitachi High Technologies America, Inc.	Particle Measuring Systems, Inc.
Honeywell Electronic Materials	Photonics Spectra
HORIBASTEC	Photronics Inc.
Inko Industrial Corp.	



Pixer Technology Ltd.	Sumika Electronic Materials, Inc.
Pozzetta Products, Inc.	Surface Finishes
Queensgate Instruments Ltd.	SUSS MicroTec Inc.
Rainbow Research Optics, Inc.	Synopsys, Inc.
Raith USA, Inc.	SynQuest Labs., Inc.
RAVE LLC	Technical Manufacturing Corp.
Renishaw Inc.	The Precision Alliance
Rohm and Haas Electronic Materials	Timbre Technologies, Inc.
RSoft Design Group, Inc.	Tokyo Ohka Kogyo America, Inc.
Rudolph Technologies, Inc.	Toppan Photomasks, Inc.
SAES Pure Gas, Inc.	Transfer Devices, Inc.
Sagantec North America	USHIO America, Inc.
SAGEM SA	Veeco Instruments
Semiconductor International Magazine	Vistec Semiconductor Systems, Inc.
SensArray Corp.	VLSI Standards, Inc.
Shin-Etsu MicroSi, Inc.	Wacom Corp.
Solid State Technology	XEI Scientific, Inc.
SPIE Industry Resources	Yield Engineering Systems Inc.
Star Tech Instruments	Zygo Corp.
Steinmeyer, Inc.	

SPIE Advanced Lithography 2007

San Jose Convention Center
408 Almaden Blvd., San Jose, CA, 95110
San Jose Marriott (Headquarters Hotel)
301 South Market Street, San Jose, CA, 95113

Registration and Information Hours

25 February–2 March 2007

San Jose Convention Center, Exhibit Hall 2

Sunday 25 February 7:00 am to 6:00 pm
Monday 26 February 7:00 am to 4:00 pm
Tuesday 27 February through
Thursday 1 March 7:30 am to 5:00 pm
Friday 2 March 7:30 am to 11:00 am

Poster Receptions

Convention Center Exhibit Hall 3

Monday 26 February 5:30 to 8:00 pm
(Conf. 6518, 6519)

Hors d'oeuvres sponsored by 

Beer and Wine sponsored by 

Thursday 1 March 5:30 to 8:00 pm
(Conf. 6517, 6520, 6521)

Beer and Wine sponsored by 

Conference attendees are invited to the poster sessions and receptions. Authors of poster papers will be on hand during these sessions to answer questions and provide in-depth discussion concerning their papers. Since poster sessions are technical events and part of the conference program, it is not appropriate for spouses and families to attend these events. Attendees are requested to wear their conference registration badges to the poster sessions.

For the poster session on Monday 26 February, poster authors can set up their posters after 10:30 am. For the Thursday poster session, the author can set-up after 9:00 am. Poster supplies (push-pins) will be available. Poster can be previewed during the day before the formal poster sessions begin at 5:30 pm.

Authors must remove their posters at the conclusion of the poster reception for that day. It is the authors' responsibility to remove their posters. Posters not removed will be considered unwanted and will be discarded. SPIE assumes no responsibility for posters left up after the end of each night's poster reception.

Exhibition Hours

Convention Center Exhibit Halls 1-2

Tuesday 27 February 10:00 am to 5:00 pm
Wednesday 28 February 10:00 am to 4:00 pm

Over 130 leading Advanced Lithography companies showcase the latest products and technologies in the industry. The current exhibitor list and floor plan is available on-line at www.spie.org/exhibitions.

There is no charge to visit the exhibition hall; however, a registration badge is required for admittance. Pre-registration and on-site registration are available for exhibition-only visitors.

Coffee Breaks

Sponsored by  **ASML** 

 **AZ Electronic Materials**

Coffee will be served during the morning and afternoon break. Please check the individual technical conference listings for exact times.

Monday 26 February 10:30 to 11:00 am; 3:00 to 4:00 pm
Convention Center, Concourse 2 Lobby

Tuesday 27 February–
Wednesday 28 February 10:00 to 11:00 am; 3:00 to 4:00 pm
Convention Center, Exhibition Halls 1-2

Thursday 1 March 10:00 to 11:00 am; 3:00 to 4:00 pm
Convention Center, Concourse 2 Lobby

Friday 2 March 10:00 to 11:00 am
Convention Center, Concourse 2 Lobby

Breakfast Breads

Sponsored by 

Breakfast breads and coffee will be served from 7:30 to 8:30 am Monday through Friday for Symposium attendees in the Convention Center, Concourse 2 Lobby.

Desserts

Sponsored by  **JSR Micro** 

Desserts will be served in the exhibition halls 1-2, on Tuesday and Wednesday, 3:00 to 4:00 pm.

Lunch Coupons

Tuesday lunch sponsored by **TOPPAN**

Full conference registrants will receive a lunch coupon redeemable towards a luncheon purchased Tuesday and Wednesday at designated areas in the Exhibition Hall. Coupons will be accepted from 11:30 am to 1:30 pm both days. Some restrictions apply; please refer to the coupons in your registration packet.

Internet Access

Convention Center - Concourse

Sunday 25 February - Thursday 1 March . . . during registration hours

Sponsored by 

At this location will be multiple workstations allowing attendees to access their internet e-mail during the conference, and several Ethernet connections to use with your personal laptop. There will be a 10-minute time limit per each person's internet session.

WiFi Access

Sponsored by  **TOKYO ELECTRON**

Complimentary WiFi access for attendees with wireless-enabled laptops and PDAs will be available Monday through Friday in the Ballroom Concourse (east end) of the Convention Center near the SPIE Marketplace and Internet Pavilion.

General Information

Speaker Audiovisual Desk / Preview Station

Convention Center, "Room D"

Sunday 25 February 2:00 to 6:00 pm
Monday 26 February through Thursday 1 March . 7:30 am to 5:00 pm
Friday 2 March 7:30 am to 12:00 pm

Course Materials Desk

Located in the registration area.

Open during registration hours.

If you have registered to attend a short course, please stop by the Course Materials Desk to pick up your course notes and to find out where the class will be located. You may also get a copy of the latest Education Services catalog to see the many courses SPIE has available at symposia, on video and CD-ROM, and to discover the opportunities of customized In-Company courses.

Exhibition Concession Stands

For those whose registration plan does not include the lunch coupons, or for obtaining food and beverage at other than lunch times, concession stands located in the halls will be open during exhibition hours. They will serve hot and cold snacks, beverages, deli-style sandwiches, salads, a few hot entrees, and pastries.

SPIE Copy Center

Sunday through Thursday during registration hours SPIE will provide a copy service during the week for symposium attendees. The rates are 5 cents/copy and \$1 per transparency. Located near registration in Exhibit Hall 2.

Oral Presentation Instructions

SPIE will provide a computer, projector, lapel microphone, and laser pointer for the Advanced Lithography 2007 Conferences. Authors are asked to check in at the Speakers Presentation Room, "Room D" San Jose Convention Center prior to the beginning of their session to confirm compatibility. Speakers that did not pre-request special audiovisual equipment are asked to stop at the Audiovisual Desk upon arrival to see if these special requests can be fulfilled.

Oral presentations are best presented in PowerPoint or Adobe Acrobat PDF formats. Presentations can be accepted on pen drive, CD-Rom, or directly from your own laptop.

SPIE will email/fax the contact authors with audiovisual details (be sure SPIE has your current email address by contacting abstract_help@spie.org).

Audiovisual questions can be emailed to AVStaff@SPIE.org.

IMPORTANT LASER POINTER SAFETY INFORMATION

- SPIE supplies tested and safety approved laser pointers for all conference meeting rooms, and for short course rooms if instructors request one. For safety reasons, SPIE requests that presenters use our provided laser pointers available in each meeting room.
- If using your own laser pointer, have it tested at your facility to make sure it has <5 mW power output. Laser pointers in Class II and IIIa (<5 mW) are eye safe if power output is correct - but don't automatically trust the labeling. Commercially available laser pointers, red or green (or any color), could be incorrectly labeled as to their wavelength and power output.
- Presenters intending to use their own laser pointer for presentations are required to come to the Audiovisual Desk onsite and test their pointer on our power meter. If the pointer fails the safe power level you may not use the pointer at the conference. You will be required to sign a waiver releasing SPIE of any liability for use of potentially non-safe laser pointers.
- Use of a personal laser pointer at an SPIE event represents user's acceptance of liability for use of a non-SPIE supplied laser pointer device. Misuse of any laser pointer could lead to eye damage. In California, it is a criminal misdemeanor to shine a laser pointer at individuals "who perceive they are at risk."

Poster Author Instructions

Authors can set up their scheduled posters on Monday after 10:30 am and on Thursday after 9:00 am, the day of their poster session. Poster supplies (Push-pins) will be available. Other supplies can be obtained from the Presenter Check-in Desk. Poster can be previewed during the day before the formal poster sessions begin at 5:30 pm.

Authors must remove their posters at the conclusion of the poster reception for that day. It is the authors' responsibility to remove their posters. Posters not removed will be considered unwanted and will be discarded. SPIE assumes no responsibility for posters left up after the end of each night's poster reception.

Audio/Video/Digital Recording Policy

Due to copyright restrictions, strictly no recordings of any kind are permitted without prior written consent of the presenter in any conference session, short course or posters. Consent forms are available at the SPIE Audiovisual Desk and anyone wishing to record must have a written consent form signed and filed for each presenter being recorded. Individuals not complying with this policy will be asked to leave a given session and to surrender their film or disc.

In the Exhibition Hall: For security and courtesy reasons, photographing or videotaping individual booths and displays in the exhibit hall is allowed ONLY with explicit permission from on-site company representatives. Individuals not complying with this policy will be asked to surrender their film and to leave the exhibition hall.

Underage Persons on Show Floor

For safety and insurance reasons, no persons under the age of 16 will be allowed in the exhibition area during move-in and move-out. During open exhibition hours, only children over the age of 12 accompanied by an adult will be allowed in the exhibition area.

Photography

Personal photographs and video taping of individual booths (and their displays) is not allowed without the explicit permission from the company representative on-site. Failure to obtain consent could result in losing your film and being asked to leave the Exhibition Hall.

Message Center

Convention Center, located near registration

Messages will be taken during registration hours Sunday through Thursday by calling: 408-271-6200. Attendees should check the message boards at the message center on a daily basis to receive their messages.

SPIE Marketplace

The SPIE Marketplace is your source for the latest SPIE Press books, Proceedings, and Educational and Professional Development materials. You can become a member of SPIE, explore the Digital Library, and take home a souvenir.

Membership

SPIE Members, through their collective talents, influence the future of optical, technical, and scientific discovery.

Take advantage of SPIE Member benefits:

- Online Journal subscription
- Digital Library discount
- SPIE Professional Member magazine
- Involvement in the Society
- Discounts on publications, and conference and course registrations

Join now: spie.org/membership

Advanced Lithography Media Center

The on-site Media Center provides press conference facilities, refreshments, and convenient one-stop-shopping for press releases. Credentialed media are invited to communicate news via the provided telephone and computer connections. Registration and exhibition fees are waived for credentialed media representatives. You are encouraged to pre-register by e-mailing: name, organization, title, address, e-mail, and phone number to media@spie.org. For more information about SPIE media services, see <http://spie.org/info/media>

Child Care

A few child sitting services available in San Jose are as follows.

1. Bay Area 2nd MOM Inc., Hotel Nanny Service, Toll Free Phone: 1-888-926-3666, or (650) 858-2469, ext. 109. Fax: (650) 493-6598, Email: oncall@2ndmom.com or parentcounselor@2ndmom.com, Website: www.2ndmom.com
2. Sitters Unlimited: Toll Free Phone: (408) 452-0225, E-mail: info@bayareasittersunlimited.com or www.bayareasittersunlimited.com

Note: SPIE does not imply an endorsement or recommendation of these services. They are provided on an "information-only" basis for your further analysis and decision. Other services may be available.

Sightseeing / Shopping / Restaurants

Visit San Jose's visitor site online at: <http://www.photonics.sanjose.org>

Also, the San Jose Convention and Visitors Bureau will be operating an Information Desk on the street level of the Convention Center near the main entrance. They will be open during core hours of the convention and will be able to help attendees with lodging, sightseeing, shopping, and restaurant arrangements.

Car Rental



Hertz Car Rental has been selected as the official car rental agency for this Symposium. To reserve a car, identify yourself as a **Advanced Lithography Conference attendee** using the **Hertz Meeting Code CV# 029B0010**. Call **1 800 654 2240**.

Shuttles, Taxis and Limo Services

From San Jose International Airport (3 miles) to downtown San Jose Hotels & Convention Center

Carrier Rate (subject to change)

The South and East Bay Airport Shuttle: \$19.00 for the first person and \$6.00 for each additional person in the same group, one way. Credit cards, cash & local checks accepted (408) 225-4444 or from courtesy phone in the baggage area dial #66; shuttle arrives within 15-20 minutes. www.sjc.org

Taxi: \$15 - \$20. Credit cards or cash. No checks. Rate is an estimate and fares can vary with traffic conditions. Rates are per taxi, not per person www.sjc.org

From San Francisco International Airport to San Jose Convention Center or downtown San Jose Hotels (1 hour)

Carrier Rate (subject to change)

Airport Commuter Limo Service: Lincoln exec town car flat rate \$85 + \$15% tax + gratuity 15-20% Arrivals from 10 pm to 6 am, add \$10 - \$30 based on arrival time. **Reservations required 24 hours in advance.** Cash or credit cards accepted (no checks) 1-888-876-1777 or 650-876-1777 24 hrs/day, 7 days/wk. www.airportcommuter.com. Up to three passengers can ride for the price of one; maximum 3 per car.

The South and East Bay Airport Shuttle: \$34.00 for the first person and \$6.00 for each additional person in the same group, one way. Credit cards, cash & local checks accepted. From SFO 408-225-4444. From SJC 1-800-548-4664. www.flysfo.com Call from Baggage claim area; shuttle picks up in 10-20 min.

Taxi: \$134(+ gratuity)one way Credit cards or cash (no checks). Rate is an estimate and fares can vary with traffic conditions. Rates are per taxi, not per person. www.flysfo.com

From San Francisco International Airport To San Jose International Airport(1 hour 15 minutes)

Carrier Rate (subject to change)

The South and East Bay Airport Shuttle: \$37.00 for the first person and \$6.00 for each additional person. Credit cards, cash & local checks accepted. From SFO 408-225-4444. From SJC 1-800-548-4664. www.flysfo.com. Call from Baggage claim area; shuttle picks up in 10-20 min.

Airport Commuter Limo Service: Lincoln exec town car flat rate \$85 + \$15% tax + grats 15-20%. Arrivals from 10 pm to 6 am, add \$10 - \$30 based on arrival time. **Reservations are required 24 hours in advance.** Cash or credit cards (no checks). 1-888-876-1777 or 650-876-177724 hrs/day, 7 days/wk. www.airportcommuter.com. Up to three passengers can ride for the price of one; maximum 3 per car.

Taxi: \$124 Estimate based on traffic conditions. Credit cards or cash (no checks). Rates are per taxi, not per person. www.flysfo.com

General Information

Parking

<http://www.sjdowntownparking.com>

(click on the area on the corner of San Carlos and Woz Way)

At the Convention Center

\$14 per day for 24 hours with no in/out privileges.
\$20 with in/out privileges. 650 spaces for public use.

Alternate Parking Downtown San Jose - River Park Tower Garage

\$1.25 per 20 minutes, \$18 daily maximum. Rates and hours subject to change without notice. Click on link below for all alternate parking lots.

http://www.sjdowntownparking.com/parking_map.php

Located on the corner of San Carlos and Woz Way, 333 W. San Carlos St. 1,000 spaces available. Open 6:30 am to 12:00 midnight, Mon to Frid, 8:00 am to 12 midnight Sat; (Sunday varies).

Parking at the Downtown Hotels

HOTEL RATES: Rates are subject to change without notice.

FAIRMONT HOTEL: No self-parking available. Valet parking for **overnight guests** (on space-available basis) is \$24 with in/out privileges. Valet parking for **visitors** (on space-available basis): 1st 30 min is \$5, each additional 20 minutes is \$1.50, maximum per day is \$24. Parking garage is beneath the hotel

MARRIOTT HOTEL: Parking for guests is available for \$21 per day with in/out privileges. Non-guests pay \$4.00 per hour with a maximum of \$21/day.

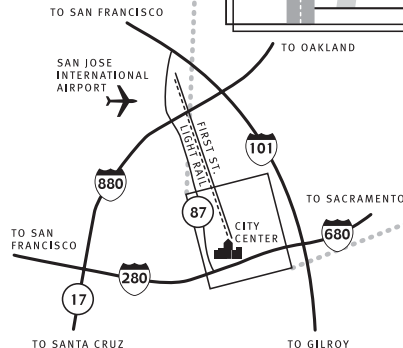
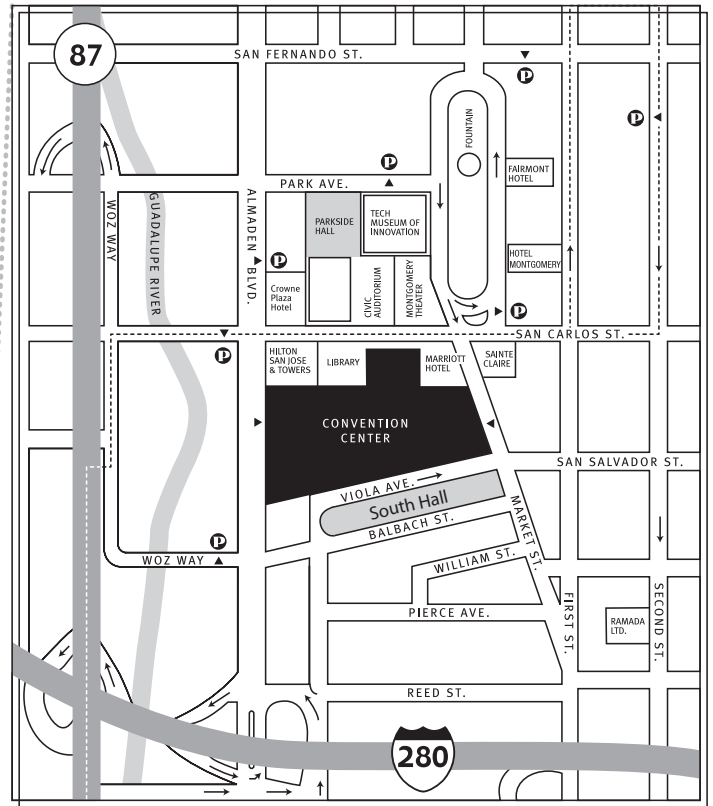
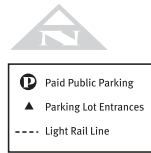
HILTON SAN JOSE & TOWERS: For Guests Self-parking \$14 max. with in/out privileges Valet-parking \$19 max. with in/out privileges & with validation at City Bar & Grille, \$8 for up to 5 hrs. For Non-Guests Self-parking - \$6 for 1st hr., \$1 each add'l 30 min up to 7 hrs with a max of \$18 per 12 hr. period. Valet parking - \$8 for up to 1st hr, \$12 1-2 hrs, \$18 2-5 Hrs, \$20 over 5 hrs, & with validation from City Bar & Grille, \$8 for up to 5 hrs.

CROWNE PLAZA: For Guests - self-parking, \$14 per day (subject to change) with in/out privileges. No valet. For non-guests - \$6. for 1st hr., \$1. every half hr. thereafter - max. \$20 per day.

SAINTE CLAIRE: For Guests only, valet parking only for \$18 overnight. In/out privileges are available to guests who charge their parking to their room.

RAMADA LTD.: Guest parking is complimentary.

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SPIE



Emerging Lithographic Technologies XI

Conference Chair: **Michael J. Lercel**, SEMATECH, Inc. and IBM Corp.

Cochair: **Franklin M. Schellenberg**, Mentor Graphics Corp.

Program Committee: **David T. Attwood, Jr.**, Lawrence Berkeley National Lab. and Univ. of California/Berkeley; **Vivek Bakshi**, SEMATECH, Inc.; **Michael Goldstein**, Intel Corp.; **Timothy R. Groves**, Vistec Lithography Ltd. (United Kingdom); **Woo-Sung Han**, SAMSUNG Electronics Co., Ltd. (South Korea); **Hiroichi Kawahira**, Sony Corp. (Japan); **Bruno M. La Fontaine**, Advanced Micro Devices, Inc.; **J. Alexander Liddle**, Lawrence Berkeley National Lab.; **Hans Loeschner**, IMS Nanofabrication GmbH (Austria); **R. Scott Mackay**, Consultant; **Pawitter J. Mangat**, Motorola, Inc.; **Christie R. K. Marrian**, Spansion LLC; **Anthony E. Novembre**, Lucent Technologies; **Laurent Pain**, CEA-LETI (France); **Kazuaki Suzuki**, Nikon Corp. (Japan); **William M. Tong**, Hewlett-Packard Co.

Tuesday 27 February

Introduction

Room: Conv. Ctr. B1 Tues. 8:00 to 8:10 am

Chair: **Michael J. Lercel**, SEMATECH, Inc.

SESSION 1

Room: Conv. Ctr. B1 Tues. 8:10 to 10:10 am

Keynote Session

Chair: **Frank M. Schellenberg**, Mentor Graphics Corp.

Keynote Presentation 8:10 am: Milliped probe-based storage (<i>Invited Paper</i>), M. Despont, IBM Corp. (Switzerland) [6517-01]
Keynote Presentation 8:50 am: Optical meta-materials at IR wavelength fabricated by nanoimprint lithography (<i>Invited Paper</i>), W. Wu, Hewlett-Packard Labs.; E. Kim, Univ. of California/Berkeley; E. Ponziovskaya, Hewlett-Packard Labs.; Y. Liu, Univ. of California/Berkeley; Z. Yu, A. M. Bratkovski, Hewlett-Packard Labs.; N. X. Fang, Univ. of Illinois at Urbana-Champaign; X. Zhang, R. Shen, Univ. of California/Berkeley; S. Wang, R. S. Williams, Hewlett-Packard Labs. [6517-02]
Keynote Presentation 9:30 am: Drop on demand (<i>Invited Paper</i>), TBA [6517-03]

Coffee Break 10:10 to 10:40 am

SESSION 2

Room: Conv. Ctr. B1 Tues. 10:40 am to 12:20 pm

EUV Systems

Chair: **Woo-Sung Han**, SAMSUNG Electronics Co., Ltd. (South Korea)

10:40 am: **SEMATECH's EUV program: a key enabler for EUVL introduction**, S. Wurm, C. Jeon, M. J. Lercel, SEMATECH, Inc. . [6517-04]

11:00 am: **EUV lithography with the Alpha Demo Tools: status and challenges**, N. Harned, ASML Wilton; M. Goethals, IMEC (Belgium); R. Groeneveld, ASML Netherlands B.V. (Netherlands); P. Kuerz, M. Lowisch, Carl Zeiss SMT AG (Germany); H. Meijer, H. Meiling, ASML Netherlands B.V. (Netherlands); K. G. Ronse, IMEC (Belgium); J. Ryan, M. D. Tittnich, Albany NanoTech; H. Voorma, ASML Netherlands B.V. (Netherlands); J. D. Zimmerman, ASML Wilton [6517-05]

11:20 am: **Nikon EUVL development progress update**, T. Miura, K. Murakami, K. Suzuki, Y. Kohama, K. Morita, K. Hada, Y. Ohkubo, Nikon Corp. (Japan) [6517-06]

11:40 am: **Path to the HVM in EUVL through the development and evaluation of the SFET**, S. Uzawa, H. Kubo, Y. Miwa, H. Tsuji, H. Morishima, Canon Inc. (Japan) [6517-07]

12:00 pm: **EUV lithography program at IMEC**, A. Goethals, R. M. Jonckheere, G. F. Lorusso, J. Hermans, K. G. Ronse, IMEC (Belgium) [6517-08]

Lunch/Exhibition Break 12:20 to 1:50 pm

SESSION 3

Room: Conv. Ctr. B1 Tues. 1:50 to 3:30 pm

Advanced Mask I

Chairs: **Emily E. Gallagher**, IBM Microelectronics Div.; **Timothy R. Groves**, Vistec Lithography Ltd. (United Kingdom)

1:50 pm: **Fast simulation of buried EUV mask defect interaction with absorber features**, C. H. Clifford, A. R. Neureuther, Univ. of California/Berkeley [6517-09]

2:10 pm: **EUV MET printing and actinic imaging analysis on the effects of phase defects in wafer CDs**, H. Han, SEMATECH, Inc. and Samsung Electronics Co., Ltd. (South Korea) [6517-10]

2:30 pm: **EUV and non-EUV inspection of reticle defect repair sites**, K. A. Goldberg, Lawrence Berkeley National Lab.; A. Barty, Lawrence Livermore National Lab.; P. Seidel, SEMATECH, Inc.; R. Fettig, NaWoTec GmbH; P. A. Kearney, H. Han, O. R. Wood II, SEMATECH, Inc. . [6517-11]

2:50 pm: **EUV mask-blank inspection at the SEMATECH Mask Blank Development Center with the Lasertec M7360**, W. Cho, P. A. Kearney, SEMATECH, Inc.; E. M. Gullikson, Lawrence Berkeley National Lab.; A. Jia, SEMATECH, Inc.; T. Tamura, A. Tajima, H. Kusunose, Lasertec Corp. (Japan); C. Jeon, SEMATECH, Inc. [6517-12]

3:10 pm: **EUVL mask substrate defect print study**, J. Cullins, Y. Tezuka, I. Nishiyama, Association of Super-Advanced Electronics Technologies (Japan) [6517-13]

Coffee Break 3:30 to 4:00 pm

Sessions 4 and 5 run concurrently.

SESSION 4

Room: Conv. Ctr. B1 **Tues. 4:00 to 5:40 pm**

EUV Optics

Chair: Patrick P. Naulleau, Lawrence Berkeley National Lab.

- 4:00 pm: **Atomic hydrogen cleaning of Ru-capped EUV multilayer mirror**, K. Motai, H. Oizumi, S. Miyagaki, I. Nishiyama, Association of Super-Advanced Electronics Technologies (Japan); A. Izumi, T. Ueno, Y. Miyazaki, A. Namiki, Kyushu Institute of Technology (Japan) [6517-14]
- 4:20 pm: **Critical parameters influencing the EUV-induced damage of Ru-capped multilayer mirrors**, S. B. Hill, I. Ermanoski, C. Tarrío, T. B. Lucatorto, National Institute of Standards and Technology; T. E. Madey, Rutgers Univ.; M. Chandhok, M. Fang, Intel Corp. [6517-15]
- 4:40 pm: **Sn cleaning methods for extended collector life time: an innovative approach for successful EUV lithography**, S. N. Srivastava, H. J. Shin, D. N. Ruzic, Univ. of Illinois at Urbana-Champaign ... [6517-16]
- 5:00 pm: **Interface engineering of Mo/Si multilayers for enhanced reflectance in EUVL applications**, A. E. Yakshin, R. van de Kruij, I. Nedelcu, E. Zoethout, E. Louis, F. Bijkerk, FOM-Instituut voor Plasmafysica Rijhuizen (Netherlands) [6517-17]
- 5:20 pm: **Development of optics for EUV lithography tools**, K. Murakami, T. Oshino, H. Kondo, H. Chiba, H. Komatsuda, K. Nomura, H. Iwata, Nikon Corp. (Japan) [6517-18]

SESSION 5

Room: Conv. Ctr. C1 **Tues. 4:00 to 5:20 pm**

NIL I

Chairs: William M. Tong, Hewlett-Packard Co.; **Pawitter J. Mangat**, Motorola, Inc.

- 4:00 pm: **Multilevel step and flash imprint lithography for direct patterning of dielectrics**, F. L. Palmieri, W. Jen, M. D. Stewart, The Univ. of Texas/Austin; J. Owens, J. T. Wetzel, Advanced Technology Development Facility, Inc.; J. Hao, Y. Nishimura, B. Li, H. Chao, P. S. Ho, G. Willson, The Univ. of Texas/Austin [6517-19]
- 4:20 pm: **A study of imprint-specific defects in the step and flash imprint lithography process**, J. Perez, F. Y. Xu, I. McMackin, P. Schumaker, S. V. Sreenivasan, Molecular Imprints, Inc. [6517-20]
- 4:40 pm: **Critical issues study of nano-imprint tool for semiconductor volume production**, H. Ina, Canon Inc. (Japan) [6517-21]
- 5:00 pm: **Imprint time optimization in hot embossing lithography**, T. Leveder, S. Landis, Lab. d'Electronique de Technologie de l'Information (France); L. Davoust, École Nationale Supérieure d'Hydraulique et de Mécanique de Grenoble (France) [6517-22]

Wednesday 28 February**SESSION 6**

Room: Conv. Ctr. B1 **Wed. 8:00 to 10:00 am**

EUV Source I

Chair: Vivek Bakshi, SEMATECH, Inc.

- 8:00 am: **Laser-produced EUV light source development for HVM**, A. Endo, H. Hoshino, T. Ariga, T. Miura, Y. Ueno, M. Nakano, T. Asayama, H. Komori, G. Soumagne, H. Mizoguchi, A. Sumitani, K. Toyoda, Extreme Ultraviolet Lithography System Development Association (Japan) [6517-23]
- 8:20 am: **EUV source development for high-volume chip manufacturing tools**, U. Stamm, M. Yoshioka, J. Kleinschmidt, C. Ziener, G. Schriever, M. C. Schürmann, G. Hergenhan, XTREME technologies GmbH (Germany); V. M. Borisov, Troitsk Institute for Innovation and Fusion Research (Russia) [6517-24]
- 8:40 am: **LPP EUV source development for HVM**, D. C. Brandt, I. V. Fomenkov, A. I. Ershov, N. R. Bowering, A. N. Bykanov, G. O. Vaschenko, W. N. Partlo, D. W. Myers, Cymer, Inc. [6517-25]
- 9:00 am: **Recent developments on the Philips' EUV source**, M. Corthout, J. Pankert, Philips GmbH (Germany) [6517-26]
- 9:20 am: **Tin inventory for HVM EUVL sources**, M. C. Richardson, K. Takenoshita, T. Schmid, College of Optics & Photonics/Univ. of Central Florida [6517-27]
- 9:40 am: **Microdischarge EUV-source array and illuminator design for a prototype lithography tool**, B. E. Jurczyk, R. A. Stubbers, D. A. Alman, Starfire Industries LLC; R. M. Hudyma, M. Thomas, Hyperion Development LLC [6517-28]
- Coffee Break 10:00 to 10:30 am

SESSION 7

Room: Conv. Ctr. B1 Wed. 10:30 am to 12:10 pm

EUV Imaging I

Chair: Kazuaki Suzuki, Nikon Corp. (Japan)

- 10:30 am: **Initial experience establishing an EUV baseline lithography process for manufacturability assessment**, O. R. Wood II, Advanced Micro Devices; D. Back, Qimonda; G. P. Denbeaux, SUNY/Univ. at Albany; D. L. Goldfarb, IBM Thomas J. Watson Research Ctr.; F. Goodwin, Qimonda; J. G. Hartley, SUNY/Univ. at Albany; K. R. Kimmel, C. Koay, IBM Corp.; B. M. La Fontaine, Advanced Micro Devices, Inc.; J. Mackey, Micron Technology, Inc.; B. Martinick, Qimonda; W. Montgomery, P. Naulleau, Albany NanoTech; U. Okoanyanwu, Advanced Micro Devices, Inc.; M. D. Tittnich, Albany NanoTech; S. Trogisch, Qimonda; T. I. Wallow, Advanced Micro Devices, Inc.; Y. Wei, Qimonda [6517-29]
- 10:50 am: **Recent results from the Berkeley 0.3-NA EUV microfield exposure tool**, P. P. Naulleau, Lawrence Berkeley National Lab.; C. N. Anderson, Univ. of California/Berkeley; K. R. Dean, SEMATECH, Inc.; P. E. Denham, K. A. Goldberg, B. Hoef, Lawrence Berkeley National Lab.; B. M. La Fontaine, T. I. Wallow, Advanced Micro Devices, Inc. [6517-30]
- 11:10 am: **EUVL mask dual pods to be used for mask shipping and for mask handling in exposure tools**, Y. Gomei, Canon Inc. (Japan); K. Ota, Semiconductor Leading Edge Technologies, Inc. (Japan); J. Lystad, D. L. Halbmaier, Entegris, Inc.; L. He, SEMATECH, Inc. [6517-31]
- 11:30 am: **Assessment of optimal focus point in EUV lithography**, M. Sugawara, Sony Electronics Inc. [6517-32]
- 11:50 am: **Electrostatic chucking of EUVL reticles**, M. Nataraju, J. Sohn, A. R. Mikkelson, R. L. Engelstad, K. T. Turner, Univ. of Wisconsin/Madison [6517-33]
- Lunch/Exhibition Break 12:10 to 1:40 pm

SESSION 8

Room: Conv. Ctr. B1 Wed. 1:40 to 3:20 pm

Maskless

Chair: Laurent Pain, CEA-LETI (France)

- 1:40 pm: **Technology mapping technique for enhancing throughput of multi-column-cell systems**, M. Sugihara, Institute of Systems & Information Technologies/KYUSHU (Japan); Y. Matsunaga, K. Murakami, Kyushu Univ. (Japan) [6517-34]
- 2:00 pm: **Stage position measurement for e-beam lithography tool**, J. M. Tingay, P. G. Harris, A. McClelland, Vistec Lithography Ltd. (United Kingdom); W. Lee, Renishaw plc [6517-35]
- 2:20 pm: **Defect inspection of positive and negative sub-60-nm resist pattern printed with variable shaped e-beam direct write lithography**, C. Arndt, Qimonda Dresden GmbH & Co. OHG (Germany); C. K. Hohle, Qimonda AG (Germany); T. Lutz, J. Kretz, M. Richter, Qimonda Dresden GmbH & Co. OHG (Germany); M. Lapidot, M. Kindler, Negvetech GmbH (Germany) [6517-36]
- 2:40 pm: **Monte Carlo simulation using voltage contrast by low-energy electron beam**, T. Ota, T. Koshiba, T. Nakasugi, Toshiba Corp. (Japan) [6517-37]
- 3:00 pm: **Alignment method of low-energy electron-beam direct writing system EBIS using voltage contrast image**, T. Koshiba, T. Ota, T. Nakasugi, Toshiba Corp. (Japan); F. Nakamura, K. Watanabe, K. Sugihara, e-BEAM Corp. (Japan) [6517-38]
- Coffee Break 3:20 to 3:50 pm

SESSION 9

Room: Conv. Ctr. B1 Wed. 3:50 to 5:30 pm

NIL II

Chair: R. Scott Mackay, Consultant

- 3:50 pm: **An electrical defectivity characterization of wafers imprinted with step and flash imprint lithography**, W. J. Dauksher, Motorola, Inc. and Florida International Univ.; K. J. Nordquist, E. S. Ainley, N. V. Le, K. A. Gehoski, Motorola, Inc.; N. Joshi, Florida International Univ. [6517-39]
- 4:10 pm: **Pattern quality and porosity characteristics of ultra-low dielectric insulator films directly patterned by nanoimprint lithography**, H. W. Ro, R. L. Jones, H. Lee, E. K. Lin, A. Karim, National Institute of Standards and Technology; D. R. Hines, Univ. of Maryland/College Park; H. Peng, D. Gidley, Univ. of Michigan; D. Y. Yoon, Seoul National Univ. (South Korea); C. L. Soles, National Institute of Standards and Technology [6517-40]
- 4:30 pm: **Ultra-violet nanoimprint lithography applicable to thin film transistor liquid-crystal display**, J. Jeong, K. Kim, D. Choi, J. Choi, E. Lee, Korea Institute of Machinery and Materials (South Korea) . . [6517-41]
- 4:50 pm: **Toward 22 nm for unit process development using step and flash imprint lithography**, D. J. Resnick, G. Schmid, E. Thompson, N. Stacey, Molecular Imprints, Inc.; D. Olynick, E. Anderson, Lawrence Berkeley National Lab. [6517-42]
- 5:10 pm: **Soft UV-based nanoimprint lithography for large-area imprinting applications**, T. Glinsner, EV Group (Austria) [6517-43]

SESSION 10

Joint Session with conference 6519: EUV Resist

Marriott San Jose Ballroom Salon III . . Wed. 6:30 to 8:50 pm

Chairs: Michael J. Lercel, SEMATECH, Inc.; Anthony E. Novembre, Lucent Technologies

- 6:30 pm: **Chemically amplified resists resolving 25-nm 1:1 line: space features following EUV exposure**, J. W. Thackeray, Rohm and Haas Electronic Materials [6517-44]
- 6:50 pm: **Resist evaluation for EUV application at ASET**, D. Goo, Y. Tanaka, Y. Kikuchi, H. Oizumi, I. Nishiyama, Association of Super-Advanced Electronics Technologies (Japan) [6519-60]
- 7:10 pm: **Patterning performance of new molecular resist in EUV lithography**, H. Oizumi, Y. Tanaka, T. Kumise, I. Nishiyama, Association of Super-Advanced Electronics Technologies (Japan) [6517-45]
- 7:30 pm: **Molecular glass photoresists containing photo-acid generator functionality: a route to a true single-molecule photoresist**, R. A. Lawson, R. Whetsell, Georgia Institute of Technology; W. Yueh, J. M. Roberts, Intel Corp.; L. M. Tolbert, C. L. Henderson, Georgia Institute of Technology [6519-61]
- 7:50 pm: **Metrology for EUV-resist outgassing using pressure-rise method**, I. Nishiyama, H. Oizumi, Association of Super-Advanced Electronics Technologies (Japan) [6517-46]
- 8:10 pm: **The resist materials study for outgassing reduction and LWR improvement in EUV lithography**, S. Masuda, S. Kamimura, S. Hirano, W. Hoshino, K. Mizutani, Fuji Photo Film Co., Ltd. (Japan) [6519-62]
- 8:30 pm: **An analysis of EUV-resist outgassing measurements**, K. R. Dean, SEMATECH, Inc.; I. Nishiyama, H. Oizumi, ASET (Japan); A. M. Keen, BOC Edwards, Inc.; H. B. Cao, W. Yueh, Intel Corp.; T. Watanabe, Univ. of Hyogo (Japan); P. Lacovig, L. Rumiz, Sincrotrone Trieste S.C.p.A (Italy); G. P. Denbeaux, SUNY/Univ. at Albany; J. Simon, CEA/LETI (France) [6519-63]

Thursday 1 March

SESSION 11

Conv. Ctr. B1 Thurs. 8:00 to 10:00 am

Advanced Mask II

Chair: James W. Blatchford, Texas Instruments Inc.

- 8:00 am: **30-nm template fabrication for step and flash imprint lithography**, H. Kobayashi, T. Sato, T. Kagatsume, O. Nagarekawa, HOYA Corp. (Japan) [6517-47]
- 8:20 am: **New requirements for the cleaning of EUV mask blanks**, A. Rastegar, S. K. Eichenlaub, Y. Ikuta, V. Kapila, P. Marmillion, SEMATECH, Inc. [6517-48]
- 8:40 am: **Experimental and simulation investigations of acoustic cavitation in megasonic cleaning of extreme-UV photomasks**, K. Muralidharan, H. Shende, M. Keswani, P. A. Deymier, S. Raghavan, The Univ. of Arizona; F. O. Eschbach, A. Sengupta, Intel Corp. [6517-49]
- 9:00 am: **Photonic band-gap masks to enhance resolution and depth of focus**, J. L. Nistler, K. Duckworth, PSIDA Lithography Software [6517-50]
- 9:20 am: **Properties of EUVL masks depending on capping layer and absorber stack structures**, H. Seo, J. Park, S. Kim, H. Cho, J. Moon, SAMSUNG Electronics Co., Ltd. (South Korea) [6517-51]
- 9:40 am: **Sub-35-nm logic device template fabrication**, Y. K. Cho, National Nanofab Ctr (South Korea) [6517-52]
- Coffee Break 10:00 to 10:30 am

SESSION 12

Room: Conv. Ctr. B1 Thurs. 10:30 am to 12:10 pm

Novel Lithography

Chair: Hans Loeschner, IMS Nanofabrication GmbH (Austria)

- 10:30 am: **Molecular ruler nanolithography**, C. Srinivasan, M. E. Anderson, P. S. Weiss, M. W. Horn, The Pennsylvania State Univ. [6517-53]
- 10:50 am: **Scissionable bile acid nanostructures for lithography**, R. P. Meagley, A. Gupta, Lawrence Berkeley National Lab. [6517-54]
- 11:10 am: **Stretched polymer nanohairs by nanodrawing**, H. E. Jeong, S. H. Lee, P. Kim, K. Y. Suh, Seoul National Univ. (South Korea) . [6517-55]
- 11:30 am: **Direct high-speed three-dimensional nanoscale thermal lithography using heated atomic-force microscope cantilevers**, Y. Hua, S. R. Saxena, J. C. Lee, W. P. King, C. L. Henderson, Georgia Institute of Technology [6517-56]
- 11:50 am: **Focused ion-beam nanopatterning for fabrications of III-nitride light emitting diodes**, M. Kim, S. Hong, D. Lee, Y. Park, B. Kim, SAMSUNG Electro-Mechanics Co., Ltd. (South Korea) [6517-57]
- Lunch Break 12:10 to 1:40 pm

SESSION 13

Room: Conv. Ctr. B1 Thurs. 1:40 to 3:20 pm

EUV Imaging II

Chair: Michael Goldstein, Intel Corp.

- 1:40 pm: **Rigorous model for registration error due to EUV reticle non-flatness and a proposed disposition and compensation technique**, B. R. Lieberman, Intel Corp. [6517-58]
- 2:00 pm: **Status and path to a final EUVL reticle protection and handling solution**, L. He, K. J. Orvek, P. Seidel, S. Wurm, SEMATECH, Inc. [6517-59]
- 2:20 pm: **Performance estimation of EUV exposure optics for below 32-nm node in consideration of Mo/Si multilayer**, T. Sasaki, K. Kajiyama, H. Morishima, T. Tsuji, M. Suzuki, M. Suzuki, H. Yokota, Canon Inc. (Japan) [6517-60]

2:40 pm: **Image formation study of EUV holographic lithography**, Y. Cheng, A. Isoyan, J. P. Wallace, F. Jiang, F. Cerrina, Univ. of Wisconsin/Madison [6517-61]

3:00 pm: **EUVL mask development status at Samsung**, H. Kim, SAMSUNG Electronics Co. Ltd. (South Korea) [6517-62]

Coffee Break 3:20 to 3:50 pm

SESSION 14

Room: Conv. Ctr. B1 Thurs. 3:50 to 5:50 pm

EUV Source II

Chair: Akira Endo, Extreme Ultraviolet Lithography System Development Association (Japan)

- 3:50 pm: **Thermal management design and verification of collector optics into high-power EUV source systems**, G. Bianucci, F. E. Zocchi, G. Pirovano, G. L. Cassol, Media Lario S.r.l. (Italy); L. Porreca, Eidgenossische Technische Hochschule (Switzerland); I. Ahmad, D. Bolshukhin, M. C. Schürmann, XTREME technologies GmbH (Germany) [6517-63]
- 4:10 pm: **Low-cost EUV collector development: design, process, and fabrication**, R. D. Venables, M. Goldstein, Intel Corp.; D. E. Engelhaupt, The Univ. of Alabama/Huntsville; S. H. Lee, E. M. Panning, Intel Corp. [6517-64]
- 4:30 pm: **Advanced debris mitigation schemes and cleaning methods: collector optics lifetime extension**, D. N. Ruzic, S. N. Srivastava, E. L. Antonsen, K. C. Thompson, H. Qiu, H. J. Shin, M. J. Neumann, J. B. Spencer, Univ. of Illinois at Urbana-Champaign [6517-65]
- 4:50 pm: **Energetic and thermal Sn interactions and their effect on EUVL source collector mirror lifetime at high temperatures**, J. Allain, M. D. Nieto, A. Hassanein, M. Hendricks, Argonne National Lab.; D. Detert, Univ. of Wisconsin/Madison; C. Tarrio, S. E. Grantham, National Institute of Standards and Technology; V. Bakshi, SEMATECH, Inc. [6517-66]
- 5:10 pm: **Application of the Energetiq EQ-10 electrodeless Z-Pinch™ EUV light source in outgassing and exposure of EUV photoresist**, P. A. Blackborow, D. S. Gustafson, D. K. Smith, M. M. Besen, S. F. Horne, R. J. D'Agostino, Energetiq Technology, Inc.; Y. Minami, Litho Tech Japan Co., Ltd. (Japan); G. P. Denbeaux, SUNY/Univ. at Albany [6517-67]
- 5:30 pm: **Optimization of EUV laser and discharge devices for high-volume manufacturing**, A. Hassanein, J. Allain, V. A. Sizyuk, Z. Insepov, T. S. Sizyuk, Argonne National Lab.; V. Bakshi, SEMATECH, Inc. . . [6517-68]

✓ Posters - Thursday

Room: Convention Ctr. Hall 3 Thurs. 5:30 to 8:00 pm

The following posters will be displayed all day Thursday. Authors will be present during the formal poster session Thursday evening between 5:30 and 8:00 pm for discussion. Authors may set-up their posters after 9:00 am on Thursday.

Advanced Mask

- ✓ **Detection signal analysis of actinic inspection of EUV mask blanks using dark-field imaging**, T. Tanaka, T. Terasawa, N. M. Iriki, H. Aoyama, Semiconductor Leading Edge Technologies, Inc. (Japan) [6517-69]
- ✓ **Development of EUV mask handling technology at Selete**, K. Ota, M. Amemiya, T. Kamono, H. Kubo, Y. Usui, T. Taguchi, O. Suga, Semiconductor Leading Edge Technologies, Inc. (Japan) . . . [6517-70]
- ✓ **Impact of interface treatment with assisted ion beam on Mo-Si multilayer formation for EUVL mask blanks**, K. Hiruma, Y. Tanaka, S. Miyagaki, J. Cullins, I. Nishiyama, Association of Super-Advanced Electronics Technologies (Japan) [6517-71]
- ✓ **Spectrally investigated optimization for the high-optical transmission of the C-shaped nano-apertures**, E. Lee, K. Kim, J. W. Hahn, Yonsei Univ. (South Korea) [6517-72]
- ✓ **Design of metal slits for higher harmonic fringe patterns generated with surface plasmon interference lithography**, Y. Lee, S. Park, E. Lee, J. W. Hahn, Yonsei Univ. (South Korea) [6517-73]

- ✓ **The effect of localized mask density variations on image quality in EUV lithography**, J. Park, H. Seo, S. Kim, H. Cho, J. Moon, SAMSUNG Electronics Co., Ltd. (South Korea) [6517-74]
- ✓ **Corning ULE® glass can meet P-37 specifications**, W. R. Rosch, L. Beall, J. E. Maxon, R. Sabia, R. D. Sell, Corning Inc. [6517-75]
- ✓ **Evaluation and selection of EUVL-grade TiO₂-SiO₂ ultra-low-expansion glasses using the line-focus-beam ultrasonic material characterization system**, M. Arakawa, Y. Ohashi, J. Kushibiki, Tohoku Univ. (Japan) [6517-76]
- ✓ **Defect mitigation and reduction in EUVL mask blanks**, A. Ma, SEMATECH, Inc.; R. V. Randive, I. Reiss, Veeco Instruments, Inc.; P. Mirkarime, Mirkarimi Enterprises; E. Spills, Spiller X-ray Optics; T. Uno, Asahi Glass Co., Ltd.; P. A. Kearney, C. Jeon, SEMATECH, Inc. [6517-77]

Nano-imprint

- ✓ **Low-viscosity and fast-curing polymer system for UV-based nanoimprint lithography and its processing**, M. Vogler, micro resist technology GmbH (Germany); M. Bender, AMO GmbH (Germany) [6517-78]
- ✓ **Pattern transfer of multilevel interconnect structures generated by step and flash imprint lithography**, M. W. Lin, F. L. Palmieri, K. Jen, J. Hao, The Univ. of Texas at Austin; Q. Zhang, Applied Materials, Inc.; J. Owens, Advanced Technology Development Facility, Inc.; K. Osberg, C. Neikirk, The Univ. of Texas at Austin; J. T. Wetzel, Advanced Technology Development Facility, Inc.; R. Cheung, Applied Materials, Inc.; G. Willson, The Univ. of Texas at Austin [6517-79]
- ✓ **Photopatternable low-K dielectrics for imprinting lithography**, J. Hao, F. L. Palmieri, M. W. Lin, Y. Nishimura, H. Chao, K. Jen, M. D. Stewart, A. Collins, G. Willson, The Univ. of Texas at Austin . . [6517-80]
- ✓ **Nanoimprinting with SU-8 epoxy resists**, D. W. Johnson, MicroChem Corp.; M. Kubenz, F. Reuther, G. Gruetzner, micro resist technology GmbH (Germany) [6517-81]
- ✓ **MR-NIL 6000: new epoxy-based curing resist for efficient processing in combined thermal and UV nanoimprint lithography**, C. Schuster, M. Kubenz, F. Reuther, M. Fink, G. Gruetzner, micro resist technology GmbH (Germany) [6517-82]
- ✓ **Structure and stability characterizations of anti-adhesion self-assembled monolayers formed by vapor deposition for NIL use**, S. Garidel, M. Zelsmann, N. Rochat, P. Michallon, Commissariat à l'Énergie Atomique (France) [6517-83]
- ✓ **Template flatness issue for UV curing nanoimprint lithography**, P. Voisin, M. Zelsmann, C. Gourgon, J. Boussey, Commissariat à l'Énergie Atomique (France) [6517-84]
- ✓ **Imprint solutions, costs, and returns of patterning LED's**, M. P. C. Watts, Impattern Solutions [6517-86]
- ✓ **Whole wafer imprint patterning using step and flash imprint lithography: a manufacturing solution for sub-100-nm patterning**, D. Lentz, G. F. Doyle, M. L. Miller, Molecular Imprints, Inc.; G. E. Schmidt, Materials Systems, Inc.; G. Ganapathisuramanian, X. Lu, D. J. Resnick, D. L. LaBrake, Molecular Imprints, Inc. [6517-87]

ML and E-beam Lithography

- ✓ **Exposure characteristics of character projection-type low-energy electron-beam direct writing system**, R. Inanami, T. Satoh, K. Hirose, K. Kishimoto, e-BEAM Corp. (Japan) [6517-88]
- ✓ **Data processing system in EB direct writing to obtain photolithography friendly resist patterns**, H. Hoshino, Y. Machida, Fujitsu Ltd. (Japan) [6517-89]
- ✓ **Recent progress of a character projection-type low-energy electron-beam direct writing system**, K. Noguchi, K. Watanabe, F. Nakamura, H. Kinoshita, H. Shinozaki, S. Morita, Y. Kojima, N. Yamaguchi, e-BEAM Corp. (Japan); T. Nakasugi, T. Koshiba, Toshiba Corp. (Japan) [6517-90]
- ✓ **Shot noise effect on LER and throughput in LEEPL systems**, T. Utsumi, Nanolith LLC (Japan) [6517-91]

EUV Imaging

- ✓ **CD budget analysis on hole pattern in EUVL**, N. M. Iriki, H. Aoyama, T. Tanaka, Semiconductor Leading Edge Technologies, Inc. (Japan) [6517-92]
- ✓ **Fidelity of rectangular patterns printed with 0.3-NA MET optics**, Y. Tanaka, Y. Kikuchi, D. Goo, I. Nishiyama, Association of Super-Advanced Electronics Technologies (Japan) [6517-93]
- ✓ **EUV exposure experiment using programmed multilayer defects for refining printability simulation**, Y. Tezuka, J. Cullins, Y. Tanaka, I. Nishiyama, Association of Super-Advanced Electronics Technologies (Japan) [6517-94]
- ✓ **Lithographic metrics for the determination of intrinsic resolution limits in EUV resists**, P. P. Naulleau, Lawrence Berkeley National Lab.; C. N. Anderson, Univ. of California/Berkeley; B. M. La Fontaine, T. I. Wallow, Advanced Micro Devices, Inc. [6517-95]
- ✓ **Absorption of extreme ultraviolet radiations in different photoresists**, R. Garg, A. Antohe, G. P. Denbeaux, SUNY/Univ. at Albany [6517-96]
- ✓ **Process window study with various illuminations for EUV lithography applications**, S. H. Lee, Z. Zhang, Intel Corp. . . [6517-98]
- ✓ **Characterization of low-order aberrations in the SEMATECH North MET tool**, P. P. Naulleau, SUNY/Univ. at Albany and Lawrence Berkeley National Lab.; J. Waterman, SUNY/Univ. at Albany; K. R. Dean, SEMATECH, Inc. [6517-99]
- ✓ **EUV lithographic flare and MTF measurements on Intel micro-exposure tool**, T. Murachi, Intel Kabushiki Kaisha (Japan) . . [6517-100]
- ✓ **Characteristics and prevention of pattern collapse in EUV lithography**, W. Chang, E. Kim, S. Park, Han Yang Univ. (South Korea); Y. Hyun, C. Lim, Hynix Semiconductor Inc. (South Korea); H. Oh, Sr., Han Yang Univ. (South Korea) [6517-101]
- ✓ **Extreme ultraviolet interference lithography with incoherent light**, P. P. Naulleau, C. N. Anderson, Lawrence Berkeley National Lab. [6517-102]
- ✓ **A short-pulsed laser cleaning system for EUVL tool**, M. Yonekawa, H. Namba, T. Hayashi, Canon Inc. (Japan) [6517-103]

EUV Optics

- ✓ **Mo/Si multilayers with enhanced capping layers**, S. A. Yulin, N. Benoit, T. Feigl, N. Kaiser, Fraunhofer-Institut für Angewandte Optik und Feinmechanik (Germany); S. B. Hill, T. B. Lucatorto, National Institute of Standards and Technology; F. J. Dollar, E. M. Gullikson, Lawrence Berkeley National Lab.; M. Fang, M. Chandhok, M. K. Shell, Intel Corp. [6517-104]
- ✓ **Polarization dependence of multilayer reflectance in the EUV spectral range**, F. Scholze, C. Laubis, C. Buchholz, A. Fischer, A. Kampe, S. Plöger, F. D. Scholz, G. Ulm, Physikalisch-Technische Bundesanstalt (Germany) [6517-106]
- ✓ **Carbon deposition on multilayer mirrors by extreme ultraviolet ray irradiation**, S. Matsunari, T. Aoki, K. Murakami, S. Terashima, M. Tanabe, H. Takase, Y. Watanabe, Extreme Ultraviolet Lithography System Development Association (Japan); Y. Gomei, Canon Inc. (Japan); Y. Kakutani, M. Niibe, Univ. of Hyogo (Japan); Y. Fukuda, Extreme Ultraviolet Lithography System Development Association (Japan) [6517-107]
- ✓ **Effect of deposition, sputtering, and evaporation of lithium debris buildup on EUV optics**, M. J. Neumann, Univ. of Illinois at Urbana-Champaign [6517-108]
- ✓ **Processes on Ruthenium surfaces related to degradation of EUV mirrors**, B. V. Yakshinskiy, R. Wasielewski, E. Loginova, T. E. Madey, Rutgers Univ. [6517-109]
- ✓ **EUVL optics substrate recovery process: reflectivity and surface roughness**, I. Nedelcu, R. W. E. van de Kruijs, A. E. Yakshin, E. Louis, F. Bijkerk, FOM-Instituut voor Plasmafysica Rijnhuizen (Netherlands); S. Mullender, Carl Zeiss SMT AG (Germany) [6517-110]

- ✓ **Long-time durability of Ru capping layer for EUVL projection optics by introducing ethanol**, Y. Kakutani, M. Niibe, Univ. of Hyogo (Japan); Y. Gomei, Canon Inc. (Japan); H. Takase, S. Terashima, S. Matsunari, T. Aoki, Y. Fukuda, Extreme Ultraviolet Lithography System Development Association (Japan) [6517-111]
- ✓ **High-accuracy EUV reflectometer**, U. Hinze, B. N. Chichkov, Laser Zentrum Hannover e.V. (Germany) [6517-112]
- ✓ **Development of optical component for EUV phase-shift microscope**, Y. Mizuta, H. Kinoshita, T. Watanabe, M. Osugi, Univ. of Hyogo (Japan) [6517-113]

Nanotechnology

- ✓ **Fabrication of fine pitch gratings by holography, electron-beam lithography, and nano-imprint lithography**, D. P. Goodchild, A. L. Bogdanov, S. Wingar, B. Benyon, F. Shepherd, National Research Council of Canada (Canada) [6517-116]
- ✓ **Three-dimensional x-ray lithography using a silicon mask with inclined absorbers**, H. Mekaru, T. Takano, K. Awazu, M. Takahashi, R. Maeda, National Institute of Advanced Industrial Science and Technology (Japan) [6517-117]
- ✓ **Photon sieve array x-ray maskless nanolithography**, G. Cheng, T. Xing, W. Lin, J. Zhou, C. Qiu, Z. Liao, Y. Yang, Institute of Optics and Electronics (China); L. Hong, Univ. of Electronic Science and Technology of China (China); J. Ma, Taishan College (China) [6517-118]
- ✓ **Micro-scale magneto-polymer boomerangs fabricated using soft lithography**, K. Herlihy, S. E. A. Gratton, The Univ. of North Carolina at Chapel Hill; B. W. Maynor, Liquidia Technologies, Inc; J. M. DeSimone, The Univ. of North Carolina at Chapel Hill [6517-119]
- ✓ **Simulating particle deposition rates during evaporation-driven self assembly**, J. J. Dyreby, G. F. Nellis, K. T. Turner, R. L. Engelstad, Univ. of Wisconsin/Madison [6517-120]

EUV Source

- ✓ **Microfocus EUV tube for at-wavelength reflectometry**, A. Egbert, S. Becker, Phoenix EUV Systems & Services GmbH (Germany) [6517-121]
- ✓ **CO₂ laser and Sn-droplet target development for EUVL**, A. Endo, H. Hoshino, T. Ariga, T. Miura, Y. Ueno, M. Nakano, T. Asayama, H. Komori, G. Soumagne, H. Mizoguchi, A. Sumitani, K. Toyoda, Extreme Ultraviolet Lithography System Development Association (Japan) [6517-122]
- ✓ **Characterization of various Sn targets with respect to debris and fast ion generation**, Y. Ueno, H. Hoshino, T. Ariga, T. Miura, M. Nakano, H. Komori, G. Soumagne, A. Endo, H. Mizoguchi, A. Sumitani, K. Toyoda, Extreme Ultraviolet Lithography System Development Association (Japan) [6517-123]
- ✓ **Small field exposure tool (SFET) light source**, T. Abe, T. Suganuma, M. Moriya, T. Yabu, T. Asayama, H. Someya, Y. Ueno, G. Soumagne, A. Sumitani, H. Mizoguchi, Extreme Ultraviolet Lithography System Development Association (Japan) [6517-124]
- ✓ **Debris characteristics from a colloidal microjet target containing tin dioxide nano-particles**, S. Kubodera, S. Suetake, Y. Senba, A. Hosotani, Y. Takahashi, Univ. of Miyazaki (Japan); T. Higashiguchi, Utsunomiya Univ. (Japan) [6517-125]
- ✓ **A model of a distributed EUV source for next-generation lithography tools**, J. B. Spencer, Univ. of Illinois at Urbana-Champaign; D. A. Alman, B. E. Jurczyk, Starfire Industries LLC; D. N. Ruzic, Univ. of Illinois at Urbana-Champaign [6517-126]
- ✓ **EUV and debris emission from laser-irradiated pure-tin droplet**, S. Fujioka, T. Aota, Osaka Univ. (Japan); E. Fujiwara, Univ. Hyogo (Japan); H. Nishimura, Osaka Univ. (Japan) [6517-127]
- ✓ **Experimental results of an addressable xenon microdischarge EUV-source array for HVM lithography**, B. E. Jurczyk, R. A. Stubbers, J. L. Rovey, M. D. Coventry, Starfire Industries LLC [6517-128]
- ✓ **XUV spectroscopy of mass-limited Sn-doped laser micro-plasmas**, S. A. George, College of Optics & Photonics/Univ. of Central Florida; C. Koay, IBM Corp.; K. Takenoshita, T. Schmid, R. Bernath, College of Optics & Photonics/Univ. of Central Florida; M. M. Al-Rabban, Univ. of Qatar (Qatar); H. A. Scott, Lawrence Livermore National Lab.; M. C. Richardson, College of Optics & Photonics/Univ. of Central Florida [6517-129]

- ✓ **High-power/high-repetition-rate laser-produced tin-doped micro-plasma source for EUVL**, T. Schmid, S. A. George, J. Cunado, S. Teerawattanasook, R. Bernath, C. G. Brown, College of Optics & Photonics/Univ. of Central Florida; C. Koay, IBM Corp.; K. Takenoshita, M. C. Richardson, College of Optics & Photonics/Univ. of Central Florida [6517-130]
- ✓ **Laser-produced plasma source system development**, I. V. Fomenkov, D. C. Brandt, A. I. Ershov, N. R. Bowering, D. W. Myers, W. N. Partlo, A. N. Bykanov, O. V. Khodykin, J. R. Hoffman, E. Vargas, J. A. Chavez, R. D. Simmons, G. O. Vaschenko, Cymer, Inc. [6517-131]
- ✓ **Gibbsian segregating alloys: a potential solution to minimize collector degradation**, H. Qiu, S. N. Srivastava, J. C. Anderson, D. N. Ruzic, Univ. of Illinois at Urbana-Champaign [6517-132]
- ✓ **Debris mitigation techniques for a Sn- and Xe-fueled EUV-light source**, K. C. Thompson, S. N. Srivastava, E. L. Antonsen, D. N. Ruzic, Univ. of Illinois at Urbana-Champaign [6517-133]
- ✓ **Comparison of optical performances of alternative grazing incidence collector designs for EUV lithography**, F. E. Zocchi, E. Benedetti, Media Lario S.r.l. (Italy) [6517-134]
- ✓ **Optimization of 13.5-nm conversion efficiencies from laser-produced tin plasmas for EUV lithography**, J. J. MacFarlane, I. E. Golovkin, P. R. Woodruff, P. Wang, Prism Computational Sciences, Inc. [6517-135]
- ✓ **Characterization of the Tin-doped droplet laser plasma EUVL sources for HVM**, K. Takenoshita, S. A. George, T. Schmid, College of Optics & Photonics/Univ. of Central Florida; C. Koay, IBM Corp.; J. Cunado, R. Bernath, C. G. Brown, College of Optics & Photonics/Univ. of Central Florida; M. M. Al-Rabban, Univ. of Qatar; W. T. Silfvast, M. C. Richardson, College of Optics & Photonics/Univ. of Central Florida [6517-136]
- ✓ **LPP EUV source by minimum mass tin targets**, Y. Izawa, H. Nishimura, S. Fujioka, M. Yamaura, Y. Shimada, T. Aota, K. Nagai, Osaka Univ. (Japan); E. Fujiwara, Univ. of Hyogo (Japan); K. Nishihara, A. Sunahara, N. Miyahara, K. Mima, Osaka Univ. (Japan) ... [6517-137]
- ✓ **A mass-limited Sn target irradiated by dual laser pulses for an EUVL source**, Y. Tao, M. S. Tillack, K. L. Sequoia, F. Najimabadi, Univ. of California/San Diego [6517-138]
- ✓ **Development of Sn-fueled high-power DPP EUV source for enabling HVM**, Y. Teramoto, Z. Narihiro, D. Yamatani, T. Yokoyama, K. Bessho, Y. Joshima, T. Shirai, S. Mouri, T. Inoue, H. Mizokoshi, G. Niimi, Extreme Ultraviolet Lithography System Development Association (Japan); H. Yabuta, K. C. Paul, Ushio Inc. (Japan); T. Takemura, Extreme Ultraviolet Lithography System Development Association (Japan); T. Yokota, Ushio Inc. (Japan); K. Kabuki, K. Miyauchi, K. Hotta, H. Sato, Extreme Ultraviolet Lithography System Development Association (Japan) [6517-139]

Courses of Related Interest

Register for courses at the SPIE registration desk.

SC100 Introduction to Electron-Beam Lithography (McCord) Sunday 8:30 am to 12:30 pm

SC101 Introduction to Microlithography: Theory, Materials, and Processing (Willson, Bowden, Thompson) Sunday 8:30 am to 5:30 pm

SC622 Nano-Scale Patterning with Imprint Lithography (Sreenivasan, Willson, Resnick) Sunday 6:00 to 10:00 pm

SC830 Recent Advances in Electron Beam Lithography (Pfeiffer) Sunday 1:30 to 5:30 pm

SC832 IP Issues in Advanced Lithography and Semiconductor Manufacturing (Gortych) Monday 1:30 to 5:30 pm

Metrology, Inspection, and Process Control for Microlithography XXI

Conference Chair: **Chas N. Archie**, IBM Corp.

Cochair: **John A. Allgair**, SEMATECH, Inc. and Freescale Semiconductors, Inc.

Program Committee: **Ofer Adan**, Applied Materials (Israel); **Michael J. Anderson**, Rohm and Haas Electronic Materials; **Jason P. Cain**, Advanced Micro Devices, Inc.; **Alain G. Deleporte**, STMicroelectronics (France); **Daniel J. C. Herr**, Semiconductor Research Corp.; **David C. Joy**, The Univ. of Tennessee; **Chih-Ming Ke**, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan); **Byoung-Ho Lee**, SAMSUNG Electronics Co., Ltd. (South Korea); **Christopher J. Raymond**, Accent Optical Technologies, Inc.; **Martha I. Sanchez**, IBM Almaden Research Ctr.; **Richard M. Silver**, National Institute of Standards and Technology; **Bhanwar Singh**, Advanced Micro Devices, Inc.; **Michael W. Stan**, MicroChem Corp.; **Alexander Starikov**, Intel Corp.; **Neal T. Sullivan**, Arradiance, Inc.; **Brian M. Trafas**, KLA-Tencor Corp.; **Vladimir A. Ukraintsev**, Texas Instruments Inc.

Monday 26 February

Opening Remarks

Room: Conv. Ctr. J2 Mon. 11:00 to 11:20 am

Chair: **Charles N. Archie**, IBM Corp.

Metrology, Inspection, and Process Control 2006 Best Paper Award Announcement

SESSION 1

Room: Conv. Ctr. J2 Mon. 11:20 am to 12:00 pm

Keynote Session

Chair: **Charles N. Archie**, IBM Corp.

Keynote Presentation
11:20 am: **Metrology challenges of double exposure/double patterning** (*Invited Paper*), **W. H. Arnold**, ASML Netherlands B.V. [6518-01]

Lunch Break 12:00 to 1:00 pm

SESSION 2

Room: Conv. Ctr. J2 Mon. 1:00 to 2:50 pm

Process Control I: Lithography Control

Chairs: **Alain G. Deleporte**, STMicroelectronics (France); **Christopher J. Raymond**, Accent Optical Technologies, Inc.

1:00 pm: **Process monitor gratings** (*Invited Paper*), **T. A. Brunner**, IBM Thomas J. Watson Research Ctr.; **C. P. Ausschnitt**, IBM Microelectronics Div. [6518-02]

1:30 pm: **Lithography equipment control using scatterometry metrology and semi-physical modeling**, **K. R. Lensing**, **J. P. Cain**, **A. Prabhu**, **A. Vaid**, **R. Chong**, **B. Singh**, Advanced Micro Devices, Inc.; **E. M. Apelgren**, Spansion Inc. [6518-03]

1:50 pm: **A comparison of focus monitoring techniques**, **K. D'havé**, **T. Machida**, **D. Laidler**, **S. Y. Cheng**, IMEC (Belgium) [6518-131]

2:10 pm: **Characterization of hyper-NA lithography focus control using scatterometry**, **C. Saravanan**, **R. Korlahalli**, **S. Nirmalgandhi**, Nanometrics Inc.; **O. Kritsun**, Advanced Micro Devices, Inc.; **A. Acheta**, Advanced Micro Devices, Inc. and Spansion Inc.; **R. Sandberg**, **B. M. La Fontaine**, **H. J. Levinson**, Advanced Micro Devices, Inc.; **M. V. Dusa**, **J. Hauschild**, **A. Pici**, ASML MaskTools Inc. [6518-05]

2:30 pm: **Focus, dose controls, and its application in lithography**, **H. Ina**, **S. Oishi**, **K. Sentoku**, **T. Miyashita**, **T. Matsumoto**, Canon Inc. (Japan) [6518-06]

Coffee Break 2:50 to 3:20 pm

SESSION 3

Room: Conv. Ctr. J2 Mon. 3:20 to 5:20 pm

CD for Development I: OPC and Metrology

Chairs: **Neal T. Sullivan**, Arradiance, Inc.; **Chih-Ming Ke**, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan)

3:20 pm: **Statistical optimization of sampling plan and its relation to OPC model accuracy**, **G. Han**, **A. Brendler**, **S. M. Mansfield**, **J. E. Meiring**, IBM Microelectronics Div. [6518-07]

3:40 pm: **Automatic setup of in-line critical dimension (CD) monitoring and OPC calibration recipes in a foundry environment**, **Y. Yudhistira**, Chartered Semiconductor Manufacturing Ltd. (Singapore); **H. A. Kek**, **S. L. Ng**, Applied Materials South East Asia Pte. Ltd. (Singapore) ... [6518-08]

4:00 pm: **Quantification of two-dimensional structures generalized for OPC model verification**, **X. Shi**, **J. F. Chen**, **D. J. Van Den Broeke**, **S. D. Hsu**, **C. M. Hsu**, ASML MaskTools Inc. [6518-09]

4:20 pm: **Setting MRC rules for OPC: balancing inspection capabilities, defect sensitivity, and OPC**, **I. P. Stobert**, **J. A. Bruce**, IBM Corp.; **M. Gheith**, **A. Seoud**, Mentor Graphics Corp. [6518-10]

4:40 pm: **Methodology to set-up accurate OPC model using optical CD metrology and atomic force microscopy**, **Y. Shim**, **J. Kang**, **S. Lee**, **Y. Lee**, **K. Kim**, DongbuAnam Semiconductor Inc. (South Korea) ... [6518-11]

5:00 pm: **SEM-contour-based OPC model calibration through the process window**, **J. E. Vasek**, Freescale Semiconductor, Inc.; **Y. Nehmadi**, **M. Poyastro**, Applied Materials; **O. Menadeva**, Applied Materials (Israel); **J. L. Sturtevant**, **G. E. Bailey**, **I. Kusnadi**, Mentor Graphics Corp. ... [6518-12]

✓ Posters-Monday

Chair: **Christopher J. Raymond**, Accent Optical Technologies, Inc.

Room: Convention Ctr. Hall 3 Mon. 5:30 to 8:00 pm

The following posters will be displayed all day Monday. Authors will be present during the formal poster session Monday evening between 5:30 and 8:00 pm for discussion. Authors may set-up their posters after 10:30 am on Monday.

✓ **Application of perturbation methods in optical scatterometry**, **B. C. Bergner**, **T. J. Suleski**, The Univ. of North Carolina at Charlotte [6518-33]

✓ **AFM characterization of resins for 193-nm photolithography**, **O. Soppera**, **V. V. Balasubramanian**, **D. Loughnot**, École Nationale Supérieure de Chimie de Mulhouse (France) [6518-58]

✓ **SEM metrology for advanced lithographies**, **B. D. Bunday**, **J. A. Allgair**, International SEMATECH Manufacturing Initiative; **N. G. Orji**, National Institute of Standards and Technology; **B. J. Rice**, SEMATECH, Inc.; **O. Adan**, **R. Peltinov**, **M. Bar-Zvi**, Applied Materials (Israel)[6518-62]

- ✓ **Across-wafer CD uniformity control through lithography and etch process: experimental verification**, Q. Zhang, Univ. of California/Berkeley; C. Tang, Spansion Inc.; J. P. Cain, A. Hui, T. Hsieh, Advanced Micro Devices, Inc.; N. R. Maccrae, Spansion Inc.; B. Singh, Advanced Micro Devices, Inc.; K. Poola, C. J. Spanos, Univ. of California/Berkeley[6518-77]
- ✓ **Image analysis of alignment and overlay marks with compound structure**, R. Chalykh, J. Shin, I. Pundaleva, S. Kim, H. Cho, J. Moon, SAMSUNG Electronics Co., Ltd. (South Korea)[6518-80]
- ✓ **Methodical approach to improve defect detection sensitivity on lithography process using DUV inspection system**, C. Lee, S. Won, D. Seo, H. S. Kim, Hynix Semiconductor Inc. (South Korea); J. Yeo, Applied Materials (Israel); C. Kwak, Applied Materials Korea (South Korea)[6518-81]
- ✓ **Etch process monitoring by electron-beam wafer inspection**, M. A. McCord, KLA-Tencor Corp.; A. Tsai, KLA-Tencor Corp. (Taiwan); I. De, A. Kang, KLA-Tencor Corp.; L. Lin, J. Chen, W. Wong, Powerchip Semiconductor Corp. (Taiwan)[6518-82]
- ✓ **Immersion-induced defects SEM-based library for fast baseline improvement and excursion monitoring**, I. Englard, Applied Materials BV (Netherlands); P. Vanoppen, E. Van Brederode, R. Stegen, T. Der Kinderen, O. Tanriseven, I. Lamers, M. B. Mantecon, R. Moerman, ASML Netherlands B.V. (Netherlands); R. Piech, Applied Materials France SARL (France); E. Valfer, L. Levin, Applied Materials (Israel)[6518-83]
- ✓ **Novel technology of automatic macro inspection for 32-nm node and best focus detection**, K. Endo, T. Omori, K. Fukazawa, Nikon Corp. (Japan); K. Yoshino, Y. Yamazaki, Toshiba Corp. (Japan) [6518-85]
- ✓ **Results from a new die-to-database reticle inspection system**, W. H. Broadbent, Y. Xiong, M. Giusti, R. Walsh, A. Dayal, KLA-Tencor Corp.[6518-86]
- ✓ **Optimization of wafer fab contamination inspection methodology for sub-65-nm node reticles**, R. J. Dover, Y. Xiong, J. D. Miller, G. A. Inderhees, KLA-Tencor Corp.[6518-87]
- ✓ **Inspection sensitivity improvement through optimization of lobe blocking on high-end memory devices**, C. Lee, S. Won, D. Seo, H. S. Kim, Hynix Semiconductor Inc. (South Korea); J. Yeo, W. Amir, Applied Materials (Israel); C. Kwak, Applied Materials Korea (South Korea)[6518-88]
- ✓ **Use of automated EBR metrology inspection to optimize the edge bead process**, A. P. Carlson, T. Le, A. Pai, Rudolph Technologies, Inc.[6518-89]
- ✓ **High-throughput polarization imaging for defocus and dose inspection for production wafers**, G. Sun, Y. Liu, Y. Fu, E. Onoichenco, O. Perez, R. Amell, R. Reddy, M. Guest, Rudolph Technologies, Inc.[6518-90]
- ✓ **Real-time spatial control of photoresist development rate**, A. E. B. Tay, W. K. Ho, N. Hu, C. Kiew, National Univ. of Singapore (Singapore)[6518-91]
- ✓ **A general predictive method to analyze spatial distribution of process variables**, Y. Chen, VIGMA Nanoelectronics[6518-92]
- ✓ **Advanced process control for hyper-NA lithography based on CD-SEM measurement**, T. Ishimoto, Hitachi High-Technologies Corp. (Japan); G. Storms, D. Laidler, S. Y. Cheng, IMEC (Belgium); N. Hasegawa, T. Maeda, K. Watanabe, Hitachi High-Technologies Corp. (Japan); K. Sekiguchi, Hitachi High Technologies Corp. (Germany)[6518-93]
- ✓ **Application of integrated scatterometry (iODP) to detect and quantify resist profile changes due to resist batch changes in a production environment**, S. Ali, L. Chen, J. E. Tiffany, A. Yadav, Qimonda AG; B. Swain, D. Dixon, S. J. Lickteig, Tokyo Electron America, Inc.[6518-94]
- ✓ **Litho cell control using MPX**, E. M. Apelgren, H. Kennemer, Spansion Inc.; J. C. Robinson, B. J. Eichelberger, C. Nelson, KLA-Tencor Corp.[6518-95]
- ✓ **Data sharing system for lithography APC**, E. Kawamura, Y. Teranishi, M. Shimabara, Fujitsu Labs. (Japan)[6518-96]
- ✓ **CD measurement in flash memory using substrate current technology**, Y. Ko, Fab Solutions, Inc.; K. Yamada, T. Ushiki, Fab Solutions, Inc. (Japan)[6518-97]
- ✓ **Overlay metrology for dark hard mask process: simulation and experiment study**, J. Shin, R. Chalykh, H. Kang, S. Kim, S. Lee, H. Cho, SAMSUNG Electronics Co., Ltd. (South Korea)[6518-98]
- ✓ **In-chip overlay metrology of 45-nm and 55-nm process wafers**, Y. Ku, H. Pang, C. Tung, Y. Lee, Industrial Technology Research Institute (Taiwan); N. P. Smith, L. Binns, Nanometrics Inc.[6518-100]
- ✓ **Evaluation of novel overlay targets for thin film head application**, Y. X. Li, G. Etheridge, G. Finken, D. Louder, Seagate Technology; A. J. Fan, KLA-Tencor Corp.[6518-101]
- ✓ **Through-focus technique for overlay metrology**, A. Liu, Y. Ku, Industrial Technology Research Institute (Taiwan); N. P. Smith, Nanometrics Inc. (Taiwan)[6518-102]
- ✓ **Improvement of front-end process overlay in 60-nm DRAM**, Y. Hwang, W. Ma, Hynix Semiconductor Inc. (South Korea) ...[6518-103]
- ✓ **Hardware materials and parameters optimization for improvement of immersion overlay**, W. Ma, Y. Hwang, Hynix Semiconductor Inc. (South Korea)[6518-104]
- ✓ **Sampling optimization for advanced overlay process control**, S. Maejima, Renesas Technology Corp. (Japan); A. Kato, KLA-Tencor Japan Ltd. (Japan); P. Izikson, KLA-Tencor Corp. (Israel); A. Widmann, KLA-Tencor Corp.; A. Marchelli, KLA-Tencor Corp. (Israel); J. C. Robinson, KLA-Tencor Corp.[6518-18]
- ✓ **45-nm design rule in-die overlay metrology on immersion lithography processes**, Y. Shih, G. Huang, C. Yu, United Microelectronics Corp. (Taiwan); M. Adel, P. Izikson, KLA-Tencor Corp. (Israel); K. Huang, KLA-Tencor Corp.; E. Kassl, KLA-Tencor Corp. (Israel); S. Mathur, C. Huang, D. Tien, KLA-Tencor Corp.; Y. Avrahamov, KLA-Tencor Corp. (Israel)[6518-106]
- ✓ **Say good-bye to DOF: statistical process window analysis with inline lithographic process variations**, W. Zhou, M. Tang, H. Koh, M. Zhou, Chartered Semiconductor Manufacturing Ltd. (Singapore)[6518-107]
- ✓ **Use in-line AFM as LWR verification tool in 45-nm process development**, M. Hsieh, K. H. Shi, J. Yeh, M. Tsai, S. F. Tzou, United Microelectronics Corp. (Taiwan)[6518-108]
- ✓ **Die-to-database verification tool for detecting CD errors, which are caused by OPC features, by using mass gate measurement and layout information**, T. Kitamura, NanoGeometry Research Inc. (Japan)[6518-109]
- ✓ **Major trends in extending CD-SEM utility**, B. D. Bunday, J. A. Allgair, International SEMATECH Manufacturing Initiative; L. R. Page, A. Danilevsky, C. Parker, Hitachi High Technologies America, Inc.; K. Yang, S. Koshihara, H. Morokuma, Hitachi High-Technologies Corp. (Japan)[6518-112]
- ✓ **Stochastic simulation of material and process effects on the patterning of complex layouts with e-beam and EUV lithography**, D. Drygiannakis, N. Tsirikas, G. P. Patsis, G. Kokkoris, I. Raptis, E. Gogolides, Institute of Microelectronics (Greece)[6518-115]
- ✓ **Macro CD contact ellipticity measurements for lithography tool qualification**, I. Englard, Applied Materials BV (Netherlands); P. Vanoppen, E. van Setten, G. Janssen, ASML Netherlands B.V. (Netherlands); O. Adan, R. Kris, A. Tam, Applied Materials (Israel)[6518-116]
- ✓ **Sub-nanometer CD-SEM matching**, T. A. Lott, R. J. Elias, V. Phanthanivong, Cypress Semiconductor Corp.; G. Grover, S. Elling, Applied Materials, Inc.[6518-117]
- ✓ **Visible light angular scatterometry for nanolithography**, R. M. Alassaad, W. Hu, L. Tao, The Univ. of Texas at Dallas[6518-118]
- ✓ **Robust sub-50-nm CD control by a fast-goniometric scatterometry technique**, J. Hazart, P. Barritault, Commissariat à l'Énergie Atomique (France); A. Lagrange, Lab. d'Électronique de Technologie de l'Information (France); P. M. Boher, ELDIM (France)[6518-119]

- ✓ **Accurate and reliable optical CD of MuGFET down to 10nm**, P. J. Leray, G. F. Lorusso, S. Y. Cheng, N. Collaert, M. Jurczak, IMEC (Belgium); S. S. Shirke, M. Tortonese, VLSI Standards, Inc. . [6518-120]
- ✓ **OCD metrology by floating n/k**, S. Yu, J. Huang, C. Ke, T. Gau, B. J. Lin, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan) [6518-121]
- ✓ **In-die critical dimension metrology using beam profile ellipsometry and reflectometry**, J. L. Opsal, H. Pois, Therma-Wave, Inc. [6518-123]
- ✓ **Mask global CD uniformity enhancement by removing local CD variation on mask**, Y. Choi, M. Kim, O. Han, Hynix Semiconductor Inc. (South Korea) [6518-126]
- ✓ **Achievement of sub-nm reproducibility for length measurements over 300 mm using the PTB's nanometer comparator**, R. G. J. Koenig, J. Flügge, H. Bosse, Physikalisch-Technische Bundesanstalt (Germany) [6518-128]
- ✓ **Aera193i: aerial imaging mask inspection for immersion lithography**, Y. Zabar, Applied Materials; C. Braude, S. Mangan, Applied Materials (Israel); D. L. Rost, Micron Technology, Inc. [6518-129]
- ✓ **Critical dimension measurements on phase-shift masks with reproducibility below 2 nanometers using an optical pattern placement metrology tool**, H. Bittner, D. K. Adam, J. Bender, A. Boesser, M. Heiden, K. Röth, Vistec Semiconductor Systems GmbH (Germany) [6518-130]
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- ✓ **Advanced CD-AFM probe tip-shape characterization for metrology accuracy and throughput**, H. Liu, J. R. Osborne, M. Osborn, G. A. Dahlen, Veeco Metrology LLC [6518-134]
- ✓ **Validation of CD-AFM image reconstruction using TEM as the reference metrology system**, G. A. Dahlen, L. Mininni, M. Osborn, H. Liu, J. R. Osborne, Veeco Metrology LLC [6518-135]
- ✓ **An advanced AFM sensor: its profile accuracy and low-probe-wear property for high-aspect ratio patterns**, M. Watanabe, S. Baba, T. Nakata, Hitachi, Ltd. (Japan); T. Kurenuma, Y. Kunitomo, M. Edamura, Hitachi Kenki FineTech Co., Ltd. (Japan) [6518-137]
- ✓ **A new in-line AFM metrology tool best suitable for LSI manufacturing in the 45-nm node and beyond**, M. Edamura, Y. Kunitomo, T. Morimoto, T. Kurenuma, S. Satoshi, Y. Kembo, Hitachi Kenki FineTech Co., Ltd. (Japan); M. Watanabe, S. Baba, K. Hidaka, Hitachi, Ltd. (Japan) [6518-139]
- ✓ **Magnification calibration standards for sub-100-nm metrology**, S. J. Deo, D. C. Joy, The Univ. of Tennessee [6518-140]
- ✓ **CD-AFM scan algorithm enhancements**, L. Mininni, Veeco Metrology LLC; J. Foucher, Lab. d'Electronique de Technologie de l'Information (France); M. Osborn, Veeco Metrology LLC [6518-141]
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- ✓ **Optical characterization of high-aspect-ratio of microstructures**, S. Tamulevicius, T. Tamulevicius, G. Janusas, M. Andrulevicius, V. Ostasevicius, A. Palevicius, Kauno Technologijos Univ. (Lithuania) [6518-143]
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- ✓ **Optimization of lithography process to improve image deformation of contact hole sub-90-nm technology node**, S. Jun, J. Kim, E. Jeong, Y. Yun, J. Kim, K. Kim, Dongbu Electronics Co., Ltd. (South Korea) [6518-146]
- ✓ **Pore-filling dynamics for nano-imprint lithography**, S. Chauhan, K. Jen, F. L. Palmieri, C. Taylor, G. Willson, The Univ. of Texas at Austin [6518-147]
- ✓ **Resolution enhancement technique using oxidation process with nitride hardmask process**, E. Jeong, J. Kim, K. Kim, Dongbu Electronics Co., Ltd. (South Korea) [6518-148]
- ✓ **Process development to improve subresolution size of hole shape in ArF lithography for flash devices**, Y. Jeon, S. Jun, S. Lee, J. Kim, Y. Lee, K. Kim, Dongbu Electronics Co., Ltd. (South Korea) . . . [6518-150]
- ✓ **Capacitive sensor for optical measurement and monitoring**, S. Shi, Shanghai Institute of Optics and Fine Mechanics (China) . . . [6518-152]
- ✓ **Purge micro-environment with ionized air to reduce chances of ESD damages to reticles/wafers**, H. Wang, Y. Liu, Entegris, Inc. [6518-153]
- ✓ **Monitoring airborne molecular contamination: a quantitative and qualitative comparison of real-time and grab-sampling techniques**, A. M. Shupp, Particle Measuring Systems, Inc. [6518-154]
- ✓ **Improved optics life with continuous parts per trillion contamination analysis and control**, L. Rabellino, SAES Pure Gas, Inc. . . . [6518-155]
- ✓ **Optimizing surface finishing processes**, M. W. Quillen, Eastman Chemical Co.; J. Moore, DAETEC; P. L. Holbrook, Eastman Chemical Co. [6518-156]
- ✓ **New filter media development for effective control of trimethylsilanol and related low-molecular weight silicon containing organic species in the photobay ambient**, A. Grayfer, O. P. Kishkovich, F. V. Belanger, P. Cate, D. J. Ruede, Entegris, Inc. [6518-157]
- ✓ **Noncontacting electrostatic voltmeter for wafer potential monitoring**, M. A. Noras, W. A. Maryniak, TREK, Inc. [6518-158]
- ✓ **Optimized molecular contamination monitoring for lithography**, D. Rodier, Particle Measuring Systems, Inc. [6518-159]
- ✓ **The novel advanced process control to eliminate AlCu-PVD induced overlay shift**, C. Huang, C. Yang, E. T. Yang, T. Yang, K. Chen, J. Ku, C. Lu, Macronix International Co., Ltd. (Taiwan) [6518-160]
- ✓ **Low-pressure drop filtration of airborne molecular organic contaminants using open-channel networks**, A. J. Dallas, J. D. Joriman, L. Ding, Donaldson Co., Inc. [6518-161]
- ✓ **Novel method of under etch defect detection for contact layer-based Si substrate using optic wafer inspection tools**, B. Lee, J. Choi, S. Chin, D. Cho, C. Song, SAMSUNG Electronics Co., Ltd. (South Korea) [6518-162]
- ✓ **CD-bias evaluation and reduction in CD-SEM linewidth measurements**, M. Tanaka, C. Shishido, W. Nagatomo, Hitachi, Ltd. (Japan); K. Watanabe, Hitachi High-Technologies Corp. (Japan) [6518-163]
- ✓ **Ellipsometric studies of the absorption of liquid by photoresist**, H. M. Jeong, S. Park, J. Kyung, K. Lee, H. Lee, H. Cheon, I. An, Hanyang Univ. (South Korea); S. Lee, Samsung Electronics Co., Ltd. (South Korea) [6518-164]
- ✓ **Advanced defect definition method using design data**, K. Lim, SEMATECH, Inc.; K. Yang, S. Koshihara, Hitachi High-Technologies Corp. (Japan); D. Patel, SEMATECH, Inc.; L. R. Page, M. Martinez, Hitachi High-Technologies America, Inc. [6518-165]
- ✓ **Image quality improvement in inspection optics using double integrator illumination**, A. Takada, Topcon Corp. (Japan) . . [6518-166]
- ✓ **The study of ADI (after develop inspection) by e-beam**, M. Saito, T. Hayashi, Tokyo Electron Ltd. (Japan); J. Y. Jau, Hermes Microvision, Inc.; J. Lin, Hermes Microvision, Inc. (Taiwan) [6518-167]
- ✓ **Three-dimensional anisotropic semiconductor grooves measurement simulations (scatterometry) using unconditionally stable FDTD for calculation time shortening**, H. Shirasaki, Tamagawa Univ. (Japan) [6518-168]
- ✓ **Metrology of replicated diffractive optics with Mueller polarimetry in conical diffraction**, T. A. Novikova, A. De Martino, P. V. Bulkin, Q. Nguyen, B. Drévillon, École Polytechnique (France); V. V. Popov, A. A. Chumakov, M.V. Lomonosov Moscow State Univ. (Russia) . . [6518-169]
- ✓ **Influence of wafer warpage on photoresist film thickness and extinction coefficient measurements**, A. E. B. Tay, X. Wu, National Univ. of Singapore (Singapore) [6518-170]

- ✓ **Angular scatterometer for line-width roughness measurement**, D. Shyu, Y. Ku, Industrial Technology Research Institute (Taiwan); N. P. Smith, Nanometrics Inc. (Taiwan) [6518-171]
- ✓ **Global and local SEM charging measurement using energy filter**, F. Levitov, G. Eytan, Applied Materials (Israel) [6518-172]
- ✓ **Contact leakage and open monitoring with an advanced e-beam inspection system**, S. Lei, United Microelectronics Corp. (Taiwan) [6518-173]
- ✓ **New simple approach for modeling and on-line identification of piezoelectric stack actuator**, Y. Wang, X. Zhao, W. Chu, Harbin Institute of Technology (China) [6518-174]
- ✓ **Understanding of CD change effect by rework process induced in sub-65-nm and its optimization to minimize**, H. Jeon, C. Shim, J. H. Hong, J. Han, K. Kim, Dongbu Electronics Co., Ltd. (South Korea) [6518-175]
- ✓ **Study on micro-bubble defect induced by RRC coating**, Y. H. Liu, C. Huang, C. Chen, United Microelectronics Corp. (Taiwan) ... [6518-176]
- ✓ **Characterization of resist thinning and profile changes using scatterometry**, J. Fullam, IBM Microelectronics Div.; K. E. Pettilo, IBM Thomas J. Watson Research Ctr. [6518-178]
- ✓ **Contamination removal from collector optics and masks: an essential step for next-generation lithography**, H. J. Shin, W. M. Lytle, S. N. Srivastava, D. N. Ruzic, Univ. of Illinois at Urbana-Champaign [6518-179]
- ✓ **Measurement and experimentation of pellicle's life time on photomask**, S. Park, Y. Kang, S. Kim, J. Park, Hanyang Univ. (South Korea); D. Kim, M. Sin, FST, Inc. (South Korea); H. Oh, Sr., Hanyang Univ. (South Korea) [6518-180]
- ✓ **A new SEM CD operator verified against Monte Carlo simulations**, C. G. Frase, D. J. Grieser, K. Dirscherl, E. Buhr, H. Bosse, Physikalisch-Technische Bundesanstalt (Germany) [6518-181]
- ✓ **Characterization and adjustment of high-performance objectives for DUV applications**, S. Müller-Pfeiffer, L. Koerner, O. R. Falkenstoerfer, H. Lauth, JENOPTIK Laser, Optik, Systeme GmbH (Germany) . [6518-182]
- ✓ **Phame™: a novel phase metrology tool of Zeiss for in-die phase measurements under scanner relevant optical settings**, S. Perlitz, T. Scherübl, Carl Zeiss SMS GmbH (Germany) [6518-183]
- ✓ **Nonlinear methods for overlay control**, M. Kupers, Qimonda Dresden GmbH & Co. OHG (Germany) [6518-184]
- ✓ **Leveraging LER to minimize linewidth measurement uncertainty in a calibration exercise**, J. Robert, G. W. Banke, Jr., IBM Corp.; R. G. Dixon, National Institute of Standards and Technology [6518-185]
- ✓ **A new AFM tip design which provides higher sidewall resolution (LER and CD) and better tip wear**, J. Foucher, Lab. d'Electronique de Technologie de l'Information (France); B. Liu, Veeco Metrology LLC [6518-186]
- ✓ **Köhler illumination analysis for high-resolution optical metrology using 193-nm light**, Y. Sohn, R. M. Silver, National Institute of Standards and Technology [6518-187]
- ✓ **Critical dimension: MEMS road map**, M. Poulingue, Nanometrics Inc. (France); P. Knutrud, Nanometrics Inc. [6518-188]
- ✓ **Enabling gate etch process development using scatterometry**, J. S. Koshy, IBM Corp.; M. Sendelbach, IBM Microelectronics Div.; A. Munoz, IBM Corp.; P. P. Herrera, KLA-Tencor Corp. [6518-189]
- ✓ **Extending high-speed optical metrology less than 20-nm resolution with stimulated emission depletion-stimulated anti-Stokes Raman spectroscopic imaging (sted-STARS)**, R. D. Frankel, Chromaplex, Inc. and RDF Consulting [6518-190]
- ✓ **ArF pellicle degradation mechanism for resolving CD variation**, H. Choi, Y. Ahn, J. Ryu, Y. Lee, S. Lee, B. An, J. Choi, SAMSUNG Electronics Co. (South Korea) [6518-191]
- ✓ **Effect and procedures of post-exposure bake temperature optimization on the CD uniformity in a mass production environment**, K. Ruck, H. Weichert, Tokyo Electron Europe Ltd. (Germany); S. R. Hornig, F. Finger, G. Fleischer, Qimonda Dresden GmbH & Co. OHG (Germany); D. Hetzer, Timbre Technologies, Inc. and Tokyo Electron Europe Ltd. (Germany) [6518-192]
- ✓ **Qualification and analysis of scatterometry measurements of polysilicon gate profiles in a 90-nm logic process**, E. B. Maiken, Intel Corp. [6518-193]
- ✓ **Mask CD control (CDC) with ultrafast laser for improving mask CDU using AIMS as the CD metrology data source**, E. Zait, G. Ben-Zvi, V. J. Dmitriev, S. V. Oshemkov, G. Gottlieb, Pixar Technology Ltd. (Israel); T. Scherübl, R. Birkner, W. Degel, Carl Zeiss SMS GmbH (Germany) [6518-196]
- ✓ **Verification of CHARIOT Monte Carlo software used for modeling of CD-SEM and defect inspection**, H. Abe, Toshiba Corp. (Japan); S. V. Babin, S. Borisov, Abeam Technologies; A. Hamaguchi, Toshiba Corp. (Japan); A. Ivanchikov, Abeam Technologies; Y. Miyano, Toshiba Corp. (Japan); I. Ruzavin, Abeam Technologies; Y. Yamazaki, Toshiba Corp. (Japan) [6518-197]
- ✓ **Operator independent measurement of beam size using BEAMETR technique**, S. V. Babin, Abeam Technologies; M. Gaevski, Univ. of South Carolina; D. C. Joy, The Univ. of Tennessee; M. Machin, A. Martynov, Abeam Technologies [6518-198]
- ✓ **Scatterometry solutions and a vision for lithography advanced process control**, T. Y. Levin, Intel Electronics Ltd. (Israel) ... [6518-199]
- ✓ **ODP scatterometry for alternating phase-shift masks**, K. M. Lee, M. Tavassoli, K. Baik, S. E. Henrichs, Intel Corp.; S. K. Yedur, Timbre Technologies, Inc. [6518-200]
- ✓ **Implementation strategies and the return on investment for integrated CD control**, L. Lane, B. Monteverde, Timbre Technologies, Inc. [6518-201]

Tuesday 27 February

SESSION 4

Room: Conv. Ctr. J2 Tues. 8:00 to 10:10 am

Overlay

Chairs: Alexander Starikov, Intel Corp.; Daniel J. C. Herr, Semiconductor Research Corp.

- 8:00 am: **Meeting overlay requirements for future technology nodes with in-die overlay metrology** (*Invited Paper*), B. Schulz, R. Seltmann, J. Busch, F. Hempel, AMD Saxony LLC & Co. KG (Germany); E. P. Cotte, Advanced Mask Technology Ctr. (Germany); B. Alles, Technische Univ. München (Germany) [6518-13]
- 8:30 am: **Zero-order imaging of device-sized overlay targets using scatterfield microscopy**, B. M. Barnes, R. Attota, L. P. Howard, J. Jun, R. M. Silver, National Institute of Standards and Technology; P. Lipscomb, KLA-Tencor Corp. [6518-14]
- 8:50 am: **Blossom overlay metrology implementation**, C. P. Ausschnitt, W. Chu, J. L. Morningstar, IBM Microelectronics Div.; L. A. Binns, N. P. Smith, Nanometrics, Inc. [6518-15]
- 9:10 am: **The application of SMASH alignment system for 65-55-nm logic devices**, M. Miyasaka, H. Saito, T. Tamura, T. Uchiyama, NEC Electronics Corp. (Japan); P. C. Hinnen, H. Lee, M. van Kemenade, M. Shahrjerdy, R. van Leeuwen, ASML Netherlands B.V. (Netherlands) [6518-16]
- 9:30 am: **Overlay metrology tool calibration**, L. A. Binns, Accent Optical Technologies, Inc. (United Kingdom); N. P. Smith, Hermes-Epitek Corp. (Taiwan) and Nanometrics, Inc. (United Kingdom); G. Ananew, P. Dasari, Nanometrics, Inc. (United Kingdom); J. L. Morningstar, C. P. Ausschnitt, C. Thomison, R. J. Yerdon, IBM Microelectronics Div. [6518-17]
- 9:50 am: **Improved overlay control through automated high-order compensation**, J. C. Robinson, KLA-Tencor Corp.; S. Maejima, Renesas Technology Corp. (Japan); Y. Ishii, S. Wakimoto, K. Yasukawa, A. Sukegawa, Nikon Corp. (Japan); A. Kato, KLA-Tencor Japan Ltd. (Japan); B. J. Eichelberger, KLA-Tencor Corp.; P. Izikson, KLA-Tencor Corp. (Israel) [6518-105]
- Coffee Break 10:10 to 10:40 am

SESSION 5

Room: Conv. Ctr. J2 Tues. 10:40 am to 12:30 pm

CDSEM: Techniques, Limits, Etc.

Chairs: David C. Joy, The Univ. of Tennessee; *Byoung-Ho Lee*, SAMSUNG Electronics Co., Ltd. (South Korea)

10:40 am: **Monte Carlo modeling of secondary electron imaging in three dimensions** (*Invited Paper*), J. S. Villarrubia, N. W. M. Ritchie, J. R. Lowney, National Institute of Standards and Technology [6518-19]

11:10 am: **Evaluation of CD-SEM measurement uncertainty using secondary electron simulation with charging effect**, H. Abe, A. Hamaguchi, Y. Yamazaki, Toshiba Corp. (Japan) [6518-20]

11:30 am: **Characterization of photo-resist dimension at virgin state and line sliming effect using in-line CDSEM**, L. Zhou, E. P. Solecky, C. J. Wu, IBM Corp. [6518-21]

11:50 am: **Carbon nanotube metrology in a CD SEM**, C. Yates, ON Semiconductor; T. Rueckes, Nantero, Inc. [6518-22]

12:10 pm: **Physical matching versus CD matching for CD SEM**, R. Kris, O. Zoran, S. Dror, Applied Materials (Israel) [6518-23]

Lunch/Exhibition Break 12:30 to 1:30 pm

SESSION 6

Room: Conv. Ctr. J2 Tues. 1:30 to 3:10 pm

Inspection

Chairs: Brian M. Trafas, KLA-Tencor Corp.; *Michael W. Stan*, MicroChem Corp.

1:30 pm: **Developing the new ADC algorithm that enables to identify the defect source**, P. Tsai, W. Chiu, T. Chen, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan); F. Endo, Y. Kariya, K. Nemoto, Hitachi High-Technologies Corp. (Japan) [6518-24]

1:50 pm: **Developing μ ADI methodology for new litho process monitoring strategies**, I. Maege, U. Seifert, Qimonda Dresden GmbH & Co. OHG (Germany); B. Saville, KLA-Tencor England (United Kingdom); M. Tuckermann, KLA-Tencor Germany (Germany) [6518-25]

2:10 pm: **Studies on EUV mask storage and contamination problem by EUV reflectometer and optical measurement tool**, S. Cho, H. Kim, S. Moon, D. Kim, SAMSUNG Advanced Institute of Technology (South Korea); J. Lee, S. Choi, SAMSUNG Electronics Co., Ltd. (South Korea) [6518-26]

2:30 pm: **Immersion lithography defectivity analysis at DUV**, E. Golan, Applied Materials, Inc.; S. Brandl, Infineon Technologies North America; B. Pierson, ASML US, Inc.; W. Montgomery, Albany NanoTech; D. Meshulach, N. Raccach, Applied Materials (Israel); O. Dassa, Applied Materials, Inc.; J. Yeo, Applied Materials (Israel) [6518-27]

2:50 pm: **Innovative inspection metrology for wafer edge defectivity in immersion lithography**, I. K. A. Pollentier, IMEC (Belgium); M. K. Kocsis, Intel Corp.; S. Vedula, A. Somanchi, F. Burkeen, KLA-Tencor Corp. [6518-28]

Coffee Break 3:10 to 3:40 pm

SESSION 7

Room: Conv. Ctr. J2 Tues. 3:40 to 5:50 pm

Scatterometry Techniques, Limits, Etc.

Chairs: Christopher J. Raymond, Accent Optical Technologies, Inc.; *Jason P. Cain*, Advanced Micro Devices, Inc.

3:40 pm: **A comprehensive study on the limits of optical critical dimension metrology** (*Invited Paper*), R. M. Silver, T. A. Germer, R. Attota, B. M. Barnes, National Institute of Standards and Technology; B. D. Bunday, J. A. Allgair, International SEMATECH Manufacturing Initiative [6518-29]

4:10 pm: **Detailed analysis of capability and limitations of CD scatterometry measurements for 65- and 45-nm nodes**, I. Pundaleva, R. Chalykh, J. Lee, S. Choi, W. Han, SAMSUNG Electronics Co., Ltd. (South Korea) [6518-30]

4:30 pm: **Real-time profile shape reconstruction using dynamic scatterometry**, S. Soulan, M. Besacier, L. Vallier, P. Schiavone, Ctr. National de la Recherche Scientifique (France) [6518-31]

4:50 pm: **Mueller polarimetry in the back focal plane**, A. De Martino, École Polytechnique (France) [6518-32]

5:10 pm: **Realizing design-based metrology**, J. A. Allgair, N. Langdon, Freescale Semiconductor, Inc.; P. Proctor, FabSolve LLC; D. Schraub, Freescale Semiconductor, Inc. [6518-194]

5:30 pm: **Modeling the effect of line and trench profile variation on scatterometry measurements**, T. A. Germer, National Institute of Standards and Technology [6518-34]

Wednesday 28 February

SESSION 8

Room: Conv. Ctr. J2 Wed. 8:00 to 10:00 am

Standards and Techniques

Chairs: Bhanwar Singh, Advanced Micro Devices, Inc.; *Vladimir A. Ukraintsev*, Texas Instruments Inc.

8:00 am: **TEM calibration methods for critical-dimension standards**, N. G. Orji, R. G. Dixon, National Institute of Standards and Technology; B. D. Bunday, J. A. Allgair, International SEMATECH Manufacturing Initiative [6518-35]

8:20 am: **Image simulation and surface reconstruction of undercut features in atomic force microscopy**, X. Qian, Illinois Institute of Technology; J. S. Villarrubia, National Institute of Standards and Technology [6518-36]

8:40 am: **Statistical approach utilizing nonlinear regression for CD error prediction**, M. Asano, S. Tanaka, H. Fujise, S. Mimotogi, Toshiba Corp. (Japan) [6518-37]

9:00 am: **X-ray reflectivity and scattering for pattern shape metrology**, H. Lee, C. L. Soles, H. W. Ro, S. Kang, R. L. Jones, E. K. Lin, A. Karim, W. Wu, National Institute of Standards and Technology; D. R. Hines, Univ. of Maryland/College Park [6518-38]

9:20 am: **Accuracy in optical image modeling**, J. E. Potzick, E. Marx, National Institute of Standards and Technology; M. P. Davidson, Spectel Research Corp. [6518-39]

9:40 am: **Single crystal critical dimension reference materials (SCDRM): process optimization for the next-generation of standards**, R. G. Dixon, W. F. Guthrie, M. W. Cresswell, R. A. Allen, N. G. Orji, National Institute of Standards and Technology [6518-40]

Coffee Break 10:00 to 10:30 am

SESSION 9

Room: Conv. Ctr. J2 Wed. 10:30 am to 12:10 pm

Reference Metrology and Instruments

Chairs: Richard M. Silver, National Institute of Standards and Technology; *Michael J. Anderson*, Rohm and Haas Electronic Materials

10:30 am: **Comparison and uncertainties of standards for CD-AFM width calibration**, R. G. Dixon, N. G. Orji, National Institute of Standards and Technology; M. Tortonesi, S. S. Shirke, VLSI Standards, Inc. [6518-41]

10:50 am: **An investigation of atomic force microscopy to measure spacer and dual-stress liner profiles**, D. Shneyder, IBM Corp.; S. Panda, Indian Institute of Technology Kanpur (India); B. Tessier, IBM Corp.; R. Jagannathan, IBM Microelectronics Div. [6518-42]

11:10 am: **Use of carbon nanotube probes in a critical-dimension atomic force microscope**, B. C. Park, Korea Research Institute of Standards and Science (South Korea); J. Choi, Korea Research Institute of Standards and Science (South Korea) and Chungnam National Univ. (South Korea); S. J. Ahn, D. Kim, Korea Research Institute of Standards and Science (South Korea); J. Lyou, Chungnam National Univ. (South Korea); R. G. Dixon, J. Fu, T. V. Vorburger, National Institute of Standards and Technology [6518-43]

11:30 am: **Profiles of buried and surface relief gratings determined by spectroscopic scatterometry and atomic force microscopy**, P. Hansen, L. K. Nielsen, J. Garnæs, M. Lang, J. C. Petersen, Danish Fundamental Metrology (Denmark); L. H. Thamdrup, A. Mironov, B. B. Olsen, Technical Univ. of Denmark (Denmark); A. Kristensen, Danmarks Tekniske Univ. (Denmark) [6518-44]

11:50 am: **In-line AFM characterization of STI profile at the 65-nm node with advanced carbon probes**, M. D. Sardo, STMicroelectronics (France); A. Berthoud, Philips Semiconductors (France); J. Royer, Lab. d'Electronique de Technologie de l'Information (France); C. Kusch, nanotools GmbH (Germany) [6518-45]

Lunch/Exhibition Break 12:10 to 1:10 pm

SESSION 10

Room: Conv. Ctr. J2 Wed. 1:10 to 2:50 pm

Metrology Challenges

Chairs: Alexander Starikov, Intel Corp.; *Ofer Adan*, Applied Materials (Israel)

1:10 pm: **Impact of thin film metrology on the lithographic performance of 193-nm bottom antireflective coatings**, C. A. Mack, Lithguru.com; D. A. Harrison, C. Rivas, Metrosol, Inc. [6518-46]

1:30 pm: **Dielectric-thickness dependence of damage induced by electron-beam irradiation of MNOS gate pattern**, M. Matsui, T. Mine, K. Hozawa, Hitachi, Ltd. (Japan); J. Inoue, H. Nagaishi, Renesas Technology Corp. (Japan) [6518-47]

1:50 pm: **OPC model data collection for 45-nm technology node using automatic CD-SEM offline recipe creation**, D. S. Fischer, M. Talbi, A. Wei, IBM Microelectronics Div.; O. Menadeva, Z. Abraham, Applied Materials (Israel); R. S. Cornell, Applied Materials [6518-48]

2:10 pm: **Optical line-width measurement below 50 nm**, C. W. See, R. J. Smith, M. G. Somekh, The Univ. of Nottingham (United Kingdom); A. Yacoot, National Physical Lab. (United Kingdom) [6518-49]

2:30 pm: **Metrology challenges for advanced lithography techniques**, I. England, Applied Materials BV (Netherlands); J. M. Finders, P. Vanoppen, J. Meessen, F. Duray, G. Janssen, ASML Netherlands B.V. (Netherlands); C. Masia, Applied Materials BV (Netherlands); R. Piech, Applied Materials France SARL (France); L. Gershtein, R. Peltinov, O. Adan, Applied Materials (Israel) [6518-50]

Coffee Break 2:50 to 3:20 pm

SESSION 11

Room: Conv. Ctr. J2 Wed. 3:20 to 5:40 pm

New Trends in Metrology

Chairs: David C. Joy, The Univ. of Tennessee; *Vladimir A. Ukraintsev*, Texas Instruments Inc.

3:20 pm: **Transition from precise to accurate critical dimension metrology (Invited Paper)**, V. A. Ukraintsev, Texas Instruments Inc. [6518-51]

3:50 pm: **Device metrology with high-performance scanning ion beams**, D. C. Joy, The Univ. of Tennessee and Oak Ridge National Lab.; J. Notte, R. Hill, B. Ward, ALIS Corp. [6518-52]

4:10 pm: **Beyond measurement uncertainty: improving the productivity of metrology tools**, E. P. Solecky, IBM Corp. [6518-53]

4:30 pm: **Realizing value-added metrology (Invited Paper)**, B. D. Bunday, International SEMATECH Manufacturing Initiative; E. P. Solecky, C. N. Archie, IBM Corp.; J. A. Allgair, International SEMATECH Manufacturing Initiative; M. A. Caldwell, Freescale Semiconductor, Inc.; B. J. Rice, SEMATECH, Inc.; B. Singh, I. Emami, Advanced Micro Devices, Inc.; G. W. Banke, Jr., IBM Corp. [6518-54]

5:00 pm: **Improved dimension and shape metrology with versatile atomic force microscopy**, M. A. Caldwell, Freescale Semiconductor, Inc.; T. Bao, Veeco Instruments, Inc.; J. Hackenberg, B. E. McLain, O. Munoz, T. Stephens, V. Vartanian, Freescale Semiconductor, Inc. [6518-138]

5:20 pm: **Enabling immersion lithography and double patterning for memory devices**, K. M. Monahan, KLA-Tencor Corp. [6518-56]

Panel Discussion

Room: Conv. Ctr. C1 Wed. 8:00 to 9:30 pm

New Frontiers in Overlay Metrology

Moderators: Timothy A. Brunner, IBM Thomas J. Watson Research Ctr.; *Harry J. Levinson*, Advanced Micro Devices, Inc.

Panelists: William H. Arnold, ASML Netherlands B.V.; *Masaomi Kameyama*, Nikon Corp.; *Christopher P. Ausschnitt*, IBM Microelectronics Div.; *Nigel P. Smith*, Nanometrics Inc.; *Michael E. Adel*, KLA-Tencor Corp.; *Richard M. Silver*, National Institute of Standards and Technology; *Pete Lipscomb*, SEMATECH

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We have entered a new era in overlay. Overlay measurements are about to become substantially further complicated with the introduction of double patterning techniques. In-chip overlay will need to be measured routinely in development and possibly in manufacturing. Target design directly affects overlay tool performance and the ability to accurately monitor overlay. New target designs are significantly more complicated from an optics and measurement perspective. Arrayed target designs, device size targets, in chip overlay, and dummy fill surrounded targets all introduce critical performance challenges. There is substantially reduced collaboration as a result of the trend to proprietary target designs. Do we need a new technology to achieve the advanced overlay requirements or an industry wide collaboration and standardization to move in a more unified direction?

Participants include experts from government laboratories and the semiconductor industry.

Thursday 1 March

SESSION 12

Room: Conv. Ctr. J2 Thurs. 8:00 to 10:00 am

Line-edge and Line-width Roughness

Chairs: Bhanwar Singh, Advanced Micro Devices, Inc.; *Neal T. Sullivan*, Arradiance, Inc.

8:00 am: **Correlation length and the problem of line-width roughness**, V. Constantoudis, G. P. Patsis, E. Gogolides, Institute of Microelectronics (Greece) [6518-57]

8:20 am: **Line-edge roughness and cross sectional characterization of sub-50-nm structures using CD-SAXS**, R. L. Jones, C. Wang, E. K. Lin, W. Wu, J. S. Villarrubia, National Institute of Standards and Technology; K. Choi, J. S. Clarke, B. J. Rice, M. J. Leeson, J. M. Roberts, R. L. Bristol, Intel Corp.; B. D. Bunday, International SEMATECH Manufacturing Initiative [6518-195]

8:40 am: **Characterization of line-edge roughness in Cu/low-k interconnect pattern**, A. Yamaguchi, D. Ryuzaki, J. Yamamoto, Hitachi, Ltd. (Japan); H. Kawada, T. Iizumi, Hitachi High-Technologies Corp. (Japan) [6518-59]

9:00 am: **Impact of acid diffusion length on resist LER and LWR measured by CD-AFM and CD-SEM**, J. Foucher, CEA/ LETI (France); A. Pikon, C. E. Andes, J. W. Thackeray, Rohm and Haas Electronic Materials [6518-60]

9:20 am: **Advanced edge roughness measurement application for mask metrology**, T. Marschner, J. Richter, U. Dersch, Advanced Mask Technology Ctr. (Germany); D. Chase-Colin, R. Katz, R. Falah, Applied Materials (Israel); T. P. Coleman, Applied Materials, Inc. (France) [6518-61]

9:40 am: **The coming of age of tilt CD-SEM**, B. D. Bunday, J. A. Allgair, International SEMATECH Manufacturing Initiative; E. P. Solecky, C. N. Archie, IBM Corp.; N. G. Orji, National Institute of Standards and Technology; R. Peltinov, O. Adan, M. Bar-Zvi, Applied Materials (Israel) [6518-114]

Coffee Break 10:00 to 10:30 am

SESSION 13

Room: Conv. Ctr. J2 Thurs. 10:30 am to 12:30 pm

Mask Metrology

Chairs: **Martha I. Sanchez**, IBM Almaden Research Ctr.; **Daniel J. C. Herr**, Semiconductor Research Corp.

10:30 am: **Scatterometry on pelliclized masks: an option for wafer fabs**, E. E. Gallagher, IBM Corp.; Y. Okumoto, M. Higuchi, Toppan Electronics; C. Benson, IBM Corp.; M. Kwon, S. Yedur, S. Li, Timbre Technologies, Inc.; S. Lee, Nanometrics Inc. [6518-63]

10:50 am: **Development of advanced mask inspection optics with transmitted and reflected light image acquisition**, R. Hirano, N. Kikui, H. Suzuki, Y. Tsuji, S. Murakami, K. Takahara, R. Ogawa, K. Usuda, Advanced Mask Inspection Technology, Inc. (Japan) [6518-64]

11:10 am: **Real-time monitoring of reticle etch process tool to investigate and predict critical-dimension performance**, R. E. Deming, K. Yung, M. Guglielmana, Intel Corp.; S. Kalicin, Intel Corp.; D. J. Bald, K. Baik, Intel Corp. [6518-65]

11:30 am: **CAD-based line/space mix-up prevention for reticle metrology**, T. Marschner, M. Enger, F. Ludewig, Advanced Mask Technology Ctr. (Germany); R. Falah, S. M. Latinsky, O. Lindman, Applied Materials (Israel); T. P. Coleman, Applied Materials, Inc. (France) [6518-66]

11:50 am: **Aspects and new developments on edge angle and edge profile metrology at PTB**, B. Bodermann, H. Bosse, E. Buhr, A. Diener, K. Dirscherl, G. Ehret, W. Haessler-Grohne, M. Wurm, Physikalisch-Technische Bundesanstalt (Germany) [6518-67]

12:10 pm: **Study of polarization and rigorous effects on phase shifting masks through simulations and in-die phase measurements**, K. M. Lee, M. Tavassoli, M. Lau, Intel Corp.; S. Perlit, T. Scherübl, Carl Zeiss SMS GmbH (Germany) [6518-68]

Lunch Break 12:30 to 1:30 pm

SESSION 14

Room: Conv. Ctr. J2 Thurs. 1:30 to 3:10 pm

Process Control II

Chairs: **Brian M. Trafas**, KLA-Tencor Corp.; **Jason P. Cain**, Advanced Micro Devices, Inc.

1:30 pm: **Advances in process overlay: alignment solutions for future technology nodes**, H. J. L. Megens, R. J. F. van Haren, S. Musa, M. Doytcheva, S. Laibahadoersing, M. van Kemenade, H. Lee, P. C. Hinnen, ASML Netherlands B.V. (Netherlands) [6518-69]

1:50 pm: **Algorithm for lithography advanced process control system for high-mix low-volume products**, E. Kawamura, Fujitsu Labs. (Japan) [6518-70]

2:10 pm: **Advanced process control with design-based metrology**, H. Yang, J. Kim, D. Yim, Hynix Semiconductor Inc. (South Korea) .. [6518-71]

2:30 pm: **Investigation of optimized wafer sampling with multiple integrated metrology modules within photolithography equipment**, T. L. Taylor, Micron Technology, Inc. [6518-72]

2:50 pm: **Advanced lithography parameters extraction by using scatterometry system**, W. Zhou, M. Tang, H. Koh, M. Zhou, Chartered Semiconductor Manufacturing Ltd. (Singapore) [6518-73]

Coffee Break 3:10 to 3:40 pm

SESSION 15

Room: Conv. Ctr. J2 Thurs. 3:40 to 5:20 pm

CD for Development II

Chairs: **John A. Allgair**, SEMATECH, Inc. and Freescale Semiconductors, Inc.; **Chas N. Archie**, IBM Corp.

3:40 pm: **A methodology to evaluate critical-dimension uniformity control for sub-32-nm technology**, Y. Ma, T. I. Wallow, B. M. La Fontaine, H. J. Levinson, Advanced Micro Devices, Inc. [6518-74]

4:00 pm: **Predicting electrical measurements by applying scatterometry to complex spacer structures**, M. Sendelbach, J. Ayala, IBM Microelectronics Div.; P. P. Herrera, KLA-Tencor Corp. [6518-75]

4:20 pm: **Characterization of bending CD errors induced by resist trimming in 65-nm node and beyond**, Y. Gu, J. B. Friedmann, G. Zhang, V. A. Ukraintsev, T. Wolf, T. Lii, R. Jackson, Texas Instruments Inc. [6518-76]

4:40 pm: **Characterization of capacitive 3D deep-trench mask open structures using scatterometry**, S. Zangoie, IBM Microelectronics Div.; P. P. Herrera, KLA-Tencor Corp.; A. Mesfin, IBM Microelectronics Div.; C. N. Archie, IBM Corp.; M. Sendelbach, IBM Microelectronics Div. .. [6518-78]

5:00 pm: **A novel CD-SEM approach to challenges in metrology accuracy**, C. Masia, I. Englard, Applied Materials BV (Netherlands); P. Vanoppen, B. Rijpers, J. Meessen, E. Van Brederode, F. Duray, ASML Netherlands B.V. (Netherlands); O. Adan, L. Gershtein, R. Peltinov, Applied Materials (Israel); R. Piech, Applied Materials France SARL (France) [6518-79]

Courses of Related Interest

Register for courses at the SPIE registration desk.

SC101 Introduction to Microlithography: Theory, Materials, and Processing (Willson, Bowden, Thompson) Sunday 8:30 am to 5:30 pm

SC105 CD Metrology and Image Formation in the Scanning Electron Microscope (SEM) (Wells, Postek) Sunday 8:30 am to 5:30 pm

SC705 Instruments and Methodologies for Accurate Metrology and Fleet Matching (Archie, Banke) Sunday 8:30 am to 5:30 pm

SC831 Introduction to Scatterometry Metrology: Theory and Application (Bao, Barry) Sunday 1:30 to 5:30 pm

SC579 Photomask Fabrication and Technology Basics (Duff) Monday 8:30 am to 5:30 pm

SC832 IP Issues in Advanced Lithography and Semiconductor Manufacturing (Gortych) Monday 1:30 to 5:30 pm

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Monday-Wednesday 26-28 February 2007 • Proceedings of SPIE Vol. 6519

Advances in Resist Materials and Processing Technology XXIV

Conference Chair: **Qinghuang Lin**, IBM Thomas J. Watson Research Ctr.

Cochair: **Clifford L. Henderson**, Georgia Institute of Technology

Program Committee: **George G. Barclay**, Rohm and Haas Electronic Materials; **Scott J. Bukofsky**, IBM Microelectronics Div.; **Sean D. Burns**, IBM Thomas J. Watson Research Ctr.; **Ralph R. Dammel**, AZ Electronic Materials USA Corp.; **Douglas J. Guerrero**, Brewer Science, Inc.; **Christoph K. Hohle**, Qimonda AG (Germany); **Nobuyuki N. Matsuzawa**, Sony Atsugi Technology Ctr. (Japan); **Dahchung Owe-Yang**, Shin-Etsu MicroSi, Inc.; **Kyle Patterson**, Freescale Semiconductor, Inc. (France); **Adam R. Pawloski**, Affymetrix, Inc.; **Vivek M. Prabhu**, National Institute of Standards and Technology; **E. S. Putna**, Intel Corp.; **Mark H. Somervell**, Texas Instruments Inc.; **Gregory M. Wallraff**, IBM Almaden Research Ctr.

Monday 26 February

Opening Remarks

Room: Conv. Ctr. Hall 3 Mon. 11:00 to 11:10 am

Chair: **Qinghuang Lin**, IBM Thomas J. Watson Research Ctr.

Presentation of the C. Grant Willson 2006 Best Paper Award

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SESSION 1

Room: Conv. Ctr. Hall 3 Mon. 11:10 am to 12:30 pm

Invited Session

Chair: **Clifford L. Henderson**, Georgia Institute of Technology

11:10 am: **Identifying the materials limits of chemically amplified photoresists** (*Invited Paper*), E. K. Lin, National Institute of Standards and Technology [6519-01]

11:50 am: **Emerging resist materials** (*Invited Paper*), D. J. C. Herr, Semiconductor Research Corp. [6519-02]

Lunch Break 12:30 to 1:30 pm

SESSION 2

Room: Conv. Ctr. Hall 3 Mon. 1:30 to 3:10 pm

Materials and Processes for Immersion Lithography I

Chairs: **Ralph R. Dammel**, AZ Electronic Materials USA Corp.; **Scott J. Bukofsky**, IBM Microelectronics Div.

1:30 pm: **Fluoro-alcohol materials with tailored interfacial properties for immersion lithography**, D. P. Sanders, L. K. Sundberg, P. J. Brock, R. A. DiPietro, H. D. Truong, R. D. Allen, IBM Almaden Research Ctr. [6519-03]

1:50 pm: **Development of non-topcoat resist polymers for 193-nm immersion lithography**, N. Shirota, Y. Takebe, S. Shu-Zhong, T. Sasaki, O. Yokokoji, Asahi Glass Co., Ltd. (Japan) [6519-04]

2:10 pm: **Progress of topcoat less resist for immersion lithography**, T. Nakamura, Tokyo Ohka Kogyo Co., Ltd. (Japan) [6519-05]

2:30 pm: **Building an immersion topcoat from the ground up: materials perspective**, I. Popova, M. Khojasteh, P. R. Varanasi, IBM Microelectronics Div.; L. K. Sundberg, IBM Almaden Research Ctr.; C. F. Robinson, IBM Corp.; D. A. Corliss, W. Huang, M. C. Lawson, IBM Microelectronics Div.; G. Dabbagh, M. Slezak, JSR Micro, Inc.; M. Colburn, K. E. Petrillo, IBM Thomas J. Watson Research Ctr. [6519-06]

2:50 pm: **Novel materials design for immersion lithography**, K. Wada, Fuji Photo Film Co., Ltd. (Japan) [6519-07]

Coffee Break 3:10 to 3:30 pm

SESSION 3

Room: Conv. Ctr. Hall 3 Mon. 3:30 to 5:30 pm

Materials and Processes for Immersion Lithography II

Chairs: **George G. Barclay**, Rohm and Haas Electronic Materials; **Mark H. Somervell**, Texas Instruments Inc.

3:30 pm: **Novel high-index resists for 193-nm immersion lithography and beyond**, A. K. Whittaker, I. Blakey, H. Liu, D. Hill, The Univ. of Queensland (Australia); G. George, Queensland Univ. of Technology (Australia); J. Forsythe, R. Donovan, Monash Univ. (Australia); W. E. Conley, Freescale Semiconductor, Inc. (France); P. Zimmerman, SEMATECH, Inc. [6519-08]

3:50 pm: **Experimental observations of high-index liquid interaction with resist**, S. V. Postnikov, Infineon Technologies AG (Germany); M. Ercken, P. Foubert, R. Gronheid, E. Hendrickx, C. Jehoul, B. Kim, F. Van Roey, J. Versluijs, N. Vandenbroeck, P. Willems, IMEC (Belgium) [6519-09]

4:10 pm: **High-refractive index materials design for ArF immersion lithography**, T. Furukawa, T. Kishida, T. Miyamatsu, K. Kawaguchi, K. Yamada, T. Tomimaga, JSR Corp. (Japan); M. Slezak, JSR Micro, Inc.; K. Hieda, JSR Corp. (Japan) [6519-10]

4:30 pm: **Adapting immersion exposure to mass production by adopting a cluster of novel resist-coating/developing and immersion-exposure equipment**, T. Fujiwara, J. Ishikawa, T. Kawakubo, Y. Ishii, Nikon Corp. (Japan); H. Kyoda, S. Wakamizu, T. Shimoaoki, Tokyo Electron Kyushu Ltd. (Japan) [6519-11]

4:50 pm: **Immersion defectivity control by optimizing immersion materials and processes**, K. Nakano, H. Kato, S. Owa, Nikon Corp. (Japan) [6519-12]

5:10 pm: **Measurement and evaluation of water uptake by resists, topcoats and stacks, and correlation with watermark defects**, P. Foubert, IMEC (Belgium); M. K. Kocsis, Intel Corp.; K. Nafus, R. Gronheid, N. Vandenbroeck, J. De Backer, M. Ercken, IMEC (Belgium) [6519-13]

✓ Posters-Monday

Room: Convention Ctr. Hall 3 Mon. 5:30 to 8:00 pm

The following posters will be displayed all day Monday. Authors will be present during the formal poster session Monday evening between 5:30 and 8:00 pm for discussion. Authors may set-up their posters after 10:30 am on Monday.

Materials and Processes for Immersion Lithography

- ✓ **Dynamic contact angles of polymer films: detailed structure/property relationships**, L. K. Sundberg, R. D. Allen, D. P. Sanders, R. Sooriyakumaran, P. J. Brock, IBM Almaden Research Ctr. . . . [6519-64]
- ✓ **High-refractive index fluids for second-generation 193-nm immersion lithography**, A. Kagayama, H. Wachi, Y. Namai, S. Fukuda, Mitsui Chemical Analysis & Consulting Service, Inc. (Japan) . . [6519-66]
- ✓ **Mechanism of immersion specific defects with high receding-angle topcoat**, M. Terai, T. Kumada, Mitsubishi Electric Corp. (Japan); T. Ishibashi, T. Hagiwara, T. Hanawa, Renesas Technology Corp. (Japan); T. Ando, Tokyo Ohka Kogyo Co., Ltd. (Japan) [6519-67]
- ✓ **Defectivity reduction studies for ArF immersion lithography**, K. Matsunaga, T. Kondoh, H. Kato, Y. Kobayashi, K. Hayasaki, S. Ito, Toshiba Corp. (Japan); S. Shimura, T. Kawasaki, Tokyo Electron Ltd. (Japan); H. Kyoda, Tokyo Electron Kyushu Ltd. (Japan) [6519-68]
- ✓ **Adjustment of surface property for immersion defect reduction at 65-nm node and beyond**, L. Jang, United Microelectronics Corp. (Taiwan) [6519-69]
- ✓ **Study on the reduction of defects in immersion lithography**, K. Ban, Hynix Semiconductor Inc. (South Korea) [6519-70]
- ✓ **Modified polymer architecture for immersion lithography**, C. S. Park, J. W. Kim, S. S. Kim, J. Y. Lee, S. K. Oh, S. Lee, J. Kim, J. Lee, D. Kim, J. Kim, Dongjin Semichem Co. Ltd. (South Korea); K. Ban, C. K. Bok, S. Moon, Hynix Semiconductor Inc. (South Korea) [6519-71]
- ✓ **Tailoring surface properties of ArF resists thin films with functionally graded materials (FGM)**, I. Takemoto, N. Ando, K. Edamatsu, Y. Fuji, K. Kuwana, K. Hashimoto, H. Yokoyama, Sumitomo Chemical Co., Ltd. (Japan) [6519-72]
- ✓ **Development of top coat materials for ArF immersion lithography**, Y. Takebe, N. Shirota, T. Sasaki, O. Yokokoji, Asahi Glass Co., Ltd. (Japan) [6519-17]
- ✓ **Transfer mechanism of defects on cover material to resist pattern in immersion lithography process and effects on etching process**, N. Takahashi, S. Shimura, T. Kawasaki, Tokyo Electron Ltd. (Japan) [6519-77]
- ✓ **Models for predicting the index of refraction of compounds at 193 nm**, R. L. Brainard, Univ. at Albany; E. Block, SUNY/Univ. at Albany [6519-78]
- ✓ **Outlook for potential third-generation immersion fluids**, J. Lopez Gejo, N. J. Turro, Columbia Univ.; W. E. Conley, Freescale Semiconductor, Inc. (France) [6519-80]
- ✓ **Behavior and effects of water penetration in 193-nm immersion lithography process materials**, T. Niwa, T. Tomita, K. Hontake, M. Enomoto, Tokyo Electron Kyushu Ltd. (Japan); S. A. Scheer, Tokyo Electron America, Inc.; H. Kyoda, J. Kitano, Tokyo Electron Kyushu Ltd. (Japan) [6519-82]
- ✓ **Process optimization for developer soluble immersion topcoat material**, H. Nakagawa, K. Goto, M. Shima, J. Takahashi, T. Shimokawa, JSR Corp. (Japan); K. Ichino, N. Nagatani, H. Kyoda, K. Yoshihara, Tokyo Electron Kyushu Ltd. (Japan) [6519-83]
- ✓ **Defect transfer from immersion exposure process to post processing and defect reduction using novel immersion track system**, O. Miyahara, T. Shimoaoki, S. Wakamizu, J. Kitano, Tokyo Electron Kyushu Ltd. (Japan); Y. Ono, S. Maejima, Renesas Technology Corp. (Japan); T. Hanawa, Mitsubishi Electric Corp. (Japan); K. Suko, Renesas Technology Corp. (Japan) [6519-84]
- ✓ **Effect of polymer sensitivity on immersion defectivity**, S. Lee, J. Kim, J. W. Kim, S. K. Oh, C. S. Park, J. Y. Lee, S. S. Kim, J. Lee, D. Kim, J. Kim, Dongjin Semichem Co. Ltd. (South Korea) [6519-85]

- ✓ **Using a DOE to reduce immersion lithography related defects**, E. Ng, Spansion Inc.; J. S. Hooge, Tokyo Electron America, Inc. [6519-86]
- ✓ **Formulated surface conditioners in 50-nm immersion lithography: simultaneously reducing pattern collapse and line-width roughness**, M. Sugiyama, M. Sanada, Sokudo, Co., Ltd. (Japan); S. Kumar, Sokudo USA, LLC; S. Wang, P. Wong, S. Sinkwitz, ASML Netherlands B.V. (Netherlands); M. Jaramillo, Jr., P. Zhang, Air Products and Chemicals, Inc. [6519-87]
- ✓ **BARC (bottom anti-reflective coating) for immersion process**, Y. Hiroi, T. Kishioka, R. Sakamoto, H. Watanabe, D. Maruyama, T. Ohashi, T. Ishida, S. Kimura, Nissan Chemical Industries, Ltd. (Japan) [6519-89]
- ✓ **Organic ArF bottom antireflective coatings for immersion lithography**, H. Zhuang, Z. Xiang, H. Wu, J. Shan, D. J. Abdallah, S. K. Mullen, M. Neisser, AZ Electronic Materials USA Corp. [6519-90]
- ✓ **Multilayer BARCs for hyper-NA immersion lithography process**, Y. Sakaida, H. Imaruya, M. Nakajima, T. Sakaguchi, K. Hashimoto, S. Kimura, Nissan Chemical Industries, Ltd. (Japan) [6519-91]
- ✓ **Process evaluation and metrology verification for next-generation immersion process**, T. Tomita, K. R. Nafus, S. Hatakeyama, H. Kosugi, M. Enomoto, Tokyo Electron Kyushu Ltd. (Japan); S. Inoue, K. Ruck, H. Weichert, Tokyo Electron Europe Ltd. (Germany); M. B. Mantecon, R. Stegen, C. de Groot, R. Moerman, ASML Netherlands B.V. (Netherlands) [6519-92]

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- ✓ **Novel polymeric anionic photo-acid generators (PAGs) and photoresists**, M. Wang, N. D. Jarnagin, The Univ. of North Carolina at Charlotte; W. Yueh, J. M. Roberts, Intel Corp.; M. Tapia-Tapia, N. Batina, Univ. Autonoma Metropolitana Iztapalapa (Mexico); K. E. Gonsalves, The Univ. of North Carolina at Charlotte [6519-93]
- ✓ **Ionic photoacid generators (PAGs) and base incorporated into main-chain of polymers for sub-50-nm patterning by EUVL**, M. Wang, The Univ. of North Carolina at Charlotte; W. Yueh, J. M. Roberts, Intel Corp.; K. E. Gonsalves, The Univ. of North Carolina at Charlotte [6519-95]
- ✓ **Development of nanocomposite resists with high plasma etch resistance**, C. Chen, H. Zhuang, P. Lu, M. Neisser, G. Pawlowski, AZ Electronic Materials USA Corp. [6519-96]
- ✓ **Chemical composition distribution analysis of photoresist copolymers and influence on ArF lithographic performance**, H. Momose, A. Yasuda, A. Ueda, T. Iseki, Mitsubishi Rayon Co., Ltd. (Japan); K. Ute, T. Nishimura, R. Nakagawa, T. Kitayama, Osaka Univ. (Japan) [6519-97]
- ✓ **Development of single component chemically amplified resist based on dehalogenation of polymer**, H. Yamamoto, T. Kozawa, S. Tagawa, Osaka Univ. (Japan); K. Ohmori, M. Sato, H. Komano, Tokyo Ohka Kogyo Co., Ltd. (Japan) [6519-98]
- ✓ **Novel 193-nm positive photoresist composed of ester acetal polymer without phenyl group**, L. Wang, Y. Huo, Beijing Normal Univ. (China) [6519-99]
- ✓ **Two-component photoresists based on acidolytic cleavage of novel ester acetal polymer**, L. Wang, Z. Chu, Beijing Normal Univ. (China) [6519-100]
- ✓ **Nonchemically amplified resists for deep-UV lithography**, J. Kim, R. Ganesan, S. Kim, S. K. Youn, Y. Cho, J. Yun, Korea Advanced Institute of Science and Technology (South Korea) [6519-101]
- ✓ **EUV printing of contact holes for the sub-40-nm node**, S. Trogisch, M. Bender, W. Domke, M. Roessiger, Qimonda Dresden GmbH & Co. OHG (Germany); Y. Wei, Infineon Technologies North America [6519-102]
- ✓ **Non-ionic photoacid generators for chemically amplified resists: evaluation results on the application-relevant properties**, T. Asakura, H. Yamato, Y. Nishimae, M. Ohwa, Ciba Specialty Chemicals K.K. (Japan) [6519-103]
- ✓ **PAG distribution and acid thermal diffusion study in ultra-thick chemically amplified resist films**, M. A. Toukhy, M. Paunescu, C. Chen, G. Pawlowski, AZ Electronic Materials USA Corp. . . . [6519-104]

ARC/Multilayer Processes

- ✓ **Study of 193-nm resist degradation mechanisms under various etch chemistries**, A. J. Bazin, STMicroelectronics (France); M. J. May, E. Pargon, P. Gautier, Lab. d'Electronique de Technologie de l'Information (France); B. P. Mortini, STMicroelectronics (France) [6519-105]
- ✓ **Development of high-performance multilayer resist process with hardening treatment**, Y. Ono, T. Ishibashi, A. Yamaguchi, T. Hanawa, M. Tadokoro, K. Yoshikawa, K. Yonekura, Renesas Technology Corp. (Japan); T. Matsunobe, K. Matsuda, Toray Engineering Co., Ltd. (Japan); Y. Fujii, T. Tanaka, Tokyo Ohka Kogyo Co., Ltd. (Japan) [6519-106]
- ✓ **Correlation between etching and optical properties of organic films for multi-layer resist**, E. Soda, F. Koba, S. Kondo, S. Ogawa, S. Saito, Semiconductor Leading Edge Technologies, Inc. (Japan) . . . [6519-107]
- ✓ **Rework/stripping of multilayer materials for FEOL and BEOL integration using single wafer tool techniques**, S. R. Turner, Brewer Science, Inc. [6519-108]
- ✓ **Spin-on organic hardmask materials in 70-nm devices**, C. Oh, D. Uh, D. Kim, J. Lee, H. Yun, I. Nam, K. Yoon, K. Hyung, J. Kim, T. Chang, CHEIL Industries, Inc. (South Korea); C. H. Lee, J. Lee, K. Park, Y. Kim, T. Kim, SAMSUNG Electronics Co., Ltd. (South Korea) [6519-109]
- ✓ **Materials for and performance of multilayer lithography schemes**, Y. Wang, M. W. Weimer, V. N. Krishnamurthy, J. B. Claypool, Z. Zu, Brewer Science, Inc. [6519-110]
- ✓ **Advanced developer-soluble gap-fill materials and applications**, R. Huang, D. M. Sullivan, A. Qin, Brewer Science, Inc. [6519-111]
- ✓ **Novel low-reflective index fluoropolymers-based top antireflective coatings (TARC) for 193-nm lithography**, T. Yamashita, T. Ishikawa, T. Hayami, T. Kanemura, Daikin Industries, Ltd. (Japan) [6519-112]
- ✓ **Effect of molecular weight and thermal cross-link rate on via filling performance in BARC and gap fill materials**, S. Takei, Nissan Chemical Industries, Ltd. (Japan) [6519-113]
- ✓ **Optimization of hardmask for dual-antireflection layers**, J. Kim, J. Hwang, J. Kim, K. Kim, Dongbu Electronics Co., Ltd. (South Korea) [6519-114]
- ✓ **Advances in developer-soluble antireflective coatings for 248-nm lithography**, R. L. Mercado, J. A. Lowes, C. A. Washburn, D. J. Guerrero, Brewer Science, Inc. [6519-115]
- ✓ **Optimization of material and process parameter for minimizing defect in implementation of MFHM process**, K. Lee, J. Heo, K. Ban, H. Seo, G. Lee, W. Kim, J. Cho, J. Sun, S. D. Lee, C. K. Bok, S. Moon, J. Kim, Hynix Semiconductor Inc. (South Korea) [6519-116]
- ✓ **A novel 248-nm wet-developable BARC for trench applications**, C. J. Neef, D. L. Thomas, Brewer Science, Inc. [6519-118]
- ✓ **Wet recess gap-fill materials for an advanced dual-Damascene process**, T. Shinjo, S. Takei, Y. Horiguchi, Y. Nakajima, Nissan Chemical Industries, Ltd. (Japan) [6519-119]
- ✓ **Spin-on organic hardmask for high-temperature application**, H. Jung, T. T. Kim, H. Ryu, Core Trust Engineering Co. Ltd. (South Korea) [6519-120]
- ✓ **Low out-gassing KrF bottom antireflective coatings**, Z. Xiang, H. Zhuang, J. Shan, J. Yin, E. Gonzalez, M. Neisser, AZ Electronic Materials USA Corp.; S. Miyazaki, AZ Electronic Materials K.K. (Japan) [6519-121]
- ✓ **Novel approach of UV cross-link process to planarization for 32-45 nm advanced lithography**, S. Takei, U. Horiguchi, T. Shinjo, Y. Mano, Nissan Chemical Industries, Ltd. (Japan); M. Muramatsu, M. Iwashita, K. Tsuchiya, Tokyo Electron Ltd. (Japan) [6519-124]
- ✓ **Overcome the challenge of CD-bias with organic bottom anti-reflective coating removal process**, S. Yanovich, G. Krasnikov, O. Gushchin, JSC Mikron (Russia) [6519-125]
- ✓ **Thin bilayer resists approach for 193 nm and future photolithography II**, Y. Hishiro, M. Hyatt, Micron Technology, Inc. [6519-126]
- ✓ **Radiation sensitive developable bottom anti-reflective coating (BARC) for 193-nm lithography first generation**, M. A. Toukhy, J. E. Oberlander, S. K. Mullen, P. Lu, M. Neisser, AZ Electronic Materials USA Corp. [6519-127]

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- ✓ **Post exposure bake unit equipped with wafer shape compensation technology**, S. Goto, Dainippon Screen Manufacturing Co., Ltd. (Japan); H. Taniguchi, K. Oyama, S. Hori, SOKUDO Co., Ltd. (Japan); K. Matsuchika, Dainippon Screen Manufacturing Co., Ltd. (Japan); H. Taniguchi, SOKUDO Co., Ltd. (Japan) [6519-128]
- ✓ **BCM (by-product capping mask) process to define subresolution size of floating gate in sub-90-nm flash memory**, S. Hwang, J. Jang, J. Kim, K. Kim, Dongbu Electronics Co., Ltd. (South Korea) . [6519-130]
- ✓ **Reducing bubbles and particles associated with photoresist packaging materials and dispense systems**, B. Alexander, W. Liu, H. Yan, K. Mikkelsen, K. T. O'Dougherty, ATMI, Inc. [6519-132]
- ✓ **Resist evaluation for contact hole patterning with thermal flow process**, R. Tiron, C. Sourd, Lab. d'Electronique de Technologie de l'Information (France); D. de Simone, STMicroelectronics (Italy); B. P. Mortini, STMicroelectronics (France); G. Cotti, E. Annoni, STMicroelectronics (Italy) [6519-133]
- ✓ **Pattern shrink process for sub-50-nm DRAM**, S. Lee, T. Kim, Hynix Semiconductor Inc. (South Korea) [6519-134]
- ✓ **Effect of novel rinsing material and surfactant treatment on the resist pattern performance**, V. Huang, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan) [6519-135]
- ✓ **Impact of airborne NH₃ and humidity against wafer-to-wafer CD variation in ArF lithography through 45-nm technology node**, R. Naito, Y. Matsuda, M. Shioguchi, T. Shibata, Tokyo Electron Kyushu Ltd. (Japan) [6519-136]
- ✓ **Proximity effect correction for the chemical shrink process of different type contact holes**, W. Hsieh, H. Liu, C. Shin, J. Lin, Nanya Technology Corp. (Taiwan) [6519-138]
- ✓ **Mechanism of post develop stain defect**, M. Harumoto, Dainippon Screen Manufacturing Co., Ltd. (Japan); A. Yamaguchi, SOKUDO Co., Ltd. (Japan); A. Hisai, Dainippon Screen Manufacturing Co., Ltd. (Japan) [6519-140]
- ✓ **New ArF resist introduction for process through-put enhancement**, M. S. Kim, Hynix Semiconductor Inc. (South Korea) [6519-141]
- ✓ **A heater plate assisted integrated bake/chill system for photoresist processing**, H. T. Chua, The Univ. of Western Australia (Australia); A. E. B. Tay, Y. Wang, X. Wu, National Univ. of Singapore [6519-142]
- ✓ **Molecular contamination control technologies for high-volume production phase in high-NA 193-nm lithography**, T. Nakano, T. Tanahashi, A. Imai, K. Yamana, T. Shimotsu, NICHIAS Corp. (Japan); N. Takahashi, M. Shioguchi, Y. Matsuda, J. Kitano, Tokyo Electron Kyushu Ltd. (Japan) [6519-143]
- ✓ **Printing of structures less than 0,3 µm by i-line exposure using resists TDMR-AR80 and TDMR-AR95**, A. Behrendt, K. Stoefflin, T. Dow, Infineon Technologies Austria AG [6519-144]
- ✓ **Various factors of the image blur in chemically amplified resist**, T. Kawakami, T. Nagai, Y. Nishimura, M. Shima, S. Kusumoto, T. Shimokawa, JSR Corp. (Japan) [6519-145]
- ✓ **Image tone optimization in advanced mask making for DUV lithography**, J. D. Kim, Y. M. Kim, S. Park, J. Lee, Y. Lee, K. Kim, Dongbu Electronics Co., Ltd. (South Korea) [6519-146]
- ✓ **Advanced photoresist dispense valve control technology for process control improvement, process stability**, M. Davison, On Semiconductor; B. W. Kidd, Integrated Designs, L.P. [6519-147]
- ✓ **Automatic viscosity controlled production of photoresist**, W. S. Chang, C. Monovoukas, Levitronix; M. Tanaka, N. Fronczak, JSR Micro, Inc. [6519-148]
- ✓ **Adhesion effect of resist reflow process**, J. M. Park, J. Lee, Hanyang Univ. (South Korea); J. Kim, Seoul National Univ. (South Korea); J. Park, C. K. Bok, S. Moon, Hynix Semiconductor Inc. (South Korea); J. Kim, S. Lee, Seoul National Univ. (South Korea); S. Park, J. Hong, H. Oh, Hanyang Univ. (South Korea) [6519-149]

- ✓ **Investigation of mechanism of pattern deformation on TiN substrate and O₂ plasma effect without BARC**, J. Moon, Y. Yun, M. Kim, J. Kim, K. Kim, Dongbu Electronics Co., Ltd. (South Korea) [6519-150]
- ✓ **62 μm-scribe-line 90-nm product alignment signal improvement: remove TIN HM on alignment mark**, C. Chen, A. Chia, A. Chang, J. Lee, C. Chen, C. Huang, United Microelectronics Corp. (Taiwan) [6519-151]
- ✓ **Accurate photoresist usage forecasting**, L. C. MacDowell, IBM Corp. [6519-152]
- ✓ **Consignment stocking of photochemicals benefits and risks**, L. C. MacDowell, IBM Corp. [6519-153]

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- ✓ **Simulation of the combined effects of polymer size acid diffusion length and EUV secondary electron blur on resist line-edge roughness**, D. Drygiannakis, Institute of Microelectronics (Greece); D. Nijkerk, TNO TPD (Netherlands); G. P. Patsis, G. Kokkoris, I. Raptis, Institute of Microelectronics (Greece); L. H. A. Leunissen, IMEC (Belgium); E. Gogolides, Institute of Microelectronics (Greece) [6519-36]
- ✓ **Distribution control of protecting groups and its effect on LER for EUV molecular resist**, D. Shiono, H. Hada, T. Hirayama, H. Yukawa, Tokyo Ohka Kogyo Co., Ltd. (Japan); K. Kojima, A. Yamaguchi, H. Fukuda, Hitachi, Ltd. (Japan); H. Oizumi, I. Nishiyama, Association of Super-Advanced Electronics Technologies (Japan) [6519-47]
- ✓ **Evaluation of the 3D compositional heterogeneity effect on line-edge-roughness**, S. Kang, W. Wu, B. D. Vogt, V. M. Prabhu, E. K. Lin, National Institute of Standards and Technology; K. L. Turnquest, SEMATECH, Inc. [6519-154]
- ✓ **Reduction of LER by controlled copolymerization in ArF lithography**, S. Matsunaga, I. Aratani, F. Okabe, M. Nakazawa, M. Kitayama, Kuraray Co., Ltd. (Japan) [6519-155]
- ✓ **A study of process extension technologies**, S. Kim, The Catholic Univ. of Korea (South Korea) [6519-156]
- ✓ **More developed mechanical modeling of pattern collapse simulation in 193-nm immersion lithography**, J. Kim, W. Chang, S. Park, H. Oh, Sr., Hanyang Univ. (South Korea); S. Lee, S. Kim, SAMSUNG Electronics Co., Ltd. (South Korea) [6519-158]
- ✓ **The rational design of polymeric, non-CAR, EUV-resist materials by QSPR modeling**, K. Jack, A. K. Whittaker, I. Blakey, H. Liu, The Univ. of Queensland (Australia); W. Yueh, H. B. Cao, M. J. Leeson, Intel Corp. [6519-160]
- ✓ **Model-based OPC for BARCless DUV process**, Y. Kim, Dongbu Electronics Co., Ltd. (South Korea) [6519-161]
- ✓ **Some nonresist component contributions to LER and LWR**, T. Kudo, S. Chakrapani, G. Lin, C. Antonio, D. Parthasarathy, R. Dammel, M. Padmanaban, AZ Electronic Materials USA Corp. [6519-163]
- ✓ **Depth-of-focus (DOF) and line-width roughness (LWR) performance of novel surface conditioner solutions for immersion lithography**, B. J. Lu, United Microelectronics Corp. (Taiwan) [6519-164]

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- ✓ **Effect of photo-acid generator concentration and developer strength on the patterning capabilities of a model EUV photoresist**, K. Choi, Intel Corp.; V. M. Prabhu, K. A. Lavery, E. K. Lin, W. Wu, J. T. Woodward, National Institute of Standards and Technology; M. J. Leeson, H. B. Cao, G. Thompson, Intel Corp. [6519-165]
- ✓ **A study of EUV resist outgassing characteristics using a novel outgas analysis system**, T. Itani, J. J. S. Santillan, Semiconductor Leading Edge Technologies, Inc. (Japan) [6519-166]
- ✓ **Sub-10-nm contact holes with aspect ratio over sixty formed by e-beam resist shrinkage techniques**, W. G. Chen, M. Kao, M. Tsai, Industrial Technology Research Institute (Taiwan) [6519-167]
- ✓ **Study on photochemical analysis system for EUV lithography**, A. Sekiguchi, Y. Kono, Y. Minami, M. Kadoi, Litho Tech Japan Co., Ltd. (Japan); T. Kozawa, S. Tagawa, Osaka Univ. (Japan); D. Gustafson, P. A. Blackborow, Energetiq Technology, Inc. [6519-168]
- ✓ **Improved lithographic performance for EUVL-resists based on activation energy for hydroxy phenol and hydrocarbone acrylate type polymer**, S. Kim, Dongjin Semichem. Co. Ltd. (South Korea) [6519-169]
- ✓ **Photoresist dissolution into a CO₂ compatible salt and CO₂ solution: rate dependence on processing conditions**, A. E. Zwebner, North Carolina State Univ.; M. I. Wagner, Micell Technologies, Inc.; R. G. Carbonell, North Carolina State Univ. [6519-170]
- ✓ **Exposure of molecular glass resist by e-beam and EUVIL**, C. Vannuffel, Lab. d'Electronique de Technologie de l'Information (France); J. Simon, Commissariat à l'Energie Atomique (France); D. Djian, Lab. d'Electronique de Technologie de l'Information (France); D. Niakoula, P. Argitis, V. Vidali, E. Couladouros, Institute of Microelectronics (Greece); A. Robinson, The Univ. of Birmingham; R. Palmer, F. Gibbons, M. Manickam, J. Preece, S. Diegoli, The Univ. of Birmingham (United Kingdom); H. Solak, Paul Scherrer Institut (Switzerland) [6519-171]
- ✓ **Sub-10-nm structures written in ultra-thin HSQ resist layer, using electron-beam lithography**, A. Grigorescu, M. van der Krogt, C. Hagen, P. Kruit, Technische Univ. Delft (Netherlands) [6519-177]
- ✓ **Phenolic molecular glasses as resists for next-generation lithography**, A. Xavier, J. Lee, Cornell Univ.; N. M. Felix, IBM Corp.; C. K. Ober, Cornell Univ.; H. B. Cao, H. Deng, Intel Corp.; H. Kudo, D. Watanabe, T. Nishikubo, Kanagawa Univ. (Japan) [6519-192]

Novel Processes and Applications

- ✓ **Study on diazonaphthoquinone positive photoresist composition for LCD**, Y. Zou, F. Zhou, Beijing Normal Univ. (China) [6519-172]
- ✓ **Characterization of a high-photospeed positive thick photoresist for lead-free solder electroplating**, W. W. Flack, H. T. Nguyen, Ultratech, Inc.; K. Saito, K. Misumi, Tokyo Ohka Kogyo Co., Ltd. (Japan) [6519-173]
- ✓ **Performance of a 55-micron copper pillar bump process using a positive thick chemically amplified photoresist**, W. W. Flack, Ultratech, Inc.; D. Craise, Motorola, Inc.; E. S. Capsuto, Shin-EtsuMicroSi, Inc.; H. T. Nguyen, J. Buchanan, Ultratech, Inc. [6519-174]
- ✓ **The use of black pigment polyimide, DARC300, as a light absorber on an optical sensor**, K. A. Gehoski, Motorola, Inc.; P. Holm, Motorola; K. Boggess, Motorola, Inc.; C. Scott, Brewer Science [6519-176]

Tuesday 27 February

SESSION 4

Marriott San Jose Ballroom Salon III .. Tues. 8:00 to 9:40 am

Resist Materials

Chairs: **Ernisse S. Putna**, Intel Corp.; **Ralph R. Dammel**, AZ Electronic Materials USA Corp.

- 8:00 am: **High-performance 193-nm photoresists based on fluoro-sulfonamide**, W. Li, K. Chen, R. W. Kwong, M. C. Lawson, M. Khojasteh, I. Popova, P. R. Varanasi, IBM Microelectronics Div. . [6519-14]
- 8:20 am: **Novel diamantane polymer platform for enhanced etch resistance**, M. Padmanaban, S. Chakrapani, G. Lin, T. Kudo, D. Parthasarathy, D. M. Rahman, D. S. McKenzie, R. Dammel, AZ Electronic Materials USA Corp. . [6519-15]
- 8:40 am: **Hybrid optical: electron-beam resists**, D. M. Lennon, S. J. Spector, T. H. Fedynyshyn, T. M. Lyszczarz, M. Rothschild, MIT Lincoln Lab.; J. W. Thackeray, K. Spear-Alfonso, Rohm and Haas Electronic Materials . [6519-16]
- 9:00 am: **Evaluation of immersion lithography process for 55-nm node logic device**, T. Nakata, T. Kodama, M. Komori, N. Onoda, T. Uchiyama, NEC Electronics Corp. (Japan) . [6519-73]
- 9:20 am: **Photo-deprotection resist based on photodegradation of o-nitrobenzyl phenol ether for near-field lithography**, T. Ito, A. Terao, Y. Inao, T. Yamaguchi, N. Mizutani, Canon Inc. (Japan) . [6519-19]
- Coffee Break 9:40 to 10:20 am

SESSION 5

Marriott San Jose Ballroom Salon III .. Tues. 10:20 am to 12:20 pm

ARC/Multilayer Process

Chairs: **Sean D. Burns**, IBM Thomas J. Watson Research Ctr.; **Douglas J. Guerrero**, Brewer Science, Inc.

- 10:20 am: **Enhancing photoresist performance with an adhesion promoting photo-acid generator**, R. P. Meagley, S. Sharma, Lawrence Berkeley National Lab. . [6519-20]
- 10:40 am: **Second-generation radiation sensitive developable bottom antireflective coatings (DBARC) and implant resists approaches for 193-nm lithography**, F. M. Houlihan, M. A. Toukhy, A. R. Romano, A. Diones, J. E. Oberlander, S. K. Mullen, A. Krawicz, P. Lu, M. Neisser, AZ Electronic Materials USA Corp. . [6519-21]
- 11:00 am: **Spin-on trilayer approaches to high-NA 193-nm lithography**, D. J. Abdallah, M. Zhang, W. Kim, H. Wu, A. Diones, A. G. Timko, F. M. Houlihan, D. M. Rahman, D. S. McKenzie, P. Lu, M. Neisser, R. R. Dammel, AZ Electronic Materials USA Corp. . [6519-22]
- 11:20 am: **Material design of Si-contained hard mask and carbon bottom layer for multilayer stack application**, H. Harada, Tokyo Ohka Kogyo Co., Ltd. (Japan) . [6519-122]
- 11:40 am: **Silicon-based antireflective spin-on hardmask materials with improved storage stability for 193-nm lithography**, S. K. Kim, S. H. Lim, D. Kim, S. R. Koh, M. Kim, H. C. Yoon, D. Uh, J. Kim, T. Chang, CHEIL Industries, Inc. (South Korea); C. H. Lee, J. Lee, K. Park, Y. Kim, T. Kim, SAMSUNG Electronics Co., Ltd. (South Korea) . [6519-24]
- 12:00 pm: **Novel developers for the positive tone EUV photoresists**, G. Sharma, S. Sharma, M. Rattner, Lawrence Berkeley National Lab.; R. P. Meagley, Intel Corp. . [6519-25]
- Lunch/Exhibition Break 12:20 to 1:30 pm

SESSION 6

Marriott San Jose Ballroom Salon III .. Tues. 1:30 to 3:10 pm

Resist Processing

Chairs: **Kyle Patterson**, Freescale Semiconductor, Inc.; **Nobuyuki N. Matsuzawa**, Sony Atsugi Technology Ctr. (Japan)

- 1:30 pm: **The application of high-refractive index photoresist for 32-nm device level imaging**, W. E. Conley, Freescale Semiconductor (France), Inc. . [6519-26]
- 1:50 pm: **Performance of chemically amplified resists at half-pitch of 45 nm and below**, Y. Wei, Infineon Technologies North America; M. Bender, W. Domke, A. Laessig, M. Sebal, S. Trogisch, Qimonda Dresden GmbH & Co. OHG (Germany); D. Back, Infineon Technologies North America . [6519-27]
- 2:10 pm: **Evaluation of ArF lithography for 45-nm logic-node implant layers**, T. C. Bailey, IBM Microelectronics Div.; J. Maynollo, Infineon Technologies North America; J. Perez, I. Popova, B. Zhang, IBM Microelectronics Div. . [6519-28]
- 2:30 pm: **Characterization of photo-acid redeposition in 193-nm photoresists**, T. I. Wallow, M. V. Plat, Advanced Micro Devices, Inc.; Z. Zhang, B. MacDonald, Spansion Inc.; Y. Ma, B. M. La Fontaine, Advanced Micro Devices, Inc.; J. Romero, J. Bernard, Spansion Inc.; A. Wilkison, H. J. Levinson, Advanced Micro Devices, Inc. . [6519-29]
- 2:50 pm: **A novel plasma-assisted shrink process to enlarge process windows of narrow trenches and contacts for 45-nm node applications and beyond**, M. Op de Beeck, W. Boullart, Z. Tokei, S. Demuynck, S. Vanhaelemeersch, IMEC (Belgium); R. Sadjadi, Lam Research Corp. and IMEC (Belgium); H. Zu, J. Kim, P. Cirigliano, Lam Research Corp. . [6519-30]
- Coffee Break 3:10 to 3:30 pm

SESSION 7

Marriott San Jose Ballroom Salon III .. Tues. 3:30 to 5:10 pm

Resist Processes and Simulation

Chairs: **Adam R. Pawloski**, Affymetrix, Inc.; **Christoph K. Hohle**, Qimonda AG (Germany)

- 3:30 pm: **A novel method for characterizing resist performance: simultaneous optimization for sensitivity, line-width roughness, and resolution**, J. H. Lammers, Philips Research Nederland BV (Netherlands); R. Gronheid, IMEC (Belgium); D. Van Steenwinckel, Philips Research Leuven (Belgium); F. Van Roey, A. M. Meyers, T. Vandeweyer, IMEC (Belgium) . [6519-31]
- 3:50 pm: **The tri-lateral challenge of LER, resolution, and photospeed: sub-32-nm modeling and experiments using ArF and EUV**, R. L. Bristol, H. B. Cao, M. Chandhok, M. J. Leeson, W. Yueh, Intel Corp. . [6519-32]
- 4:10 pm: **PAG segregation during exposure affecting innate material roughness**, T. H. Fedynyshyn, D. K. Astolff, A. Cabral, MIT Lincoln Lab.; J. M. Roberts, Intel Corp. . [6519-33]
- 4:30 pm: **A mechanistic model for line-edge roughness**, M. D. Smith, J. J. Biafore, S. Robertson, KLA-Tencor Corp. . [6519-34]
- 4:50 pm: **The characterization of photoresist for accurate simulation beyond Gaussian diffusion**, L. Wang, P. Wu, Q. Wu, H. Ding, X. Li, C. Sun, Shanghai Hua Hong NEC Electronics Co., Ltd. (China) . [6519-35]

Wednesday 28 February

SESSION 8

Marriott San Jose Ballroom Salon III . . . Wed. 8:00 to 9:40 am

Resist Fundamentals

Chairs: **Vivek M. Prabhu**, National Institute of Standards and Technology; **Clifford L. Henderson**, Georgia Institute of Technology

- 8:00 am: **Direct measurement of the in-situ developed latent image: the residual swelling fraction**, V. M. Prabhu, A. B. Rao, S. Kang, K. A. Lavery, E. K. Lin, S. K. Satija, National Institute of Standards and Technology; K. L. Turnquest, SEMATECH, Inc. [6519-37]
- 8:20 am: **Fundamental limits to EUV photoresists: what resolution, LER, and sensitivity can be achieved?**, G. M. Gallatin, Applied Math Solutions, LLC; P. P. Naulleau, Lawrence Berkeley National Lab. and Univ. at Albany; R. L. Brainard, Univ. at Albany [6519-38]
- 8:40 am: **Etch resistance: comparison and development of etch-rate models**, D. Perret, Rohm and Haas Electronic Materials (France); C. E. Andes, K. Cheon, M. Sobhian, G. G. Barclay, P. Trefonas, Rohm and Haas Electronic Materials [6519-39]
- 9:00 am: **Dissolution behavior of resist polymers studied by Quartz-Crystal-Microbalance method II**, M. Toriumi, Osaka Univ. (Japan) [6519-40]
- 9:20 am: **Investigation of capillary bridges growth in NIL process**, S. Landis, Lab. d'Electronique de Technologie de l'Information (France) [6519-41]
- Coffee Break 9:40 to 10:20 am

SESSION 9

Marriott San Jose Ballroom Salon III Wed. 10:20 am to 12:20 pm

LER

Chairs: **Gregory M. Wallraff**, IBM Almaden Research Ctr.; **Vivek M. Prabhu**, National Institute of Standards and Technology

- 10:20 am: **Component segregation in model chemically amplified resists**, J. T. Woodward, National Institute of Standards & Technology; T. H. Fedynyshyn, D. K. Astolfi, S. G. Cann, MIT Lincoln Lab.; M. J. Leeson, Intel Corp. [6519-43]
- 10:40 am: **FTIR measurements of compositional heterogeneities**, S. Kang, B. D. Vogt, W. Wu, V. M. Prabhu, D. L. VanderHart, A. B. Rao, E. K. Lin, National Institute of Standards and Technology; K. L. Turnquest, SEMATECH, Inc. [6519-44]
- 11:00 am: **Changes in resist glass transition temperatures due to exposure**, T. H. Fedynyshyn, I. Pottebaum, A. Cabral, MIT Lincoln Lab.; J. M. Roberts, Intel Corp. [6519-45]
- 11:20 am: **The study and material design for the reduction of LWR**, H. Tsubaki, T. Yamanaka, S. Tarutani, F. Nishiyama, K. Kodama, N. Nishikawa, N. Ooshima, K. Shitabatake, Fuji Photo Film Co., Ltd. (Japan) [6519-46]
- 11:40 am: **Line-edge roughness in 193-nm resists: lithographic aspects and etch transfer**, T. I. Wallow, A. Acheta, Y. Ma, Advanced Micro Devices, Inc.; A. R. Pawloski, Affymetrix, Inc.; S. Bell, Advanced Micro Devices, Inc.; B. L. Ward, Spansion Corp.; C. E. Tabery, S. N. McGowan, B. M. La Fontaine, R. Kim, M. V. Plat, I. Matthew, A. Wilkison, H. J. Levinson, Advanced Micro Devices, Inc. [6519-162]
- 12:00 pm: **Impact of line-width roughness on Intel's 65-nm process devices**, M. Chandhok, S. Datta, D. Lionberger, S. Vesecky, Intel Corp. [6519-48]
- Lunch/Exhibition Break 12:20 to 1:30 pm

SESSION 10

Marriott San Jose Ballroom Salon III . . . Wed. 1:30 to 3:10 pm

NGL

Chairs: **George G. Barclay**, Rohm and Haas Electronic Materials; **Dahchung Owe-Yang**, Shin-Etsu MicroSi, Inc.

- 1:30 pm: **New resists and processes for UV-imprint lithography**, K. R. Carter, S. B. Jhaveri, Univ. of Massachusetts/Amherst; E. C. Hagberg, M. W. Hart, IBM Almaden Research Ctr. [6519-49]
- 1:50 pm: **Impact of curing kinetics and materials properties on imprint characteristics of resists for UV-nanoimprint lithography**, F. A. Houle, G. Dubois, D. C. Miller, R. Sooriyakumaran, H. D. Truong, M. I. Sanchez, B. Davis, T. Magbitang, R. D. Allen, IBM Almaden Research Ctr. [6519-50]
- 2:10 pm: **Material design of negative-tone polyphenol resist for EUV and EB lithography**, K. Kojima, H. Fukuda, Hitachi, Ltd. (Japan); H. Hada, D. Shiono, J. Onodera, Tokyo Ohka Kogyo Co., Ltd. (Japan) [6519-51]
- 2:30 pm: **Photo-acid generator quantum efficiency and line-edge roughness behavior in novel polymer-bound PAG 193 nm and EUV photoresists**, C. Lee, Georgia Institute of Technology; N. D. Jarnagin, M. Wang, K. Gonsalves, The Univ. of North Carolina at Charlotte; W. Yueh, J. M. Roberts, Intel Corp.; C. L. Henderson, Georgia Institute of Technology [6519-52]
- 2:50 pm: **Novel anionic photoacid generator (PAGs) monomers and photoresist polymers for sub-50-nm patterning by EUV and electron-beam lithography**, M. Wang, The Univ. of North Carolina at Charlotte; C. Lee, C. L. Henderson, Georgia Institute of Technology; W. Yueh, J. M. Roberts, Intel Corp.; K. E. Gonsalves, The Univ. of North Carolina at Charlotte [6519-53]
- Coffee Break 3:10 to 3:30 pm

SESSION 11

Marriott San Jose Ballroom Salon III . . . Wed. 3:30 to 5:30 pm

Novel Processes/Applications

Chairs: **Gregory M. Wallraff**, IBM Almaden Research Ctr.; **Adam R. Pawloski**, Affymetrix, Inc.

- 3:30 pm: **Fabrication of silica 3D structures from polyhedral oligomeric silsesquioxane (POSS) by multibeam interference lithography**, S. Yang, J. S. Seo, J. H. Moon, Univ. of Pennsylvania [6519-54]
- 3:50 pm: **Self-aligned, self-assembled organosilicate line patterns of ~20nm half-pitch from block-copolymer mediated self assembly**, H. Kim, J. Cheng, C. Rettner, O. Park, W. D. Hinsberg, R. D. Miller, M. W. Hart, L. Sundstrom, IBM Almaden Research Ctr.; Y. Zhang, IBM Thomas J. Watson Research Ctr. [6519-55]
- 4:10 pm: **Gray-scale lithography of photosensitive polyimide and its graphitization**, S. Akbar, Qimonda Richmond LLC; E. Imhoff, F. Kub, Naval Research Lab. [6519-56]
- 4:30 pm: **A novel top surface imaging approach utilizing direct-area selective atomic layer deposition of hardmasks**, A. K. Sinha, D. W. Hess, C. L. Henderson, Georgia Institute of Technology [6519-57]
- 4:50 pm: **Novel photodefinable low-k dielectric polymers based on polybenzoxazines**, M. Romeo, Georgia Institute of Technology; K. Yamanaka, K. Maeda, Central Glass Co., Ltd. (Japan); C. L. Henderson, Georgia Institute of Technology [6519-58]
- 5:10 pm: **Patterning of biomolecules on a biocompatible nonchemically amplified resist**, J. Kim, R. Ganesan, S. Y. Yoo, J. Choi, S. Y. Lee, Korea Advanced Institute of Science and Technology (South Korea) [6519-59]

SESSION 12

Marriott San Jose Ballroom Salon III . . Wed. 6:30 to 8:50 pm

Joint Session with Conference 6517 on EUV Resists*Chairs: Anthony E. Novembre*, Lucent Technologies; *Michael J. Lercel*, SEMATECH, Inc.6:30 pm: **Chemically amplified resists resolving 25-nm 1:1 line: space features following EUV exposure**, J. W. Thackeray, Rohm and Haas Electronic Materials[6517-44]6:50 pm: **Resist evaluation for EUV application at ASET**, D. Goo, Y. Tanaka, Y. Kikuchi, H. Oizumi, I. Nishiyama, Association of Super-Advanced Electronics Technologies (Japan)[6519-60]7:10 pm: **Patterning performance of new molecular resist in EUV lithography**, H. Oizumi, Y. Tanaka, T. Kumise, I. Nishiyama, Association of Super-Advanced Electronics Technologies (Japan)[6517-45]7:30 pm: **Molecular glass photoresists containing photo-acid generator functionality: a route to a true single-molecule photoresist**, R. A. Lawson, R. Whetsell, Georgia Institute of Technology; W. Yueh, J. M. Roberts, Intel Corp.; L. M. Tolbert, C. L. Henderson, Georgia Institute of Technology[6519-61]7:50 pm: **Metrology for EUV-resist outgassing using pressure-rise method**, I. Nishiyama, H. Oizumi, Association of Super-Advanced Electronics Technologies (Japan)[6517-46]8:10 pm: **The resist materials study for outgassing reduction and LWR improvement in EUV lithography**, S. Masuda, S. Kamimura, S. Hirano, W. Hoshino, K. Mizutani, Fuji Photo Film Co., Ltd. (Japan)[6519-62]8:30 pm: **An analysis of EUV-resist outgassing measurements**, K. R. Dean, SEMATECH, Inc.; I. Nishiyama, H. Oizumi, ASET (Japan); A. M. Keen, BOC Edwards, Inc.; H. B. Cao, W. Yueh, Intel Corp.; T. Watanabe, Univ. of Hyogo (Japan); P. Lacovig, L. Rumiz, Sincrotrone Trieste S.C.p.A (Italy); G. P. Denbeaux, SUNY/Univ. at Albany; J. Simon, CEA/LETI (France)[6519-63]**Courses of Related Interest***Register for courses at the SPIE registration desk.*

SC101 Introduction to Microlithography: Theory, Materials, and Processing (Willson, Bowden, Thompson) Sunday 8:30 am to 5:30 pm

SC103 Resists for Deep UV Lithography (Willson) Thursday 8:30 am to 5:30 pm

SC355 Fundamentals of Photochemical Contamination Control for Lithographic Tools (Kunz) Sunday 6:00 to 10:00 pm

SC616 Practical Photoresist Processing (Dammell) Thursday 1:30 to 5:30 pm

SC780 Tracks 101: Microlithography Coat and Develop Basics (Daggett, Williams) Sunday 8:30 am to 5:30 pm

SC579 Photomask Fabrication and Technology Basics (*Duff*) Monday 8:30 am to 5:30 pm

SC832 IP Issues in Advanced Lithography and Semiconductor Manufacturing (Gortych) Monday 1:30 to 5:30 pm

SC833 Lithography Integration for Semiconductor Back-End-Of-The-Line (BEOL) (Lin) Sunday 8:30 am to 12:30 pm


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Optical Microlithography XX

Conference Chair: **Donis G. Flagello**, ASML US, Inc.

Cochair: **Harry J. Levinson**, Advanced Micro Devices, Inc.

Program Committee: **Pary Baluswamy**, Micron Technology, Inc.; **Han-Ku Cho**, SAMSUNG Electronics Co., Ltd. (South Korea); **Willard E. Conley**, Freescale Semiconductor, Inc. (France); **Mircea V. Dusa**, ASML US, Inc.; **Nigel R. Farrar**, Cymer, Inc.; **Jan-Willem Gemmink**, Philips Semiconductors (France); **Andrew Grenville**, SEMATECH, Inc., and Intel Corp.; **Tatsuhiko Higashiki**, Toshiba Corp. (Japan); **Yao-Ching Ku**, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan); **Kafai Lai**, IBM Microelectronics Div.; **Koichi Matsumoto**, Nikon Corp. (Japan); **Wilhelm Maurer**, Infineon Technologies AG (Germany); **Bruce W. Smith**, Rochester Institute of Technology; **Akiyoshi Suzuki**, Canon Inc. (Japan); **Geert Vandenberghe**, IMEC (Belgium); **Gary Zhang**, Texas Instruments Inc.

Tuesday 27 February

Introduction

Room: Conv. Ctr. A2 Tues. 8:10 to 8:20 am

Chair: **Donis G. Flagello**, ASML US, Inc.

SESSION 1

Room: Conv. Ctr. A2 Tues. 8:20 to 10:20 am

Past, Present, and Future Directions

Chairs: **Donis G. Flagello**, ASML US, Inc.; **Harry J. Levinson**, Advanced Micro Devices, Inc.

8:20 am: **Marching of the microlithography horses: electron, ion, and photon: past, present, and future** (*Invited Paper*), B. J. Lin, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan) [6520-01]

9:00 am: **Future directions for CMOS device technology development from a system application perspective** (*Invited Paper*), T. H. Ning, IBM Thomas J. Watson Research Ctr. [6520-02]

9:40 am: **Optical lithography: 40 years and holding?** (*Invited Paper*), J. H. Bruning, Corning Tropol Corp. [6520-03]

Coffee Break 10:20 to 10:50 am

SESSION 2

Room: Conv. Ctr. A2 Tues. 10:50 am to 12:30 pm

Immersion Status and Performance

Chairs: **Willard E. Conley**, Freescale Semiconductor, Inc. (France); **Andrew Grenville**, Intel Corp.

10:50 am: **Defects, overlay, and focus performance improvements with five generations of immersion exposure tools**, J. Mulken, B. Streefkerk, H. C. Jasper, S. Kruijswijk, F. de Jong, L. Levasier, M. Leenders, ASML Netherlands B.V. (Netherlands) [6520-05]

11:10 am: **Current status of high-index immersion lithography development**, Y. Ohmura, A. Sukegawa, H. Nagasaka, T. Matsuyama, T. Nakashima, S. Wakamoto, H. Kohno, S. Owa, Nikon Corp. (Japan) [6520-06]

11:30 am: **Integrating immersion lithography in high-volume manufacturing for the 45-nm node**, M. Benndorf, Philips Semiconductors (France); W. E. Conley, S. P. Warrick, D. Cruau, Freescale Semiconductor, Inc. (France); D. DeSimone, J. Chapon, ST Microelectronics (France); S. Gaugiran, Commissariat à l'Energie Atomique

(France); K. Mestadi, C. Monget, V. Farys, ST Microelectronics (France); J. Gemmink, Philips Semiconductors (France) [6520-07]

11:50 am: **Performance of immersion lithography for 45-nm node CMOS and ultra-high density SRAM with 0.25 μ m²**, S. Mimotogi, Toshiba Corp. (Japan); F. Uesawa, Sony Atsugi Technology Ctr. (Japan); M. Tominaga, NEC Electronics Corp. (Japan); H. Fujise, K. Sho, Toshiba Corp. (Japan); M. Katsumata, H. Hane, A. Ikegami, Sony Atsugi Technology Ctr. (Japan); S. Nagahara, NEC Electronics (Japan); T. Ema, M. Asano, H. Kanai, T. Kikura, M. Iwai, Toshiba Corp. (Japan) [6520-08]

12:10 pm: **Benefit of ArF immersion lithography in 55-nm logic device manufacturing**, T. Uchiyama, T. Tamura, K. Yoshimochi, NEC Electronics Corp. (Japan); K. Kornitzer, Carl Zeiss SMT AG (Germany); H. Bakker, E. v. Setten, ASML Netherlands B.V. (Netherlands); K. Morisaki, ASML Japan Co., Ltd. (Japan) [6520-09]

Lunch/Exhibition Break 12:30 to 1:30 pm

SESSION 3

Room: Conv. Ctr. A2 Tues. 1:30 to 3:40 pm

Hyper-NA and Polarization

Chairs: **Gary Zhang**, Texas Instruments Inc.; **Jan-Willem Gemmink**, Philips Semiconductors (France)

1:30 pm: **Snell or Fresnel: the influence of material index on hyper-NA lithography** (*Invited Paper*), B. W. Smith, J. Zhou, Rochester Institute of Technology [6520-10]

2:00 pm: **Hyper-NA polarized imaging of 45-nm DRAM**, C. Lim, S. Park, Y. Hyun, J. Kim, T. Eom, J. Park, S. Moon, J. Kim, Hynix Semiconductor Inc. (South Korea) [6520-11]

2:20 pm: **Pushing the boundary: low-k₁ extension by polarized illumination**, E. van Setten, N. Le Masson, G. Swinkels, W. P. de Boeij, M. van de Kerkhof, M. Wehrens, K. Simon, ASML Netherlands B.V. (Netherlands) [6520-12]

2:40 pm: **Modeling polarization for hyper-NA lithography tools and masks**, K. Lai, IBM Microelectronics Div.; A. E. Rosenbluth, IBM Thomas J. Watson Research Ctr.; G. Han, J. Tirapu-Azpiroz, IBM Microelectronics Div.; A. Goehnermeier, B. Kneer, M. Totzeck, Carl Zeiss SMT AG (Germany); L. de Winters, W. P. de Boeij, M. van de Kerkhof, ASML Netherlands B.V. (Netherlands) [6520-13]

3:00 pm: **Polarization-dependent proximity effects**, J. K. Tyminski, Nikon Precision Inc.; T. Matsuyama, T. Nakashima, Nikon Corp. (Japan); T. Schmöller, SIGMA-C Software AG (Germany); J. Lewellen, Sigma-C [6520-14]

3:20 pm: **The impact of projection lens polarization properties on lithographic process at hyper-NA**, B. Geh, Carl Zeiss / ASML-TDC; P. Graeupner, O. Dittmann, J. Zimmermann, M. Totzeck, Carl Zeiss SMT AG (Germany); W. P. de Boeij, L. de Winter, ASML Netherlands B.V. (Netherlands) [6520-15]

Coffee Break 3:40 to 4:10 pm

SESSION 4

Wednesday 28 February

Room: Conv. Ctr. A2 Tues. 4:10 to 5:50 pm

Double Patterning Technology

Chairs: **Han-Ku Cho**, SAMSUNG Electronics Co., Ltd. (South Korea); **Bruce W. Smith**, Rochester Institute of Technology

- 4:10 pm: **Pitch doubling through dual-patterning lithography challenges in integration and litho budgets**, M. V. Dusa, ASML MaskTools Inc.; J. M. Finders, G. Dickers, A. van Oosten, J. Messen, P. Nikolsky, ASML Netherlands B.V. (Netherlands); V. Wiaux, IMEC (Belgium); K. van Ingen-Schenau, ASML Netherlands B.V. (Netherlands); M. Maenhoudt, S. Verhaegen, IMEC (Belgium); J. H. Peters, E. P. Cotte, M. Peschke, Advanced Mask Technology Ctr. (Germany) [6520-16]
- 4:30 pm: **Issues and challenges of double patterning lithography in DRAM**, S. Kim, S. Koo, J. Choi, Y. Hwang, J. Park, E. Kang, C. Lim, S. Moon, J. Kim, Hynix Semiconductor Inc. (South Korea) [6520-17]
- 4:50 pm: **Manufacturability issues with double patterning for 50-nm half-pitch single damascene applications using Relacs shrink and corresponding OPC**, M. Op de Beeck, J. Versluijs, V. Wiaux, T. Vandeweyer, I. Ciofi, H. Struyf, IMEC (Belgium) [6520-18]
- 5:10 pm: **The modeling of double exposure and double patterning lithographic processes**, S. A. Robertson, J. J. Biafore, T. Graves, M. D. Smith, KLA-Tencor Corp. [6520-19]
- 5:30 pm: **Dark-field double-dipole lithography (DDL) for back-end processes**, M. Burkhardt, IBM Corp.; J. Park, S. D. Hsu, ASML MaskTools Inc. [6520-97]

Panel Discussion

Room: Conv. Ctr. A2 Tues. 6:40 to 8:10 pm

Virtual Lithography: The Next Generation?

Chairs: **Mircea V. Dusa**, ASML US, Inc.; **Nigel R. Farrar**, Cymer, Inc.

Sponsored by **Canon**

We have entered a new era in lithography. Traditional developments based on “what will be the next exposure tool” is about to become more complicated with the introduction of ultra-high NA immersion, potential use of frequency-doubling patterning techniques and indeed EUV. The long-established hardware approach is transformed through the addition of an increasingly strong soft content which modifies the center of gravity of lithography development towards a math-driven activity where optimization and metrology add to modeling and simulation as key to achieve practical manufacturing at and below 32nm. Complex algorithms become the common denominator and the drivers of the growing math-driven lithography. They are present in all aspects of lithography, from design-based metrology algorithms to modeling, simulation, scanner and process optimization to determine realistic litho-aware design rules.

Will next generation lithography becoming a virtual lithography?

Our panel will explore the needs for advanced lithography developments and introduction into manufacturing from the perspective of a math -driven virtual algorithms compliant to next generation lithography. Participants include experts from semiconductor industry and universities.

SESSION 5

Room: Conv. Ctr. A2 Wed. 8:00 to 10:00 am

Optimization, Control, and Performance

Chairs: **Tatsuhiko Higashiki**, Toshiba Corp. (Japan); **Wilhelm Maurer**, Infineon Technologies AG (Germany)

- 8:00 am: **Evaluating the performance of a 193-nm hyper-NA immersion scanner using scatterometry**, O. Kritsun, R. Sandberg, A. Acheta, B. M. La Fontaine, H. J. Levinson, Advanced Micro Devices, Inc.; M. V. Dusa, J. Hauschild, A. Pici, ASML MaskTools Inc.; C. Saravanan, R. Korlahalli, S. Nirmalgandhi, Nanometrics Inc. [6520-21]
- 8:20 am: **Distinguishing dose, focus, and z-blur for lithography characterization and control**, C. P. Ausschnitt, IBM Microelectronics Div.; T. A. Brunner, IBM Thomas J. Watson Research Ctr.; J. Fullam, R. P. Deschner, IBM Microelectronics Div. [6520-22]
- 8:40 am: **Patterning control budgets for 45-nm and 32-nm generations incorporating lithography, design, and RET variations**, K. D. Lucas, J. L. Cobb, B. Ward, M. E. Kling, C. M. Cork, M. Drapeau, M. L. Rieger, Synopsys, Inc.; J. A. Allgair, International SEMATECH Manufacturing Initiative [6520-23]
- 9:00 am: **Control of polarization and apodization with stratified films on photomasks and pellicles for immersion lithography**, W. Cheng, Intel Corp. [6520-24]
- 9:20 am: **Global optimization of masks to maximize process-window through focus, including film stack design to restore TM contrast at high-NA**, A. E. Rosenbluth, IBM Thomas J. Watson Research Ctr.; N. Seong, IBM Microelectronics Div.; D. Melville, IBM Thomas J. Watson Research Ctr.; K. Tian, K. Lai, IBM Microelectronics Div.; D. Pfeiffer, M. Colburn, IBM Thomas J. Watson Research Ctr. [6520-25]
- 9:40 am: **A solution for exposure tool optimization at the 65-nm node and beyond**, D. Itai, Canon Inc. (Japan) [6520-26]
- Coffee Break 10:00 to 10:30 am

SESSION 6

Room: Conv. Ctr. A2 Wed. 10:30 am to 12:10 pm

OPC and Advanced Modeling I

Chairs: **Geert Vandenberghe**, IMEC (Belgium); **Kafai Lai**, IBM Microelectronics Div.

- 10:30 am: **Fast and accurate 3D mask model for full-chip OPC and verification**, P. Liu, Y. Cao, L. Chen, G. Chen, M. Feng, H. Liu, Brion Technologies, Inc. [6520-27]
- 10:50 am: **Process window and interlayer aware OPC for the 32-nm node**, R. M. Terry, Texas Instruments Inc. [6520-28]
- 11:10 am: **Optical proximity correction in memory-device patterns using boundary layer model for 3D mask topography effect**, Y. Kim, SAMSUNG Electronics Co., Ltd. (South Korea); J. L. Cobb, Synopsys, Inc.; S. Suh, S. Lee, S. Kim, SAMSUNG Electronics Co., Ltd. (South Korea); S. Lee, Synopsys (South Korea); Y. Cheon, S. Lee, S. Lee, H. Cho, J. Moon, SAMSUNG Electronics Co., Ltd. (South Korea) [6520-29]
- 11:30 am: **Generalized inverse lithography methods for phase-shifting mask design**, X. Ma, G. R. Arce, Univ. of Delaware [6520-30]
- 11:50 am: **Visualizing the impact of the illumination distribution upon imaging, and applying the insights gained**, S. D. Slonaker, Nikon Precision Inc. [6520-118]
- Lunch/Exhibition Break 12:10 to 1:10 pm

SESSION 7

Room: Conv. Ctr. A2 Wed. 1:10 to 3:10 pm

Image Quality and Characterization

Chairs: **Koichi Matsumoto**, Nikon Corp. (Japan); **Yao-Ching Ku**, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan)

- 1:10 pm: **Assessing the extendibility of chemically amplified resists through the use of MTF analysis employing 193 immersion IL, EUV IL, and e-beam lithography**, G. M. Wallraff, J. A. Hoffnagle, IBM Almaden Research Ctr.; P. Naulleau, Univ. at Albany; T. Honda, Canon Inc. (Japan); H. D. Truong, IBM Almaden Research Ctr. [6520-32]
- 1:30 pm: **Sources and scaling rules for LER and LWR**, T. Sandstrom, C. Rydberg, J. Bengtsson, Micronic Laser Systems AB (Sweden) ... [6520-33]
- 1:50 pm: **Polarization aberration analysis using Pauli-Zernike representation**, N. Yamamoto, Spansion Inc. (Japan); J. Kye, H. J. Levinson, Advanced Micro Devices, Inc. [6520-34]
- 2:10 pm: **Best focus determination: bridging the gap between optical and physical topography**, F. Kahlenberg, R. Seltmann, AMD Saxony LLC & Co. KG (Germany); B. M. La Fontaine, AMD Strategic Lithography Technology; R. Wirtz, AMD Saxony LLC & Co. KG (Germany); A. Kisteman, R. Vanneer, M. Pieters, ASML Netherlands B.V. (Netherlands) ... [6520-36]
- 2:30 pm: **In-situ measurement systems for realizing image performance at the 45-nm node and its effects**, K. Mishima, S. Miura, Y. Ohsaki, T. Yoshihara, Y. Hasegawa, Canon Inc. (Japan) [6520-37]
- 2:50 pm: **Study of iso-dense bias (IDB) sensitivity to laser spectral shape at the 45-nm node**, K. Yoshimochi, T. Tamura, T. Uchiyama, NEC Electronics Corp. (Japan); T. Theeuwes, R. Peters, H. Bakker, ASML Netherlands B.V. (Netherlands); K. Morisaki, ASML Japan Co., Ltd. (Japan); T. Oga, Cymer, Inc. [6520-138]
- Coffee Break 3:10 to 3:40 pm

SESSION 8

Room: Conv. Ctr. A2 Wed. 3:40 to 5:20 pm

Challenges for Water Immersion

Chairs: **Akiyoshi Suzuki**, Canon Inc. (Japan); **Pary Baluswamy**, Micron Technology, Inc.

- 3:40 pm: **Immersion defect reduction, part II: the formation mechanism and reduction of patterned defects**, L. Shiu, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan) [6520-38]
- 4:00 pm: **Optical error sensitivities of immersion lithography**, Z. G. Chen, IBM Corp.; K. Lai, IBM Microelectronics Div. [6520-39]
- 4:20 pm: **Contamination and particle control system in the immersion exposure tool**, M. Kobayashi, H. Nakano, M. Arakawa, K. Toyoda, T. Chibana, Y. Matsuoka, Y. Kawasaki, M. Tanabe, Canon Inc. (Japan) [6520-40]
- 4:40 pm: **Extending immersion lithography to the 32-nm node**, S. P. Warrick, W. E. Conley, Freescale Semiconductor, Inc. (France); M. Benndorf, J. Belledent, J. Gemmink, Philips Semiconductor (France); D. DeSimone, J. Chapon, C. Monget, V. Farys, P. Goirand, ST Microelectronics (France) [6520-41]
- 5:00 pm: **Immersion defectivity study with volume production immersion lithography tool**, K. Nakano, H. Kato, Y. Iriuchijima, T. Fujiwara, K. Shiraishi, S. Owa, Nikon Corp. (Japan) [6520-42]

SESSION 9

Room: Conv. Ctr. A2 Wed. 6:20 to 8:00 pm

Joint Session with conference 6521 on Computational Lithography

Chairs: **Alfred K. K. Wong**, Magma Design Automation; **Donis G. Flagello**, ASML US, Inc.

- 6:20 pm: **Model-based assist feature generation**, A. Sezginer, Invarium Inc. [6521-22]
- 6:40 pm: **Three-dimensional mask effect approximate modeling for sub-50-nm node device OPC**, S. Suh, S. Lee, SAMSUNG Electronics Co., Ltd. (South Korea) [6521-23]
- 7:00 pm: **Lossless I.C. layout compression: intra-cell, inter-cell sub-cell detection**, A. X. Gu, A. Zakhor, Univ. of California/Berkeley . [6520-43]
- 7:20 pm: **Advances in compute hardware platforms for computational lithography**, T. A. Kingsley, Mentor Graphics Corp. [6520-44]
- 7:40 pm: **SEM image contouring for OPC model calibration and verification**, C. E. Tabery, Advanced Micro Devices, Inc.; H. Morokuma, R. Matsuoka, Hitachi High-Technologies Corp. (Japan); L. R. Page, High-Technologies America, Inc.; G. E. Bailey, I. Kusnadi, T. Do, Mentor Graphics Corp. [6520-167]

Thursday 1 March

SESSION 10

Room: Conv. Ctr. A2 Thurs. 8:20 to 10:20 am

Advanced Resolution Enhancement

Chairs: **Harry J. Levinson**, Advanced Micro Devices, Inc.; **Tatsuhiko Higashiki**, Toshiba Corp. (Japan)

- 8:20 am: **Phase-shifted assist feature OPC for sub-45-nm node optical lithography**, G. Yoon, H. Kim, J. Lee, S. Choi, W. Han, SAMSUNG Electronics Co., Ltd. (South Korea) [6520-45]
- 8:40 am: **The random contact hole solutions for future technology nodes**, A. C. Chen, ASML Taiwan Ltd. (Taiwan); S. G. Hansen, ASML US, Inc.; M. H. P. Moers, ASML Netherlands B.V. (Netherlands) [6520-46]
- 9:00 am: **Patterning with amorphous carbon spacer for expanding the resolution limit of current lithography tool**, W. Y. Jung, Hynix Semiconductor Inc. (South Korea) [6520-48]
- 9:20 am: **32-nm SOC printing with double exposure techniques, regular design, inverse lithography, and 1.2 NA scanner**, Y. Trouiller, Lab. d'Electronique de Technologie de l'Information (France) ... [6520-49]
- 9:40 am: **Ultra-low k1 oxide contact hole formation and metal filling using resist contact hole pattern by double L&S pattern formation method**, H. Nakamura, M. Omura, S. Yamashita, Y. Taniguchi, J. Abe, S. Tanaka, S. Inoue, Toshiba Corp. (Japan) [6520-50]
- 10:00 am: **RET application in 45-nm node and 32-nm node contact hole dry ArF lithography process development**, X. J. Miao, X. Xu, Y. Chen, Applied Materials, Inc. [6520-47]
- Coffee Break 10:20 to 10:50 am

SESSION 11

Room: Conv. Ctr. A2 Thurs. 10:50 am to 12:30 pm

Mask Effect and Technologies

Chairs: Wilhelm Maurer, Infineon Technologies AG (Germany); Pary Baluswamy, Micron Technology, Inc.

- 10:50 am: **Optical mask CD calibration for hyper-high-NA 193-nm applications**, R. Ziebold, Qimonda Dresden GmbH & Co. OHG (Germany); R. Koehle, Qimonda AG (Germany); F. Katzwinkel, Qimonda Dresden GmbH & Co. OHG (Germany); A. C. Duerr, Advanced Mask Technology Ctr. (Germany) [6520-51]
- 11:10 am: **Pupil plane analysis on AIMS™ 45-193i for advanced photomasks**, Y. Morikawa, T. Sutou, Y. Inazuki, T. Adachi, N. Toyama, Y. Kitahata, T. Yokoyama, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan); U. Stroessner, W. Degel, R. Richter, Carl Zeiss SMS GmbH (Germany) [6520-52]
- 11:30 am: **The impact of the mask stack and its optical parameters on the imaging performance**, A. Erdmann, P. Evanschitzky, T. Fühner, Fraunhofer-Institut für Integrierte Systeme und Bauelementetechnologie (Germany) [6520-53]
- 11:50 am: **Mask 3D effect on 45-nm imaging using attenuated PSM**, K. Sato, M. Itoh, T. Sato, Toshiba Corp. (Japan) [6520-54]
- 12:10 pm: **Effects of reticle birefringence on 193-nm lithography**, S. L. Light, Micron Technology, Inc.; C. Petz, Univ. of Washington; I. Tsyba, B. Rolfson, P. Baluswamy, Micron Technology, Inc. [6520-55]
- Lunch Break 12:30 to 1:30 pm

SESSION 12

Room: Conv. Ctr. A2 Thurs. 1:30 to 3:30 pm

Immersion Advancements beyond Water

Chairs: Andrew Grenville, Intel Corp.; Han-Ku Cho, SAMSUNG Electronics Co., Ltd. (South Korea)

- 1:30 pm: **Early look into device level imaging with beyond water immersion**, W. E. Conley, S. P. Warrick, Freescale Semiconductor, Inc. (France); P. Goirand, STMicroelectronics (France); J. Gemmink, D. Van Steenwickel, Philips Semiconductors (France) [6520-56]
- 1:50 pm: **Extending immersion lithography with high-index materials**, H. Sewell, ASML US, Inc.; J. Mulken, ASML Netherlands B.V. (Netherlands); P. Graeupner, Carl Zeiss SMT AG (Germany); D. C. McCafferty, L. Markoya, ASML US, Inc.; S. Donders, ASML Netherlands B.V.; R. Duesing, Carl Zeiss SMT AG (Germany) [6520-57]
- 2:10 pm: **Development status of high-index lens material LuAG for ArF hyper-NA immersion systems**, L. Parthier, G. Wehrhan, D. Keutel, K. Knapp, SCHOTT Lithotec AG (Germany) [6520-58]
- 2:30 pm: **High-index immersion lithography with second-generation immersion fluids to enable numerical apertures of 1.55 for cost effective 32-nm half pitches**, R. H. French, D. J. Adelman, J. Feldman, M. F. Lemon, S. J. McClain, W. Qiu, A. L. Shoe, H. V. Tran, R. C. Wheland, M. K. Yang, DuPont Co. [6520-59]
- 2:50 pm: **High-index fluoride materials for 193-nm immersion lithography**, T. Nawata, Y. Inui, T. Mabuchi, I. Masada, E. Nishijima, Tokuyama Corp. (Japan); H. Sato, T. Fukuda, Tohoku Univ. (Japan) [6520-60]
- 3:10 pm: **Feasibility of 37-nm half-pitch with ArF high-index immersion lithography**, Y. Sekine, M. Kawashima, E. Sakamoto, T. Honda, Canon Inc. (Japan) [6520-61]
- Coffee Break 3:30 to 4:00 pm

SESSION 13

Room: Conv. Ctr. A2 Thurs. 4:00 to 5:40 pm

OPC and Advanced Modeling II

Chairs: Bruce W. Smith, Rochester Institute of Technology; Donis G. Flagello, ASML US, Inc.

- 4:00 pm: **Application of full-chip optical proximity correction for sub-60-nm memory device in polarized illumination**, H. Yune, Y. Ahn, D. Lee, J. Moon, B. M. Nam, D. Yim, Hynix Semiconductor Inc. (South Korea) [6520-62]
- 4:20 pm: **Utilization of optical proximity effects for resist image stitching**, Y. Fan, T. Castro, Intel Corp. [6520-63]
- 4:40 pm: **Methods for comparative extraction of OPC response**, T. E. Zavec, TEA Systems Corp. [6520-64]
- 5:00 pm: **ACLV driven double-patterning decomposition with extensively added printing assist features (PrAFs)**, J. E. Meiring, IBM Microelectronics Div.; H. Haffner, Infineon Technologies NA Corp.; C. A. Fonseca, S. D. Halle, S. M. Mansfield, IBM Microelectronics Div. [6520-65]
- 5:20 pm: **A discussion of the regression of physical parameters for photolithographic process models**, L. S. Melvin III, J. P. Shiely, Synopsys, Inc. [6520-66]

✓ Posters- Thursday

Room: Convention Ctr. Hall 3 Thurs. 5:30 to 8:00 pm

The following posters will be displayed all day Thursday. Authors will be present during the formal poster session Thursday evening between 5:30 and 8:00 pm for discussion. Authors may set-up their posters after 9:00 am on Thursday.

Developments in RET

- ✓ **Optical performance enhancement technique for 45-nm node with binary mask**, J. Jung, H. Kim, J. Lee, S. Choi, W. Han, SAMSUNG Electronics Co., Ltd. (South Korea) [6520-78]
- ✓ **Size tolerance of subresolution assist features for sub-50-nm node device**, B. Kim, S. Lee, H. Shin, N. Lee, SAMSUNG Electronics Co., Ltd. (South Korea) [6520-79]
- ✓ **A method for generating assist-features in full-chip scale and its application to contact layers of sub-70-nm DRAM devices**, D. Park, C. Hwang, S. Lee, H. Cho, J. Moon, SAMSUNG Electronics Co., Ltd. (South Korea) [6520-80]
- ✓ **Process window optimization of CPL mask for beyond 45-nm lithography**, S. Tan, Q. Lin, Chartered Semiconductor Manufacturing Ltd. (Singapore); C. J. Tay, C. Quan, National Univ. of Singapore (Singapore) [6520-82]
- ✓ **SRAF placement and sizing using inverse lithography technology**, T. Lin, Luminescent Technologies, Inc.; F. Robert, Crolles II Alliance (France); A. Borjon, Philips Semiconductors (France); G. Russell, Luminescent Technologies, Inc.; C. Martinelli, Crolles II Alliance (France); A. Moore, Luminescent Technologies, Inc.; Y. F. Rody, Philips Semiconductors (France) [6520-83]
- ✓ **Optimal SRAF placement for process window enhancement in 65-nm/45-nm technology**, C. S. Sarma, K. Herold, P. Schroeder, Infineon Technologies North America; A. Thomas, IBM Microelectronics Div. [6520-84]
- ✓ **Intensity weighed focus drilling exposure for maximizing process window of sub-100-nm contact by simulation**, S. Jung, E. T. Yang, T. H. Yang, K. Chen, C. Lu, Macronix International Co., Ltd. (Taiwan) [6520-85]
- ✓ **Process margin improvement using custom transmission EAPSM reticles**, E. Byers, S. Agarwal, B. Rolfson, Micron Technology, Inc.; C. J. Proglar, Photronics, Inc. [6520-86]
- ✓ **Verification of high-transmittance PSM with polarization at 193-nm high-NA system**, C. Chiu, C. Chen, J. Lee, Nanya Technology Corp. (Taiwan) [6520-88]

Double Patterning and Exposure Technology

- ✓ **A litho-only solution to double patterning**, A. Vanleenhove, D. Vansteenwinckel, Philips Research Leuven (Belgium) [6520-20]
- ✓ **Novel lithographic technique for differential exposure of distinct patterns on the same mask**, M. Bollin, E. Annoni, G. Capetti, G. Cotti, STMicroelectronics (Italy) [6520-89]
- ✓ **A study of double exposure process design with balanced performance parameters for line/space applications**, J. Zhu, P. Wu, Q. Wu, H. Ding, X. Li, C. Sun, Shanghai Hua Hong NEC Electronics Co., Ltd. (China) [6520-90]
- ✓ **The improvement of photolithographic fidelity of two-dimensional structures through double exposure method**, H. Ding, X. Li, C. Sun, J. Zhu, Q. Wu, Shanghai Huahong NEC Electronics Co., Ltd. (China) [6520-91]
- ✓ **Double patterning with multilayer hard mask shrinkage for sub-0.25 k1 lithography**, R. Liu, W. Hsieh, C. Yeh, W. Wu, F. Chen, C. Shih, T. Huang, J. Lin, Nanya Technology Corp. (Taiwan) [6520-92]
- ✓ **Sub-k1 = 0.25 lithography with double patterning technique for 45-nm technology node flash memory devices at $\lambda = 193\text{nm}$** , G. Capetti, P. Cantu', G. Cotti, E. Galassini, F. D'Angelo, C. Turco, A. Vaccaro, STMicroelectronics (Italy); A. Vaglio Pret, STMicroelectronics (Italy) and Politecnico di Milano (Italy); P. Rigolli, STMicroelectronics (Italy) [6520-93]
- ✓ **Extending DUV lithography to 10-nm resolution with the combination of photoresist quantum state control and stimulated emission depletion imaging techniques**, R. D. Frankel, RDF Consulting and Chromaplex, Inc. [6520-94]
- ✓ **Double exposure using 193-nm negative tone photoresist**, R. Kim, T. I. Wallow, J. Kye, H. J. Levinson, Advanced Micro Devices, Inc.; D. C. White, Tokyo Ohka Kogyo America, Inc. [6520-95]
- ✓ **The feasible study of splitting pitch technology on 45-nm contact patterning with 0.93 NA**, Y. Cheng, Y. Chou, T. C. Tseng, B. Hsueh, C. Yang, United Microelectronics Corp. (Taiwan) [6520-96]
- ✓ **A study of process window capabilities for two-dimensional structures under double exposure condition**, Q. Wu, P. Wu, J. Zhu, H. Ding, X. Li, C. Sun, Shanghai Hua Hong NEC Electronics Co., Ltd. (China) [6520-98]
- ✓ **New double exposure technique without alternating phase-shift mask**, T. Yamamoto, T. Yao, H. Futatsuya, T. Chijimatsu, S. Asai, Fujitsu Ltd. (Japan) [6520-99]
- ✓ **ILT and double exposure: materials, mask-making and mask-to-mask alignment considerations**, A. A. Poonawala, Univ. of California/ Santa Cruz; Y. A. Borodovsky, Intel Corp.; P. Milanfar, Univ. of California/ Santa Cruz [6520-100]

Exposure Tools, Subsystems, and Materials

- ✓ **Development and characterization of a 300-mm dual-side alignment stepper**, W. W. Flack, R. Hsieh, E. True, R. Ellis, Ultratech, Inc. [6520-101]
- ✓ **Characterization of absorbance losses and wavefront deformation in DUV optics**, K. Mann, U. Leinhos, B. Schäfer, T. Miede, Laser-Lab. Göttingen e.V. (Germany) [6520-102]
- ✓ **Flare effect of different shape of illumination apertures in 193-nm optical lithography system**, Y. Yun, J. Kim, K. Kim, Dongbu Electronics Co., Ltd. (South Korea) [6520-103]
- ✓ **Silicon verification of flare model and application to real chip for long-range proximity correction**, Z. D. Qing, B. Choi, Chartered Semiconductor Manufacturing Ltd. (Singapore) [6520-104]
- ✓ **Thermal aberration control for low-k1 lithography**, Y. Uehara, T. Matsuyama, T. Nakashima, Y. Ohmura, T. Ogata, K. Suzuki, N. Tokuda, Nikon Corp. (Japan) [6520-105]
- ✓ **Quasi-telecetricity: the effects of unbalanced multipole illumination**, S. P. Renwick, Nikon Precision Inc.; K. E. Huggins, Intel Corp. [6520-106]
- ✓ **Novel high-throughput micro-optical beam shapers reduce the complexity of macro-optics in hyper-NA illumination systems**, T. Bizjak, T. Mitra, L. Aschke, LIMO-Lissotschenko Mikroskopik GmbH (Germany) [6520-107]

- ✓ **Advanced polarizer for 193-nm immersion lithography**, H. Bernitzki, M. Klaus, H. Lauth, U. Schuhmann, JENOPTIK Laser, Optik, Systeme GmbH (Germany); J. Bruebach, M. Klaassen, ASML Netherlands B.V. (Netherlands) [6520-108]
- ✓ **A solid state 193-nm laser with high-spatial coherence for sub-30-nm interferometric immersion lithography**, A. J. Merriam, Actinix; D. S. Bethune, J. A. Hoffnagle, M. Jefferson, IBM Almaden Research Ctr.; J. J. Jacob, Actinix; T. J. Litvin, Kimokeo, Inc. [6520-109]
- ✓ **New investigations regarding the prevention of depolarization of ArF excimer laser irradiation by CaF2 laser optics**, U. Natura, D. Keutel, SCHOTT Lithotec AG (Germany); M. Letz, SCHOTT AG (Germany); L. Parthier, K. Knapp, SCHOTT Lithotec AG (Germany) [6520-110]
- ✓ **Reliable high-power injection locked 6kHz 60W laser for ArF immersion lithography**, H. Watanabe, S. Komae, R. Nohdomi, T. Yamazaki, H. Nakarai, J. Fujimoto, Gigaphoton Inc. (Japan); T. Matsunaga, K. Kakizaki, Komatsu Ltd. (Japan); H. Mizoguchi, Gigaphoton Inc. (Japan) [6520-111]
- ✓ **Increased availability of lithography light sources using advanced gas management**, W. J. Dunstan, R. N. Jacques, K. O'Brien, A. Ratnam, Cymer, Inc. [6520-112]
- ✓ **A study of overlay mark robustness and enhanced alignment techniques for alignment improvement on metal layers of sub-100-nm technology**, K. Dubey, T. Nakamura, Canon Singapore Pte., Ltd. (Singapore) [6520-114]
- ✓ **The optimization of zero-spaced microlens for 2.2 μm and 1.7 μm** , H. Nam, J. Park, J. Park, J. Choi, J. Lee, MagnaChip Semiconductor, Ltd. (South Korea) [6520-115]
- ✓ **Laser durability studies of high-index immersion fluids: fluid degradation and optics contamination effects**, V. Liberman, S. T. Palmacci, M. Rothschild, MIT Lincoln Lab.; A. Grenville, Intel Corp.; P. A. Zimmerman, SEMATECH, Inc. [6520-197]

Illumination Optimization and Control

- ✓ **Illumination optimization with actual information of exposure tool and resist process**, K. Tsujita, K. Mikami, R. Naka, N. Baba, T. Ono, A. Suzuki, Canon Inc. (Japan) [6520-116]
- ✓ **Impact of illumination performance on hyper-NA imaging for 45-nm node**, K. Mori, A. Yamada, T. Shiozawa, K. Takahashi, Canon Inc. (Japan) [6520-117]
- ✓ **Optimal solutions for the illuminator and final lens pupil coupled distributions beyond the axial symmetry**, I. A. Ivonin, T. Sandstrom, Micronic Laser Systems AB (Sweden) [6520-120]
- ✓ **Sensitivity of hyper-NA immersion lithography to illuminator imperfections**, W. Gao, SIGMA-C Software AG (Germany); L. De Winter, ASML Netherlands B.V. (Netherlands) [6520-122]

Image and Process Modeling

- ✓ **The calibration of process window model for 55-nm node**, I. Y. Su, Synopsys, Inc. (Taiwan); C. Wu, I. Huang, C. Yang, C. W. Huang, T. Tsai, United Microelectronics Corp. (Taiwan); B. Falch, Synopsys, Inc. [6520-123]
- ✓ **Contour-based data extraction for model calibration**, T. H. Wu, United Microelectronics Corp. (Taiwan) [6520-124]
- ✓ **Distributed model calibration using Levenberg-Marquardt algorithm**, M. Lu, L. Zhu, Grace Semiconductor Manufacturing Corp. (China); L. Li, G. Zhang, W. Chan, X. Zhou, Anchor Semiconductor Inc. (China) [6520-125]
- ✓ **Analytical approach to high-NA images**, S. Kim, The Catholic Univ. of Korea (South Korea) [6520-126]
- ✓ **Modeling and performance metrics for longitudinal chromatic aberrations, focus-drilling, and Z-noise: exploring excimer laser pulse spectra**, M. D. Smith, KLA-Tencor Corp.; J. Bendik, Dynamic Intelligence; I. Lalovic, N. R. Farrar, Cymer, Inc.; W. B. Howard, C. Sallee, KLA-Tencor Corp. [6520-127]

- ✓ **Dr.LiTHO: a development and research lithography simulator**, T. Fühner, T. Schnattinger, G. Ardelean, A. Erdmann, Fraunhofer-Institut für Integrierte Systeme und Bauelementetechnologie (Germany) . [6520-131]
- ✓ **Lithographic characterization of evanescent-wave imaging systems**, T. Graves, S. Robertson, M. D. Smith, KLA-Tencor Corp. [6520-132]
- ✓ **32-nm OPC design rule evaluation through virtual patterning**, S. W. Jessen, G. Zhang, M. E. Mason, Texas Instruments Inc.; Y. Zhang, D. A. Legband, C. Sallee, KLA-Tencor Corp. [6520-133]
- ✓ **Heuristics for truncating the number of optical kernels in Hopkins image calculations for model-based OPC treatment**, C. D. Zuniga, ASML MaskTools Inc. [6520-134]

Image Quality and Characterization

- ✓ **Topography induced defocus with a scanning exposure system**, B. R. Liegl, N. M. Felix, D. M. Dobuzinsky, IBM Corp. [6520-136]
- ✓ **Precise measurement of process bias and its relation to MEEF**, T. E. Zavec, TEA Systems Corp. [6520-139]
- ✓ **Assessment of trade-off between resist resolution and sensitivity for optimization of hyper-NA immersion lithography**, Y. Kishikawa, T. Honda, Y. Iwasaki, A. Ohkubo, M. Kawashima, M. Yoshii, Canon Inc. (Japan) [6520-140]
- ✓ **Understanding the impact of rigorous mask effects in the presence of resist models**, M. C. Lam, K. Adam, Mentor Graphics Corp. [6520-141]
- ✓ **Transistor-based electrical test structures for lithography and process characterization**, W. J. Poppe, J. A. Holwill, P. D. Friedberg, L. Alarcon, L. Pang, Q. Liu, A. R. Neureuther, Univ. of California/Berkeley [6520-142]
- ✓ **Use of starburst patterns in optical lithography**, M. Burkhardt, IBM Corp.; C. E. Tabery, Advanced Micro Devices, Inc. [6520-143]
- ✓ **Challenging to meet 1-nm iso-dense bias (IDB) by controlling laser spectrum**, T. Oga, Cymer, Inc. (Japan) [6520-144]
- ✓ **Impact of mask error on OPC for 45-nm node**, O. Park, Infineon Technologies North America [6520-145]
- ✓ **Taking image quality factor into the OPC model tuning flow**, C. Wang, Q. Liu, Semiconductor Manufacturing International Corp. (China); L. Zhang, Mentor Graphics Corp. (China) [6520-147]
- ✓ **Effects of laser bandwidth on iso-dense bias and line-end shortening at the 65-nm/45-nm node**, R. C. Peng, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan) [6520-148]
- ✓ **On the quality of measured optical aberration coefficients using phase wheel monitor**, L. V. Zavyalova, A. R. Robinson, A. Bourov, B. W. Smith, Rochester Institute of Technology [6520-149]
- ✓ **A comparative study for mask defect tolerance on phase and transmission for dry and immersion 193-nm lithography**, M. L. Ling, C. J. Tay, C. Quan, National Univ. of Singapore (Singapore); Q. Lin, G. S. Chua, Chartered Semiconductor Manufacturing Ltd. (Singapore) [6520-150]
- ✓ **Understanding the causes of horizontal-vertical (H-V) bias in optical lithography, part II**, J. J. Biafore, KLA-Tencor Corp.; C. A. Mack, Lithoguru.com; S. Kapasi, M. D. Smith, S. A. Robertson, KLA-Tencor Corp. [6520-151]

OPC and Implementation

- ✓ **OPC-free on-grid fine random hole pattern formation utilizing double resist patterning with double RETs**, S. Nakao, S. Maejima, A. Imai, T. Hanawa, K. Suko, Renesas Technology Corp. (Japan) [6520-153]
- ✓ **Virtual OPC for hyper-NA lithography**, S. Lee, SAMSUNG Electronics Co., Ltd. (South Korea) [6520-155]
- ✓ **Mask-friendly OPC correction for higher throughput and lower mask costs**, A. M. Yehia, Mentor Graphics Corp. (Egypt) . . . [6520-156]

- ✓ **Methods and factors for OPC run-time optimization**, A. Dave, C. P. Babcock, Advanced Mirco Devices, Inc.; S. N. McGowan, Y. Zou, Advanced Micro Devices, Inc. [6520-157]
- ✓ **Golden curve method for reticle and OPC signature stability control of optimized lithography in advanced high-MEEF applications under DFM flows**, K. Geidel, Advanced Mask Technology Ctr. GmbH & Co. KG (Germany); T. Franke, Qimonda AG (Germany); S. Roling, AMD Saxony LLC & Co. KG (Germany); E. Mittermeier, Qimonda AG (Germany); M. Sczyrba, R. B. Cinque, Advanced Mask Technology Ctr. KG (Germany); E. L. Carpi, P. D. Buck, C. A. West, A. R. Eckert, Toppan Photomasks, Inc.; C. A. Spence, AMD Saxony LLC & Co. KG (Germany) [6520-158]
- ✓ **Mask enhancement using an evanescent wave effect**, N. V. Lafferty, J. Zhou, A. Bourov, B. W. Smith, Rochester Institute of Technology [6520-159]
- ✓ **The gate CD uniformity improvement by the layout retarget with refer to the litho process**, N. Chung, SAMSUNG Electronics Co., Ltd. (South Korea) [6520-160]
- ✓ **Toward standard process models for OPC**, Y. Granik, D. M. Medvedev, N. Cobb, Mentor Graphics Corp. [6520-161]
- ✓ **Modular process modeling for OPC**, M. C. Keck, C. T. Bodendorf, Qimonda AG (Germany) [6520-162]
- ✓ **Predictive post-OPC contact and via printability metric and validation**, P. Yu, D. Z. Pan, The Univ. of Texas/Austin [6520-163]
- ✓ **Analysis of pattern density on process proximity compensation**, S. Jung, F. Lo, T. C. Yang, T. Yang, K. Chen, C. Lu, Macronix International Co., Ltd. (Taiwan) [6520-165]
- ✓ **Advanced new OPC method to improve OPC accuracy for sub-90-nm technology**, J. Y. Choi, J. Kang, Y. Shim, K. H. Yun, J. H. Hong, Y. S. Lee, K. Kim, Dongbu Electronics Co., Ltd. (South Korea) . . . [6520-166]
- ✓ **Improving the model robustness for OPC by extracting relevant test patterns for calibration**, M. Jeong, Samsung Electronics Co., Ltd (South Korea); S. Lee, J. Jung, C. Hyon, I. Choi, Y. Kang, Y. Park, Samsung Electronics Co., Ltd. (South Korea) [6520-168]
- ✓ **Two-dimensional dry-etch modeling using local density approach for 65-nm node and beyond**, A. Borjon, Philips Semiconductors (France); C. Gardin, Freescale Semiconductor, Inc. (French Polynesia); J. Belledent, Philips Semiconductors; Y. Trouiller, Lab. d'Electronique de Technologie de l'Information; C. Couderc, Philips Semiconductors; F. Sundermann, F. Foussadier, J. Urbani, STMicroelectronics; Y. F. Rody, Philips Semiconductors [6520-169]
- ✓ **Rapid search of the optimum placement of assist feature to improve the aerial image gradient in iso-line structure**, J. Li, Q. Yan, L. S. Melvin III, Synopsys, Inc. [6520-170]
- ✓ **Implementation of pixel-based OPC considered process variation with process window model**, J. Maeng, S. Bae, Y. Yun, B. Seo, S. Lee, H. Shin, N. Lee, SAMSUNG Electronics Co., Ltd. (South Korea) [6520-171]
- ✓ **A feasible model-based OPC algorithm using Jacobian matrix of intensity distribution functions**, Y. Chen, Z. Shi, X. Yan, Zhejiang Univ. (China) [6520-172]
- ✓ **Geometrical description of the microloading effect in silicon trench structures**, I. Titarenko, E. Altshuler, R. Tweg, Tower Semiconductor Ltd. (Israel) [6520-173]
- ✓ **Investigation of DFM-lite ORC approach during OPC simulation**, C. Lim, V. Temchenko, Infineon Technologies AG (Germany); M. Niehoff, Mentor Graphics Corp. (Germany); D. Kaiser, K. Peter, D. Wallis, I. Meusel, Infineon Technologies AG (Germany) [6520-174]
- ✓ **Migrating from traditional OPC to field-based OPC for 45-nm node production**, R. Farnbach, J. P. Tuttle, M. M. St. John, R. Brown, D. J. Gerold, R. M. Lugg, J. P. Shiely, M. L. Rieger, Synopsys, Inc. [6520-175]

Optimization, Control, and Performance

- ✓ **A study of 3D mask effect on CD variation for 65/45nm**, C. Hung, Semiconductor Manufacturing International Corp. (Singapore); Y. Gong, Jade Semiconductor Ltd. (China) [6520-176]
- ✓ **CDU minimization at the 45-nm node and beyond: optical, resist, and process contributions to CD control**, S. A. Scheer, M. Carcasi, Tokyo Electron America, Inc.; T. Shibata, T. Otsuka, Tokyo Electron Kyushu Ltd. (Japan) [6520-177]
- ✓ **ACLV performance dry versus immersion on 45-nm ground rules**, U. P. Schröder, Infineon Technologies North America; C. C. Yap, IBM Corp.; C. S. Sarma, Infineon Technologies North America; A. Thomas, IBM Corp. [6520-179]
- ✓ **The feasible study of 45-nm metal patterning on 0.93 NA**, Y. Cheng, Y. Chou, Y. Hou, B. J. Lu, C. Yang, United Microelectronics Corp. (Taiwan) [6520-181]
- ✓ **Optimization of DUV lithography for high-energy well implantation**, R. P. Deschner, IBM Microelectronics Div.; R. W. Mann, IBM Corp.; S. Stiffler, P. Nguyen, G. M. Johnson, IBM Microelectronics Div. [6520-182]
- ✓ **Challenges and solutions for transferring a 248-nm process to 365-nm imaging**, A. Serebriakov, E. Shi, H. van den Broek, L. Zhao, ASML Netherlands B.V. (Netherlands) [6520-183]
- ✓ **New color alignment for CMOS image sensor**, M. Kish-Dagan, Tower Semiconductor Ltd. (Israel); R. D. M. Edart, ASML Netherlands B.V. (Netherlands); H. Rechtmann, Tower Semiconductor Ltd. (Israel); Y. Kanfi, P. Warnaar, ASML Netherlands B.V. (Netherlands); O. Moshe, Tower Semiconductor Ltd. (Israel); R. J. F. van Haren, ASML Netherlands B.V. (Netherlands) [6520-184]
- ✓ **A thin FinFET Si-fin body structure fabricated with 193-nm scanner photolithography**, W. Liao, United Microelectronics Corp. (Taiwan) [6520-185]
- ✓ **ARC stack development for hyper-NA imaging**, V. Farys, STMicroelectronics (France) [6520-186]
- ✓ **A thick CESL stressed ultra-small (Lg=40nm) SiGe-channel MOSFET fabricated with 193-nm scanner lithography and TEOS hard mask etching**, W. Liao, United Microelectronics Corp. (Taiwan) [6520-187]

Photomask Technology

- ✓ **Three-dimensional mask effects and source polarization impact on OPC model accuracy and process window**, M. Saied, Freescale Semiconductor, Inc. (France); F. Foussadier, STMicroelectronics (France); J. Belledent, Philips Semiconductors (France); Y. Trouiller, Lab. d'Electronique de Technologie de l'Information (France); I. Schanen, École Nationale Supérieure d'Electronique et de Radioélectrique de Grenoble (France); C. Gardin, Freescale Semiconductor, Inc. (France); J. Urbani, STMicroelectronics (France); A. Borjon, L. Le Cam, Philips Semiconductors (France); P. K. Montgomery, Freescale Semiconductor, Inc. (France); F. Sundermann, STMicroelectronics (France); Y. F. Rody, Philips Semiconductors (France); F. Robert, Crolles II Alliance (France); C. Couderc, Philips Semiconductors (France); F. Vautrin, G. Kerrien, J. Planchot, STMicroelectronics (France); E. Yesilada, Freescale Semiconductor (France); C. Martinelli, Crolles II Alliance (France); B. Winkinson, Freescale Semiconductor, Inc. (France) [6520-188]
- ✓ **The choice of mask in consideration of polarization effects at high-NA system**, S. Kim, SAMSUNG Electronics Co., Ltd. (South Korea) [6520-189]
- ✓ **Analysis of diffraction orders including mask topography effects for OPC optimization**, Y. Inazuki, N. Toyama, T. Adachi, T. Nagai, T. Sutou, Y. Morikawa, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan) [6520-190]

Polarization, Hyper-NA, and Immersion Lithography

- ✓ **Immersion lithography with numerical apertures above 2.0 using high-index optical materials**, J. Zhou, N. V. Lafferty, A. Bourov, B. W. Smith, Rochester Institute of Technology; J. Burnett, National Institute of Standards and Technology [6520-191]
- ✓ **Immersion defect reduction, part I: analysis of water leaks in an immersion scanner**, F. Liang, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan) [6520-193]
- ✓ **Defect testing using an immersion exposure system to apply immediate pre-exposure and post-exposure water soaks**, R. Watso, B. Pierson, K. D. Cummings, ASML US, Inc. [6520-194]
- ✓ **Characteristics of state-of-art lithography optics represented using the first canonical coordinate of lie group**, T. Fujii, Y. Kudo, Y. Oomura, K. Suzuki, J. Kogo, Y. Mizuno, N. Kita, Nikon Corp. (Japan) [6520-195]
- ✓ **Characteristics analysis of polarization module on optical proximity effect**, C. Park, Hynix Semiconductor Inc. (South Korea) ... [6520-196]

Friday 2 March

SESSION 14

Room: Conv. Ctr. A2 Fri. 8:15 to 9:55 am

Advanced Exposure Systems and Components I

Chairs: **Akiyoshi Suzuki**, Canon Inc. (Japan); **Gary Zhang**, Texas Instruments Inc.

8:15 am: **Latest results from the hyper-NA immersion scanners S609B and S610C**, J. Ishikawa, T. Fujiwara, Nikon Corp. (Japan); K. Shiraishi, Nikon Cop. (Japan); Y. Ishii, M. Nei, Nikon Corp. (Japan) [6520-67]

8:35 am: **Immersion exposure tool for the 45-nm HP mass production**, H. Kubo, H. Hata, F. M. Sakai, N. Deguchi, T. Iwanaga, T. Ebihara, Canon Inc. (Japan) [6520-68]

8:55 am: **Performance of a 1.35NA ArF immersion lithography system for 40-nm applications**, J. de Klerk, M. Suddendorf, R. Droste, L. Jorritsma, L. Levasier, ASML Netherlands B.V. (Netherlands); T. Heil, Carl Zeiss SMT AG [6520-69]

9:15 am: **Exposure and compositional factors that influence polarization induced birefringence in silica glass**, U. Neukirch, D. C. Allan, M. Mlejnek, C. M. Smith, Corning Inc. [6520-70]

9:35 am: **XLR 500i: recirculating ring ArF light source for immersion lithography**, P. J. O'Keeffe, V. B. Fleurov, R. Rokitski, R. Bergstedt, I. V. Fomenkov, D. Brown, N. R. Farrar, W. N. Partlo, Cymer, Inc. [6520-71]

Coffee Break 9:55 to 10:25 am

Best Student Paper Award

Room: Conv. Ctr. A2 Fri. 10:25 to 10:35 am

Chair: **Donis G. Flagello**, ASML US, Inc.

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SESSION 15

Room: Conv. Ctr. A2 Fri. 10:35 am to 12:15 pm

Advanced Exposure Systems and Components II*Chairs: Geert Vandenberghe*, IMEC (Belgium); *Koichi Matsumoto*, Nikon Corp. (Japan)10:35 am: **Catadioptric projection lens system for 1.3 NA scanner**, T. Matsuyama, Y. Ohmura, J. Misawa, Y. Fujishima, T. Koyama, Nikon Corp. (Japan)[6520-72]10:55 am: **New projection optics and aberration control system for the 45-nm node**, T. Yoshihara, Y. Hasegawa, B. Takeshita, Y. Ohsaki, K. Mishima, S. Miura, Canon Inc. (Japan)[6520-73]11:15 am: **Integration of a new alignment sensor for advanced technology nodes**, P. C. Hinnen, J. Depre, ASML Netherlands B.V. (Netherlands); S. Tanaka, ASML Japan Co., Ltd. (Japan); S. Lim, M. Shahrjerdy, ASML Netherlands B.V. (Netherlands); K. Ishigo, T. Kono, T. Higashiki, Toshiba Corp. (Japan)[6520-74]11:35 am: **Ultra-narrowed injection lock laser light source for higher NA ArF immersion lithography tool**, M. Shimbori, Ushio Inc. (Japan); T. Matsunaga, T. Suzuki, K. Kakizaki, Komatsu Ltd. (Japan); S. Tanaka, M. Yoshino, Gigaphoton Inc. (Japan); T. Kumazaki, S. Nagai, Y. Kawasuji, H. Umeda, Komatsu Ltd. (Japan); H. Nagano, Y. Sasaki, Ushio Inc. (Japan); H. Taniguchi, H. Mizoguchi, Gigaphoton Inc. (Japan)[6520-75]11:55 am: **Demonstration of sub-45-nm features using azimuthal polarization on the 1.3NA exitech immersion microstepper**, E. C. Piscani, S. R. Palmer, C. K. Van Peski, SEMATECH, Inc.[6520-77]**Courses of Related Interest***Register for courses at the SPIE registration desk.*

SC101 Introduction to Microlithography: Theory, Materials, and Processing (Willson, Bowden, Thompson) Sunday 8:30 am to 5:30 pm

SC102 Optical Lithography Modeling (Neureuther, Smith) Sunday 6:00 to 10:00 pm

SC105 CD Metrology and Image Formation in the Scanning Electron Microscope (SEM) (Wells, Postek) Sunday 8:30 am to 5:30 pm

SC116 Lithographic Optimization: A Theoretical Approach (Mack) Sunday 8:30 am to 5:30 pm

SC117 The Fundamental Limits of Optical Lithography (Smith) Sunday 8:30 am to 12:30 pm

SC118 Anti-Reflective Coatings: Theory and Practice (Dammel) Thursday 8:30 am to 12:30 pm

SC120 193-nm Photoresist Materials (Dammel) Sunday 8:30 am to 12:30 pm

SC124 Pushing the Limits: Optical Enhancement, Polarization, and Immersion Lithography (Smith) Sunday 1:30 to 5:30 pm

SC355 Fundamentals of Photochemical Contamination Control for Lithographic Tools (Kunz) Sunday 6:00 to 10:00 pm

SC540 Applying Optical Proximity Correction and Design for Manufacturability to Product Designs (Capodiceci, Lucas) Sunday 8:30 am to 5:30 pm

SC579 Photomask Fabrication and Technology Basics (*Duff*) Monday 8:30 am to 5:30 pm

SC705 Instruments and Methodologies for Accurate Metrology and Fleet Matching (Archie, Banke) Sunday 8:30 am to 5:30 pm

SC706 Imaging and Optics Fundamentals in Microlithography (Flagello) Sunday 1:30 to 5:30 pm

SC707 Basics of Optical Imaging in Microlithography: A Hands-on Approach (Milster, Flagello, Brooker) Sunday 8:30 am to 12:30 pm

SC779 Polarization for Lithographers (Kye, McIntyre) Monday 8:30 am to 12:30 pm

SC832 IP Issues in Advanced Lithography and Semiconductor Manufacturing (Gortych) Monday 1:30 to 5:30 pm

SC833 Lithography Integration for Semiconductor Back-End-Of-The-Line (BEOL) (Lin) Sunday 8:30 am to 12:30 pm

SC834 Lithography Friendly Design and Beyond - A Broader Review of DfM (Liebmann, Mansfield, Wong) Tuesday 8:30 am to 5:30 pm



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Design for Manufacturability through Design-Process Integration

Conference Chair: **Alfred K. K. Wong**, Magma Design Automation

Cochair: **Vivek K. Singh**, Intel Corp.

Program Committee: **Juan Antonio Carballo**, IBM Corp.; **Hiroichi Kawahira**, Sony Corp. (Japan); **Lars W. Liebmann**, IBM Microelectronics Div.; **Mark E. Mason**, Texas Instruments Inc.; **Kevin M. Monahan**, KLA-Tencor Corp.; **Michael L. Rieger**, Synopsys, Inc.; **John L. Sturtevant**, Mentor Graphics Corp.; **Dennis M. Sylvester**, Univ. of Michigan; **Jörg Thiele**, Qimonda AG (Germany)

Wednesday 28 February

SESSION 7

Room: Conv. Ctr. A2 Wed. 6:20 to 8:00 pm

Joint Session with conference 6520: Computational Lithography

Chairs: **Alfred K. K. Wong**, Magma Design Automation; **Donis G. Flagello**, ASML US, Inc.

6:20 pm: **Model-based assist feature generation**, A. Sezginer, Invarium Inc. [6521-22]

6:40 pm: **Three-dimensional mask effect approximate modeling for sub-50-nm node device OPC**, S. Suh, S. Lee, SAMSUNG Electronics Co., Ltd. (South Korea) [6521-23]

7:00 pm: **Lossless I.C. layout compression: intra-cell, inter-cell sub-cell detection**, A. X. Gu, A. Zakhor, Univ. of California/Berkeley . [6520-43]

7:20 pm: **Advances in compute hardware platforms for computational lithography**, T. A. Kingsley, Mentor Graphics Corp. [6520-44]

7:40 pm: **SEM image contouring for OPC model calibration and verification**, C. E. Tabery, Advanced Micro Devices, Inc.; H. Morokuma, R. Matsuoka, Hitachi High-Technologies Corp. (Japan); L. R. Page, High-Technologies America, Inc.; G. E. Bailey, I. Kusnadi, T. Do, Mentor Graphics Corp. [6520-167]

Thursday 1 March

Opening Remarks

Room: Conv. Ctr. C1 Thurs. 8:30 to 8:40 am

Chair: **Alfred K. K. Wong**, Magma Design Automation

SESSION 1

Room: Conv. Ctr. C1 Thurs. 8:40 to 10:00 am

Keynote Presentation

Chair: **Alfred K. K. Wong**, Magma Design Automation

Keynote Presentation
8:40 am: **Collaborative platform for DFM (Invited Paper)**, A. R. Neureuther, Univ. of California/Berkeley [6521-01]

Keynote Presentation
9:20 am: **DFM for the common platform (Invited Paper)**, W. Ng, Chartered Semiconductor Manufacturing, Inc. [6521-02]

Coffee Break 10:00 to 10:30 am

SESSION 2

Room: Conv. Ctr. C1 Thurs. 10:30 am to 12:10 pm

Layout Verification

Chairs: **Hiroichi Kawahira**, Sony Corp. (Japan); **Michael L. Rieger**, Synopsys, Inc.

10:30 am: **Lithography simulation in DfM: achievable accuracy versus requirements**, S. M. Mansfield, G. Han, I. C. Graur, L. W. Liebmann, J. E. Meiring, IBM Microelectronics Div. [6521-03]

10:50 am: **Structural failure prediction using simplified lithography simulation models**, P. Niedermaier, T. C. Roessler, Qimonda AG (Germany) [6521-05]

11:10 am: **Unified process aware system for circuit layout verification**, A. Torres, F. G. Pikus, Mentor Graphics Corp. [6521-06]

11:30 am: **Double patterning design split implementation and validation for the 32-nm node**, M. Drapeau, Synopsys, Inc. (Canada); E. Hendrickx, IMEC (Belgium); A. M. Biswas, J. Li, Synopsys, Inc.; V. Wiaux, S. Verhaegen, IMEC (Belgium) [6521-07]

11:50 am: **DRC Plus: augmenting standard DRC with pattern matching on 2D geometries**, V. Dai, J. Yang, L. Capodiceci, N. P. Rodriguez, Advanced Micro Devices, Inc. [6521-08]

Lunch Break 12:10 am to 2:00 pm

SESSION 3

Room: Conv. Ctr. C1 Thurs. 2:00 to 3:20 pm

Layout Optimization

Chairs: **J'rg Thiele**, Qimonda AG (Germany); **John L. Sturtevant**, Mentor Graphics Corp.

2:00 pm: **Process window aware layout optimization using hot spot fixing system**, S. Kobayashi, S. Kyoh, T. Kotani, S. Inoue, Toshiba Corp. (Japan) [6521-09]

2:20 pm: **Automated full-chip hotspot detection and removal flow for interconnect layers of cell-based designs**, E. Roseboom, ATI Technologies Systems Corp.; F. Chang, P. Hurat, Clear Shape Technologies, Inc.; M. Rossman, Cadence Design Systems, Inc. [6521-10]

2:40 pm: **Model-assisted routing for improved lithography robustness**, A. K. K. Wong, Magma Design Automation [6521-11]

3:00 pm: **Model-based approach for physical design verification and design/manufacturability co-optimization**, D. Pery, Qualcomm, Inc.; P. Hurat, Clear Shape Technologies, Inc.; R. Radojicic, M. Nakamoto, Qualcomm, Inc.; F. Chang, Clear Shape Technologies, Inc.; W. J. Poppe, Univ. of California/Berkeley [6521-12]

Coffee Break 3:20 to 3:50 pm

SESSION 4

Room: Conv. Ctr. C1 Thurs. 3:50 to 5:30 pm

Process-aware Timing and Power Analysis

Chairs: Lars W. Liebmann, IBM Microelectronics Div.; Dennis M. Sylvester, Univ. of Michigan

3:50 pm: **Context specific leakage and delay analysis of a 65-nm standard cell library for lithography induced variability**, C. Wang, United Microelectronics Corp. (Taiwan); D. Tsien, United Microelectronics Corp.; N. Verghese, Y. Ran, P. Hurat, Clear Shape Technologies, Inc.; W. J. Poppe, Univ. of California/Berkeley [6521-13]

4:10 pm: **Patterning effect and correlated electrical model of post-OPC MOSFET devices**, Y. Cheng, C. Lai, R. Liu, M. Wu, I. Shih, C. Chang, W. Liu, C. Chang, S. Tsai, H. T. Lin, Y. Ku, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan) [6521-14]

4:30 pm: **Coupling aware mixed dummy metal insertion for lithography**, L. Deng, M. D. F. Wong, Univ. of Illinois at Urbana-Champaign; K. Chao, Intel Corp.; H. Xiang, IBM Thomas J. Watson Research Ctr. [6521-15]

4:50 pm: **Prediction of interconnect delay variations using pattern matching**, E. Chin, J. A. Holwill, A. R. Neureuther, Univ. of California/Berkeley [6521-16]

5:10 pm: **OPC to reduce variability of transistor properties**, K. Koike, K. Nakayama, K. Ogawa, H. Ohnuma, Sony Corp. (Japan) [6521-17]

Panel Discussion

Convention Center C1 Thurs. 7:30 to 9:00 pm

Design for Manufacturability: Open Mic Night

Moderator: Juan Antonio Carballo, IBM Corp.

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✓ Posters-Thursday

Room: Convention Ctr. Hall 3 Thurs. 5:30 to 8:00 pm

Chair: Mark E. Mason, Texas Instruments Inc.

The following posters will be displayed all day Thursday. Authors will be present during the formal poster session Thursday evening between 5:30 and 8:00 pm for discussion. Authors may set-up their posters after 9:00 am on Thursday.

✓ **Litho-aware method for circuit power analysis through process**, R. S. Fathy, M. Al-Imam, H. Diab, M. M. Fakhry, Mentor Graphics Corp. (Egypt); A. Torres, B. Graupp, J. Brunet, Mentor Graphics Corp.; M. S. Bahnas, Mentor Graphics Corp. (Egypt) [6521-24]

✓ **Circuit size optimization with multiple sources of variation and position-dependant correlation**, Q. Y. Tang, P. D. Friedberg, C. Cheng, C. J. Spanos, Univ. of California/Berkeley [6521-25]

✓ **Multidimensional physical design optimization for systematic and parametric yield loss reduction**, L. N. Karklin, A. Arkhipov, Y. G. Belenky, D. Lay, V. Manuylov, Sagantec North America; B. W. Watson, J. P. F. Willekens, Sagantec Netherlands (Netherlands) [6521-26]

✓ **Highly accurate model-based verification using SEM image calibration method**, B. Cho, D. Park, D. Chang, J. Choi, C. Kim, D. Yim, Hynix Semiconductor Inc. (South Korea) [6521-27]

✓ **The study for increasing efficiency of OPC verification by reducing false errors from bending pattern by using different size of error nonchecking area with various corner lengths**, S. Lee, Y. Lee, K. Kim, DongbuAnam Semiconductor Inc. (South Korea) [6521-28]

✓ **DFM flow by using combination between design based metrology system and model-based verification at sub-50-nm memory device**, C. Kim, J. Kim, J. Choi, H. Yang, D. Yim, J. Kim, Hynix Semiconductor Inc. (South Korea) [6521-29]

✓ **Application of enhanced dynamic fragmentation to minimize false error from post OPC verification**, J. Kang, S. Lee, Y. Lee, K. Kim, DongbuAnam Semiconductor Inc. (South Korea) [6521-30]

✓ **Pattern decomposition for double patterning from photomask viewpoint**, N. Toyama, T. Adachi, Y. Inazuki, T. Sutou, Y. Morikawa, H. Mohri, N. Hayashi, Dai Nippon Printing, Co., Ltd. (Japan) [6521-31]

✓ **A methodology to analyze impacts of proximity effects and layout topologies on circuit performances**, M. You, P. C. W. Ng, Y. Su, K. Tsai, Y. Lu, National Taiwan Univ. (Taiwan) [6521-32]

✓ **Manufacturing for design (MFD) in practice: improving OPC convergence considering design intent**, Y. Su, P. C. W. Ng, K. Tsai, National Taiwan Univ. (Taiwan) [6521-33]

✓ **Lithography enhanced manufacturability analysis by using multilevel simulated contours**, B. Seo, J. Park, W. Choi, S. Woo, S. Lee, SAMSUNG Electronics Co., Ltd. (South Korea) [6521-34]

✓ **Characteristics aware OPC modeling and correction**, J. K. Tyminski, Nikon Precision Inc.; L. Depre, Synopsys, Inc. (France); P. J. M. VanAdrichem, Q. Zhang, Synopsys, Inc. [6521-35]

✓ **Design CD pattern recognition for metrology recipe automation**, Y. Cui, K. Baik, M. Tavassoli, Intel Corp. [6521-36]

✓ **Wire sizing/spacing for lithographic printability optimization**, K. Cao, J. Hu, Texas A&M Univ. [6521-37]

✓ **A rigorous method to determine printability of a target layout**, B. Yenikaya, A. Sezginer, W. Staud, Invarium Inc. [6521-38]

✓ **Computational complexity of image calculation and OPC at the 32-nm node**, B. Yenikaya, A. Sezginer, F. X. Zach, W. Staud, Invarium Inc. [6521-39]

✓ **Novel technique to separate systematic and random defects during 65-nm and 45-nm process R&D stage**, J. Yeh, United Microelectronics Corp. (Taiwan); A. Park, KLA-Tencor Corp. [6521-40]

✓ **Intelligent fill pattern and extraction methodology for sensitive RF/analog or SoC products**, A. P. Balasinski, J. Cetin, A. Kahng, Cypress Semiconductor Corp. [6521-41]

✓ **Scanner parameter sensitivity analysis for OPE**, T. Matsuyama, T. Nakashima, T. Fujiwara, Y. Ishii, Nikon Corp. (Japan) [6521-42]

✓ **OPC and design verification for DFM**, J. Kim, H. Yang, J. Song, D. Yim, J. Kim, Hynix Semiconductor Inc. (South Korea); T. Hasebe, M. Yamamoto, NanoGeometry Research Inc. (Japan) [6521-44]

✓ **Self-assembled dummy patterns for lithography process margin enhancement**, J. Moon, B. S. Nam, J. H. Jeong, B. M. Nam, D. Yim, Hynix Semiconductor Inc. (South Korea) [6521-45]

✓ **Modeling micron-scale gate length variation and spatial correlation**, P. D. Friedberg, G. H. Cheng, Q. Y. Tang, C. J. Spanos, Univ. of California/Berkeley [6521-46]

✓ **Implementation of a design manufacturing interface for 65 nm and beyond**, L. Le Cam, P. Simon, R. Goncalves, P. Le Maitre, Philips Semiconductors (France); R. Boone, Freescale Semiconductors, Inc. (France); F. Parmentier, STMicroelectronics (France); D. de Vries, Philips Semiconductors (France); J. Marin, F. Vautrin, STMicroelectronics (France); Y. Trouiller, Lab. d'Electronique de Technologie de l'Information (France) [6521-47]

✓ **Novel method for quality assurance of two-dimensional pattern fidelity**, S. Maeda, R. Ogawa, Toshiba Corp. (Japan); S. Shibazaki, Toshiba Microelectronics Corp. (Japan); T. Nakajima, Toshiba Information Systems Japan Corp. (Japan) [6521-48]

✓ **A systematic approach for capturing interconnects hot spots**, T. H. Wu, C. W. Huang, United Microelectronics Corp. (Taiwan) ... [6521-49]

- ✓ **Ensuring production-worthy OPC recipes using large test structure arrays**, C. M. Cork, Synopsys, Inc. (France)[6521-50]
- ✓ **Intelligent visualization of lithography violations for 45-nm and beyond**, D. H. Ziger, Synopsys, Inc.[6521-51]
- ✓ **Production-worthy OPC verification methods for protecting against process variability**, J. A. Bruce, IBM Corp.; N. S. Chen, Advanced Micro Devices Inc.; V. Chinta, R. E. De La Cruz, Y. Lin, IBM Corp.[6521-52]
- ✓ **New dimensions of control for optical proximity correction**, J. C. Word, J. L. Sturtevant, N. Cobb, T. M. Donnelly, D. Dudau, L. Hong, P. J. LaCour, Mentor Graphics Corp.[6521-53]
- ✓ **SOFT: smooth OPC fixing technique for ECO process**, H. Zhang, Y. Zhang, Z. Shi, X. Yan, Zhejiang Univ. (China)[6521-54]
- ✓ **Extrapolation and portability of physically based photoresist models**, J. J. Biafore, M. D. Smith, S. Robertson, KLA-Tencor Corp.[6521-55]
- ✓ **Feedback flow to improve model-based OPC calibration test patterns**, W. A. Tawfic, M. Al-Imam, Mentor Graphics Corp. (Egypt); G. E. Bailey, I. Kusnadi, K. Madkour, Mentor Graphics Corp.[6521-56]
- ✓ **Double pattern EDA solutions for 32-nm HP and beyond**, G. E. Bailey, A. V. Tritchkov, J. Park, L. Hong, Mentor Graphics Corp.; V. Wiaux, E. Hendrickx, S. Verhaegen, IMEC (Belgium); P. Xie, Rochester Institute of Technology[6521-57]
- ✓ **Optimizing gate layer OPC correction and SRAF placement for maximum design manufacturability**, J. L. Sturtevant, T. Brist, L. Hong, S. Shang, Mentor Graphics Corp.[6521-58]
- ✓ **Assist features for modeling three-dimensional mask effects in optical proximity correction**, Q. Yan, Z. Deng, J. P. Shiely, L. S. Melvin III, Synopsys, Inc.[6521-61]
- ✓ **Circuit-based SEM contour OPC model calibration**, J. E. Vasek, C. Yuan, K. Patterson, Freescale Semiconductor, Inc.; G. E. Bailey, I. Kusnadi, J. L. Sturtevant, Mentor Graphics Corp.[6521-62]
- ✓ **Boundary based cellwise OPC for standard-cell layouts**, D. M. Pawlowski, L. Deng, M. D. F. Wong, Univ. of Illinois at Urbana-Champaign[6521-63]
- ✓ **Statistical analysis of gate CD variation for yield optimization**, J. A. Holwill, Univ. of California/Berkeley; J. Kye, Y. Zou, Advanced Micro Devices, Inc.[6521-64]
- ✓ **Minimizing poly end-cap pull back by application of DFM and advanced etch approaches for 65nm and 45nm technologies**, K. A. Romero, G. Grasshoff, S. Roling, R. Callahan, AMD Saxony Manufacturing GmbH (Germany); J. Shannon, S. N. McGowan, Advanced Micro Devices, Inc.; A. Nomura, AMD Saxony Manufacturing GmbH (Germany); C. E. Tabery, Advanced Micro Devices, Inc.; R. Stephan, AMD Saxony Manufacturing GmbH (Germany)[6521-65]
- ✓ **Real-time VT5 model coverage calculations during OPC simulations**, I. C. Graur, S. M. Mansfield, IBM Microelectronics Div.; M. Gheith, M. Al Imam, Mentor Graphics Corp. (Egypt)[6521-66]
- ✓ **A simple and practical approach for building lithography simulation models using a limited set of CD data and SEM pictures**, J. Ho, Y. Wang, Xilinx, Inc.; B. Lin, S. Hsu, Y. Gong, United Microelectronics Corp. (Taiwan); K. Wu, Anchor Semiconductor Inc.[6521-67]
- ✓ **Accelerating physical verification using STPRL: a novel language for test pattern generation**, A. Nouh, Mentor Graphics Corp. (Egypt)[6521-68]
- ✓ **DRC and mask-friendly aberration and polarization monitors**, J. A. Holwill, A. R. Neureuther, Univ. of California/Berkeley[6521-69]
- ✓ **Mask manufacturing rules checking (MRC) as a DFM strategy**, P. D. Buck, R. Gladhill, Toppan Photomasks, Inc.; J. Straub, Toppan Photomasks, Inc.[6521-70]
- ✓ **DFM approach to APSM 2nd-level mask patterning**, S. E. Henrichs, M. Chandramouli, Intel Corp.; M. Tsai, Synopsys, Inc.[6521-72]
- ✓ **Cell-based aerial image analysis of design styles for 45-nanometer generation logic**, M. C. Smayling, M. Duane, Applied Materials, Inc.; V. Axelrad, Sequoia Design Systems, Inc.[6521-73]

Friday 2 March

SESSION 5

Room: Conv. Ctr. C1 Fri. 8:30 to 10:10 am

DFM Efficiency

Chairs: **Kevin M. Monahan**, KLA-Tencor Corp.; **Vivek K. Singh**, Intel Corp.

8:30 am: **Improving the power performance of multicore processors through optimization of lithography** (*Invited Paper*), A. H. Gabor, IBM Microelectronics Div.[6521-18]

9:00 am: **Cost-performance tradeoff between design and manufacturing: DfM or MfD?** (*Invited Paper*), A. P. Balasinski, J. Cetin, Cypress Semiconductor Corp.; L. N. Karklin, Sagantec North America[6521-19]

9:30 am: **Hardware verification of litho-friendly design (LfD) methodologies**, R. März, K. Peter, S. Gröndahl, K. Keiner, Infineon Technologies AG (Germany); B. Choi, S. Quek, A. Khoh, N. S. Chen, S. M. Goh, Chartered Semiconductor Manufacturing Ltd. (Singapore) .[6521-20]

9:50 am: **Lithography and yield sensitivity analysis of SRAM scaling for the 32-nm node**, A. Nackaerts, IMEC (Belgium) and ASML (Netherlands); S. Verhaegen, IMEC (Belgium); M. V. Dusa, H. Kattouw, F. van Bilsen, ASML Netherlands B.V. (Netherlands); S. Biesemans, G. Vandenbergh, IMEC (Belgium)[6521-21]

Courses of Related Interest

Register for courses at the SPIE registration desk.

SC105 CD Metrology and Image Formation in the Scanning Electron Microscope (SEM) (Wells, Postek) Sunday 8:30 am to 5:30 pm

SC116 Lithographic Optimization: A Theoretical Approach (Mack) Sunday 8:30 am to 5:30 pm

SC505 Data to Silicon: Understanding the Fundamentals of MDP, Frame Generation, RET and DFM (Morse) Monday 8:30 am to 5:30 pm

SC540 Applying Optical Proximity Correction and Design for Manufacturability to Product Designs (Capodiceci, Lucas) Sunday 8:30 am to 5:30 pm

SC705 Instruments and Methodologies for Accurate Metrology and Fleet Matching (Archie, Banke) Sunday 8:30 am to 5:30 pm

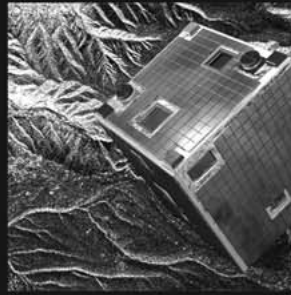
SC708 Impact Of Variability On VLSI Circuits (Puri, Gupta) Tuesday 1:30 to 5:30 pm

SC778 Introduction to Advanced Process Control (APC) for Semiconductor Manufacturing (Misra) Sunday 8:30 am to 5:30 pm

SC832 IP Issues in Advanced Lithography and Semiconductor Manufacturing (Gortych) Monday 1:30 to 5:30 pm

SC833 Lithography Integration for Semiconductor Back-End-Of-The-Line (BEOL) (Lin) Sunday 8:30 am to 12:30 pm

SC834 Lithography Friendly Design and Beyond - A Broader Review of DfM (Liebmann, Mansfield, Wong) Tuesday 8:30 am to 5:30 pm



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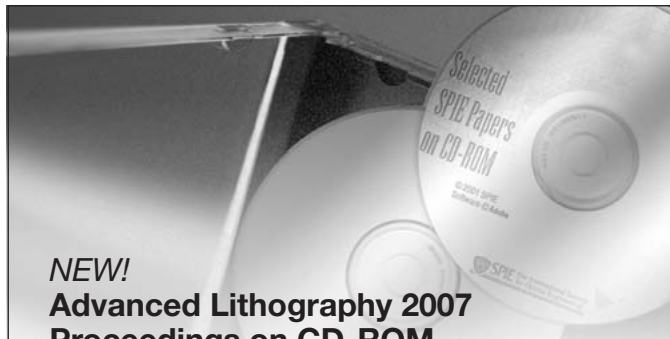
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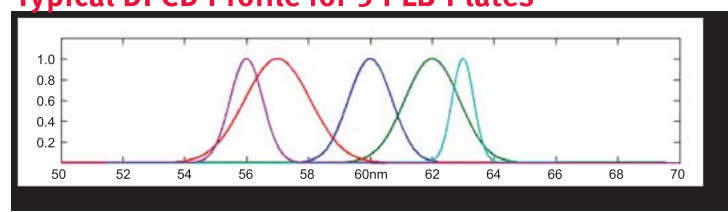


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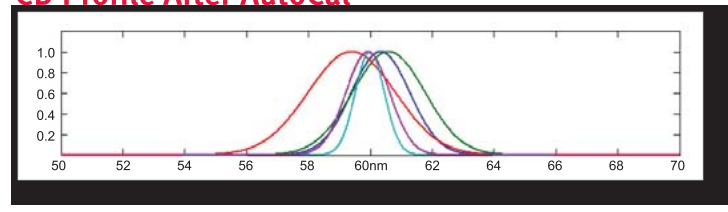
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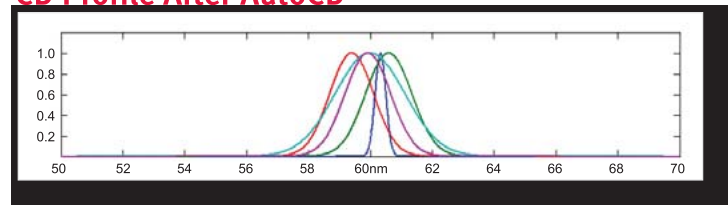
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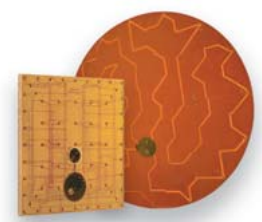
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