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# Conference 9776: Extreme Ultraviolet (EUV) Lithography VII

Monday - Thursday 22–25 February 2016

Part of Proceedings of SPIE Vol. 9776 Extreme Ultraviolet (EUV) Lithography VII

9776-1, Session 1

## EUV Progress Toward HVM Readiness *(Keynote Presentation)*

Britt Turkot, Intel Corp. (United States)

No Abstract Available

9776-2, Session 1

## EUV Lithography: Progress and Perspective *(Keynote Presentation)*

Seong-Sue Kim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

No Abstract Available

9776-3, Session 2

## Recent progress in nanoparticle photoresists development for EUV lithography

Kazuki Kasahara, JSR Corp. (Japan) and Cornell Univ. (United States); Vasiliki Kosma, Jeremy Odent, Hong Xu, Mufei Yu, Emmanuel P. Giannelis, Christopher K. Ober, Cornell Univ. (United States)

Extreme ultraviolet (EUV) lithography is a promising candidate for next generation lithography. For high volume manufacturing of semiconductor devices, significant improvement of resolution and sensitivity is required for EUV resists. The performance requirement for EUV resists requires the development of entirely new resist platforms. Cornell University has intensively studied metal oxide nanoparticle photoresists with high sensitivity for EUV lithography applications. Zirconium oxide nanoparticles with PAG enabling sub 30nm line negative tone patterns at an EUV dose below 5 mJ/cm2, show one of the best EUV sensitivity results ever reported. In this paper, recent progress in metal oxide nanoparticle resists will be discussed. Several studies regarding new metal elements, composition investigation and new ligand design are included.

Regarding the new metal core study, new metal elements will be applied to nanoparticle resists in terms of high EUV absorbance for higher sensitivity. The result of exposure experiments of this new metal nanoparticle will be discussed.

A composition study of nanoparticle resists is critical for improvement of litho performance. A key step in our nanoparticle photoresist patterning process is the exposure of a photoligand generator (PLG), typically a photoacid generator. We will discuss the lithographic performance dependence on the various PLG structures.

The new ligand designs are also important for enhancing solubility contrast. While the nanoparticle photoresists show excellent sensitivity to date, the contrast appears to be limited. New ligands with higher solubility contrast are investigated and the effect on litho performance will be discussed.

9776-4, Session 2

## Novel ultra-high sensitive ‘metal resist’ for EUV lithography

Toru Fujimori, Toru Tsuchihashi, Shinya Minegishi, Takashi Kamizono, Toshiro Itani, EUVL Infrastructure Development Ctr., Inc. (Japan)

Extreme ultraviolet (EUV) lithography is considered to be the most effective strategy for realize sub-10 nm manufacturing and beyond. A key factor for the realization of EUV lithography is the choice of EUV resist material that is capable of resolving below 20-nm half pitch with high sensitivity. Recently, some researchers have reported concerns on the limitations in the performance of positive-tone chemically amplified resist (CAR). Consequently, there is a critical need for new chemistry and development of new resist materials.

To the breakthrough of the performance of EUV resist materials, non-CAR materials have been studied by many research groups for latest these years. Especially, the metal containing resist materials were received a lot of attention, which had high sensitivity performance. It will be very helpful for cover the low energy power source to realize EUV lithography.

This paper describes novel ultra-high-sensitive ‘metal resist’ for EUV lithography. Herein, the developments of ‘metal resist’ have been studied for improvement of sensitivity using ‘metal containing non-CAR materials’ called EIDEC standard metal EUV resist (ESMR). The results of novel ‘metal resist’ indicate ultra-high sensitivity using EB lithography will be shown. In SPIE 2015, we presented the 1st original ESMR, which was observed 17 nm line with 1.5 mJ/cm2: equivalent in EUV lithography (Fig. 1). The core structure and the resist formulations were studied and confirmed the sensitivity and LWR improvement (Fig. 2). Also, the properties of ESMR were studied, like resist solution stability, PCD (post coated delay) stability and PED (post exposure delay). Furthermore, we confirmed the 20 nm lithographic pattern with high sensitivity with EUV exposure tools (Fig. 3). In addition, the latest EUV exposure results will be presented in the presentation.

9776-5, Session 2

## Novel metal containing resists for EUV lithography extendibility

Danilo De Simone, IMEC (Belgium); Safak Sayan, Intel Corp. (Belgium); Satoshi Dei, JSR Micro N.V. (Belgium); Ivan Pollentier, IMEC (Belgium); Yuhei Kuwahara, Tokyo Electron Kyushu Ltd. (Netherlands); Geert Vandenberghe, IMEC (Belgium); Kathleen Nafus, Tokyo Electron Europe Ltd. (Netherlands); Motohiro Shiratani, JSR Engineering Co., Ltd. (Japan); Hisashi Nakagawa, Takehiko Naruoka, JSR Corp. (Japan)

Strong interest has recently developed among the researchers in the use of metals in extreme ultraviolet (EUV) lithography photoresists [1, 2] aiming to simultaneously achieve the resolution, line-width roughness and sensitivity (RLS) requirements for 10nm technology node and below and have the highest productivity with low exposure dose requirements (below 20mJ/cm2). In this paper two different metal containing resists (MCR) are discussed: the first one by introducing metal species (the sensitizer) into a conventional chemically amplified EUV photoresist to increase the optical density and have a greater number of absorbed EUV photons with respect to the purely organic resist and thus increase its sensitivity. The second one by using metal oxide nanoparticles (MONP) resist as alternative non

chemically amplified EUV photoresist.

The initial work is discussed from a manufacturing compatibility prospective, as metal cross-contamination and outgassing, to an imaging prospective, through the patterning on NXE:3300 full field scanner exposure tool, looking at RLS material performances. Particular emphasis is put on the material stability of MONPs looking at the aging of different formulations through EUV exposures. Imaging results at different process conditions are also reported and discussed.

9776-6, Session 3

## Challenge toward breakage of RLS trade-off by new resists and processes for EUV lithography *(Invited Paper)*

Seiji Nagahara, Tokyo Electron Ltd. (Japan); Michael A. Carcasi, Tokyo Electron America, Inc. (United States); Gosuke Shiraishi, Yuichi Terashita, Yukie Minekawa, Kosuke Yoshihara, Masaru Tomono, Hironori Mizoguchi, Tokyo Electron Kyushu Ltd. (Japan); Hideo Nakashima, Tokyo Electron Ltd. (Japan); Seiichi Tagawa, Akihiro Oshima, Osaka Univ. (Japan); Hisashi Nakagawa, Takehiko Naruoka, Tomoki Nagai, JSR Corp. (Japan); Elizabeth Buitrago, Michaela Vockenhuber, Yasin Ekinci, Paul Scherrer Institut (Switzerland); Oktay Yildirim, Marieke Meeuwissen, Coen Verspaget, Rik Hoefnagels, Gijsbert Rispens, Raymond Maas, ASML Netherlands B.V. (Netherlands)

For the insertion of EUV lithography into device mass production, higher sensitivity of EUV resists is helpful for better cost of ownership of EUV tool and light source. However, it is very hard to get better sensitivity, high resolution, and low line edge roughness simultaneously. The previous experiments by lithographers proved the existence of this Resolution, Line edge roughness, and Sensitivity (RLS) trade-off. This paper tries to propose a solution to break the RLS trade-off relationship by introducing new type of chemically amplified resists and new processes which can be done in an in-line track tool connected to EUV exposure tool. In this paper, we will discuss the reaction mechanisms and simulation models of the new resist system. The new simulator will predict the capability of the new resists and processes. Next, we will show exposure results of the new resist processes. Finally, the lithography performance with improved resist sensitivity will be discussed using the exposure results.

9776-8, Session 3

## Negative-tone imaging with EUV exposure toward 13nm hp

Hideaki Tsubaki, Wataru Nihashi, Toru Tsuchihashi, Kei Yamamoto, Takahiro Goto, FUJIFILM Corp. (Japan)

Negative-tone imaging (NTI) with EUV exposure has major advantages with respect to line-width roughness (LWR) and resolution due in part to polymer swelling and favorable dissolution mechanics. In NTI process, resist, organic solvent, and other alternative technology play important roles in determining lithography performances. The present study describes novel chemically amplified resist materials based on NTI technology for 13 nm hp and beyond.

This study has shown the fundamental advantage of NTI process with respect to fine pattern formation for 1x nm hp. It is well known that bridge and collapse limit resolution below 20 nm hp, indicating that swelling is one of major causes for preventing tight pitch resolution. Collapse and bridge mitigation technologies based on EUV-NTI were investigated in this study. First, we further manipulated solubility parameter of organic solvents to get optimal dissolution character for current EUV resist. We investigated effects of solubility parameter of organic solvents on resolution below 20 nm hp. According to the solubility parameter ?p and ?d of solvents and EUV resist, new candidates were found only for rinse materials. Lithographic data of the new rinse solvents showed better collapse performance than FN-RP311 which is our standard rinse material for EUV-NTI. Ultimate resolution data of this new NTI process will be described in this paper. Additionally, we explored benefits of ACCEL (Advanced Chemical Contrast Enhancement Layer) for tight pitch resolution in EUV lithography. The other new technologies to have positive impacts on bridge and collapse performances will be also described in this paper.

Fundamental advantage of NTI process to utilize it for dark mask application is described with a detailed CD-SEM data of dot and block mask features under exposures with an E-beam and EUV light. It is emphasized that clearly better dot resolution was obtained without any collapse and peeling when using NTI process. Detailed performance benefits using NTI process will be also described in this paper.

9776-9, Session 3

## Approach to hp-10nm resolution by applying dry development rinse materials (DDRP) and materials (DDRM)

Wataru Shibayama, Shuhei Shigaki, Satoshi Takeda, Ryuji Onishi, Makoto Nakajima, Rikimaru Sakamoto, Nissan Chemical Industries, Ltd. (Japan)

EUV lithography has been desired as the leading technology for single nm half-pitch patterning. However, the source power, masks and resist materials still have critical issues for mass production. Especially in resist materials, RLS trade-off is the key issue. To overcome these issues, we are suggesting Dry development rinse process (DDRP) & materials (DDRM) as the pattern collapse mitigation approach. This DDRM can perform not only as pattern collapse free materials for fine pitch, but also as the etching hard mask against bottom layer (spin on carbon : SOC). In this paper, we especially propose new approaches to achieve high resolution around hp10nm. The key points of our concepts are 100% water solvent system and PR smoothing. This new DDR technology can be the promising approach for hp10nm level patterning in N7/N5 and beyond.

9776-10, Session 4

## EUV lithography performance for manufacturing: status and outlook *(Invited Paper)*

Alberto Pirati, Rudy Peeters, Daniel A. Smith, Sjoerd Lok, Martijn van Noordenburg, Roderik van Es, Eric Verhoeven, Henk Meijer, Arthur W. E. Minnaert, Jan-Willem van der Horst, Hans Meiling, Jörg Mallmann, Christian Wagner, Judon Stoeldraijer, Geert Fisser, Leon Levasier, Jo Finders, Carmen Zoldesi, Uwe Stamm, Herman Boom, David C. Brandt, Daniel J. Brown, Igor V. Fomenkov, ASML Netherlands B.V. (Netherlands)

NXE:3300B systems have been operational at customer sites for almost two years, and the NXE:3350 systems, the 4th generation EUV systems. All ASML EUV systems now operate using MOPA Pre-pulse EUV source technology, which enabled significant productivity scaling at customers.

Having achieved the required power level to support device development, the priority of ASML EUV program has been in improving stability and availability; this paper will cover the status and outlook for availability and productivity performance.

Overlay and Imaging results are in line with the requirements of 7nm logic devices have been demonstrated; Matched Machine overlay to ArF immersion below 2.5 nm and full wafer CDU performance of less than 1.0nm are regularly achieved.

Progresses in defectivity reduction and in the realization of a reticle pellicle will be reviewed.

This paper will present an overview of the current EUV performance and of the on-going developments in productivity, imaging, overlay and mask defectivity reduction as well as the future roadmap.

9776-11, Session 4

## Demonstration of an N7 integrated fab process for metal oxide EUV photoresist

Danilo De Simone, Ming Mao, Frederic Lazzarino, Geert Vandenberghe, IMEC (Belgium); Michael K. Kocsis, Peter de Schepper, Jason K. Stowers, Stephen T. Meyers, Benjamin L. Clark, Andrew Grenville, Inpria Corp. (United States); Vinh Luong, TEL Technology Ctr., America, LLC (United States); Fumiko Yamashita, Tokyo Electron Miyagi Ltd. (Japan); Doni Parnell, Tokyo Electron Europe Ltd. (United States) and TEL Technology Ctr., America, LLC (United States)

Inpria has developed a directly patternable metal oxide hard-mask as a robust, high-resolution photoresist for EUV lithography. The Inpria Gen2 photoresists are capable of 10nm half-pitch resolution and exhibit very high etch resistance. In this paper we will demonstrate the full integration of the Inpria resist into an IMEC N7 BEOL process module, more specifically in the block layer for metal patterning . We examine in detail both the lithography and etch patterning results. In doing so, we also investigate the respective process windows as well as routes to maximize the process latitude.
By leveraging the high differential etch resistance of Inpria metal oxide photoresists, we explore opportunities for process simplification and cost reduction looking at different integration schemes. We review 2D imaging results from the IMEC N7 block mask patterns, underlayer integration, etch transfer with a variety of chemistries, cross sections, track integration, and selective resist strip. Finally, concerns about process equipment metal cross contamination are also addressed.

9776-12, Session 4

## EUV process establishment through litho and etch for N7 node

Yuhei Kuwahara, Tokyo Electron Kyushu Ltd. (Belgium); Philippe Foubert, Ming Mao, IMEC (Belgium); Nihar Mohanty, TEL Technology Ctr., America, LLC (United States); Anne-Marie Goethals, IMEC (Belgium); Kathleen Nafus, Koichi Matsunaga, Shinichiro Kawakami, Tokyo Electron Kyushu Ltd. (Japan); Eric Hendrickx, IMEC (Belgium)

Extreme ultraviolet lithography (EUVL) technology is steadily reaching high volume manufacturing for 16nm half pitch node and beyond. In addition to scanner availability, further improvement of resist performance (smoother LER, finer resolution and so on) is required.

Advance EUV patterning on the ASML NXE:3300/ CLEAN TRACKTM LITHIUS ProTM Z- EUV litho cluster is launched at imec, allowing for finer pitch patterns for L/S and CH. Tokyo Electron Limited (TELTM) and imec are continuously collaborating to develop manufacturing quality POR processes for NXE:3300. TELTM's technologies to enhance CD uniformity, defectivity and LWR/LER can improve patterning performance. The patterning is characterized and optimized in both litho and etch for a more complete understanding standing of the final patterning performance.

In this study, we establish POR with NXE:3300 by using TEL's best known method for patterning performance and defectivity through litho and etch. In addition, etch curing process optimization to obtain smoother LWR/LER is reported.

9776-13, Session 4

## Comparison of EUV and 193i based patterning for advanced node integration

Christopher Wilson, IMEC (Belgium)

The requirements of advanced CMOS scaling puts a high demand on lithography resolution and patterning techniques. Innovation in the industry has enabled scaling to N10 and N7 dimensions, but this has come at the cost of flow complexity and tighter uniformity and overlay specs. EUV insertion is therefore inevitable, yet comes with its own complexities. In this work we compare the pattering integrity results of product like structures using EUV single pattering and different 193i lithography pattering techniques to study the tradeoff between the two and make recommendations for EUV insertion. Both metal trench and via flows are evaluated.

EUV offers the possibility of single print for advanced nodes. We used the ASML NXE 3300 to fabricate N10 product like wafers with both trench and via patterns. During this development we encountered hard mask selectivity constraints impacting pattering integrity and wafer uniformity and used resist curing and hard mask material optimization to address these issues. We also developed and tested 193i lithography based flows using multiple litho etch (LE) and doubling pattering (SADP+Keep) to reach sub resolution pitch. These both add additional films and steps in the pattering process representing approximately a 3x and 2x increase the process number of steps for the two techniques respectively compared to EUV.

The EUV single print flow showed better CDU but slightly worse LWR when compared to the 193i lithography based flows. In either case CDU and LWR can lead to open or bridging. Overlay, litho-etch bias uniformity and line end pull back were key issues to solve in developing these 193i lithography based flows. Greater corner rounding was observed in both the litho etch and litho-etch and double pattering flows when compared to the EUV single print flow. This resulted in clearly better patterning fidelity in the EUV single print flow compared to the 193i lithography based solutions.

To enable better comparison we developed image processing techniques to compare full wafer maps of 2D logic patterns. Using this methodology we could extract variability bands of real device structures and identify critical points in the pattering causing shorts or opens. A number of factors impacting the ultimate electrical integration were identified. These include proximity effects, corner rounding, necking/narrowing and line end pullback. Such factors can increase or decrease the process window when analyzing via contact area overlay.

9776-14, Session 4

## Improvement of EUV mix-match overlay for production implementation

Byongseog Lee, Sarohan Park, Inwhan Lee, Byoung-Hoon Lee, Chang-Moon Lee, Young-Sik Kim, Noh-Jung Kwak, SK Hynix, Inc. (Korea, Republic of)

The improvement of overlay control in EUV lithography (EUVL) is one of critical issues for successful mass production by using it. Especially it is important to improve the matched machine overlay (MMO) between EUV and ArF immersion tool, because EUV process will be applied to specific layers that have more competitive cost against immersion multiple patterning with the early mass productivity of EUV. Therefore it is necessary to consider the EUV overlay target with comparing the overlay specification of double patterning technology (DPT) and spacer patterning technology (SPT)

In this paper, we will present the EUV MMO performance of NXE3300 with ArF immersion system and compare them with previous NXE3100 results. The overlay stability is investigated through marathon expose test. It is obvious that the 1st wafer effect and wafer to wafer variation observed in NXE3100 are improved. And the further improvement is achieved by apply the higher order CPE (correction per expose), even though available terms are different from those of ArF immersion tool by limitation of EUV optics. We have also studied the major contributors of MMO error by overlay

budget breakdown analysis to find out which areas should be improved in EUV for mass production.

9776-16, Session 5

## 3D mask effects of absorber geometry and chief ray angles in EUV lithography systems

Riaz R. Haque, Zac Levinson, Bruce W. Smith, Rochester Institute of Technology (United States)

Accurate modeling of 3D mask effects has played a critical role in past lithography process development. It has been previously shown through rigorous simulation that the 3D mask geometry in DUV systems introduces azimuthally symmetric phase shifts. This phase effect is typically compared to spherical aberration, which can result in best focus shifts and Bossung tilt. Accurate modeling of these effects becomes even more critical in reflective EUV systems, where the phase effects are different than in transmissive DUV counterparts. The non-zero chief ray angle at the object (CRAO) in EUVL systems introduces azimuthally asymmetric phase shifts. Understanding and characterizing these effects is critical to EUVL system and mask design. In this paper, we will examine the effects of 3D mask absorber geometry, absorber material properties, and CRAO on diffraction efficiencies and phase through rigorous simulation. The diffraction phase distribution will be subsequently split into even and odd components. This methodology enables analogies between the well-known effects of lens aberrations and EUV 3D mask effects. Specifically, this analysis reveals that the odd component of the phase distribution is non-zero in off-axis optical systems. This effect can be seen in Figure 1, where there are both even and odd components to the pupil phase distribution. This odd parity component is analogous to coma, which manifests in off-axis magnification errors and through-focus pattern shift.

9776-17, Session 5

## Etched multilayer type black border formed on EUV mask: Does it cause image degradation during pattern inspection using EB optics?

Tsuyoshi Amano, Susumu Iida, Ryoichi Hirano, EUVL Infrastructure Development Ctr., Inc. (Japan); Tsukasa Abe, Dai Nippon Printing Co., Ltd. (Japan); Hidehiro Watanabe, EUVL Infrastructure Development Ctr., Inc. (Japan)

The inspection technology for patterned mask especially for the Extreme Ultraviolet lithography (EUVL) is always been a center of attention. Because the feature sizes for EUVL is smaller compared with deep ultraviolet (DUV) lithography and such a shrinking of the pattern size induces a lack of the image contrast captured by a pattern inspector that employs DUV optics. To achieve the inspection sensitivity and applicability for 1X nm node EUV mask, inspection technique using electron beam (EB) optics are suggested [1, 2]. By applying the EB optics, the inspector can capture the pattern images with higher resolution compared with the images captured by the DUV optics.

In this presentation, influence of the etched multilayer type black border on the image quality captured by EB optics like a mask pattern inspection technique or a metrology tool is described. To analyze the impact of the black border structure on the EB images, two types of the mask structure was prepared. One was a normal mask structure that is to say the multilayer was coated on the substrate directly. The other was a mask structure with an under layer inserted between the substrate and the multilayer. The role of the under layer is to keep electrical conductivity between the inside and the outside of the black border, and also etching stopper layer during the multilayer etching process. The under layer was made of ruthenium and the thicknesses were changed from 1.5 to 10 nm to investigate the impact of the sheet resistivity on EB images. The defect counts on the multilayer did not change even if the under layer were coated below the multilayer. The sheet resistivity will be measured and the influence of the sheet resistivity on the EB images will be described.

This work was supported by NEDO.

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9776-18, Session 5

## Aerial imaging study of the mask-induced line-edge roughness of EUV lithography mask

Antoine J. Wojdyla, Alexander P. Donoghue, Markus P. Benk, Kenneth A. Goldberg, Lawrence Berkeley National Lab. (United States)

Extreme ultraviolet (EUV) lithography photomasks are based on reflective multilayer mirrors whose intrinsic roughness causes speckle [1] and is responsible for mask-induced line edge roughness (LER) in the aerial image that ultimately gets printed on the wafer. As mask critical dimensions are reduced over time, these effects become more appreciable [2], adversely impacting the LER on the resist. The roughness of the photomask absorber pattern has been studied using scanning electron microscopy (SEM)[3], but such investigations are insensitive to actinic-only effects created in the resonant-reflection of the multilayer.

SHARP [4] is a synchrotron-based, EUV mask-imaging microscope that uses Fresnel zoneplate lenses as high-magnification imaging elements. It features a Fourier synthesis illuminator that provides full control of the illumination coherence and angular spectrum. SHARP records continuous gray-scale aerial images of blank and patterned masks, enabling at-wavelength assessment of aerial image LER and the conditions that affect it.

Building on previous work in this area [5], we have conducted mask-imaging experiments to probe LER measurement limits under varying partial coherence, normalized image log-slopes (NILS), and with varying exposure levels. This work establishes baseline requirements for experimenters to achieve given confidence levels in the measurement of line properties. Photon shot noise forms the dominant contribution to observed line roughness when exposure levels are too low.

Some line properties, such as contrast, CD, and NILS, can be measured well under low light conditions by integrating the measured intensity values in the direction parallel to the lines. However, LER measurements rely on an ensemble of edge positions or line widths detected in each available image row along the lines. For this reason, shot noise affects measurements; a clear understanding of the interdependence of intensity and edge slope are important for successful analysis. The results of this study can be applied to other actinic mask-imaging microscopes, and possibly to measurements made at different wavelengths.

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9776-19, Session 5

## Throughput compensation through optical proximity correction for realization of an extreme-ultraviolet pellicle

Ki-Ho Ko, Hye-Keun Oh, Soo-Yeon Mo, In-Seon Kim, Hanyang Univ. (Korea, Republic of); Ju-Hwan Kim, Mentor Graphics Corp. (United States)

The extreme-ultraviolet lithography (EUVL) is the most prospective technology for high resolution patterning below 1x nm node. However, it is very hard to protect a mask from various contaminations without a pellicle, so that many companies try to develop the pellicle which can be applied to a EUVL equipment. The pellicle for EUVL should be very thin due to strong absorption property of EUV source, and the thickness of under 50 nm has been considered for larger transmission.

A lot of problems of the EUV pellicle were reported recently, such as thermal and mechanical stability, but the transmission loss due to the absorption could be the most critical problem because the EUV source power still not be enough for achieving mass production. The absorption ratio of a pellicle which is composed of 50 nm-thick silicon is about 8 %, and then the total loss is about 16 % for two-pass, so that we need about 16 % more dose to make the same patterning with a pellicle.

Optical proximity correction (OPC) has been widely used to make a high quality pattern for various and complex patterning. OPC was tried to the mask with a EUV pellicle to evaluate whether the transmission loss can be compensated or not.

Figure 1 (a) illustrates a basic layout of 16 nm node mask pattern that we want to make on the wafer and (b) shows corrected layout through a OPC simulation without a EUV pellicle. Figures 1 (c) and (d) are OPCed mask layouts simulated with 90 % single pass transmission pellicle and those with 80 % single pass transmission to make exactly the same pattern without a pellicle, respectively. As one can see, mask patterns are much more downsized in Fig. 1 (d) because it needs more spacious reflected area to be the same patterning at the wafer without a pellicle. Figure 2 (a) shows a difference of two dimensional aerial image contours at the same threshold intensity with or without a pellicle. Blue indicates an aerial image contour of the pellicle-less mask, and it is broader from red (90 % pellicled mask) to green (80 % pellicled mask) and a bridge appears due to the transmission loss caused by the pellicle. Figure 2 (b) shows the aerial image contours of three OPCed mask corresponding to the layouts in Figs. 1 (b), (c) and (d). The contours are almost same even though the high absorption pellicles are used.

We will show the possibilities that transmission loss due to the EUV pellicle can be compensated through proper OPC of a pellicled mask. The more specific values, such as contrast and normalized log slope (NILS) representing the patterning quality of the OPCed mask will be shown in this paper. In addition, the process window that shows exposure latitude (EL) and depth of focus (DOF) should be verified as well to check the actual effect of OPCed mask with a pellicle to the patterning. We can be free from not only the restriction of the thickness, but also the thermal and mechanical problems if a proper OPC to a EUV pellicled mask is applied. In other words, a pellicle of much thicker and other materials with more absorption can be used as a EUV pellicle.

9776-20, Session 6

## Performance of new high-power HVM LPP-EUV source

Hakaru Mizoguchi, Hiroaki Nakarai, Tamotsu Abe, Krzysztof M. Nowak, Yasufumi Kawasuji, Hiroshi Tanaka, Yukio Watanabe, Tsukasa Hori, Takeshi Kodama, Yutaka Shiraishi, Tatsuya Yanagida, Georg Soumagne, Tsuyoshi Yamada, Taku Yamazaki, Takashi Saitou, Gigaphoton Inc. (Japan)

We have reported engineering data from our resent test such around 43W average clean power, CE=2.0%, with 100kHz operation and other data 1). We have already finished preparation of higher average power CO2 laser more than 20kW at output power cooperate with Mitsubishi electric cooperation2). Recently we achieved 140W with 50kHz, 50% duty cycle operation and two hours operation at one hundred watt power range3). Recently we have demonstrated 24 hours operation at 80-50W level operation under power feedback at proto type #2 system.

We are now constructing new high power HVM LPP-EUV source with >25kW CO2 driver laser system made by Mitsubishi Electric. At the conference we will report the performance of the new system and updated data of old systems.

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9776-21, Session 6

## Advancements in predictive plasma formation modeling

David C. Brandt, Michael Purvis, Daniel J. Brown, Igor V. Fomenkov, Alexander Schafgans, Cymer LLC (United States); Harry Kreuwel, Andrei M. Yakunin, ASML Netherlands B.V. (Netherlands); Steve Langer, Howard A. Scott, Lawrence Livermore National Lab. (United States)

We present highlights from plasma simulations performed in collaboration with Lawrence Livermore National Labs and other institutions. This modeling is performed to advance the rate of learning about optimal EUV generation for laser produced plasmas and to provide insights where experimental results are not currently available. The goal is to identify key physical processes necessary for an accurate and predictive model capable of simulating a wide range of conditions. This modeling will help to drive source performance scaling in support of the EUV Lithography roadmap. The model simulates pre-pulse laser interaction with the tin droplet and follows the droplet expansion into the main pulse target zone. Next, the simulated target is transferred into a plasma physics code where the interaction of the expanded droplet with the main laser pulse is simulated. We demonstrate the predictive nature of the code and provide comparison with experimental results.

9776-22, Session 6

## High-radiance LDP source: Clean, reliable, and stable EUV source for mask inspection

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High-throughput actinic mask inspection tools are needed as EUVL begins to enter into volume production phase. One of the key technologies to realize such inspection tools is a high-radiance EUV source of which radiance is supposed to be as high as 100 W/mm2/sr. Ushio is developing laser-assisted discharge-produced plasma (LDP) sources. Ushio’s LDP source is able to provide sufficient radiance as well as cleanliness, stability and reliability. Radiance behind the debris mitigation system was confirmed to be 120 W/mm2/sr at 9 kHz and peak radiance at the plasma can be as

high as 180 W/mm2/sr. One of the unique features of Ushio's LDP source is cleanliness despite liquid tin as fuel material. Source cleanliness was evaluated by placing a Ru mirror sample behind the debris shield. Multiple samples were exposed for at least 100 Mpulse and surface of each sample was analyzed with XRF and SEM. Deposition of tin was negligible and sputter rate of ruthenium was a few nm per Gpulse. Collector lifetime is therefore considered to be sufficiently long. Days-long, non-interrupted runs were also carried out to address system reliability and long-term stability. A prototype machine has been built and tested for product development. Detailed and up-to-date results of the development will be presented at the conference.

9776-23, Session 6

## Study of Sn removal processes for in-situ collector cleaning

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An in-situ hydrogen plasma cleaning technique to clean Sn off of EUV collector optics is studied in detail. The cleaning process uses hydrogen radicals (formed in the hydrogen plasma) to interact with Sn-coated surfaces, forming SnH4 and being pumped away. This technique has been used to clean a 300mm-diameter stainless steel dummy collector optic, and EUV reflectivity of multilayer mirror samples was restored after cleaning Sn from them, validating the potential of this technology.

This method has the potential to significantly reduce downtime and increase source availability. However, Sn removal is governed not just by radical density but also by decomposition of the SnH4 molecule upon impact with the collector and the resulting re-deposition of Sn. This decomposition limitation is present in all cleaning systems that make use of hydrogen radicals, and it must be further understood in order to design effective cleaning systems. Thus, an investigation into the fundamental processes governing Sn removal is being performed. To calculate net removal rate, the redeposition rate must be subtracted from the raw etch rate. The number of hydrogen radicals required to remove a Sn atom from the surface has been experimentally determined, yielding raw etch rates. Experiments are being performed to determine the decomposition probability of SnH4 atoms on a Sn-coated surface. Results from these decomposition experiments are presented. Measurements of etching probability and decomposition probability allow for the formation of a theoretical framework that enables predictions of net Sn removal rates. This framework can be useful for designing and integrating cleaning techniques in production-level EUV sources.

9776-24, Session 6

## Simulation study of impact of collector contamination on imaging quality

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For the miniaturization of IC (integrated circuits), a patterning with small CD(critical dimension) with smaller variation and small overlay is highly required. To exceed the physical limits (NA, ?) for smaller patterning and simplification of the process, a smaller wavelength, EUV(extreme ultra violet, ?=13.5nm) is being introduced. However, EUV also brings up many EUV specific issues. Collector contamination is one of them. This not only decreases productivity, but also lowers imaging quality. Contamination on collector mirror changes source pupil and increases the variation of source pupil across the slit. This induces energy imbalance across the pupil and increase telecentricity error in illumination, and leads to increase of variation in CD and pattern shift across the slit. Due to the design of EUV illuminator, collector contamination randomly attenuates point elements in source pupil, which was not seen in previous ArF system. This makes patterning quality vary with respect to the pitch of given pattern.

This paper presents the impact of collector contamination on patterning. It focuses on pattern shift and CD changes due to source pupil changes from collector contamination. A simulation analysis of pattern shift and CD variation across the slit with respect to collector contamination will be presented. By simulation using through-pitch line and space pattern with sub-20nm CD, sensitivity of pattern pitch in CD and pattern shift will be also studied. From preliminary research, simulation with contaminated collector (reflectivity approx. 60%) shows increase in CD variation up to 1.5x in comparison with lightly contaminated collector (reflectivity approx. 90%). For pattern shift case, simulation with contaminated collector shows that collector contamination can increase up to 2.5x pattern shift. This is evident in isolated pattern and shot edge. Quantitatively, this pattern shift can take more than 10% of overlay budget. This can set collector swap/cleaning criteria because pattern can go out-of-spec at certain level of contamination before collector reaches the productivity limit.

9776-25, Session 7

## Revisiting Li as potential EUV source using dual-laser beam systems

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Further advancement of EUV lithography for future chips manufacture calls for detail analysis of various ways to improve EUV photon sources. Three elements were studied during more than ten years of photon sources development, i.e, Xe, Li, and Sn. Currently small droplets of liquid tin are considered the most promising targets to produce EUV radiation by laser beams. These targets have the main advantage of having relatively higher conversion efficiency (CE) of the produced EUV sources as well as the small mass of the targets allows reducing mirrors contaminate/damage by ionic/atomic debris. The high CE of such targets is provided by using dual-beam lasers irradiation, which allows increasing the CE in 6-7 times in comparison with single pulse of CO2 laser.

Lithium targets were investigated several years ago showing lower CE in comparison with Sn targets. Large amount of debris/splashing produced during laser/target interaction is another disadvantage, which did not favor Li for further consideration for EUV lithography.

We revisited lithium and studied possible ways to increase the CE of the produced source as well as to reduce debris from the developed plasma/vapor. We used dual-beam technique and investigated the influence of pre-pulses and main pulse laser parameters on the source evolution and characteristics, EUV photons emission, and absorption.

We used our comprehensive HEIGHTS package that was benchmarked with experimental studies of laser-produced plasmas from Li target at our CMUXE laboratory. Advanced models for laser photons interaction with lithium droplet/vapor/plasma, target vaporization and ionization, plasma hydrodynamic expansion, thermal conduction and radiation transport, included in the HEIGHTS package, were benchmarked and compared with experimental results of plasma expansion and produced ions characteristics and EUV photons collection. Detail analysis of the main laser interaction with the evolving plasma/vapor and EUV source size and strength allowed predicting and optimizing of both lasers parameters that influence source efficiency.

9776-26, Session 7

## Pulse widths optimization of dual-beam laser systems for high-power EUV sources

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Development of high power EUV sources is critical to produce high quality chips with sufficient throughput. This requirement together with concerns related to the efficiency of laser energy conversion to EUV photon output and collection as well as energies of ions and fluences of neutrals from

the developed plasma/vapor plumes lead to challenging tasks for source optimization. Analysis of source throughput limits and ways for extension should be done exploring variation in laser beams parameters and target characteristics to find optimum solution to achieve the high-power requirements.

Dual-beam laser interacting with small Sn droplets are most suitable systems for high volume manufacture and optimization paths and opportunities for source improvements. The EUV source efficiency is influenced by a combination of several parameters need to be studied in details. We continued optimization of EUV sources using our comprehensive HEIGHTS package and experimental facilities at our CMUXE center. We investigated parameters of pre-pulse laser in combination with different parameters of the main laser, optimized delay time between these pulses and considered various droplet sizes to produce most efficient EUV source and to predict ways for the enhancement of EUV source power. We also simulated energies of ions and angular distribution of debris resulted from both lasers interactions with target/plasma. Our studies predicted the optimization limits of EUV high-power output from droplets with various sizes and the dependence on main laser pulse duration.

Realistic predictions can only be done using well-benchmarked models with detail description of all the processes involved in complex dual-beam laser systems. The HEIGHTS package contains full 3-D description of all phases of laser target evolution. These include advanced modeling of laser photons interaction with droplet/vapor/plasma, target vaporization and ionization, plasma hydrodynamic expansion, thermal and radiation energy redistribution, and photons collection as well as detail mapping of photons source location and size. Modeling results were benchmarked against various experimental studies for laser systems comparing EUV photons output, images of EUV sources, and energies of produced ions.

9776-27, Session 7

## Energy effective dual-pulse bispectral laser for EUV lithography

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The creation of high volume manufacturing lithography facilities with the technological standard of 10-20 nm is related to the implementation of resist exposure modes with pulse repetition rate of 100 kHz.

One of the promising schemes supporting such mode is based on the extreme ultraviolet (EUV) radiation emitted from plasma formed by illumination of target with a focused laser beam. The highest efficiency of EUV radiation is achieved under the two-pulse bispectral target irradiation using a hybrid primary source consisting of solid-state and ??2 lasers. In such systems the solid state laser (SSL) emits a pulse of relatively low power for the preliminary heating of the target and the plasma initiation. The main power pulse comes from the ??2 laser with a certain time delay, thereby increasing the conversion efficiency.

The possibility to reduce power consumption in the channel of primary laser, which provides the main powerful pulse for the converter plasma irradiation, is modeled in this study. The effect of a gigantic image contrast transfer in the nonlinear inorganic resist observed under illumination by the high-intensity radiation provides a high resolution of the integrated circuit (IC) topology elements. It contains the master oscillator SSL, stimulated Raman scattering (SRS) conversion cascades and the ??2 amplifier. In this scheme SSL serves for preliminary target heating and plasma initiation and as a pump source for the series of SRS converters. Radiation of the second Stokes component with the wavelength of 10.6 μm from the final SRS converter is injected into the ??2 amplifier as an input. Note that in this case the SRS converters do not require a power supply. They are pumped solely by the low power SSL radiation with wavelength of 1.06 μm and the first Stokes component obtained from the conversion of this radiation. Several rotated mirrors are set for adjustment of the time delay between the preliminary and main pulses in the final SRS cell containing hydrogen by pressure of 60 bar. Low power consumption of the proposed scheme makes it promising for the creation of LPP EUV sources

9776-28, Session 7

## Enabling laboratory EUV research with a compact exposure tool

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In this work we present the capabilities of the designed and realized extreme ultraviolet laboratory exposure tool (EUV-LET) which is developed at the RWTH-Aachen, Chair for the technology of optical systems (TOS), in cooperation with the Fraunhofer institute for laser technology (ILT) and Bruker ASC GmbH. Main purpose of this laboratory setup is the application in research facilities and small batch production, where the fabrication of high resolution periodic arrays over large areas is required. The efficiency and productivity of the method is compared with alternative technologies like nanoimprint or electron beam lithography.

A commercially available xenon/argon discharge produced plasma (DPP) source optimized for a working wavelength of 10.77 nm (3.12 % bandwidth) is utilized. The setup allows exposures of wafers up to 100 mm diameter with single exposure fields up to 4x4 mm? in proximity mode and at defined distances up to 150 μm between mask and wafer. Taking advantage of the achromatic Talbot effect exposure results show structure periods that are reduced by a factor of two compared to the initial mask structure period.

The optical system consists of high precision positioners for mask and wafer (encoder resolution < 10 nm) and a laser-PSD-system allowing parallelization of mask and wafer with ~100 μrad-precision. The distance and tilt between mask and wafer are measured by capacitive sensors and adjusted by high-precision positioners during exposure and minimized by an active vibration cancelling system.

Dose monitoring is realized by a diode based dose monitor with full range transmission filter (9 nm to 16 nm) in combination with a compact in-line transmission grating spectrograph for measuring the spectral distribution of the source before and after exposure. The setup is additionally equipped with a quadrupole mass spectrometer to monitor the outgassing behavior of the photoresists before and during exposure.

Results of source characterization and optimization concerning spectral purity and source diameter at different gas mixtures are shown as well as lifetime studies of the electrode system.

Additionally, recent progress in the developed transmission mask fabrication process for wavelengths below the silicon L-absorption edge at 12.4 nm is presented. Transmission masks consisting of niobium membranes in combination with nickel absorber structures fabricated by electron beam lithography and ion beam etching patterning are utilized.

As a demonstration of the capabilities of the system several positive and negative tone photoresists (ZEP-520A-7, XR1541, PMMA and CSAR62) are characterized by measuring the contrast at the working wavelength of 10.77 nm directly in the EUV-LET. Cold development procedure is investigated for the positive tone resist ZEP520A-7 and the influence of the resist thickness on the contrast is investigated.

Exemplary exposure results in proximity distance and achromatic Talbot distance are presented. Dose-to-size and size-to-distance exposure results illustrate the image formation for lines and spaces (LNS) structures as well as for rectangular and hexagonal arrangements of pinholes in agreement with simulation results. LNS and pinhole arrays down to 40 nm half pitch with feature sizes below 20 nm in up to 50 nm thick photoresist are shown.

9776-29, Session 7

## Experimental tests of tin LPP plasma control in the argon cusp source

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The argon cusp plasma has been introduced for 500W class tin LPP exhaust control [1] in view of its high power handling, predicted low tin back-scatter from a beam dump into the reaction chamber, and avoidance of hydrogen usage. Using a surrogate argon plasma its stability and disc geometry have been proved at full scale [2] with further power handling extended in the present report to 15kW, the equivalent of 300W usable EUV. We have verified another critical functional aspect of the argon cusp, the plasma barrier that maintains high argon density next to the collector and low density in the long path toward the intermediate focus. This optimizes both collector protection and EUV transmission efficiency. A pressure differential of 2Pa has already been demonstrated. Tin LPP plasma control by the cusp has been demonstrated using a low Hz 120mJ CO2 laser pulse onto a solid tin surface at the cusp center. Plasma is rejected at the <0.5% level at the collector location using the cusp magnetic field alone. Plasma also is rejected using a low argon density (1x1015cm-3). Measurements will further be presented on the tin plasma flow pattern toward the large area annular beam dump. In view of these detailed tests argon cusp exhaust control appears to be very promising for 500W class tin LPP sources.

[1] M. W. McGeoch, "Power Scaling of the Tin LPP Source via an Argon Cusp Plasma", Proc. Sematech Intl. Symp. on EUV Lithography, Washington DC, 27th Oct (2014).

[2] M. W. McGeoch, "Test of an Argon Cusp Plasma for Tin LPP Power Scaling", Proc. SPIE 9422, paper 79, 24th Feb (2015).

9776-30, Session 7

## Free electron lasers for 13nm EUV lithography: RF design strategies to minimise investment and operational costs

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The most promising alternative to create high power 13nm extreme ultra-violet (EUV) frequencies for photolithography applications is to use a Free Electron Laser (FEL). These next-generation systems present an opportunity to generate monochromatic light intensities far beyond current industrial capabilities, but would require significant investment in infrastructure and running costs. However, developments in FEL technology mean that infrastructure and running costs can be significantly reduced by careful design and exploitation of physical principles.

A major contribution to the costs of first-generation FELs is the cryogenic cooling system required to maintain the resonant cavities of the linear electron accelerator (LINAC) at liquid helium temperatures. This requires provision and continuous operation of closed circuit helium cryostats. However, following recent developments, FEL designs are now able to use room temperature normal conducting RF cavities, which have the dual bonus of lower operational costs and reducing the space required for the particle accelerator, due to their increased accelerating gradient.

Ampegon has been working with the Laboratory for High Power Electronic Systems at ETH Zürich to develop a short pulse RF modulator system specifically designed from first principles to feed normal conducting cavities tuned for C-Band (5.7 GHz) RF. Similarly, we have developed long pulse modulator systems for superconducting FEL accelerators requiring lower operational frequencies (1.3GHz). The primary requirement of these systems is to provide up to 25MW (peak) RF pulses of variable durations, with demanding rise-time and flat-top droop limits. As well as meeting these requirements, systems should incorporate measures to ensure greatest possible efficiency, best possible pulse-to-pulse stability and operational reliability. These characteristics are all critical to the performance of an FEL intended for lithography applications. We will present further details of different FEL design strategies in our paper.

Since any future EUV FEL photolithography systems will need to be operated with almost 100% reliability, provision of a high specification FEL is only one consideration: For industrial roll-out, the entire system should also be highly reliable, modular, feature precautionary redundancy, be designed for little or no maintenance requirements, and require minimal operating costs over its lifetime. Our paper explains how such demanding goals can be fulfilled in order to meet the emerging EUV photolithography requirements of the semiconductor industry while minimising investment and operational costs.

9776-31, Session 7

## Characterization of wavefront and coherence properties of EUV sources

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Comprehensive characterization of the propagation behaviour of short wavelength radiation is a supposition for the successful implementation of EUVL systems. Corresponding metrological tools are being developed at Laser Lab. Göttingen, with strong emphasis on wavefront and spatial coherence diagnostics.

The wavefront is characterized with the help of a Hartmann-type sensor developed for the EUV/soft x-ray range. In contrast to interferometric wavefront measurements, the Hartmann technique affords rather compact setups and can be employed for both coherent and partially coherent radiation, enabling a fast characterization and optimization of optical beam line elements. The Hartmann device is employed for beam characterization and actinic fine-tuning of beam line optics of different types of sources emitting in the EUV range, i.e. free electron lasers (FEL), synchrotrons, High Harmonic (HHG) and plasma based systems.

Since the free-electron laser is a candidate for HVM EUV lithography sources, its coherence properties must be understood in depth to accomplish the proper design of optical systems for beam transport, homogenization and imaging. Studying the related literature reveals strongly varying experimental coherence values for FEL radiation, ranging from almost incoherent to nearly fully coherent beams. The Wigner distribution function (WDF) describes the entire propagation properties of a directed radiation field, including all information on its spatial coherence. It can be reconstructed from beam profiles taken at different positions along its propagation direction. Here, we present measurements of the WDF conducted at the Free-electron laser FLASH at DESY. As a result, we derive the entire four-dimensional mutual coherence function, the coherence lengths and the global degree of coherence. The influence of the FEL control parameters (e.g. e-beam optics, charge saturation) on the coherence properties is discussed.

9776-76, Session PSTue

## Purification solution for EUV pod

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Extreme ultraviolet(EUV) pod is one of the most favorable technologies for transport and shipping reticle, while maintaining reticle quality. Since the feature size miniaturization of semiconductor process, the purification requirement is becoming more strictly. Therefore, many suppliers of semiconductor equipments devote to the purification issue of manufacturing processes of EUV pod. In this work, the Taguchi method was used to obtain the optimal condition to improve the purification quality of EUV pod by relative humidity(RH). Then, another goal of this paper was to investigate the effect of rubber strength on maintaining RH% after purging. The result showed that most important factor is flow rate which could reduce the purge time. The contribution of flow rate and filter size for purification of EUV pod was 91.2% and 8.2%, respectively. The influence of gas type and the layout of inlet/outlet position were not significant. The higher the flow rate and the greater the filter size was the shorter the purge time. Moreover, the influence of rubber strength on maintaining RH% after purging was not significant. The Taguchi method has an efficient reduction of cost and time of experiment and could determine the optimum condition to enhance the ability to remove the water-vapor inside EUV pod.

9776-77, Session PSTue

## 100W EUV light-source key components technology update for HVM

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Key components technology update of 100W LPP-EUV (laser produced plasma extreme ultraviolet) light source for high volume manufacturing which enable sub-10nm critical layer patterning for semiconductor device fabrication are introduced. This EUV light source system is composed of several key components such as a magnetic debris mitigation system, a high power short pulse CO2 drive laser system, a unique pre-pulse laser system, a small droplets generator and a laser-droplet shooting control system. These components contribute higher EUV output power and longer stable operation. The magnetic debris mitigation system protects a EUV collector mirror from rapid reflectivity degradation with tin contamination resulting shorter operating time. The mitigation system prevents tin ions created in plasma from incidence on a collector mirror but guides tin ions to ion catcher efficiently with less hydrogen gas usage. Lower tin deposition rate, <0.0007 nm/Mpls on collector mirror with < 20 Pa hydrogen pressure was achieved. The high power shorter pulse CO2 laser can generate EUV emission efficiently and realize higher EUV power. The high power CO2 drive laser system composed of higher gain amplifiers realizes a shorter laser pulse with higher output power. 20kW of CO2 laser output and 15 nsec pulse duration with 100 kHz was achieved. The pre-pulse laser system makes higher conversion efficiency, CE, CO2 laser energy to EUV energy efficiency, possible by optimizing tin mist distribution for efficient EUV generation with a short pulse CO2 laser radiation. 4.5% of CE was achieved with optimizing pre-pulse laser properties. New pre-pulse system also improved tin ionization rate to ~99% from ~60% and this contributes longer EUV system operation time. The improved droplet generator can create smaller size and stable droplets suitable for longer operation time due to less tin debris generation. ~20 um diameter droplets and position stability of less than +/- 5 was achieved. The laser-droplet shooting control system controls several actuators, laser properties and droplet properties for accurate tin droplets shooting. Shooting error is cause of shorter operation time due to much amount of tin debris generation. The improved metrology system also contributes shooting accuracy and shooting error is decreased. These components worked harmoniously to produce stable plasma and to evacuate tin debris from a EUV vessel effectively in order to realize a high power and a long life EUV light source system. The latest system performance results obtained from our proto systems with key components which support 100 W output power of LPP-EUV light source will be reported.

9776-78, Session PSTue

## Stress-induced pellicle analysis for extreme-ultraviolet lithography

Eun-sang Park, Hye-Keun Oh, Hanyang Univ. (Korea, Republic of)

Recently, extreme ultraviolet lithography (EUVL) has received much attention as a promising candidate to achieve 10 nm node or below high resolution patterning. However, EUVL faces a lot of obstacles before it could be used for high volume manufacturing (HVM). For instance, in case of EUVL, a very small size defect turns out to be quite critical which is otherwise negligible for conventional lithography.

Consequently, the image quality degradation due to the defect size near the focal plane of EUV mask poses a serious problem for HVM. Using a pellicle could decrease the critical size of a defect by taking the defect away from the focal plane of a mask. However, the thickness of the pellicle should be kept very thin since most of the materials used as pellicle have high absorption for EUV light.

Considering the double pass transmission for HVM (which allows at most 80% EUV transmission) the thickness of EUVL pellicle should be ~ nm thin. For ~ nm thin pellicle, thermal heating (produced by the exposure to EUV light) induces thermal stress, which beyond certain threshold value may damage the pellicle. Therefore, a careful investigation of thermal stress is desired for reliable EUV light transmission through pellicle.

To this end, we revisited thermal stress analysis along radial direction with suitable boundary conditions applied to the pellicle model. The maximum thermal stress in case of 50 nm thick silicon pellicle is found to be within the range 0.08 ~ 0.12 GPa. And the radial stress $\sigma_{rr}$ at the center of the pellicle follows the behavior of temperature T variation during 10 ms exposure time t as shown in Fig. 1.

In Fig. 1, the thermal stress induced to the silicon pellicle by EUV light exposure is only shown, however the mechanical stress and the residual stress also affect the pellicle. Therefore, we calculated the total stress and compared with ultimate tensile strength (UTS) of the pellicle. The mechanical deformation by gravity was calculated by our previous work and well fitted with the finite element method (FEM). Therefore the mechanical stress is calculated with FEM.

The residual stress is dependent on not only the material properties but also the deposition condition. And we arbitrary chose some deposition condition by considering thin film manufacture environment since exact condition is not known.

The breaking or the safety of the pellicle could be determined by the induced total stress, however, the cyclic exposure heating could decrease the UTS of the pellicle. The high cycle exposure could give the damage to the pellicle although the low cycle EUV light exposed pellicle could be easily recovered by sufficient radiative cooling time.

9776-79, Session PSTue

## Update on EUV radiometry at PTB

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With the introduction of EUV Lithography into high volume manufacturing, the focus of development expands. In particular, all approaches to increase throughput and availability of EUV steppers are persued vigorously. For example, development of EUV compatible pellicles is one approach to adopt an approved method from optical lithography for EUVL. To support these developments, PTB with its decades of experience in EUV metrology provides a wide range of actinic and non actinic measurements at inband EUV wavelengthes as well as out of band. Two dedicated and complimentary EUV beamlines are available for radiometric characterizations benefiting from small divergence or from adjustable spot size respectively. The wavelength range covered reaches from below 1 nm to 45 nm for the EUV beamlines to longer wavelengthes if in addition the VUV beamline is employed. The standard spot size is 1 mm by 1 mm with an option to go as low as 0.1 mm to 0.1 mm. A separate beamline offers an exposure setup. Exposure power levels of 20 W/cm2 have been employed in the past, lower fluences are available by attenuation or out of focus exposure. Owing to a differential pumping stage, the sample can be held under defined gas conditions during exposure. We present an updated overview on our instrumentation and analysis capabilities for EUV metrology and provide data for illustration.

9776-80, Session PSTue

## LWR and defectivity improvement on EUV track system

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Co., Ltd. (Japan); Harold Stokes, Yan Thouroude, SCREEN SPE Germany GmbH (Germany); Koji Kaneyama, Charles Pieczulewski, Masaya Asai, SCREEN Semiconductor Solutions Co., Ltd. (Japan)

EUV lithography (EUVL) is well known to be a strong candidate for next generation, single exposure sub-30nm half-pitch lithography. Furthermore, high-NA EUV exposure tool(s) released two years ago gave a strong impression by finer pattern results. On the other hand, it seems that the coat develop track process remains very similar and in many aspects returns to KrF or ArF dry process fundamentals, but in practice 26-32nm pitch patterning coat develop track process also has challenges with EUV resist.

As access to EUV lithography exposures became more readily available over the last five (5) years, several challenges and accomplishments in the track process had been reported, such as the improvement of ultra-thin film coating, CD uniformity, defectivity, line width roughness (LWR) and so on. The coat-develop track process has evolved along with novel materials and metrology capability.

Line width roughness (LWR) control and defect reduction are demonstrated utilizing the SOKUDO DUO coat develop track system with ASML NXE:3100 and NXE:3300 exposures in the IMEC (Leuven, Belgium) clean room environment. Additionally, we will show the latest lithographic results obtained by novel processing approaches in the EUV coat develop track system.

9776-81, Session PSTue

## Fundamental study on dissolution behavior of poly(methyl methacrylate) using by quartz crystal microbalance

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Recently, the fabrication of sub-10 nm features has attracted much attention. Electron beam and extreme ultraviolet (EUV) radiation are regarded as the most promising exposure source for next-generation lithographic technology. In the realization of high resolution lithography, it is necessary for resist materials to improve the trade-off relationship among sensitivity, resolution, and line width roughness (LWR). In order to overcome them, it is essential to understand basic chemistry of resist matrices in resist processes. In particular, the dissolution process of resist materials is a key process. However, the detail in dissolution process has not been investigated so far. In chemically amplified resists used for ionizing radiations, acid generators are decomposed through the dissociative electron attachment of thermalized electrons. This sensitization mechanism induces a resolution blur. On the other hands, poly(methyl methacrylate) (PMMA) is decomposed from their radical cations. The thermalized electrons are considered not to contribute to the decomposition of PMMA. From the viewpoint of sub-10 nm fabrication, the sensitization mechanism of PMMA is attractive. Therefore, we investigated the dissolution behavior of PMMA with various molecular weight using EUV exposure tool and quartz crystal microbalance (QCM) method. Also, the change of PMMA induced by radiation in molecular weight was analyzed by gel permeation chromatography (GPC).

Four kinds of PMMA with different molecular weight (Mw=50000, 120000, 350000, and 996000) were used as a resist. Propylene glycol monomethyl ether acetate (PGMEA) was used as casting solvent. In the sample preparation for sensitivity and QCM experiment, PMMA solutions were filtered through a 0.20 nm PTFE syringe filter prior to spin-coating onto silicon or QCM substrates in order to make clean films. PMMA solutions were spin-coated onto silicon or QCM substrates to form thin films with c.a. 100 nm film thickness and exposed to EUV radiation (Energetic, EQ-10M). The exposure doses ranged from 0.01 to 40 mJ/cm2. They were immersion-developed in o-xylene and 1:3 solution of methyl isobutyl ketone (MIBK): isopropanol (IPA) for 30 s and rinsed in IPA for 15 s before drying. The effect of molecular weight of PMMA on dissolution behavior was investigated by the QCM-based development analyzer (RDA-Qz3). Resist film thickness was measured with a surface profiler (ET200 (Kosaka Laboratory Ltd.)) and spectroscopic elipsometry(UVISEL(Horiba)). Also, the molecular weight of the PMMA degraded by 60Co ?-radiation was analyzed using a GPC system (Shodex GPC-104).

We measured sensitivity and dissolution behavior of four kinds of PMMA with different molecular weight. With increase of molecular weight, the sensitivity of PMMA decreased. Also, it was observed that dissolution behavior of PMMA varies with the molecular weight of PMMA, exposure dose and developer from QCM measurement. It was indicated that the change of swelling behavior in PMMA with different molecular weight might lead to LWR. Furthermore, the correlation between molecular weight after radiation and development rate was observed in spite of the initial molecular weight of PMMA.

9776-82, Session PSTue

## Imaging plate analysis of extreme-ultraviolet light from laser-produced plasmas

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To produce the next generation of integrated circuits, industry and researchers have primarily focused on optimization of extreme ultraviolet (EUV) lithography at 13.5 nm using laser-produced plasmas (LPPs). For high-volume manufacturing (HVM), the EUV light source requires an array of mirrors by which to reflect the generated light for lithography of the circuits. Optimization of the system has been extensive to date, with research investigating many aspects such as target types/dimensions, laser pulse lengths and plasma dynamics amongst other points of interest to increase the overall efficiency of the system. The EUV and other high energy species generated are scattered from the point of ablation, therefore a better understanding of the light from a large angular distribution compared to a single point could be used to further develop light sources. In the laboratory, a grazing incidence spectrometer (GIS), calibrated energy meter (E-mon) and other calorimeters are the standard tools used to detect EUV. However, this is perhaps not the most sufficient means by which to continue to develop EUV light sources as these techniques are fixed at a specific angle from the target, therefore valuable information of the light is lost at the larger and smaller angles. This paper demonstrates extensive use of a phosphor (BaFBr:Eu) imaging plate (IP) (BAS-TR) to analyze EUV light generated by a tin LPP as method to further complement GIS data. The BAS-TR imaging plate is optimized to detect fast neutrons, and was employed characterize EUV light generated from a planar tin target (13.5 nm) using a Nd:YAG 1064 nm laser ($\varphi$ = 1.6 x 1011 W cm-2) between 9-90 degrees, were the laser is referenced at 0 degrees, in conjunction with a GIS. The EUV light was shown to be dependent on the angle from the EUV source, with the highest intensity observed to be most parallel to the laser, and the lowest perpendicular to the laser. A zirconium (Zr) filter was also used to control the light intensity the imaging plate was exposed to, but the angular dependency relationship remained consistent. Imaging plate data in comparison to GIS data was consistent for either with, or without, the zirconium filter, with both IP and GIS data recording much higher intensities without a Zr filter compared with a Zr filter. In summary, use of phoshor imaging plates were used to analyze and obtain a greater understanding of EUV from LPPs at a larger angular distribution than previously reported. This technique could be adopted to further develop EUV light sources, for example in target or mirror design.

9776-83, Session PSTue

## Novel chemically amplified resist development for line-edge roughness reduction using by Monte Carlo simulation in extreme-ultraviolet lithography

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Extreme-ultraviolet (EUV) lithography with wavelength of 13.5 nm is the most promising candidates for 10x nm patterning and beyond. The resist trade-off relationship among resolution, line edge roughness (LER), and sensitivity is a key role to the realization of EUV high-volume manufacturing (HVM). Especially, the LER reduction is very difficult, while resolution and sensitivity have already reached to target values.

The LER is formed as a result of various chemical reaction through many material and process parameters in lithography environment such as exposure and post exposure bake (PEB), and development process. Among them, the LER depends on the characteristics of synthesized resist with regard to material parameters; a molecular size of resist, ratio of resist composition elements, and homogeneity of resist composition elements. According to the international technology roadmap for semiconductor (ITRS), the LER is required to be less than 2 nm for 10x nm feature size, so that making a novel resist that can obtain smaller LER with various material parameters is needed.

We tried to demonstrate a new approach of EUV resist composition that of high performance molecular-resist since the extent of LER is typically proportional to molecular size of resist. We investigated the dependence of various resist composition and LER control by Monte-Carlo simulation. Figure 1 shows the probability distribution of de-protection reaction (gray color) with different molecular-resist size considering a random walk algorithm. We can see that the LER cannot be controlled well as the molecular-resist size goes larger even if the de-protection ratio is the same. Furthermore, we also changed various resist composition parameters such as ratio of protected site, photo acid generator (PAG), and quencher in order to find the optimum resist composition for smaller LER (~ 2 nm).

9776-84, Session PSTue

## Modeling of initial interaction between the laser pulse and Sn droplet target and pre-plasma formation for the LPP EUV source

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Improvement of efficiency and output of the laser pumped plasma (LPP) extreme ultra-violet (EUV) light source has critical importance for the realization of EUV lithography, which demands an optimization based on numerical modeling. It is shown that an irradiation by a low intensity pre-pulse laser is used to produce uniform low-density plasmas. By the irradiation, the Sn droplet target is broken up to small particles [1], which are distributed into the sphere with a radius of few 100 micrometers, resulting in the averaged density of the plasma to be 10-3 solid density, which is suitable for efficient EUV emission by the irradiation of the main CO2 laser pulse [2]. The Sn target is heated upto few thousands K to cause melting and evaporation, and the particles are considered to be produced through several mechanisms. The rapid heating may cause boiling of Sn to cause particle emission. Particles may also be produced by condensation during the expansion cooling of the Sn vapor. Moreover, high pressure is produced in the laser and plasma interaction to produce the shock wave inside the solid to cause fragmentation of the target [3].

We show a development of a hydrodynamics simulation of laser irradiated Sn target to calculate its temporal and spatial evolution. We show a test calculation of the evaporation of the heated Sn target, showing initially bubbles are formed inside the target, which grows rapidly until evaporated vapor expands including small particles inside. The model is based on the two dimensional Lagrangian hydrodynamics, in which the mesh is organized according to the distribution of the material. Each cell is determined to be either in the gas phase or solid/liquid phase and the mixed phase condition is represented by the arrangement of the cells. The gas phase is represented by the ideal gas equation of state, and the solid/liquid phase is considered as an elastic body. The temperature of solid/liquid phase is determined according to the Dulong-Petit law from the thermal energy. The energy is also stored as the potential energy according to the strain. The transition between gas and solid/liquid phase is determined based on the Van-der-Waals equation of state of Sn [4], from which the ratio between gas and solid/liquid phase is obtained for a given temperature and volume. The cells are split and united at each time step to maintain the aspect ratio of the cell to be within the acceptable values. The technique is also used to have the appropriate ratio between the gas and solid/liquid phase at the steady state for groups of the cells. In the presentation, the concept of the model, numerical methods, inclusion of physics specific to the laser matter interaction as well as results of test calculations and validation of the code for its application to the EUV source are discussed.

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9776-85, Session PSTue

## Multi-mirror adaptive optics for control of thermal aberrations in extreme-ultraviolet lithography

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Extreme ultraviolet lithography (EUVL) uses light with a wavelength of 13.5 nm, which is strongly absorbed by most materials. Therefore, EUVL operates in vacuum and uses reflective instead of refractive optics. The projection optics (PO) transmit light from the reticle to the wafer using six multilayer coated mirrors. The mirrors are heated by the absorption of the EUV light, leading to deformations that degrade the imaging quality of the PO. With the semiconductor industry's need for both higher resolution and higher productivity, thermal aberration prediction and control becomes more important. The thermal aberrations are field dependent, since the pupils from different field points encounter different parts of the deformed mirrors when traveling through the PO. This motivates the use of multiple deformable mirrors. In this paper, we evaluate methods to reduce thermal induced aberrations by actively deforming the reflective surface of multiple mirrors in the PO, or Multi-Mirror Adaptive Optics (MMAO).

Previously, the aim was to minimize the total RMS WFE, but this is not always the best solution when taking specific lithography criteria into account. While the WFE directly expresses the error in optical path length, its derivative is related to the displacement of rays at the wafer [1,2]. This enables the inclusion of constraints into a Quadratic Constrained Quadratic Program, which then finds a solution that optimizes several image criteria for each object point individually. Examples are RMS WFE, RMS spot size and overlay in x and y.

Our study is based on a fully coupled multiphysics model [3] of a six mirror ring field projection system that is obtained from the patent literature [4]. We simulate the first two hours of a worst case off-axis y-dipole illumination of a dense line pattern, with a source power at intermediate focus equal to 1 kW. Only the in-band 13.5 nm EUV radiation is considered.

The thermal induced aberrations are first corrected with the rigid body adjustments of the mirrors, reticle and wafer (RBA). Thereafter, we show an improved performance by actively deforming one (RBA+M2) and then two (RBA+M1+M2) of the mirror surfaces. Both deformable mirrors have an equidistant actuator spacing of 10 mm. The closed loop simulation results show that the latter configuration can bring the performance close to the nominal performance of the PO.

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9776-86, Session PSTue

## Design and development of low-activation energy based n-CARs for next-generation EUV lithography

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The rendition of EUV resists is one of the major challenges for the cost-effective realization of next generation EUV lithography into the high-volume production of sub 20 nm technology nodes. EUV lithography (EUVL) is a promising technique as per the 2013 ITRS roadmap, predicted to print high resolution features, 16 nm line patterns and beyond. However, high throughput will be required for the realization of EUV tools in order to make them feasible for next generation manufacturing. Thus EUV resists must have exceptionally higher sensitivity than current resists, and stringent photo speed, because scaling of resists isolated lines (PLY Gate) after etch and LWR have been set to ~15 nm and ~ 1.5 nm to avoid the impact on CMOS device performance, like high leakage current, power consumption and heat generation etc. It is very challenging to meet photo sensitivity and LWR & LER simultaneously with the traditional resists and techniques. Although, chemically amplified resists (CARs) have been the workhorse resists used for commercialization of deep ultraviolet (DUV) lithography, yet unfortunately, the random walk nature of photo acid diffusion, exceptionally higher LER and LWR and minimal critical dimension (CD) control, process complexity, post exposure instability and environmental sensitivity etc. are fundamental apparent concerns at the sub-20 nm node. This confines adeptness of these resists to be front end resists for EUV technology. Therefore, in the present study, novel non chemically amplified negative tone (n-CARs) resists, MAPDST–i-PrMA [Mw = 14000 g/mol] and MAPDST-t-BMA copolymer [Mw = 12686 g/mol] have been designed and synthesized from suitable monomers containing the radiation sensitive sulfonium functionality. Dose to clearance EUV exposure established their E0 sensitivity at 11.3 mJ cm-2, and 50 mJ cm-2 respectively, as revealed in FESEM Fig.1 (a), inset (b) and inset of AFM (c) micrographs at 25000X and 100000X magnifications, complementing with the exposure characteristics of MAPDST homo-polymer reported earlier, however with improved performance over line width roughness (LWR) and line-edge roughness (LER) control, at optimum dose for EUV lithography. Since all the polarity switching of the novel n-CARs typically occur during EUV exposure and avoid acid diffusion, blur they are therefore anticipated to have superior resolution even beyond the 20 nm node and CD control. Though, it is still not well established among the exposure dose or processing parameters, which factors have the prominent dominance over the control of LER & LWR, it is clear that to attain the 16 nm technology node and beyond, that is for EUV technology realization, a high sensitivity, low line edge roughness/line width roughness is essentially needed. Over and above very limited outgassing to avoid contamination of the optics in vacuum is indispensable. In summary, we address the capabilities of low activation energy based novel n–CARs resists, primarily the MAPDST–i-PrMA copolymer EUV resists to meet the stringent patterning requirements, and highlight areas where acceleration is required to meet prerequisites of the next generation EUV technology roadmap.

9776-87, Session PSTue

## Investigating the plasma cure on improving LER/LWR of narrow trench for sub-10nm node technology with EUV lithography

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The 13.5-nm wavelength extreme ultraviolet lithography (EUVL) is expected to become one of the potential candidates for critical patterning at narrow pitch for 7-nm technology node and beyond. Since EUV lithography technique introduces newer types of resists that are thinner and softer compared to conventional 193-nm resists, the main challenge is to find the key etch process parameters to improve the EUV resist selectivity, reduce line edge/width roughness (LER/LWR), minimize line end pull-back, improve tip-to-tip degradation and avoid line wiggling.

Due to the small dimensions, stochastic effects of a discrete nature start playing a fundamental role in the definition of the feature edges which impact the device performances such as time dependent dielectric breakdown (TDDB) and electrical resistivity. As a result, LER/LWR must be improved and, according to the international technology roadmap for semiconductors (ITRS), should go below 2-nm for 16-nm CD line at 32-nm pitch.

EUV photo resist (PR) backbone is styrene-based and contains multitude of carbonyl and ester groups. These groups absorb vacuum ultra-violet light (VUV) that is known to cause chain scission reactions in the PR. This phenomenon result in resist reflow and rearrangement which enables smoothening of the PR. In this study, we investigate the LER/LWR mitigation techniques at PR level by using plasma treatment. Different chemistries such as H2, HBr, H2/N2, H2/Ar and He/H2 are tested using different plasma settings (power, pressure, gas flow...) in a TEL CCP-type reactor.A 10-nm technology node back-end-of-line vehicle was chosen for on-pattern roughness analysis using CD-SEM, blanket wafers were used to study modifications of the PR using FTIR, ellipsometry and AFM and finally, VUV emission spectra were collected to complete the study.

Our results show that, for 24-nm dense lines, LER was improved with all the chemistries. However, LWR was only improved with the N2/H2 based chemistry. In summary, N2/H2 based plasma cure appears as the most promising PR treatment to lower both LER and LWR. We observe about 23% LER reduction and 32% LWR improvement for 24-nm HP Line-Space.

9776-88, Session PSTue

## Alternative irradiation scheme for EUV source for inspection applications

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Extreme Ultraviolet Lithography (EUVL) is one of the leading technologies for future photolithography techniques. It will allow the surpassing of the critical resolution limits of current ArF lithography techniques for the generation of 10 nm semiconductor chip node size and beyond. The generation of light in the EUV range through a Laser Produced Plasma (LPP) is one of the leading technologies for the development of high volume

manufacturing (HVM) lithography light sources. In particular through the irradiation of tin droplets by high-irradiance laser pulses, that generate plasmas that are highly emissive around 13.5 nm.

At the Applied Laser Plasma Science (ALPS) laboratory of LEC-ETH Zürich, a droplet-based laser-produced plasma (LPP) soft X-ray source with application in EUV metrology has been developed. The main source ALPS II is a prototype source equipped with a large capacity droplet dispenser and a high power (kW), high repetition rate Nd:YAG laser.

To optimize the overall source performances it is fundamental to improve current debris mitigation techniques in order to limit the amount of produced plasma debris (high energy ions, low energy neutral particles and neutral cluster debris). The distribution and composition of plasma debris in the source is also dependent on the early stage droplet-laser interaction and the subsequent ablation process. Recent work at the ALPS laboratory has been focused on the understanding of the plasma debris dynamics. In particular, alternative irradiation schemes that show potential for spatially shaping the debris composition and for increasing the coupling between the fuel and main pulse laser energy.

In this work, these alternative droplet irradiation schemes will be discussed. The fuel droplet and subsequent debris breakup has been imaged for different laser irradiances ranging from 5-150 GW/cm2 with a high-speed shadowgraph imaging system. For the different laser irradiances, the debris velocity and trajectory are measured on the parallel plane to the laser axis. An analytical model is derived, which describes the neutral cluster debris velocity and trajectory using conservation of energy and momentum. The model is validated against the experimental results being in good agreement with the measurements. It is demonstrated that the dominant mechanism transferring momentum to the neutral cluster debris is the ablation pressure acting on the unablated droplet volume. A relation is also derived and experimentally validated which describes the neutral cluster debris deflection as a function the laser spot size, droplet diameter and droplet-laser misalignment. The results discussed in this work have an important relevance for the shaping of liquid droplet targets both in terms for the understanding of fundamental droplet-plasma dynamics and for their implications in EUVL applications.

## 9776-89, Session PSTue

### EUV resist outgassing analysis for the new platform resists at EIDEC

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The suppression of outgassing from the EUV resist is one of the most significant challenges to be addressed for realizing EUV lithography (EUVL) since the outgassing might be the main contributor to the contamination of the mirror optics in scanners which result in the reflectivity loss. The pragmatic outgassing test utilizing the witness sample (WS) has been used as the general method to quantify the outgassing level for commercially available chemically amplified resists (CAR). There are two kinds of contaminations. One is the cleanable contamination mainly consisted of hydrocarbon which can be removed by the hydrogen radical cleaning. Another is the non-cleanable contamination which remains on WS after the hydrogen radical cleaning. There are many outgas qualification results evaluated at EIDEC [1, 2]. Those data indicates contaminations by CAR are mainly consisted of the cleanable contaminations. The data also indicates there are almost negligible non-cleanable contaminations from CAR.

On the other hand, EUV resist communities are accelerating the development of high sensitivity resist to compensate the low power of EUV source. Non-chemically amplified resist (non-CAR) with new platform is one of the candidates for high sensitivity resists. The non-CAR includes some kinds of metal elements which has high absorbance for EUV light. However there is very few knowledge about outgassing characteristics for non-CAR. Considering EUV exposure process in the actual EUV scanner, EUV resists are exposed in hydrogen environment. For the non-CAR resist, there is a possible risk that hydrogen radical generated by EUV light reacts with the metal element in Non-CAR and the metal hydride outgases from the resist. Then outgassing from Non-CAR has potential risk to be a non-cleanable contamination on EUV mirror [3].

EIDEC has prepared the outgas test infrastructures for non-CAR and/or new platform resist in hydrogen. We also prepared some materials including metal elements as non-CAR model samples. In this paper we will report on the recent results in resist outgassing analysis for the new platform resists at EIDEC.

This work was supported by Ministry of Economy, Trade and Industry (METI) and New Energy and Industrial Technology Development Organization (NEDO).

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## 9776-90, Session PSTue

### Modeling of EUV target irradiated by shaped laser beam

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This paper presents computational results for the laser-based plasma EUV sources at a wavelength of 13.5 [1] and ~ 6.7 nm [2, 3]. By 2D radiation-hydrodynamics code [4], the plasma dynamics and collectable conversion efficiency in single and/or multiple laser pulses irradiation scheme are investigated. We have constructed database for the equation-of-state, including the spectral emissivity and opacity for pure and mass-limited targets by the detailed population atomic kinetics code. Modeling results are benchmarked against available observations. The possible effect of the laser pedestal on the target dynamics for the contrast ratio from 0.01-0.1 is examined. It is found that a laser pedestal can modify the dynamics of energy coupling between the main laser pulse and the initial target by producing a pre-plasma that can change the interaction mechanism. The results also demonstrated the influence of spatial and/or temporal laser pulse shaping on the plasma dynamics and conversion efficiency of pure and mass-limited targets.

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## 9776-91, Session PSTue

### High-power EUV irradiation tool setup for resist outgas evaluation in hydrogen

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The suppression of outgassing from the EUV resist is one of the most significant challenges to be addressed for realizing EUV lithography (EUVL) since the outgassing might be the main contributor to the contamination of the mirror optics in scanners which result in the reflectivity loss. The pragmatic outgassing test utilizing the witness sample (WS) has been used as the general method to quantify the outgassing level for commercially available chemically amplified resists (CAR). There are two kinds of contaminations. One is the cleanable contamination mainly consisted of hydrocarbon which can be removed by the hydrogen radical cleaning. Another is the non-cleanable contamination which remains on WS after the hydrogen radical cleaning. There are many outgas qualification results

evaluated at EIDEC [1, 2]. Those data indicates contaminations by CAR are mainly consisted of the cleanable contaminations. The data also indicates there are almost negligible non-cleanable contaminations from CAR.EUV resist communities are accelerating the development of high sensitivity resist to compensate the low power of EUV source. Non-chemically amplified resist (non-CAR) with new platform is one of the candidates for high sensitivity resists. The non-CAR includes some kinds of metal elements which has high absorbance for EUV light. However there is very few knowledge about outgassing characteristics for non-CAR. Considering EUV exposure process in the actual EUV scanner, EUV resists are exposed in hydrogen environment. For the non-CAR resist, there is a possible risk that hydrogen radical generated by EUV light reacts with the metal element in Non-CAR and the metal hydride outgases from the resist. Then outgassing from Non-CAR has potential risk to be a non-cleanable contamination on EUV mirror [3]. EIDEC has already reported the high-power EUV irradiation tool (HPEUV tool) equipped with laser-produced plasma source which we constructed. HPEUV tool was utilized to investigate the effect of EUV power and pulsed irradiation on the resist outgassing and the preliminary results were introduced [4, 5].

In this paper, we will mainly report the details of the setup of HPEUV tool for the outgas testing in hydrogen and also report the recent results of Non-CAR outgassing obtained by HPEUV tool.

This work was supported by Ministry of Economy, Trade and Industry (METI) and New Energy and Industrial Technology Development Organization (NEDO).

9776-92, Session PSTue

## Feasibility of a new absorber material for anamorphic high-NA extreme-ultraviolet lithography

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The extreme-ultraviolet lithography (EUVL) has been regarded as best candidate to achieve high resolution patterning below 1x nm node. Reflective optics should be applied to the EUV lithography tool due to high absorption of EUV light with 13.5 nm wavelength. Shadowing area is introduced due to the incidence angle to the mask and it causes intensity loss, and horizontal-vertical pattern bias (H-V bias).

From the Rayleigh criterion, a numerical aperture (NA) should be increased to achieve high resolution patterning. It means that the angle distribution on the EUV mask is also increased, and then it makes the more shadowing area problem. A new absorber structure which has sufficient image contrast and small height is needed to minimize this problem for realization of high NA optics.

The image contrast is varied in the shape of sinusoidal wave with increasing absorber thicknesses, because of the phase difference between the light reflected from the absorber plane and mask plane passing through inside of the absorber. A material which has lower refractive index and higher absorption coefficient is needed because it has faster phase velocity, so that the phase shifting is occurred quickly even though the smaller absorber thickness is used.

We suggested a new material for an absorber stack and evaluated the patterning performance by using lithography simulation. The material that we suggested is ruthenium oxide (RuO2). The thickness was optimized to ~30 nm from image contrasts for aerial images of 1:1 line and space pattern. To evaluate the performance, several absorber materials are compared and illumination conditions which have 0.33, 0.45, and 0.55 anamorphic NA are considered.

In this study, various pattern sizes, shapes and illumination conditions are considered, including 0.55 anamorphic NA. The feasibility of a RuO2 absorber for high resolution patterning below 10 nm node is studied through the comparison of the image contrast, the normalized image log slope (NILS) and H-V bias.

Figure 1 illustrates image contrasts for 7 nm 1:1 line and space aerial images with various absorber materials. Three materials, 70 nm-thick TaN, 50 nm-thick TaBN, and the RuO2 are compared. Refractive index of a ruthenium is decreased with oxidation, so that we can obtain higher image contrast even though it has small thickness as one can see in Fig. 1. The optimized thickness is 28 nm and the contrast is about 0.65. Figure 2 shows H-V bias for 1:1 line and space aerial images with varying half pitches. It is clearly shown that the H-V bias is improved when we use a 28 nm thickness RuO2 absorber.

9776-93, Session PSTue

## Diamond $CO_2$ laser windows with sub-wavelength surface structures

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Over the past few years, diamond has become the material of choice for high power laser windows in multi-kilowatt CO2 laser systems due to diamond's combination of excellent thermal, mechanical, and optical characteristics. Extreme-ultraviolet lithography is one exciting application for such high power CO2 laser pumps [1]. These windows are typically coated with antireflective (AR) thin films to maximize throughput laser power, increasing transmission at 10 micron wavelength from 71% to 99% or more. As diamond is a remarkably robust material, it is the AR coatings which eventually fail when power density becomes very high. With EUV lithography trending to even more powerful CO2 laser sources and the high costs associated with system downtime, the need for more durable and reliable anti-reflective laser windows is apparent. Surfaces with sub-wavelength structures (SWS) have been proposed as an effective alternative to AR coatings [2], with strong potential for much higher reliability and durability in extremely high power laser applications.

In this paper, we report on design and fabrication of SWS surfaces on synthetic diamond windows. Conventional semiconductor processing equipment and techniques were used to create structure patterns over large areas, currently up to 40 mm in diameter, on both sides of the diamond windows. The structures were designed to give the window surfaces antireflective properties optimized for the CO2 laser wavelength of 10.6 μm. Measurements by FTIR spectroscopy and with a CO2 laser confirmed total window transmission of > 99% at 10.6 μm wavelength and reflection < 0.5%. Process improvements are identified to further increase transmission. Replacing AR coatings with an all-diamond antireflective SWS solution greatly increases LIDT and allows much higher power densities to be transmitted through a window. In a comparison test of continuous wave (CW) LIDT at 10.6 μm, an SWS diamond window far outperformed a thin film coated diamond window. LIDT of the thin film coated window was determined to be ~0.25 MW/cm2 while the same CW laser was unable to damage the SWS window at all, even at power densities as high as 3.5 MW/cm2.

Thermal response is another important performance parameter for high-power windows. AR coatings contribute significantly to the overall absorption of a diamond window and possess poor thermal properties. Exchanging AR coatings with sub-wavelength structured surfaces decreases overall window absorption, helping to keep window operating temperatures low and minimize thermally induced beam distortion.

In summary, the antireflective sub-wavelength structured surfaces presented in this paper demonstrate strong improvement in laser damage reliability and performance over thin film coatings under high power CO2 laser irradiation and may be a key enabler for EUV lithography to reach its wafer throughput target.

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**Conference 9776:**
**Extreme Ultraviolet (EUV) Lithography VII**

9776-94, Session PSTue

## Improvement of line-edge roughness through acid diffusion behavior analysis considered stochastic effect for extreme-ultraviolet resist

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Extreme ultraviolet lithography (EUVL) is one of the most promising lithography technologies for mass production of semiconductor devices. However, critical issues that should be resolved for high volume production still remain. Among them, it is well known that the resolution, line edge roughness (LER) and sensitivity trade-off should be met simultaneously.

Chemically amplified resist (CAR) is composed of a base polymer with protection groups. The protection group in CAR is de-protected by acid catalyzed reaction during post-exposure bake (PEB). And the de-protection region becomes soluble. Therefore the variables related acid reaction mechanism affect the pattern formation and LER. The study of LER considering all of the acid diffusion characteristics is required to find better resist.

Generated acid by EUV photon during exposure process is randomly diffused along all directions. Thus, we investigated the stochastic effects of acid generation and acid catalyzed reaction using a new Monte Carlo simulation. Figure 1 shows acid distribution after exposure and de-protected region depending on acid diffusion length. When acid diffusion length is short, the reaction region is small. Therefore, the short acid diffusion length is needed in order to have small LER. We also investigated LER behavior to determine optimum acid diffusion characteristics such as acid diffusion length, photo-acid generator (PAG) concentration, and homogeneity of PAG distribution.

9776-95, Session PSTue

## An automated image-based tool for pupil plane characterization of EUVL tools

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Pupil plane characterization will play a critical role in image process optimization for EUV lithography (EUVL), as it has for several lithography generations. In EUVL systems there is additional importance placed on understanding the ways that thermally-induced system drift affect pupil variation during operation. In-situ full pupil characterization is therefore essential for these tools. To this end we have developed Quick Inverse Pupil (QUIP)—a software suite developed for rapid characterization of pupil plane behavior based on images formed by that system. The software consists of two main components: 1) an image viewer, and 2) the wavefront analyzer. The image viewer, as seen in Figure 1, analyzes CD-SEM micrographs or actinic mask micrographs to measure either CDs or through-focus intensity volumes. The software is capable of rotation correction and image registration with subpixel accuracy. The second component analyzes the results from the image viewer for inverse solutions of pupil plane behavior. Both pupil amplitude and phase variation can be extracted using this software. Inverse solutions are obtained through a model based algorithm which is built on top of commercial rigorous full-vector simulation software.

9776-96, Session PSTue

## Screening EUV resists for sub-10nm nodes via EUV interference lithography

Tero S. Kulmala, Michaela Vockenhuber, Yasin Ekinci, Paul Scherrer Institut (Switzerland)

Extreme ultraviolet lithography (EUVL) at 13.5 nm wavelength is considered as the most promising technology for increasing further the resolution in high-volume manufacturing (HVM) of integrated circuits. Still, some challenges need to be overcome before the technique can enter the industrial production phase. One of the main challenges in EUVL is the development of EUV resists that fulfill strict sensitivity, resolution and line-edge roughness (LER) requirements. As the photon flux from current EUV light sources is still insufficient, chemically amplified resists (CARs) where improved sensitivity is achieved via chemical amplification, have thus far been the preferred resist platform. In the meantime, remarkable advances have also been achieved in development of inorganic resists.

Here, we use EUV interference lithography (IL) for investigating the performance of selected resists. In IL, aerial image is created without the limitations of projection optics making it a simple and low-cost technique. As the diffracted beams interfere with each other an aerial image with a period half of that of the original grating is created for first order diffracted beams, enabling patterning at very high resolution. The EUV-IL tool at Paul Scherrer Institute combines the benefits of interference lithography, achieving patterning down to 7 nm half-pitch (HP) and even below, marking the current world record resolution in photolithography.

Using EUV-IL, we have tested a wide range of CARs and inorganic resists in their developmental phase from our collaborators from around the world with the main focus on identifying the most promising materials when moving towards 10 nm HP. We present detailed analysis of the performance of these materials and discuss the observed trends in light of their possible insertion into HVM.

As the patterned feature sizes approach 10 nm HP, pattern collapse due to capillary attraction forces becomes a significant problem. Reducing the thickness of the resist can partially solve this issue but at the expense of an increased LER. Therefore, other approaches that allow for the use of thicker resists capable of meeting the requested LER specifications have to be developed. Here, we present our results on various pattern collapse mitigation techniques that significantly mitigate the issue.

9776-97, Session PSTue

## Energy deposition and charging in EUV lithography: Monte Carlo studies

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EUV photons expose photoresists by complex interactions including photoionization to create primary electrons (~80 eV), and subsequent ionization steps that create secondary electrons (10-60 eV). The mechanisms by which these electrons interact with resist components are key to optimizing the performance of EUV resists and EUV lithography as a whole. As these photoelectrons and secondary electrons are created, they deposit their energy within the resist, creating ionized atoms along the way. Because many photo- and secondary electrons can escape the resist through the surface, resists can become charged. Charging and energy deposition profiles within the resist may play a role in the sensitivity and line-edge roughness of EUV resists.

In this paper, we will present computational analysis of charging-influenced electron behavior in photoresists using LESiS (Low energy Electron Scattering in Solids), a software developed to understand and model

electron-matter interactions. We will discuss the implementation of charge and tracking and the model used to influence electron behavior. We will also present the potential effects of charging on EUV and electron beam lithography by investigating secondary electron blur in charging and non-charging models.

9776-98, Session PSTue

## Non-isotropic shadow effect with various pattern direction in anamorphic high-NA system

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Extreme ultraviolet lithography (EUVL) is the leading lithography technology among the possible next generation technologies. EUV has opened the possibility of high resolution patterning because of very small wavelength of 13.5 nm. Even though EUV lithography has extremely short wavelength source, high numerical aperture (NA) system which is larger than 0.5 is required to make fine patterns with 1X nm and below. For extension of resolution limitation, 0.45 NA illumination system which has 9 degree of incident angle is suggested. However this system has serious telecentricity error and intensified shadow effect such as contrast loss, pattern shift and horizontal-vertical bias (HV bias). In order to avoid reflective efficiency loss and decrease of chief ray angle of incident light, anamorphic high NA is suggested. Suggested anamorphic high NA system has non-isotropic magnification which is varied 4X to 8X and the mask NA shape is ellipse due to non-isotropic magnification distribution (Fig. 1). By taking non-isotropic magnification distribution, 6 degree of incident angle is maintained and half field is achieved not quarter filed.

For anamorphic high NA system, new mask design rule will be required. Owing to non-isotropic magnification, pattern size is dependent on the direction and the angle of diagonal pattern is different between mask and wafer as shown in Fig. 2. Furthermore shadow effect appears differently with pattern direction due to variation of incident angle distribution. For these reasons, we should modify mask design rules as a function of pattern directions.

In this study we will discuss the shadow effect in anamorphic high NA system. We mainly focused on the shadow effect along the various pattern directions. By comparing the patterning results with isomorphic NA system and anamorphic NA system, we will report the non-conventional pattern directivity and the correction of the mask pattern size with various pattern directions for anamorphic high NA system.

9776-99, Session PSTue

## An update on Entegris' EUV pellicle compatible EUV inner pod development

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Traditional photolithography reticles have a pellicle mounted to their pattern side at a distance from the surface to act as a "dust cover" and keep the particles out of focus, so that relatively small particles don't cause lithography defects during pattern transfer to wafers. These pellicles are transparent to the photolithography light. In EUV (Extreme Ultra Violet) lithography on the other hand, the EUV light can be absorbed by most materials. Pellicles of new materials have to be developed for EUV application. Although EUV lithography has been in development for more than a decade now, EUV pellicles are only recently becoming ready for production testing.

The current EUV reticle storage and transport solutions rely only on the EUV pod, which has an all metal inner pod (EIP) comprising of a cover and a baseplate, and an outer pod, to protect the EUV reticles from particle contamination. However, once the reticle is taken out of the EIP inside the lithography chamber, there is no protection, which can result in excessive particle contamination issue.

In 2015 EUV pellicle development at ASML has made significant progress such that it is mature enough for production testing. To support the implementation of the pellicle, the current EIPs needs to be modified to accommodate the addition of a pellicle to the reticle, which primarily involves adding a pellicle pocket to the baseplate of the EIP.

Working closely with ASML, Entegris has developed a pellicle-compatible EUV inner pod (designated as EUV 1008P) which has passed ASML's preliminary testing. Full qualification testing is in progress. This paper presents the key design features of the Entegris EUV 1008P pod, and the testing results.

The none-pellicle EIP baseplate is a flat plate and is designed to be very close the underside (also pattern side) of the reticle to create a particle diffusion barrier to minimize contamination by particles from outside the pod. In EUV 1008P an approximately 2.5mm deep pocket is added to the baseplate to accommodate the pellicle and its frame. For compatibility purpose, the weight of the pellicle-compatible baseplate needs to be kept about the same as the non-pellicle baseplates. Since material is remove on the front side to make the pellicle pocket, same amount of material is added on the backside of the current design by fill some pockets. In addition, a strategic location on the baseplate is chosen where the plate thickness is different between the non-pellicle and the pellicle-compatible versions of the baseplate, so that a sensor in the ASML NXE tool can tell whether it's a pellicle or non-pellicle pod.

In addition to the addition of the pellicle pocket, the Entegris EUV 1008P also has an improved plating on the EIP that can significantly extend its life.

The ASML preliminary tests involved full system cycle test, RH transfer path test, In-system habitat test (venting), and EIP outgas test. The Entegris EUV 1008P samples passed all of the above tests.

9776-100, Session PSTue

## Emulation of scanner illumination using coherent diffractive imaging

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Extreme ultraviolet (EUV) lithography is the most likely successor to deep UV immersion lithography for upcoming technology nodes below 10 nm. One of the major obstacles to tackle remains the realization of mask metrology methods compatible with industry's demand for high-volume manufacturing. Among the proposed methods, scanning coherent diffraction imaging (SCDI) is a promising approach providing various advantages over methods relying on imaging optics.

Regular scanning transmission x-ray microscopy as well as its more advanced imaging methods have in common that their resolution depends largely on the minimally achievable spot size which, in turn, is dependent on the coherence of the incident illumination. In contrast, SCDI methods reconstruct the sample - as well as the incident illumination profile in certain cases – using redundant data gathered from scanning across the sample in small steps. As the achievable resolution with SCDI is not limited by the spot size, it is widely believed that also the degree of coherence of the incoming illumination has only weak influence on the final reconstructed aerial image.

Here, we investigate the effects of varying incident illumination conditions on the modulation transfer function of the reconstructed image. We evaluate the achievable reconstruction quality as a function of the incident illumination applying various filters for partial blocking of the focusing optics (e. g. mimicking a high-pass filter using annular illumination) as well as limiting the detector q-space. Our motivation is to show that SCDI as a lens-less method can mimic the image formation of projection optics. Furthermore, we present an approach to decouple the grid sizes of the optical elements in the simulation that allows an accurate estimation of the achievable resolution of realistic detectors. Our presented model is implemented in a scalable way that runs on any processor architecture, determining the available virtual memory and CPU cores and splitting the calculation in the fastest way possible.

**Conference 9776:**
**Extreme Ultraviolet (EUV) Lithography VII**

9776-101, Session PSTue

## Continuing studies focused on high-resolution contact hole printability

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The drive towards smaller and smaller lithographic patterning, has motivated the development of a number of techniques to overcome the limits of the present semiconductor fabrication technology. It has been shown that ArF immersion lithography, using NTD (Negative Tone Development), can be used to make a contact hole with a minimum feature size of 40nm. EUV lithography has been able to pattern ~25nm contacts. However, published results have shown that patterning those 25nm contacts remains a challenge; exhibiting poor resolution, a small process window and in some cases a degree of ellipticity 1,2. The biggest problem manifests as decreased resolution. There are a number of new approaches focused on solving the resolution problem. Specifically, lithographers have tried to use extension of ArF and EUV lithographic technologies to pattern sub-25nm contact holes. The approaches have included using EUV lithography with a number of contact hole shrink materials such as WASOOM (WAter SOluble Over-coating Material) , RELACS (Resolution Enhancement of Lithography by Assist of Chemical Shrink), and NTO (Negative Tone Over-coating). These, chemistry focused, methods of contact hole shrinking seem to offer the best potential due to their simplicity. At the 2006 Interface Conference, Chun et al, detailed the resolution enhancement photolithography process using WASOOM. They observed 50% CD size reduction without a loss in pattern integrity. The WASOOM process was designed for Positive tone resists., In this paper, we will describe a negative tone contact hole shrink process; which we are calling " Negative Tone Over-coating" or simply NTO; it leverages learning obtained using the WASOOM process.

Reference

1) 2015 Proc. SPIE: Novel processing approaches to enable EUV lithography toward high volume manufacturing.

2) 2014 EUV Symposium, Washington DC, USA : Driving EUV Lithography towards HVM: Joint Project SEMATECH and Tokyo Electron Limited.

9776-102, Session PSTue

## Potential evaluation of sulfonium functionality bearing non-chemically amplified resists for nanopatterning by helium ion-beam lithography (HIBL)

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Recently a library of new radiation sensitive non chemically amplified photoresists have been developed for nanopatterning particularly at sub 20 nm node and beyond. Potential of some of those resist materials have been evaluated using electron beam lithography (EBL) and extreme ultraviolet lithography (EUVL). They have been found to pattern nanofeatures with good resolution and low line edge roughness (LER)/line width roughness (LWR). While chemically amplified resists have been the workhorses in semiconductor industries in the last few decades, it has been projected that they are approaching their limit particularly for sub 20 nm technology largely because of post exposure acid diffusion problem. In this context, non chemically amplified photoresists (nCARs) are expected to overcome those issues, especially the acid diffusion problem as nCARs work without the concept of external chemical amplification.

While EUVL is approaching well into commercialization as one of the most promising high-volume manufacturing lithography tools for sub 20 nm technology, helium ion beam lithography (HIBL) has also garnered interest of researchers mainly for its advantages that include smaller focusing spot, less proximity effects, and hence potentially higher resolution than both EBL and EUVL. It can serve as an adequate research tool for evaluating intrinsic resist performances.

The present work demonstrates an initial performance evaluation of two recently developed non chemically amplified ionic photoresists bearing trifluoromethane sulfonate functionality as radiation sensitive unit in HIBL of patterning nanofeatures. One-dimensional grating patterns of different pitches and line-space ratios are used to cover a design space of future circuit fabrication applications.

9776-103, Session PSTue

## Pattern fidelity optimization focused grating pattern for optical lithography expansion

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Through the continuous scaling, required accuracy of patterning becomes more difficult capability.

The point of gaze in current trend might be the design fidelity and edge placement error (EPE).

In the case of line patterns, it has close relation between the roughness and design fidelity.

Furthermore, controllability of critical dimension (CD), in either case line CD or space CD, is one of the most important parameter. Therefore, the technique of roughness smoothing performed concurrently with improvement of local CD uniformity can be thought of as the effective method.

In this paper, we will report the approach of the improvement of roughness on photoresist pattern including extreme ultraviolet (EUV) and transferred under-layer pattern based on carbon and improvement result of design fidelity mainly focused self-aligned type multiple patterning. We will discuss effective scheme and technique for the smoothing of line patterns and the focal points of the smoothing.

9776-104, Session PSTue

## Toward a contamination-tolerant EUV power sensor

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A reproducible measurement of in-band EUV power over time is essential in EUV lithography, e.g. for dose control, monitoring the transmission of (parts of) the optical path and detecting changes in EUV source performance. However, all currently available sensors suffer from sensitivity degradation over time due to photon-induced contamination and/or structural degradation. For instance, a carbon layer on a sensor surface, as may be deposited during exposure to EUV, inhibits detection of a significant fraction of the EUV power.

To avoid a change of sensor response over time, TNO is developing a carbon-contamination-insensitive EUV power sensor that can operate under typical EUV scanner vacuum conditions. The sensor uses the photo-electric effect to distinguish between in- and out-of-band EUV. The sensor has been tested in the EUV beam line at TNO using a Xe EUV source. Here, we present the latest experimental results, showing the time-resolved response of the sensor to the EUV pulse.

9776-32, Session 8

## EUV resists: What's next? *(Invited Paper)*

Anna Lio, Intel Corp. (United States)

No Abstract Available

9776-33, Session 8

## Benchmarking study of EUV resists for NXE3300

Jun Sung Chun, Mac Mellish, Warren Montgomery, SUNY CNSE/SUNYIT (United States); Cecilia A. Montgomery, Yu-Jen Fan, SUNY Poly SEMATECH (United States)

Since we agree carefully that EUV is getting closer to HVM soon with NXE3300, accordingly, production worthy materials such as photoresist and etch process should be ready for that environment. CNSE of SUNY Polytech associated with SUNY Polytech SEMATECH have supported fundamental research program for EUV resist materials and various EUV resist evaluation work over the years1~4. With the program, we could accumulate meaningful data for the industry to understand the general trend of EUV photoresist development over the years. The accumulated data could be utilized as a point of reference and could guide to the right way for the EUV photoresist development.

Discussions indicate that the use of EUV lithography with NXE3300 would be at the contact layer initially and then line and space patterns.

In this paper, latest data from recent benchmark study including smoothing process, chemical trick for shrink and post-etch from NXE3300 will be discussed.

Reference

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2. Jun Sung Chun et al., " SEMATECH's Cycles of learning test for EUV photoresist and its applications for process improvement" PROC. SPIE 2014

3. Cecilia Montgomery, Jun Sung Chun, Yu-Jen Fan, Shih-Hui Jen, Mark Neisser, Kevin Cummings, Warren Montgomery, Takashi Saito, Lior Huli, David Hetzer, Hiroie Matsumoto, Andrew Metz and Vinayak Rastogi "Novel Processing Approaches to Enable EUV Lithography toward High Volume Manufacturing", 2014 International Symposium on Extreme Ultraviolet Lithography, Washington DC, USA.

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9776-34, Session 8

## Process development of 'metal resist' for EUV lithography

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Extreme ultraviolet lithography (EUVL) which extends photolithography to extreme short wave length (13.5nm) is capable of achieving sub-20 nm half pitch resolution by single exposure. Therefore, EUV lithography is the leading candidate to succeed 193nm immersion lithography. However, Resolution, Line Width Roughness (LWR) and Sensitivity (RLS) trade-off is still a significant issue for EUV resists. We have evaluated the EUV resist characteristics and lithographic performance using the several analysis tools and the small-field exposure tool (SFET) and EB exposure tool for fundamental study for breaking the deadlock of this trade-off. One possibility to break thorough the trade-off relationship is the employment of metal resist. Non-CAR type metal resist does not depends on acid amplifying, and several metal resist showed very high sensitivity compared to conventional EUV resist [1-4]. Metal resist has a potential for high sensitivity to EUV dose because of high EUV absorption, and this character enable high through-put EUV lithography. Another notable character is high etching resistance and this allows higher resolution by thinner resist thickness.

In this work metal resist was developed for advanced patterning. The resists shows significantly high sensitivity (8mJ/cm2) and fine pattering (22nm 1:1 L/S) by EUV lithography (Figure 1). Further investigation for higher sensitivity and better resolution is in progress. A distinctive feature of metal resist is it has high etching resistance, and the character is the large advantage for etching resistance. Metal resist was investigated on several underlayers, and not only lithography performance but also etching mask property is also reported, and the metal resist is confirmed to have high etching resistance (Figure 2). Further investigation of metal resist dissolution study, shelf life study and metal contamination test are under progress.

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9776-35, Session 8

## Patterning performance of chemically amplified resist in EUV lithography

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Extreme Ultra Violet (EUV) lithography is one of the most promising candidate technologies for the high-volume manufacturing (HVM) of semiconductor devices for 7 nm node and beyond. This industry has faced issues such as manufacturing cost and overlay/ edge placement error accuracy by extending current optical lithography (193 nm immersion) with multiple patterning so far. EUV lithography is expected to be replaced from current lithography and solve these issues at 7 nm node by its resolution and process simplification. [1-2] One of the major challenges for EUV lithography is through-put to be able to apply it for HVM. Steady progresses in source power have been achieved in recent years, but further improvement of through-put seems needed for HVM. [3] Therefore, EUV resists which show fast enough photo speed are strongly required to overcome its challenge. It is well known that relationships between resolution (R), line width/ edge roughness (L) and sensitivity (S) are trade-off one. [4] To improve sensitivity, resolution and roughness need to be potentially improved at the same time for overcoming the trade-off and satisfying requirements for HVM. In chemically amplified (CA) systems, increasing acid generation efficiency as much as possible is essentially important. The acid generation mechanism in CA resists upon exposure to EUV was reported. [5-6] To increase acid generation efficiency, increasing proton generation is needed. 4-Hydroxystylene (HSt) is especially well known as a good proton source. Additionally, acid diffusion control and protecting group (PG) reaction during post exposure bake (PEB) process are the most important factor for improving lithographic performance. [7] To improve resolution, acid diffusion length has to be controlled to suppress chemical blur, however, it causes a decrease in the efficiency of de-protection reaction and resulting in sensitivity loss. Hence, the enhancement of PG reaction under the acid diffusion control is needed.

In this study, acid generation efficiency as function of HSt content in polymer was investigated by acid titration method in which Coumarin 6

derivative was used as indicator. [8] As a result, acid generation efficiency increased without saturation by increasing HSt content from 0% to 100%. This result suggests that maximization of proton source in resist formulation is effective to enhance acid yield and de-protection reaction efficiency at exposed area. Resist polymer generally contains PG unit, adhesion unit and Tg enhancer unit, so optimization of each unit ratio is needed when proton source is introduced to polymer. CA Resist-A was developed by combination of shorter diffusion length PAG and maximized HSt content. Figure 1-a showed the exposure result of Resist-A on Paul Scherrer Institute (PSI). Resist-A resolved 15 nm hp at 36.0 mJ/cm2. Additionally, Resist-B was developed by introducing low activation energy (Ea) PG based on Resist-A. Figure 1-b, c showed that Resist-B resolved 15 nm and 13 nm hp at 32.8 mJ/cm2. Experimental results on CA resist will be shown to study the influence of proton source and the other materials on lithographic performance, and then resist formulation designed for maximizing de-protection reaction efficiency and improving RLS trade-off will be discussed.

9776-36, Session 8

## Sensitivity enhancement of chemically amplified resist and evaluation using EUV interference lithography

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Extreme ultraviolet lithography (EUVL, λ = 13.5 nm) still is the most promising candidate to manufacture electronic devices for future technology nodes in the semiconductor industry. Nonetheless, EUVL has faced and continues to face many technological challenges as it moves toward high-volume manufacturing (HVM). A key bottleneck from the tool design and performance point of view has been the development of an efficient, high power EUV light source for high throughput production. Consequently, there has been extensive research on different methodologies to enhance EUV resist sensitivity. Ito H. et al., [1] introduced the chemical amplification concept (by means of an acid catalyst) for the first time in the early 1980's. Since its inception, chemical amplification has been the base upon which state-of-the art photoresist technology has been continuously designed and developed. Resist performance is measured in terms of its ultimate printing resolution, line edge roughness (LER), sensitivity (S or exposure dose) and exposure latitude (EL). Nonetheless, there are well known fundamental trade-off relationships (LRS trade-off) among these parameters. We have investigated a method that has the potential for super high sensitivity enhancement without compromising other important performance characteristics. In this article we have evaluated the performance of different state-of-the art EUV CARs with the aim of resolving features of 13 nm half-pitch (HP). While the availability of high resolution EUV exposure tools for resist research and development has been limited due to its high cost, EUV interference lithography (IL) has provided a simple yet powerful platform for academic and industrial research to occur in the meantime. With EUV IL, high resolution periodic images can be printed by the interference of two or more spatially coherent beams through a transmission-diffraction grating mask [2, 3]. For this reason, our experiments have been performed by EUV-IL at Swiss Light Source (SLS) synchrotron facility located at the Paul Scherrer Institute (PSI) [4] using an additional process step.

9776-37, Session 8

## EUV extendibility via dry development rinse process

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Ultimate resolution improvement via pattern collapse (PC) mitigation in EUV lithography by 0.25NA EUV full field scanner exposure tool has been demonstrated by applying the dry development rinse process (DDRP) [1]. Selection of photoresist material is crucial for line-width-roughness (LWR) performance, while the cross-sectional profile being the most critical factor [1,2]. In this contribution, we report the impact of the photoresist thickness increase as a viable option towards improving LWR without compromising sensitivity due to PC mitigation by DDRP. Further, we present the extendibility of EUV lithography combining DDRP and 0.33NA EUV full field scanner exposure tool beyond 13 nm LS half-pitch. Some aspects of DDR material compatibility for high volume manufacturing will also be discussed.

9776-38, Session 9

## The reaction mechanism and patterning of photosensitized chemically amplified resists

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In EUV lithography (EUVL), the most critical issue has been low intensity of the EUV light source.

Light-source intensity and resist sensitivity have a complementary relationship. Therefore, the sensitization of EUV resist is very important to compensate the low intensity of the EUV light source.

However, dramatically improving the resist sensitivity of chemically amplified resist (CAR) is very difficult because of so-called trade-off relation among the resolution, line-width roughness, and sensitivity. Therefore, we propose a very new process: high resist sensitization by the combination lithography of EUV pattern exposure with UV flood exposure (PF combination lithography) of photosensitized chemically amplified resist (PS-CAR). Rough patterning processes and experimental results of the combination lithography of EB pattern exposure with UV flood exposure of PS-CAR have been reported since 2013. The present paper describes the detailed reaction mechanisms and less than 20 nm dense contact hole patterning of PF combination lithography of PS-CAR for high volume manufacturing. Especially the relation of resist sensitization with resolution and roughness of PS-CAR is discussed based on experimental results and reaction mechanisms.

9776-39, Session 9

## Measurement of dynamic absorption coefficients of CAR and non-CAR resists at EUV

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Recently, a new class of metal oxide based resists is being developed

for EUV lithography. In these materials, the large atomic absorption cross section of the metal brings the advantage of a significantly higher absorbance and secondary electron yield. Among other benefits, such properties are expected to bring a substantial reduction in photon shot noise. Accurate modeling of the chemical, physical, and lithographic process requires the knowledge of the photoresists' absorption coefficients, both the unbleachable and bleachable components (Dill A & B parameters).

In this work we measured experimentally the Dill A & B absorption parameters of several photoresists at EUV (13.5 nm) at the XIL beamline of the Swiss Light Source. The following resists were studied: poly-(methyl methacrylate), hydrogen silsesquioxane, three chemically amplified resists and two metal oxide based resists. We performed the experiments by spin coating the resists onto a semi-transparent silicon nitride membranes of ≈ 100 nm thickness and measured the reduction in transmittance using a photodiode.

In this experiment, determining the film thickness is the major source of uncertainty on the absorption coefficients. We developed a methodology to measure the thickness of the resists spin-coated onto the transparent membranes by optical ellipsometry. Our model provides the most accurate estimation of the resist thickness and it has the advantage to analyze the thickness on the same area that was actually exposed. Because the membrane also absorbs part of EUV light, we calibrated the net flux across a blank membrane. The variability of membrane thickness was also taken into account by measuring several blank membranes.

It was found that for all EUV resists the bleachable A coefficient is positive but much smaller than the non-bleachable coefficient B. The absorption coefficient of the metal oxide based resists was found to be ≈ 17 ± 3 μm^-1, while the CAR resists were ≈ 5 and 3 μm^-1. The absorption of PMMA was found to be 5.8 μm^-1, in agreement with previous studies. PMMA was the only resist to have a relatively large A coefficient, among those analyzed in this study. In conclusion, the presence of metallic core increases the absorption by as much as 4 times relative to conventional CAR resists. The high absorption is expected to enable high sensitivity without chemical amplification and to reduce photon shot noise, which are the key benefits offered by metal-containing photoresists for EUV lithography.

9776-40, Session 9

## Effects of acid diffusivity on line-edge roughness in extreme-ultraviolet chemically amplified resist pattern

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Extreme-ultraviolet lithography (EUVL) is one of the next generation lithography technologies for the accomplishment of 16 nm patterning. One of the most significant problems for the mass production is reducing the line edge roughness (LER) on chemically amplified resist (CAR) pattern. LER, however, cannot be controlled easily because the factors affecting LER are various and related each other such as aerial image quality, post exposure bake process environment, acid diffusion phenomenon, and so on. Many researchers have been studied the LER of CAR pattern using Monte-Carlo simulation based on normal random walk, which is usually described by the Gaussian distribution, ignoring the interactions between acidic molecules and with medium. The acidic diffusion process through resist medium should be considered more precisely for better understanding of LER phenomenon. In order to investigate LER correctly, we develop a Monte-Carlo simulation which considers the random walk with atomic interactions. When the intermolecular interaction is considered, the diffusion type is decided with interaction force such as attraction and repulsion. Figure 1 shows a relation between mean square distance (MSD) and time step with three different diffusion types. The MSD of the normal diffusion increases linearly, but others increase with a certain power. Through the extensive Monte-Carlo simulation, we investigate the effects of acid diffusivity on LER and how interaction types change the LER quantitatively.

9776-41, Session 9

## Optimization and sensitivity enhancement of high-resolution molecular resist for EUV lithography

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The International Technology Roadmap of Semiconductors (ITRS) has EUV lithography as one of the most promising candidates in replacing current integrated circuit manufacturing processes for the transition to future technology nodes. However unresolved issues still remain - such as low available source power. Using a much shorter wavelength for patterning has made the development of new photoresist platforms necessary, a challenging task in itself. Significant research into new materials has been undertaken, but to date no resist has been able to simultaneously meet all the specifications laid out in the roadmap. In addition to fulfilling the current resist targets for the next generation of devices, new material platforms must also have the potential to meet the outlined specifications beyond that point to ensure a useful lifespan for next generation lithography. Recently interest in novel metal-based resist materials has increased as a possible route to improved sensitivity at high resolution. But concerns about integration of all-metal resists still persist.

Our work focuses on the development of an organic molecular resist for EUV application, which has previously demonstrated 14 nm half-pitch (hp) resolution at moderate doses ~ 30 mJ/cm2. We will report on our progress in improving the patterning performance of this material class through optimization of the process conditions as well as improvements in resist formulation and synthesis. We show patterning at the Paul Scherrer Institute (PSI) interference lithography tool down to 11 nm hp with improved contrast compared to previous results. As the patterning dose for a resist typically goes up as the feature size goes down we are also developing sensitivity-enhancing additives with little impact on the pattern quality of the material. Addition of ~5 % of one of the sensitizers was seen to lower the dose-to-size by as much as 25 %. In this way it is possible to stabilize the patterning dose while moving to smaller line widths.

9776-42, Session 10

## Novel EUV mask black border and its impact on wafer imaging

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EUV lithography is the most promising technology for semiconductor device manufacturing of the 10nm node and beyond. The EUV mask is a key element in the lithographic scanner optical path. The image border is a pattern free dark area around the die on the photomask serving as transition area between the parts of the mask that is shielded from the exposure light by the Reticle Masking (REMA) blades and the die. When printing a die at dense spacing on an EUV scanner, the reflection from the image border overlaps edges of neighboring dies, affecting CD and contrast in this area. This is related to the fact that EUV absorber stack reflects 1-3% of actinic EUV light. To reduce this effect several types of image border with reduced EUV reflectance (<0.05%) have been proposed; such an image border is referred to as a black border. In particular, an etched multilayer type black border was developed; it was demonstrated that CD impact at the edge of a die is strongly reduced with this type of the black border (BB). However, wafer printing result still showed some CD change in the die influenced by the black border reflection. It was proven that the CD shift was caused by DUV Out of Band (OOB) light which is emitted from the EUV light source.

New types of a multilayer etched BB were evaluated and showed a good potential for DUV light suppression.

In this study, a novel BB called 'Hybrid Black Border' (HBB) has been developed which allows to eliminate EUV and DUV OOB light reflection. A new test mask with HBB is fabricated. Direct measurements of OOB light from HBB and BB are performed on NXE:3300 ASML EUV scanner; it is shown that HBB OOB reflection is ~3x lower than that of BB. Imaging performance is also demonstrated on NXE:3300 system for N10 imaging structures 16nm dense lines and 20nm isolated spaces. These results are compared to the imaging results obtained for a mask with the earlier developed BB and ~2x improvement is achieved; less than 0.2 nm CD changes are observed in the corners of the die. A CD uniformity budget including impact of OOB light in the die edge area is developed which shows that the OOB impact from HBB becomes comparable with other CDU contributors in this area. Finally, we state that HBB is a promising technology allowing for CD control at die edges.

9776-43, Session 10

## EUV and optical lithographic pattern shift at the 5nm node

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At the 5 nm node there are competing strategies for patterning: high-NA EUV, double patterning low-NA EUV and a combination of optical SAQP and EUV. This paper investigates the impact of pattern shift based on the patterning strategy chosen. A logic standard cell from PC to M1 is simulated to determine the impact of lithographic pattern shift on the overlay budget. At 5 nm node dimensions, high-NA EUV is necessary to expose the most critical layers with a single lithography exposure. The need for high-NA EUV lithography is illustrated by comparing the pattern shift resulting from 0.33 NA vs. 0.52 NA. For the example 5 nm transistor, cost-beneficial lithography layers are patterned with EUV and the other layers are patterned optically. Both EUV and optical lithography simulations are performed to determine the maximum net pattern shift. Here, lithographic pattern shift is quantified in terms of through focus error (TFE) as well as pattern placement error (PPE). The phenomenon of pattern shift is not unique to EUV lithography, though it is more severe than in optical lithography due to the reflective optics imaging system. The overlay error associated with an optical patterning scheme is compared with the results of an EUV solution, providing an assessment of each patterning solution and its impact the overall overlay budget.

9776-44, Session 10

## Polarization aberrations induced by graded multilayer coatings in EUV lithography scanners

Thiago S. Jota, Russell A. Chipman, The Univ. of Arizona (United States)

The functional form of coating-induced polarization aberrations is evaluated in a class of EUV lithography systems through an example 4X EUV scanner with state-of-the-art, graded multilayer coatings (Si/C/Mo/C stacks with a Titanium Dioxide capping layer). Graded thickness multilayer coatings are unavoidable solutions for a high-throughput optical path over the range of angles of incidence at each mirror. The polarization effects of these coatings on the point spread function (PSF) are analyzed using the Polaris-M polarization ray tracing code from the University of Arizona. The image has a brighter s-polarized component and astigmatic effects are brought by the polarized wavefronts. In particular, the impact of coating-induced on-axis astigmatism, as well as diattenuation and retardance on image quality are investigated. The PSF of a partially or unpolarized source consists of the linear superposition of four polarization-dependent components, two which are nearly diffraction limited and two which are highly apodized, all of which can be described by a Mueller matrix Point Spread Matrix (PSM). The highly apodized PSM components are "ghost" images that are larger than the diffraction limit. Thus, the coatings reduce resolution by spreading the spatial extent of the encircled energy and are spatially shifted, reducing image contrast, justifying concern regarding coating-induced polarization effects.

9776-45, Session 10

## Image-based pupil plane characterization via principal component analysis for EUVL tools

Zac Levinson, Andrew Burbine, Rochester Institute of Technology (United States); Erik A. Verduijn, Obert R. Wood, Pawitter J. Mangat, GLOBALFOUNDRIES Inc. (United States); Kenneth A. Goldberg, Markus P. Benk, Antoine J. Wojdyla, Lawrence Berkeley National Lab. (United States); Bruce W. Smith, Rochester Institute of Technology (United States)

Pupil plane phase characterization has played a critical role in image process optimization over several lithography generations. The criticality of pupil characterization continues into EUV lithography (EUVL) with an additional importance placed on understanding the ways that the pupil variation evolves during system operation. Interferometric methods are the de facto standard of pupil phase metrology but can be challenging to implement during tool use in an EUVL system. In addition, we have previously shown that amplitude pupil variation in EUV imaging systems can be non-uniform. In this talk, we will present an approach to image-based pupil plane amplitude and phase characterization using models built with principal component analysis (PCA). PCA is a statistical technique to identify the directions of highest variation (principal components) in a high-dimensional dataset. A polynomial model is constructed between the principal components of through-focus intensity for the chosen binary mask targets and pupil amplitude or phase variation, as seen in Figure 1. This method separates model building and pupil characterization into two distinct steps, thus enabling rapid pupil characterization following data collection. The pupil plane variation of several zone-plate lenses from the Semiconductor High-NA Actinic Reticle review Project (SHARP) at Lawrence Berkeley National Laboratory will be examined using this method. Results will be compared to pupil plane characterization using a previously proposed methodology where inverse solutions are obtained through an iterative process involving least-squares regression.

9776-46, Session 10

## Improved Ru/Si multilayer reflective coatings for advanced extreme-ultraviolet lithography photomasks

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Extreme ultraviolet (EUV) lithography with reflective photomasks continues to be a potential patterning technology for high volume manufacturing at the 7 nm technology node and beyond. EUV photomasks with alternative materials to the commonly used Mo/Si multilayer (ML) reflector and

patterned Ta-based absorber (both of which are known to require shadow effect corrections and lead to large through-focus pattern placement errors) are being actively explored. Because the reflective bandwidth of a Ru/Si ML is significantly wider than the reflective bandwidth of a Mo/Si ML and the effective reflectance plane in Ru/Si is closer to the ML surface, Ru/Si ML coatings may be viable alternatives to the Mo/Si ML coatings that are commercially available today. In this paper, improvements in the peak reflectivity and the reflective bandwidth of Ru/Si ML reflectors with B4C interlayers to sharpen the Ru-Si interfaces are discussed.

Just as is the case with the Mo/Si ML coatings that are present on nearly all EUV reflective optics today, the width and roughness of the metal-Si interfaces play a large role in determining the performance of Ru/Si ML coatings. Information on Ru-Si interfaces for this paper was obtained by depositing Ru/Si ML coatings on Si wafers in low pressure Ar gas using a commercially available PVD tool with surprisingly good defectivity performance and characterizing those coatings using x-ray reflectivity (XRR), x-ray diffraction (XRD), atomic probe tomography (APT), cross-sectional transmission electron microscopy with electron energy loss spectroscopy (XTEM/EELS), and with EUV reflectometry. All of the Ru/Si ML coatings were designed to have a Si layer at the bottom of the film stack and a Ru layer at the top of the film stack, to have a multilayer period of ~70.2 Å to provide maximum reflectivity at 13.5 nm wavelength in the presence of ML period contraction, and to have a total of 20 bilayers.

XRD showed that the Ru and the B4C layers tended to be polycrystalline whereas the Si layers were amorphous and that the Ru layers tended to have (002) texture in both Si/Ru and Si/B4C/Ru samples. XRR was used to determine the ML period with sub-Å accuracy and provided accurate numbers for the ML period contraction that took place as the Ru-Si and Ru-B4C-Si interfaces were formed. Both the ML period contraction values and data from the EELS scans of the interfaces were used to determine the optimum the B4C interlayers thicknesses. As is the case with Mo-Si, the metal-on-Si interlayers were found to be significantly wider than Si-on-metal interlayers. The optimum B4C interlayer thicknesses occur where the increase in the EUV reflectance due to the sharper Ru/Si interfaces when B4C interlayers are present and the decrease in reflectivity due to the higher net EUV absorption losses when B4C layers are present are in balance (see figure on the left). With values of total B4C thickness in the 5 – 10 Å range, Ru/Si ML films with engineered interfaces are found to have a wider reflective bandwidth and a higher peak reflectivity (see figure on the right) and are expected to have improved long term stability when exposed to humidity and to elevated temperatures. These and the other conclusions of the paper will be supported with both experimental measurements and rigorous simulations.

9776-47, Session 11

## Actinic review of EUV masks: Performance data and status of the AIMS EUV System

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The EUV mask infrastructure is of key importance for the successful introduction of EUV lithography into volume production. In particular, for the production of defect free masks, actinic review of potential defect sites is required. Such review can determine whether a defect prints, and if it needs to be repaired or compensated for. It also serves as verification for the repair or compensation process performed with the MeRiT® electron beam repair tool, thereby providing a closed loop mask repair solution. ZEISS and the SUNY POLY SEMATECH EUVL Mask Infrastructure consortium started a development program for an EUV aerial image metrology system, the AIMS™ EUV for the realization of actinic mask review.

In this paper, we provide an update on the program and the system qualification status. We will show measurement data on the system's key specifications and discuss its performance and capability status.

9776-48, Session 11

## Fourier Ptychography imaging for the study of EUV lithography photomasks

Antoine J. Wojdyla, Markus P. Benk, Kenneth A. Goldberg, Lawrence Berkeley National Lab. (United States)

The reflective nature of the imaging mode in extreme ultraviolet (EUV) lithography makes it highly sensitive to phase defects on photomasks and speckle due to the roughness of the substrate. Moreover, the advancing high resolution of mask patterning calls for extended resolution and higher demands on inspection tools. Non-interferometric, actinic imaging techniques offering high-resolution at-wavelength are of great interest for research and the industry.

Fourier Ptychography (FP) is an emerging imaging technique [1] that allows the reconstruction amplitude and phase of an object, based on a set of coherent, real-space images acquired with different illumination angles. SHARP is a synchrotron-based EUV mask-imaging microscope designed to emulate the imaging properties of EUV lithography tools, [2] and it is the first short-wavelength microscope to enable FP. We have analyzed a wide variety of samples, to demonstrate quantitative phase imaging and increased resolution, and we have gathered a wide collection of mixed amplitude and phase defects. This provides unique information for defect repair and gives us a more complete understanding of the underlying optical phenomenon that occur in advanced photomask designs than conventional imaging allows.

We have also assessed the validity of the results quantitatively, e.g. by comparing FP reconstructions to through-focus data, incoherent imaging, other phase-retrieval techniques or non-optical techniques such as scanning electron microscopy or atomic-force microscopy. Data collection for FP requires a comparable number of images as through-focus data collection on SHARP. Compared to conventional ptychography, based on diffractograms and which has been adapted to EUV lithography [3], Fourier Ptychography relies on real-space images, what allows live navigation over the sample to search and locate defects.

Computing the full, complex-valued angular spectrum of the object opens up new possibilities for the study of image formation based on real mask data. It enables the study of illumination synthesis for source-mask optimization, the study of the influence of the numerical aperture to emulate the imaging properties of anamorphic lenses, and the study of sub-resolution assist and OPC features used to improve imaging metrics.

[1] G Zheng et al. "Wide-field, high-resolution Fourier ptychographic microscopy" Nature Photonics 7, 9 (2013)

[2] K A Goldberg et al. "Actinic mask imaging: Recent results and future directions from the SHARP EUV Microscope" Proc. SPIE 9048 (2014)

[3] S Lee et al. "A novel concept for actinic EUV mask review tool using a scanning lensless" Proc SPIE 9048 (2014)

9776-49, Session 11

## EUV mask and wafer defectivity: Strategy and evaluation for full die defect inspection

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It was reported in a recent study that EUV Mask defect printability on wafer has a non-linear trend and as a result of post-exposure processing effects their dimensions are much larger than predicted from optical simulations. Due to reflective nature of the mask and unavailability of a pellicle, a comprehensive strategy to monitor defectivity on mask and wafer is

required for implementing EUV Lithography in High Volume Manufacturing. In this work we assess various strategies for mask and wafer defect inspection including a two-fold solution to leverage resolution of e-beam inspection along with the speed of optical inspection. Defect capture rates for inspections based on full-die area, critical areas based on priority and hotspots based on design and prior inspection data are evaluated. Each strategy has merits and de-merits, mainly throughput, effective die coverage and computational overhead. Design errors, pattern defects and surface defects are captured through optical mask inspection post EUV mask fabrication. An approximate signature of buried defects can also be captured by mask optical inspection as well as wafer based inspections. This information can help mask known defect locations to filter out process and mask use added defect data. As initial mask qualification requires the need for complete defectivity information, we use e-beam mask and wafer defect inspection to qualify the mask, also leveraging optical mask defect inspection. This creates an initial reference state for the mask. Once the mask is qualified for use, an optical wafer inspection tool is utilized to monitor defectivity on the mask by inspecting patterned wafers.

9776-50, Session 11

## Enhancing defect sensitivity by pupil optimization for EUV actinic mask inspection

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For EUV mask infrastructure to be ready, inspection tool is needed to identify critical defects which will deteriorate the image quality on the wafer. In order to reduce position error of critical defects and meet the tighter requirement on defect size for future technology nodes, high defect sensitivity is needed for actinic inspection tool to solve these issues. In our previous study [1, 2, 3], we proposed to utilize Zernike phase contrast microscopy to improve phase defect sensitivity on the EUV mask blank. However, in reality, most of the defects on patterned mask or mask blank possess both phase and absorption component. Thus conventional 90-degree phase shift Zernike phase contrast microscopy cannot maximize defect sensitivity for most real world defects. To address this shortcoming, we study the impact of phase and amplitude function optimization for blank and patterned mask inspection by simulation and experiment.

As previously reported, a comprehensive experiment study on a programmed phase defect mask shows a significant improvement on defect sensitivity at focus by implementing a 90° phase shift in the pupil plane [3]. However, for the 55 nm programmed defect which has a 1 nm height and FWHM of approximately 40 nm on the surface of the mask blank [4], the peak signal is not at the best focus position and it causes a 20% drop from peak value as shown in figure 1. Based on the defect information retrieved from through-focus images [5], the defect has both phase and absorption components. Therefore, the ideal 90° phase shift in the pupil plane is not the optimum design for this defect. As shown in figure 2, the simulation results indicates that the peak defect signal of the 55 nm program defect is at focus with optimized phase shift close to 117°.

Moreover, noting that optimized phase shift also maximizes defect signal, this approach further improves the measurement signal to noise ratio by preferentially boosting the signal relative to the noise. In figure 3a, the trends of speckle noise vary with different phase shifts in the pupil plane. As shown in figure 3b, the speckle noise at focus drops 11% from the ideal Zernike phase contrast method and the combination with increased defect signal will give you a total 14% improvement on its signal-to-noise ratio (SNR) while using 117° phase shift.

To apply this method to both blank and patterned mask inspection, we will study the impact of optimum phase shift on various types of defect by simulation and experiment using customized zoneplate design on the SHARP EUV microscope at Lawrence Berkeley National Laboratory (LBNL).

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9776-51, Session 11

## EUV patterned mask inspection performance of an advanced projection electron microscope (PEM) system for 11nm half-pitch (hp) generation

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Extreme Ultraviolet Lithography (EUVL) stands at the foremost next-generation lithographic technology after the ArF immersion lithography has reached its limit to deliver smaller features. High-sensitivity EUV mask pattern defect detection is one of the major issues in order to realize the device fabrication by using the EUV lithography. According to the ITRS2013 and defect printability simulations the sensitivity requirement for an EUVL patterned mask inspection system is to be better than 13 nm for hp 11 nm node devices. We have already designed a novel Projection Electron Microscope (PEM) optics that has been integrated into a new inspection system named EBEYE-V30 (“Model EBEYE” is an EBARA’s model code) , and, which seems quite promising for hp 16 nm node EUVL patterned mask inspection. A learning system has been exploited for the mask inspection tool to meet the requirement for hp 11 nm node EUV patterned mask inspection. The defect is identified by the PEM system using the “defectivity” defined as a calculated number in the direct product space of the characteristics of the acquired image. An appropriate adjustment for the contribution of each characteristic determines the value of the defectivity, the latitude of detection capability. The process to optimize the each contribution for the newly defined defect, for a new product series of masks, requires great labor. The learning system has been developed to reduce the labor and the cost to adjust the detection capability to cope with the newly defined mask defect. The learning system fully optimizes the detection capability reconciling the previously registered defects and the newly registered defect. To improve the inspection throughput for 11 nm hp generation defect detection, it would require a data processing rate of greater than 1.5 Giga-Pixel-Per-Second (GPPS) that would take less than eight hours of inspection time. For a higher throughput and higher defect detection sensitivity, new electron-sensitive area image sensor with high-speed data processing unit, bright and stable electron source and simultaneous deflector of image capture area to the mask scanning motion are developed. As a result of the synchronous deflection with mask scanning, the image can be integrated into the fixed area image sensor as well as the TDI image sensor.

In this paper, we describe the experimental results of the EUVL patterned mask inspection using the above- mentioned system. We have verified the effectiveness of the learning system. We registered the captured image of the defect on hp 11 nm mask in the learning system previously optimized for hp 16 nm, and obtained the enhanced detection capability for hp 11 nm. Developing elements’ integration to the inspection tool and verification of the designed specification has been conducted.

This study is supported by New Energy and Industrial Technology Development Organization (NEDO) and Ministry of Economy, Trade and Industry (METI).

9776-52, Session 11

## Scanning coherent diffractive imaging methods for actinic EUV mask metrology

Patrick Helfenstein, Istvan Mohacsi, Yasin Ekinci, Paul Scherrer Institut (Switzerland)

For the successful implementation of extreme ultraviolet (EUV) lithography in the 10 nm technology node and beyond, a major challenge to overcome is the stable and reliable detection of mask defects. We recently presented a reflective mode EUV mask scanning lens-less imaging tool (RESCAN) installed at the XIL-II beamline of the Swiss Light Source and showed reconstructed aerial images of test patterns on EUV masks. RESCAN uses scanning coherent diffraction imaging (SCDI) methods to obtain actinic aerial images of EUV photomasks and was designed for 20 nm on-wafer resolution. Our SCDI algorithm reconstructs the measured sample by iteratively solving the phase-problem using overdetermined diffraction data gathered by scanning across the specimen with a finite illumination. Contrary to scanning transmission x-ray microscopy and similar techniques, the achievable resolution with our method is not limited by the spot-size – and therefore the coherence on the incoming illumination – but rather on the detector noise and NA. To increase the reconstruction quality, we upgraded RESCAN with a new detector and optics.

Here we discuss the results gathered with the upgraded version of RESCAN that is capable of up to 10 nm on-wafer resolution. Additionally, we have developed methods to evaluate the theoretical resolution of RESCAN and compare this to the experimental data.

We believe that the realization of our prototype marks a significant step towards overcoming the limitations imposed by methods relying on imaging optics and shows a viable solution for actinic mask metrology.

9776-53, Session 11

## Advances in the detection capability on actinic blank inspection

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Extreme ultraviolet lithography (EUVL) is a promising technology for ultra-large-scale integration devices with a half-pitch of 16 nm and beyond. However, the fabrication of defect-free mask blanks and their inspection pose great challenges in the implementation of EUVL. In a multilayer, a phase defect is initiated by a certain imperfection that is generated during film growth where impurity particles or vacancies happen to reside on a substrate surface. Such defects, if buried within the multilayer, are difficult to notice using conventional inspection tools. An alternative technique, an actinic blank inspection (ABI), is being pursued to address this issue. A full-field ABI verification tool (MIRAI-tool) employing dark-field imaging was developed by Selete and EIDEC. Based on a high-volume manufacturing (HVM) feasibility study performed with the MIRAI-tool, a HVM ABI prototype has been developed by EIDEC and Lasertec. In both tools, light scattered from a mask blank surface reaches a sensor in a CCD camera, where the defect is captured in images as a bright spot against a darker background, which is attributed to light scattered from the rough surface of the mask blank. The two systems can detect a defect when the signal intensity is larger than a pre-set threshold. From evaluation results with programmed phase defects, the HVM ABI prototype could detect a printable phase defect for a 16-nm node with almost 100 % capture rate. Among the native defects detected by this prototype, almost half of the defects were smaller than 20 nm in a sphere equivalent diameter but printable. To detect such a small printable defect is a key advantage of ABI. However, although printable phase defects of aspect ratio under 0.01 were merely existed, they could not be detected by the HVM ABI prototype. To understand this, reflected and scattered light from a low-aspect printable phase defect were analyzed. The result showed that an enlargement of the illumination numerical aperture (NA) of the HVM ABI prototype was found to enhance the signal intensity of low-aspect phase defects. With an enlargement from 0.07 to nearly 0.1, the signals of low-aspect phase defects became quite apparent. This showed that all of the printable phase defects for a 16-nm node could be detected by the HVM ABI prototype.

In this presentation, the latest development status of the HVM ABI prototype is reported and the outlook of its readiness will be discussed.

This work was supported by New Energy and Industrial Technology Development Organization (NEDO) and Ministry of Economy, Trade and Industry (METI).

9776-54, Session 11

## Through-pellicle defect inspection of EUV masks using an ArF-based inspection tool

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The use of EUV photomasks in a semiconductor manufacturing environment requires their periodic inspection to ensure they are continually free of defects that could impact device yield. Defects can occur from fall-on particles or from surface degradation such as “haze”. The proposed use of a polycrystalline silicon-based EUV pellicle to prevent fall-on particles would preclude periodic through-pellicle inspection using e-beam, as well as DUV inspection tools (pellicle is opaque at DUV wavelengths). Thus, to use these types of inspection tools would require removal of the EUV pellicle before inspection. After inspection, the pellicle would need to be re-attached and the mask re-qualified using a test wafer, thus causing expense and delays. While EUV-wavelength inspection tools could inspect through such a pellicle precluding the need to remove the pellicle, such tools are not likely to be available in the commercial marketplace for many years. An alternate EUV pellicle material has been developed that is semi-transparent to DUV wavelengths, thus allowing through-pellicle inspection using existing ArF-based mask inspection tools. This eliminates the requirement to remove the pellicle for inspection. In this work, we will evaluate the performance of an existing ArF-based mask inspection tool when inspecting patterned EUV reticles through such a semi-transparent pellicle. The evaluation will include such performance factors as defect detection sensitivity, false detection rates, throughput, and membrane impact. Further, we will report on the expected future performance of such an inspection system after proposed modifications to optimize performance for such a semi-transparent pellicle.

9776-55, Session 12

## EUV high-NA scanner and mask optimization for sub-8nm resolution *(Invited Paper)*

Jan van Schoot, Koen van Ingen Schenau, Kars Troost, ASML Netherlands B.V. (Netherlands); John D. Zimmerman, ASML (United States); Sascha Migura, Bernhard Kneer, Jens Timo Neumann, Winfried Kaiser, Carl Zeiss SMT GmbH (Germany)

EUV lithography for resolutions at 8 nm half pitch and below requires the numerical aperture (NA) of the projection lens to be significantly larger than the current state-of-the-art 0.33NA. In order to be economically viable, a throughput above 100 wafers per hour is needed.

As a result of the increased NA, the incidence angles of the light rays at the reticle increase significantly. Consequently the shadowing deteriorates the aerial image contrast to unacceptably low values.

As shown before [1], the only solution to reduce the angular range at the reticle is to increase the magnification in the scanning direction. Simulations show that we have to double the magnification to 8x in order to overcome the shadowing effects. This results into an anamorphic step and scan system, with which we can print fields that are half the size of the current full field, where the main assumption is that we keep the current 6" mask size. By increasing the transmission of the optics and by increasing the acceleration of the wafer- and reticle stage we can enable a throughput in excess of 150 wafers per hour, making this an economically viable lithography solution.

In this paper we will show how we can further optimize throughput, CDU and overlay by optimizing the main system and mask design parameters.

[1] J.B.P van Schoot, K. van Ingen Schenau, C. Valentin and S. Migura, "EUV lithography scanner for sub-8nm resolution," Proc. SPIE 9422, (2015).

9776-56, Session 12

## Emulation of anamorphic imaging on the SHARP EUV mask microscope

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The Semiconductor High numerical aperture Actinic Reticle review Project (SHARP) is a synchrotron-based, extreme ultraviolet (EUV) microscope dedicated to photomask research. SHARP emulates the illumination and imaging conditions of current EUV lithography scanners and several generations into the future.

Printing smaller features in future generations of EUV lithography requires a larger numerical aperture (NA) at the wafer side. This can be achieved by increasing the mask-side NA or the demagnification of the optical system. An increased mask-side NA in the y-direction would result in adversely high angles of incidence at the photomask. One recent proposal to overcome this limitation and extend EUV lithography beyond 0.33 NA is to increase the mask side-NA in the x-direction and increase the demagnification in the y-direction using an anamorphic imaging optic.1

SHARP uses off-axis Fresnel zoneplate lenses as imaging optics. The instrument offers standard lenses with mask side apertures ranging from 0.0625 to 0.15625 (equivalent to 0.25 to 0.625 wafer-side NA in a 4x scanner). To emulate the mask-side solid angle of an anamorphic projection lens, the authors have created a set of Fresnel zoneplate lenses with an almost elliptical aperture of 0.1375 in x (0.55 4xNA) and 0.06875 in y (0.55 8xNA) at 6º central ray angle. Figure 1 shows an illustration of the pattern of an elliptical off-axis Fresnel zoneplate lens and an electron-microscopic image of a region at the border of one of the newly produced elliptical zoneplates. The optics are currently being mounted for installation and testing in the SHARP microscope.

Although the pupils are non-circular, the various zoneplates have a physical isometric magnification ratio ranging from 1250x to 1636x. With the anamorphic emulation, the pixels in the recorded images represent different length scales on the mask surface in the x and y directions. The oversampling in the y direction will be between 6 and 9 times the resolution of the lenses.

In addition to matching the mask-side numerical aperture, the angular spectrum of the illuminator has to be matched in order to emulate imaging in an EUV scanner. SHARP's programmable Fourier synthesis illuminator produces arbitrary angular spectra with a range of angles exceeding the collected solid angle of the newly designed elliptical zoneplates. Standard pupil fills and freeform sources used with anamorphic projection optics can be produced.

The paper discusses the design and production of elliptical zoneplate lenses for the emulation of anamorphic imaging, and will present the first imaging results, testing the resolution limits in x and y and the modulation transfer function of the optics.

This work is performed by the University of California Lawrence Berkeley National Laboratory under the auspices of the U.S. Department of Energy, Contract No. DE-AC02-05CH11231. Funding by Intel is gratefully acknowledged.

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## Influence of anamorphic high-NA for mask defect inspection in EUV lithography

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The defect free extreme ultraviolet (EUV) mask manufacturing is the most important issue in EUV lithography. To obtain clear pattern on a wafer, the defect free EUV mask is required even if a numerical aperture (NA) is increased for 11 nm node and below. In addition to that, the EUV mask inspection for defect free is essential for high-volume manufacturing. Recently anamorphic high-NA system is suggested to make even smaller patterns. And, the EUV mask inspection with anamorphic high-NA needs some attention. The suggested anamorphic high-NA has 8x magnification for x-direction while 4x magnification for y-direction. This asymmetry magnification will induce a difference of pattern error and defect inspection for each direction at the same mask defect size. Thus, there is a need to check the EUV mask structure of asymmetry magnification with mask defects.

In this study, we investigated the impact of multi-layer (ML) defect with anamorphic high-NA and how to inspect the ML defect in different directions. Figure 1 shows critical dimension (CD) errors as a function of height of ML defect at the same width. The CD error of isomorphic NA is compared with the anamorphic high-NA for each direction, vertical and horizontal line, as shown in the right side of the Figure 1. The CD error for vertical line is reduced by using the anamorphic high-NA because its line and space is widen with the same defect size. However, the CD error for horizontal line is increased by using the anamorphic high-NA. This tells us that we need to give a special attention to the ML defect which is placed at horizontal line when the anamorphic high-NA is used for 11 nm node and below.

The EUV mask inspection ability for anamorphic high-NA is different with mask directions under the identical inspection condition because the pattern size twice along x-direction as compared to the pattern size along y-direction. As a result, the inspection of asymmetry magnification EUV mask gives different result with directions (Figure 2).

We also tried to optimize the condition of EUV mask inspection with anamorphic high-NA to detect the EUV mask defects regardless of defect sizes, positions, and shapes on the EUV mask.

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## High-NA EUV projection lens with central obscuration

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Production of the defect-less masks is one of the key factors in the EUV lithography development. Analysis of the known versions of the mirror lens off- axis schemes shows that the numerical aperture NA>0.3 is usually

combined with demagnification 4-5. In this case, the pattern in the mask plane must contain a reticle with 40-80 nm size of the IC picture elements for printing a half- pitch lines and spaces 10-20 nm at semiconductor plate plane. This requirement significantly determines the mask production complexity, defect removing difficulties and causes high manufacturing cost. In addition, the (6-8th) multimirror lenses with the off-axis aspheric optics can have instability in adjustment of the assembly due to a substantial distance from the mask to the image plane.

Compared to the off-axis optics, the lenses with coaxial mirrors allow obtain NA up to values of 0.8 and $\beta > 10$. They are more compact and less technically complicated in term of setting. The greater value of demagnification leads to the mask cost reduction, as in this case, the elements of the IC pattern template can be made bigger and, therefore, with fewer defects.

However, the coaxial schemes can engender a problem due to the image plane removal beyond the projection lens elements boundaries. Under these conditions, one should locate a subsystem with one-fold magnification between the high-NA multimirror lens and the semiconductor plate with resist. This subsystem consisting of three mirrors (concave, convex and plate) transfers the image formed by the multimirror lens on the wafer plane. The plane is located far from the nearest lens aspherical mirror at a distance sufficient for moving and exposure of large-scale plates with resist during the high-production IC manufacturing.

We have designed a projection lens consisting of four coaxial mirrors with NA= 0.485 and $\beta = 12$ combined with the imaging subsystem, the obscuration factor - 0.407.

High-NA lens design includes the nanopositioning actuators which provide a specified adjustment corresponding to an ultrahigh resolution. The design parameters of the "Vanguard" subsystem provide aberration correction of a wide sloping beam for the image field point with the values of the wave aberrations across the entire aperture of at most $0.05\beta$ ( 13.4 nm). The optical axis of the three-mirror subsystem is shifted from the optical axis of the high-NA coaxial objective to the value of H/2, where H is half diameter of a concave mirror. The ratio of curvature at the tops of a convex and concave mirrors has the order of 1.6-1.8, and the ratio of the distance from plane of the intermediate image to the first (concave) mirror to the distance between the concave and convex mirrors is of the order of 1.9 - 2.3.

The use of multimirror lens with demagnification I > 10 leads to a significant reduction of the defect-less masks manufacturing complexity for high-NA EUV tool. We have developed a four mirror lens (NA = 0.485; S = 12) with a central obscuration. It has a 1.24 mm image field size. The simulation predicts the resolution of lens L&S 10 nm in the center and 20 nm on the edge of image field. The RMS wavefront aberration across the field: 0.0573 - 0.1181. The results of our work could be applied to making a projection lens with a NA >0.5 when using coaxial MIRROR.

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## Comprehensive characterization of Gd and Tb laser plasma emission near $\lambda = 6.7$nm

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Plasmas emitting near $\lambda = 6.7$ nm are of interest for beyond extreme ultraviolet (BEUV) lithography. Highly ionized Gd and Tb plasmas can produce intense emission through unresolved transition arrays (UTA) at wavelengths around $\lambda = 6.7$ nm, which fall in the spectral region of La/B-based multilayer mirrors which have high reflectivity at that wavelength. Several studies of laser-created Gd and Tb plasmas emitting near $\lambda = 6.7$ nm have been reported for different laser parameters. However these measurements were conducted using different lasers and experimental setups. Here we report results of a comprehensive study of the spectral characteristics, conversion efficiency (CE) and source size of Gd and Tb plasmas created over a broad range of laser pulsewidths (220 ps to 4 ns) and intensities (2.8x1011 - 9.1x1013W/cm2) using a single laser for the first time. In this study, we used a diode-pumped, chirped pulse amplification (CPA) laser system based on cryogenically-cooled Yb: YAG producing pulses of up to 100 mJ at $\lambda = 1030$n. With a systematic scanning of three driver laser parameters (pulsewidth, pulse energy, and focal spot size) the angular distribution of the in-band BEUV emission was measured using an array of calibrated energy-monitors that allow us to make more accurate conversion efficiency measurements than previous studies. The BEUV emission is observed to decrease at larger angle from target normal. The angular distribution of BEUV emission becomes more convex when laser pulsewidth decreases and is rather insensitive to the focus spot size and pulse energy. Measurements of the conversion efficiency of Gd plasma for different laser parameters are summarized in Figure 1. A maximum conversion efficiency of 0.47% into a 0.6% bandwidth centered at $\lambda = 6.7$nm was obtained with 2ns laser pulsewidth for Gd plasma. The plasma properties behind these trends are explained by an analysis of the spectral emission and plasma images. As laser pulsewidth increases, the peak of spectral emission of Gd and Tb plasma shifts to shorter wavelength and the spectrum becomes narrower. At-wavelength plasma images were also obtained for different laser parameters.

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## Current development status of HSFET (high-NA small field exposure tool) in EIDEC

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From the mid-90's, several small field micro exposure tools have been developed for EUVL process development. In Japan, SFET (Small Field Exposure Tool) was developed in 2007 as part of the MIRAI-Selete project. SFET was constructed using a two-mirror Schwarzschild objective and compact Xe DPP source. SFET was utilized to support early access of EUV resist development and EUV process control considerations such as mask shadowing effects, flare effects, and so on. EIDEC then took over the SFET for developing 16nm half pitch resist development.

But full field EUV exposure tool design has now caught up with the 0.3 NA small field micro exposure tool. Now a higher NA tool is required for developing 11nm half pitch exposure and beyond. Consequently, several worldwide sites are aimed at developing 0.5NA micro exposure tools. Since early 2012, the possibility of realizing a 0.5 NA small field micro exposure tool for next generation lithography had been researched at EIDEC. As of 2013, we decided on the basic optical design concept for the tool. We chose to upgrade the Projection Optics, Illumination Optics and Xe DPP source, while retrofitting the SFET chambers, and called the new tool "HSFET" (High NA Small Field Exposure Tool).

The basic configuration of HSFET is as follows; Xe DPP EUV source of 65mW at the IF position, 6 mirror illumination unit constructed in a critical illumination configuration, rotationally moving turret parts which can hold several sigma apertures placed separately from the main chamber in order to exchange the aperture without breaking vacuum condition, a two-mirror PO Box well controlled and guaranteed to operate at a field size of larger than 30um x 200um field size from an aberration point of view, and variable NA mechanics supporting various patterning conditions to bridge from the current generation of 0.33NA tools to the next of 0.5NA tools and beyond.

From the end of last year, we started to assemble the illumination optics, while the PO Box was just installed in August of 2015. The PO Box optical performance is well suited for our required 11nm half pitch patterning. The flare value is less than 3%. Transmitted WFE value is measured and confirmed at far less than the required 0.6nm RMS at the field center and field corner positions. We plan to start to expose the wafers using a newly designed reticle for HSFET patterning. We will report the basic printing performance of HSFET and discuss the possibility of patterning beyond the sub-10nm region.

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9776-61, Session 13

## EUV patterning successes and frontiers

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The feature scaling and patterning control required for the 7nm node has introduced EUV as a candidate lithography technology for enablement. To be established as a front-up lithography solution for those requirements, all the associated aspects with yielding a technology are also in the process of being demonstrated, such as defectivity process window through patterning transfer and electrical yield. This paper will review the current status of those metrics for 7nm at IBM, but also focus on the challenges therein as the industry begins to look beyond 7nm.

To address these challenges, some of the fundamental process aspects of holistic EUV patterning are explored and characterized. This includes detailing the contrast entitlement enabled by EUV, and subsequently characterizing state-of-the-art resist printing limits to realize that entitlement. Because of the small features being considered, the limits of film thinness need to be characterized, both for the resist and underlying SiARC or inorganic hardmask, and the subsequent defectivity, both of the native films and after pattern transfer. Also, as we prepare for the next node, multi-patterning techniques will be validated in light of the above, in a way that employs the enabling aspects of EUV as well. This will thus demonstrate EUV not just as a technology that can print small features, but one where all aspects of the patterning are understood and enabling of a manufacturing-worthy technology.

9776-62, Session 13

## Contrast optimization for 0.33NA EUV lithography

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0.33 NA EUV lithography is expected to be introduced into High Volume Manufacturing at k1 values of approximately 0.4...0.5. This is significantly larger than state of the art immersion lithography which can operate at k1 of 0.3. Key enabler in immersion lithography to achieve this low-k1 was contrast optimization by aggressive off-axis illumination. In EUV we typically observe image contrast, expressed in terms of normalized image log slope of 2 and larger, whereas the NILS in immersion lithography can be as low as 0.5. In terms of exposure latitude this would give 20% in EUV versus 5% in immersion lithography. From Critical Dimension Uniformity (CDU) point of view, for 1D features there is no strong need for contrast enhancement in EUV at this moderate k1: a NILS of 2 will yield exposure latitude of 20% and thus a very small contribution from dose errors (with dose errors approaching 1%). Nevertheless there can be drivers to enhance the contrast as much as possible.

- Enhanced contrast for 1D structure which will allow lower resolution.
- Enhanced contrast for 2D structures, allowing smaller dimensions for tip-to-tip and tip-to-line
- Enhanced contrast for 1D and 2D features resulting in lower roughness of the features and better pattern fidelity.
- Enhanced contrast for 1D and 2D features resulting in a lower exposure dose

Two main parameters in the optical column influencing the contrast in EUV lithography are:

- The incidence angles at mask level. This comprises both the maximum angle and the spread of angles.
- The mask absorber material and thickness.

The two competing mechanisms driving the contrast are:

- Capture as many diffraction orders as possible
- For each incidence angle the aerial image is shifted due to the Mask 3D induced odd phase effects. This shift increases with incidence angle. Using a large spread of angles leads to contrast loss: Mask 3D induced fading. The spread of incidence angles is linked to the pupil fil ratio.

As an example of the impact of pupil fill ratio Figure 1 shows the NILS for equal lines and spaces and regular contact holes arrays. The pupil shapes are calculated, taking the two competing mechanisms described above into account:

For pitches close to the resolution limit the illumination angles need to be close to the edge of the illuminator NA (?=1) to capture the diffracted light, for larger pitches it is more optimum to concentrate the light closer to the center of the pupil (?=0) to reduce the Mask 3D induced fading. We will show experimental data of contrast enhancement by means of reducing pupil fill ratio and changing absorber (thickness, material type). Amongst the figures of merit we will look at resolution for 1D and 2D type features, including tip-to-tip and tip-to-line and (local) CDU. Figure 2 shows an example how the local CDU of a CH array will change, dependent on the contrast. The local CDU is measured as the variation of CD across the different holes in the array. A direct correlation between NILS and experimental local CDU is observed, making contrast and thus NILS a main parameter to optimize in the litho.

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## Extension of practical k1 limit in EUV lithography through optimization of illumination modes

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Sub 0.3k1 regime has been widely adopted for HVM of optical lithography due to various resolution enhancement technologies. It is not certain when such low k1 is feasible in EUV, though most technologies are available in EUV also. in this paper, we will present experimental results on patterning performance of line space (L/S) and contact hole (C/H) in EUV lithography. First, practical k1 value with 0.33NA EUV lithography is investigated through experiment using NXE3300 EUV tool. Patterning limit, process window, LWR for L/S and LCDU for C/H pattern are measured with respect to various design rules. And we have evaluated the effect of off axis illumination (OAI) mode with various illumination conditions to improve the patterning performance and reduce k1 limit. Then the experimental results of LWR/LCDU are compared with NILS values from stochastic simulation. As results, we apply EUV source mask optimization (SMO) technologies to increase the NILS with FlexPupil option of EUV scanner. As a conclusion, we try to suggest the practical k1 limit of EUV with up to date resist performance

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**Extreme Ultraviolet (EUV) Lithography VII**

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## Application of EUV resolution enhancement techniques (RET) to optimize and extend single-exposure bi-directional patterning for 7nm and beyond logic designs

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EUV lithography is uniquely positioned to extend single exposure solutions for critical imaging layers at the 7 nm technology node and beyond. In this work, we demonstrate the application of advanced EUV resolution enhancement techniques to enable bidirectional printing of 36 and 32 nm pitch standard logic cell and SRAM designs with 0.33 NA optics using a proven OPC model. Prior work [1] has highlighted the issues of pattern placement errors and image contrast loss due to the telecentricity that is inherent in EUV reflective imaging systems and masks and demonstrated utilizing asymmetric pupil to reduce the pattern placement error. It has been previously shown that there is a potential reduction in common process window due to through-pitch best focus shifts with non-optimized SRAF placement. In this paper, we demonstrate the use of pattern placement error aware SMO, asymmetric illumination shape, and SRAF placement optimization to increase the overall common process window by as much as 40% compared to OPC only optimization. Consequently, we demonstrate manufacturable single patterning solution for 0.33 NA EUV bi-directional 7 nm node logic designs. We show that these techniques can achieve the required performance for MEEF, best focus shift across features, and ILS, which is known to be important for reducing stochastics and subsequent line-edge-roughness (LER).

9776-65, Session 14

## Assist features: placement, impact, and relevance for EUV imaging

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Assist features are commonly used to improve lithographic process window of isolated features under illumination conditions that enable the printability of dense features. With the introduction of EUV lithography, the interaction between 13.5nm light and the mask features generates strong mask 3D effects. On wafer, these 3D effects manifest as pitch-dependent best focus shifts, induced pattern asymmetries and image contrast loss. To minimize these effects, we explore the use of assist features, their size and placement, on isolated features and two-bar structures consistent with 7nm node designs using 0.33NA and specific illumination settings. We define a position-aware process window that takes into account both process latitude and the placement of each image edge. We also report the standard process window that only accounts for CD because this is needed to match to wafer data. Wafer imaging and simulation results will be compared and an assessment of optimal assist feature configuration and use will be made. It is essential to understand the potential benefit of using assist features and to weigh that benefit against the price of complexity associated with adding sub-resolution features. To that end, we include an OPC study comparing data with and without assist features using full-chip complexity metrics like data size.

9776-66, Session 14

## EUV masks manufacturing: challenges and opportunities

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No Abstract Available

9776-67, Session 14

## EUV implementation of model-based assist features in contact patterns

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As the feature size goes smaller and smaller, sub-resolution assist features (SRAFs) start to play an important role in EUV lithography. However, unlike ArF lithography, EUV has unique characteristics, including the shadowing effects and through slit effect. These effects may require different SRAF rules for different directions at the edges and corners, and also different rules at different slit locations, under certain printing criterions. Another difficulty in EUV SRAFs comes from the SRAF size. Due to mask manufacturing limit and the small main feature size in the advance nodes, the size of the SRAF is no longer much smaller than the main feature size, and the SRAF printing becomes a significant problem. In order to make SRAFs useful and also avoid its printing in certain process window conditions, the possible SRAF location is very limited, and it is sensitive to the change of main feature size and pitch. Small difference in the main feature size or pitch may require different rules of placing SRAFs. Therefore, comparing to ArF lithography, generating a good set of rules for placing SRAFs in EUV lithography is much more challenging and time-consuming. A model-based SRAF tool chooses the SRAF location based on the mask simulation. It takes the mask change, slit location and SRAF size into account, and generates the best SRAF location based on the process variation band and SRAF printing.

Contact patterns are good test cases to show all the difficulties in EUV SRAF. So in this paper, we use different contact patterns, and use both simulation and wafer data to investigate if the model-based SRAF solution gives better printing results than the rule-based SRAF solution in EUV lithography, based on different image quality parameters.

9776-68, Session 14

## Photolithographic patterning reaches 6nm half-pitch using EUV interference lithography

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One method to extend the resolution of photolithography is to use the shorter EUV wavelength of 13.5 nm and record the interference pattern produced by two coherent beams. The coherent beams can be formed by diffraction gratings on a silicon nitride membrane mask. The pitch of the interference pattern is then half the pitch of the diffraction gratings and thus, high resolution patterning requires high resolution diffraction grating masks. Furthermore, high diffraction efficiency materials at EUV wavelength are typically metals such as molybdenum, ruthenium, and iridium, which are difficult to pattern transfer into. Simulations using rigorous coupled wave analysis show that the diffraction efficiencies using such metals are

up to 10 times more efficient than the currently used direct-write hydrogen silsesquioxane (HSQ) photoresist based gratings.

Diffraction grating masks are produced by electron-beam lithography, and for high resolution gratings become very challenging due to the electron proximity effect. Pattern transfer into diffraction efficient metals by etching or electroplating at such small feature sizes is also difficult. To overcome both hurdles, we patterned HSQ photoresist at a relaxed pitch and deposited iridium over the HSQ grating using atomic layer deposition. The top and bottom iridium were removed using directional argon based ion milling, leaving the iridium deposited on the side of the HSQ grating lines. The HSQ was removed by buffered oxide etch leaving an iridium grating at double the spatial frequency of the original HSQ grating. Using this method at the XIL-II beamline for EUV interference lithography, Swiss Light Source, we achieved 6 nm half-pitch line/space patterns recorded in HSQ, a world record resolution for photolithography.

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9776-69, Session 14

## EUV patterned templates with grapho-epitaxy DSA at the N5/N7 logic nodes

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Using grapho-epitaxy for directed self-assembly (DSA) of block co-polymers (BCPs) provides a promising route for via and/or block layer patterning. This approach allows definition of holes with small CD and pitches. One of the primary concerns, however, is in the placement accuracy of the holes. There are three primary contributors to the final overlay of the DSA hole: 1) overlay accuracy in the lithography step of the template definition, 2) variability in the edge placement of the template, and 3) intrinsic variability of the DSA process. 1) is a well-understood lithography problem and largely defined by the overlay accuracy of the scanner. 2) highly depends on the employed lithography (and etch) process for template definition. 3) mainly depends on BCP characteristics (such as its chi-parameter) and the processing conditions.

EUV lithography enables much higher precision for template definition compared to what can be achieved using ArF immersion lithography. This is expected to improve the placement accuracy of the DSA process through improved edge placement definition of the template as well as through pre-shaping of the template (e.g. in 'peanut shapes'). Reversely, local CD uniformity (LCDU) is a well-known issue in EUV lithography, mainly caused by stochastic effects. LCDU performance typically deteriorates for high sensitivity (high throughput) EUV resists. The CD in DSA is defined through the BCP composition and DSA is therefore expected to be able to repair LCDU of an EUV pre-pattern. DSA and EUV are therefore very suited to be used as complementary technologies. In recent work the use of such a process for N7 and N5 logic patterning has been discussed.

In this paper the imec templated DSA process based on NXE:3300 exposed EUV pre-patterns will be described. The performance of the process in terms of placement accuracy and LCDU performance will be compared to simulations.

9776-70, Session 14

## Novel detection and process improvement for organic coating-film defect

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Spin coating has been used as a photoresist application method for many years and it has been continued to include applications like the tri-layer with stacked photoresist, Si containing anti-reflected coating (Si-ARC), and Spin on Carbon (SOC). Last year we reported EUV defectivity improvement but the causes of some types of the defects were not found.

In this study, the unique defects on the organic coating-film could be detected using an LS-9300 by Hitachi High-Technologies, and some of these defects were able to be mitigated by optimization of the SOKUDO-DUO Track System.

Utilizing both systems together, we have revealed the mechanism of EUV pattern defect reduction linked to novel detected film coating defects. During the conference, we will discuss expansion of this concept to other film coatings.

9776-71, Session 15

## NXE pellicle: offering a EUV pellicle solution to the industry *(Invited Paper)*

Derk Brouns, Eric Casimiri, Dennis De Graaf, Paul Janssen, Ronald Kramer, Matthias Kruizinga, Frits Van Der Meulen, Daniel A. Smith, Beatrijs Verbrugge, David Van De Weg, Noelie Wojewoda, Carmen Zoldesi, ASML Netherlands B.V. (Netherlands); Peter Delmastro, Aage Bendiksen, Hilary G. Harrold, ASML (United States)

Towards the end of 2014, ASML committed to provide a EUV pellicle solution to the industry.

Last year, during SPIE Microlithography 2015, we introduced the NXE pellicle concept, a removable pellicle solution that is compatible with current and future patterned mask inspection methods.

This year we will present results of how we took this concept to a complete EUV pellicle solution for the industry. We will highlight some technical design challenges we faced developing the NXE pellicle and how we solved them. We will also present imaging results of pellicle exposures on a 0.33 NA NXE scanner system. In conjunction with the NXE pellicle, we will also present the supporting tooling we have developed to enable pellicle use. Finally we will present a roadmap for the adoption of the NXE pellicle for EUV high volume manufacturing.

9776-72, Session 15

## Study of nanometer-thick graphite film for high-power EUVL pellicle

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Extreme ultraviolet (EUV) lithography has received much attention in the semiconductor industry as a promising candidate to extend dimensional scaling beyond 10 nm. The pellicle development is required to improve particle level inside scanner for EUV mass production. Silicon materials have the highest EUV transmittance than any other materials as prepared same thickness but they are not thermally stable enough under EUV exposure. Si pellicle have short lifetime until it breaks down under EUV exposure (less than 128hrs at EUV source power 80W). Poly silicon starts to crystallize around 540C. This indicates that such a thin membrane made out of poly silicon can undergo film deformation and rupture when silicon grains are subject to rearrangement and inter-collision as a membrane is heated up

to crystallization temperature. This is severe limit of silicon for EUV pellicle because these thermal characteristics are intrinsic material properties of Si and cannot be improved while Si membranes are supposed to be heated up to above the crystallization temperature during exposure.

Here, we have invented a freestanding graphite thin film composed of multi-layer graphene for EUV pellicle. It is confirmed that nanometer-thick graphite film (NGF) exhibits superior radiation emissivity (0.4 at RT, 0.51 at 400C or above) by which graphite membrane can maintain temperature below 400C during EUV exposure. Since graphite thin film has much higher tolerance to thermal damage compared to Si or other alternatives, this pellicle membrane can be safe during EUV exposure. Graphene is also known to have extreme mechanical stability even as mono-layer and thus a graphite film composed of laminated many graphene layers should have mechanical stability strong enough to sustain freestanding large area. Large-scale of 5cm?5cm freestanding NGF pellicle membrane developed for the first time represents such a strong mechanical and structural stability as freestanding pellicle membrane (shown in the figure).

NGF pellicle membranes stable enough in terms of thermal and mechanical properties can show EUV transmittance as high as 92% when they are fabricated down to 18nm. Excellent properties of NGF membranes from thermal, mechanical, chemical and optical perspectives signify that the NGF membranes can be a promising and superb candidate for EUV pellicle

9776-73, Session 15

## EUV lithography imaging using novel pellicle membranes

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EUV mask protection against defects during use remains a challenge for EUV lithography. A stand-off protective membrane – a pellicle – is targeted to prevent yield losses in high volume manufacturing during handling and exposure, just as it is for 193nm lithography. The pellicle is thin enough to transmit EUV exposure light, yet strong enough to remain intact and hold any particles out of focus during exposure. The development of pellicles for EUV is much more challenging than for 193nm lithography for multiple reasons including: high absorption of most materials at EUV wavelength, pump-down sequences in the EUV vacuum system, and exposure to high intensity EUV light. To solve the problems of transmission and film durability, various options have been explored. In most cases a thin, continuous film is considered , since the deposition process for this is well established and because it is the simplest option. The transmission specification typically dictates that membranes are very thin (~50nm or less), which makes both fabrication and film mechanical integrity difficult. As an alternative, porous films will allow thicker membranes for a given transmission specification, which is likely to improve film durability. The risk is that the porosity could influence the imaging.

At imec, both film approaches are investigated for the pellicle application. Examples of candidate films will be presented. For the case of porous films, example investigations are : fibrous or porous material (such as CNT or CNS) incorporated in the stack, or nanometer-sized patterns that are etched in a film. Promising membranes are tested relative to the primary specifications: transmission and film durability. A risk assessment of printing performance is provided based on simulations of scattered energy. General conclusions on the efficacy of various approaches will provided.

9776-74, Session 15

## Thermomechanical behavior of EUV pellicle under dynamic exposure conditions

Dario L. Goldfarb, IBM Thomas J. Watson Research Ctr. (United States); Max O. Bloomfield, Rensselaer Polytechnic Institute (United States); Matthew E. Colburn, IBM Corp. (United States)

The utilization of EUV pellicles as protective layers for EUV masks requires the use of refractory materials that can tolerate large temperature excursions due to the non-negligible EUV radiation absorption during exposure. Additionally, the mechanical stress induced on the EUV pellicle by the thermal load is dependent on the thermal expansion of the material which can be responsible for transient wrinkling. In this study, an ultrathin (15-20nm) free-standing membrane based on silicon nitride is utilized as a learning vehicle to understand the material requirements of EUV pellicles under dynamic exposure conditions that are typical of commercial EUV scanners. First, the nanoscale radiative properties (emissivity) and thermo-mechanical failure temperature of the dielectric film under vacuum conditions are experimentally investigated utilizing a pulsed ArF (193nm) probing laser. The silicon nitride membrane is found to be marginally compatible with an equivalent 80W EUV source power under steady state illumination conditions. Next, the thermal behavior of the EUV pellicle under dynamic exposure conditions is simulated using a finite element solver, running in parallel with dynamic load balancing and adaptive refinement. The transient temperature profile and stress distribution across the membrane under stationary state conditions are extracted for relevant EUV source power values. The present work provides a generalized methodology to anticipate the thermal response of a EUV pellicle under realistic exposure conditions.

9776-75, Session 15

## Inspection of extreme-ultraviolet lithography pellicles using ellipsometry

Changho Lee, Seulki Kim, Sungmo Park, Eunsung Kim, Hye-Keun Oh, Min-Su Kim, Jin-Goo Park, Jin-ho Ahn, Ilsin An, Hanyang Univ. (Korea, Republic of)

Extreme ultraviolet lithography (EUVL) is an unavoidable next generation technology to achieve smaller pattern than that of the current technology level. Although EUVL is usually performed in the ultra-high vacuum(UHV) environment, the surface of mask can be contaminated by particles and residues formed from the photochemical reaction and dusts from handling process. These contaminated layers or spots cause non-uniform light transmission during the exposure process, which causes the image distortion on photoresist. In this reason, a pellicle is necessary to protect the mask and extend its life. The pellicle is a thin and transparent polymer membrane in deep UV lithography. However, in EUVL, the pellicle should be made of an inorganic material due to the poor EUV transmission rate of a common organic pellicle. Therefore, the candidate materials for EUVL-pellicle are solid materials such as Si, poly-Si, or multistack. The EUVL-pellicles need to be very thin to reduce absorption, large enough to cover the full field mask and robust enough to survive from any mechanical shock. Moreover, they should be free of defects. Thus, the fabrication of good EUVL-pellicle is quite challenging. In this work, we introduce ellipsometric technique to characterize the quality of EUVL-pellicle. Ellipsometry is one of the most powerful techniques for the thin-film characterization. Ellipsometry measures two parameters $\{\Delta, \Psi\}$ as functions of (free-space) wavelength. These parameters represent changes in polarization states upon reflection from the sample. Ellipsometry has two types, spectroscopic ellipsometry (SE) and imaging ellipsometry (IE). SE has two remarkable advantages over other techniques for thin-film characterization: (1) it determines microstructural quantities such as volume fractions of physical constituents and thickness of multi-layers with monolayer sensitivity, and (2) it measures the spectra of both refractive index and extinction coefficient (i.e., absorption) simultaneously. Meanwhile, IE can map of large-area samples for inspecting the uniformity of thickness or optical properties. Test pellicles are made of SiNx using MEMS technique. We find that small spot SE can be used to control the thickness of pellicles, whereas IE can be used to reveal defects in microscopic area.

# Conference 9777: Alternative Lithographic Technologies VIII

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9777-1, Session 1

## Lithography alternatives meet design style reality: How do they "line" up? *(Keynote Presentation)*

Michael C. Smayling, Tela Innovations, Inc. (United States)

Optical lithography resolution scaling has stalled, giving innovative alternatives a window of opportunity. One important factor that impacts these lithographic approaches is the transition in design style from 2D to 1D for advanced CMOS logic. How do the alternatives benefit from 1D layout? Can there be additional design / process co-optimization? Can any of the alternatives complement each other or optical lithography? Does one (shrinking) size fit all? It's truly an exciting and challenging time for lithographers.

9777-2, Session 1

## Emerging nanopatterning opportunities in electronics, displays, and healthcare *(Keynote Presentation)*

S. V. Sreenivasan, The Univ. of Texas at Austin (United States)

While semiconductor industry has been a key driver in the development of high throughput micro- and nano-lithography, other large lithography markets such as patterning for displays have emerged outside the semiconductor area. This talk will start by briefly summarizing the established lithography markets and their requirements. This will be followed by a discussion of a variety of significant potential emerging opportunities for lithography. The talk will emphasize state-of-the-art in each of these areas; and the key technology gaps both in lithography and the broader infrastructure such as etch, metrology, defect characterization, and yield management. The nanofabrication infrastructure based on semiconductor photolithography will be used as a benchmark to explore the level of maturity in each of these emerging opportunities of nanopatterning.

9777-3, Session 1

## Multiple electron-beam direct-write lithography: an overview *(Keynote Presentation)*

Shy-Jay Lin, Jaw-Jung Shin, Jensen Yang, Wen-Chuan Wang, Burn J. Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

Multiple e-beam direct write (MEBDW) lithography with nanometer resolution, using >10,000 e-beams writing in parallel, proposed 10 years ago by MAPPER, KLA-Tencor, and IMS is a promising solution in exposure cost reduction for 20-nm half-pitch and beyond, comparing with multiple-patterning ArF immersion lithography.

However, MEBDW development still stays in the feasibility demonstration stage, not catching up with the pace of Moore's law desired by the industry. Though the coattail effect of EUV lithography plays a role in slowing down MEBDW development, the inevitable reasons of the slow pace are the long learning cycle to integrate and validate the MEMS chip, building many reliable e-beam columns, and calibration of the massively parallel beams. As a result, the interest of the industry shifted back to multiple-patterning ArF immersion lithography, unless some NGL catches up with the pace of Moore's law in imaging, economy, reliability, defects, and infrastructure.

We will also give an overview of the MEBDW technology based on the current MEBDW development efforts in TSMC, focusing on the technical challenges with our solutions on MEMS chip making, the column design to reduce overlay and dose errors, and the prediction of overlay errors induced by Coulomb interaction.

9777-4, Session 2

## Device fabrication using nanoimprint lithography and challenges in nano-defect management *(Invited Paper)*

Tatsuhiko Higashiki, Toshiba Corp. (Japan)

Many believe that continuous shrinkage of design rule (DR) in semiconductor devices will come to an end in near future. However, according to ITRS roadmap 20131), DR shrinkage is increasingly required in DRAM, NAND flash, 3D Memory, ReRAM and SOC devices. The demand for the total amount of memory will be increased exponentially due to the information explosion symbolized by the Big Data. 3D memory has very high potential to meet both, the capacity and the cost target however, current process cost of 3D memory is higher than that of 2D memory.

The cost reduction of memory device will be continued. However, investment costs in pattern shrinking technologies, such as multi-patterning and EUVL become enormous. The framework in these pattern shrinking technologies has not been able to provide lower-cost semiconductor devices. Therefore, in order to significantly reduce investment cost in lithography, nanoimprint lithography technology has been developing2). One of the most significant challenges in nanoimprint technology is nano-defect management (NDM) technology in which defect inspection of templates and imprinted wafer, the resist material innovation and the defect mitigation is implemented. These problems have been overcome through intensive collaboration with template, nanoimprint lithography equipment, resist, metrology and inspection equipment and cleaning equipment providers. Nano-imprint specific problem has been predicted and corrected with computational lithography technology development3). Moreover, resist defects are generated after etching and resist pattern etching resistance under sub 20 nm hp is a critical issue for NIL as well as EUVL. Resist material innovation is required for all upcoming lithography technologies.

In this paper, status of the nanoimprint lithography application to the semiconductor devices, progress of nanoimprint related technology and NDM will be shown.

9777-5, Session 2

## Nanoimprint system development and status for high-volume semiconductor manufacturing

Tsuneo Takashima, Yukio Takabayashi, Naosuke Nishimura, Keiji Emoto, Atsushi Kimura, Canon Inc. (Japan); Jin Choi, Philip Schumaker, Canon Nanotechnologies, Inc. (United States); Takahiro Matsumoto, Tatsuya Hayashi, Canon Inc. (Japan)

Imprint lithography is an effective technique for replication of nano-scale features. Jet and Flash Imprint Lithography (J-FIL) involves the field-by-field deposition and exposure of a low viscosity resist deposited by Drop-On-Demand inkjet onto the substrate. The patterned mask is lowered into the

fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, the mask is removed, and leaves a patterned resist on the substrate.

Previous studies have demonstrated J-FIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

There are many other criteria besides resolution that determine whether a particular technology is ready for manufacturing. On the mask side, there are stringent criteria for imprint mask defectivity, critical dimension uniformity (CDU), image placement (IP) and imprint defectivity. With respect to the nanoimprint lithography tool, both CDU and line edge roughness meet the criteria of 2nm.

Other criteria specific to any lithographic process for the semiconductor industry include overlay, throughput and defectivity. Canon designs nanoimprint lithography tools by creating production infrastructure which includes resist production, collaborations with mask vendors, and close collaborations with the end user. This approach has resulted in the advancement of the three criteria mentioned above.

The purpose of this presentation is to describe the technology advancements made and introduce the new imprint systems that will be applied for the fabrication of advanced devices such as NAND Flash memory and DRAM. In particular, we will announce a cluster tool designed to meet both the technical and cost of ownership requirements of semiconductor manufacturing. The FPA-1200 NZ2C is a four-station imprint tool. Current performance characteristics include defectivity levels of ~ 9 defects/cm2 (for both the mask and imprint process), a throughput of 40 wafers per hour and champion overlay data of better than 5nm. Methodologies developed to achieve and now improve these values will be presented in detail, including doubling the throughput and driving the cost of ownership well below 193nm immersion lithography. In particular, we will discuss important aspects of particle control and particle control mechanisms which have a direct impact on mask life. Additionally, we will elaborate on the overlay budget model and discuss contributions of the tool, wafer, mask and the influences of other related processes. Finally, we will show Canon's overlay road map as well new technologies designed to address higher order distortions.

9777-6, Session 2

## Improvement of nanoimprint lithography templates toward 1x generation lithography

Ichimura Koji, Katsutoshi Suzuki, Ryogo Hikichi, Hironori Sasaki, Masaaki Kurihara, Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan)

Nanoimprint lithography is gathering much attention as one of the most potential candidates for the next generation lithography for semiconductor. This technology needs no pattern data modification for exposure, simpler exposure system, and single step patterning process without any coat/develop truck, and has potential of cost effective patterning rather than very complex optical lithography and/or EUV lithography.

Working templates are proposed to be made by the replication of the EB written high quality master templates for the use of nanoimprint for the semiconductor lithography. Maintaining the quality of the master templates in replication process is very important. Nanoimprint technique is also used for the replication of the templates, and optimization of the nanoimprint process is very important as well as pattern transfer etching process after imprint.

Nanoimprint is expected to be applied to the 1x generation lithography. High resolution is the one of the key of the nanoimprint templates. For the fine feature master fabrication, electron beam direct writing is the most preferable method and this requires high resolution e-beam writing and good EB resist. Application of the SADP to master fabrication is also one of the candidates for high resolution master.

Regarding the replica fabrication, imprint process itself has good pattern fidelity and the following pattern transfer process is the key. Nanoimprint templates have a limitation of the aspect ratio in imprint process and this means the resist height decreases at high resolution features. Etching process needs to be carefully optimized for high resolution replica fabrication.

In this presentation, our development results on the high resolution template fabrication will be reported as well as recent template quality improvement.

9777-7, Session 2

## Design for nanoimprint lithography (NIL): Total layout refinement utilizing NIL process simulation

Sachiko Kobayashi, Motofumi Komori, Kyoji Yamashita, Akiko Mimotogi, Toshiba Corp. (Japan); Ji-Young Im, SK Hynix, Inc. (Korea, Republic of); Masayuki Hatano, Takuya Kono, Shimon Maeda, Toshiba Corp. (Japan)

1. INTRODUCTION

Technologies for pattern fabrication using nanoimprint process are being developed for various devices. Nanoimprint lithography is attractive candidate for its clear pattern transfer characteristics of mold contact patterning with fewer process steps comparing multi-patterning, and so the effect of greatly shortened TAT. To apply smaller pattern size device, layout dependent hotspots becomes a significant issue, so design for manufacturing (DFM) flow considering imprint process has to be prepared. In this paper, resist spread, stress distribution on pattern and mold, resist shrinkage through UV cure are extracted as targets of layout compensation, and various imprinting simulation utilizing stress model and fluid model are verified. DFM flow to prepare imprint friendly design, and to apply imprint proximity correction (iPC) is proposed.

2. NANOIMPRINT LITHOGRAPHY COMPLIANCE CHECKING SYSTEM

Figure 1 shows an example of schematic flow of NIL processes. The processes consist of template making, resist application, mold imprinting, and mold removal. In these processes, patterns are transferred through imprint process contacting mold to wafer. To avoid lithography hot spot occurrence through the process, predict hotspots and fix them through litho-compliance check. An example of NIL compliance check flow is proposed in figure 2. Layout is analyzed with design rule checker (DRC), and hotspot candidate is extracted. And then, each hotspot is examined with NIL process simulation. Critical hotspots are modified in design or process, so NIL friendly design data is provided. At detailed NIL simulation, nano-scale three-dimensional process simulation, such as mechanical, structural, and resist fluid type simulation is indispensable, so computational cost as well as data volume are considerable issues. Modification rule is added to NIL design rules, so design rules are updated through compliance checking flow. We focused on hotspots caused by following three major factor: 1) CD variation caused by resist residual layer thickness (RLT) variation, 2) Resist extrusion out of border of the shot, 3) de-molding defect through peeling process, analyzed and proposed NIL-friendly design.

3. RESULT AND DISCUSSION

RLT variation strongly depend on resist drop arrangement. RLT hotspot is extracted using NIL simulator, and drop arrangement is refined based on simulation. Resist extrusion issue is also analyzed using NIL simulation, and then NIL friendly border dummy pattern is proposed. De-molding defect occurring mechanism is analyzed using stress simulation, and then layout adjustment through iPC (imprint Proximity effect Correction) rule is proposed. In this way, NIL process friendly design is coodinated. The detailed result will be shown in the presentation.

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9777-8, Session 2

## 200mm wafer scale NIL process assessment for sub-micrometer CD uniformity with the SmartNIL process

Hubert Teyssedre, Stefan Landis, CEA Grenoble (France); Christine Thanner, Viktoria Schauer, Laure MARIA, EV Group (Austria); Cyril Vannufel, CEA Grenoble (France); Markus Wimplinger, EV Group (Austria); Laurent Pain, CEA Grenoble (France)

NanoImprint techniques stick out from other more conventional lithography processes (photolithography, electronic lithography, EUV lithography) by virtue of the fundamental mechanisms that create the structures. With conventional approaches the structures are created through a chemical contrast, whereas a topographic one is formed in the case of NanoImprint thanks to the flow of the resist through the stamp's cavities.

In twenty years, consequent technical developments have been achieved to make the technology more mature and ready for high volume manufacturing. Among a plenty of technology alternatives, the UV based imprint, using transparent stamp, became the standard technology. Two well established options are now available on the market: the full wafer imprint (the size of the stamp correspond to the size of the wafer to be printed) and the step and flash imprint were a small stamp (i.e. die size) is stepped like in optical lithography across the wafer to be processed.

If the step and flash technology is more prone to address the semiconductor markets with high requirement levels for alignment capability and defectivity density, the full wafer option seems to be the reference for the emerging and growing markets like LED and Photonics based devices. However this wafer scale imprint solution still lacks from quantitative data regarding technology assessment for high volume manufacturing. Commercially available types of equipment and resists are cornerstones of this technology. Nevertheless some blocs of a full supply chain (design rules, master manufacturing and repair, in-line metrology, integration solutions) need to be established and qualified to make the technology mature enough to rapidly meet the market's needs.

To accelerate this technology adoption, CEA-Leti and EV Group recently launched a new program called INSPIRE to demonstrate the benefits of the NIL technology and spread its use for applications beyond semiconductors. Much more than an industrial partnership, the INSPIRE program is designed to demonstrate the technology's cost-of-ownership benefits for a wide range of application domains by supporting the development of new applications, from the feasibility-study stage to the first manufacturing steps, and by transferring integrated process solutions to their industrial partners, thus significantly lowering the entry barrier for adoption of NIL for manufacturing novel products.

In the frame of the INSPIRE program, we present in this paper a first Critical Dimension (CD) uniformity assessment onto 200 mm wafers printed with the SmartNIL technology available in the HERCULES®NIL equipment platform. The work brings focus on sub micrometer resolution features (Figure 1). The silicon masters were manufactured with 193 optical lithography and dry etching. A complete Atomic Force Microcopy (AFM) and Scanning Electron Microscopy (SEM) characterizations were performed over the full master surface prior to the imprint process (Figure 2). The master depth was 433 nm and it was then replicated with the SmartNIL process and printed in the UV/E3 resist from EVG to target 40 nm residual layer thicknesses. Repeatability tests were performed over 25 wafers to collect statistics and the CD distribution within a wafer and also wafer to wafer.

9777-9, Session 3

## Defectivity prediction for droplet-dispensed UV nanoimprint lithography, enabled by fast simulation of resin flow at feature, droplet, and template scales *(Invited Paper)*

Hayden K. Taylor, Univ. of California, Berkeley (United States) and Simprint Nanotechnologies Ltd. (United Kingdom)

Full-field, physically-based simulation of nanoimprint lithography (NIL) is needed to address the throughput-versus-yield challenges that are currently faced by NIL. We demonstrate a simulation framework that can track the spreading and coalescence of tens of thousands of picoliter-volume resin droplets beneath a nanoimprint template, predicting evolution of feature filling and residual layer thickness (RLT) uniformity during the imprinting of geometrically complex designs such as found in solid-state memory.

Our new approach builds upon our existing simulation techniques for chip-scale, spun-on thermal and UV-curing resists and for roll-to-roll imprint. These techniques discretize the imprinted area on a square grid, and employ a mechanical impulse response that describes how the surface of the resist deforms when loaded by the template in each grid location. Template–resist contact pressures are computed for multiple timesteps.

To simulate droplet-dispensed imprinting, it is essential to account for the merging of multiple droplets within each grid location before template filling occurs. Previous work simulating droplet spreading has been constrained by computational requirements to only a few features or droplets; in contrast, our approach does not need to solve for the behavior of each individual droplet and can simulate the spreading of >10^4 droplets.

To avoid entrapment of chamber gases between merging droplets, most processes initially bow the template and spread the resist radially outwards. We find that for typical droplet properties, the template must have a radius of curvature of ~500 mm where it meets the propagating fluid front to prevent gas entrapment.

Spreading droplets interact with cavities on the template resulting in accelerated RLT reduction compared with a flat template, as well as highly directional spreading along lines. We have used simulations of single droplets spreading across multiple features to model spreading acceleration and directionality versus pattern parameters.

We have integrated our new droplet deformation model with models for elastic template deflections and cavity filling, and have explored the imprinting of a 30 mm-by-40 mm field that is reminiscent of Flash memory. If only part of the template area is in contact with resist droplets because it overlaps the edge of the wafer, simulations show ~2 nm greater RLT variability and less complete cavity filling after a given imprinting time. We attribute this deterioration of imprint quality to the asymmetrical pressure distribution experienced by the template in a partial field.

Our simulation technique can be used to evaluate multiple template layouts, e.g. to help optimize the protrusion density of a template border region. A border density of 50% offers superior RLT uniformity compared with 0% or 100% densities, by controlling RLT reduction rate at the edge. Simulations on a 1 mm grid take ~5 s to run on a standard personal computer; those using a 0.1 mm grid require ~5 minutes. This simulation approach thus offers NIL users a rapid method for evaluating ways of achieving production throughput targets of ~1 s/field spreading time.

9777-10, Session 3

## Jet and flash imprint lithography material development for high-throughput semiconductor memory

Niyaz Khusnatdinov, Dwayne L. LaBrake, Zhengmao Ye, Tim Stachowiak, J. W. Irving, Whitney Longsine, Matthew

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**Alternative Lithographic Technologies VIII**

C. Traub, Van Truskett, Brian Fletcher, Weijun Liu, S. V. Sreenivasan, Canon Nanotechnologies, Inc. (United States)

Nanoimprint lithography techniques are known to possess replication resolution below 5nm. A specific form of imprint lithography known as Jet and Flash ImprintTM* Lithography (J-FILTM) has been developed for manufacturing advanced CMOS memory. A one step patterning at 15nm half-pitch can be achieved with J-FIL eliminating the need of complicated and expensive Self-Aligned-Quadruple–Patterning. In addition, patterns are not limited to repeating structures such as lines and spaces thereby leading to significant cost savings in patterning. J-FIL involves field-by-field inkjet deposition of a low viscosity resist fluid followed by imprinting with nano-scale precision overlay. A mask with a relief structure is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is separated from the substrate leaving a patterned resist on the substrate.

The key to achieving high throughput is the filling step, in which the resist drops must merge together and fill all relief images on the imprint mask. There are several parameters that can impact resist filling. Key parameters include:

- Resist drop volume (smaller is better),
- System controls (which address drop spreading after jetting),
- Design for Imprint or DFI (to accelerate drop spreading)
- Material engineering (to promote wetting between the resist and underlying adhesion layer).

In addition, it is mandatory to maintain fast filling, even for edge field imprinting. Previous work has discussed resist drop volume and systems controls that allow fast filling of both full and partial fields).1 This paper addresses the material improvements made to accelerate resist filling through the use of optimized drop patterns and by the surface engineering of the materials that come in contact with the liquid resist.

Drop pattern algorithms are designed to minimize the time it takes for drops to merge into a continuous film. The software must recognize the difference between one and two dimensional patterns and compensate accordingly. As an example, one dimensional line patterns typically found in NAND Flash designs benefit from a correctly designed gridded drop pattern that takes advantage of the preferential filling along the lines. Figure 1 shows examples of the filling of vertical lines with a standard square drop pattern and a diamond-like drop pattern that compensates for the preferential filling along the y axis.

Another key to fast fill is material wetting that promotes the merging of the drops both before and after contact with the mask. The liquid resist is typically deposited on a thin customized adhesion layer. To further promote fast filling, an additional pretreatment is done that promotes rapid and even spreading of the discrete portions of the imprint resist. The improvement in resist spreading before the mask contacts the resist is shown in Figure 2. Process efficacy was also tested by performing defect studies as a function of filling time and monitoring non-fill defectivity. Figure 3 shows the results of two different pretreatment conditions that enable filling times less than 1 second.

*Jet and Flash Imprint Lithography and J-FIL are trademarks of Molecular Imprints Inc.

1. N. Khusnatdinov et al., Proc. SPIE 9049, Alternative Lithographic Technologies VI, 904910 (April 8, 2014).

9777-11, Session 3

## NIL defect performance toward high-volume mass production

Masayuki Hatano, Hiroyuki Kashiwagi, Kei Kobayashi, Hiroshi Tokue, Takuya Kono, Tetsuro Nakasugi, Toshiba Corp. (Japan); Eun Hyuk Choi, Woo-Yung Jung, SK Hynix, Inc. (Korea, Republic of)

A low cost alternative lithographic technology is desired to meet with the decreasing feature size of semiconductor devices. Nano-imprint lithography (NIL) is one of the candidates for alternative lithographic technologies. NIL has advantages such as good resolution, critical dimension (CD) uniformity and smaller line edge roughness (LER). On the other hand, NIL involves some risks. Defectivity is the most critical issue in NIL. The progress of the defect reduction in template shows good reduction recently. It indicates that the defect reduction on silicon wafer by NIL process improvement is a key for mass production.

In this paper, we describe evaluation results of long-run defect performance of NIL using up-to-date tool, Canon FPA-1100 NZ2, and discuss future potentials of NIL in terms of defect performance. The impact of various kinds of defects such as template defects, non-filling defects, separation related defects, pattern collapse are discussed. Our data indicates that pattern collapse has a strong correlation with the strength of resist pattern. Chemical contamination management is also important for reducing defect as same as conventional photo lithography.

From these analysis based on actual NIL defect data on long-run stability, we'll show the way to reduce defects and the possibility of NIL in device mass production.

9777-12, Session 3

## Improved defectivity and particle for mask life extension, and imprint mask replication for high-volume semiconductor manufacturing

Keiji Emoto, Fumio M. Sakai, Chiaki Sato, Yukio Takabayashi, Hitoshi Nakano, Tsuneo Takashima, Kiyohito Yamamoto, Tadashi Hattori, Mitsuru Hiura, Toshiaki Ando, Yoshio Kawanobe, Hisanobu Azuma, Takehiko Iwanaga, Canon Inc. (Japan); Jin Choi, Ali Aghili, Brian Fletcher, Zhengmao Ye, J. W. Irving, Canon Nanotechnologies, Inc. (United States)

The Jet and Flash Imprint Lithography (J-FIL) process uses drop dispensing of UV curable resists to assist high resolution patterning for subsequent dry etch pattern transfer. The technology is actively being used to develop solutions for memory markets including Flash memory and DRAM. It is anticipated that the lifetime of a single imprint mask will be on the order 100,000 imprints. This suggests that hundreds or thousands of masks will be required to satisfy the needs of a manufacturing environment. Electron-beam patterning is too slow to feasibly deliver these volumes, but instead can provide a high quality master mask which can be replicated many times with an imprint lithography tool.

For the semiconductor market, a variety of feature types must be resolved, although for memory applications such as NAND Flash, the dominant feature set consists of 1:1 line/space patterns for critical front-end layers. For production Flash memory, the most aggressive production designs are now pushing to half pitches of 19 nm and below. For such designs, mask critical dimension uniformity (CDU) must be less than 10 percent of the minimum device half pitch, defectivity of the mask is required to be less than 1 defect/cm2 and mask image placement must be well below 3nm.

Semiconductor requirements dictate the need for a well-defined form factor for both master and replica masks which is also compatible with the existing mask infrastructure established for the 6025 semi standard, 6" x 6" x 0.25" photomasks. Complying with this standard provides the necessary tooling needed for mask fabrication processes, cleaning, metrology, and inspection. The replica form factor has additional features specific to imprinting such as a pre-patterned mesa. In 2012, an MR5000 mask replication tool was developed specifically to pattern 6" x 6" x 0.25" replica masks from an e-beam written master. Previous work by Ichimura et al. using this tool, demonstrated that a CDU of less than 1.5nm 3 sigma can be achieved on both the master and replica masks. In this paper, we review the advancements in particle control, master mask life and image placement.

Just as a replica mask must last 100,000 imprints, it is essential to maintain the master mask defect density at less than 0.1 defects/cm2. The controlling

factor in master mask life is particle generation, and the key particle contributor is the tool itself. Although particle generation in the MR5000 system was well controlled, a few particle adders were observed. By implementing several particle reduction methods such as material surface processing, air flow control and ionization techniques, it is possible to drive the particle adders down drastically.

As nanoimprint lithography as readied for 1x nm production, mask image placement errors from the mask replication tool will need to be reduced to approximately 1 nm. Current performance of the MR5000 is on the order of 2-3 nm 3 sigma. To further reduce image placement errors, it will be necessary to first improve system imprint and separation controls on the existing replication platform and then later address mask chuck and mask flatness on a new system, the MR2.

Finally, additional data as well as the roadmap necessary for production applications will be discussed.

9777-13, Session 3

## Experiments toward establishing of design rules for R2R-UV-NIL with polymer working shims

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Roll-to-Roll-UV-nanoimprint lithography (R2R-UV-NIL) enables high resolution large area patterning of flexible substrates and is therefore of increasing industrial interest [1-4].

We have set up a custom-made R2R-UV-NIL pilot machine which is able to convert 10 inch wide web with velocities of up to 30 m/min. In addition, we have developed self-replicable UV-curable resins with tunable surface energy and Young's modulus for UV-imprint material as well as for polymer working stamp manufacturing.

Now we have designed test patterns for the evaluation of the impact of structure shape, critical dimension, pitch, depth, side wall angle and orientation relative to the web movement onto the imprint fidelity and working stamp life time.

This test design contains line/space-patterns and crosshatch lines with various pitches and orientations as well as square dots with various pitches and isolated crossed lines.

We have used female (recessed structures) silicon masters of that design with critical dimensions of CD = 200 nm, 400 nm, 800 nm and 1600 nm, and structure depths of

d = 500 nm and 1000 nm - all with vertical as well as slightly inclined (~80°) side walls.

These entire master patterns have been transferred onto single male (protruding structures) R2R polymer working shims, which in turn have been used for R2R-UV-NIL runs of several hundred meters.

In combination with R2R-process parameters such as web speed, UV-power and counter roller pressure, the imprint fidelity and its durability - i.e. the working stamp lifetime - of the various test patterns have been compared.

This study is intended as a first step towards establishing of design rules and developing of nanoimprint proximity correction strategies for industrial R2R-UV-NIL processes using polymer working stamps.

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9777-14, Session 4

## Pattern fidelity improvement of chemo-epitaxy DSA process for high-volume manufacturing

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Directed self-assembly (DSA) is one of the candidates for next generation lithography1. Mainly, cylinder or lamellar structures decided by the block co-polymer (BCP) have been investigated for applying to contact holes or lines, and a lot of conference presentations and papers have showed the advantages of DSA2-5.

One of the biggest challenges to apply DSA technology on semiconductor manufacturing is how to remove the pattern defects. Typical defect types of DSA holes in physical guide are missing and bridge hole. And, dislocation and line bridge typed defect are often observed regarding DSA lines. It has been suggested that those defect causes are particles on the substrate, guide pattern mismatching, and chemical issues. Especially, in case of DSA hole shrink process with the physical guides, it has reported that the critical dimension (CD) and the surface affinity of the guide pattern are main cause of the missing defects. In the same manner, defects of DSA line process have to be understood what the causes are. However, it is not substantially found except that the part of dislocation defects is known to be caused by insufficient bake process. In particular, understanding the defect is significantly difficult for chemo-epitaxy DSA line process since the many process steps are necessary to prepare the chemical guide.

Another challenge of DSA line patterns is how to improve the Line Edge Roughness (LER). In general, LER of DSA lines are related with the interfacial length between two domains. In case of PS-b-PMMA, the length is predicted 3nm, and, approximately 2-2.5nm LER is observed by experimentation. On the other hand, high volume manufacturing requests that the LER number is about 10% of target CD. Most of DSA line process target is sub. 20nm, therefore less than 2nm LER have to be achieved. The interfacial length effect on LER is related with chi number of the BCP. Then, most effective method is using other BCP which has higher chi number than PS-b-PMMA. However, it still takes time for practical use. Therefore, other methods to improve the LER generated by PS-b-PMMA BCP are necessary.

In this report, we will present the latest results regarding the defect reduction work and explain the root cause of the defects. And, LER/LWR reduction results will be also showed. Those improving method will be not only DSA own process but also etch transfer process to under layer.

9777-15, Session 4

## Block co-polymer contributions to the defectivity and roughness performance of the 14nm half-pitch LiNe flow @ imec

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Directed self-assembly (DSA) of block co-polymers (BCPs) is a very simple pattern generation technique that has been studied both by industry and academia from a variety of perspectives. DSA has been up-held as a promising candidate for patterning in future device fabrication schemes. Achieving production-friendly defect densities in DSA flows has been identified as one of the major milestones for demonstrating the maturity of DSA.

In our previous work, we demonstrated our results on defect reduction after transferring 14 nm half-pitch DSA line/space (see Figure 1 for process flow) patterns into the Si substrate in a fully integrated 300 mm wafer production environment. We reported a golden defect density of 24 cm-2, including the DSA and non-DSA defect modes [1]. This was possible due to a collective optimization of the DSA materials, processing conditions and etch conditions.

In this manuscript, we report our recent efforts in identifying the exact contributions of the DSA materials to the final defectivity and LER/LWR performance. We have observed that the three DSA materials, namely the block co-polymer, the brush and the cross-linking mat material have a significant effect, in addition to the process contributions, towards the final defectivity. This manuscript will focus on identifying the factors of the DSA materials that have an effect on the assembly defects, namely the dislocations and 1-period bridges and the level of control needed in the quality of these materials to achieve low defectivity in DSA flows.

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9777-16, Session 4

## Defect annihilation in DSA: Systematic study of optimal materials selection and processing conditions

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Directed Self-Assembly (DSA) of block copolymers on chemically patterned substrates offers considerable promise for next-generation sub-lithographic patterning. One of the remaining challenges in DSA is to understand the precise origin of any defects that may arise. Previous studies have shown that defect formation energy in DSA is of the order of hundreds of kT; the probability of encountering defects at equilibrium is therefore extremely small. Recent studies indicate that defect annealing in DSA is an activated process, where kinetics, not only thermodynamics, plays a key role. In this study, we use a combination of experiments and simulations to understand the relation between the system conditions and relevant kinetic free energy barriers in order to develop optimal defect annihilation processes. Specifically, using a string method with a Theoretically Informed Coarse-Grained (TICG) simulation approach, we identify the kinetic pathways for removal of dislocation pairs in lamellar structures of block copolymer thin films on chemically patterned substrates (with 3X density multiplication). We examine the role of the width and strength of the guiding stripes on such kinetic pathways, and we explore the behavior of a wide range of polymeric material combinations and conditions. Our study provides new molecular-level insights into defect-reduction strategies in DSA, which could in turn find applications in materials selection and process development.

9777-17, Session 4

## Directed self-assembly of silicon-containing block copolymers for 20nm lithography

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The directed self-assembly [DSA] of a 20 nm full pitch lamellar-forming, silicon-containing block copolymer, poly(4-methoxystyrene)-b-poly(4-trimethylsilylstyrene), was performed using a chemo-epitaxy process flow patterned with immersion lithography. The effects of architecture and surface energy on the DSA were systematically investigated to determine the optimum conditions for the DSA of this system. Prepattern pitches commensurate with the natural periodicity of the block copolymer (L0) produced the best DSA, and chemical guidestripes of width equal to 0.5 L0 and 1.5 L0 produced well-aligned features. Changing the chemical guidestripe from cross-linked polystyrene, which is weakly preferential to the poly(4-methoxystyrene) component of the block copolymer, to cross-linked poly(4-methoxystyrene), improved the DSA of the system, presumably due to the higher chemical contrast in the prepattern and the greater affinity of the guidestripe to a component of the block copolymer. In addition, experiments showed that the optimal background brush chemistry for DSA is not neutral for the bulk block copolymer but rather closer in surface energy to the component of the block copolymer not being guided. The best DSA performance was produced when topography was added to the chemical prepattern via a thicker guidestripe material to produce a hybrid chemo- and grapho- epitaxy flow. Pattern development and pattern transfer were also performed with a focus on etch selectivity. These results show a promising route to scale to below 20nm full-pitch patterning with DSA.

9777-18, Session 4

## Fabrication of half-pitch sub-15nm metal wire circuits using directed self-assembly of block copolymers with line density multiplication

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Directed self-assembly (DSA) of block copolymers (BCPs) with line density multiplication has been expected to become one of the most promising next generation lithography candidates for half pitch (HP) sub-15 nm patterning. There have ever been reported several HP sub-15nm patterning processes with polystyrene-block-poly(methyl methacrylate) (PS-b-PMMA) lamellar BCPs such as lift-off process , LiNe process2, SMARTTM process3 and COOL (coordinated line epitaxy) process.4, 5

The COOL process was reported as one of the most practical HP sub-15 nm patterning processes with low cost of ownership (COO), since it requires neither special pinning guide materials to control surface free energy nor resist strip processes after guide line pattern fabrication when compared to the other HP sub-15nm patterning processes.

In order to carry out its process verification across 300 mm wafer for practical semiconductor device manufacturing, electrically process level-test element group (PL-TEG) yields were demonstrated using the COOL process for HP 15 nm patterning with PS-b-PMMA.6 The electrically PL-TEG yields could reveal its process viability from the perspective of total practical performance including critical dimension (CD) control, defect control, positioning error, line edge roughness (LER), line width roughness (LWR), and process window in pattern transfer process. Characterization of HP 15 nm metal wire circuits allowed crucial evidence of the process verification.

In this work, extension of the DSA of BCPs with line density multiplication

such as the COOL process to HP sub-10 nm patterning processes as well as development of high (chi) lamellar BCPs is also investigated through fabrication of HP sub-10 nm metal wire circuits.

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## 9777-19, Session 4

# Sub-15nm patterning technology using directed self-assembly on nanoimprinting guide

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1. INTRODUCTION

In next generation lithography to make sub-15nm pattern, some technologies (Directed self-assembly (DSA) [1] and Nano-imprint lithography (NIL) etc.) are proposed.

In the case of DSA, it is feasible to make sub-15nm pattern by optimizing a block co-polymer and a guide pattern. However, the current DSA process is complicated and it is difficult to decrease width and line edge roughness of a guide pattern for sub-15nm patterning. On the other hand, in the case of NIL, it is possible to get nanometer structure by preparing a master template recorded with electron beam (EB). However, it is difficult to make the master template having sub-15nm pattern.

This paper describes cost-effective lithography process for making sub-15nm pattern using DSA on a guide pattern replicated by Nano-imprinting (NIL + DSA). Simple process for making sub-15nm pattern with a narrow guide width and small line edge roughness by NIL + DSA is explained. Experimental results after dry etching of hp12nm line/space pattern and some methods to make hp9,5nm line /space pattern will be reported.

2. DIRECTED SELF-ASSEMBLY ON NANO-IMPRINTING GUIDE (NIL + DSA)

Process flow of NIL + DSA is explained. First, quartz template having a guide pattern is produced with EB lithography. The resin of NIL resist material is coated on surface of a substrate. After UV irradiation, the template is separated and the guide pattern is replicated on the surface of the substrate. The width of the guide of 12nm for hp12nm line/space patterning and that of 9.5nm for hp9.5nm patterning are confirmed. Next, the neutral layer material (NL) and the DSA material are coated on the NIL resist guide surface directly. Then DSA pattern is made after baking. Finally, through development process and dry etching process, sub-15nm pattern is made on the substrate.

3. RESULTS AND DISCUSSION

In NIL+DSA process, one of key technical points is NIL resist material. The current NIL resist is easily deformed after coating NL and it is also deformed during baking process. Regarding development process, it is necessary to make not only DSA line but also NIL resist guide line simultaneously. In order to decrease the deformed issue and to improve the development issue, the new NIL resist material has been developed. Using the new NIL resist, quartz templates were made with NIL + DSA process. Line/space pattern of hp12nm was made and its depth was more than 20nm. The line edge roughness was less than 2nm.

To reduce half pitch size, some technologies are tried. One of technologies is using newly developed block copolymer. The other is using the shrink material technology [2]. Line/space pattern of hp9.5nm was obtained.

4. CONCLUSION

For sub-15nm pattering, DSA on a guide pattern replicated by Nano-imprinting (NIL + DSA) was proposed. The quartz templates were made and line/space patterns of hp12nm and hp9.5nm were obtained by NIL + DSA.

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## 9777-20, Session 5

# DSA via hole shrink for 7nm node applications

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Directed self-assembly (DSA) of block copolymers (BCPs) has become a promising patterning technique for 7nm node hole shrink process due to its material-controlled CD uniformity and process simplicity.[1] For such application, cylinder-forming BCP system has been extensively investigated compared to its counterpart, lamella-forming system, mainly because cylindrical BCPs will form multiple vias in non-circular guiding patterns (GPs), which is considered to be closer to technological needs.[2-5] This technological need to generate multiple DSA domains in a bar-shape GP originated from the resolution limit of lithography, i.e. those vias placed too close to each other will merge and short the circuit. In practice, multiple patterning and self-aligned via (SAV) processes have been implemented in semiconductor manufacturing to address this resolution issue.[6] The former approach separates one pattern layer with unresolvable dense features into several layers with resolvable features, while the latter approach simply utilizes the superposition of via bars and the pre-defined metal trench patterns in a thin hard mask layer to resolve individual vias, as illustrated in Fig 1 (upper). With proper design, using DSA to generate via bars with the SAV process could provide another approach to address the resolution issue.

In this paper, DSA of lamella-forming BCP was evaluated as a candidate for forming SAV, which requires the DSA process to support structures from circular via to lines and spaces. The basic process flow is similar to general graphoepitaxy method as shown in Fig. 1 (lower). The morphologies of the DSA vias derived from lamellar BCPs were found to be less sensitive to the BCP coating thickness compared to the cylindrical BCP system of similar L0, as reported by Liu et al. This implies that lamellar BCP may provide a larger process window and higher tolerance for local pattern density variation. The profile and the thickness of the residual PS layer of DSA structures were studied using Monte Carlo simulation and FIB cross-section SEM.

Furthermore, a series of defectivity study using the lamellar system will be discussed, including film stack, DSA, and etch process fine-tuning. Structural and electrical demo using DSA of lamellar BCP and SAV process will be presented. Finally, the benefits and challenges of implementing DSA for 7nm via process will be discusses.

9777-21, Session 5

## New placement estimator for contact hole printed with DSA

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Recent industrial results around directed self-assembly (DSA) of block copolymers (BCP) have demonstrated the high potential of such technique. One of the main advantages of this method is the reduction of lithographic steps printing thus leading to cost reduction. In the same time, the associated correction for mask creation had to account for the introduction of this new technique maintaining a high level of accuracy and reliability.

In order to create Vertical Interconnect Layer (VIA) layer, graphoepitaxy DSA is the main candidate. The technique relies on the creation of confinement guide where the BCP can separate into distinct region and the resulting pattern are etched in order to obtain an ordered contact layer. The printing of the guiding pattern required a classical lithography and optical proximity correction (OPC) is necessary to obtain the best suited guiding pattern for a specific target. Thus it is necessary to perform simulations of the BCP behavior in order to correctly determine contact hole placement.

However most existing model which simulates the BCP phase segregation have a computational cost that is too high and cannot be used to efficiently correct a full layout. In this study, we propose an original compact model that resolves this issue.

The model is based on the calculation of the density probability of PMMA (Polymethyl Methacrylate) domain centers (figure 1). It is compared with both rigorous simulations (based on Otha-Kawasaki model) and experiments as shown in figure 2. For this analysis, test cases are contact shrink and contact multiplication.

The number of PMMA domains inside a structure is also discussed and an analytic formula is derived and compared to experiments (figure 3). The overall consistency of the compact model is presented.

9777-22, Session 5

## Directed self-assembly (DSA) compliant correction flow with immersion lithography

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At 7nm and below, multi-patterning is required before EUV is ready, which presents tough challenges both for printability and cost. Directed self-assembly (DSA) of block copolymer (BCP) is a promising alternative technology to extend optical lithography that it may provide equivalent yields with fewer patterning steps. It uses topological (grapho-epitaxy) or chemical (chemo-epitaxy) guiding patterns to direct BCPs into desired single or multiple uniform features with sizes and pitches being well below the optical resolution limit. In this paper, we focus on the via/contact application with grapho-epitaxy.

Unlike most photo-resists for 193i, the diblock copolymer blend defines the ideal guiding pattern shapes to enable the design targets on wafer. However, various aspects such as DSA process and lithography capability etc. limit the faithful realization of ideal guiding patterns on wafer.

People across the industry are concerned about the printability of the dog-bone shaped guiding pattern, which has been widely used as a type of guiding pattern to create DSA targets in pitches other than the di-block copolymer's natural pitch for via/contact applications. It is very challenging to print the thin neck region with large process window with 193i, which is critical to control the guiding pattern modulation thus defect rates. In addition, due to the non-uniformity of the design, the guiding pattern density would vary from place to place, which will result in non-uniform BCP material fillings across chip. If guiding pattern confinement wells are overfilled so they become connected, and then the DSA proximity effect will influence the outcome of the DSA process in the neighboring guiding pattern confinement wells in terms of placement errors and shapes as well as critical dimensions (CDs).

Furthermore, as expected, new set of design constraints and rules, which are different from those with other technologies such as multiple patterning, would impose on a DSA-compliant design. In particular, people are concerned about mask solutions and patterning capability for designs resulting in randomly slanted-angle guiding patterns.

In this paper, we will touch on DSA-compliant designs and focus on the correction flow including DSA proximity correction and OPC correction. First, we will investigate the grouping impact, one of the DSA-specific characteristics, on the DSA-compliant design and the corresponding decomposition scheme by using via-layer designs from GLOBALFOUNDRIES. Next, we will combine SMO and inverse lithography technology (ILT) with DSA compact model, and demonstrate a correction flow using template error enhancement factor (TEEF) to account for both DSA proximity and optical proximity effects in patterning dog-bone shaped guiding patterns. Finally, different schemes to print assist features will be used to compensate the DSA proximity effects, and the solutions will be assessed by comparing the final DSA holes placement errors and shapes/CDs with Mentor's compact DSA model and MC simulations. Figure 1 shows a SMO/ILT solution when printed assist features are used for DSA proximity effect compensation in printing the dog-bone-shape guiding pattern.

9777-23, Session 5

## Investigation of coat-develop track system for placement error of contact hole shrink process

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Directed Self-Assembly (DSA) is a well-known candidate for next generation sub-15nm half-pitch lithography. DSA processes on 300mm wafers have been demonstrated for several years, and have given a strong impression due to finer pattern results. On the other hand, specific issues on DSA processes have begun to be clear through recent challenges. Pattern placement error, which means the pattern shift after DSA fabrication, is recognized as one of these typical issues.

Coat-Develop Track systems contribute to the DSA pattern fabrication and also influence the DSA pattern performance. In this study, the placement error was investigated using a simple contact-hole pattern and subsequent contact-hole shrink process, implemented on the Sokudo DUO track. Thus, we will show the placement error of contact-hole shrink using a DSA process and discuss the difference between DSA and previous shrink methods.

9777-24, Session 5

## Manufacturability of dense hole arrays with directed self-assembly using the CHIPS flow

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Directed self-assembly (DSA) of block copolymers (BCP) has attracted significant interest as a patterning technique over the past few years. We have previously reported the development of a new process flow, the CHIPS flow (Chemo-epitaxy Induced by Pillar Structures), where we use ArFi lithography and plasma etch to print guiding pillar patterns for the DSA of cylindrical phase BCPs into dense hexagonal hole arrays of 22.5 nm half-pitch and 15 nm half-pitch [1]. The ability of this DSA process to generate dense regular patterns makes it an excellent candidate for patterning memory devices. Thus, in this paper we study the applicability of the CHIPS flow to patterning for DRAM storage layers. We report the impact of various process conditions on defect density, defect types and pattern variability, and also investigate methods to define boundaries of the dense DSA array.

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9777-52, Session PS1

## Nanoimprint lithography using disposable biomass template

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Dilution solvents and cracked gasses generated from resist materials cause transcriptional defects on template materials in nanoimprint lithography. This study aimed to create the novel gas permeable nanoimprint template materials to prevent transcriptional defects by dilution solvents and cracked gasses from nanopatterning materials. A biomass based template was investigated in UV nanoimprint lithography, instead of the conventionally template such as quartz, PMDS, DLC, block copolymers, and polymers. Gas transmission coefficient, light transmission rate, and hardness in cellulose nanofibers were evaluated for transparent template materials with thermal cross-link urethane groups. The approach to use the biomass into template material was expected to be suitable as the next generation of clean separation technology in nanoimprint lithography.

9777-53, Session PS1

## Nano-imprint lithography using poly (methyl methacrylate) (PMMA) and polystyrene (PS) polymers

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Nano-imprinting technology, as one of the most promising fabrication technologies, has been demonstrated to be a powerful tool for large-area replication up to wafer-level, with features down to nanometer scale. This study aims to develop capabilities in patterning nano structure using thermal nano-imprint lithography (NIL). Nano scale Si molds are patterned by electron-beam lithography (EBL) using hard mask and deep etch method. The Poly (Methyl Methacrylate) (PMMA) and Polystyrene (PS) polymers possess a variety of characteristics desirable for NIL, such as low viscosity, low bulk-volumetric shrinkage, high Young's modulus, high thermal stability, and excellent dry-etch resistance. PMMA materials have been utilized for positive electron beam lithography for many years, offering high resolution capability and wide process latitude. In addition, it is preferable to have a negative resist like PMMA, which is a simple polymer with low cost and practically unlimited shelf life, and can be dissolved easily using various solvents to give the preferred film thickness. Polystyrene is such a resist, as it undergoes crosslinking when exposed to deep UV light or an electron beam. Detail process of PMMA and PS polymers using for nano-imprint lithography and silicone mold fabrication will be presented in SPIE Advanced Lithography 2016.

9777-54, Session PS1

## Improvement of sub-20nm pattern quality with dose modulation technique for NIL template production

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Nano-imprint lithography(NIL) is a candidate of next-generation lithography process with low cost and high resolution. NIL is the unmagnified lithography technique using template. Therefore, the lithography performance depends greatly on the quality of the template pattern.

According to ITRS 2013, finer patterns less than 15nm will be required on master template for NIL template production. In order to fabricate finer patterns on master template, higher resolution EB mask writer and high performance fabrication process will be required.

In our previous study, we investigated a potential of photomask fabrication process for finer patterning and achieved 15.5nm line and space (L/S) pattern on template by using VSB (Variable Shaped Beam) type EB mask writer and chemically amplified resist. At the same time, we found that a lowering of a contrast by backscattering is complicating pattern formation. Especially, in sub-20nm patterning on template, beam resolution gets near to pattern size. When finer pattern is located around bright field, energy profile contrast is not enough caused by backscattering from substrate. For semiconductor devices manufacturing, we must fabricate high and low density patterns other than L/S pattern and develop a technique to solve this problem.

In this study, we constructed finer patterning method in bright field area by using dose modulation technique. This technique makes it possible to apply the appropriate exposure dose for each pattern size. Therefore, bright field area is written with low exposure dose and we can evade unnecessary backscattering. As a result, we succeed to improvement the performance of finer patterning in bright field area. These results show that the performance of current EB lithography process have the potential to fabricate NIL template.

9777-46, Session PS2

## Deep-UV interference lithography combined with masked contact lithography for pixel wiregrid patterns

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**Conference 9777:**
**Alternative Lithographic Technologies VIII**

Laser interference lithography is an inexpensive lithographic tool for achieving nanoscale periodic patterns. However, its inability to place arbitrary geometries has been an impediment to its widespread use in several applications. One such application is the pixel wiregrid polarizer, required in polarimetric imaging systems. Pixels of wiregrids oriented in different directions (usually zero, 45-deg, 90-deg and 135-deg) are required to extract the Stokes parameters and the degree of polarization (DOP) from an image. Such polarimetric images are needed in areas such as surveillance, search and rescue and atmospheric sensing. In order to function as polarizers and not as grating reflectors, the wire period has to be significantly smaller than the shortest wavelength of interest in the incident medium. In the infrared spectrum, this is relatively easy to achieve since the dimensions are larger. In the visible spectrum, where most of the applications currently are, the wiregrids must have linewidths smaller than 100nm. The metal, preferably aluminum, has to be at least 50 – 100nm thick to achieve a high polarization extinction coefficient. Such resolutions and aspects ratios present a challenge, especially since these wires have to be placed above the photodetector surface, and has to be performed after the back-end-of-line process. An alternative method is to fabricate the wiregrids on a separate transparent substrate and flip chip bond to the image sensor. Laser interference lithography would be an inexpensive method if it could be performed in combination with a masked system. Unfortunately, the requirement for two beam interference and a steep angular incidence of the beams makes it incompatible with conventional masking methods.

In this work, we demonstrate a 266nm deep-UV interference lithography system combined with a traditional i-line contact lithography to create pixels of wiregrids at different orientations. The deep-UV system is built around a diode-pumped YAG lasers that is quadrupled to 266nm, and the substrate stage utilizes the well-known Lloyds mirror configuration for exposures. First, a uniform periodic line pattern on the entire wafer is created using a deep-UV chemically amplified resist. Then aluminum is deposited, lifted-off, and then masked with an i-line resist to etch away the unwanted areas of the aluminum. The challenge is in making the second and subsequent pixels. For the second pixel, we deposit a thick planarizing layer of molybdenum on the entire wafer, perform the second i-line masked lithography to remove the molybdenum at the second pixel sites and expose the underlying substrate. Then the deep-UV interference lithography is repeated at a rotated orientation. Subsequently, the planarizing molybdenum films are released in hydrogen peroxide without affecting the underlying aluminum wiregrids, but lifting off the overlying aluminum wires.

9777-55, Session PS2

## Resist roughness improvement by a chemical shrink process

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While EUV lithography is expected as emerging technology, still several efforts are required to utilize in actual device production. In such situation, extension of immersion ArF lithography with some supporting materials and processes is realistic choice of lithography technique on current and near future device manufacturing processes. NTD (Negative Tone Development) process is one of the promising solutions for ArF extension. The advantage of NTD process over commonly used PTD (Positive Tone Development) process has been reported in many literatures. .

However, even using ArF immersion lithography on NTD process, CD (Critical Dimension) size achieved is more than 30nm, so that additional technic is being sought to target much smaller resist pattern CD size.

For this purpose, NTD shrink process has been developed as supporting material and process. NTD shrink process is categorized in chemical shrink process which is already widely used on PTD lithography processes and is composed with the following steps such as 1) coating Shrink Material, 2) applying bake step and 3) rinse step to remove Shrink material. Detailed process step was described in previous reports in SPIE 2013 and SPIE 2014.

As the benefits of chemical shrink process, these three items are well known.

1) Reduction of resist pattern CD size

2) Improvement of DoF (Depth of Focus) margin

3) Small pattern pitch bias

As our shrink process is to utilize the phenomenon of intermixing at the interface in between resist polymer and shrink polymer, the component of shrink material could migrate to the surface of resist pattern side wall, then making intermixing layer which is not soluble for the rinse solution to remove pure shrink material, during the bake step after shrink polymer coating onto resist pattern features.

In this paper, we will discuss another benefit of this shrink process, pattern roughness improvement which would be achieved by polymer diffusion. A new shrink material that shows significant improvement of roughness has been developed by controlling migration behavior between resist polymer and shrink polymer and this result was investigated not only by CD-SEM but also by SPM (Surface Probe Microscope).

9777-56, Session PS2

## Attaining precision control over carbon nanotube placement on oxide substrates

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Carbon nanotubes (CNTs) are one of the most promising candidates for high speed, low power electronics. Simulations (1,2) of suitable CNT based transistors require placement of CNTs at very tight pitch (sub 10nm inter CNT distance), to allow for the density scaling and source/drain contact scaling. To achieve this, high density of purified semiconducting CNTs (s-CNTs) need to be precisely placed on oxide substrates. The solution based purification processes yield the highest purity, cheapest s-CNTs and have been used to place the CNTs at ~10^9 cm^-2. However, the current methods rely on multiple expensive lithographic steps, or suffer from instability of CNT dispersions, or have low precise placement yield, etc. Most importantly the conventional techniques lack the ability to control CNT placement and pitch, especially at sub 10nm.

DNA nanotechnology offers a route to bottom-up, parallel self-assembly of CNTs with nanometer precision. However, the challenge of self-assembly of DNA-CNTs on technological substrates still remains unresolved. We have, in the past, demonstrated surface-based self-assembly of DNA wrapped CNTs into viable CNT device geometries using DNA nano structures (3). This talk will address techniques for placement of DNA-CNTs on relevant oxide substrates, with precise orientation and position control, in order to establish their device behavior. Furthermore, first ever fabrication of sub ten nanometer DNA-CNT devices on SiO2 and HfO2 along with their device behavior will be discussed.

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9777-57, Session PS2

## Nanoscale patterning in ambient conditions using liquid electromigration

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In this work, we introduce 'electrolithography' — a new patterning technique based on electric field induced material transport. Electrolithography can be used for drawing patterns having dimensions from a few nanometres to a few hundred micrometres. It does not need any UV or e-beam source, and can be performed in ambient conditions.

Electric current, assisted by Joule heating, can induce long-range flow of material; this phenomenon is known as liquid electromigration. In particular case of Cr thin film deposited on an insulating substrate, application of high electric-field between two point electrodes results in liquefaction and subsequent flow of the liquefied material in a radially symmetric fashion away from the cathode. Electrolithography uses this phenomenon for writing patterns, as described below.

In electrolithography, we use a thin Cr film as a masking layer and a polymer layer beneath it as a pattern transfer layer. A negatively biased scanning probe is used to perform electromigration in the metal film. The conducting tip is moved on the Cr layer in a predefined path to etch metal according to the desired pattern. Once the metal is etched, the polymer layer below it gets exposed. The pattern drawn on the metal layer is transferred to the polymer layer by etching the polymer with an appropriate solvent. Hence, the substrate gets exposed in the desired pattern. Subsequently, the pattern is transferred to the desired material layer using a standard film deposition technique, followed by conventional lift-off process. Same pattern can be transferred to the substrate by etching it also.

Using this technique, best resolutions achieved are of 9 nm on the polymer, and 40 nm on transferring the pattern to another material. Depending on the probe diameter and speed, throughput for this process has been achieved in the range 10^6 to 10^9 μm^2/hour, which is considerably higher than the conventional scanning probe lithography (SPL) techniques. In common SPL techniques, the depth of the patterns drawn on the polymer layer are often very small. Thus, transferring those patterns to other materials becomes very difficult. However, in electrolithography process, etch depth in the polymer is same as the polymer layer thickness (usually ~ 200 nm). Therefore, patterns are easily transferrable and final patterned structures can be as thick as 100 nm, enabling their usage in microelectronic devices. In electrolithography, polymer is used only to transfer the patterns. Hence, any polymer and corresponding developer can be used in this process thereby, removing need of costly and toxic chemicals from lithography processes. We also demonstrate direct writing or resist less patterning for making mask using this technique.

Considering the complexity and the cost of the lithography processes, this technique is far better than the e-beam lithography or ultra-violet based photolithography, which require high energy e-beam or UV sources, ultra-high vacuum and very expensive instrumentation to reach nano-scale resolutions.

## 9777-58, Session PS2

## Complex patterns realized by quantum optical lithography

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Direct Laser Writing (DLW) optical lithography uses photons instead of electrons (Electron Beam Lithography-EBL). Because it is a maskless technique, DLW has a high flexibility, being able to work with various shapes of the patterns. Optical diffraction limit imposes a barrier below 210 nm.

We have developed novel optical lithography instruments, and lithography techniques for the fabrication of complex nanostructures. Quantum Optical Lithography could produce complex patterns at nanoscale dimensions. 1 nm, 2 nm and 5 nm resolution, by optical means, using new materials (fluorescent photosensitive glass-ceramics and ultra-thin QMC-5 resist) have been demonstrated [1-3]. 3D Direct Laser Writing was possible at 5 nm resolution [3].

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## 9777-59, Session PS3

## Control of morphological defects at the boundary between the periodic and non-periodic patterns in directed self-assembly process

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The directed self-assembly (DSA) of block copolymers has demonstrated the ability to generate straight line/space patterns over a wafer-scale area. The chemoepitaxy and/or graphoepitaxy methods are commonly used for aligning the self-assembled lamella domains in one direction. A limitation of the DSA is the difficulty in varying pitch and/or width of the line/space patterns. In this study, we demonstrate how to introduce a non-periodic pattern to the DSA periodic line/space patterns in a relatively simple and inexpensive way. The non-periodic pattern here indicates a wide line structure lying in between the two blocks of 30nm-pitch line/space patterns. Such pattern is desired for memory products.

A hybrid approach that combines chemoepitaxy and graphoepitaxy methods is used to generate PMMA-attractive pinning guide patterns directly from ArF resist. The process steps are as follows (see also Fig. 1 in Supplemental File): 1) 90nm-pitch and non-periodic resist patterns are fabricated on the wafer coated with spin-on-glass (SOG) by ArF immersion lithography, 2) ArF resist patterns are trimmed horizontally and vertically by etching, 3) SOG surface between the resist patterns is covered with neutral layer. Through the etching step at 2), surface of the resist patterns becomes PMMA-attractive. 4) Symmetric polystyrene-block-poly(methyl methacrylate) (PS-b-PMMA) with the natural period of 30nm is spin-coated on the pre-patterned surface, and it is annealed until the vertically-oriented lamella domains are sufficiently aligned with the PMMA-attractive pinning guides. Note that on top of the non-periodic guiding pattern, thin PMMA layer is formed, followed by PS layer. 5) After annealing, PMMA domains are removed by etching, and the remaining PS patterns are used as a template for pattern transfer to the SOG hardmask.

The advantage of this process is reduction of the number of lithographic processes, whereas the challenge is how to prevent from forming fingerprint morphology (i.e., defect) around the boundary between the periodic and non-periodic patterns. For minimizing the defect, first we estimate optimal process conditions (e.g., PS-b-PMMA film thickness) and design of the non-periodic pattern (e.g., width and space) by performing simulations. Our preliminary results from Monte Carlo (MC) simulations show that the film thickness and the space between the periodic block and non-periodic structure affect largely on the formation of fingerprint morphology (Fig. 2 in Supplemental File). Similar effects can be observed in the SEM images obtained from 300mm wafer. Note that the fingerprint morphology often spread over a large area; MC simulations may be computationally demanding. To overcome this issue, we are currently developing a simplified model based on the Ohta-Kawasaki (OK) model. The OK model is grid-based and it can easily be implemented with parallel computing. We will calibrate the model parameters with some top-down and cross-section SEM images, find the optimal process conditions and design of non-periodic pattern, and verify the results with 300mm wafer data.

**Conference 9777:**
**Alternative Lithographic Technologies VIII**

9777-60, Session PS3

## Directed self-assembly of Si-containing and topcoat free block copolymer

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Directed self-assembly (DSA) of block copolymers (BCPs) with conventional lithography is being thought as one of the potential patterning solution for future generation devices manufacturing. Many studies have been reported to fabricate the aligned patterns both on graphoepitaxy and chemoepitaxy for semiconductor applications. [1, 2] Poly (styrene-block-methyl methacrylate) (PS-b-PMMA) has been widely used as BCP platform from some reasons such as relatively simple polymer synthesis, resolution around 12nm half pitch (HP) with reasonable thermal annealing process, and simple surface control for perpendicular orientation. However, there are also the discussions on PS-b-PMMA limitations such as resolution below 10nm HP, roughness, and defect characteristics, which was caused by the weak phase separation kinetics by relatively lower chi value on flory-huggins interaction parameter. As the further research on BCP material, PS-b-PMMA with additives and alternative BCP structure that are having higher chi value than PS-b-PMMA have been suggested to overcome PS-b-PMMA limitation [3-5]. And we also reported the silicon containing BCP with 8.5nm HP resolution and graphoepitaxy hole shrink demonstration, and PS-b-PMMA with additives. [6, 7] On the other hand, technical challenge on the high chi BCP application is orientation control at the both of top and bottom of thin BCP film, especially on perpendicular lamellar orientation. There are some options to obtain perpendicular orientation such as topcoat, solvent annealing, and chemical modification [8, 9], but these candidates would leads the raise of cost and throughput on high volume manufacturing. In this study, we will introduce the newly developed Si-containing high chi BCP which can apply perpendicular lamellar orientation with topcoat free, mild thermal annealing under N2 process conditions.

At first it will be shown in the concept of BCP material design to achieve topcoat free, and mild thermal annealing under N2 process. AB di-block copolymer was designed and modified to prevent surface segregation of one block segment in thin film. Furthermore the Si-containing structure as domain A was applied to obtain high dry etch selectivity and high chi?value. Then fundamental experiment of phase separation in bulk and thin film was carried out, and it was found d spacing=16.2nm lamellar morphology by small-angle X-ray scattering (SAXS) analysis (Fig. 1) and perpendicular lamellar orientation of L0=16.2nm (8.1nm HP) on appropriate neutral brush layer under 180°C-1min. annealing under N2 conditions. (Fig. 2) Thus, it was indicated that newly developed high chi BCP can be achieved topcoat free, Si-containing (etch selectivity), sub-10nm and reasonable thermal annealing at the same time. Finally, experimental results of graphoepitaxy process for L/S multiplication using the high chi BCP will be shown. And it will be discussed on the possibility whether this newly developed high chi BCP become the material solution beyond PS-b-PMMA for sub-10nm HP in terms of the overall characteristics.

9777-61, Session PS3

## Numerical placement analysis in hole multiplication patterns for directed self-assembly

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Directed self-assembly (DSA) is one of the key topics for next generation lithographic technology. DSA has an attractive feature in view of reducing the photo masks because the template patterns can be shrunk or multiplied by self-aggregation of block co-polymers (BCPs). DSA holes fabrication has been researched intensively since it can be reduced critical dimension of the hole and placed in tight pitch. Analysis of the hole placement is significant because the pattern fluctuation cannot be negligible. In our previous researches, we studied DSA hole placement fluctuations computationally induced by thermal motion of BCPs using dissipative particle dynamics in single hole shrink patterns. In spite of technological importance, there are still a few reports in a variety of template conditions. Therefore, we present the results of numerical analysis of the hole placement for pattern multiplication processes in this report.

Figure 1 shows the time-integrated domain image of phase-separated DSA cylinders in grapho-epitaxial rounded-rectangle guide for hole multiplication patterns. By modifying the affinity of side wall and underlayer, the cylinders can be touched on the underlayers. Additionally, two cylinders were clearly separated, which is desirable for pattern transfer processes. Figure 2 shows the results of the cylinder placement analysis on these conditions. Averaged center of connected cylinders were vertically shifted in X direction. This shift was not observed in separated ones without sudden increase of center fluctuation 3σ, called DSA-oriented placement error.

In addition, the effect of guide CD and guide shape on the placements will be discussed in the presentation.

9777-62, Session PS3

## Simulation study of defective states analyzing the polymer chain conformations in direct self-assembly lithography

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One of the major challenges in Directed self-assembly (DSA) lithography is the defect mitigation concerning the microphase separation of diblock copolymers (BCP). Many simulation studies on defectivity in DSA have been reported recently, such as self-consistent field theory (SCFT)[1], dissipative particle dynamics (DPD)[2], Monte-Carlo theory (MC)[3] and approximated mean field theory[4]. These simulations and the wafer experiments[5] have manifested that it is critical to carefully design both the lithographically defined prepatterns and the structures of the BCP chains in order to diminish the defect densities.

In this work, we focus on the conformations of the BCP chains in defective states, such as dislocation, disclination and the grid defects[5], using a simulation method based on self-consistent field theory (SCFT). We found some characteristic BCP chain conformations, which are considered to be related with the origins of the defective states. Figures 1, 2 and 3 show the typical BCP chain conformations observed in single dislocation defects, double dislocation defects, and the grid defects, respectively. In all cases, the terminal segments of BCPs were found to be localized in the encircled specific regions. These results imply that the delocalization of the terminal segments is effective for the defect mitigation in DSA. In order to circumvent the localization of the terminal segments, we studied some preliminary simulation studies on the optimization of the design of the prepattern (topography, surface free energies, etc.) and BCPs (chemical properties of the terminal segments, miktoarm/triblock/additives, etc.).

In the presentation, we will discuss the optimization results of the design of the prepattern/BCPs for low defect densities. And the simulation results will be compared with the experimental results obtained in EIDEC's DSA process.

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9777-63, Session PS3

## Grapho-epitaxial sub-10nm line and space patterning using lamellar-forming Si-containing block copolymer

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Since directed self-assembly (DSA) utilizes self-assembly of polymer molecules, it is considered to be one of the promising candidates to achieve sub-10nm patterning and beyond. The Flory-Haggins chi parameter is an important characteristic index of block copolymers (BCP). In order to obtain fine DSA patterns, block copolymers with high chi value is indispensable. Moreover considering pattern transfer to the underlayers, Si-containing BCPs are preferable because of high etching contrast between Si-containing segment and organic materials.

We have already reported on hp-7nm line and space patterning using cylinder-forming Si-containing block copolymer [1]. In this work, we introduce gapho-epitaxial sub-10nm line and space patterning using lamellar-forming Si-containing BCP. Our patterning method does not need both neutral layer and top-coating material to achieve perpendicular lamellae structure of the BCP [2].

Fig.1 shows CD-SEM images of hp-8nm line and space patters after microphase separation of the BCP. Fig.2 shows cross-sectional SEM images after dry development.

In the conference, pattern transfer to under layer and defectivety will be discussed.

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9777-64, Session PS3

## Sub-10nm lines and spaces patterning using grapho-epitaxial directed self-assembly of lamellar block copolymers

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In order to evaluate a directed self-assembly (DSA) technology for semiconductor device manufacturing, we developed a grapho- and chemo-hybrid coordinated line epitaxy (COOL) process, which requires neither special pinning guide materials nor resist strip process for sub-15 nm line and space (L/S) patterning by using polystyrene-block-poly(methyl methacrylate) (PS-b-PMMA) lamellar block copolymers (BCPs); and we verified DSA process performances such as defects, local placement errors and pattern transfer [1,2]. Furthermore we fabricated half pitch (HP) 15 nm metal wire circuit using the COOL process and fully integrated it onto 300 mm wafers for an electrical yield test, which successfully revealed that metal wire circuits were electrically connected with the 700 ?m metal wire line length [3].

In a next stage, sub-10 nm L/S DSA patterning process, carried out by using grapho-epitaxial DSA [4] of lamellar organic BCPs and Si-containing BCPs, is investigated for the fabrication of sub-10 nm metal wire circuits.

Figure 1 shows top-down SEM images of HP 10 nm L/S patterns using grapho-epitaxial DSA of lamellar organic BCPs, after a micro phase separation. Guides consisting of neutral layers of SiO2 and Si were formed in the heights of 30 nm (Figures 1 (a) and (b)) and 10 nm (Figure 1 (c)). HP 10 nm L/S patterns were formed in the guide spaces of about 2*L0 (lamellar period) and 3*L0. In this study, DSA patterning performance and pattern transfer will be reported.

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9777-65, Session PS3

## High-chi block copolymers for contact hole shrink DSA

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In recent years major advancements have been made in the directed self-assembly (DSA) of block copolymers (BCP). DSA is now widely regarded as a leading complementary patterning technique for future node integrated circuit (IC) device manufacturing and is seriously considered for the 7 nm node. The BCP is directed into the desired morphology using a topographical (graphoepitaxy) or chemical (chemoepitaxy) guiding pattern which can be obtained by conventional 193i or EUV lithography. One of the most straightforward approaches for implementation of DSA is via patterning by graphoepitaxy. Here, the guiding pattern dictates the location and pitch of the resulting hole structures while the material properties of the BCP control the feature size and uniformity. Such a technique has drawn great attention in semiconductor, hard disk drive, and non-volatile memory applications due to its capability for pattern density multiplication and defect rectification.

Tight pitches need to be available for a successful implementation of DSA for the 7 nm node via patterning which requires DSA in small guiding pattern CDs. We will show strategies how to enable the desired CD shrink in these small guiding pattern vias by utilizing high chi block copolymers and controlling the surface properties of the template, i.e. sidewall and bottom affinity to the blocks. Challenges due to the increased mismatch

in the surface energies of the two blocks of high chi BCP will be discussed and solutions towards improved wetting behavior will be shown. The progress to date demonstrates encouraging results, however, in order to gain a deeper understanding of the role of the BCP composition, we systematically analyzed the DSA behavior of a wide range of BCP compositions ranging from cylindrical to lamellar BCPs. The experimental results were corroborated by Monte Carlo Simulations. We found that the DSA process window widens and shifts towards smaller guiding pattern CDs when the volume fraction of the hole forming block is increased whereas the rectification rate is decreased.

9777-66, Session PS3

## Chemoepitaxial guiding underlayers for density asymmetric and energetically asymmetric diblock copolymers

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Block copolymers (BCPs) are a current technology being explored in order to further advance the ability for conventional optical lithography to continue making smaller feature sizes. One method BCP's can be used in this way is to use conventional lithography to form a chemoepitaxial guiding underlayer - an underlayer that is patterned with different regions that are preferential to different blocks of the BCP - and allow the BCP to phase separate on top of the underlayer, increasing the density of the optical lithographic pattern. Much work has been done exploring the optimal design of these underlayers such as exploring the geometry of the patterns and exploring the chemical nature of the different regions. However, these studies typically have been done using BCPs that are composed of two blocks that are relatively similar, such as polystyrene and poly(methyl methacrylate). As the industry advances and higher ? BCPs are sought, the blocks of the BCPs will likely become more dissimilar. For example, new BCPs may have blocks that have different densities or cohesive energy densities which could greatly alter the ability for a chemoepitaxial guiding underlayer to effectively align the BCP. In this work, a coarse-grained molecular dynamics model will be used to explore the effect various BCP parameters have on the ability for traditional chemoepitaxial underlayers to align the BCP. Various hypothetical BCPs will be simulated, such as density asymmetric BCPs, energetically asymmetric BCPs, high molecular weight versus low molecular weight BCPs, and high x versus low x BCPs. These BCPs will be tested on a series of 2x density multiplying underlayers, composed of a one lamellae wide pinning stripe followed by a three lamellae wide background. Both blocks of the BCP will be individually tested as the pinning stripe. A series of underlayers will be formed systematically varying the composition of the BCP in the background region. These simulations will yield the process windows for these underlayers, which will then be analyzed and compared as a function of the BCP properties as well as a function of film thickness.

9777-67, Session PS3

## A route for industry-compatible directed self-assembly of high-chi PS-PDMS block copolymers

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The main difficulties of directed self-assembly (DSA) of block copolymers (BCP) namely, low reproducibility, long processing time and incompatibility with microelectronics fabrication tools (especially for solvent vapor annealing (SVA)) remain still unresolved. High-? PS-PDMS is a promising candidate for DSA due to its high resolution capabilities and the high etching resistance of PDMS. With the prospect to introduce DSA in industry processes, we present here fully industry adapted graphoepitaxy processes for two PS-PDMS BCPs (Mw = 45.5 kg/mol, L0 = 35nm and Mw = 16kg/mol, L0 = 20nm). DSA is performed on trenches within standard silicon antireflective coating/spin-on-carbon (SiARC/SOC) stacks and Si pattern transfer by using plasma etching processes similar to those used for gate etching in industry.

The wetting behavior of PS-PDMS in SiARC/SOC lines have been investigated by GISAXS, STEM and SEM and confirm that the SOC surface favors the good alignment of PDMS cylinders without the need to apply any surface treatment such as a polymer brush. The study concludes further that the trench depth should be sufficiently flat in order to obtain reproducible and well aligned features.

PS-PDMS (45.5k) with its higher molecular weight requires extended thermal annealing at high temperature or SVA in order to be aligned with long range order. We developed a reproducible process of SVA (75min, Toluene) to obtain well-aligned horizontal cylinders within guiding lines. GISAXS measurements confirm a period of 35nm after annealing. Nevertheless, with the objective of industry integration it is necessary to find alternative solutions to Toluene, a toxic and not adapted solvent for industrial production lines. For instance, we propose the introduction of plasticizer molecules into the BCP in order to avoid SVA and to accelerate the process. Plasticizers do not chemically modify the BCP, but increases the chain mobility and allow self-assembly by short thermal annealing even with higher molecular weight.

Having a PDMS etching mask of 15nm width and only about 10nm height, the transfer of the PDMS pattern into the substrate is particularly difficult. Hence, two etching processes have been compared: pulsed HBr/O2 and continuous CHF3/SF6 plasma etching allowing us to obtain Si lines up to 115nm height.

Another very important point for IC production is critical dimension (CD) uniformity and line roughness (LER, LWR). We present first results on the evaluation of PS-PDMS (45.5k) after PS removal by SEM measurements showing a LER of ~17% of CD and a strong influence of the guiding trench width on the LWR of BCP lines.

Finally, in order to be comparable to ITRS requirements, BCP lithography has to present aggressive resolutions. In this prospect, we propose also a fully industry adapted process for a 10 nm half-pitch PS-PDMS (16k) in SiARC /SOC guiding trenches. Due to the advantageous properties our SOC guiding lines, this BCP can be thermally annealed in a fast process (15min) to well aligned, highly reproducible nanocylinders parallel to the guiding pattern. We show here also the anisotropic pattern transfer of the formed 10 nm lines in silicon by CHF3/SF6 continuous plasma etching.

9777-68, Session PS3

## Tunable BCP L0 achievement

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Polystyrene block poly (methyl methacrylate) (PS-b-PMMA) has been successfully used to study process integration requirements when using directed self-assembly (DSA) flows with values of L0 limitation at less than 20-nm. Brewer Science Inc offers a simplified path for implementing chemoepitaxy DSA flows with excellent photolithographic capabilities. We are capable of customizing high chi BCP materials with surface energy matching a comprehensive library of random copolymer brush under-layers. BCP formulations were synthesized using the approach of enhancing the PS block of the BCP material with selective monomers. A complete library of L0 values measuring from standard 28-nm to high chi results with L0 values

of 12-14-nm were synthesized. Using the approach of selective monomer control techniques with complimentary brush layers, lines as small as 6 nm were demonstrated. In addition to high chi properties, our BCP materials have the significant advantage in that no topcoat or solvent annealing is required for alignment of BCPs inside chemoepitaxy guide structures. We accomplished 7x multiplication factor within a pitch of 112 nm spaces having 20 nm wide guide structures. Typical bake anneal conditions are at 140˚-180˚C for 5 minutes to achieve best-case alignment. An optional multifunctional (hard mask neutral layer) HM NL has been synthesized to enhance etch resistance for BCP pattern transfer in a graphoepitaxy flow. Results with either the brush layer or HM NL will be shown for the tunable BCP. We continue to address the industry need to have available a wide portfolio of tunable L0 chemical solutions plus a library of varying neutral layers supporting simplification of implementing DSA technology into complementary lithography process flow.

9777-69, Session PS3

## The effects of surface topography of nanopatterned substrates on the directed self-assembly of block copolymers

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The equilibrium morphology of a block copolymer melt in a directed self-assembly process is determined by a combination of effects stemming from the intrinsic properties of the polymer and the boundary conditions of the system guiding the assembly of the polymer. Chemically patterned substrates have proven to be an effective method for controlling the assembled microphase separated structures and have enabled the fabrication of defect-free features over large areas. However, current fabrication of the patterns used to direct copolymer assembly can create topographic features on the substrate, which are difficult to characterize. The impact of such features on the stability of assembled morphologies is not well known. In this work, a coarse grained model is used to develop an understanding of how small variations in the topography of a chemically patterned substrate changes the stability of defective and desired self-assembled structures. The structures investigated are analogous to morphologies observed in experimental DSA processes. The stability of these structures is characterized by calculating the free-energy of well-defined assemblies using thermodynamic integration. A systematic study of well-defined assemblies, which include grain orientation and dislocation defects, resulting from the DSA of lines-and-spaces over chemically patterned substrates with periodic topographical features is presented. By calculating the free-energies of these well-defined morphologies we identify the substrate architectures that provide the highest selectivity for desired, defect-free assembly. The results of the molecular simulations are compared with experimental findings to elucidate the impact of surface topography on DSA processes using block copolymers.

9777-70, Session PS3

## Hybrid DSA for self-aligned unidirectional wiring applications

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Sub-lithographic patterning extensions of 193 nm immersion lithography are a vital part of semiconductor manufacturing at the 22 nm node and beyond. These techniques are in use for fin, gate via and wiring levels using a combination of self-aligned multiple patterning and multiple exposure techniques. The use of directed self-assembly (DSA) for fin and via patterning has been widely explored as a way to extend 193 nm immersion patterning to the sub 40 nm pitch regime without the complexities of self-aligned triple or quadruple patterning.

In this paper we present the application of DSA patterning to arbitrary unidirectional Mx constructs using the hybrid DSA process (J. Cheng, SPIE 2015). Hybrid DSA uses a neutral hard mask (HM) layer as a template pattern. For PS-b-PMMA, the final pattern after etch is produced by the superposition of the PS phase and the neutral HM material. Self-aligned customization (line cutting) is achieved by removing regions from the neutral HM material before the DSA process.

We explore 3 styles of routing in this work: (1) limited utilization of the tracks adjacent to the power rail, unaligned line ends, (2) limited utilization of the tracks adjacent to the power rail, aligned line ends, and (3) full utilization of the tracks adjacent to the power rail, aligned line ends. In all 3 cases, template generation strategies were developed that resulted in nearly defect free large area patterns.

In contrast to most sub-lithographic patterning extensions, pattern customization is accomplished through the template definition. This enables a single expose template pattern with sufficient resolution to be used without a further cut mask process. The limitation of this technique is that it produces wiring of a single CD. This requires an additional lithography for formation of 2 or 2.5X wires for power distribution. Details of the process and decompositions strategy will be discussed.

9777-71, Session PS3

## Improved cost-effectiveness of the block co-polymer anneal process for DSA

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Block co-polymer (BCP) self-assembly has been explored as a viable patterning option for line-space and contact hole patterning. The major issues that continue to gate the implementation of DSA in the industry are 2 fold: defectivity (and roughness) control and cost-effectiveness.

In our previous work, we demonstrated our results on defect reduction in the 14 nm half-pitch LiNe flow (Figure 1) to 24 defects cm-2, including the DSA and non-DSA defect modes [1]. In spite of the promising trend in the defect reduction strategies of DSA flows, DSA implementation remains a challenge because, low defect levels typically need long BCP anneal durations (typically around 2 hours). This has a negative impact on the throughput of DSA flows and hence their cost-effectiveness.

In this manuscript, we first present a cost of ownership model for DSA that shows the primary factors impacting the cost negatively. To address the issue of long anneals, we present our results on the feasibility study of using a batch anneal process to achieve BCP phase separation in vertical furnaces that are capable of annealing around 150 wafers in parallel. This considerably decreases the total cost of ownership of DSA flows, thus improving its over-all desirability for the industry. The efficacy of the batch anneal process will be judged based on defectivity and roughness performance.

9777-72, Session PS3

## Defectivity study for directed self-assembly (DSA) contact hole shrinkage

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Directed Self-Assembly (DSA) is one of the candidates for scaling feature sizes beyond 10nm node. DSA has shown the capability for pitch reduction, contact hole (CH) shrinks and improvement in pattern profile and pattern collapse margin.1-2 Defectivity is one of the critical criteria for implementation of DSA as a technically viable approach. However, only few defectivity studies of DSA shrink in various topography have been reported.3-5 In this paper, we investigated wafer-level defectivity of DSA shrink at various stages of the DSA patterning process. The contribution from each process step and materials are partitioned and studied using defect source analysis methodology. The DSA defectivity was reduced by optimizing the material quality, surface treatment and pattern transfer processes. Systematic defect sources over the wafer map have been reduced. Finally, the outlooks and challenges of DSA CH shrinkage process will be discussed.

9777-73, Session PS3

## An integrated topcoat and pattern transfer approach for sub-10nm directed self-assembly

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Critical research issues must be addressed in order to push the directed self-assembly (DSA) technology over the tipping point to widespread implementation in nanomanufacturing. A key roadblock is the establishment of proven pathways to realize sub 10 nm resolution, and scaling to 5 nm. Neither the semiconductor industry nor the hard drive industry will implement DSA for a single generation of products. Here, we seek to lower the resolution limit, such that DSA manufacturing processes can serve multiple future generations of products. Whereas substantial effort is being expended by many groups, including ours, to identify block copolymer systems capable of self-assembling into the sub 10 nm regime, technology gaps exist in fundamental and technological understanding as to how those materials may be processed and directed to assemble and continue to meet the constraints of manufacturing.

The polymer physics governing the thermodynamics and dynamics of the DSA process is relatively well understood. For a given material system and annealing conditions the perfection of assembly, and the ability to fabricate structures of the correct size, spacing, and shape (i.e. through film domains with interfaces between domains perpendicular to the substrate) can be directly related to key parameters of the chemical pre-pattern. Much of the fundamental science, development and understanding of the DSA process were carried out using PS-b-PMMA, a system limited in resolution to ~12nm. Fortunately, all the rules of assembly and pattern transfer established for PS-b-PMMA may be applied to other higher-resolution block copolymer systems with minor adjustments. One such adjustment, for example, in systems for which the surface energies of the lamellae-forming blocks are not nearly equal, is to deposit a layer called a topcoat on the top of the block copolymer to illicit nearly equal interfacial energies instead of surface energies.

Here, we report a strategy to use initiated chemical vapor deposition (iCVD) as an effective method to prepare a polymeric topcoat on a high-resolution BCP film. Key concepts of the approach include the ease of deposition, conformal nature, and uniformity of the ultrathin iCVD topcoats, and the development of a pattern transfer process that does not require the topcoat to be removed. The concepts are demonstrated by directing the assembly of polystyrene-block-poly(2-vinylpyridine) (PS-b-P2VP) on chemically pre-patterned substrates with 4x and 5x density multiplication to realize at full pitch pattern dimensions of 18 and 14 nm, respectively. An iCVD topcoat is deposited on top of a BCP film priori to thermal annealing. After deposition of the block copolymer and the iCVD topcoat, and thermal annealing, pattern transfer is enabled by sequential infiltration synthesis (SIS) techniques. Alumina is selectively deposited only in the P2VP domains, not the iCVD topcoat nor the PS domains, with the SIS precursor molecules diffusing through the topcoat. Reactive ion etching allows the topcoat and PS domains to be removed and the pattern of the PVP domains to be transferred into the underlying silicon.

9777-74, Session PS3

## Hexagonal dot patterning using colloidal silica grafted with a concentrated polymer brush

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Directed self-assembly (DSA) using diblock copolymer (BCP) has been attracting much attention as a bottom-up lithography [1]. DSA provides a simple process for making large-area periodic nanostructures, which is expected to be suitable for pattern-template for photonic devices, patterned media, nonvolatile memory, and logic devices. DSA of BCP has been investigated as fine templates having feature size below 20 nm. One of the issues of this fine pattern template is the durability as an etching mask to transfer the pattern onto a substance. The polymer materials' etch-rates are limited by their molecular structures. On the other hand, inorganic nanoparticles have been investigated as an etch-resistant material [2]. Recently we have reported our challenges to apply self-assembly of inorganic nanoparticles for formation of nano-scaled hexagonal dot-array. However, there are several issues for mask application of self-assembled nanoparticle pattern. We focused on two issues; one is the controlling of Van der Waals attraction between the nanoparticles on a substrate, which is an important factor to form an ideal hexagonal dot pattern. We have succeeded to form a well-ordered hexagonal dot pattern using Au particles with polymer grafted onto their surface [3]. The second issue is the film uniformity to solely form single layer of nanoparticles. Neither formation of multi-layered areas nor particle-vacant areas are desirable for mask pattern. By controlling the evaporation speed of the solvent in the dip-coating process, we have managed to fabricate a uniform monolayer film [3].

In this paper we applied previous work for colloidal silica nanoparticle patterning. The colloidal silica is an attractive material for a wider range of particle-size than metal crystals. However, it has been a challenging effort to graft the polymer onto a silica surface with the desired density and molecular weight. Recently, direct polymerization from the surface of the silica particle was developed and we have succeeded in synthesizing silica nanoparticles grafted with a concentrated polymer brush covering on their surface [3]. Using these newly synthesized nanoparticles we investigated the ordering of self-assembly and the monolayer formation.

The monodisperse silica nanoparticles (SiPs) with a diameter of 130 nm were surface-modified with reversible addition–fragmentation chain transfer polymerization. The SiPs were grafted with PMMA having a molecular weight of 59 kg/mol (PMMA-SiPs-59) and 120 kg/mol (PMMA-SiPs-120). Fig. 1 shows the SEM image of the monolayer film of the PMMA-SiPs-59 and PMMA-SiPs-120 using methyl ethyl ketone (MEK) as a dispersing solvent. Hexagonal ordering was obtained in large area. Average pitch size of PMMA-SiPs-59and PMMA-SiPs-120 were 219.5 and 275.4 nm, respectively. The pitch distribution were 3.3 and 8.0 %, respectively. SiPs with the lower-molecular weight polymer show a better hexagonal ordering. The effect of the grafted-polymer to the SiPs ordering will be discussed. We will also discuss on the pattern transfer of hexagonal colloidal mask onto the substrate.

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9777-75, Session PS3

## Reversible nano-lithography for commercial approaches

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One of the two main processes of engineering nanostructures is the top down method, which is a direct engineering method for Si-type materials using photolithography or e-beam lithography. The other method is the bottom-up method, using nano-imprinting. However, these methods are very dependent on the equipment used, and have a high process cost. They are also relatively inefficient methods in terms of processing time and energy. Therefore, some researchers have studied the replication of nano-scale patterns via the soft lithographic concept, which is more efficient and requires a lower processing cost. In this study, accurate nanostructures with various aspect ratios are created on several types of materials. A silicon (Si) nanomold is preserved using the method described, and target nanostructures are replicated reversibly and unlimitedly to or from various hard and soft materials. The optimum method of transferring nanostructures on polymeric materials to metallic materials using electroplating technology was also described. Optimal replication and demolding processes for nanostructures with high aspect ratios, which proved the most difficult, were suggested by controlling the surface energy between the functional materials. Relevant numerical studies and analysis were also performed. Our results showed that it was possible to realize accurate nanostructures with high depth aspect ratios of up to 1:18 on lines with widths from 300–400 nm.

In addition, we were able to expand the applicability of the nano structured mold by adopting various backing materials, including a rounded substrate. The application scope was extended further by transferring the nanostructures between different species of materials, including metallic materials as well as an identical species of material. In particular, the methodology suggested in this research provides the great possibility of creating nanostructures composed of various materials, such as soft polymer, hard polymer, and metal, as well as Si. Such nanostructures are required for a vast range of optical and display devices, photonic components, physical devices, energy devices including electrodes of secondary batteries, fuel cells, solar cells, and energy harvesters, biological devices including biochips, biomimetic or biosimilar structured devices, and mechanical devices including micro- or nano-scale sensors and actuators.

9777-25, Session 6

## Opportunities and challenges for DSA in logic and memory *(Invited Paper)*

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In this paper the opportunities and challenges for integrating DSA for IC manufacturing will be discussed. Aspects for application to logic as well as memory technologies will be discussed. The paper will consider various process flows for integration. All aspects of the integration process for these process flows will be discussed, including process defectivity, design compatibility, manufacturability and cost of ownership.

9777-26, Session 6

## DSA patterning options for FinFET formation at 7nm node

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Directed self-assembly (DSA) of block copolymers (BCPs) is an alternative approach to extend optical lithography, which utilizes a topographical or chemical guiding pattern to direct the BCPs into a desired morphology at a pre-determined location while the material properties of the BCPs control the feature size and uniformity of the resulting structures. Such a technique has drawn great attention in logics, hard disk drive, and memory applications due to its capability for pattern density multiplication and defect rectification. Recent studies on 193i/High Volume Manufacturing (HVM) compatibility, defectivity, and device demonstration of DSA further reinforce its role as a potential candidate for lithography extension rather than merely a lab-scale nanofabrication method.[1-3] However, as pattern density increases, the conventional approach for Fin structure formation in FinFET device fabrication, i.e. removing or preserving one single or multiple lines in a dense array, is limited by the combined effect of CD uniformity, LER/LWR, and placement error control of the lithography system. At 7nm technology node, the required placement accuracy for sub-30nm pitch pattern, such as fin, is approaching the limit of current manufacturing tolerance and design space constraints.

In this work, two DSA options for fin patterning are proposed and discussed. The first approach is the conventional fin-array-plus-cut method, [1] as illustrated in Fig. 1, which is known to be limited by placement error composed of overlay control, LER, and pitch-uniformity. By analyzing the LER along each processing steps, the contribution of each step can be understood and potential improvement are demonstrated. The learning of pursuing fully integrated FinFET device with this DSA patterning approach will also be discussed. The second approach is a hybrid DSA scheme with self-aligned cut by embedded hard mask as demonstrated by Cheng et al.[4] The design concept is similar to the graphoepitaxy process reported previously, [5] except the resist covered region defines the active fins to be preserved as opposed to the grapho case where the non-resist region defines the active fins, as illustrated in Fig. 2. The self-alignment property of the hybrid process alleviates the challenge in placement error, however, new challenges arise, such as the fabrication of the guiding pattern, material optimization, and pattern transfer of the DSA structure into substrate. Preliminary learning and structural results, as well as the extendibility of using DSA for devices with smaller pitches will be further discussed.

9777-27, Session 6

## Defect characterization in templated DSA through electrical measurements

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The use of directed self-assembly (DSA) of cylinder forming block

copolymers (BCP) for contact hole shrink applications has gained increased attention due to the dimensions that can be achieved with this materials and the potential to multiply the density of features obtained with optical lithography. Theoretical and experimental work has focused on engineering the dimensions and surface energy of the templates to obtain straight profiles of the cylinders assembled in them. In addition, the use of assist features has been used to control the pattern density and fill level, which have been identified as critical parameters in this process. Despite these efforts, the impact of process optimization on defect formation are currently measured using scanning electron microscopy (SEM) before and after transferring the BCP features to a hard mask. Even though top-down SEM allows for the initial determination of the process window, the impact of fine changes in the processing conditions on defect formation cannot be captured with this technique, especially as the defect densities approach zero. Therefore, in order to identify the presence of single defects in arrays of various sizes, we use the imec 28nm node via chain electrical test vehicle, Everest, in combination with the templated DSA flow implemented on 300mm wafers. In this work, we used this grapho-epitaxy approach to functionalized the templates with materials of different compositions to tune their surface energy. In addition, we controlled the dimensions of the templates through the exposure conditions and investigated the impact of different pattern densities on a single wafer through the chain structures available in the test vehicle. Finally, the contact holes obtained with templated DSA of BCP were transferred into the underlying substrate and used as test vehicles for advanced metallization processes and submitted for electrical validation.

9777-28, Session 6

## Process highlights to enhance DSA contact patterning performances

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Directed Self-Assembly (DSA) of block copolymers (BCPs) is a promising complementary technique to conventional lithography for advanced patterning [1-4]. Therefore, DSA materials and process continue to be finely tuned in order to ensure patterns of high performances in terms of uniformity, alignment and defectivity and finally meet the requirements of the future technology nodes.

In this paper, we focus on the DSA application for contact hole (CH) patterning using PS-b-PMMA BCP. We highlight the DSA advantages for CH shrink, repair and multiplication which are extremely needed to push forward the limits of currently used lithography. The main goal of our study is to show an overview of DSA capabilities as function of different material properties with optimizing process conditions for each material. Different key parameters were monitored to evaluate the resulting DSA patterning performances which are: CD uniformity (CDU), placement error (PE) and hole open yield (HOY). Our approach is based on the graphoepitaxy inside organic hard mask guiding patterns predefined by 193 immersion lithography. DSA planarization (BCP overfilling and etch back as shown in Figure 1) is employed allowing us to perform patterns of various densities on the same processed wafer (Figure 2) and thus breaking through the barriers of pattern-density related defects encountered with the commonly-used DSA process flow [5,6].

First, we compare CH shrink performances obtained by using a large panel of BCP materials (pure vs. blended BCPs [7], BCPs of different molecular weights). The self-assembly kinetics were also studied for each material by measuring CDU and PE variations after DSA as function of annealing times and temperatures (Figure 3). The latter measurements were based on statistical analysis over thousands of inspected contacts per wafer. These results allow us to accurately determine the best process conditions needed for a specific material formulation and to understand its related thermodynamic behavior.

Furthermore, the HOY, defined as the ratio of valid shrunken holes to total holes, was also determined at each step of the DSA process (guiding, PMMA removal and etching transfer) and over a large inspection scale (millions of inspected contacts per wafer). We report here our latest development work on defectivity for DSA CH shrink. We used both optical and defect-review SEM tools in order to cover a wide range of detected defects and to help for their classification. The HOY parameter would be a good qualification gauge of DSA maturity for high volume manufacturing. Furthermore, the 3D morphology of the self-assembled BCP inside guiding patterns is monitored by cross-sectional SEM on CH shrink features after DSA (Figure 4). Thus, one can anticipate about the related sources of defects observed after the DSA transfer etching to underlayers. These defects are not detectable by top-down SEM inspection after DSA but are revealed after transfer by dry etching. In addition, simulation results on 3D morphology and CD variation as function of BCP morphology are represented and compared to experimental ones. Meanwhile, we monitored key manufacturing process parameters (CD, CDU, Local-CDU and PE) over the time and we showed a good stability of the DSA process.

9777-29, Session 7

## Design and directed self-assembly of Si-containing block copolymers *(Invited Paper)*

C. Grant Willson, The Univ. of Texas at Austin (United States)

Various incredibly clever process tricks based on chemical principles have been devised that extend the resolution limits of photolithography, some of which are already in use in full scale manufacturing. One promising approach is based on the directed self-assembly of block co-polymers. We have tried to design block co-polymers that are optimized for this application and capable of forming structures with minimum dimensions below 10nm in width. Doing so requires blocks with very high interaction parameters, chi, and for some applications, incorporation of silicon in one of the blocks. These high-chi block copolymers form very small structures, but aligning the structures and orienting them in a way that is useful for microelectronics has been a challenge. For example, achieving orientation control by a long solvent annealing process is not compatible with high throughput requirement for microelectronics manufacturing. We have therefore worked to develop new high-chi block copolymers and a DSA processes based on fast, thermal annealing of these materials. A discussion on our progress in the design, synthesis and process development will be presented.

9777-30, Session 7

## Topcoat free orientation control strategies for high-$\chi$ block copolymers

Ankit Vora, Anindarupa Chunder, Gabriela Alva, Noel Arellano, Kristin Schmidt, Teddie Magbitang, Melia Tjio, Hoa Troung, Elizabeth M. Lofano, IBM Research - Almaden (United States); Hsinyu Tsai, Hiroyuki Miyazoe, IBM Thomas J. Watson Research Ctr. (United States); Chi-Chun Liu, Albany NanoTech (United States); Joy Cheng, Daniel P. Sanders, IBM Research - Almaden (United States)

DSA of block copolymers provides a material based solution to extend the patterning capabilities of optical lithography. Although PS-b-PMMA is the most widely used block copolymer for DSA, the minimum half-pitch is limited to ~10nm because of lower interaction and interaction parameter ($\chi$) between PS and PMMA. To enable further feature scaling for the advanced nodes, new BCP materials with higher interaction parameter between two blocks (higher $\chi$) is needed.

In this work, a polycarbonate (PC) containing BCP platform with sub-20 nm pitch resolution for DSA application will be disclosed. To enable perpendicular orientation of the PC-containing BCPs, a new phase-selective, surface active polymer (SAP) additive-based approach was developed. The effect of block copolymer $\chi$, block copolymer architecture (diblock v/s triblock), the composition and loading amounts of the SAP on the self-assembly (SA) of PC containing high-$\chi$ BCPs ranging from 12-26 nm pitch will be described. Finally, the results on pattern transfer and DSA of these materials will also be discussed.

9777-31, Session 7

## Pushing the limit of directed self-assembly and double patterning to 4nm half-pitch and beyond

Shuaigang Xiao, XiaoMin Yang, Yautzong Hsu, Seagate Technology LLC (United States); Stefano Dallorto, Lawrence Berkeley National Lab. (United States) and The Molecular Foundry (United States); Deirdre L. Olynick, The Molecular Foundry (United States) and Lawrence Berkeley National Lab. (United States); Kim Y. Lee, David Kuo, Seagate Technology LLC (United States)

Nowadays prototype nanodevice fabrication requests lithography at the single digit nm level, especially in IC industry and data storage industry. As an example, bit-patterned media as a next-generation magnetic recording technology requires a dense dot pattern of 2 teradot/in2 (corresponding to a sub-10 nm half pitch) as a takeoff point1. It put forwards stringent challenges on pattern formation, pattern transfer and process integration.

By utilizing a highly incompatible block copolymer of polystyrene-block-polydimethylsiloxane (PS-b-PDMS), we have demonstrated 5 teradot/in2 dot patterns (without long-range order) and 12-nm-pitch aligned line patterns previously2. Here ~5 teradot/in2 dot arrays with long-range order (Fig. 1) are further enabled by using a low-topography resist prepattern generated via nanoimprint. Moreover, a 16-nm-pitch line pattern consisting of aligned lying-down PS-b-PDMS cylinders, generated by directed self-assembly (DSA) using a 48-nm-pitch imprinted resist prepattern, is employed for pattern transfer into a mandrel mask forming a sacrificial line pattern at the same density. Atomic layer deposition is then applied for pattern doubling so as to form a final line pattern in SiO2 with a half pitch of 4 nm (Fig. 2). The resist prepattern is found to be critical for the control of DSA pattern parameters such as line space uniformity/line width roughness/line edge roughness. Also tedious experiment on various etch mask materials and etch process conditions is performed to enhance pattern quality. Opportunities and challenges using PS-b-PDMS as a high-resolution DSA material will be summarized finally.

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2. S. Xiao et al., Proc. SPIE 9423 (2015).

9777-32, Session 8

## Directed self-assembly at molecular length scales and the interplay between experiment, theory, and simulation *(Invited Paper)*

Juan J. de Pablo, The Univ. of Chicago (United States)

Directed block polymer self-assembly (DSA) has emerged as a promising strategy for patterning at sub-lithographic length scales. Much progress has been made over the past decade, largely as a result of constructive combinations of experiments, theory and simulation. In this presentation, I will provide an overview of recent calculations that have allowed us to identify the origin of experimentally observed defects, and the pathways that one can engineer to anneal them in a variety of systems. I will also provide a description of newly developed formalism that permits extraction of precise three-dimensional morphology information from x-ray scattering measurements. Throughout this presentation, particular emphasis will be placed on the necessary interplay between experiment and theory that is required to reach meaningful conclusions as critical dimensions and DSA reach molecular length scales.

9777-33, Session 8

## Shape optimization for DSA

Gaddiel Y. Ouaknin, Nabil Laachi, Kris T. Delaney, Glenn H. Fredrickson, Frederic Gibou, Univ. of California, Santa Barbara (United States)

Directed self-assembly (DSA) of block copolymers is used in tandem with lithography in the positioning of features such as VIAs in integrated circuits for connecting different layers. Typical topologies include two parallel VIAs, three parallel VIAs, VIAs arranged in a triangular shape, a L-shape or a V -shape. These VIAs have approximately 10 nm diameters and comparable center-to-center distances. DSA implemented with graphoepitaxy relies on the proper shape of a confined domain in which polymers will self-assemble into the targeted design. Self-consistent field theory (SCFT) optimization is successfully used to predict the resulting morphology given the shape of the confined domain and known physical parameters. However, finding the shape of the confined domain that will result in the proper morphology after self-assembly occurs is largely based on trial and error approaches. We introduce a computational approach that makes use of shape optimization algorithms combined with self-consistent field theory to solve the inverse problem in an automated way. Within this algorithm, the VIAs are detected automatically their sizes, positions, and shapes fed back to the optimization process in order to correct the potential mismatch with the desired target. We will present the method and discuss example calculations in two and three spatial dimensions. We will show how the selectivity on the confined domain's wall, coupled with its optimal shape, enhances the process window for defect free structures. Finally, we will show that our methodology can accurately produce a wide variety of designs that fits the desired target in terms of the number of VIAs, the center-to-center distances and topologies.

9777-34, Session 8

## Modeling and parameter tuning for templated directed self-assembly

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Directed Self Assembly (DSA) on topographical guides, so-called templated DSA, is considered a viable option for patterning Vias, Fins or Metal layer block masks for the 7nm technology node. The exact shape as well as material properties of these templates, or guide patterns, is crucial for controlling critical dimension (CD) and positioning accuracy of the DSA pattern.

Any predictive simulation model of DSA of block co-polymers comprises several free model parameters which must be calibrated to experimental data. Typically, this calibration process must not only reproduce key properties of the DSA material like natural period L0 and the actual morphology (lamellae, cylinder, ...), but also take into account geometric and material properties of the DSA templates, such as the affinities of topographical guides. Here, we demonstrate how the properties of the guide wetting as well as its modeling treatment impact pattern formation. In particular, we analyze the role of guide pattern affinity variations when calibrating our model against experimental grapho-epitaxy results. Further parameters in our models represent the natural period and the phase morphology of the DSA material, for which we explore the significance

within the calibration process.

While a simple phase field model was shown to be satisfactory for common DSA scheme, the so called "weakly- guided " structures however need new model enhancement to prevent local free energy trapping. Inclusion of new model feature can alleviate this at the expense of runtime increase. We demonstrate the effectiveness of this feature to recover from local free energy trapping to a global convergence of this "difficult" structure, that could enable Design Technology Co-optimization (DTCO) study and defect kinetic study.

Due to the fast speed of this DSA model, we found that it is well suited for quantitate DTCO study by demonstrating simulation on large area as well as using post-OPC 3D contours

This work was partly performed in Synopsys Inc.. and IBM Research and Development Facilities.

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9777-35, Session 8

## Virtual fabrication using directed self-assembly for process optimization in a 14nm DRAM node

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For DSA to be deployed in advanced semiconductor technologies, it must reliably integrate into a full process flow. We present a methodology for using virtual fabrication software, including predictive DSA process models, to develop and analyze the replacement of SAQP patterning with LiNe chemoepitaxy on a 14nm DRAM process. To quantify the impact of this module replacement, we investigate a key process yield metric for DRAM: interface area between the capacitor contacts and transistor source/drain. Additionally, we demonstrate virtual fabrication of the DRAM cell's hexagonally-packed capacitors patterned with an array of diblock copolymer cylinders in place of LE4 patterning.

Virtual fabrication has previously been proven accurate and efficient for modeling design-technology interaction in complex process flows, such as 22nm and 14nm logic technology. Since the majority of systematic defect mechanisms are purely physical in nature, virtual fabrication is adept at rapidly exploring the statistical relationships of process variation, and improving yield in the presence of multiple interacting effects. The methodology for virtual fabrication is easily extended to advanced DRAM development, and herein used to analyze the incorporation of advanced DSA processes.

In this advanced 14nm DRAM flow, two different DSA processes are used: a LiNe chemoepitaxy process for active area patterning and a cylindrical multiplication process for the hexagonally-packed capacitor patterning. To predictively model the DSA process for both the LiNe flow and the cylinders, the Cahn-Hillard equation is solved numerically. This has previously been shown to capture block copolymer behavior well when its coefficients are calibrated from experiment or detailed simulation. We demonstrate variations in the DSA process itself, showing the effect on defect density of brush strength, anneal time and pattern commensurability. The computation time for each behavioral DSA modeling step is in seconds and scales linearly with the build area. When integrated into the DRAM process flow, the DSA modeling time is a few minutes compared to the overall integrated virtual fabrication time of roughly one hour.

SAQP and 4x multiplication using the LiNe DSA chemoepitaxy process step are compared as part of the active area patterning of a 14nm 6F2 DRAM design. 20 degree angled lines are patterned at a 193nm lithographic capable 110nm pitch, resulting in 27.5nm final active area pitch. Capacitor contacts, packed on a rectangular grid to fit between word and bit lines, can only make fractional contact with the angled active lines underneath, and are thus highly sensitive to process variation. Virtual fabrication for the nominal case shows that the SAQP module contact area varies up to 50% within the set of contacts, while DSA only 5%. Under 2-sigma variation of lithographic exposure, deposition thickness and over-etch percentage, DSA is similarly found to be far less sensitive with a maximum loss in area of 14% relative to the nominal case, compared to 70% for SAQP.

This analysis validates both the methodology of virtual fabrication for analysis of complex process changes in the face of inherent variation, and the potential integrated benefit of DSA processes over alternative multi-patterning schemes.

9777-36, Session 8

## Effect of underlayer on block copolymer defect annihilation kinetics

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Block copolymers (BCPs) are an attractive material for optical lithography due to their ability to form common geometries (lines and contact holes) at small spacings (> 5 nm). To align these features, a method known as chemoepitaxy is used whereby regions of the underlayer are patterned with preferential and "neutral" stripes to induce guidance. Despite this, the number of defects in phase separated BCP films (i.e. jogs, dislocations, etc) are still high and are a current obstacle in the way of their implementation. The theoretical equilibrium defect density on patterned underlayers is expected to be very low, suggesting the current defect levels are due to kinetic entrapment and highlighting the importance of fast annihilation times of defects. Previous molecular dynamic simulations have shown that defect annihilation is a two step process, first by forming a bridge between domains comprising the defect followed by molecular diffusion to correct the defect. Bridge formation is considered to be the rate limiting step, which implies that by making bridges easier to form, the energetic barrier for annihilation decreases. This paper proposes that this barrier can be lowered by causing one of the BCP blocks to foot due to a preference in the underlayer. This hypothesis is explored by measuring the growth of the persistence length of a lamellae forming BCP film on top of an unpatterned mat of varying composition. In this case, it is assumed that the persistence length of lamellae in a finger-print pattern is a good proxy for the defect density of a patterned film. It is expected that for a more preferential underlayer the persistence length will grow at a faster rate, but reach a lower maximum than if the BCP were on a neutral underlayer. This will suggest that a more preferential underlayer alters the kinetics of annealing defects leading to a larger annihilation rate at the cost of a higher defect density at equilibrium. This hypothesis will be tested both with a coarse-grained molecular dynamic model as well as with experiments using lamellae forming PS-b-PMMA. Films on a variety of unpatterned preferential underlayers will be annealed for varying times and persistence length measured from SEM images.

9777-37, Session 9

## Development of a MEMS electrostatic condenser lens array for nc-Si surface electron emitters of the massive parallel electron-beam direct-write system *(Invited Paper)*

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Developments of a Micro Electro-Mechanical System (MEMS) electrostatic Condenser Lens Array (CLA) for a Massively Parallel Electron Beam Direct

Write (MPEBDW) lithography system are described. The CLA focuses parallel electron beams for fine patterning. The structure of the CLA was designed on a basis of analysis by a finite element method (FEM) simulation. The lens was fabricated with precise machining and assembled with a nanocrystalline silicon (nc-Si) electron emitter array as an electron source of MPEBDW. The nc-Si electron emitter has the advantage that a vertical-emitted surface electron beam can be obtained without any extractor electrodes(1).

We have developed an electron optic column of the prototype MPEBDW to expose 10 000 pixels of 10 x 10 nm2 size on the target(2). The schematic of the column shown in Fig.1 is the reduction electron optic system which consists of the 100 x 100 nc-Si electron emitter array integrated with active matrix LSI, the CLA, an anode, and an objective lens (OL) as a reduction lens. The cross-sectional structure of the CLA is shown in Fig. 2. The CLA provides the parallel electron beams with small divergent angles to diminish a spherical aberration(3) caused by a high reduction factor (1/100) of the OL. Figure 3 shows a simulation result that the CLA focuses the vertically emitted surface electron beam from the nc-Si electron emitter. Since the electron optics is cylindrical, the electron trajectories in the upper half are indicated. A distance from CLA and a beam accelerating voltage of the anode are 36 mm and 5 kV respectively. The simulation shows that the proposed structure can focus the beams with size of less than 1/10 of the emitted beams at adjusted electrical potentials indicated in the Fig. 3.

The CLA shown in Fig. 4 was fabricated using the precise machining processes. A 70 μm-thick copper film was deposited on a 0.1 mm-thick glass epoxy substrate. Through-holes with a diameter of 60 μm were formed by micro-drilling the substrate. The CLA is formed by fixing three substrates in the accurate position (Fig. 2). The spacers shown in Fig.4 adjust the gap between the electron emitter array and the CLA to 100 μm. Figure 5 shows one of the spacers measured by a digital microscope. The CLA was assembled with nc-Si electron emitter array to evaluate the characteristics of the electron optics and to compare the experimental results with the simulations.

9777-38, Session 9

## Non-CAR resists and advanced materials for massively parallel e-beam direct-write process integration

Marie-Line Pourteau, Isabelle Servin, Bernard Dal'Zotto, Philippe Essomba, Kevin Lepinay, Jonathan Pradelles, Ludovic Lattard, CEA-LETI (France); Pieter Brandt, Marco Wieland, MAPPER Lithography (Netherlands)

The emerging Massively Parallel-Electron Beam Direct Write (MP-EBDW) is an attractive high resolution high throughput lithographic technology, targeted to address 90 nm to 14 nm technology nodes. CEA-Leti is leading a collaborative program since 2009 to support this mask-less technology developed by MAPPER Lithography; their 300 mm pre-production tool FLX-1200 has been installed in CEA-Leti cleanroom in 2014, targeting a throughput of 10wph. In particular, CEA-Leti is developing the process and integration aspects required by this multi-beam approach.

A complete stack has already been qualified for FLX-1200 tool, including high sensitivity CAR resist, SOC and Si-HM underlayers, and an outgassing mitigation top-coat layer. The focus was put on CAR resists for their very high sensitivity, aligned with FLX-1200 requirements, and their ready-for-industry production status as they are derived from EUV resist platforms. Nevertheless E-beam CAR resists are still limited by the Line Width Roughness (LWR). Even though the LWR is comparable to EUV's achievements, it remains above the ITRS specifications (< 8% of CD, leading to LWR < 3.4 nm at 28 nm node). Biasing the design improves the LWR, but brings the dose-to-size out of specifications. Furthermore, we demonstrated that the top-coat layers tested, while clearly reducing the resist outgassing rate, slightly degraded the lithographic performances of the stack, showing some dark erosion and a slightly increased LWR.

This paper presents alternative advanced materials that have been investigated to improve the performances on those aspects. Non-CAR resists show lithographic improvements in terms of resolution and LWR reduction; they also show recent sensitivity gain which is expected to fit MP-EBDW specifications. Several experimental products have been tested. A new top-coat has also been tested for its lithographic performances and compared to the previous products. Key parameters such as dose-to-size, resolution, contrast, LWR, and energy latitude have been monitored.

Besides the lithographic stack, a conductive Anti-Charging Layer (ACL) might be needed to dissipate the charges in MP-EBDW systems. The conduction capability and integration into the lithographic process of a new spin-coatable material were investigated.

A pre-screening of all these products has been performed on 50kV variable-shaped-beam or 100kV Gaussian electron beam VISTEC exposure tools to set out the processes, before the fine tune and final tests on the Mapper FLX-1200 5kV system.

9777-39, Session 9

## Complete data preparation flow for massively parallel e-beam lithography on 28nm node full-field design

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Massively parallel mask-less electron beam lithography (MP-EBL) offers a large intrinsic flexibility at a low cost of ownership in comparison to conventional optical lithography tools. This attractive direct-write technique needs a dedicated data preparation flow to correct both electronic and resist processes. Moreover, Data Prep has to be completed in a short enough time to preserve the flexibility advantage of MP-EBL.

While the MP-EBL tools have currently entered an advanced stage of development, this paper will focus on the data preparation side of the work for specifically the MAPPER Lithography FLX-1200 tool [1-4], using the ASELTA Nanographics Inscale® software. The complete flow as well as the methodology used to achieve a full-field layout data preparation, within an acceptable cycle time of less than 24 hours, will be presented. Layout used for Data Prep evaluation was one of a 28 nm technology node Metal1 chip with a field size of 26x33mm?, compatible with typical stepper/scanner field sizes and wafer stepping plans.

Proximity Effect Correction (PEC) was applied to the entire field, which was then exported as a single file to MAPPER Lithography's machine format, containing fractured shapes and dose assignments. The Soft Edge beam to beam stitching method was employed in the specific overlap regions defined by the machine format as well. In addition to PEC, verification of the correction was included as part of the overall data preparation cycle time (see Figure 1 for data prep flow overview). This verification step was executed on the machine file format to ensure pattern fidelity and accuracy as late in the flow as possible. Verification over the full chip, involving billions of evaluation points, is performed both at nominal conditions and at Process Window corners in order to ensure proper exposure and process latitude (see Figure 2).

Resulting file size and shapes count after the complete data preparation flow will be presented first. Simulation results over process parameters variation such as exposure dose and tool spot size are then investigated as part of the process window corner verification. This work demonstrates that a complete MP-EBL data preparation flow is achievable for a 28 nm node layout within 24 hours while ensuring the product specifications.

The research leading to these results has been performed in the frame of the industrial collaborative consortium IMAGINE driven by CEA-Leti.

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9777-40, Session 9

## Demonstrating multi-beam lithography for 28nm technology node

Ludovic Lattard, Jonathan Pradelles, Isabelle Servin, Marie-Line Pourteau, Laurent Pain, CEA-LETI (France); Marco Wieland, Marcel Van Kervick, Guido De Boer, MAPPER Lithography (Netherlands)

The emerging massively parallel Electron Beam Direct Write (EBDW) is an attractive high resolution-high throughput technology, targeted to address 90 nm to 14 nm technology nodes. CEA-Leti is leading a collaborative program since 2009 to support the mask less technology developed by MAPPER Lithography; its 300 mm pre-production platform FLX-1200 has been installed in CEA-Leti cleanroom in 2014. In particular, CEA-Leti is developing the process and integration aspects required by this multi-beam approach.

Multi-beam lithography has now reached a high level of maturity and CEA-LETI is focused to demonstrate FLX-1200 as a production tool for 28nm technology. Mapper has shown performance improvement for the tool FLX-1200 in terms of productivity and beam qualification2.

Leti evaluates the FLX-1200 tool performance and the performance of each individual beam to have a full focus on beam characteristic. Beam metrology will be a key enabler to demonstrate yielding chip with Mask Less Lithography (ML2). Leti will demonstrate beam characteristic with embedded metrology and inline metrology. The most important parameters for beam characteristics are the following: beam position on Grid, beam angular error for each beam and current measurement.

Thanks to the collaboration with IDM partner CEA-LETI was able to demonstrate the integration scheme which is required for a 28nm production flow CMOS product including etch process optimization.

CEA-Leti and EDA partners were able to demonstrate a full flow for data preparation i.e. e-beam proximity correction, fracturing in oasis.mapper file format and verification through the process window. Thanks to this demonstration CEA-LETI was able to process the data preparation flow for a 28nm product with a full field coverage of 26x33mm in an acceptable time for production environment.

The research leading to these results has been performed in the frame of the industrial collaborative consortium IMAGINE driven by CEA-Leti.

9777-41, Session 9

## Requirements of the e-beam shot quality for mask patterning of the sub-1X device

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As the integration node becomes smaller in ArF generation of optical lithography, the complexity of the optical proximity correction (OPC) continues to grow and pattern design is subject to more aggressive modification, for instance, in inverse lithography technique (ILT), towards the effect of achieving greater fidelity to the target design on wafers. The complexity level of mask patterns is determined by original design as well as the OPC that the original patterns go through. The number of corners is generally used to assess the pattern complexity for both original design and OPC-ed design. In addition, the degree to which assist features are created in OPC-ed design serves as another index to represent the pattern complexity.

From the perspectives of patterning on masks, the complexity of mask patterns is said in terms of the shape of a shot – the unit of electron-beam exposure in variable shaped beam (VSB) writers, and the distribution of shot sizes. Increased number of corners and assist features raises the fraction of small shots in e-beam data which contain the shot information. In 1X nm logic device, the fraction of small shots below 20 nm is about 20% and this number is expected to increase in sub-10 nm device because of smaller features and aggressive OPC. The typical size of a main pattern in extreme ultraviolet (EUV) masks being a few tens of nm, the patterning quality will become more critically affected by small shots.

In this article, results of study aimed at evaluating the small shot handling capabilities of e-beam machines are presented. The study taught us that the number of small shots (of size less than 20nm) generated during data fracturing has to be considered as a factor that defines the complexity of patterns in e-beam writing. Applying this definition to project the pattern complexity in sub-1X devices, it shows that the small shot printing in e-beam machines need to be improved in order to guarantee acceptable mask pattern quality. Developing a new data fracturing scheme and advanced e-beam technology for handling small shots are among potential candidates to achieve this.

9777-42, Session 9

## Prediction of positioning error due to resist charge up effect on photomask in EB lithography

Masaki Kimura, Meisei Univ. (Japan)

Photomask is fabricated with 50keV EB. The position accuracy of photomask is degraded to max ±10nm by the deflection of EB due to resist charge up effect. The required accuracy is ±3nm1). This study is about the position shift caused by the resist charge up effect with simulation method.

The mask consists of resist, earthed metal film and quartz substrate from the incident side of EB. Charges are produced in the resist and inside the quartz by the EB irradiation. The charge in the quartz is shielded by the earthed metal film. The charge in the resist operates as electric dipole vertical to the mask by electron image effect from the earthed metal film. We propose the electric dipole distribution deflects the orbit of EB, and deteriorates the position accuracy. In this study, we have simulated the deflection of EB by the dipoles produced in resist and obtained the dipole distribution that led to the position shift of experiment.

We made orbital calculation simulation program about the electron beam deflected by the electric field formed by various types of dipole distributions. We simulated the position error from basic distribution module of the dipoles. First we calculated the shift from one dipole. We define x, y coordinates in the resist plane and z vertical to the plane. The dipole moment is in the z direction. As a basic distribution, we calculated the position shift of EB emitted at x from the dipoles which are long arrayed linearly along y axis at x0. We denote the shift f(x) (response function). Furthermore, we denote dipole distribution g (distribution function) where the above distribution extends along the x direction with various densities for a limited width. The position shift of the EB from these dipole distributions can be obtained as a function of x as

$$(f*g)(x) = \int_{\tau} f(\tau) g(\tau - x) d\tau$$

We chose the experimental result of the position shift of the test pattern shown by Babin group in reference2) for the evaluation of our dipole distribution model. Long load pattern along the y direction is written by the exposure with a fixed dose. Measurement points are set up along the x direction and the position shift at x is measured. The result of this experiment is treated as one dimension. From the above relation of the

convolution we have obtained the dipole density distribution for the long load pattern.

We constructed the dipole distribution model that led to the measurement result of position shift. The position shift occurred by the dipole distribution depends on writing pattern. As for 50keV electron beam, the displacement becomes linear phenomenon and fast computation from convolution becomes possible.

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9777-43, Session 10

## A paradigm shift in patterning foundation from frequency multiplication to edge placement accuracy: A novel processing solution by selective etching and alternating-material self-aligned multiple patterning

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Complementary lithography, in which a spacer based SAMP technique is used to pattern the high-density 1-D grating array while several cut steps help to form the desired structures, faces severe challenges of edge-placement inaccuracy. Apparently, a satisfactory edge-placement yield of the cut-hole patterning process is critical for its future success. In this paper, we propose a novel approach to significantly reduce the edge-placement-error (EPE) effect by combining selective etching and alternating-material self-aligned multiple patterning (altSAMP) processes.

The line arrays fabricated by an altSAMP process will be made of two different materials (e.g., A and B), which is different from the conventional SAMP processes wherein the final lines/spacers are made of the same material. As shown in Fig. 1, a line array arranged in an alternating order A-B-A-B... can be fabricated by an alternating-material self-aligned quadruple/octuple (altSAQP/altSAOP) patterning process, while a line array arranged in a quasi-alternating order A-B-B-A-B-B... can be fabricated by a self-aligned triple/sextuple (SATP/SASP) patterning process. Consequently, we can decompose the holes over the lines made of material A into one mask, while arrange the holes over the lines made of material B into the other mask, as illustrated in Fig. 2. Since the targeted-line density for each decomposed mask (e.g., in an altSAQP process) is half of the original array, and a following highly selective etching process to cut the targeted lines (ideally) will not attack the neighboring non-targeted lines, we expect more severe EPE can be tolerated.

Nevertheless, the actual material loss (and consequently the patterning yield loss) of non-targeted lines depends on the etching selectivity and miscut amount (see Fig. 3(a)). Therefore, it is necessary to develop a physical model to quantify the corresponding cut-process yield loss. In particular, the cut-hole overlay errors (e.g., x), cut-hole and grating line/space CD variations (e.g., y, z1, z2) are the main impact factors, as shown in Fig. 4. We assume the probability of a cut failure (POF) is a linear function of the material loss of non-targeted lines determined by the ratio of the etched area (e.g., gd) to the total cross-sectional area (e.g., GD) of a line (see Fig. 3(b)). We also assume the probability density function is correlated to x, y, z1 and z2 in a Gaussian form, and the cut-process yield can be calculated.

According to Fig. 5, we can optimize the process parameters (e.g., overhang as indicated in Fig. 4) to improve the cut patterning yield. Our calculations (see Fig. 6) show that the cut-process yield using a conventional single-material SAMP process is very low at sub-7nm half pitch, and the proposed solution can significantly improve the patterning yield and potentially extend the complementary lithography for 1 or 2 more generations.

9777-44, Session 10

## Contact hole patterning by electric-field assisted assembly of core-shell nanoparticles

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Aggressive scaling of contact hole features without loss in critical dimension (CD) uniformity or pattern placement accuracy has been a significant challenge for traditional optical lithography. Efforts have been made to develop alternative nanoscale patterning techniques, including directed self-assembly (DSA) of block copolymer, nanoimprint and maskless direct-write electron beam lithography. Ultra-high-resolution features can be achieved by these techniques. However, the adoption of these techniques has been limited by factors such as overlay error, limited pattern complexity, defects, and/or low throughput.

Here, we demonstrate a new technique to create arrays of uniform contact hole patterns by electric-field assisted assembly of core-shell nanoparticles. A spatially varying dielectrophoretic (DEP) force produced by lithographically defined guiding features is used to assemble nanoparticles with tight size control and high core-to-shell etch selectivity within the predefined features. In this strategy, the half- and full-pitch of the contact hole array is defined by the starting nanoparticle core and shell diameter rather than by lithography.

This work evaluates the self-healing potential of this technique by exploring a range of guiding features with CD non-uniformities inherent in aggressively scaled optical lithography. A range of guiding features were investigated, including merged circular patterns, well-separated circular patterns with equal diameters, and well-separated circular patterns with unequal diameter. The center-to-center spacing of the adjacent circular features was equal to the particle diameter. The particle arrays assembled using each of these guiding features are nearly identical to one another. This shows that particle placement is determined by the center-to-center spacing rather than the size and shape of the guiding feature, which provides a route to heal non-uniformities in the lithographic pattern for subsequent pattern transfer steps.

9777-45, Session 10

## Single-step patterning on inclined surfaces with ensured alignment for 3D nanofabrication

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Progress in nanofabrication techniques plays a key role in the growth of nanotechnology and its applications. The capabilities of three-dimensional (3D) structures are less explored because of the difficulties in their realization. Current nanostructure fabrication is usually limited to planar structures as they are defined by a planar mask. In order to realise 3D nanostructures by etching one needs technologies beyond planar masks. Hence we present a method to pattern inclined surfaces in a single step. We use focused ion beam milling to make a 3D etch mask that enables us to fabricate a large variety of 3D nanostructures for nanophotonics, opto-electronics and sensing [1].

The patterning is performed in a hard-mask layer that is deposited on two adjacent inclined surfaces of a Si wafer. The pattern that is being projected on the inclined surfaces consists of two 2D patterns called a an b. Therefore the mutual alignment between both patterns on the inclined surfaces is ensured in the design. The 2D patterns a an b for the different surfaces can be completely independent and still be in perfect mutual alignment.

As a proof-of-concept we demonstrate a patterning procedure for a 3D mask to fabricate 3D photonic band gap crystals in silicon. We show that the fabricated crystals reveal a broad stop photonic gap in optical reflectivity measurements. We propose patterns for 3D nanostructures

with five different Bravais lattices, namely cubic, tetragonal, orthorhombic, monoclinic, and hexagonal. We demonstrate a mask for a 3D hexagonal crystal, and the mask for a diamond-structured crystal with a 3D array of cavities. We observe an alignment accuracy better than 3.0 nm between the 2D mask patterns on the inclined surfaces, which permits one to fabricate well-defined monolithic 3D nanostructures with high accuracy.

9777-47, Session 11

## Enhanced patterning by tilted ion implantation

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Double-patterning techniques allow features with higher density to be achieved, but require additional process steps with significant associated incremental cost [1]. In this work, tilted ion implantation (TII) is proposed as a lower-cost approach for achieving sub-lithographic features and for pitch-halving in a self-aligned manner, in comparison with spacer lithography [2], also known as self-aligned double patterning (SADP) [3].

The basic concept is to use ion implantation to enhance the etch rate of a thin masking layer, and to perform the implant(s) at a tilted angle to achieve sub-lithographic implanted regions that are self-aligned to pre-existing photoresist or hard-mask features over the masking layer on the surface of a wafer. An exemplary process flow, in which silicon dioxide (SiO_2) is used as the masking layer together with overlying linear amorphous silicon (a-Si) hard-mask features, is illustrated in Fig. 1: (a) a first implant is performed at positive tilt angle to selectively damage portions of the masking layer to the left of the hard-mask features, (b) a second implant is performed at negative tilt angle to selectively damage portions of the masking layer to the right of the hard-mask features, (c) the implanted regions of the masking layer are selectively removed in dilute hydrofluoric acid (HF) solution [4], resulting in a masking layer with etched features of average pitch equal to one-half the pitch of the a-Si features. The length of each implanted region is x ~ W_trench – y(tan(θ) + cot(a)) where W_trench is the base spacing between a-Si features, c is the tilt angle, y and a are the hard-mask height and sidewall angle, respectively.

Fig. 2 shows that the etch rate of a 5 nm-thick SiO2 layer can be enhanced by almost 10x, by Ar+ implantation at 1.5 keV acceleration energy and 3E14 cmˆ-2 dose. For initial proof of concept, a single 15-degrees-tilted Ar+ implantation step was performed on a wafer with features as illustrated in Fig. 1(a). Afterwards it was subjected to a dilute-HF etch followed by a silicon reactive ion etch (RIE) to allow the implanted regions to be easily distinguished under a scanning electron microscope (SEM). The cross-sectional SEM image in Fig. 3(a) demonstrates that TII is effective for achieving sub-lithographic features (~45 nm wide in this initial experiment). Considering that the height of the a-Si hard-mask features was reduced during the RIE step, the width of the selectively etched features is in accordance with expectations, as shown in Fig. 3(b). The plan-view SEM image in Fig. 3(c) shows that the features defined by TII are self-aligned to the edges of the hard-mask features, i.e. the edge shape of the a-Si hard mask is reproduced with good fidelity.

Fig. 4 and Table I compare the number of steps and costs associated with the TII approach, against those of SADP. The TII approach is much less costly, and does not require new or aggressive process capabilities. Therefore, it should be straightforward to implement in high-volume manufacturing to help extend Moore's Law.

9777-48, Session 11

## Exploring the potential of multiphoton laser ablation lithography (MP-LAL) as a reliable technique for sub-50nm patterning

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The laser ablation of polymeric films when introduced in early 1980s was envisioned as an attractive alternative lithographic approach especially for direct writing applications. Nevertheless, the critical dimensions demonstrated so far with this technology are usually higher than several hundred nanometers and its penetration in the lithography field is mainly limited to the fabrication of specific microsystems and to master preparation for optical discs. On the other hand the last 15 years an increasing interest has been devoted to ultra high resolution patterning with laser multiphoton lithography based on polymerization processes, which however has not significantly affected the state of the art in laser ablation patterning.

Recently we started exploring possibilities of laser ablation for ultra high resolution patterning and a paper entitled 'Multiphoton Laser Ablation Lithography (MP-LAL) using 375 nm Continuous Wave Laser Enabling Patterning down to the 30 nm Regime and beyond' has been accepted for presentation at MNE conference (Hague, September 2015). We have demonstrated a Laser Ablation process using a CW diode laser source (375nm) to expose a dye-doped poly (methylmethacrylate) (PMMA) film allowing nanopatterning at the sub 100 nm regime with potential for even sub30 nm structure formation. The polymeric material formulations comprised perylene molecules which absorb in the exposing laser wavelength, where the polymeric matrix is transparent. The combination of a non-linearly responsive material with a focused continuous laser beam (the laser ablation experiments were conducted using a r-Theta Laser Lithography/Exposure Tool developed by Opticon/Greece for NanoTronix/USA) has as a result the creation of holes in the polymeric material and Nickel pillars after metallization down to the sub 25 nm regime. The Ni metallization process includes 100nm Ni films through thermal evaporation and subsequent electroplating to create hard masks.

Despite the satisfactory ablation results of perylene-doped PMMA, issues like structure quality and process reliability need to be addressed. In this work, new tailor-made methacrylic copolymers and polymer/dye formulations with optimized characteristics are developed to improve the control of the multiphoton laser ablation process. The most known problem in laser ablation lithography is the berm-production around the created hole which can be addressed by tuning the polymeric material properties including Tg, dye distribution in the polymer matrix and adhesion of the substrate. The copolymers have to show good adhesion to the glass wafer used but after the metallization process should be easily removed from the nickel stamp. The methacrylic copolymers contain monomers bearing groups that are especially selected to improve material properties, whereas the synthetic routes adopted allow effective control of their composition. Capability for creating arrays of well-defined sub 50 nm Ni pillars free from berm problems has been demonstrated using the developed polymeric material and continuous wave 375 nm multiphoton laser ablation lithography (MP-LAL). Further materials development work is under way for optimizing properties such as etch resistance to enable the transfer of the technique to diverse lithographic applications.

**Conference 9777:**
**Alternative Lithographic Technologies VIII**

9777-49, Session 11

## Complementary patterning using plasmon-excited electron beamlets

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Optical lithography transfers fixed geometric patterns from a photo mask to photoresist wafers. Current tools cost more than 50 million US dollars each, and much more for the masks. To keep up with Moore's law, future tools and processes will become increasingly expensive. The achievable half pitch of hole patterns in projection lithography is always larger than what can be resolved for lines and spaces, and the current patterning process cannot provide a cost-effective way to pattern small via and contact holes at advanced nodes. The next-generation extreme-UV tools have sufficient resolution, but current pilot tools will need substantial upgrades in source and process infrastructures to have sufficient throughput and yield.

Complementary patterning using focused electron beams has emerged as a potential approach to meet the industry's patterning needs at advanced nodes. Focused electron beam writers can direct pattern semiconductor chips at very high resolution without the need of expensive photomasks but only in low throughput. Practical throughput in focused electron beam lithography is possible only by using massively-parallel electron beamlets, however researchers have not been able to find a robust method to generate and utilize a massive number of beamlets with satisfactory brightness and uniformity.

Here we report our recent research progress aiming to enable massively-parallel electron-beam lithography by using a novel nanoscale electron beam source array. We use plasmonic lenses to excite and focus surface electron waves to generate massively-parallel electron beamlets (Nature Nanotech. 3:733, 2008; Sci. Rep. 1:175, 2011; JVST B. 31:041601, 2013; Opt. Lett. 40:3918, 2015). Specifically, the proposed SPEP device consists of an array of plasmonic lens and electrostatic micro-lens pairs. Each pair independently produces a beamlet. During lithography, optical modulator dynamically controls the light incident onto the plasmonic lenses. The photons incident onto each plasmonic lens are concentrated into a diffraction-unlimited spot to excite the local electrons above their vacuum levels. Meanwhile, the electrostatic micro-lens extracts the excited electrons to form a focused beamlet, which can be rastered across a wafer to perform maskless lithography in mass quantities. We investigate the fundamentals of localized electron excitation, build a proof-of-concept nanoscale source array and implement the device to demonstrate lithography.

9777-50, Session 11

## Dots-on-the-fly electron beam lithography

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We demonstrate a novel approach for electron-beam lithography (EBL) of periodic nanostructures. This technique can rapidly produce arrays of various metallic and etched nanostructures with line and pitch dimensions approaching the beam spot size. The approach is based on often neglected functionality which is inherent in most modern EBL systems.

Rather than defining the dimensions of the shapes themselves, the raster/vector beam exposure system of the EBL software is exploited to produce arrays of pixel-like spots. In addition to simple arrays of nano-dots as described before, we expand the technique to produce more complex, highly tunable arrays and structures. Concentric metallic rings, hexagons, rectangles and rhomboids as well as several novel combinations of shapes have been produced in resists for both metal lift-off and etching processes. Metallic structures were fabricated on silicon substrates as well as on ITO and FTO coated glass. Etching was performed on silicon.

The single-pixel nature of this approach allows easier minimizing of line-width and pitch compared with traditional EBL techniques. Since multiple objects are defined by a single pattern element, software resources are reduced significantly, allowing larger arrays than traditional EBL methods. Additionally, patterning times for select geometries can be reduced by up to 3 orders of magnitude.

Concentric circular arrays of nano-dots were fabricated with dot spacing as small as 40 nm for 30 nm dots. By varying the annular and radial spacing of dots, a wide variety of configurations can be produced. We have modeled the resulting configurations with a Matlab code and verified a large range of novel emergent shapes. By sufficiently reducing the annular dot spacing, it is possible to obtain continuous rings separated radially by nano-scale gaps. We demonstrate the dots-on-the-fly approach with a Zeiss Ultra Plus scanning electron microscope equipped with Elphy Plus add-on from Raith.

Continuous metallic nanorings were fabricated to a minimum inner radius of 30 nm. The line-width of the nanorings can be adjusted from approximately 20 nm up to nearly 100 nm. A minimum separation of approximately 40 nm between concentric rings has been achieved for up to ten rings.

Large, concentric metallic rings were fabricated with line-width of approximately 20 nm, separation of 80 nm and largest ring diameter of approximately 35 μm. Concentric rectangular, rhomboid and hexagonal structures have also been fabricated, with similar line width and pitch and outer dimensions up to several micrometers. Combining rings and periodic nano-wire arrays, it is possible to create a wide variety of complex structures and thus, build up a robust "tool box" of component parts to build up larger circuit-like systems.

The presented approach is useful for producing large arrays of periodic nanostructures for research applications in nanophotonics and plasmonics. Concentric rings allow tailoring of the optical resonances by coupling of the resonances in consecutive rings according to plasmon hybridization principle. Resonance tuning from visible to mid-IR wavelength is possible merely by changing the diameters of the rings. We shall present the optical characteristics and possible applications of these nano-patterns in the conference.

9777-51, Session 11

## Novel approaches for high-volume conformal replication of advanced 3D patterns for the manufacturing of complex monolithic micro-optical components

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The application of advanced technologies such as for the manufacturing of specific ?-optical elements is often associated with high costs. As specific examples, diffractive optical elements or microlenses with unique features - such as specified focal lengths or shapes - can be manufactured by advanced technologies, eg. Inkjet-printing (IJP) or two photon polymerization (2PP) [1,2]. Nevertheless, the fabrication throughput based on such approaches may be hampered due to the lack of parallelization.

A possible solution is the combination of nanoimprint lithography (NIL) approaches with IJP or 2PP as it enables the parallelized manufacturing of multiple monolithic components by replication [3]. The additional compatibility of NIL to Roll-to-Roll (R2R) makes it compatible to large scale manufacturing paths [4, 5]. Moreover, replicated monolithic components are expected to show improved optical behavior and higher reliability. In this paper the preparation of complex substrates, with a focus into the IJP of microlens arrays (MLAs) containing lenses with individual characteristics and the following combination with UV-imprint high-throughput replication into commercially available optical polymers is presented. Moreover the characterization of both master and replicated components will be presented and compared to theoretical expectations. Last but not least, the possibility of inversing the complete process and therefore the polarity of the optical components enabling more freedom for integration into functional devices will be discussed.

The control of the microlens profile is possible by confining inkjet-printed

cross-linkable inks [6] onto substrates with pre-patterned platforms as recently described [1]. As depicted in Figure 1, the required masters are produced by photolithography leading to platforms with a nominal height of 7 μm and diameters ranging from 50 μm to 300 μm (Step 1). Subsequently, a transparent working stamp is produced by UV-casting (Step 2). The coating with an anti-sticking layer enables easy de-molding. The following UV-replication leads to substrates made of OrmoComp® or PDMS (Step 3). The IJP step follows the process described in [1] but achieving herein convex MLAs with individual-lens characteristics (Step 4) which are replicated into a working stamp - of OrmoStamp® - with inversed pattern polarity (Step 5). Then, the final UV-replication can be performed leading to convex monolithic MLAs (Step 6). The described process allows high-throughput fabrication of OrmoComp® or PDMS MLAs while preserving their shape and optical characteristics. A typical inkjet-printed MLA and its focal plane are shown in Figure 2. A replicated working stamp is shown in Figure 3 and the final monolithic MLAs in Figure 4 (OrmoComp® MLA example). Optical characterization has been performed and will also be presented.

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# Conference 9778: Metrology, Inspection, and Process Control for Microlithography XXX

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9778-1, Session 1

## Holistic Lithography and Metrology's Importance in Driving Patterning Fidelity *(Keynote Presentation)*

Martin van den Brink, ASML Netherlands B.V. (Netherlands)

No Abstract Available

9778-2, Session 1

## Smart Metrology for Continuing Moore's Law Scaling *(Keynote Presentation)*

Zhiyong Ma, Intel Corp. (United States)

No Abstract Available

9778-3, Session 2

## Scatterometry modeling for gratings with roughness and irregularities

Jörg Bischoff, OSIRES (Germany); Karl Hehl, Optimod (Germany)

Over the last about 20 years scatterometry has evolved into a standard technology of CD-metrology. Its success relies considerably on highly accurate models for electromagnetic diffraction computation from regular grating patterns. The algorithms behind are preferably FEM or modal method based such as RCWA or C-method. With ever shrinking feature sizes most assumptions about ideal regularity and smoothness do not hold anymore. On the other hand, roughness, i.e. particularly line edge roughness (LER) is becoming a major concern with regard to the electrical circuit performance and contributes to undesired thermal losses. Therefore it would be highly desirable to include roughness as an additional parameter in scatterometry to retrieve from measurement.

However, roughness and irregularities are not restricted to one grating period but extent over a great many of it. Therefore, the modeling has to be likewise extended over large areas driving the computation costs heavily. In order to accommodate these statistical effects a supercell approach could be applied for modal methods resulting in a corresponding increase of the required truncation number (modes to be kept during computation). Unfortunately, the computation time scales with the third power of it (and this even doubles for 3D).

In this paper, an alternative approach is presented taking advantage of the still strong similarity between adjacent grating periods. It is based on near field stitching and relies on the assumption that the cross talk between neighboring periods is negligible. The basic idea is to run a separate simulation for each grating period. The concrete profiles are obtained from the regular basic profile superposed by roughness and, if required, irregularities on the individual cells. The roughness function for the supercell is derived from a statistical model such as an auto-correlation function (only 3 parameters are required – correlation lengths, rms roughness and exponential coefficient). Finally, the nearfields from the separate simulations are stitched together and the far field diffraction modes are obtained by a propagation step. Numerically, these operations can be written in a double sum over the modes and the cells for equidistant cells. The numerical cost of this operation is negligible as compared with the modal method efforts. Thus the overall computation time increase scales only linearly with the growth of the simulation area.

Two examples are discussed to show the potential of the approach. The first one is a sinusoidal L/S-grating overlain by roughness. Here the C-method is applied due to its superiority over RCWA for many non-binary gratings 1/ and its suitability. The simulation provides the same diffraction efficiencies for the propagation modes of the regular standard algorithm for vanishing rms roughness while with increasing roughness, the scattering background between the orders is growing and the propagation modes become weaker. As a second example, a L/S-grating with LER is discussed. In this case, a 2D-grating has to be simulated due to LER. In order to reduce computation costs, the similarity between the cells can be exploited by using a perturbation approach 2/.

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9778-4, Session 2

## Modeling ellipsometric measurement of novel 3D structures with RCWA and FEM simulations

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Agreement between rigorous coupled wave approximation (RCWA) and finite element method (FEM) simulations is well accepted for ordinary materials and basic samples. For nanostructured samples and materials with extraordinary properties, the assumption that RCWA and FEM produce equally accurate simulations needs to be tested. In this work, we will compare these two methods as a means of finding areas where one or both fail. This will allow us to tune the fine details of the simulators where there are unforeseen issues or favoring one method over the other in certain situations.

One area where RCWA has struggled in the past is with plasmonically active materials. To begin, the metallic materials used to induce plasmons require much more computational power due to slower convergence to solution. For this work, the most complex samples will be copper cross-gratings (i.e. Cu gratings overlapping and patterned in orthogonal directions) which are particularly interesting due to the presence of both surface plasmons and localized "spoof" plasmons. Surface plasmons have frequently been confirmed as appearing in ellipsometric spectra both experimentally and in RCWA simulations though overall agreement between approaches has been mediocre. The simulations for this work show excellent agreement over the entire spectra for such samples. Localized "spoof" plasmons are formed by nanopatterning thin metal films in a periodic fashion and are dependent on the entire geometry of the sample. These are very rarely studied in the context of ellipsometry even though they have remarkable properties that have potential uses in industry. This work serves as a first look at full confirmation of their properties using FEM to back up previous RCWA simulations.

In theory, some of these samples might converge so slowly that they cannot be modeled properly with RCWA. While relatively slow compared to RCWA, FEM is highly accurate due to the exact eigenvalue solution method used. Once the FEM solution is found, comparison to multiple RCWA simulations can determine if the latter converges and the minimum computation time.

This analysis must be carried out on a case by case basis but is essential to confirm that simulations are accurate and produce agreement with experiment. With ellipsometric measurement as the end goal, analysis will be performed in the Mueller matrix formalism. Starting with simple samples such as thin film stacks and simple gratings and moving on to the plasmonically active samples mentioned before, we will show that there is very good agreement between RCWA and FEM for our tested cases.

9778-5, Session 2

## Improving optical metrology time to solution using signal response metrology

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As transistor density on integrated circuits (ICs) increases exponentially while critical dimensions (CD) of device reduce to sub-nanometer region, the number of critical semiconductor process steps with extremely unforgiving tolerances increase sharply and the associated precision limits of metrology techniques were driven down as well. Such demand forces the industry to pursue innovative solutions to enable superior accurate and quick turnaround metrology solutions continuously. In recent technology nodes, optical CD metrology (OCD) has proved its capability to precisely detect intricate details on the complex structures prevailed in advanced processes and integration schemes, such as side wall angle (SWA), spacer widths, spacer pull-down, epitaxial proximity, footing/undercut, over-fill/ under-fill of 2-dimentional (HKMG) and 3-dimentional profile(FinFETs). However, conventional RCWA-based (rigorous coupled wave analysis) scatterometry has the limitations of long time-to-results and lack of flexibility to adapt to wide process variations. Signal Response Metrology (SRM) is a new metrology technique targeted to alleviate the consumption of engineering and computation resources by eliminating geometric/ dispersion modeling and spectral simulation from the workflow. This is achieved by directly correlating the spectra acquired from a set of wafers to the known process or structure variations encoded in those wafers. In SPIE 2015, we presented the results of SRM application in lithography metrology and control, setting up a new measurement recipe of focus/dose monitoring in hours1. This work will demonstrate our exploration of SRM implementation in 20nm technology and beyond, including focus metrology for scanner control; post etch geometric profile measurement, and actual device profile metrology.

Capability of in-die metrology to direct measure device profile has been one of the everlasting themes in industry, which enables better yield correlation of process control by ruling out the discrepancies between test sites on frame and real product in-die. Conventional imaging metrology (CD-SEM) is used to measure critical dimensions on products, but has limited capability to measure complex structure details and contamination/damage due to the electron beam is a concern that prevents use on some device structures. Optical metrology can provide more profile details and free of device electrical or morphology damage, but conventional RCWA-based solution requires sufficient diffraction based volume of repeating arrays and extensive engineering and computational resources, both are challenging for compact device design and cost-saving need. Implementation of SRM can be a good candidate to solve this problem, it does not require a geometric or dispersion model, it is less sensitive to non-periodicity than RCWA analysis, and does not require substantial computing resources; the measurement set-up of a device-like structure is same as design-rule test site, in terms of hours. Furthermore, an 'apples-to-apples' comparison demonstrates that SRM consistently provides accurate and precise profile readouts while conventional OCD models fail to do so in many cases. SRM therefore is able to provide direct measurement on device, potentially improving correlation of geometric profile to electrical performance on products. Paper will present results from SRM OCD measurement on device/SRAM structures; which are typically too complex to model using conventional RCWA OCD technique.

9778-7, Session 2

## Innovative scatterometry approach for self-aligned quadruple patterning (SAQP) process control

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The 193 nm immersion lithography patterning method reaches its optical resolution limit around 80 nm pitch using a single exposure. Therefore, in order to be able to reach lower nodes using 193 nm lithography, advanced multi patterning concepts have been proposed, such as self-aligned multi patterning or litho-etch-litho-etch. For the 7 nm (N7) technology node self-aligned quadruple patterning (SAQP) is a promising technique for fin patterning in the FEOL and Metal 1 in the BEOL, where pitch requirements to enable proper scaling are below 25nm. Due to subsequent processing and device performance requirements, CD and pitch walking uniformity specifications are challenging for process tools; thus, effective metrology is needed for process development and in-line monitoring and control.

In SAQP, the final performance of the device depends on the final dimensions of the four populations of lines and spaces. Dimension difference of these populations are called pitch walking, which should be minimized to allow 7nm device functionality. Key process steps include Mandrel 1 Lithography, spacer depositions, and various etches (Figure 1). Scatterometry has long been used to measure structural parameters such as shape and profile, but is often challenged by complex geometries with measurement parameters that have a weak optical signal, such as pitch walking for SAQP structures.

This work addresses the use of innovative scatterometry solutions in measuring other key parameters of the SAQP process flow, including photoresist profile after development, Mandrel 1 and Mandrel 2 profiles after etch, spacer conformality, and the final etch profile. This allows the determination of the key contributors to pitch walking and the development of the best process conditions to eliminate pitch walking.

Scatterometry is a model-based non-destructive optical technique where geometrical details of the pattern are extracted by fitting the theoretical response of a geometrical model to the measured signal. Measuring important profile parameters such as sidewall angles and spacer shapes, scatterometry is becoming critical for SAQP process development. In addition, scatterometry allows high sampling over large areas, thus providing fast and low-noise critical dimension uniformity (CDU) information for the whole wafer and batch. In this work, the SAQP process is developed using amorphous Carbon (a-C) and amorphous Silicon (a-Si) as mandrels, and SiO2 spacers (1 and 2) deposited by atomic layer deposition (ALD). In this work we reveal the influence of the resist profile on the mandrel etch. We also show the effect of the Mandrel profile and sidewall angle on the SAQP process flow. The conformality of the ALD-SiO2 spacer is found to be well controlled and therefore is a minimal contributor to the pitch walking. On the other hand, it is shown that the profiles of the a-C and a-Si mandrels can induce significant pitch-walking, since any change in the mandrel is translated in CD variation. . The etch profile and CD can also be affected by variations of the film thicknesses of mandrel materials. Using scatterometry, we investigate the role of thin film thickness non-uniformity for the a-C and a-Si layers in the final pattern pitch walking.

In this work, we use parallel interpretation of multiple scatterometry targets with slightly variable pitches. . Furthermore, information feed-forward from scatterometry or CD-SEM is shown to further enhance the metrology performance, by decorrelation of process parameters. Additionally, during the multiple patterning process minor variations were intentionally introduced to create different sources of pitch walking in a controlled manner.

In conclusion, the main aim of this work is to evaluate innovative scatterometry methods to enhance the CD performance using in-line monitoring and process control after critical steps of the SAQP process flow. We report the capabilities of scatterometry in identifying within wafer and wafer to wafer process variations of the critical dimensions in order to implement improved pitch walk process control.

9778-15, Session 2

## Lensless spectromicroscopy with a tabletop extreme-ultraviolet source

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Introduction

High-harmonic generation (HHG), when implemented in a phase matched geometry, produces bright, spatially coherent beams on a tabletop, spanning the entire VUV, EUV and soft X-ray regions of the spectrum, up to photon energies >1.6 keV [1]. In recent work we demonstrated high quality, high-contrast, full-field 3D imaging by using extreme ultraviolet (EUV) multilayer mirrors to select a single harmonic order [2]. Here we extend our work to employ the multiple wavelengths intrinsic to our high-harmonic source. We simultaneously retrieve images for each individual harmonic without the need for any hardware-based wavelength separation. This work represents the most efficient use of EUV radiation for imaging to date because there is no energy loss from any multilayer mirrors or monochromatizing optics.

**Lensless imaging using Ptychography Information Multiplexing**

Coherent diffractive imaging (CDI) is a lensless, full-field imaging technique that can achieve diffraction-limited resolution. In CDI, a spatially coherent beam illuminates an object, and the intensity of the scattered light is collected on a detector. An iterative algorithm replaces imaging optics by numerically solving for the complex-valued map of the sample that satisfies both the measured data and one or more a-priori sample plane constraints [3]. The resulting image contains quantitative amplitude (material composition) and phase (thickness/height) information. Ptychography CDI is particularly powerful because many diffraction patterns are collected from overlapping fields of view, rather than one diffraction pattern as in traditional CDI [4,5]. This information redundancy provides a powerful constraint leading to high-fidelity, high-contrast images in both reflection and transmission-modes [6,7].

Here we use a modified version of ptychography, known as ptychographical information multiplexing (PIM) [8], to simultaneously extract the complex spatial light field (both amplitude and phase information) of each phase-matched harmonic order. No EUV multilayer mirrors are used to select a single harmonic, instead the phase-matched harmonics, centered around 30 nm, are steered with a pair of gold mirrors and gently focused onto the sample, illuminating a 10 μm2 area, using an Ni-coated ellipsoidal mirror (Fig. a-b). The illuminated sample is raster scanned, area-by-area, and the diffracted light is collected on a EUV sensitive charge coupled detector.

**Spectromicroscopy with Multiple EUV Wavelengths**

Using the PIM algorithm, complex images are reconstructed for each wavelength showing amplitude (Fig. c-e) and phase (Fig. f-h) information. Within the highlighted region in Fig. (c) we compare the reflectivity ratio (Fig i) and phase difference (Fig j) of the star feature (Ti) and the substrate (Si). We compare these reflectivity and phase measurements with both our previous single color imaging results [1] and with theoretical predications that include native oxide layers and surface roughness. The good agreement confirms this technique's ability to characterize the response of the sample at multiple wavelengths simultaneously, thus enabling spectromicroscopy.

This work, in combination with the long penetration depth of EUV with respect to visible microscopy, demonstrates a potential non-destructive tool for characterization of materials with applications in defect inspection and metrology of buried surfaces.

9778-8, Session 3

## Virtual rough samples to test 3D nanometer-scale SEM stereo photogrammetry

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FinFETs, memory cells, and other advanced structures often require non-traditional dimensional measurements, such as heights or angles, that require knowledge of the vertical dimension in addition to the lateral ones. Scanning electron microscope (SEM) stereo photogrammetry, the construction of a 3D model based on images from 2 or more viewpoints, could in principle provide a solution for such measurements. Indeed, commercial suppliers already provide software to process such SEM data. Such reconstructions are sensitive to errors in viewing angles and in pattern recognition. To assess such errors, it is useful to have test problems for which the correct answer is known. To make such a test problem, we first constructed a basic shape: a 50 nm wide, 80 nm high trapezoidal line with 3º (from vertical) wall angles. We separately produce a rough surface with any desired power spectral density, wrap the rough surface around the basic shape, and resolve collisions (surface self-intersections that may arise at inside corners). The result is a virtual line with a rough surface at which all surface coordinates are known. The virtual line was represented in JMONSEL (our SEM image simulator) as the intersection of height maps from 3 viewpoints, one from above and one each from left and right, in order to accurately represent horizontal surfaces and both sidewalls. It produced simulated images of the virtual sample at sample rotations of –20º, –10º, –5º, 0º, 5º, 10º, and 20º. One of these is shown in Fig. 1. These images then become the inputs for stereo photogrammetry software. We will compare their results with the known reference values.

9778-9, Session 3

## Improvements to the analytical linescan model for SEM metrology

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A critical dimension (CD) scanning electron microscope (SEM) converts a measured linescan into a single dimension number. To better understand how the linescan relates to the actual dimensions of the feature being measured, it is important to understand how the systematic response of the SEM measurement tool to wafer structures impacts the shape of the resulting linescan. Rigorous 3D Monte Carlo simulations of SEM linescans can be extremely valuable for this purpose, but they are often too computationally expensive for day-to-day use. Thus, one approach will be to develop a simplified, analytical linescan model (ALM) that will be more computationally appropriate to the task of analyzing linescans. This analytical linescan expression will then be fit to the rigorous Monte Carlo simulations to both validate and calibrate its use.

In this work, JMONSEL simulation [1,2] is used to better understand how various SEM parameters, beam size/shape, and sample profile influence the linescan (Figure 1). In our previous studies [3,4], an analytical linescan model was developed for trapezoidal features of varying height, width, pitch, and sidewall angle. This model was shown to fit JMONSEL simulations extremely well (Figure 2) for silicon and PMMA features on a silicon wafer over a range of dimensions and shapes. In this study, the linescan model will be extended over a wider range of features sizes and sidewall angles, and for different materials including resist on BARC. In addition, corner rounding of the top of the feature and the presence of a foot at the bottom of the feature will be added to simulate real-world complications to the feature shape. The result will be a calibrated linescan model that could prove very useful for better analyzing and interpreting experimental linescans.

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9778-10, Session 3

## Gaining insight into effective metrology height through the use of a compact CDSEM model for lithography simulation

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Computer simulation of lithographic performance, including resist CD, film thickness, sidewall angle and profile has been extensively studied during the past three decades. Lithography simulation has been widely adopted as an enabling technology for high-volume chip manufacturing.

However, measurement artifacts arising from CD-SEM metrology are typically ignored in simulation, due to the difficulty of accurately modeling the effect of the CD-SEM at acceptable computational speed.

In this paper, we demonstrated how simulations can be improved by including a fast, compact CD-SEM model. For example, the variation in effective resist metrology height along contour lines extracted from a simulated CD-SEM image is characterized for a range of structures through focus and dose. We also demonstrated how SEM settings affect the shape of extracted SEM contour and metrology height at contour edge. The key process parameters (layout and resist profile shape etc.) contributing to metrology height variation are studied more closely. Finally, we make recommendations on how to use the compact CD-SEM model to improve the accuracy of simulations for a variety of common applications.

9778-11, Session 3

## Electric fields in SEM simulations

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In semiconductor industry, the decreasing feature sizes which are accompanied by increasing complexity such as 3D topography pose new challenges for scanning electron microscopy (SEM) inspection and metrology [1]. Dedicated SEM simulation environments can be used to enhance resolution and extract 3D information (e.g. sidewall-angle, structure depth, buried defects) by optimizing the experiment parameters such as beam energy, developing optimized system configurations and sophisticated signal processing. To achieve the accuracy needed, SEM simulators have to be extended by a fast and accurate 3D electric field engine.

In this work, electric field distribution and charging effect in SEM were studied. A multigrid method based solver has been implemented and integrated into virtualSEM, a Monte-Carlo based SEM simulator currently under development by GenISys GmbH. The focus is to develop physics based models with easily accessible parameter, predictive power for a wide range and the potential of simulating realistic scenarios in minutes.

One major challenge for such simulation environment is the efficient modelling of feature dimensions on a nanometer scale for a cm-scale tool setup (e.g. position of electron source, chamber wall or, detectors). The simulation has to be accurate enough for the nm-range and fast for the full set-up. For that purpose, two different field solvers were implemented in this work, each using non-uniform grids. A reference solver was built based on the Red Black Gauss-Seidel method and, a fast solver was implemented by utilizing the multigrid method [2]. The reference solver was tested for several basic test cases and proven its reliability. As the name suggest, it acts as reference and verification method for the much faster but less proven fast solver. By the means of multigrid method, a gain in computational speed of roughly a factor of 40 compared to the reference solver where the difference in accuracy between the results is in order of? 10?^(-6) V.

The tracking of electrons in the electric fields generated by various components of an SEM and charging of the sample are part of the model and have been taken into consideration in the integration process (demonstrated in Fig. 1).

We have evaluated the accuracy of the simulation results using SEM measurements of basic 2D and more complex 3D structures (demonstrated in Fig. 2 and Fig. 3). The results of the simulations were generally in good agreement with experimental data; all major feature of the actual SEM image could also be observed in according simulations.

Thus, with this work SEM simulation has been improved to be usable in terms of speed and accuracy, including the dynamic modelling of charging. More data, especially regarding the comparison of both simulation and experiment and on realistic industrial application, will be presented in the conference.

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9778-12, Session 3

## GPU accelerated Monte-Carlo simulation of SEM images for metrology

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In nano lithography, scanning electron microscopy (SEM) image simulators can be of great benefit in the study of dimensional metrology.

An example is the interpretation of the true size, shape and roughness characteristics of three dimensional resist features in top-down SEM images.

In the case of rough features, the number of elements required to define the sample, hence the computation time, increases dramatically.

This problem is tackled, for example, with voxel based geometries, height maps and tetrahedra with shared faces. Although these solutions seem to work well, computation time can still be a problem, especially when statistics in the metrology play a role.

A typical example is the determination of line edge roughness (LER) using the power spectral density (PSD).

Another example is when one or more input parameters are varied over a range of values.

Our quest in reducing the computation time of SEM image simulation further has led us to investigate the use of graphics processing units (GPUs) for metrology.

We consider the physical scattering models from a previous study, which is based on the work of Kieft et al.

Instead of solid elements, we only consider the hull, i.e. the triangular faces that constitute the boundary of the material interface.

This means that every triangle of the hull now has a different material on each side.

In addition, detectors are also triangular shaped elements, which can be defined inside material as well.

The simulation now proceeds as follows.

For any given electron, there are four possible discrete events: the electron may (1) hit a detector, (2) cross a material interface, (3) scatter elastically and (4) scatter inelastically.

A particle in vacuum is terminated if there is no material interface and no detector in the direction of the particle.

A particle is also terminated if the kinetic energy is lower than the work function of the material.

For parallel processing, we consider all primary electrons in the SEM image at once. In every iteration, the running and terminated particles form separate groups.

The group of active particles is split into subgroups, where each subgroup is identified by a particular discrete event and thus follow the same execution path.

Each subgroup is now calculated separately in parallel on the GPU with an enormous gain in calculation speed.

The whole procedure is repeated until all particles are terminated.

At the SPIE conference, we will present the details of the simulation code and demonstrate with metrology applications the power and performance of SEM image simulation using the GPU.

9778-6, Session 4

## Spectroscopic imaging of buried layers in 2+1D via tabletop ptychography with high-harmonic EUV illumination

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We use extreme ultraviolet coherent microscopy to obtain high-resolution images of buried interfaces, with chemical specificity, in 2+1 dimensions. We perform reflection mode [1,2], ptychographic [3-5], coherent diffractive imaging [6-8] with EUV light produced by high harmonic generation at 29 nm [9-11]. Our damascene samples (SEMATECH) consist of copper structures inlaid in TEOS-deposited SiO2, polished nearly flat via chemical mechanical polishing. We obtain images of both an uncoated damascene as well as one buried below a 100 nm thick layer of evaporated aluminum. The aluminum is opaque to visible light and thick enough that neither optical microscopy, SEM, nor AFM can reveal the buried interface. EUV microscopy is capable of imaging the buried structures in situations where other techniques cannot due to the high transmissivity of 29 nm light through aluminum [12].

In our EUV images, the presence of amplitude contrast alone confirms that we are observing the buried damascene (which yields contrast between the Cu and the SiO2), as opposed to features on the aluminum layer (which would produce no amplitude contrast since that layer is a single material). We modify the ePIE algorithm [4] with position correction [13, 14] to use the measured input EUV beam power, forcing the algorithm to produce absolute reflectivity values for the sample by normalizing the probe to this power at every iteration. Low measured reflectivities in our Al coated damascene image (which could not be explained by Fresnel effects) allowed us to determine that diffusion had occurred at the boundary between the Al layer and the damascene, causing the drop in reflectivity. We confirmed the presence of this interstitial diffusion layer via Auger electron spectroscopy. Given this diffusion, we find good agreement in our measured absolute reflectivities with theory for both a damascene coated with Al and an uncoated damascene.

In order to filter out parasitic harmonic light, we further refine our images using a spectral multiplexing algorithm [15]. Using this multiplexing algorithm, we obtain higher fidelity 29.1 nm images of the coated and uncoated damascenes than with ePIE alone.

In addition to amplitude images, ptychography also yields phase images that contain height information. We mask our phase images and assign correct Fresnel phases to the Cu and SiO2 regions based on information from our measured reflectivities, as well as the Auger spectroscopy and ellipsometry. This allows us to produce height maps of the coated and uncoated damascenes. The uncoated damascene height map agrees well with an AFM measurement. We cannot verify the height map of the coated damascene since the AFM is only capable of imaging the top Al layer, whereas our height map provides the topography of the buried layer.

EUV microscopy is an incredibly promising method for imaging buried structures. EUV light is an optimal probe for buried layer microscopy because many materials are transmissive at EUV wavelengths, allowing imaging of structures below these materials. This technique will likely be useful for applications in the semiconductor industry for overlay metrology.

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9778-13, Session 4

## HVM metrology challenges toward the 5nm node *(Invited Paper)*

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As the industry continues to progress down the ITRS [1], not only do device dimensions shrink, but architectures increase in 3D complexity, including new incorporated materials. To enable efficient process development, yield ramp and eventual successful production, demonstrated metrology capability must be realized at the forefront; such new critical in-line metrology will be needed to not only keep pace with these changes, but to provide process developers with the information necessary to accurately and efficiently evaluate the structural results of their work and to aid them in understanding their paths to profitable yields.

FinFETs and tri-gates are the current typical CMOS devices, yet still pose some metrology challenges.[2][3] These challenges will continue to increase as fins evolve into nanowires. 3D NAND memories will continue to increase in aspect ratios, presenting yet more metrology difficulties.[4] The possibility of DSA lithography raises potential metrology problems, depending on whether the metrology is to be done before or after removal of the sacrificial component [5]. Complex periodicities resulting from multi-patterning add more complications [6][7], and the small dimensions and volumes of the resulting features cause low signal-to-noise ratios. And not only are the patterns shrinking, but films become thinner [8] and smaller defects become yield detractors.[9]

This presentation will examine at a high level the future for in-line high volume manufacturing (HVM) metrology for the semiconductor industry. First, we will take a broad view of the needs of patterned defect, critical dimensional (CD/3D) and films metrology, and present the extensive list of applications for which metrology solutions are needed. Commonalities and differences among the various applications will be shown. We will then report on the gating technical limits of the most important of these metrology solutions to address the metrology challenges of future nodes, highlighting key metrology technology gaps requiring industry attention and investment.

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9778-14, Session 4

## Multiple beam ptychography

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Ptychography is a robust coherent diffraction imaging (CDI) technique that replaces an imaging lens with computational reconstruction algorithms. Ptychography relies on information redundancy resulting from overlapping scan areas to simultaneously solve for the amplitude and phase of both the probe and the diffracting sample. Typically, for large field of view ptychographic imaging, many scan positions are needed. This makes the prospect of using ptychography for large area imaging or metrology challenging due to the large number of scan positions.

Here we present a new technique to efficiently increase the field of view of ptychography through use of multiple illuminating probes, to speed up ptychographic CDI without adversely impacting the spatial resolution. Past work has shown that multiple incoherent modes in a probe beam can be reconstructed using multi-mode ptychography algorithms [1]. In our work, by separating these modes spatially, we can simultaneously image multiple areas on the sample. We implement this technique by using two probe beams of different wavelengths and using two probe beams of orthogonal polarizations. The former allows for spatially resolved spectroscopy from a single ptychography scan, while the latter allows for spatially resolved polarization spectroscopy from a single scan.

This technique can be applied for any mutually incoherent probes - however, it would be most beneficial if it could be applied to multiple probes of the same mode. We demonstrate that through digital filtering of the diffraction data, the case of multiple coherent probes can be reduced to the case of multiple incoherent probe beams. This allows us to use an array of beams of the same wavelength and polarization state to image multiple areas of a sample simultaneously.

Further, under certain experimental conditions, we are also able to make use of the interference between coherent probes to isolate the contribution to the total diffraction pattern from each beam. Thus we can collect a single diffraction pattern from multiple probes and analytically extract one diffraction pattern for each individual probe. This allows us to use single mode ptychography algorithms, which exhibit faster convergences than multi-mode ptychography algorithms. Additionally, if the multiple probes are similar enough, then all of the extracted single-beam diffraction patterns can be used together as if they were diffraction patterns taken from a large single-beam ptychography scan.

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9778-16, Session 4

## Measurement of asymmetric side wall angles by coherent scanning Fourier scatterometry

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With the ever increasing demand for higher packaging density, feature sizes on modern semiconductor chips have now reached the 14 nm node. Against this background, a quantitative inspection of even the smallest grating asymmetries, such as side wall angles (SWAs), gains in importance. Although existing techniques offer sufficient precision for major grating parameters like line width and height, they still struggle with the measurement of SWAs.

We propose a measurement technique which is based on the evaluation of higher diffraction orders. It enables the precise determination of the SWA with respect to absolute value and sign. Additionally, in case of a grating line with an asymmetric cross-section, we are able to differentiate between the SWAs on the left- and right-hand side of the line.

Through rigorous simulations of silicon line gratings, we verify the validity of our method for SWAs considerably smaller than 1°. The grating period is on the order of a few micrometers. Each grating line consists of a fine sub-grating with 40 nm period, 20 nm critical dimension (CD) and identical SWAs on each of the sub-grating lines.

Our approach is based on coherent high-NA Fourier scatterometry. A tightly focused spot from a spatially coherent, monochromatic light source is laterally scanned over the object. The reflected light is collected by the same microscope objective. Subsequently, the positive diffraction orders are coherently superposed with their negative counterparts (and vice versa) by a 180°-shearing element. An image of the pupil plane of the microscope objective is recorded for each scan position, thus allowing for an angle-resolved analysis.

The resulting set of pupil images is evaluated point-wise. For each pupil point, we obtain a sinusoidal intensity signal as a function of the scan position over the grating. This signal shows a distinct local extremum in the close vicinity of the center of the compound grating line (consisting of the sub-grating with several fine lines). For sub-grating lines with symmetric cross-sections (rectangular or trapezoidal), the position of the local extremum exactly coincides with the center of the compound grating line for all points in the pupil image. In contrast, asymmetric cross-sections cause a certain shift of the extremum. The shift varies as a function of the pupil coordinate and enables a detailed analysis of the grating shape.

An interferometric extension of the setup by a reference arm in Linnik configuration and a structured aperture stop greatly enlarges the flexibility with respect to the accessible evaluation region in the pupil image and the range of measurable samples.

9778-17, Session 4

## Non-contact thermal distance sensing and thermal microscopy as a high-resolution inspection and metrology solution

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At a beating pace the semiconductor industry finds itself facing increasingly more difficult challenges at every technology node; not only in manufacturing, but also in inspection and metrology. For the 14 nm node and beyond high resolution imaging and high throughput seem to be mutually exclusive. Scanning probe technologies such as atomic force microscopy offer the potential of imaging at the atomic level by scanning a microscopic probe over the sample and recording the response. The high resolution, however, comes at a cost of an inherent low speed and the need for (intermittent) contact between the probe and the sample. Especially for damage prone high aspect ratio features such as FinFETs full non-contact methods are preferred. With this in mind a generation of new imaging techniques needs to find its way to industrial application: the meta-instrument. These instruments allow the application of non-contact near-field imaging techniques such as solid immersion lenses (SILs), hyperlenses and superoscillatory lenses (SOLs); technologies that all offer the potential of high resolution, high throughput imaging. These technologies, however, share one major challenge: the need for exceptional position control at extreme proximity to the sample. A hyperlens or SIL can only provide the predicted performance when the lens is positioned at a distance from the sample that is measured in tens of nanometers. Superoscillatory lenses can be used at a distance of micrometers, but at a position accuracy of nanometers. These requirements raise two important questions: 1) how to determine the distance between lens and sample in a nanoinspection/nanolithography system and 2) how to keep the lens at the required distance, without the risk of contact? In this paper, we address the first question and propose using near-field thermal radiation as a mechanism for an integrated distance sensing system (patent pending). Ongoing theoretical and experimental research shows that for materials that support phonons, radiative heat transfer surpasses the black-body limit at distances below the characteristic thermal wavelength (approx. 10 μm at room temperature) and is strongly distance dependent. A calorimeter can thus be used as a sensitive distance sensor. Such a heat flux sensor can be made using a bilayer cantilever of materials with distinct thermal expansion rates. A changing heat flux causes the temperature of the cantilever to change and the cantilever to deflect consequently. The deflection is measured using an optical beam deflection system. In such system a laser beam is incident on the cantilever and reflected to a position sensitive detector (PSD). The optical power of the laser is then tuned to counteract the deflection using a control loop. With this system sub-nanowatt heat fluxes are measured that are equivalent to sub-nanometer changes in distance. Using a large scale experimental setup the principle is demonstrated and the system performance is determined for distance measurement and non-contact microscopy. Future work will be focused on miniaturization for integration in a meta-instrument.

9778-18, Session 4

## Reliable characterization of materials and nanostructured systems 50nm using coherent EUV beams

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Advances in nanofabrication now make it possible to grow films with precise thicknesses from the single-atomic-layer up, as well as to pattern nanostructures with dimensions <10nm. At these length scales, traditional macroscopic models cannot accurately describe the thermal-mechanical properties of even simple material systems, due to their small dimension and the increasing influence of interfaces. Therefore precise characterization of materials in nanostructured devices is necessary for understanding the unique physics of such small-scale systems: Is isotropy a valid assumption for the elastic properties of <<50nm thin films? How do the phonon spectra of materials allow us to tailor thermal transport in nanostructured systems?

To overcome these challenges, we implement a non-destructive photoacoustic metrology technique that uses coherent extreme ultraviolet (EUV) light from tabletop high harmonic generation (HHG) in place of more conventional optical-wavelength laser probes. The short wavelength of EUV beams is sensitive to picometer-scale displacements of the surface; and the femtosecond duration of HHG pulses is fast enough to capture sub-picosecond thermal and acoustic dynamics of nanostructured systems. Previously we have proven the success of our technique by fully characterizing 100nm thin films, and uncovering the collectively-diffusive regime of nanoscale thermal transport, where close-spaced nanowires cool faster than widely-spaced ones.

Samples consist of periodic gratings of metallic nanowires deposited on dielectric or semiconductor substrates and thin films. A femtosecond 800nm laser pump is focused on the samples and the resulting impulsive heating of the nanostructures causes thermal expansion and also launches acoustic waves throughout the system: surface acoustic waves (SAWs) in

the substrate/film with wavelength set by the nano-grating period, and longitudinal waves (LAWs) within the nanostructures and the substrate/film. By diffracting our EUV probe beam from the deforming surface onto a CCD camera as a function of delay time between pump and probe pulses, we simultaneously extract the heat dissipation rate and wave velocities, which are exquisitely sensitive to the thermo-mechanical properties of the sample. Since the penetration of the SAWs is limited to a fraction of their wavelength, the periodicity of the nanostructures is tuned to probe different depths.

The fabrication of nano-gratings with periods as small as 45nm allow us to go beyond our previous capabilities and to simultaneously extract the Young's modulus and Poisson's ratio of low-k dielectric films as thin as 5nm. We characterize a series of films of same materials but varying thicknesses bellow 50nm to test deviations from isotropy and bulk properties. We also confirm a previously unobserved upward trend in the Poisson's ratio with decreasing Young's modulus, below a critical value of the films' material bond coordination. In addition, by studying the heat dissipation away from the periodic nano-gratings with same linewidth but different periodicities, we confirm and quantify the effects of the recently identified collectively-diffusive regime in sapphire, silicon and fused-silica. These measurements allow for a better extraction of the phonon-MFP spectra of these materials, and provide a unique opportunity to understand the fundamental physics of this regime through direct comparison with numerical modeling using the time-dependent Boltzmann transport equation.

9778-19, Session 5

## High-throughput CDSAXS with compact x-ray sources

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Next generation nanodevices such as sub-10 nm finFETs will require new dimensional metrology methods for high throughput, non-destructive process control. Currently used optical methods are running into fundamental limits for determining the dimensions of ever smaller and more complex nanostructures. Cross-sectional TEM measurements are too slow and result in the loss of an entire wafer for each measurement set. We will discuss the development of CDSAXS as a potential next generation, high throughput dimensional metrology measurement. We will show the current status of CDSAXS with commercially available compact X-ray sources and discuss the future improvements possible with next generation X-ray sources under development. We have characterized the absolute scattering intensity of a series of industrial relevant finFET samples and will discuss the strong effect of the materials on the scattering intensity. CDSAXS analysis requires inverse data modeling similar to, but much less computationally demanding than optical scatterometry. We will conclude with a study of the effect of the signal to noise of the raw data on the final shape profile uncertainty extracted through data modeling.

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9778-20, Session 5

## Characterization of cross-sectional profile of resist L/S and hole pattern using CD-SAXS

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The scale of semiconductor device is continuously shrinking, and the critical dimension is now expected to reach down close to ten-nanometers. The performance of such a fine device can be easily affected by a slight variation in the shape of the resist pattern. It is, therefore, important to carry out quality control over the cross-sectional profile of resists. Critical dimension scanning electron microscope (CD-SEM) is used for CD metrology on mass production lines. However, the CD-SEM cannot measure cross-sectional profile, especially when there is an inverse tapered shape. In addition, it is well known that the electron beam can make a serious damage on the resist pattern. This arouses a doubt whether cross-sectional electron microscope methods, either scanning (SEM) or transmission (TEM), measure correct shapes. Small angle x-ray scattering (SAXS) is one of the candidates for measuring cross-sectional profile non-destructively. X-ray metrology can detect a slight shape variation, because the wavelength is well shorter than the critical length of the pattern structure. We have developed a new SAXS-based metrology tool. The system utilizes grazing incidence geometry and the geometry is suitable for measuring surface structure high sensitivity in a shorter collecting time.

Firstly, we have applied our new CD-SAXS to two kinds of resist L/S pattern wafers. The both have a 130 nm pitch size, but they were intentionally fabricated with different material composition and exposure condition to obtain different cross-sectional profile. Monochromatic x-rays with wavelength of 0.15418 nm (Cu K? line) were irradiated to the sample surface with shallow glancing angle and the sample was rotated around the vertical axis at the irradiated point during the measurement. Diffraction peaks corresponding to the pitch size were observed in the lateral direction. The average pitch and the line width can be determined by the diffraction angle and the intensity ratio of these peaks, respectively. Characteristic fringe patterns, which strongly depend on the order of diffraction h, were observed in the vertical direction. Depth, sidewall shape, and corner rounding shape can be determined by the periodicity and the phase of the fringe patterns. These shape parameters were optimized by a non-linear least square method using measured and simulated diffraction patterns. Obtained cross-sectional profiles showed an inverse tapered shape in the two resists and a difference in the top corner rounding shape between the two.

Secondary, we have applied the CD-SAXS to two kinds of resist hole-patterned wafers. The holes are arranged in a 2D square lattice-like form in the lateral plane with a 90 nm pitch. Diffraction data were collected in two directions [1 0] and [1 -1] to analyze 3D shape. The 3D cross-sectional profile was determined in a similar way of the 2D cross-sectional profile analysis. The obtained cross-sectional profiles had the following characteristics. One was the rather vertical cylindrical shape and the other was the heavily undercut shape.

The cross-sectional profiles obtained by the CD-SAXS were compared with cross-sectional SEM observations. The results were consistent between the two metrologies.

9778-21, Session 5

## Hybrid enabled x-ray thin film metrology

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Advanced transistor technologies are continuing to integrate thinner and multi-stack films of novel material compositions. Process control of ultra-thin films in the 1-2nm range require a Total Measurement Uncertainty (TMU – relative accuracy metric) and Fleet Matching Performance (FMP – tool matching metric) on the order of 0.1 Angstrom for entire metrology fleet. Optical metrology techniques (such as Spectral Ellipsometry – currently the throughput-intensive workhorse of thin film measurements) are reaching their performance limits. Ability to accurately identify 0.1 Angstrom

change in film thickness is fundamentally limited by cross-talk with other parameters of the film stack (thickness of other layers, variable materials composition). X-ray Photoelectron Spectroscopy (XPS) has emerged as one of the key in-line methods for accurate independent measurement of thickness and composition of ultra-thin films. However, XPS-based measurements have lower throughput than their optical-based counterparts, limiting high sampling plan deployment of XPS.

Two trends are emerging in thin film metrology: "measure what matters" and "more eyes on the wafer". In the context of thin film metrology, "what matters" is the film thickness as deposited on the actual device, instead of a simplistic un-patterned test sites. Micro-loading and topography effects often create differences between thickness on un-patterned test sites and patterned structures and even between various patterned structures (due to differences in their pitch, logic, shape or location). Metrology of thin films on patterned structures is targeted to augment and ultimately replace traditional thin films measurements. "More eyes on the wafer" is designed to enable continuous yield improvement program that require higher sampling plans for more complete metrology coverage of dies at the edge of the wafer. High metrology sampling is imperative to understand and resolve the sources of process variability whether its lot to lot, wafer to wafer, across wafer or even across-die.

Neither X-ray nor optical technique provide ideal solution for thin films: X-ray is accurate, but throughput limited, whereas optical techniques are fast, but lack the inherent accuracy (both absolute & relative) and sensitivity required to meet tight metrology budget. Here, we extend the Hybrid Metrology concept to thin films by combining the strengths of both toolsets – x-ray and optical.

To substantiate transition to accurate metrology for films-on-pattern, we use an application example where 6-wafer DOE is processed for the deposition of HK/IL film stack. In another application example 5-wafer DOE is processed for deposition of a thin SiON film. The lower-throughput XPS tool can accurately extract independently thickness and N-dose. Optical measurements cannot independently measure thickness & N-dose (optical properties) for such thin films. To extend XPS measurements over the whole wafer with improved throughput we hybridize sparse XPS sampling plan into a dense optical sampling plan.

The paper will cover several key 1X and beyond applications (ultra-thin, multi-stack) to demonstrate hybrid extension of X-ray metrology performance with assistance from optical toolset to solve two critical use-cases for advanced nodes: transition to films-on-pattern and throughput extension of X-ray performance.

9778-22, Session 5

## XPS-XRF hybrid metrology enabling FDSOI process

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Planar fully-depleted silicon on insulator (FDSOI) technology potentially offers comparable transistor performance as FinFETs with less process complexity and lower unit costs. FDSOI transistors consist of an ultra-thin layer of silicon on top of a buried oxide (BOX) and provide limited short channel effects, good subthreshold slope, minimum junction capacitance and low leakage. A thin BOX layer can provide back bias capability, enabling better gate control and low power circuit operations. FDSOI pFET devices are based on a thin layer of silicon germanium (SiGe) on top of the BOX with the N-doped interfacial layer (IL), high-k (HfO2) layer and the metal gate stacks being successively built on top of the SiGe. SiGe introduces uniaxial strain in the channel and replaces Si as the channel material to boost carrier mobility and Vt tunability. Current metrology techniques to monitor SiGe thickness and %Ge, inline, are dominated by high resolution X-ray diffraction (HRXRD) and optical metrology. However, thin cSiGe layers (<100Å) fall below the detection limit of inline HRXRD for symmetric (004) scans and are also challenging for reciprocal space maps (RSMs) methodology. Optical metrology techniques on the other hand cannot measure the thickness and composition directly and also suffers from complex modeling and correlation issues between and measure the high-k, IL, N-dose as well as the SiGe thickness and %Ge in one single measurement.

Hybrid metrology (HM), which combines more than one equipment type or technique, is being implemented in the industry in recent times to enable or improve measurement of critical parameters, where a single measurement type is insufficient or is challenged by fundamental limitations of the tool or the technique. The methodology and benefits of HM have been demonstrated in earlier works. In one of the recent findings, integrated X-ray photoelectron spectroscopy (XPS) and low energy X-ray Fluorescence (LE-XRF) were used to simultaneously measure SiGe thickness and %Ge on bulk and SOI substrates. In addition, unique and independent XPS signals from the IL, high-k and nitrogen allows simultaneous detection of IL thickness, high-k thickness and N-dose.

Moreover, subsequent metal layers built on top of high-k can also be measured using XPS feed forward (FF) technique. The fundamental limitation of XPS in measuring stacks greater than 100Å in total thickness is overcome by FF. The real-time feed forward of data from previous (pre) layers enables direct, in-film atomic composition and thickness measurement capability for subsequent layers.

In this paper, we will discuss the approaches, challenges, and results associated with the first-in-industry implementation of XPS-XRF hybrid metrology for simultaneous detection of high-k thickness, IL thickness, N-dose, cSiGe thickness and %Ge, all in one signal measurement on a FDSOI substrate in a manufacturing fab. From a design of experiment (DOE) data set, we will present the sensitivity and correlation of one or more of these inline parameters to electrical data. In addition, static precision with 30 repeated measurements will also be included.

9778-23, Session 6

## Impact of pulse-to-pulse stability on CD resolution for next generation inspection tools using VUV or EUV laser produced plasma light sources

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The temporal pulse-to-pulse stability of the light source directly affects the performance of the inspection tool and thus constitutes a primary requirement of a VUV or an EUV light source in the context of metrology and inspection applications. Pulse-to-pulse energy stability of the light source is directly linked to the slight temporal instability of the droplet stream in a laser produced plasma (LPP) light source, which results in variations in the time between subsequent laser pulses and hence in the laser pulse energy transferred to the droplet. This in turn directly impacts the performance characteristics of the inspection tool via two major mechanisms. First, the laser pulse energy influences the EUV pulse energy as the laser pulse energy is directly linked to the characteristics of the generated plasma in terms of electron density and temperature and therefore in terms of the plasma radiative emission properties including the total amount of photons per pulse. The amount of photons and energy per pulse is highly relevant for the throughput capabilities of an inspection tool as the detector of the imaging system needs a certain amount of photons to get above a critical threshold. Second, the laser pulse energy and spot size also determine the temperature and expansion velocity of the plasma and thus the effective plasma source size. The source size is directly related to the brightness of the EUV or VUV source, which in turn affects the resolution capabilities of the inspection tool. Thus, as the plasma size positively affects emitted energy but negatively affects source brightness, which affect the throughput and resolution capabilities respectively, there exists a certain trade-off. Achieving a high temporal droplet stability and thus a high temporal pulse stability allows better control of this trade-off.

In the first part of this work, the impact of the laser pulse energy on the EUV and VUV energy as well as the brightness is determined. Based on this, an analytical model, which includes the variations in the laser energy

resulting from the temporal drop-to-drop instabilities, is developed that quantifies how temporal droplet stability relates to variations in EUV pulse energy as well as in source brightness. The final part then analyses how the performance characteristics of the inspection tool, such as CD resolution capabilities as well as throughput capabilities are affected by variations in EUV and VUV pulse energy as well as in source brightness as a result of droplet stream instabilities.

9778-24, Session 6

## Study of design-based e-beam defect inspection for hotspot detection and process window characterization on 10nm logic device

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When design rule is mitigating from 14nm to 10nm and 7nm, confined process window continues to be one of the main challenges limiting device yield. Masks, scanners, and etching processes have to meet very tight specifications in order to keep defect, CD, as well as overlay within the margins of the process window. Conventionally, integration engineer relies on a scheme of using optical defect inspection followed by extremely intensive SEM based defect review to trace process window boundary and center. However, challenging defect detection sensitivity by optical inspection and prolonged defect review process fall behind the needs of identifying precise process window in timely manner for new tapeouts. Due to superior resolution, E-beam technology naturally fits for review and/or detection of subtle pattern infidelities, aka defects. The capability of integrating design information (GDS file) with defect detection, dimension measurement of critical structure, and defect classification provides added values for engineers to identify yield limited systematic defects and to provide feedback to design.

In this work, we study a design-based e-beam defect inspection technology for wafer level process window characterization and intra-field defect variability on 10nm logic devices. The experimental wafers are etched substrates with a complex two-dimensional metal layer fabricated through three litho-etch cycles by using 193nm immersion lithography with negative tone resist. Multiple wafers with modulation dies have been exposed. These wafers have comprehensive split conditions on focus and dose settings together with normal dies on best focus and dose settings been printed and etched. The experimental platform is compromised of a 2nm resolution large field of view (LFOV) e-beam defect inspection system and a supercomputer running sophisticated algorithms for alignment of SEM image to design files and execution of defect detection and classification. The whole system could run at either real-time mode or offline mode.

A metrology chip consisting majority of pattern types was scanned by using LFOV image for every die on a wafer, while the die-to-database (D2DB) defect detection scheme is employed. The basic concept of D2DB is to leverage design information to achieve highest detection sensitivity on systematic defects, a sensitivity that cannot be achieved by traditional die-to-die (D2D) defect detection mode. Moreover, design information could be used to significantly enhance defect binning capability, which is critical to generate correct process window by screening out non-modulation defects while identifying systematic defects through repeater analysis and pattern grouping. Figure 1 shows an example of systematic defects detected by e-beam D2DB inspection. The final GDS pattern consists of tri-colored polygons indicating patterns fabricated by distinct litho-etch cycles. The GDS pattern is overlapped with SEM image. Furthermore, an intra-field defect footprint can be identified through hot spot inspection at systematic defect locations. The intra-field results could be used to further refine process window and to reveal variabilities caused by masks and scanners. Figure 2 shows intra-field defect performance.

In summary, confined process window in 10nm technology node and beyond places increasing demands for higher defect detection sensitivity to identify precise process window as well as yield limited systematic defects. Superior resolution from e-beam inspection together with capability of handling GDS information provides sufficient defect detection sensitivities and defect binning capabilities.

9778-25, Session 6

## Electromagnetic field modeling for defect detection in 7nm node patterned wafers using the vector boundary element method

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By the year of 2017 the critical dimension in patterned wafers will shrink down to 7nm, which brings great challenges to the current optics-based techniques for “killer defects” inspection. The difficulty in the defect inspection mainly arises from the ever-decreasing signal to noise ratio with respect to the shrinkage of defect size. Hence, to design an optimized instrument and a corresponding signal processing algorithm for reducing noise pollution, it is of great importance to simulate the scattered far-field of the patterned wafer with and without defects to find the most sensitive and strongest optical response with respect to the defects. Though traditional numerical methods such as the finite element method and finite difference time domain can meet the requirements of scattered field modeling, they usually result in the extreme consumption of memory and computational time. This motivates the development of a more effective and resource-saving technique for scattered field modeling.

In the present article, we focus on the electromagnetic far-field modeling of three 7nm node Intentional Defect Arrays (IDA) with “Bx”, “By” and “J” defects using the vector boundary element method (VBEM), as presented in Fig. 1. The space under calculation is divided into four homogeneous regions S1 to S4 that are separated by three boundaries Γ1 to Γ3, as shown in the left side of Fig. 2. A plane wave with the wave vector k = [sinθcosφ, sinθsinθ, cosφ] having unit amplitude is incident on the dummy boundary ?1. For a point rip in region Si, its electric field Ei(rip) and magnetic field Hi(rip) can be respectively calculated by [1, 2]

In above equations , , , and are the incident electric field, the incident magnetic field, the tangential electric field on surface Γ, the tangential magnetic field on surface Γ and the scalar Green’s function, respectively. Here Γ is the surface of region Si. δi is 1 if the source is in region Si, otherwise δi is 0. is a step function that is 1 in space and 0.5 on the continuous boundary. The surface Γ of region Si is firstly discretized into a series of serendipity vector boundary elements, as presented in Fig. 2. Then, by using the Galerkin’s method, we can obtain a set of linear equations from Eq. (1) and Eq. (2), which are

In the above equations , , and are the coefficient matrices with whose elements are surface integrals with respect to the scalar Green’s function, and are the coefficient vectors with whose elements are surface integrals with respect to the electric and magnetic components of incident light, respectively, while and are unknown vectors consisting of the line integrals of the and along the edges of all the serendipity vector boundary elements on the surface Γ of region Si. Next, by applying the boundary conditions and the LU-decomposition, the unknown vectors and can be obtained. Finally, the scattered field at an arbitrary point above Γ1 can be calculated according to Eq. (1) and Eq. (2).

For simplicity, in this abstract we only present the scattered field intensity distribution simulation of a grating with a single line using the VBEM, as shown in Fig. 3. The grating is illuminated by a normal incidence plane wave with TE polarization and unit amplitude, under which the VBEM can be simplified into the scalar BEM. However, for the more complex nanostructures as shown in Fig. 1, the solution process following from Eq. (1) to Eq. (4) should be performed rigorously, which will be presented in the conference proceedings article.

9778-26, Session 6

## Detection of metallic buried void by effective density contrast mode

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For sub-2Xnm technology nodes, metallic buried voids in metal contacts have become critical yield and reliability issue for high volume semiconductor device manufacturing. Especially as the scaling continues, void-free metal filling becomes more challenging for advanced technology development, which poses great need for effective in-line detection methodology. In this paper we demonstrate comprehensive study of a special buried metallic void detection mode by backscatter electron (BSE) signals based on effective density contrast (EDC), especially for the case of partial conduction while the conventional voltage contrast (VC) mode has no detection due to minimum detectable resistance difference requirement. Successful application of EDC mode in buried metallic void detection by in-line electron beam inspection (EBI) is presented on various metal contact chemical mechanical planarization (CMP) layers, together with Monte Carlo simulations and other characterization methodology which show consistent correlation with experimental observations. Thus an extrapolation based on simulation result is illustrated to predict the detection capability of EDC mode in buried metallic void detection for the popular metal contact material systems including tungsten and copper. Despite of the detection limitation as well potential damage by the charged particle exposure, EDC mode is demonstrated as a very effective detection methodology for buried metallic void in advanced technology development.

9778-27, Session 6

## Critical via hole detection in electron-beam inspection using multi-layer design analysis

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The via-hole layer integrity is vital for chip functionality and becomes critical in cases where only a single or double count of via holes make the connection. An improper etch or improper metal fill of these critical via holes may result in an open connection between the two interconnecting process layers. Electron Beam Inspection (EBI) in Voltage Contrast (VC) mode is performed for the discovery of defects to detect any such electrical connection issues for process qualification. Owing to the large cycle time for each of the steps involved in E-Beam inspection – e.g., recipe setup time, inspection run time and post-inspection defect analysis and classification -- it is always a challenge to improve the throughput. In this paper we report a methodology whereby we perform multi-layer design analysis to determine the location of critical via-holes, and then optimize the ROIs (Regions of Interest where inspections are done) so as to reduce the total EBI run time. By using this methodology, we can reduce inspection run time up to 5x in a 28nm product. To filter out nuisance defects from the inspection results, we perform defect-to-design overlay and sample locations for cross-section analysis, thus increasing the chances of locating critical via failures.

An open single-path via-hole (rendering floating metal) appears as a Bright Voltage Contrast (BVC) defect in a negative mode electron beam inspection while the normal metal connection to N+ active is dark and the gate connection is relatively gray. In the case of double-path via-holes where only one of the vias is blocked, the defect does not appear completely bright, but has a less bright gray level. Calibration is needed in the inspection tool's Auto Defect Classification (ADC) system to separate such (non-critical) gray defects from the real (or critical) Bright VC defects. The Figure 1 provides an overview of the methodology that was developed. More real examples of the defects found and their causal mechanisms will be discussed in this paper.

The benefit of this approach lies in the determination of all critical locations that are prone to failure, as compared to the thousands of the other robust locations. This helps to streamline the efforts in optimizing the inspection strategy for detection of connection failures. Multi-layer design with overlay analysis helps to identify such weak locations. The advanced tools for layout pattern grouping, which can adapt to multi-layer design data, further help to improve the turnaround time of finding the critical locations in the die before consolidating them into a set of optimized inspection care areas or Regions of Interest.

9778-28, Session 7

## Focus control enhancement and focus response analysis methodology on product

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With decreasing CDOF for 20/14nm technology and beyond, focus errors are becoming increasingly critical for on-product performance. Current on product focus control techniques in high volume manufacturing are limited; It is difficult to define measurable focus error and optimize focus response on product with existing methods due to lack of credible focus measurement methodologies. Next to developments in imaging and focus control capability of scanners and general tool stability maintenance, on-product focus control improvements are also required to meet on-product imaging specifications. In this paper, we discuss focus monitoring, wafer (edge) fingerprint correction and on-product focus budget analysis through diffraction based focus measurement (DBF) methodology. Several examples will be presented showing better focus response and control on product wafers. Also, a method will be discussed for a focus interlock automation system on product for a high volume manufacturing (HVM) environment via integrated metrology. Finally, several topics will be highlighted which are essential for a HVM friendly solution (target design/optimization and recipe creation cycle time, target placement limitations and metrology matching)

9778-29, Session 7

## Analysis of wafer heating in 14nm DUV layers

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As the process nodes keep shrinking, achieving overlay requirements of critical layers is becoming increasingly challenging. By using state of the art scanners, linear, higher order wafer and field corrections, foundries have been able to achieve these stringent requirements. Many foundries have also started to use corrections per exposure where overlay error of every field is modeled independently and corrected. To improve process window and image contrast, NTD process is being used at many layers at the 1x nodes. One of the drawbacks of NTD masks is that they have a higher transmission value, which leads to higher energy being propagated through the lens and

on to the wafer. Apart from effects like lens heating, this energy will also cause wafer heating which can manifest as an overlay fingerprint difference in scan up and scan down directions in the DUV process [1].

In this paper we characterize the effects of wafer heating by measuring the scan up and scan down overlay delta obtained by exposing reticles of differing transmission values and different dose; then we study the resulting effect of wafer heating on overlay on consecutive sets of layers. The second layer aligns to the first and has different dose and transmission values. Due to this difference, the scan up and scan down overlay will be different among the two layers which will cause an overlay error. Figure 1 compares the delta in the scan up and scan down signatures of various 14nm production layers as measured to the first layer. In the figure, L1 is the first layer. This shows that the difference in overlay signature has a linear dependency with the dose delta. Once we understand the effects of wafer heating we then propose overlay modeling techniques to compensate for this effect.

9778-30, Session 7

## Line-edge roughness accuracy analysis during pattern transfer in self-aligned quadruple patterning process

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As the Critical Dimension (CD) continues to shrink, the accuracy of Line Edge Roughness (LER) and Line Width Roughness (LWR) measurements assumes a role that becomes more and more predominant. However, even though it is well know that the roughness accuracy depends on many measurement parameters (pixel size, frame averaging, and field of view, among the others), only the impact of the measurement box length is included in the ITRS roadmap guidelines. Alternative approaches have been proposed to minimize the impact of the measurement parameters, as in the case of bias-free algorithms, used to avoid the dependence on image noise [1]. However, even in these cases, choosing the most trustworthy setting is not a trivial decision. The goal of this paper is to investigate the accuracy provided by existing roughness algorithms and measurement parameters by comparing the results with reference metrology techniques, such as Transmission Electron Microscopy (TEM) and Three-Dimensional Atomic Force Microscopy (3D AFM).

To this aim, LER and LWR are analyzed during pattern transfer in a self-aligned quadruple patterning (SQDP) process. This patterning process leads to a final pitch of 22.5nn, relevant for N7/N5 technologies. Measurements performed by CD SEM (Critical Dimension Scanning Electron Microscope) with different settings in terms of averaging, field of view, and pixel size are compared with reference metrology performed by planar TEM and 3D AFM for each patterning process step in order to investigate the optimal condition for an in-line LWR characterization. An example of the comparison of CD SEM, AFM and TEM images is shown in Figure 1. Pattern wiggling is also quantitatively analyzed during LER/LWR transfer in the SAQP process.

[1] Atsuko Yamaguchi, Robert Steffen, Hiroki Kawada and Takashi Iizumi, "Bias-Free Measurement of LER/LWR with Low Damage by CD-SEM", Proc. of SPIE Vol. 6152 61522D-1 (2006)

9778-31, Session 7

## Design-based metrology: Beyond CD/EPE metrics to evaluate printability performance

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For the latest technology nodes, metrology has become more challenging and above all a necessity. Starting from standard CD (Critical Dimension) measurement approaches, the industry quantifies the printability performance on wafer based on SEM (Scanning Electron Microscope) pictures and algorithms that determine distances (CD) at specific locations, referred as measurement boxes. This quantification, also called verification, allows assessing the quality of a resist model that was calibrated by an OPC (Optical Proximity Correction) engineer, or the quality of a certain process compared to others. However, these specific locations at which distances are determined, within the FOV (Field-of-View) of the SEM picture, are limited in scope. In fact, we don't even use the full information given by the SEM picture. In other words, we are not using a lot of the available information that could matter for a more statistically complete evaluation of the printability performance at key locations. Worse, the measured features might not even be considered as limiting features (Hot-Spots) that compromise the functionality of the chip. Also, setting up the locations of these measurement boxes is not straightforward, and can be prone to errors. Since these results are of primary importance, a proper quantitative verification on wafer is needed to account for unavoidable errors in the scanner (dose and focus for example).

To evaluate the process window on wafer more accurately, we take advantage of design based metrology and extract experimental contours from the CD-SEM measurements. Then we implement an area metric to quantify the area coverage of the experimental contours with respect to the intended ones, using a defined "sectorization" for the logic structures. This sectorization aims to differentiate specific areas on the logic structures being analyzed, such as corners, line-ends, short and long lines. This way, a complete evaluation of the information contained in each CD-SEM picture is performed, without having to throw away any piece of information.

This solution doesn't look at the area coverage of an entire feature, but uses a sectorization to differentiate specific feature areas such as corners, line-ends, short and long lines, and thus look at those area coverages. An assessment of resist model/OPC quality/process quality at sub nm-level accuracy is rendered possible.

This solution could be implemented in the standard metrology flow. Evaluations of the printability performance could be improved more accurately, based on the outputs from this methodology.

9778-32, Session 7

## A new approach to process control using instability index

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The merits of a robust Statistical Process Control (SPC) methodology have long been established. In response to the numerous SPC rule combinations, processes, and the high cost of containment, the Instability Index (ISTAB) is presented as a tool for managing these complexities. ISTAB focuses limited resources on key issues and provides a window into the stability of the manufacturing operation.

ISTAB takes advantage of the statistical nature of processes by comparing the observed average run length to the expected average run length (ARL), resulting in a gap value called the ISTAB index. The ISTAB index has three characteristic behaviors that are indicative of statistical defects in an SPC instance.

Case 1: The observed average run length is excessively long relative to expectation. ISTAB > 0 is indicating the possibility that the limits are too wide.

Case 2: The observed average run length is consistent with expectation. ISTAB near zero is indicating that the process is stable.

Case 3: The observed average run length is inordinately short relative to expectation. ISTAB < 0 is indicating that the limits are too tight or the process is unstable or both.

The probability distribution of run length is the basis for establishing

an ARL. We demonstrate that the geometric distribution is a good approximation to run length across a wide variety of rule sets. Excessively long run lengths are associated with one kind of defect in an SPC instance; inordinately short run lengths are associated with another. A sampling distribution is introduced as a way to quantify excessively long and inordinately short observed run lengths. This paper provides detailed guidance for action limits on these run lengths.

ISTAB as a statistical method of review facilitates automated instability detection. This paper proposes a management system based on ISTAB as an enhancement to more traditional SPC approaches.

9778-33, Session 8

## Enabling quantitative optical imaging for in-die-capable critical dimension targets *(Invited Paper)*

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Optical methods are proficient for measuring nanoscale features over large areas for effective process control. However, as critical dimensions (CDs) continue to decrease in size, a critical need has emerged for optical targets and methodologies capable of characterizing CD variability within the active area of the die. While scatterometry has long been utilized for in-line process control, we explore the potential for optical imaging for in-die measurement capabilities. Use of a high-magnification imaging platform would allow for multiple relatively small targets to be spatially isolated from one another within the imaging field-of-view. The key challenge for quantitative optical imaging however is characterizing the effects of the physical optics upon simulation-to-experiment comparisons, as aberrations and other tool errors can affect the measured scattered intensities.

We have recently demonstrated the quantitative measurement of 30-line arrays approximately 2 um x 6 um in area using a high-magnification imaging platform with feature mid-widths as small as 18.2 nm ± 1.1 nm (3sigma), i.e. 1/25th the measurement wavelength of 450 nm.[1] The proper treatment of systematic errors inherent to optical imaging has significantly improved the reliability of these quantitative measurements. We have previously identified one required element of this analysis, the normalization of scattering components in the Fourier domain.[2] To summarize, each spatial frequency scattered by the target scatters at a different angle, and illumination and collection tool path functions are required to scale the simulated Fourier components in accordance with the observed tool imperfections, hence leading to a more thorough comparison between simulated and measured values.

In this work we expound upon rigorous treatments of significant, but difficult to measure tool errors. Assuming a zero mean bias, these errors are directly related to the parametric uncertainties through the covariance matrix, and special caution has to be taken in order to account for correlations within these tool errors. Furthermore, we discuss the sensitivity of the microscope configuration to non-zero mean biases that may arise, e.g. from line edge roughness, provide quantitative measures of the impact such biases have on the parametric values and uncertainties through simulations, and review available options for accounting for such biases. For example, strategies such as tailoring the angle of incidence and Fourier filtering in the collection plane may minimize the role of bias upon the parametric modeling. Prospects for the extensibility of these techniques to feature sizes as small as 7 nm are discussed, including applicability of these techniques when imaging at 193 nm wavelength.

[1] J. Qin, et al., "Deep-subwavelength Nanometric Image Reconstruction using Fourier Domain Optical Normalization," accepted, Light: Science & Applications (2015).

[2] J. Qin, et al., "Fourier domain optical tool normalization for quantitative parametric image reconstruction," Appl. Opt. 52, 6512-6522 (2013).

9778-34, Session 8

## Optical metrology solutions for 10nm films process control challenges

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Operating transistors with reliable performance within 1V threshold voltage as required by newer mobile processors requires excellent electrostatic control of the transistor. Tight control of thickness and composition of high-k gate dielectrics and metal layers are critical to control the threshold voltage and drive current, especially with the move to 3D topography in FinFET structures. The thickness control limits have approached 0.4-0.6Å at the 10nm node, and the process impact of the subsequent metal gate deposition steps can alter the thickness and composition of underlying films through diffusion and introduction of crystalline defects. Therefore, it has become necessary to measure and control each layer in the gate stack before and after dielectric and metal gate deposition sequences.

Measuring the thickness of individual layers in complex stacks such as these has traditionally been done by optical and x-ray films metrology on planar film stack pads present in the scribe lane of product wafers. A ratio of metrology precision to process tolerance (P/T) of 10% is generally considered acceptable for in-line process control. Given the tight process tolerance, meeting a P/T of 10% is extremely challenging for a multi-layer film stack with very thin films. This is due to the required precision of <0.06Å combined with the very small scattering volume of the thin films that requires very high signal/noise for sufficient measurement sensitivity. We show that using a laser-driven light source for spectroscopic ellipsometers has been a viable solution for the signal/noise issue, and has recently been adopted in 14nm production for in-line films metrology. An additional problem is the correlation of the film properties measured on these proxy planar pads to those of the device film stack degrades as the control requirements shrink at 10nm and the substrate geometries have become 3D instead of planar. Therefore, there is a need to move toward measuring films properties on device/product or failing which, to measure films on proxy targets that more closely resemble the 3D geometry of the device. Since any given process step can alter the properties of the layer that was previously deposited, each layer of a complex stack has to be measured individually, which introduces measurement and modeling correlation issues. One potential solution is to add more signal pathways (or channels) to reduce modeling parameter correlations. In this paper, we present the benefit of using spectroscopic ellipsometry with multiple angles of incidence to accurately determine the thickness of individual layers in a high-k/interfacial layer stack. We will also show the benefit of using a different signal channel, an advanced laser-based ellipsometer, for ultra-precise measurement of the interfacial layer oxides. Finally, we will present the capabilities of measuring film thickness at sub-Angstrom precision on 2D fin grating based on a new algorithmic approach that minimizes the time to results and systematic errors introduced by conventional optical CD modeling.

9778-35, Session 8

## Advanced in-line optical metrology of sub-10nm structures for gate all around devices

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Gate-all-around (GAA) nanowire (NW) devices have long been acknowledged as the ultimate device from an electrostatic scaling point of view. The GAA architecture offers improved short channel effect (SCE) immunity compared to single and double gate planar, FinFET and trigate structures. One attractive proposal for making GAA devices involves the use of a multilayer fin-like structure consisting of layers of Si and SiGe with 30% Ge fraction. This structure allows for selective removal of the SiGe in the gate trench after the dummy gate removal. This removal process allows for the gate stack to wrap around the remaining Si channel material forming a GAA device structure. Integration with a fin-like structure consisting of multiple materials poses an interesting material challenge. CD control of both materials in the stack is required to produce a stable integration scheme. Unfortunately, accurate CD determination of both films is challenging using CD SEM. While oblique angle SEM may be capable of obtaining sidewall information, subtle geometry may not be adequately detected. Optical Scatterometry, also called optical critical dimension (OCD) is a potential fast, accurate and non-destructive in-line metrology technique capable of measuring these subtle CD and structural variations across the wafer. However, material optimization, spectral sensitivity and high correlation between parameters pose significant challenges for accurate and precise OCD model development.

We setup and qualify OCD as enabler for process development of nanowire devices, and extend the capabilities to learn new material and process aspects specific to this novel device integration. Building on an SOI substrate, Ge condensation is the first step, enabler to higher Ge concentration than normally achievable through direct epi growth (reference). Using OCD as thin film metrology we extract both composition and thickness of the condensed SiGe film results confirmed through XRD & XPS. Second step is sequential growth of a Si/SiGe stack, where we use the same toolset to independently extract thickness of all 6 layers, and Ge% for the two epi-grown SiGe layers. We find that the Silicon bulk optical properties do not provide a good spectral match to the measurements, and instead we extract and use optimized material properties for improved accuracy. This result is consistent with quantum confinement (band structure distortion), and is perhaps the first experimental confirmation of this effect in nanowire-based devices by a high throughput optical measurement technique. Also, the other significant metrology difference in the fin module is the fin RIE (etch), where different etch rates of Si and SiGe can alter the fin profile by preferentially removing the SiGe material (which can have an impact at later stages of device process). We setup and qualify fin profile measurements and extract a single parameter for the SiGe undercut.

Also, paper discusses about methodologies and optimization approaches required for successful implementation of in-line OCD metrology. Major challenges for model development are complex material optimization and limited spectral sensitivity to some of the critical structural features. Careful analysis of optical signature, multi-stack, multi-target spectral optimizations are several key strategies that provide means to address these challenges. Optical model solutions developed at several key process steps in both single and multi-stack NW device integration flow are also presented. Further, we compare the results with relevant reference metrology for validation.

9778-36, Session 8

## Optimizing noise for defect analysis with through-focus scanning optical microscopy

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High-throughput and economical three-dimensional (3-D) shape analysis or process monitoring of nanoscale objects is extremely desirable and at the same time challenging in this age of nanotechnology where usage of three-dimensional components is increasing. It is further beneficial if this can be achieved using widely available, low cost, conventional optical microscopes. It is much more desirable if the same method can be extended to micro-scale targets. The through-focus scanning optical microscopy (TSOM) appears to satisfy these requirements. In addition, the TSOM also shows promise for defect analysis. It is important to minimize the total system noise of TSOM method for defect analysis application since the noise level determines the smallest defect that can be detected. However, a systematic noise-analysis study for TSOM has been lacking. Here we study various parameters that influence noise and their optimization to achieve peak performance of the TSOM method for defect analysis.

The following method was chosen to identify the total noise. Generate a differential TSOM image (DTI) using two independently constructed TSOM images from the same target under the exact same experimental conditions. If done correctly, this process cancels out the signal from the target. The resultant DTI contains purely total system noise. It was observed that this noise is usually random in nature. In the current study optical intensity range (OIR, defined as the absolute difference between the maximum and the minimum optical intensity in a given TSOM image or DTI multiplied by 100) of the DTI was used as a metric to define the noise signal strength. In this presentation we study and optimize seven parameters that affect the noise. The noise OIR in the current study varied from a minimum of 0.26 to a maximum of 3.5.

As an example here we present the effect of focus step size on the noise level. A 300 nm focus step has a noise OIR of 0.77 (Fig. 1(a)). The noise OIR increases to 0.94 for 1000 nm focus step (Fig. 1(b)) showing an increasing trend. A summary of the noise OIR is plotted in Fig. 1(c). It shows tapering of noise above 1000 nm step under the experimental conditions used. However, we have to bear in mind that this noise itself depends on the other parameters selected. This noise analysis makes sense when we look at the signal strength of a 7 nm type A defect shown in Fig. 1(d), which has an OIR of 0.9. Its signal strength is slightly under the noise OIR of 0.94 for 1000 nm focus step, and hence may not be detectable. However, the same defect has better chance of detectability at 300 nm focus step, which has a lower noise OIR of 0.77.

This demonstrates the importance of noise reduction by optimizing parameters to push the limits of defect detection.

9778-37, Session 8

## Monitoring of ion implantation in microelectronics production environment using multi-channel reflectometry

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In modern semiconductor manufacturing, control of implanted structures is a challenge. Two typical issues are control of the implant dose and determination of the thicknesses and critical dimensions (CD) of implanted and annealed structures. Accurate in line control of implant dose for high volume production is often limited by current Fab metrology. As the global trend of miniaturization dictates a continuous decrease of the energy and dose of the implants, the measurement capabilities should match stricter requirements. Typical methods used for these measurements, such as LEXES (Low energy Electron induced X-ray Emission Spectrometry), SIMS (secondary ion mass spectroscopy), or FPP (four point probe/sheet resistance measurements), are sensitive to implant ion dose but limited by throughput and/or the necessity of wafer removal from the production line.1 Spectroscopic ellipsometry (SE) and spectroscopic reflectometry (SR), in addition to determination of thickness and CD (scatterometry), are good candidates for the monitoring of ion implantation in line in a production Fab. Both methods are fast and non-destructive. Typical fab

systems operate in UV and VIS light range. This allows one to determine thickness and CD, but the spectral range will significantly limit sensitivity to implant energy and dose. Typically, the infrared (IR) part of the spectrum is needed to distinguish between silicon wafers implanted with different doses or energies. However, utilization of far IR ellipsometers/reflectometers requires a relatively long measurement time and more complex optical system, and therefore is not yet introduced to mass production. It is still possible to investigate the depth of implantation with the UV/VIS range using ellipsometry directly after implantation.1, This method uses the fact that implanted crystalline substrates are amorphized, and amorphous media have very different optical properties from crystalline media. In traditional models, ion-beam-induced amorphization occurs as a phase transition induced by an adequate number of point defects created by the individual ions. The situation is different for thermally annealed implanted materials such as polycrystalline Si (pc-Si). Implanted and amorphized portions of pc-Si after thermally induced epitaxial regrowth change back into their initial structure - polycrystalline (though the crystal grain size might differ). Optical properties of modified and unmodified pcSi layers become again very optically similar and, therefore, it is difficult to optically distinguish the materials in order to measure their individual thicknesses when they are stacked together. However, implantation in production flows typically occur through thin (30 Å) layer of SiO2 (as shown in Figure 1). After ion bombardment and thermal annealing an interface layer consisting of a mixture of SiO2 and pc-Si is formed. We could model optically this interface using classical BEMA (Bruggeman Effective Media Approximation) by mixing pc-Si and SiO2 optical properties. The optical properties of this interface differ significantly from pc-Si due to two phenomena: an intermix with SiO2, and change of the grain size of pc-Si after regrowth. We used reflectometry with normal and oblique channels and s- and p-polarizations for each channel to measure implanted structures. We found that the thickness of the modeled interface scales with implant dose and, therefore, can be used for implant monitoring in production, as shown in Figure 2. This could be due to two combined phenomena: the implant dose might increase the SiO2 diffusion into the pc-Si (transient and thermally enhanced diffusion) and/or change the grain size of pc-Si after thermal regrowth. Furthermore, the majority of the literature studies use SE due to its expected higher sensitivity to interfaces/surface conditions, and not SR. However, the combination of different channels and polarizations increases SR sensitivity for implanted and annealed interfaces. Accurate determination of interfaces altered by implant allows us to resolve 2D applications. In this work, we “inject” separately determined damaged interface thicknesses as well as other parameters into 2D scatterometry models of implanted transistors. With this method we achieve the same TMU (Total Measurement Uncertainty) level as for measurements of a non-implanted transistor, as shown in Figure 4. Furthermore, good correlation between in-line electrical parameters and metal-gate BCD scatterometry measurements was achieved. This approach can be extended to other technology nodes as well.

9778-90, Session 8

## Advanced in-line metrology strategy for self-aligned quadruple patterning

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Self-Aligned Quadruple Patterning (SAQP) is a promising technique extending the 193-nm lithography to manufacture structures that are 20nm half pitch or smaller. This process adopts multiple sidewall spacer image transfers to split a rather relaxed design into a quarter of its original pitch. Due to the number of multiple process steps required for the pitch splitting in SAQP, the process error propagates through each deposition and etch, and accumulates at the final step into structure variations, such as pitch walk and poor critical dimension uniformity (CDU). They can further affect the downstream processes and lower the yield. The impact of this error propagation becomes significant for advanced technology nodes when the process specifications of device design CD requirements are at nanometer scale. Therefore, semiconductor manufacturing demands for strict in-line process control to ensure a high process yield and improved performance, which must rely on precise measurements to enable corrective actions and quick decision making for process development. This work aims to provide a comprehensive metrology solution for SAQP.

During SAQP process development, the challenges in conventional in-line metrology techniques start to surface. For instance, critical-dimension scanning electron microscopy (CDSEM) is commonly the first choice for CD and pitch variation control. However, it is found that the high aspect ratio at mandrel level processes and the trench variations after etch prevent the tool from extract the true bottom edges of the structure in order to report the position shift. On the other hand, while the complex shape and variations can be captured with scatterometry, or optical CD (OCD), the asymmetric features, such as pitch walk, show low sensitivity with strong correlations in scatterometry. X-ray diffraction (XRD) is known to provide useful direct measurements of the pitch walk in crystalline arrays, yet the data analysis is influenced by the incoming geometry and must be used carefully.

A successful implementation of SAQP process control for yield improvement requires the metrology issues to be addressed. By optimizing the measurement parameters and beam configurations, CDSEM measurements distinguish each of the spaces corresponding to the upstream mandrel processes and report their CDs separately to feed back to the process team for the next development cycle. We also utilize the unique capability in scatterometry to measure the structure details in-line and implement a “predictive” process control, which shows a good correlation between the “predictive” measurement and the cross-sections from our design of experiments (DOE). The ability to measure the pitch walk in scatterometry were also demonstrated. This work also explored the frontier of in-line XRD capability by enabling an automatic RSM fitting on tool to output pitch walk values. The hybrid metrology approach for more accurate pitch walk measurement is also discussed. With these advances in metrology development, we are able to demonstrate the impacts of in-line monitoring in the SAQP process, to shorten the patterning development learning cycle to improve the yielding.

9778-38, Session 9

## Process monitor of 3D-device features by using FIB and CD-SEM

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Due to recent progress in manufacturing 3D-devices, metrology of 3D-features has been a hot topic. At the same time, in-die or in-pad variability is issue in manufacturing yield [1] because variability of individual 3D-features within scatterometry spot-size is not easy to measure. Now the most practical method is TEM that can measures individually dense feature’s cross-sections contained in several-micrometer-large lamella sample. TEM that has been used for reference metrology is recently used for near-line process monitor for manufacturing.

However, the in-die or the in-pad variability control is limited by the speed of FIB lamella-sampling and TEM measuring procedures. To achieve the higher manufacturing yield, process and/or manufacturing engineers want to measure the more frequently the more number of 3D-features.

In this article, we demonstrate on-wafer-3D-profile measurement using CD-SEM and FIB. We used CD-SEM for sub-nanometer precision to measure feature’s cut-off image exposed on a FIB-cut slope. For instance, we firstly cut an a-few-micrometer-wide and 45-degree-descending slope on a wafer surface. The slope is cut in die or pad where line features have been processed, as illustrated in Fig. 1. Because the descending direction

is parallel to the line features, cut-off image of the lines is exposed on the slope surface.

Then, we transferred the wafer to CD-SEM to measure the cut-off image from top-down view. According to the descending angle set at 45 degrees, the CD-SEM-measured-length between the top and the bottom of the cut-off line is equal to the actual height of the line; as illustrated in Fig. 2. Also the top-CD, the bottom-CD, and the side-wall angle can be directly measured for the individual features by CD-SEM with sub-nanometer precision.

The in-die or the in-pad variability can be rather easily monitored in manufacturing because cutting a simple slope by FIB and measuring it by CD-SEM is easier and faster, than preparing a lamella sample by FIB and measuring it by TEM. Obtaining enough number of cut-off image data, we demonstrate statistical analysis of neighboring device-feature's CD that is measured in a-few-ten-micrometer diameter.

Reference:

[1] Tactical and strategic metrology perspectives for advanced integrated circuit development and manufacturing, Eric Solecky, Alok Vaid, GLOBALFOUNDRIES Inc, [9424-1] (Keynote Presentation), SPIE Conference of Advanced Lithography, 2015.

9778-39, Session 9

## Free surface BCP self-assembly process characterization with 3D CDSEM

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A simple and common practice to evaluate Self Assembly performances of block copolymers (BCP), is on a free surface wafer. With no guiding pattern the block copolymers designed to form line space pattern for example, spontaneously rearranges to form a random finger print type of a pattern. The nature of the rearrangement is dictated by the physical properties of the BCP moieties and the self-assembly process parameters.

To investigate and optimize the thermal budget of a DSA processes, we used a statistical image segmentation method, it separates the pattern in the SEM image, into different postulations, materials and border.

The attributes of each population for the different processes, reflected interesting results. When pattern rearrangement became poor at the boundaries of the thermal budget process window, segment distribution of the different populations changed. A significant increase of the border area indicated PCP dislocations due to variations in the DSA process.

Identifying pattern edges we could statistically measure critical dimensions and uniformity of arbitrary 2D pattern. Combined with 3D SEM we could explore morphology variations as a function of DSA process variations.

In this paper we propose a metrology method to measure arbitrary BCP pattern on a bare wafer. We present experimental results using this method for thermal budget optimization of a DSA process.

9778-40, Session 9

## Advanced CD-SEM metrology for qualification of DSA patterns using coordinated line epitaxy (COOL) process

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Directed self-assembly (DSA) applying chemical epitaxy is one of the promising lithographic solutions for next generation semiconductor device manufacturing. Especially, directed self-assembly lithography using coordinated line epitaxy (COOL) process is obviously one of candidates which is the first generation of DSA applying PS-b-PMMA block copolymer (BCP) for sub-15nm dense line patterning [1]. Generally speaking, density multiplication technologies, including DSA and SAQP, not only enhance the pitch resolutions, but also mitigate CD errors to the values much smaller than those of the originally exposed guiding patterns. On the other hand, local line placement error after density multiplication often results in a worse value, with distinctive trends depending on the process conditions. To address this issue, we have introduced a novel measurement method using CD-SEM, which enables to evaluate the individual DSA lines, distinguishing their location against the position of the guiding patterns [2]. The method was successfully applied to estimate the placement offsets of the lines on, as well as those interpolating, the guiding stripes, which were fabricated by COOL process with density multiplication as presented in Figure 1.

In this study, we introduce an enhanced measurement technology of DSA line patterns with distinguishing their locations in order to evaluate nature of the edge placement and roughness corresponding to the individual line pattern locations. In figure2, the examples of power spectrum density (PSD) analysis are shown. Correlations among edge roughness of each line and each space (correlation factors) are evaluated and discussed. The measurement criteria, including measurement condition and uncertainty, are discussed to realize the optimized measurement for qualification control of the COOL process. As a result, we found the followings. (1) Line placement error and line placement roughness of DSA were slightly different each other depending on their relative position to the chemical guide patterns. (2) In middle frequency area of PSD analysis graphs, it was observed that shapes were sensitively changed by process conditions of chemical stripe guide size and anneals temperature. (3) PSD analysis of correlation factors was able to define characteristics corresponding to physical property of BCP materials.

9778-41, Session 9

## Identification of multilayer structure using secondary electron yield curves: Effects of native oxide film, material density, and surface contamination

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The formation of native oxide film or contamination, and the film density have a great impact on the accuracy of CD-metrology and sensitivity of inspection using electron beam technology. This is due to the change of the secondary electron yield (SEY) and also due to the charging effect. In most cases, these two effects cannot be isolated, because the most of the oxide films are insulator. However, native oxide film of Ruthenium, RuO2, is known as a conductive film. Therefore, the impact of native oxide film on SEY can be investigated without affecting the charging effect. The SEY of Ru metal with 1nm thick native oxide (RuO2) is larger than that of RuO2 bulk and that of Ru metal without native oxide. This is because that the elastically backscattered electrons at the interface between Ru metal and native oxide generate secondary electrons (SE) in the native oxide. Moreover, the energy barrier for electrons to escape from the sample surface of oxide film is lower than that of a metal. Therefore, the SEs generated in the Ru metal are easily to escape from the surface of native oxide film. As a result, these SEs enhance the SEY of the Ru metal with native oxide. The simulation shows the dependence of the SEY on the thickness of the native oxide film and the density of Ru metal. The density of the material is known to be changed depending on the deposition procedure. In general, the density of sputter-deposited film is several percent smaller than that of epitaxially grown crystal. In this study, all the layers were deposited by magnetron sputtering method at room temperature. And the simulated SEY curves are in good agreement with experimental data when the densities of the materials are approximately 8 % lower than the crystalline ones. This result indicates that the thickness of native oxide can be estimated if the density is known, or the density can be estimated if the thickness of the native oxide is known. In the case of Boron Carbide (B4C), the native oxide film is not formed. Therefore, the impact of surface contamination on SEY was investigated without affecting the charging effect and also the native oxide film. A contamination

film of oxygenated hydrocarbon with the thickness of < 1nm had an effect to enhance the SEY. This work was supported by NEDO

9778-42, Session 10

## Simultaneous AFM nano-machining and imaging for photomask repair

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Optical lithography is the main patterning technology for semiconductor industries. Thus, production, inspection and repair of high precision photomasks remain one of the challenges in high volume manufacturing. Thanks to its nanoscale resolution, the atomic force microscopy (AFM) has already been suggested as one of the instrument for inspection and repair of 64 and 32nm node photomasks. However, there are still some challenges regarding the throughput of AFM based mask repair. These techniques usually require multiple times scanning the sample with different modes and different cantilevers which altogether result in time consumption of about 2 hours per each defect.

In this paper, we present a simultaneous imaging and nanomachining method which does not require multiple cantilevers or scanning steps and can increase the throughput of the defect repair process.

The AFM based nanomachining is done by increasing the tip-sample interaction force on defect area, followed by cleaning of the residuals. The current technologies use the tapping mode AFM for imaging and inspection because of its stability and lower damage, and use contact mode AFM for nanomachining because it is easy to apply high tip-sample forces in a controlled manner.

However, using only the tapping mode AFM, it is also possible to increase the tip-sample forces in a controlled manner and without interrupting the image. This enables simultaneous imaging and nanomachining.

The tip-sample forces are mainly attributed to the amplitude and stiffness of the cantilever which are impossible to change without interrupting the image. However, the excitation frequency is actually by far the most important imaging parameter that affects the tip-sample forces. Provided that the free-air and set-point amplitudes are kept constant, one can increase and decrease the forces by changing the excitation frequency without interrupting the image.

In order to verify this theory, we have designed and fabricated a force sensing setup which measures the time resolved tip-sample forces in tapping mode AFM.

Both the theoretical and experimental results suggest that above-resonance excitation increases the forces and enables nanomachining.

In order to demonstrate the proof of concept for nanomachining, we have created a rectangle on the surface of glass using a single crystal diamond tip by increasing the force, and immediately imaged with the same tip with low forces.

9778-43, Session 10

## Nanoscale chemical and topology imaging of block copolymers assemblies with photo-induced force microscopy

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Supramolecular self-assembly provides a powerful and low-cost way to achieve nanoscale materials synthesis and pattern formation for applications in advanced lithography, nanophotonics, photovoltaics, therapeutics, and related areas. The chemical and structural morphology of these materials ranges in size from 5 – 100 nm, which is not easily interrogated in real space via existing instruments based on optics (due to insufficient spatial resolution arising from the diffraction limit) or electrons (due to limited contrast between materials and the possibility of sample damage).

Infrared Photo-induced Force Microscopy (IR PiFM) is based on an atomic force microscopy (AFM) platform that is coupled to a widely tunable mid-IR laser. PiFM measures the dipole induced at or near the surface of a sample by an excitation light source by detecting the dipole-dipole force that exists between the induced dipole in the sample and the mirror image dipole in the metallic AFM tip. This interaction is strongly affected by the optical absorption spectrum of the sample, thereby providing a significant spectral contrast mechanism which can be used to differentiate between chemical species. Due to its AFM heritage, PiFM acquires both the topography and spectral images concurrently and naturally provides information on the relationship between local chemistry and topology. Due to the steep dipole-dipole force dependence on the tip-sample gap distance, PiFM spectral images surpass topographical spatial resolution, showcasing sub 10 nm spatial resolution despite the increase tip radius of metal coated tips.

PiFM studies on various self-assembled block copolymer systems will be presented. The results consist of PiFM spectral images associated with several absorption bands of different blocks along with broad spectra associated with nano-spots on sample surfaces. Images of fingerprint patterns, parallel lamellae and vias (prepared via directed self-assembly) for poly (styrene-b-methyl methacrylate) showed a clear spectral contrast between the two blocks of each material system. By enabling imaging at the nm-scale with chemical specificity, PiFM provides a powerful new analytical method for deepening our understanding of nanomaterials and facilitating technological applications of such materials.

9778-44, Session 10

## Device level 3D characterization using peakforce AFM

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Traditional metrology solutions face a range of challenges at the 1X node such as three dimensional (3D) measurement capabilities, shrinking overlay and critical dimension (CD) error budgets driven by multi-patterning and via in trench CD measurements. With advent of advanced technology nodes and 3D processing, an increasing need is emerging for in-die metrology including across-structure and structure-to-structure characterization. This paper explores the latest capability offered by PeakForceTM Tapping Atomic Force Microscopy (PFT-AFM).

The use of traditional harmonic tapping mode for scanning high aspect ratio, and complex “3D” wafer structures, results in limited depth probing capability as well as excessive tip wear. These limitations arise due to the large tip-sample interaction volume in such confined spaces. PeakForce Tapping eliminates these limitations through direct real time control of the tip-sample interaction contact force. The ability of PeakForce to measure, and respond directly to tip-sample interaction forces results in more detailed feature resolution, reduced tip wear, and improved depth capability. In this work, the PFT-AFM tool was applied for multiple applications, including the 14nm fin and replacement metal gate (RMG) applications outlined below.

With the fin application, precision of 0.3nm is demonstrated by measuring 5 dies with 10 consecutive runs. Capability to resolve within-die and localized within-macro height variation is also demonstrated. In Figure 2, fin height measured on various in-die targets from two wafers with process offset are plotted in a bar chart for comparison. It is shown that under the same design of experiment (DOE) split, the wafer-to-wafer delta on different in-die targets is different. It is worth noting that, on target 2, localized fin height variation is observed in these measurements, as shown in Figure 3. On target 2, the fin bottom within the center long fin pair is slightly elevated compare to the outer area surrounding the fin pair. This results in

a localized fin height variation of about 2nm. Figure 4 is a comparison of the fin height on a scatterometry target in the scribe and two in-die targets. The scatterometry target is measured with both OCD and AFM which show good correlation. The two in-die targets are measured with AFM, and when plotted vs OCD data in the scribe, no correlation is found. This data strongly supports increasing trend that measurements in the scribe line do not represent in-die geometry.

In-die measurement capability of PFT on wafers at post-poly-removal step in the RMG module is also evaluated. Figure 5 illustrates the capability for direct in-die measurement of the overburden, the spacer pulldown, total gate height, and even the fin height beneath the gate using the PFT-AFM. Precision of 1.22nm for the fin height under the gate, 1.06nm for the total gate height, and 0.77nm for the overburden are achieved in this application on a semidense structure. To the knowledge of the authors, this is the first demonstration of a robust in-die measurement of the fin height under the gate.

The paper will discuss several use-cases of PFT AFM for measurement of 3D structures in advanced technology nodes. The work will demonstrate both structure-to-structure variation and localized variation within the structure. Results from DOE wafers, detailed measurement precision studies and correlation to reference metrology are presented for validation of this methodology.

9778-45, Session 10

## Large dynamic range scanning probe microscope for overlay improvements

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Most overlay metrology tools evaluate the overlay performance based on marker features which are printed along with the product features within each layer. However, due to various errors, correct overlay of marker features does not directly guarantee correct overlay of the product features. This project is aimed to develop a metrology tool for measuring the positioning error of product features with respect to the marker grid within each process layer, in order to allow for overlay improvements within the lithography process.

Figure 1 depicts a situational sketch of a typical die area with the marker features in the scribe lane. In order to compensate for scale mismatches between the metrology tool and other machines used in the lithography process, the location of the product feature will be measured relative to three alignment markers. The measured marker to product feature distance can be scaled back towards the coordinates system of other lithography and metrology tools using the marker grid as a reference.

Within this concept Scanning Probe Microscopy (SPM) techniques are used to measure the location of both the marker and product features within each layer. The major advantages of SPM over other imaging methods are the direct nature of the measurement, the high imaging resolution at (sub-) nanometer level and being non-destructive. Furthermore, SPM allows to fully trace the profile of each alignment marker. This marker profile information can be used to predict the marker position interpretation of other metrology and alignment tools, and thus compensate for tool matching errors. To compensate for the line-edge roughness several line traces are taken of each product feature and marker feature.

The major challenge in performing such marker to product feature measurement lies within the huge dynamic range requirements for the metrology tool; the marker and product feature can be several mm apart, while a sub-nanometer measurement accuracy is required in order to allow effective overlay improvement. Current available SPM tools are not capable of providing such high dynamic range measurements. Therefore, this project focusses on developing a novel SPM-based metrology tool that is capable of measuring the position of nano-features with sub-nanometer accuracy over several mm, in combination with the capability of measuring the 3D profile of the high aspect ratio marker features, and the ability to provide full coverage over a 300mm wafer.

In order to show the feasibility of this metrology concept a technology demonstrator is developed as depicted in figure 2. The concept utilizes a newly developed 6 DOF stage to control the position and orientation of the probe with respect to the sample with minimal Abbe-errors. The metrology concept utilized 6 heterodyne interferometers which measure the position and orientation of the probe with respect to the sample. For initial alignment of the SPM probe with the alignment markers a camera is used as depicted in figure 3.

In this presentation the metrology concept is further explained and the first results are shown demonstrating the potential of the SPM-based metrology tool.

9778-46, Session 10

## Parallel, high throughput atomic force metrology and inspection for EUV masks and wafers

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There are several challenges in current semiconductor metrology and inspection, where existing tools face several limitations for both EUV masks and Wafers. Measuring CD, pitch, height and profile of FIN and nanowire, resist profile characterization and its step height, inspecting ML and phase defects on EUV mask and blank, and also accurate profile characterization of absorber are examples of such challenges.

We have developed a high throughput atomic force microscope (AFM) with multiple mini AFMs (parallel AFM) to solve some of the aforementioned challenges. The demonstrator can measure both wafers as well as EUV masks. In this paper we show the experimental measurement results on wafers as well as EUV masks with four parallel AFMs. Figure 1 shows the photo of the parallel AFM demonstrator, ready for further testing.

The second generation of mini AFM and positioning unit have been developed with increased performance in terms of repeatability, reproducibility, speed of measurement and up-time percentage. Figure 2 shows the second generation of mini AFM and positioning unit, used in parallel AFM demonstrator.

With this demonstrator, several measurements have been performed, including:

1- Defect review on both mask and wafer

2- Roughness measurement on pre and post CMP

3- Patterned resist wafer

4- Patterned wafers after etch

Moreover, the system includes automatic tip exchange and alignment. The automated tip exchange system consists of two conveyor robots, one at each side of the machine, provided with multiple chip manipulators. In parallel motion, the manipulators take the chips from the input stock, move to above the scan heads, align the chips to the OBD-system, and place the chips at the scan heads. At the same time, a second conveyor removes the chips from the scan heads, and transfers them to the output stock. This enables a full chips replacement at all of the scan heads in less than 6 seconds. The input and output stock capacity is 220 chips. The system will be able to accept or reject input chips on the basis of support chip dimensions, cantilever size, and tip quality.

In this talk, we will present the details of the tool development status, as well as experimental measurements on wafer and EUV mask.

9778-47, Session 11

## SEM based overlay measurement between resist and buried patterns

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With the continuous shrink in pattern size and increased density, overlay control has become one of the most critical issues in semiconductor manufacturing. Recently, SEM based overlay of AEI (After Etch Inspection) wafer has been used for reference and optimization of optical overlay (both Image Based Overlay(IBO) and Diffraction Based Overlay (DBO)). At the AEI stage it is already too late to take any corrections into account from SEM measurements. Therefore, there is a clear need to have SEM based overlay measurements of ADI (After Develop Inspection) wafers in order to serve as reference for optical overlay and make necessary corrections before wafers go to etch. Furthermore, to make the corrections as accurate as possible, actual device like feature dimensions need to be measured post ADI. This is currently possible only with the CD-SEM.

In this study, we assess SEM based overlay measurement of ADI wafer by using several different samples from different stages of an N10 process flow. Simple as well as complex structures were evaluated. A simple structure consisting of resist/Si-ARC on silicon trench was measured and evaluated. These were similar to wafers used for scanner control. In order to use CD-SEM based measurements as reference for scanner overlay control both ADI and AEI wafers are required. The AEI wafers are usually needed for high order corrections. We will also discuss the overlay measurements between litho-etch-litho stages of a triple patterned metal 1 layer (M1) layer. To illustrate the complexities in image acquisition and measurement we will measure overlay between M1B resist and buried M1A-Hard mask trench. Finally, we will show how high accelerating voltage can detect buried pattern information by BSE (Back Scattering Electron). Finally, we discuss the merits of this method combined with standard optical metrology based corrections.

9778-48, Session 11

## In depth analysis of sampling plan optimization for overlay and alignment

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In advanced lithography nodes, overlay feedback is typically done with higher order grid and intra-field models. These models require a good coverage of overlay measurements over the wafer to prevent over-correction. But a very dense measurement is not possible in high volume production, so a smart sampling plan needs to be applied. Usage of higher order wafer alignment models also requires a good distribution of alignment marks over the wafer. The selection of a reduced set of alignment marks is of equal importance, because too many alignment marks reduce the throughput of the exposure tool, whereas a non-optimal distribution has severe impact on the overlay performance.

In this paper, we discuss two different types of methods determining a new sampling plan for both alignment and overlay metrology. The first method is a so-called geometrical optimization method. it takes into account the type of model that is used, the locations of chips and fields on the wafer and the location of the marks (templates). But no overlay or alignment measurement information is used. The advantage is that it is not biased by a sample data set containing only a subset of possible overlay or alignment signatures. But the disadvantage is that it is not process specific.

The second method is a so-called data based optimization method. For this method, a set of densely measured alignment or overlay data is needed. The optimization tries to determine a sampling plan whose modeling results resemble the results of the dense sample data set. The advantage of such a method is that it is fine-tuned to a specific process, but on the other hand, it may not cover all possible overlay or alignment signatures.

For both methods there are several different approaches to optimize the sampling plan. And there are a lot of knobs that can be used to adjust the method to a specific process or to make the result more applicable to current measurement limitations. We will discuss the impact of these knobs in several use cases.

It is not trivial to assess the quality of the overlay sampling plan for implementation in high volume manufacturing. There are three different factors that need to be taken into account. First, the overlay model parameters calculated from the optimized sampling plan should represent the dense measurement as closely as possible. Second, there should be no impact on feedback loops. This requires that the individual parameters are not destabilized. Third, the dispositioning criterion, like the Mean+3-Sigma of the overlay values should be equal to the value of the dense measurement. We propose a novel method to judge the quality of the sampling plan using the above three factors.

For alignment sampling plan optimization, the impact on the overlay measurement must be taken into account as well. We will show this based on extensive simulation. In summary, we weigh the pros and cons of different optimization methods and propose a standard procedure.

9778-49, Session 11

## Device overlay method for high-volume manufacturing

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Advancing technology nodes with smaller process margins require improved photolithography overlay control. Overlay control at develop inspection (DI) based on optical metrology targets is well established in semiconductor manufacturing. Advances in target design and metrology technology have enabled significant improvements in overlay precision and accuracy. One approach to represent in-die on-device as-etched overlay is to measure at final inspection (FI) with a scanning electron microscope (SEM). Disadvantages to this approach include inability to rework, limited layer coverage due to lack of transparency, and higher cost of ownership (CoO). A hybrid approach is investigated in this report whereby infrequent DI/FI bias is characterized and the results are used to compensate the frequent DI overlay results. The bias characterization is done on an infrequent basis, either based on time or triggered from change points. On a per-device and per-layer basis, the optical target overlay at DI is compared with SEM on-device overlay at FI. The bias characterization results are validated and tracked for use in compensating the DI APC controller. Results of the DI/FI bias characterization and sources of variation are presented, as well as the impact on the DI correctables feeding the APC system. Implementation details in a high volume manufacturing (HVM) wafer fab will be reviewed. Finally the impact on electrical test and yield will be discussed as well as future directions of the investigation.

9778-50, Session 11

## Eliminating the offset between overlay metrology and device pattern cell using computational target design

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Designing metrology targets that mimic process device cell behavior is becoming a common component in overlay process control. For an advanced DRAM process, the extreme illumination methods needed to pattern the critical device features makes it harder to control the aberration induced overlay delta between metrology target and device patterns. To compensate for this delta, a Non-Zero-Offset is applied to the metrology measurement that is based on a manual calibration measurement using CD-SEM Overlay. This method is laborious and slow, requiring regular measurement and offset correction in a High Volume Manufacturing scenario. Ultimately, inline Yield measurements may also be required to verify if the offsets are optimal. Another disadvantage is that these offsets are scanner dependent as aberrations can very per machine lens and vary over time, thus requiring these offsets to be managed continuously on a per scanner basis.

In addition to these scanner lens aberration effects, the processed induced asymmetry which results from etch, CMP, CVD affects both the precision and accuracy performance of a target. Optimization must balance device matching with process robustness in a target which will be both printable and detectable.

In this paper, we document how this mismatch can be minimized through the right choice of metrology targets and measurement recipe. The device matching capabilities of the Design for Control computational application have been utilized on a DRAM process to reduce the delta between device cell and the ASML YieldStar metrology tool targets between two critical layers which had previously suffered from severe offset effects. We will present results showing that we could almost completely eliminate the offset and hence reduce the need for regular manual correction.

9778-51, Session 11

## Accuracy in optical overlay metrology

Barak Bringoltz, Tal Marciano, Tal Yaziv, Yaron DeLeeuw, Yoel Feler, Ido Adam, Evgeni Gurevich, Noga Sella, Ze'ev Lindenfeld, Tom Leviant, Lilach Saltoun, Eltsafon Island-Ashwal, Dror Alumut, Yuval Lamhot, KLA-Tencor Israel (Israel); Xindong Gao, KLA-Tencor China (China); James R. Manka, Bryan Chen, KLA-Tencor Taiwan (Taiwan); Mark P. Wagner, Dana Klein, KLA-Tencor Israel (Israel)

Overlay metrology in modern advanced semiconductor manufacture has an accuracy budget which can be as tight as a few nanometers. To measure overlay all currently available optical metrologies rely on measurements of signal asymmetry assumed to be the result of overlay between patterning steps. However, process variations may cause asymmetries in the measured structures, violating this assumption and consuming the overlay metrology budget. In this paper we discuss the mechanism by which process variations determine the accuracy performance of optical metrology. We start by focusing on scatterometry, and show that the underlying physics of this mechanism involves interference effects between cavity modes that travel between the upper and lower gratings in the scatterometry target. A direct result is the behavior of accuracy as a function of wavelength, and the existence of relatively well defined spectral regimes in which the overlay accuracy and process robustness degrades (`resonant regimes'). These resonances are separated by wavelength regions in which the overlay accuracy is better and independent of wavelength (we term these `flat regions'). The combination of flat and resonant regions forms a spectral signature which is unique to each stack and carries certain universal features with respect to different types of process variations.

We discuss this universality, demonstrate it with simulations, present a phenomenology which describes it, and a model to understand universality from first principles.

Next, we show how to characterize overlay performance with a finite set of metrics, derived from the theory and phenomenology of accuracy, and especially, from the angular behavior of the signal and the way it flags resonances. Importantly this can be defined on a per measurement basis. These metrics are used to guarantee the selection of accurate recipes for the metrology tool, and for process control with the overlay tool.

We explain the metrics, how they reflect overlay inaccuracies and how they can be used to optimize metrology recipes and targets.

We end with comments on the similarity of imaging overlay to scatterometry overlay, and on the way the pupil overlay scatterometry and field overlay scatterometry differ from an accuracy perspective.

9778-52, Session 11

## A study of swing-curve physics in diffraction-based overlay

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With the increase of process complexity in advanced nodes, the requirements of process robustness in overlay metrology continues to tighten. Especially with the introduction of newer materials in the film-stack along with typical stack variations (thickness, optical properties, profile asymmetry etc.), the signal formation physics in diffraction-based overlay (DBO) becomes an important aspect to apply in overlay metrology target and recipe selection.

In order to address the signal formation physics, an effort is made towards studying the swing-curve phenomena through wavelength and polarizations on production stacks using simulations as well as experimental technique using DBO. The results provide a wealth of information on target and recipe selection for robustness. Details from simulation and measurements will be reported in this technical publication.

9778-53, Session 11

## Enhacement of intrafield overlay using a design based metrology system

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We are going to cerify that the overlay values extracted from optical measurement cannot represent the circuit level overlay values and also, we are going to demonstrate the possibility to correct misregistration between two layers using the overlay data obtained from the DBM system.

9778-60, Session PSWed

## A novel method to quantify the complex mask patterns

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Immersion technology has successfully extends the life of 193nm wavelength lithography in the semiconductor patterning process. However, as we are pushing the k1 factor further to the cliff of 0.3x regime, the patterning fidelity degraded significantly. In this article, a novel method to quantify the mask fidelity of complex 2D patterns is proposed. By this method, the critical dimension (CD) error of both edge placement and corner rounding can be well described by using two indices "bias" and "blur" respectively. The "bias" is defined as the distance between the real mask results and the ideal targets, and the "blur" is defined as standard deviation of a Gaussian

kernel to quantify the mask corner rounding. These two indices are not only able to describe the mask performance but also able to link with model parameters that used in optical proximity correction (OPC) and some other applications. In this article, we demonstrate how to link the mask specification and wafer CD performance on the critical and aggressive mask patterning

9778-67, Session PSWed

## The effect of quantum noise on line-edge roughness

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The throughput of a lithographic system is an important parameter in a typical production line.

This parameter can be increased in several ways. In optical lithography, for example, a more powerful source is one solution.

In electron-beam lithography, an increase of the number of parallel beams is another solution. In either case, the use of a more sensitive chemically amplified resist (CAR) results in a reduction of the required illumination dose, and hence a reduction of the exposure time of the wafers.

In order to maximize throughput, it is tempting to choose the most sensitive CAR with the lowest possible illumination dose.

In that limit, however, an increase of line edge roughness (LER), and hence an insufficient control of critical dimension (CD) is observed.

This increase of LER is primarily caused by fundamental quantum noise (shotnoise) effects and becomes the dominant mechanism in the formation of LER.

Our attempt in this theoretical study, is to develop a Monte-Carlo framework for the investigation of shotnoise limited LER formation.

At first we determine the initial distribution of photo acid generators (PAGs) by using our home-built simulator for electron-matter interaction.

The distribution of PAGs is then used to determine the breaking of bonds in the resist by considering a diffusion like process in the post exposure baking (PEB) phase.

We now determines the boundary between exposed and unexposed resist.

In reality, there is also a development phase, which we so far have ignored in this study.

We acknowledge that this is a simplified view of post lithographic processing.

The exposed resist gives rise to a three dimensional feature which is then fed into our scanning electron microscopy (SEM) image simulator, because this is how LER/shotnoise effects are measured.

The line edge roughness in the resulting two dimensional top-down image is further processed using PSD analysis.

Our expectation is that this model will provide insight in the effects on LER of changing parameters such as resist thickness, PAG diffusion and dose distribution.

9778-68, Session PSWed

## Scatterometry-based process control for nanoimprint lithography

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Nanoimprint lithography (NIL) is regarded as one of the candidates for next-generation lithography (NGL) toward single-nanometer manufacturing. Among the wide variety of imprint methods, Jet and Flash imprint (J-FIL) is the most suitable for IC manufacturing for which high productivity and high yield are required. In J-FIL, resist is selectively applied by an inkjet to an imprinting field whose size is almost the same as that of an exposure field of a conventional optical scanner (~26mm x 33mm), and then a patterned mask (template) is directly contacted to the field under UV exposure. This resist apply and imprint process is carried out from field to field with step and repeat, which is similar to a conventional stepper or scanner.

In principal, the critical dimension (CD) of NIL resist pattern is determined by the CD of template pattern. Unless one template is changed to another, NIL does not have a knob to directly control CD on a wafer, such as exposure dose and focus in optical lithography. Alternatively, CD would be controlled by adjusting residual layer underneath NIL resist pattern and controlling the etch process to transfer the NIL pattern to a substrate. Controlling the residual layer thickness (RLT) and etch condition can change etch bias, resulting in controlling the CD of etched pattern. RLT is controllable by the dispense condition of the inkjet. For CD control, the metrology of RLT and feedback of the results to the dispense condition are extremely important.

Scatterometry is the most promising metrology for the task because it is nondestructive 3D metrology with high throughput. In this paper, we discuss how to control CD in the NIL process and propose a process control flow based on scatterometry.

9778-69, Session PSWed

## 2D and 3D isolation mounts scatterometry using RCWA and FDTD method

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Scatterometry is capable of measuring the critical dimension and profile measurements of grating structure. It is possible to get down to approximately 8nm with high precision in semiconductor manufacturing process control. The quality of measurement results depends on the setting groove model parameters, and on algorithms used by the analysis software. So, we develop the simulator to test the efficient parameter settings to raise the scatterometry's performance. In the papers on Microlithography in 2004-2008, we completed the 3D-FDTD analysis of the arbitrary shapes for isotropic and anisotropic mediums. In Microlithography 2010-2012, we developed the scatterometry simulation software that has the spectroscopy calculation and optimization algorithm systems. We calculated the spectroscopy using the Rigorous Coupled Wave Analysis that provides a method for calculating the diffraction of electromagnetic waves by periodic grating structures. The Conjugate Gradient and the Binary-Coded Genetic Algorithm methods were used to automatically search data that matches the given spectrum. In 2013, we sped up the scatterometry simulation for the 3D RCWA by using GPU and CUda LApack. The 2D scatterometry simulator was improved using a Real-Coded GA. In Microlithography 2014-2015, we examined the sensitivity of scatterometry for the 2D and 3D isolation mounts on the substrate by applying the Perfectly Matching Layer in the RCWA. The RCWA is usually used for the period grooves and the scatterometry is now used for measuring the period groove shapes. However, by using the PML to absorb the outgoing waves from the interior of a period computational region for RCWA, we can analyze the scatterometry for the isolation mounts. We analyzed the reflectance from the silicon and resist single mount and the silicon double mounts on the silicon substrate by changing the mount length, width and height for single mount and the mount positions for the double mounts.

In this paper, we continue to examine the scatterometry's sensitivity for the 2D and 3D isolation mounts by applying the PML in the RCWA. The scatterometry characteristic is examined by choosing the n-th power cosine type mounts and approximating the smoothly changing mount shape with three or more trapezoids. We analyze the reflectance from the silicon and resist single mount and the silicon double mounts on the silicon substrate by changing the mount length, width, height and the n-th power cosine shape for single mount and the mount positions for the double mounts. First, we investigate the beam width dependences of reflectance. We also show the propagation properties of the electromagnetic fields propagating for the isolation mounts on the substrate. Next, we calculate the optical scattering property from the isolation mounts by the 2D and 3D FDTD analysis. And, we compare the scattering property results obtained from RCWA and FDTD method. Finally, the scatterometry simulator is developed for the isolation

mounts using the Conjugate Gradient method and the Real-Coded Genetic Algorithm. The CG method and the RCGA are used to automatically search the data which resembles the given spectrum. The optimum solution sometimes falls into another local field in the CG method. We use the RCGA to make a more sensitive solution and to get better fitting mount figures. Then, we understand the scatterometry observation is possible in several microns beam widths.

9778-70, Session PSWed

## Comparison of left and right side line-edge roughness in lithography

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The line edge roughness (LER) is a critical yield-limiting factor in the fabrication of semiconductor devices. Therefore, accurate metrology and characterization of LER is important. The left and right side LER of a line or space feature are usually thought to be the same by most of the people. However, a few researchers pointed out that this may not be true one decade ago[1,2]. V. Constantoudis et al, found that right side 3? LER is 10-20% higher than left side for different resists, but no detailed analysis and reason were shown[2].

In this paper, a comprehensive comparison of left and right side LER will be shown. The analysis will cover multiple factors in lithography, such as horizontal and vertical directions, through-pitch and through CD, post litho and post etch.

In a preliminary analysis, the horizontal and vertical direction L/S patterns are measured. Right side LER is same with left side in low frequency region, but is higher than left side in middle and high frequency regions for both horizontal and vertical directions. Left side LER PSD is same for both horizontal and vertical directions. Similar for right side LER PSD. Therefore, the difference of left and right side LER is not due to horizontal and vertical directions in lithography.

To verify whether this effect is induced by metrology, horizontal line is scanned in both 0° and 180° rotations in CDSEM metrology. The left side edge in 0° rotation becomes right side edge in 180° rotation. The right side edge in 0° rotation becomes left side edge in 180° rotation. The large right side LER in 0° rotation, which is the left side in 180° rotation, becomes smaller than the left side in 0° rotation, which is the right side in 180° rotation. It contradicts with the experiment result. Therefore, metrology, not lithography process, induces the left and right side LER difference. Left side LER PSD in 0° rotation is same for both 0° and 180° rotations. Similar for right side LER PSD. This is a clear evidence that the left and right side LER are same if scanned in same manner, for example, e-beam scans from trench to line direction. Detailed data pending for approval.

In conclusion, the left and right side LER are same from lithography process. But the metrology scan direction induces difference. The right side 3? LER is 19% and 12% larger than left side for the L/S in horizontal and vertical directions, respectively in the experiment. Since most of the LER difference is in high frequency region, the noise induced by the electron scattering in CDSEM metrology may be the real reason.

Reference:

1.M. Ercken, et al, “Line edge roughness and its increasing importance”, Proceeding of Interface, (2002)

2.V. Constantoudis, et al, “Photo-Resist Line-Edge Roughness Analysis Using Scaling Concepts”, Proc. SPIE, 5038, 901-909, (2003)

9778-71, Session PSWed

## Generalized measurement configuration optimization for accurate reconstruction of periodic nanostructure using optical scatterometry

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Optical scatterometry, also referred to as optical critical dimension (OCD) metrology, is currently a state-of-the-art technique for the in-line wafer-to-wafer process monitoring and control in lithography and etch processes, due to its typical advantages such as low cost, high throughput, small hardware, and minimal sample damage when compared with traditional image-based metrology techniques. Generally, the process of reconstructing periodic nanostructures is formulated as a minimization problem of the least square (LSQ) function, which requires abundant measurement information to guarantee that the minimization problem is overdetermined. Hence, the measurement signature should be a vector containing multiple data points, which directly requires the variability of measurement conditions such as wavelength, incident angle and azimuthal angle. In practice, considering the efficiency of data acquisition and analysis, it is common to choose a subset of the three measurement conditions from their available ranges. The combination of the selected wavelengths and incidence and azimuthal angles is defined as the measurement configuration. It is worthwhile to point out that the measurement accuracy varies with the measurement configuration [1], which brings up the issue of measurement configuration optimization for achieving the highest measurement accuracy.

In the present article, we propose a general measurement configuration optimization method arising from the theoretical analysis of the error propagation using the first order Taylor expansion of the LSQ function [2], which is generally expressed as

In the above equation, yj is the jth measured data point, and y is the measured signature as a vector containing m data points. fj(x) is the jth calculated data point with respect to the profile parameters x = [x1, x2, ..., xn]T that describe the geometry, and a, the measurement configuration, which in general consists of the wavelength, the incident angle and azimuthal angle. f(x,a) is the calculated signature as a vector containing m data points. wj is the jth weight factor, and w is an m ? m diagonal matrix with diagonal elements {wj}. Then by using the single value decomposition (SVD) technique and related matrix theory, we can deduce that the optimal measurement configuration is within the following set

where is the domain of measurement configuration a, is the Jacobian matrix with respect to the LSQ function, and denotes the Frobenius norm. ? is a pre-selected positive real number, the choice of which depends on the user’s belief about the reliability of the measurement configuration optimization procedure.

Figure 1 presents the measurement setup of a dual-rotating compensator Mueller matrix ellipsometer (DRC-MME) as well as the scanning electron microscope (SEM) cross-section image of a trapezoidal etched Si grating. We can obtain the full Mueller matrix elements of the Si grating under measurement with the DRC-MME setting. Figure 2(a) presents the simulation results of the Frobenius norm of the error propagation matrix under different incident and azimuthal angles, while Fig. 2(b) presents the corresponding sum of absolute values of the geometrical parameter departures. As expected, Fig. 2(b) presents the same downtrend as that of Fig. 2(a) when the value of azimuthal angle keeps growing. We then set the value of ? as 0.0125, and pick out those measurement configurations that correspond to those values of smaller than 0.0125. As can be seen in Fig. 3, under all these small the corresponding extracted error sums are smaller than seven nanometers, while for those large nearly all of the extracted error sums are larger than eight nanometers. The above simulations have demonstrated the feasibility of the proposed method in finding optimized measurement conditions.

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9778-72, Session PSWed

## Hybrid overlay metrology for high-order correction by using CD-SEM

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Overlay control has become one of the most critical issues for semiconductor manufacturing. Advanced lithographic scanners use high-order corrections or correction per exposure to reduce the residual overlay. It is not enough in traditional feedback of overlay measurement by using ADI wafer because overlay error depends on other process (etching process and film stress, etc.). It needs high accuracy overlay measurement by using AEI wafer. WIS (Wafer Induced Shift) is the main issue for optical overlay, IBO (Image Based Overlay) and DBO (Diffraction Based Overlay).

We designed dedicated SEM overlay targets for dual damascene process of N10 by i-ArF multi-patterning. The pattern is same as device-pattern locally. Optical overlay tools select segmented pattern to reduce the WIS. However, segmentation has its limits, especially for via-patterns, where keeping sensitivity and accuracy is challenging. In this work we evaluated the difference between via-patterns and relaxed pitch gratings which are similar to optical overlay target at AEI. CD-SEM can estimate asymmetry property of target from image of pattern edge. We will compare full map of SEM overlay to full map of optical overlay for high order corrections ( correctables and residual fingerprints).

9778-73, Session PSWed

## Application of overlay modeling and control with Zernike polynomials in an HVM environment

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Shrinking technology nodes and smaller process margins require improved photolithography overlay control. Generally, overlay measurement results are modeled with Cartesian polynomial functions for both intra-field and inter-field target locations and the model coefficients are sent to an advanced process control (APC) system operating in an XY Cartesian basis. Dampened overlay corrections, typically via exponentially or linearly weighted moving average in time, are then retrieved from the APC system to apply on the scanner for subsequent lot exposure. The goal of the above method is to process lots with corrections that target the least possible overlay misregistration in steady state as well as in change point situations. In this study, we model overlay errors on product using Zernike polynomials with same fitting capability as the process of reference (POR) to represent the wafer-level terms, and use the standard Cartesian polynomials to represent the field-level terms. APC calculations for wafer-level correction are performed in Zernike basis while field-level calculations use standard XY Cartesian basis. Finally, weighted wafer-level correction terms are converted to XY Cartesian space in order to be applied on the scanner, along with field-level corrections, for future wafer exposures. Since Zernike polynomials have the property of being orthogonal in the unit disk we are able to reduce the amount of collinearity between terms and improve overlay stability. Our real time Zernike modeling and feedback evaluation was performed on a 20-lot dataset in high volume manufacturing (HVM) environment. The measured on-product results were compared to POR and showed a 7% reduction in overlay variation including a 22% reduction in linear model terms variation. This led to an on-product raw overlay Mean + 3Sigma X&Y improvement of 5% and resulted in statistically significant yield improvement. As a next step, we will evaluate the combination of Zernike modeling for wafer-level and Legendre modeling for field-level. By being orthogonal on the unit square, Legendre polynomials have the potential to reduce the amount of cross-talk between field-level terms and improve intra-field overlay stability.

9778-74, Session PSWed

## Highly sensitive focus monitoring technique based on illumination and target co-optimization

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Although the semiconductor industry has made significant improvements to the achievable resolution of the lithography patterning, this impressive success comes at the cost of losing the process window (PW) of the devices. In particular, the inverse proportionality to the square of numerical aperture (NA) in depth of focus (DOF) is a major challenge, especially in an advanced high NA immersion lithography, raising the importance of process control in semiconductor manufacturing. As a result, real-time monitoring capability to detect process variations on production wafers is emerging as a new industry requirement. Currently, routine monitoring of focus and dose variation on a dedicated simple stack wafer using a dedicated mask is still essential, however controlling the manufacturing process within such a small PW requires monitoring process variations with much higher sensitivity.

Several different process monitoring techniques corresponding to different types of metrology tools for the use of specialized targets have been proposed and adapted in semiconductor manufacturing. A phase shift focus monitor (PSFM) based on an alternating phase shift mask (PSM) has been one of the well-known methods since it was first introduced by T. Brunner in 1994. This technique is basically measuring the lateral shift caused by focus errors using a 90 degree PSM illuminated by a small sigma coherent source. Another notable approach is to use an additional Cr mask in the backside of the reticle for generating asymmetric illumination. The main physical principle behind these two approaches is to break telecentricity of the exposure system, and therefore the aerial image formed by the interference between multiple diffraction orders having different phase delays can cause image displacement error with focus variation, which is described in Fig.1. While these techniques have certain advantages such as the linearity of pattern shifts to focus variation and the simplicity of the measurement, the critical issue is complex mask manufacturing, resulting in excessive mask cost.

Since 2010, the advanced immersion scanner can provide the freeform illumination that enables the use of any kind of custom source shape by using a programmable array of thousands of individually adjustable micro-mirrors. Therefore, one can produce nontelecentricity using an asymmetric illumination in the scanner with the optimized focus target on the cost-effective binary OMOG mask. Then, focus variations directly translate into easily measurable overlay shifts in the printed pattern with very high sensitivity ($\Delta$Shift/$\Delta$focus ~=0.66nm/1nm). In addition, such a freeform illumination allows us to computationally co-optimize the source and the target, simultaneously, providing not only vertical or horizontal shifts, but also diagonal shifts. Further introducing sub-resolution assist features (SRAF) and/or sub-resolution inverse features (SRIF) can successfully yield the design of robust focus metrology targets that ensure printability on the wafer. Focus-induced pattern shifts can be accurately measured by standard wafer metrology tools such as CD-SEM and imaging based overlay metrology tool, as shown in Figs 2 and 3. In the conference, we will present a novel focus monitoring technique with several new focus target designs.

9778-75, Session PSWed

## Scan direction induced charging dynamics and the application for detection of gate to S/D shorts in logic devices

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Gate to source/drain (S/D) short is the most common and detrimental

failure mechanism for advanced process technology development in Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) device manufacturing. Especially for sub-1Xnm nodes, MOSFET device is more vulnerable to gate-S/D shorts due to the aggressive scaling. The detection of this kind of electrical short defect is always challenging for in-line electron beam inspection (EBI), especially new shorting mechanisms on atomic scale due to new material/process flow implementation. The second challenge comes from the characterization of the shorts including identification of the exact shorting location. In this paper, we demonstrate unique scan direction induced charging dynamics (SDCD) phenomenon which stems from the transistor level response from EBI scan at post metal contact chemical-mechanical planarization (CMP) layers. We found that SDCD effect is exceptionally useful for gate-S/D short induced voltage contrast (VC) defect detection, especially for identification of shorting locations. The unique SDCD effect signatures of gate-S/D shorts can be used as fingerprint for ground true shorting defect detection. Correlation with other characterization methods on the same defective location from EBI scan shows consistent results from various shorting mechanism. A practical work flow to implement the application of SDCD effect for in-line EBI monitor of critical gate-S/D short defects is also proposed, together with examples of successful application use cases which mostly focus on static random-access memory (SRAM) array regions. Although the capability of gate-S/D short detection as well as expected device response is limited to passing transistors due to the design restriction from standard 6-cell SRAM structure, SDCD effect is proven to be very effective for gate-S/D short induced VC defect detection as well as yield learning for advanced technology development.

9778-76, Session PSWed

## High-throughput atomic force microscope for self-assembled monolayers metrology and defect inspection

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Self-Assembled Monolayers (SAM) are a promising new development for patterning and templating for Atomic Layer Deposition (ALD). For this application quality of the SAM is critical. Major issues to have under control are surface coverage and presence of defects (pinholes). Even the smallest pinholes (< 1nm) can be disastrous as Atomic Layer Deposition will grow material on each exposed surface site. Evaluating the quality of the SAM therefore poses stringent requirements for the resolution and accuracy of inspection tools. We report here on the use of high throughput Atomic Force Microscopy (AFM) as a tool to inspect SAMs. In our view, having a high-throughput automated AFM system and analysis is critical to reach statistically relevant results and perform inspection over a significant distribution of sites on the substrate.

We present an analysis of a SAM grown on two different substrates to highlight the impact of substrate on the quality of the resulting monolayer and subsequent ALD process. We inspected 100 sites in a semi-random pattern on each sample and perform automated post-processing to extract the surface coverage and number and size of pinholes for each sample. We correlate the results from AFM inspection of the monolayers on each sample with final quality of samples that have undergone ALD. We see that very small pinholes (<10 nm) are common underlining the necessity of an inspection tool which can detect such small defects reliably.

9778-77, Session PSWed

## Image-based overlay (IBO) target segment design on self-aligned patterning process

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Self-Aligned Double Patterning (SADP) is widely applied in advanced sub-4X patterning technology, especially for the 1D resolution shrinkage of memory technology. As the application of SADP make lithography minimum pitch down to half of design pitch with the remaining spacer aside core, its alignment mark and overlay (OVL) mark have to be well-segmented to ensure enough mark contrast. In this paper, we designed two types of IBO BIB OVL target: bar-segmentation and background–segmentation with different duty ratio. Based on these two designed types of marks, we focus on the OVL of 2nd photo layer to 1st SADP layer with the core removed (which means spacer grating structure remained). We studied the effect of the overlay target segmentation on the precision and robustness of wafer-level overlay performance. Different lithography processes were also studied, including single layer lithography and tri-layer lithography with planarized spacer grating structures. We found there are strong correlations between overlay measurement accuracy and background segmentation rules. The results of our study will be presented and discussed in this paper.

9778-78, Session PSWed

## Improving focus performance at litho using diffraction-based focus metrology, novel calibration methods, interface and control loop

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In advanced optical lithography the requirements of focus control continues to tighten. Usable depth of focus (DoF) is already quite low due to typical sources of focus errors, such as topography, wafer warpage and the thickness of photoresist. And now the usable DoF is further decreased by hotspots (design and imaging hotspots). All these have put extra challenges to improve focus metrology, scanner focus stability calibrations and on-product correction mechanisms.

Asymmetric focus targets are developed to address robustness in focus measurements using diffraction-based focus (DBF and μDBF) metrology. A new layout specific calibration methodology is introduced for baseline focus setup and control in order to improve scanner focus uniformity and stability using the measurements of the above mentioned asymmetric targets. A similar metrology is also used for on product focus measurements. Moreover, a few novel alternative methods are also investigated for on-product focus measurements.

Data shows good correlation between DBF and process on record (POR) method using traditional FEM. The new focus calibration demonstrated robustness, stability and speed. This technical publication will report the data from all the above activities including results from various product layers.

9778-79, Session PSWed

## Assistant researchers from Institute of Microelectronics, Chinese Academy of Sciences

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As the shrink of critical dimension (CD), it is difficult to enlarge the process window, and the process window/depth of focus (DOF) tightens for advanced technology nodes. From the 16nm node onwards, the limits of immersion projection systems makes much more difficult to absorb the challenges of scaling since the DOF will be less than 100nm, which leads to the full manufacturing focus budget. It becomes evident that the monitor and control of focus error is becoming more and more critical for maintaining the viable process latitude. There are lots of focus monitor

techniques discussing the accurate prediction options for the scanner focus error in previous papers.

With the purpose of measuring the scanner focus error more accurate, a new focus monitor mask having novel grating structure is proposed in this paper. It had been demonstrated that if the mask pattern had a property of being able to generate asymmetry between positive and negative diffraction orders, the prediction of defocus could be translated to an easily measured the pattern shift perpendicular to the optical axis. As the phase shift mask is the common structure which can satisfy this requirement, the phase shift mask is applied in this paper. Firstly, by using the rigorous vector imaging theory, the relationship between the defocus and pattern shift of mask image is established in a compact expression which can be easily solved by numerical calculation. Applying the Fourier series decomposition to intensity distribution of mask pattern, the pattern shift can be translated to the phase shift of first order spectrum. Secondly, the detail of mask pattern structure is described on the theoretic basis. The grating pattern is composing of transparent line, opaque line, ϖ -phase shift groove and ϖ/2-phase shift groove with their width ratio equivalent to 1:4:1:2. Under the circumstance of immersion lithography with ArF excimer laser, the depth of these two grooves are and , respectively, where is positive integer, is the wavelength of laser, and is the refractive index of mask material. With this structure, the one of the first order and one of the second order of diffraction spectrum are eliminated. Both the two orders are positive or negative. As a result, the lithography image is formed by the interference of the zeroth order and the other two orders, which is more sensitive to the change of focus. At last, we choose immersion lithography with a numerical aperture of 1.35 and conventional illumination as an example to demonstrate the accuracy of the new focus monitor mask. The conventional phase grating focus monitor (PGFM) is also selected in the order of comparing. The simulations are accomplished by the lithography simulator PROLITH. In the simulations, the sigma of illumination source is 0.12. The width of transparent line, opaque line, -phase shift groove and -phase shift groove are 41nm, 164nm, 41nm and 82nm, respectively. The simulation results showed that the accuracy is improved more than 20%, comparing with the conventional PGFM.

9778-80, Session PSWed

## Spacer multi-patterning control strategy with optical CD metrology on device structures

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Spacer multi patterning process continues to be a key enabler of future design shrinks in DRAM and NAND process flows. Improving Critical Dimension Uniformity (CDU) for main features remains high priority for multi patterning technology and requires an improved metrology and control solutions.

In this paper Spacer Patterning Technology is evaluated by using an angle resolved scatterometry tool for both intra field control of the core CD after partition etch (S1) and interfield pitch-walking control after final etch (S1-S2). The intrafield measurements were done directly on device using dense sampling. The dense inter-field corrections were based on sparse full-wafer measurements on biased OCD targets. The CDU improvement after partition-etch was verified by direct scatterometer and CD-SEM measurement on device. The final etch performance was verified with scatterometer on OCD target and CD-SEM on device.

The scatterometer metrology in combination with the control strategy demonstrated a consistent CDU improvement of core (S1) intrafield CD after partition etch between 23-39% and 47-53% on interfield pitch-walking (S1-S2) after final etch. To confirm these improvements with CD-SEM, oversampling of more than 10 times is needed compared to scaterometer.

Based on the results it is concluded that scatterometry in combination with the evaluated metrology and control strategy in principle qualifies for a spacer process CDU control loop in a manufacturing environment.

9778-81, Session PSWed

## Study on overlay AEI-ADI shift on contact layer of advanced technology node

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As semiconductor integrated circuit industry has been driven into advanced technology node (28nm, 14nm, etc.), the device CD (Critical Dimension) is getting smaller, therefore the overlay budget control is more and more tightened and crucial for device performance and yield guarantee. Understanding overlay AEI-ADI (AEI: After Etch Inspection; ADI: After Develop Inspection) shift is extremely important, because it is the basis for using overlay ADI result to control lithographic process into final satisfactory AEI outcome. In this paper, we focus on one wafer-level overlay AEI-ADI shift on contact layer of one advanced technology node. In intra-shot level, a special finger print of center-edge difference is also found, which is that the shift vectors within shot center area are one group of being almost the same length and direction and the shift vectors on the shot edges are the other group of being much smaller length and varied directions. We did the overlay slice subtraction (overlay at an offset focus slice subtracts overlay at best focus slice) at ADI on an IBO (Image Based Overlay) optical overlay machine and found that the overlay slice subtraction map matches well the overlay AEI-ADI shift map, both at wafer level and shot level. We did a lot of study to investigate this interesting correlation and found that the overlay slice subtraction result actually reflects the PR (Photo Resist) profile tilt, and etch shadow effect due to PR tilt finally leads to AEI pattern location shift. We also did further investigation to check what causes the PR tilt and finally pinned down to the stress induced by the CVD-deposited (CVD: Chemical vapor Deposition) thick hard mask film. We also came out with a suspected model to explain the mechanism how hard mask film stress induces the PR tilt that finally leads to overlay AEI-ADI shift.

9778-82, Session PSWed

## ADI defect reduction of SADP film stack for sub-40nm flash memory application

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Before EUV (Extreme Ultra-Violet) dominates the lithography technology as semiconductor industry shrinks feature sizes to 40nm and beyond, DPL (Double Pattering Lithography) becomes the mainstream patterning strategy. Among all these DPL technologies of SADP (Self-Aligned Double Patterning), DELE (Dual-Etch Double Patterning) and SEDL (Single-Etch Double Patterning), SADP has attracted the highest attention due to its robustness against overlay errors for pitch reduction, spacer mask pattering and sidewall spacer transfer patterning . In particular, in NAND Flash Memory, SADP has been widely used in AA (Active Area), CG (Control Gate) and Metal interconnects (e.g. Metal.1 and Metal.2).

In this work, ADI (After Development Inspection) of film stack for SADP in AA and CG loops of NAND Flash Memory has found serious particle performance. Diverse defects, in different appearance of in-film buried particles, bumps, bubbles, surface fallings, and wafer-edge peelings and so on, have been observed. Continuous improvement actions have been carried out in two ways: One is the process optimization of APF (Advanced Patterning Films, hereby, it is a-C: H and being used both as etch core and

hard mask) layers, key parameters like process temperature, RF power, chamber pressure, carrier gas, pre- deposition purge with Argon gas, post-deposition O2-pasma modification and RF purge with Helium plasma. The other is hardware upgrade with shadow ring settings at wafer edge.

Achievements have been obtained in the following aspects:

1) By increasing defect scanner's sensitivity from 90nm to 40nm, single-layer and multi-layer samples could be characterized more properly. By process optimization, adder defect count on bare Si wafers has been reduced significantly by 10 times lower.

2) With film stack optimization and wafer-edge shadow ring settings, no wafer edge peelings have been found any more, neither on bare Si wafers nor on pattern wafers, which means that all the wafer edge dies are saved efficiently.

3) By-10-lots impact has been reduced by 20%, by-100pcs-wafer impact reduced by 50%.

4) Long-term statistic trace of mass-production has found a reduction of defect density by 30% and a yield improvement by 3%.

5) Redundancy ratio of massive products has been reduced by 15% successfully.

6) WAT performance has been well kept stable.

9778-83, Session PSWed

## Design-guided data analysis for identifying systematic pattern defects and establishing process window

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In order to analyze the hot scan results on FEM/PWQ wafer more carefully and extract more defects-of-interest (DOI) from those results, we describe a technique that introduces image-and-design integration methodologies into the data analysis workflow. The end results are weak-pattern activity based on lithography modulation and a more accurate process window.

These image-and-design techniques include contour extraction from SEM images, align extracted contour to design, defect detection based on contour to design comparison, precise defective/nuisance pattern retrieval, confirmed defective/nuisance pattern overlay with inspection data, and modulation-related weak-pattern ranking for systematic pattern failure identification. The resulting workflow exhibits greater automation as well, from automatic defect detection and defective pattern retrieval, to various decision-making steps. Statistical summaries are also generated automatically. This degree of automation provides better quality reports and reduces the overall time-to-results, but the savings in time can be used another way – the savings can be used to increase the number of SEM images taken or to increase the inspection care areas on the wafer while maintaining the same time-to-results as the conventional approach.

In short, improved statistical summaries produce improved actionable information, and increased coverage leads to a more comprehensive assessment of the impact of each focus/exposure modulation and to an improved characterization of the impact of systematic patterning defects. Taken together, this methodology leads to a more comprehensive identification of weak patterns and a more accurate determination of the process window.

9778-84, Session PSWed

## Mixed-mode, high-order multi-patterning control strategy with small-spot, optical CD metrology on device structures

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As chip manufacturers aggressively push design rules, the need for more sophisticated means of controlling multi-patterning processes increases. Process equipment requirements are tightening to enable technology node transitions, while process integration and control mechanisms are becoming more sophisticated to drive final yield to maturity. Furthermore, with these strict process constraints, the challenge of maintaining a stable production baseline across process modules asks for more frequent and precise control [1].

An established means of enabling cross-module CD control includes after-etch dose correction feedback to state-of-the-art scanners, in order to control interfield and intrafield CD variation. Here, we show a novel means of controlling spacer-based multi-patterning space CD by feeding back to the scanner intrafield signatures after core etch, in combination with interfield signatures after final etch.

The ability to measure on-device structures further allows manufacturers to both save space in their overall chip design and secure direct device dimensions without the need to correlate measurements to "device-like" targets. Regular, repeating on-device patterns, such as those found in DRAM structures, can leverage scatterometry techniques for CD metrology if spot sizes are small enough to fit in the printed device areas.

By utilizing a high-NA full-azimuth angle-resolved scatterometry system to measure advanced DRAM post-etch multipatterning structures at core & final etches in conjunction with mixed mode correction capability, we demonstrate the ability to improve multipatterning pitch bias by >20% at high wafer sampling speeds. Additionally, we demonstrate the capability to measure small areas (below 12X12μm2), which allows for high-order intrafield & interfield sampling as well as on-device CD metrology for stable HVM monitoring and control.

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9778-85, Session PSWed

## Toward a laboratory CD-SAXS solution: An x-ray study

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CD-SAXS has been on the technology roadmap [1] for metrology for several years now, after pioneering work from Wen Li Wu and his group at NIST [2]. However a commercial solution is not available yet, greatly due to the lack of an adequate laboratory high brightness source [3, 4, 5] and due to the availability of optical scatterometry and CD SEM solutions at the 10nm node [6].

In this work, we report an X-ray feasibility study performed at the European synchrotron ESRF with a 20 micron diameter beam. The measurements were done in transmission geometry CD-SAXS on reference scatterometry pads (photoresist, SiO2, etc..) and in reflection geometry GISAX. The data collected at the synchrotron are used as a benchmark for the technique and for the robustness of the software algorithms.

Measurements times were in the range of sub seconds to few seconds, which would translate in few minutes on a laboratory type of instrumentation (depending on the materials).

Improvements of other relevant technologies for X-rays applications, beyond the X-ray source, can play also an important role in the realization of such laboratory instrument. Possible scenarios for a reference metrology solution at different stages of the manufacturing processes below 10 nm technology node will be discussed.

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9778-86, Session PSWed

## Overlay optimization for 1x node technology and beyond via rule-based sparse sampling

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Further downscaling of devices (14 nm technology and beyond) and increase in process complexity have demanded a strict control on overlay. The failure to apply such control generates overlay errors which lead to serious undesirable results such as critical dimension variation. The current state-of-the-art scanners are able to realize a 3nm overlay requirement by employing the most advanced models to correct linear as well as certain high-order intra- and inter-field overlay errors. In general, overlay modeling with more samples and fields will provide better model parameters. However, this improved overlay corrections comes at the expense of longer metrology time, which adversely affects the production. Compromising the trade-off between the correction accuracy and metrology time requires the optimization of the number of samples and its layout on the wafer. Optimized sampling scheme must be cost-effective and be able to detect the systematic and random components of overlay errors. In addition, due to the considerable number of data points of interest and process complexities, an automatic sampling is highly desirable. Here, we address these requirements by proposing an automated sparse sampling method that can detect the spatial variation of overlay errors as well as the overlay signature of the fields. Our technique satisfies the following three rules: (i) homogeneous distribution of ~200 samples across the wafer, (ii) equal number of samples in scan up and scan down condition and (3) equal number of sampling on each overlay marks per field. The implementation of these conditions will be discussed in the paper, along with some preliminary results.

9778-87, Session PSWed

## Monitoring CD-SEM performance using linewidth independent method

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The results of CD-SEMs change with time due to cathode degradation, system instability, and column contamination. The measured values of critical dimensions (CDs) directly depend on the performance of the SEM at the time of the measurement. Methods to confirm performance of CD-SEM are laborious and time consuming.

A linewidth independent method that is capable of quantitative extraction of SEM performance was developed. The method is independent from linewidth, LER, and LWR, and has high sensitivity. The software, Q-SEM, automatically evaluates image quality based on multiple factors. SEM images can include lines or contact holes; for contact holes, the Q-SEM additionally extracts the astigmatism of the electron beam.

Thousands of CD-SEM images were input into the software. Although Q-SEM does not measure linewidth, it was found that the results of the software correlate well with the variation of CD results arising from the CD-SEM performance. Moreover, modern CD-SEMs have very good repeatability; nonetheless, it was confirmed that the noise of Q-SEM is smaller than the linewidth variation from CD-SEM results.

Q-SEM allows the performance of CD-SEMs to be monitored and prompted for proper calibration and preventive maintenance. In addition, the software has the capability for real time monitoring of CD-SEM results, showing red flags when CD results go out of range due to tool issues. When this happens in production, the reason for CD jump should be established - either it is on the scanner/process side, or it is a metrology problem. Q-SEM helps to resolve this dispute instantaneously.

9778-89, Session PSWed

## Quantitatively measuring nanomechanical, time-varying interaction forces in atomic force microscope imaging

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Atomic Force Microscope (AFM) has already proven itself as a versatile tool for R&D in semiconductor industrial applications and leading the nanotechnology to new applications like, high throughput defect inspection, high resolution metrology or high resolution defect review. AFM uses a sharp tip attached to the free end of a cantilever to sense the sample surface and obtain the map of morphological, mechanical, electrical or thermal properties of the sample surface. AFM can image the sample surface in various operation modes, such as contact mode, tapping mode or non-contact mode. Among them, Tapping Mode AFM (TM AFM) is known as the most preferred operation mode for sensitive and fragile samples because of its small shear forces and short contact time. During imaging in TM, the cantilever oscillates around its fundamental frequency (lowest resonance frequency) and tip periodically approaches, interacts and retracts from the sample surface and experiences both long range attractive forces and short range repulsive forces. According to theoretical analysis, tip sample interaction forces in TM AFM are periodic impulse like functions with a periodicity equal to the oscillation frequency. Amplitude and phase of the cantilever oscillation are the only observables and impulse like forces cannot be extracted from the sinusoidal amplitude signal or phase. Forces applied on the sample surface during imaging in TM has been studied for especially designed probes, such as micromachined membrane with an integrated displacement sensor, torsional harmonic cantilever and cantilever with interferometric force sensor but an experimental proof for commercial

cantilevers is still missing.

In this talk, we introduce a new method (patent pending) which can be used for measuring the nanomechanical, time-varying forces applied on the sample surface during imaging in TM AFM. This method is using a resilient element as a sample surface which deflects with respect to the applied force so that the tapping forces are being measured directly from the sample surface which provides opportunity to use all types of commercial or special design cantilevers. An optical beam deflection method is used for monitoring the deflection of the sensor and a special calibration procedure is applied to convert the deflection of the sensor into force.

The experimental results to be presented are quite promising for the future applications of the system. We envision using this setup for calibrating the tapping forces with respect to excitation frequency and oscillation amplitude to predetermine the applied force on the sample surface. One of the most important motivations is to calculate the true height of the surface structures because the surface structures are being compressed due to the tapping forces. The true height of the surface structures can be calculated using the forces applied and the mechanical properties of the surface material. Moreover, AFM is being used as metrology and inspection tool of sensitive and fragile samples like semiconductor or biological samples, which requires precise control on the tapping forces to prevent damage on the sample surface. The system also provides opportunity to simulate different surface structures or scenarios such as steep step so that the change in the tapping forces during imaging different surface structures with different imaging parameters can be simulated.

9778-91, Session PSWed

## Overlay metrology performance prediction fidelity: the factors which enable a successful target design cycle

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The purpose of this work is to demonstrate 3 key factors which enable consistency in ranking between simulated and measured metrology performance for target design. As previously reported , the first factor to enable high fidelity simulations for the purpose of target design is stack and topography verification of model inputs. In this publication we will report in detail the best known film metrology methods required to achieve model integrity. The second factor is the method of calculation of metrology performance metrics based on target cell reflectivities calculated by RCWA (Rigorous Coupled Wave Analysis). The two main metrics that are computed are "Diffraction Efficiency" (DE), and "Sensitivity to Overlay" (SE). These target design performance metrics enable ranking of different designs, and subsequent choice of the best performing designs among all simulated design options, the ranking methodology being the third factor.

We have applied the above steps to a specific stack, where five different designs have been considered. A good agreement between simulation and measurement has been demonstrated when comparing the performance metrics. A further result that demonstrated the capability to achieve the subsequent ranking step has been a successful "blind test" in which the ranking of each one of the five target designs has been compared with the metrology results for the unmarked printed designs measured on the wafer.

9778-92, Session PSWed

## Advanced cverlay sampling and modeling for optimized run-to-run control

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In recent years overlay (OVL) control schemes have become more complicated in order to meet the ever shrinking margins of advanced technology nodes. As a result, this brings up new challenges to be addressed for effective run-to-run OVL control. This work addresses two of these challenges by new advanced analysis techniques: (1) sampling optimization for run-to-run control and (2) bias-variance tradeoff in modeling.

The first challenge in a high order OVL control strategy is to optimize the number of measurements and the locations on the wafer, so that the "sample plan" of measurements provides high quality information about the OVL signature on the wafer with acceptable metrology throughput. We solve this tradeoff between accuracy and throughput by using a smart sampling scheme which utilizes various design-based and data-based metrics to increase model accuracy and reduce model uncertainty while avoiding wafer to wafer and within wafer measurement noise caused by metrology, scanner or process. This sort of sampling scheme, combined with an advanced field by field extrapolated modeling algorithm helps to maximize model stability and minimize on product overlay (OPO).

Second, the use of higher order overlay models means more degrees of freedom, which enables increased capability to correct for complicated overlay signatures, but also increases sensitivity to process or metrology induced noise. This is also known as the bias-variance trade-off. A high order model that minimizes the bias between the modeled and raw overlay signature on a single wafer will also have a higher variation from wafer to wafer or lot to lot, that is unless an advanced modeling approach is used. In this paper, we characterize the bias-variance trade off to find the optimal scheme.

The sampling and modeling solutions proposed in this study are validated by advanced process control (APC) simulations to estimate run-to-run performance, lot-to-lot and wafer-to-wafer model term monitoring to estimate stability and ultimately high volume manufacturing tests to monitor OPO by densely measured OVL data.

9778-93, Session PSWed

## Probe microscopy for metrology of next-generation devices

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As device geometries shrink and the number of transistors on the wafer grows, new metrology solutions are required to support the development and production of next generation structures for the 10 nm node and beyond. The capabilities of the atomic force microscope (AFM) to provide non-destructive high resolution sub-nm information in all 3 dimensions are well suited to support these requirements. However, the adoption of AFM for high volume manufacturing (HVM) has been limited by its lack of suitability to the production environment due to fragility and dimensions of the probe, limited speed of operation and lack of automation.

In this paper, a novel probe microscope will be presented called the Rapid Probe Microscope (RPM) which addresses these limitations of the AFM. The RPM is a platform supporting new imaging modes which are optimised for profiling narrow high aspect ratio structures as found in semiconductor devices. A conventional AFM measures and maintains a constant interaction between the tip of the probe and surface of the sample by adjusting the separation between the probe and sample using a feedback loop. This is very powerful and versatile methodology; however, it is not well suited to imaging structures with abrupt changes in surface topography. In contrast to a conventional AFM, the presented RPM operates by periodically moving the tip towards and away from the surface. Each cycle of moving the probe towards and away from the surface corresponds to a single height measurement which is used to construct one pixel of the image. Between

each cycle, and thus between each pixel of the image, the tip is completely removed from proximity with the surface.

The capabilities of the RPM will be demonstrated by providing measurements on structures with features sizes equivalent to 10 nm node devices and beyond. Additionally, the presented RPM system can operate with high throughput, long maintenance intervals and in both ambient and vacuum environments enabling in-situ hybrid metrology solutions, for example operating alongside a CD or defect review SEM.

9778-94, Session PSWed

## Improving scanner wafer alignment performance using mark optimization

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In the process nodes of 10nm and below, the patterning complexity along with the processing and materials required has resulted in a need to optimize alignment targets in order to achieve the required precision, accuracy and throughput performance. Recent industry publications on the metrology target optimization process have shown a move from the expensive and time consuming empirical methodologies, towards a faster computational approach.

ASML's Design for Control (D4C) application, which is currently used to optimize YieldStar Diffraction Based Overlay (DBO) metrology targets, has been extended to support the optimization of scanner wafer alignment targets. This allows the necessary process information and design methodology, used for DBO target designs, to be leveraged for the optimization of alignment targets.

In this paper, we show how we applied this computational approach to wafer alignment target design. We verify the correlation between predictions and measurements for the key alignment performance metrics and finally show the potential alignment and overlay performance improvements that an optimized alignment target could achieve.

9778-95, Session PSWed

## New approaches in diffraction based optical metrology

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Requirements for on-product overlay, focus and CD uniformity continue to tighten in order to support the demands of 10nm and 7nm nodes. This results in the need for simultaneously accurate, robust and dense metrology data as input for closed-loop control solutions, thereby enabling wafer-level control and high order corrections.

In addition the use of opaque materials and stringent design rules drive the expansion of the available wavelength and target design parameter space.

Diffraction-based optical metrology has been established as the leading methodology for integrated and standalone optical metrology, enabling overlay, focus and CD monitoring and control in state of the art chip manufacturing.

We are presenting the new approaches to diffraction based optical metrology designed to meet the ≤10nm node challenges. These approaches have been implemented in the latest addition to the YieldStar metrology platform, the YS350E, introducing a new way of acquiring and processing diffraction-based metrology signals.

In this paper, we will present the new detection principle and its impact on key performance characteristics of overlay and focus measurements. We will also describe the wide range of applications of a newly introduced increased measurement spot size, enabling significant improvements to accuracy and process robustness of overlay and focus measurements.

With the YS350E, the optical CD measurement capability is also extended to 10x10μm2 targets. We will discuss the performance and value of small targets in after-develop and after-etch applications.

9778-96, Session PSWed

## Process window optimizer for pattern-based defect prediction on 28nm metal layer

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At 28nm technology node and below, hot spot prediction and process window control across production wafers have become increasingly critical to prevent hotspots from becoming yield limiting defects. Traditional computational lithography applications are effective in eliminating major layout related issues before a mask is made, but are not usually directed towards predicting on-wafer performance, largely due to unavailability of detailed data on actual process variations before tape-out.

ASML has introduced a new concept, process window optimizer (PWO) for hotspot detection, defect prediction, process window monitoring and control [Ref.1], which identifies, ranks and characterizes process window limiters (hotspots) and their detailed process window performance. PWO then combines this information with scanner focus data, mask metrology and wafer topography data. Using this flow we demonstrate prediction and verification of defect probabilities on wafer that arise from topography variations approaching or exceeding focus margins of device hotspots.

Proof of concept has been demonstrated on a full-field product layout in STMicroelectronics and a metal layer production process at 28nm technology. After etch hotspots that arise from resist profile variations are identified by resist-profile aware simulations using ASML's R3D (resist 3D) model [Ref.2], and further qualified by CD-SEM verification using contour analysis for complex logic patterns. Focus variations are characterized by determining a systematic fingerprint that can be combined with per-wafer topography data into dense focus maps to determine if and where across a production wafer focus-sensitive hotspots may turn into device defects.

Further work in the project will investigate the influence of additional process parameters, in particular correlation of dose sensitive hotspots or defects with effective dose wafer maps. We will also apply the PWO flow in monitoring mode to device in production in order to correlate results with yield data that will be available in STMicroelectronics.

9778-97, Session PSWed

## Studying post-etching silicon crystal defects on 300mm wafer by automatic defect review AFM

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Single crystal silicon wafers are the fundamental elements of semiconductor

manufacturing industry. The wafers produced by Czochralski (CZ) process are very high quality single crystalline materials with known defects that are formed during the crystal growth or modified by further processing. While defects can be unfavorable for yield for some manufactured electrical devices, a group of defects like oxide precipitates can have both positive and negative impacts on the final device. The spatial distribution of these defects may be found by scattering techniques. However, due to limitations of scattering (i.e. light wavelength), many crystal defects are either poorly classified or not detected. Therefore a high throughput and accurate characterization of their shape and dimension is essential for reviewing the defects and proper classification. While scanning electron microscopy (SEM) can provide high resolution two-dimensional images, atomic force microscopy (AFM) is essential for obtaining three-dimensional information of the defects of interest (DOI) as it is known to provide the highest vertical resolution among all techniques. [1] However AFM's low throughput, limited tip life, and laborious efforts for locating the DOI have been the limitations of this technique for defect review for 300 mm wafers. To address these limitations of AFM, automatic defect review AFM has been introduced recently [2], and is utilized in this work for studying DOI on 300 mm silicon wafer. In this work, we carefully etched a 300 mm silicon wafer with a gaseous acid in a reducing atmosphere at a temperature and for a sufficient duration to grow the crystal defects to a size capable of being detected as light scattering defects. The etched defects form a shallow cone structure and are inspected by laser light scattering (LLS). However, several groups of defects couldn't be properly sized by the LLS due to the very shallow depth. For the same reason, SEM cannot be used effectively for post-inspection defect review and classification of these types of defects. To obtain accurate shape and three-dimensional information of those defects and verification of defects, automatic defect review AFM (ADR AFM) is utilized for accurate locating and imaging of DOI. In ADR AFM, non-contact mode imaging is used for non-destructive characterization and preserving tip sharpness for data repeatability and reproducibility. Locating DOI and imaging are performed automatically with a throughput of several defects per hour. Topography images of DOI has been collected and compared with SEM images. The ADR AFM has been shown as a non-destructive metrology tool for defect review and obtaining three-dimensional topography information.

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9778-98, Session PSWed

## Comparison study of diffraction-based overlay and image-based overlay measurements on programmed overlay errors

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Overlay (OVL) control is one of the main challenges in lithography for the advanced technology node like 14nm and beyond. Diffraction based Overlay (DBO) and Image Based Overlay (IBO) are two main OVL techniques in the advanced semiconductor manufacturing. In this paper we will present the comparison study of these two methods on programmed errors of critical layers of 14nm technology node. Programmed OVL errors were made on certain fields during the exposure. Full coverage OVL measurements were performed using both IBO and DBO. Linear, interfiled high order process correction (HOPC) and intra-field high order process correction (iHOPC) modeling has been done from non-programmed fields. Then modeling has been subtracted from these certain programmed fields, and Reticle contribution was also calculated and subtracted. In this way we compared the accuracy and distribution of the measurement results on such programmed OVL errors of both techniques, providing guidelines for the best implementation of each technology. In this study, metrology measurement accuracy and stability can be feasible and more accurate OVL control is enabled by selecting better OVL measurement techniques. We are also showing that this technique can be also used for a metric of metrology recipe parameter optimization for both DBO and IBO.

9778-99, Session PSWed

## Metrology target design (MTD) solution for diagonally orientated DRAM layer

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The semiconductor industry has been successfully moving toward increasing the number of transistors on integrated circuits for more than four decades. However, the pace of advancement has slowed, starting at the 20nm node due to the challenges of improving resolution of lithography systems while precisely controlling the overlay between layers. One of the challenges in optical lithography is to improve image quality by manipulating the optical wavefront exiting the projection lens which requires advanced resolution enhancement techniques (RET) including (1) optical proximity correction (OPC) to manipulate the mask pattern shape, (2) source optimization to adjust the illumination of the mask, (3) phase shifting mask (PSM) to improve normalized image log-slope (NILS), and (4) multiple exposures. Such degrees of freedom can lead to impressive successes in shrinking device dimensions in semiconductor manufacturing.

On the other hand, relying on advanced RETs can generate several serious issues, potentially damaging the accuracy of overlay metrology. (1) Although there are no aberration-free imaging optics, lithography projection systems are comprised of at least three dozen lens elements to minimize aberrations. Nonetheless, using an extreme dipole or an optimized illuminator can significantly increase the pattern placement error (PPE) sensitivity to existing scanner aberrations, causing varying biases between the overlay target and actual device for each layer, which may seriously impact device performance, especially for multiple patterning layers (2). Another issue is achieving device process windows. Specifically, the inverse proportionality to the square of NA in depth of focus is a major challenge. In order to solve the above mentioned issues, device-like overlay targets as well as in-die and on-die measurements are emerging as industry requirements (3). However, due to opacity of many hardmask layers at short wavelengths, overlay metrology still relies on coarse pitches significantly larger than device pitches; simply making device-like segmentation may not completely solve all issues. In both exposures of the pattern, resist profile degradation (i.e. different CD and PPE bias) is exacerbated by focus variation under the inevitable situation of existing high aberration sensitivity and limited PW. Figure 1 shows an example of a lithography-aware optimal target design, providing the maximized target process window as shown in Figure 2, while maintaining good metrology performance in terms of its precision and diffraction efficiency.

In the conference, we will present a novel framework using exit pupil wavefront analysis together with Zernike sensitivity analysis (ZSA) based on a Monte-Carlo technique which enables the design of robust metrology targets that maximize target PW while minimizing placement error discrepancies with device features in the presence of spatial and temporal variation of the aberration characteristics of the exposure tool. Knowing the limitations of lithography systems, design constraints, and detailed lithography information including illumination, mask type, etc., one can successfully design an optimal target. We have validated our new metrology target design (MTD) method for one of the challenging DRAM active layers consisting of diagonal line and space patterns illuminated by a rotated extreme dipole source. We find that an optimal MTD target gives maximized

PW and strong device correlation, resulting in dramatic improvement of overall overlay performance.

9778-100, Session PSWed

## Electrostatic risks to reticles and damage prevention methodology

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In recent years many new products have been developed to try and reduce the reticle ESD damage problem. These are almost all based on the standardized principles developed for the protection of ESD sensitive electronic devices, but reticles are not the same as electronic devices. Reticles are predominantly damaged by electric field rather than the conductive transfer of static charge, and the physical mechanisms that damage reticles are different from those that damage electronic devices. This paper explains why some of the established methods for ESD prevention are not the best way to protect reticles against damage and in some cases actually increase the risk of reticle damage. Measurements are presented showing that, contrary to the widely held opinion and current practice in semiconductor manufacturing, static dissipative plastic is not the best material to use for the construction of reticle pods. An appropriate combination of insulating material and metallic shielding is shown to provide the best electrostatic protection for reticles.

9778-101, Session PSWed

## Investigation on the relationship between CD and CDU in memory devices

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As pattern design rule of device shrinks, CD control becomes more critical and important especially for resistance devices.

As CD (Critical Dimension) increases, CDU (Critical Dimension Uniformity) becomes worse generally. The question with this relationship is a starting point of our study. Mainly we focused on two points. One is which factor affects CDU. The other is whether CDU degradation with large CD happens at all cases or not.

We have analyzed with simulation and experiment results about CDU with splitted mask layout CD under limited conditions such as same equipment, illumination and exposure dose.

As a result, we will show the relationship between CD size and CDU.

9778-102, Session PSWed

## Triple IBO evaluation and application on advanced node

En Chuan Lio, Gary Wang, United Microelectronics Corp. (Taiwan)

Triple AIM evaluation and application on advanced node

A novel method on advanced node for overlay data extraction accuracy is demonstrated, and here we have special design in triple-AIM(Advanced Imaging Metrology) to realize the approach.

Since triple AIM exist 3 layers space for marks insertion, we plan a design previous layers, assumed layer A and layer B, as inserting 2 marks locations by once pattering, and the 2 marks group(pair) with/or without a predetermined overlay offset through original mask database design.

And then, as following current layer, assumed layer C, patterning process complete, full triple-AIM patterns is generated, and 3 sets of overlay data could be obtained, A to B, C to B, C to A. If we calculate the overlay of current to previous layers by averaging [C to B] and [C to A], then we could have a more confident raw data for exact site, since the local marks variation could be minimized through the raw data averaging procedure. And from raw data [A to B], we could have a filtration to purify the raw data, which finally will be input into scanner parameter generation by algorithm analysis. That potentially could make the APC control system more stable.

9778-103, Session PSWed

## Applications of on-product diffraction-based focus metrology in logic high-volume manufacturing

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The integration of on-product diffraction-based focus (DBF) capability into the majority of immersion lithography layers in leading edge logic manufacturing has enabled new applications targeted towards improving cycle time and yield. Three main applications are:

1. Scanner focus excursion detection

2. Focus targeting for a given layer across the full production scanner fleet

3. Per-exposure focus feedback corrections

For the first application, a CD-based detection method is the process of record (POR). The drawback of this method is increased cycle time and limited sampling due to CD-SEM metrology capacity constraints. The new DBF-based method allows the addition of focus metrology samples to the existing overlay measurements on the integrated metrology (IM) system. The result enables the addition of measured focus to the SPC system, allowing for a cycle time neutral excursion detection method.

For the second application, the current method involves re-targeting of focus using a dedicated focus-exposure matrix (FEM) on all scanners intended to run the layer in question. This is a CD-SEM metrology-heavy method, and analysis of the data requires human judgment of specific patterns to determine final best focus, resulting in lengthy analysis times as well as a significant uncertainty in the final best focus number. The new diffraction-based focus method allows the measurement to occur on the IM system, on a regular production wafer, at the same time as the exposure. The measured focus can then directly be referenced to the best focus of the scanner on which the layer was initially qualified, removing the need for offline analysis. This results in a cycle time gain as well as a less subjective determination of best focus.

The third application aims to use the novel on-product focus metrology data in order to apply per-exposure focus corrections to the scanner in order to fine-tune product yield. These corrections are particularly effective at the edge of the wafer, where systematic layer-dependent effects such as roll-off or level sensor process dependency can be removed using DBF-based scanner feedback.

This paper will discuss the development of a methodology to accomplish each of these applications in a high-volume production environment. The new focus metrology method, sampling schemes, feedback mechanisms and analysis methods lead to improved focus control, as well as earlier detection of failures.

9778-104, Session PSWed

## Study of correlation between overlay and displacement measured by coherent gradient sensing (CGS) interferometry

Jeffrey Mileham, Doug Anberg, David M. Owen, Byoung-

**Conference 9778: Metrology, Inspection, and Process Control for Microlithography XXX**

Ho Lee, Eric Bouche, Ultratech, Inc. (United States); Yasushi Tanaka, Toshiba Corp. (Japan)

Within all device patterning processes, lithography is one of the most critical. In order to realize high device performance, semiconductor technology is approaching the 10 nm design rule, which requires progressively smaller overlay budgets. Simultaneously, structures are expanding in the 3rd dimension with many lithographic layers, thereby increasing the potential for inter-layer distortion. For these reasons, device patterning is becoming increasingly difficult as the portion of the overlay budget attributed to process-induced variation increases. After lithography, overlay gives valuable feedback to the lithography tool; however overlay measurements are very limited in number due to throughput considerations. Moreover, since overlay is measured after lithography, it can only react to, but not predict the process-induced overlay.

This study is a joint investigation in a high-volume manufacturing environment of the portion of overlay associated with displacement induced by many processes (i.e., etch, CMP, anneal, deposition). Displacement measurements are measured by Coherent Gradient Sensing (CGS) interferometry, which generates high-density displacement maps (>3 million points on a 300 mm wafer) such that the stresses induced die-by-die and process-by-process can be tracked in detail. The results indicate the relationship between displacement and overlay shows the ability to forecast overlay values before the lithographic process.

9778-105, Session PSWed

## Topological study of nanomaterials using surface-enhanced ellipsometric contrast microscopy (SEEC)

Sylvain G. Muckenhirn, Iris Versicolor Corp. (United States)

Surface-Enhanced Ellipsometric Contrast Microscopy (SEEC) allows live wide field optical imaging techniques with sub-nanometer level Z resolution. SEEC is applicable to observations realized in air/dry and liquid/wet environments in reflected optical systems (upright or inverted).

We will explore principle, constraints, advantages and limits of the technique. As a result of research on contrast enhancement, SEEC sensors maintained initial polarization of light during reflection allowing blocking of any undisturbed light before the detector. Thus only light whose polarization is disturbed by a sample is reaching the detector, allowing for an increased signal to noise ratio.

The technique implies a major constraint: the need for the user to perform characterization using the SEEC sensor. the SEEC sensor is a silicon based multi layer based available from wafer shape down to small samples sizes. The sensor in effect often replaced slides in fields like life sciences.

The technique also has a limitation: samples must be transparent to light.

We will present results obtained on nano-materials and nano-objects demonstrating sub-nanometer Z visualization and measurements, as well as sub-optical resolution X and Y detection.

We will discuss applications with example of thin film characterization down to 1nm thickness (HMDS, Liquid crystal, adhesive residues, graphene damages induced by Raman spectroscopy, nanopatterning thickness variations, AFM induced damages on liquid display layers...), as well as examples of live monitoring of evolution of co-polymer versus temperature.

We will present visualization of nanowires, carbon nanotubes, gold dots and to illustrate limits 1.2nm DNA strands.

We will present thickness measurements with repeatability better than 0.2nm (30 measurements, ISO17025, PTB certification).

We will suggest other potential applications.

9778-106, Session PSWed

## Controlling bridging and pinching with pixel-based mask for inverse lithography

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Inverse Lithography Technology (ILT) has become a viable computational lithography candidate in recent years as it can produce mask output that result in process latitude and CD control in the fab which is hard to match with conventional OPC/SRAF insertion approaches.

An approach of solving the inverse lithography problem as nonlinear, constrained minizimation problem over a domain mask pixels was suggested in the paper by Yu. Granik ``Fast pixel-based mask optimization for inverse lithography'' in 2006. The present paper extends this method to satisfy bridging and pinching constraints imposed on print contours.

Namely, there are suggested objective functions expressing penalty for constraint violations and their minimization with gradient descent methods is considered. This approach has been tested with ILT-based Local Printability Enhancement (LPE) tool in an automated flow to eliminate hot spots that can be present on the full chip after conventional SRAF placement/OPC, and has been applied in 14nm, 10nm node production, single and multiple-patterning flows.

9778-108, Session PSWed

## An evaluation of edge roll off on 28nm FDSOI (fully depleted silicon on insulator) product

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For 28nm FDSOI product wafers, scanner focus is better controlled at the wafer center than at the wafer edge. This is due, in a large part, to edge roll off effects. Edge roll off is the average height per per raduis measured by the scanner level sensor. Log files, generated by every wafer exposed, make it possible to use the scanner as an in-line metrology tool for monitoring edge roll off.

Reduced focus control can lead to yield loss or killer defects on the wafer. In order to quantify the impact of edge roll off and to verify the validity of using it as a metric this paper correlates it to scanner leveling non-corectable errors. On-product effects are then compared to these results.

The main contributors are evaluated, including processing, lot to lot variation, within lot variation, wafer substrate vendor and chuck to chuck effects. Then the root cause and mitigation methods are presented a NXT:1950 scanner.

9778-109, Session PSWed

## EUV blank defect and particle inspection with high-throughput immersion AFM with 1nm 3D resolution

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Inspection of EUV mask substrates and blanks is a demanding inspection application as typically a full surface area of 152 x 152 mm needs to be inspected at 1 nm resolution. Currently this is performed in two stages, first by e-beam inspection to detect defects and subsequently by atomic force microscopy (AFM) on the defect locations for detailed characterization and review. Based on our experience with high throughput parallel AFM we here propose to do a full surface characterization of EUV mask substrates

with AFM, removing one processing step and enabling full 3D sub 1 nm resolution over the entire surface. This will require speeding up our existing high throughput AFM solution substantially. For surfaces such as EUV mask substrates which are extremely flat, control bandwidth of the AFM (to follow the surface topography) is not a limiting factor, and consequently specifications for mechanical performance are also easily met. The only limiting factor to enable this application is in the sensor itself: the limiting factor for throughput is the time that the cantilever needs to adjust its oscillation amplitude to the surface topography while scanning.

The response time of the cantilever for changes in amplitude due to variations in topography is ?=Q/(ϖ*f0), where Q is the quality factor (related to damping of the cantilever system) and f0 is the cantilevers resonance frequency. From our measurements we see that the cantilevers response is indeed the limiting factor for throughput in our instrument. There are two ways to increase response speed: we can raise the resonance frequency and we can lower Q, equivalent to increasing damping. Raising the resonance frequency is limited by both the readout method (optical beam deflection) and the requirement to have a tip at the end of the cantilever. Damping can be increased however. To increase damping, we propose to encase the cantilever and fill the encasing with liquid. Liquid increases damping by a factor of about 100 for water or even more for other liquids. This method is relatively simple and is compatible with ultra clean requirements for inspection of critical substrates. By increasing damping by a factor of over one hundred and using a cantilever with a resonance in the MHz range we can reach a measurement bandwidth which allows us to scan a 152 x 152 mm substrate with 1nm resolution in 1.5e9 seconds or 17.000 days using one AFM cantilever. Employing a parallel AFM concept we envision to use up to 10.000 cantilevers in parallel for a throughput of one substrate per 2 days. If the resolution requirements are relaxed a bit the throughput can even become just a few hours.

9778-110, Session PSWed

## Dedication break-up for semi-critical layers to enable efficient product ramp

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In leading-edge lithography processes, the most advanced exposure tool types are used to expose the most critical layers. This is necessary to be able to have sufficient CD control for critical features. In order to satisfy tight overlay budgets, subsequent layers are exposed on the same tool. For stability and logistical simplicity during development phase, all critical and semi-critical layers are exposed on the same tool. During product ramp, it becomes more cost effective to break up this single-tool dedication where possible, so that older tool generations can be used for less critical layers. In addition to potentially worse single machine performance of the older tool, there is a matched machine overlay penalty on the overlay budget. Therefore the impact on the overlay budget must be analyzed to prevent yield loss.

In this feasibility study, we focus on a number of different layers that are divided in three different categories. In the first category are the most critical layers, so that dedication break-up is not possible. In the second category are semi-critical layers with significant non-litho process influences. Because of these process influences, there is not much room in the overlay budget, so the matched machine impact must be minimized. Therefore, these layers are exposed on tools that are only one generation older. In the third category are semi-critical layers that have little process effects, allowing older generation exposure tools. The analysis focuses on the layers in the second and third category.

In our analysis, we use different zones near the wafer edge because process effects as well as matched machine overlay effects typically have the most severe impact at the wafer edge. This analysis by zone allows us to get a very detailed insight into the overlay impact of switching from single-machine to matched-machine exposure. In addition, we compare the impact to non-correctable intra-field errors, but found that this is not a primary factor in the overlay budget. We compare the performance at different layers and for different exposure tool types to estimate the effect on high volume production.

In addition to high order process corrections, intra-field higher order process corrections and Baseliner corrections, the improvement potential of different CPE correction models is evaluated that are applicable for different exposure tool generations. The older tool generations have less correction capabilities in the CPE. To improve the matched machine overlay performance on the older tools, we evaluated applying the reverse corrections needed for the matching penalty on the newer tools, using the latest correction possibilities in the CPE This means that the first layers that are exposed on the newest generation tools are deliberately tuned to the grid and intra-field performance of the older generation tools.

9778-111, Session PSWed

## Process tool monitoring and matching using interferometry technique

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The semiconductor industry makes dramatic device technology changes over short time periods. Semiconductor devices are heading for 10nm design rule while device functionality and capability has requested much better than previous generation, which has required precise management and control of processing tools. Some processes require multiple tool sets and some tools have multiple chambers for mass production. Tool and chamber matching has become a critical consideration for meeting today's manufacturing requirements. Additionally, process tools and chamber conditions have to be monitored to ensure uniform process performance across the tool and chamber fleet. There are many parameters for managing and monitoring tools and chambers. Particle defect monitoring is a well-known and established example where defect inspection tools can directly detect particles on the wafer surface. However, leading edge processes are driving the need to also monitor invisible defects, i.e. stress, contamination, etc., because some device failures can not be directly correlated with traditional visualized defect maps or other known sources. Some failure maps show the same signatures as stress or contamination maps, which implies correlation to device performance or yield.

In this paper we present process tool monitoring and matching using an interferometry technique. There are many types of interferometry techniques used for various process monitoring applications. We use a Coherent Gradient Sensing (CGS) interferometer which is self-referencing and enables high throughput measurements. Using this technique, we can quickly measure the topography of an entire wafer surface and obtain stress and displacement data from the topography measurement. For improved tool and chamber matching and reduced device failure, wafer stress measurements can be implemented as a regular tool or chamber monitoring test for either unpatterned or patterned wafers as a good criteria for improved process stability.

9778-112, Session PSWed

## Reducing overlay sampling for APC-based correction per exposure by replacing measured data with computational prediction

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One of the keys to successful mass production of sub-20nm nodes in the semiconductor industry is the development of an overlay correction strategy

that can meet specifications, reduce dedicated chuck overlay (DCO), and minimize measurement time. Three important aspects of this strategy are: correction per exposure (CPE), integrated metrology (IM), and the prioritization of automated correction over manual subrecipes.

The first and third aspects are accomplished through an APC system that uses measurements from production lots to generate CPE corrections that are dynamically applied to future lots. The drawback of this method is that production overlay sampling must be extremely high in order to provide the system with enough data to generate CPE. That drawback makes IM particularly difficult because of the throughput impact that can be created on expensive bottleneck photolithography process tools.

The goal is to realize the cycle time and feedback benefits of IM coupled with the enhanced overlay correction capability of automated CPE without impacting process tool throughput. This paper will discuss the development of a system that sends measured data with reduced sampling via a sample scheme optimization (SSO) layout to the exposure tool's computational modelling platform to predict and create "upsampled" overlay data in a customizable output layout that is compatible with the fab customer CPE APC system.

The new system, called Single Wire, was implemented through software patches applied to overlay metrology tools and upgrades to the computational modeling software. Sparsely-sampled raw data is sent from the metrology tool to the computational system for modeling to mimic a customer-specific measurement layout and the upsampled data is sent back to the metrology tool (Fig. 1). The customer overlay computation module (OCM) software was also modified to accept the upsampled data from the metrology tool for use in APC CPE correction. The result is dynamic CPE without the burden of extensive measurement time, which leads to increased utilization of IM.

9778-113, Session PSWed

## Overlay metrology method in nanoscale semiconductor devices using an image processing technique

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As semiconductor processing becomes more complicated and pattern sizes shrink, the overlay metrology has become one of the most important issues in the semiconductor industry. Therefore, in order to obtain correct, reliable overlay values in semiconductor fabrication facilities (fab), quantization methods for the efficient management and implementation of a measurement algorithm are required, as well as an understanding of the target structures in the semiconductor device. We implemented correct, reliable overlay values in the pattern using the image processing method. The quantization method, through correlation analysis and a new algorithm for target structures, were able to improve the sensitivity to misalignment in the pattern and enable more stable and credible in-line measurement by decreasing the distribution of the residuals in overlay values. Since overlay values of the pattern in the fab were measured and managed more reliably and quickly, it is expected that our study will be able to contribute to the yield enhancement of semiconductor companies.

9778-114, Session PSWed

## Automated klarf-based defect inspection by electron-beam inspection tool: a novel approach to inline monitoring and/or process change validation

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Electron-beam (E-beam) inspection is of broad technological and fundamental interest owning to its outstanding detection capability of a wide range of inline defects in many advanced technology nodes such as device leakage, open contact and tiny physical defects. With the shrinking dimensions, tightening process tolerances and enlarged aspect ratio of semiconductor devices, e-beam inspection has been becoming a promising toolset for learning curve acceleration, yield improvement and process monitoring. However, its role is challenged due to lower throughput, smaller scan area and less die sampling. Generally, the overall in-line defect inspection flow is subdivided into two main streams: one is optical inspection coupling with sampled scanning electron microscopy (SEM) review and other is e-beam inspection. Optical – SEM inspection suffers its limited number of review defects due to constraint cycle time while low throughput is bottleneck of sole e-beam inspection. With the aim of developing an alternative high throughput methodology of in-line e-beam inspection, we report an optical inspection guided e-beam inspection method for inline monitoring and/or process change validation. We illustrate its advantage through the case of detection of buried voids/unlanding vias, which are identified as yield-limiting defects as causing electrical connectivity failures. The problem cause by buried voids/unlanding vias is its high interconnect resistance due to the vacancy of copper atoms which degrades device performance or even makes device failure. The voids tend to move along electrical current flows, which leads to potential device reliability issue. The migrating voids localize to a necking point pushing away the remaining copper which disconnects circuit. In this context, we inspected a back end of line (BEOL) wafer after the copper electro plating and chemical mechanical planarization (CMP) process with bright field inspection (BFI) and employed EBI to inspect full wafer with guidance of BFI klarf file. Voltage contrast (VC) mode was selected to detect dark VC defects in this case. When primary electron beam strikes a voided structure, the electrical path from wafer surface to substrate is isolated. As a result, the local electron yield on the defective structure is less due to the lack of supplemental electrons from substrate. By using this mode, the dark VC defects which are suspected voids are well identified and classified by using EBI superior resolution patch images. An impressive throughput of few hundreds defects per minute is archived on EBI tool compared with conventional SEM review of few hundreds defects per hour. The DVC defects were confirmed as buried voids by transmission electron microscopy (TEM). Such a complementary methodology benefiting from both high throughput BFI and EBI for expanded defect sampling rate and reasonable overall throughput has been rarely discussed but is crucial for inline defect detecting and monitoring in high volume semiconductor manufacturing foundry, especially for advanced sub-20nm technology nodes.

9778-115, Session PSWed

## Sub-20nm particle inspection on EUV mask blanks

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The Rapid Nano is a particle inspection system developed by TNO for the qualification of EUV reticle handling equipment [1]. The detection principle of this system is dark-field microscopy. The performance of the system has been improved via model-based design. Through our model of the scattering process we identified two key components to improving the inspection sensitivity [2]. The first component is to illuminate the substrate from multiple azimuth angles. This illumination mode averages out the variance in the background scattering, allowing for a lower detection threshold to be used. Two years ago, this illumination mode was implemented in our existing inspection system [3].

The second component to improve the sensitivity is to decrease the wavelength of illumination. A shorter wavelength increases the total scattering and reduces the background scattering relative to the defect signal. A new Rapid Nano inspection system (RN4) will be completed in the beginning of 2016, which combines the multi-azimuth illumination mode

with a 193 nm source. This system will have a sub 20 nm LSE sensitivity, in-line with the requirements of the ITRS roadmap for defects on EUV masks (Figure 1). Model predictions and measured results are shown in Table 1.

The Rapid Nano inspection system makes use of dark-field imaging, in which an area of a substrate is imaged on a camera (Figure 2). Previous generations of the Rapid Nano system made use of commercially available optics for the imaging step. In the DUV wavelength regime diffraction limited imaging over a large field is more challenging and suitable optics were not available off-the-shelf. Therefore TNO designed and fabricated an objective lens specifically for the Rapid Nano 4 inspection system.

Other challenges in changing the illumination to the DUV include handling the high peak power of the pulsed laser source and the lifetime of the optics. The design of the Rapid Nano 4 and first results comparing it to the model predictions will be presented.

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9778-116, Session PSWed

## Next-generation of metrology software platform dedicated to nanopatterns: application to semiconductor industry

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The dimensional scaling in IC manufacturing strongly drives the demands on CD and defect metrology techniques and their measurement uncertainties. Defect review has become as important as CD metrology and both of them create a new metrology paradigm because it creates a completely new need for flexible, robust and scalable metrology software. Current, software architectures and metrology algorithms are performant but it must be pushed to another higher level in order to follow roadmap speed and requirements. For example: manage defect and CD in one step algorithm, customize algorithms and outputs features for each R&D team environment, provide software update every day or every week for R&D teams in order to explore easily various development strategies. The final goal is to avoid spending hours and days to manually tune algorithm to analyze metrology data and to allow R&D teams to stay focus on their expertise. The benefits are drastic costs reduction, more efficient R&D team and better process quality

In this paper, we propose a new generation of software platform & development infrastructure which can integrate specific metrology business modules. For example, we will show the integration of a chemistry module dedicated to electronics materials like Direct Self Assembly features. We will show a new generation of image analysis algorithms which are able to manage at the same time defect rates, images classifications, CD and roughness measurements with high throughput performances in order to be compatible with HVM. In a second part, we will assess the reliability, the customization of algorithm and the software platform capabilities to follow new specific semiconductor metrology software requirements: flexibility, robustness, high throughput and scalability. Finally, we will demonstrate how such environment has allowed a drastic reduction of data analysis cycle time.

9778-117, Session PSWed

## Root cause analysis of overlay metrology excursions with scatterometry overlay technology (SCOL)

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First order scatterometry overlay metrology, here on a KLA-Tencor Archer 500 LCM model overlay tool, relies on detection of the angular distribution of diffracted light from a pair of grating over grating structures for each direction of measurement. Such structures may be regarded as a grating resonator for which specific resonant modes systematically appear in the wavelength spectrum. These resonances manifest themselves as rapid variations in the intensity of the various diffracted spectral orders in certain narrow frequency bands [1]. The resonant modes affect the accuracy of the overlay measurements and, in addition, are extremely sensitive to the grating over grating geometry. Any small changes in their structure, asymmetric or otherwise affect the modes in different ways. We propose using such properties for identifying, classifying and mapping process variations (PV) in order to monitor overlay metrology excursions. We will show that in addition to the classical overlay metrics, we can develop new metrics that can be used for creating wafer maps of process variations without any additional measurement requirements. In parallel, this methodology also lets us identify the most optimized on-tool measurement setup.

9778-118, Session PSWed

## Charging model in a fast analytical simulation of SEM images

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Having the ability to predict SEM images with high accuracy would improve setup optimization in factories and help in system development. Advanced Monte Carlo simulators of electron scattering and image formation provide highly accurate results by modeling fast and slow secondary electrons, the detectors, electromagnetic fields and charging. However, these methods suffer from long simulation times, typically several hours. A few extremely simple models of SEM, or emulators, have been developed recently. While the modeled images look roughly like SEM images, the capabilities of such emulators are extremely limited and, in fact, misleading.

An analytical model of the SEM was developed that takes into account the major effects of electron scattering and image formation in the SEM. The beam voltage, current and size, the scanning parameters of the beam, the physical properties of the materials and the 3D shapes of the features are considered. The locations and properties of backscattering and secondary electron detectors are modeled. Extracting or suppressing electrical fields over the sample are also taken into account. The model was upgraded to include a sample charging model. In this way, the accuracy of the analytical model approaches the accuracy of Monte Carlo simulators. In other words, this is not just an emulator, but an actual SEM simulator. Furthermore, the simulation time is approximately one minute, far faster than Monte Carlo.

The A-SEM software was used to simulate a variety of SEM images, especially images with charging. The industry is especially interested in SEM images of tip to tip test samples used in the calibration of optical proximity correction, where the accuracy of the measurements is especially important. A variety of such images have been simulated. It was confirmed that the analytical model is capable of reproducing most major and minor effects of charging, including variations in edge brightness depending on the direction of beam scanning and shadows behind areas with the brightest edges. Examples of the simulations are discussed and compared to SEM images.

9778-119, Session PSWed

## Scanner baseliner control monitoring in high-volume manufacturing

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With ever shrinking node, especially 14nm and beyond, overlay targets are reaching close to tool overlay specifications. The relative importance of scanner stability and scanner induced overlay control in overall overlay budget has steadily increased to maintain best manufacturing yields. Currently, scanner finger print is maintained by Baseliner application which corrects for any drift in grid signature. Vendor provided non product wafers are periodically run and extensive sampling is done all across wafer. A predefined model is applied on sampled data to identify any drift that would later be dialed in baseliner sub-recipe. Using a single predefined model could limit our ability to correct all the different drifts the tool has. Frequent correction also limits us in identifying any tool drift signature as the corrections happen with every baseliner run. The extensive sampling used for baseliner also puts the tool down for considerable amount of time thus affecting tool productivity. In this paper, we explore (i) different analytic models [1] that could be applied on baseliner data to optimize residual finger print; (ii) optimize sampling that reduces metrology time and still has similar overlay corrections, (iii) time monitoring of tool overlay parameters to identify any drift, (iv) multiple illumination dependent overlay monitoring to catch any potential issue on product overlay in 14nm and beyond high volume manufacturing.

9778-120, Session PSWed

## Efficient electromagnetic field solver for metrology applications

Sven Burger, Philipp Gutsche, Jan Pomplun, Frank Schmidt, Lin Zschiedrich, JCMwave GmbH (Germany)

Electromagnetic field (EMF) solvers are an integral part of optical metrology setups in the semiconductor industry. It is expected that decreasing IC feature sizes result in lower budgets for numerical error of EMF solvers [1]. Efficiency of rigorous numerical solvers is measured in terms of the ratio of numerical accuracy to numerical costs (i.e., computation time). For high-accuracy applications, finite-element method (FEM) based methods for EMF simulations can outperform other numerical methods [2]. In this contribution we report on further performance improvements of FEM, achieved by hp-refinement and efficient meshing strategies.

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9778-121, Session PSWed

## Sensitivity study and parameter optimization of ocd tool for 14nm finfet process

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Due to the feature size shrinking and more complicated structures adopting in the semiconductor manufacturing industry, the critical dimension metrology for the IC process control and monitoring becomes more and more important to the product yield improvement. Currently, Optical critical dimension (OCD) technique, with advantages of non-destructiveness, high throughput, and high precision, has been widely applied, as one of the most import process control tools. Since the measurement precision of OCD technology highly depends on the optical hardware configuration, spectra types, and inherently interactions between the incidence of light and various materials with various topological structures, here a method is introduced for seeking the most sensitive measurement configuration to enhance the metrology precision and reduce the noise impact to the greatest extent. In seeking the best mode and spectrum type for data collection, system noise of tools were estimated based on hardware precision. All spectrum types (SE, SR, Mueller matrix) were normalized for comparability. The sensitivity of different normalized spectra modes with several hardware configurations of incidence angles and azimuth angles were investigated. The optimal hardware measurement configuration and spectrum parameter can be identified. The minimum parameter tolerance of a given model can be retrieved by theoretical simulations. FinFET models of 14 nm nodes were constructed to validate the algorithms. The best measurement mode was selected. This method can provide guidance to the measurement precision before measuring actual device CDs. Basically, OCD hardware system (with uncertainties involved) and metrology target should be taken as a whole system. Combination of spectrum type, angle of incidence (theta) and azimuth angle (phi) was defined as the light incidence measure mode. The noise retrieved from any machine part uncertainty or processing randomness, will hide in the collected spectral signals, and can be quantitatively embodied in the spectra intensity difference for corresponding certain measure condition and target. However, when light incidence mode varied, the noise presentation is at another place. Similarly, the controllable measure precision can also be retrieved from the relationship between above mentioned spectral signal difference and structure parameter variation, when the measure mode and optical measure target are identified. In terms of the definition of sensitivity, ergodic calculation on all modes was conducted on the transformation from system configure uncertainties to noise (MSE for a statistical processing). Then the noise can be transformed into controllable measure precisions of parameters of interest. As one of crucial parameters, Fin_CD is set to be floating in the OCD model for detail sensitivity investigation. Ergodic calculation of controllable measure precisions of all the modes was conducted. The selected waveband ranged from 250 to 800 nm, with 5nm as interval to collect signal points. The sensitivity analysis results that the most sensitive region was near theta = 65 deg and phi = 5 deg. Optimum measure mode can simultaneously be filtered out to guide optical-mechanical system design of OCD machine. The simulation results shown that the controllable measure precisions of key structural parameter under respective optimum measure modes were significantly improved, comparing with those under traditional modes as reference. This method will be beneficial for the OCD tool engaged at advanced node and beyond without apparent movement of machine hardware.

9778-122, Session PSWed

## Metrology target design simulations for accurate and robust scatterometry overlay measurements

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In this work we make use of an angular-resolved scatteromerty for overlay technique in which the intensity of a reflected coherent light spot from a grating-over-grating target in pupil plane is examined. An induced offset between the lower and upper gratings is introduced to enforce asymmetry between the +1st and -1st diffraction orders. Subtraction of the -1st order from the +1st order, which is termed the “differential signal”, gives a measure to the asymmetry due to that offset. In measurements the overlay is calculated from the differential signals of two cells, which together consist of an overlay metrology target.

Overlay metrology target design is an essential step prior to performing overlay measurements. This step is done through the optimization of target

parameters for a given process stack. In order to reduce the development time, using simulations for estimating the accuracy and robustness of various metrology target designs in the process stack has therefore become a common customer requirement. A simulation tool is therefore used to improve the overlay performance and ultimately the device yield.

Overlay targets are required to be printable, to have a relatively large process window, a sufficiently good TMU (Total Measurement Uncertainty) for repeatability specs, small overlay residual errors and sufficiently good accuracy. Finding targets that meet all these requirements demands an advanced simulation tool. This work shows how our Metrology Target Design (MTD) simulator helps in successfully dealing with several of these challenges.

A step by step process has been adopted to ensure minimal number of iterations in the simulation process while optimizing the overlay targets. The stack input (geometry and material dispersions) validation and verification has become an important intermediate step through the steps of designing good metrology targets for cutting edge process nodes. Using film and Optical CD (OCD) measurements has shown to make the necessary difference in being able to design accurate targets and predict the measurement performance by simulations.

Figure 1 presents an example of the analysis of the simulation versus measurement of the sensitivity to overlay metric. The figure shows that by simulating thousands of combinations of pitch, CD, segmentation type, it is possible to find an optimal target. Firstly, we show that in this case it was possible to design a target that meets all necessary target design requirement. Secondly, we show that using film and OCD verified inputs we have achieved an excellent matching between simulation and measurement.

Figure 2 shows how OCD verification can help to find a correct printed CD that has been biased by the process. The input is used to check if the current design still accurate and robust and also to prepare and design more accurate overlay target on the next target printing tape-out.

In this paper we will present how accurate and robust targets can be designed using an advanced simulation tool developed by KLA-Tencor Corporation. We will show how the stack inputs are validated using film and OCD tools, and demonstrate the impact of wrong stack input on target design process flow.

9778-123, Session PSWed

## An ultrasensitive bio-surrogate for nanoporous filter membrane performance metrology directed toward contamination control in microlithography applications

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The semiconductor industry employs filtration technologies for removing contaminants from microlithography processes to reduce wafer defects and to improve yield. Contamination tolerances in photochemical manufacturing processes have changed dramatically in the past two decades, and have reached sub-20 nm sizes according to the recent guidelines of the International Technology Roadmap for Semiconductors. The move to narrower line widths drives the need for innovative filtration technologies that can achieve higher particle retention performance and cleaner process fluids. The filter metrology tools that have been the workhorse over the past decade are also now reaching limits. Parallel development in finer filter membranes and their performance metrology methods are required to meet future market demands.

Fine filter membranes are commonly characterized using porosimetry and nanoparticle (NP) challenge test methods. The limitations of current porosimetry methods include a restriction to sub-15 nm pore-size, potential solvent-filter material interaction, and lack of direct retention performance evaluation. NP challenge test methods for directly assessing particle retention of filter membrane have limitations in quantifying filter membrane performance due to low NP detection sensitivity, potentially high NP-filter affinity, and lack of size distribution assessment. Therefore, filter membrane challenge testing is commonly performed with high concentration of NPs in the presence of surfactant/ligand for reducing non-specific interactions, which is not a representative condition commonly encountered by filter membrane consumers.

To address some of the existing challenges in fine filter membrane metrology, we report a novel bio-surrogate for evaluating particle retention performance of various types of nanoporous filter membranes. This bio-surrogate has been developed by combining components from nanotechnology and biological sciences. A technique capable of single molecule detection is employed to detect sparse concentration of bio-surrogate in filter permeate providing >1000-fold higher detection sensitivity than any existing NP enumeration technique. This bio-surrogate also offers low size distribution, high stability, and chemical tunability.

Results demonstrate that the bio-surrogate can discriminate various sub-15 nm nanoporous filter membranes based on their retention performance. Results are also compared with the gold NP test, which is the current testing standard at Pall Corporation and elsewhere. Due to high bio-surrogate detection sensitivity, lower challenge concentration of bio-surrogate (as compared to other NPs of this size) can be used for filter testing, providing a better representation of customer applications.As this novel test method provides quantitative evaluation of fine filter membrane particle removal performance, it may be very helpful in the development of next generation filtration solutions towards controlling contaminants in microlithography applications.

9778-124, Session PSWed

## Co-optimization of RegC® and TWINSCANTM corrections to improve the intra-field on-product overlay performance

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Improving wafer On Product Overlay (OPO) is becoming a major challenge in lithography, especially for multi-patterning techniques like N-repetitive Litho-Etch steps (LEN, N ≥ 2). When using different scanner settings and litho processes between inter-layer overlays, intra-field overlay control becomes more complicated. In addition to the Image Placement Error (IPE) contribution, the TWINSCANTM lens fingerprint in combination with the exposure settings is playing a significant role as well. Furthermore the scanner needs to deal with dynamic fingerprints caused from lens and reticle heating.

This paper will demonstrate the complementary RegC® and TWINSCANTM solution for improving the OPO by co-optimizing the correction capabilities of the individual tools, respectively. As a consequence, the systematic intra-field fingerprints can be decreased along with the OVL error at wafer level. These solutions perfectly fit into the ASML Litho InSight (LIS) product in which feedforward and feedback corrections based on YieldStar overlay measurements are used to improve the OPO. The RegC® application takes the intra-field systematic fingerprint and the OVL error based on YieldStar overlay measurements and induce a predictable deformation elements inside the quartz (Qz) material of the reticle, the deformation introduced by the RegC® is optimized for the actual wafer print taking into account the systematic fingerprints and the wafer overlay and making use of the scale and ortho compensation by the scanner. Alternatively, a pre-determined signature could be induced by the RegC® into the reticle enabling the full correction capability of the scanner. These two applications might be very powerful and could contribute for achieving a better OPO performance.

9778-125, Session PSWed

## Within-wafer CD variation induced by wafer shape

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In order to meet the increasing storage capacity demand and reduce bit cost of NAND flash memories, 3D stacked vertical flash cell array has been proposed. In constructing 3D NAND flash memories, the bit number per unit area is increased as increasing the number of stacked layers. However, the increased number of stacked layers has made the film stress control extremely important for maintaining good process quality. The residual film stress alters the wafer shape accordingly several process impacts have been readily observed across wafer, such as film deposition non-uniformity, etch rate non-uniformity, scanner chucking error, materials coating/baking defects and critical dimension (CD) non-uniformity.

The residual tensile and compressive stresses on wafers will result in concave and convex wafer shapes, respectively. This study investigates within-wafer CD uniformity (CDU) associated with wafer shape change induced by the 3D memory processes. Within-wafer CD uniformity was correlated with several critical parameters including different bow height values of concave and convex wafer shapes, various photo resists with different post exposure baking (PEB) temperature sensitivities, PEB conditions on stressed wafers and DoseMpaper compensation. The results indicate the trend of within-wafer CD uniformity maintains flat for convex wafer shapes with bow height up to +230um and concave wafer shape with bow height ranging from 0 ~ -70um, while the within-wafer CD uniformity trends up from -70um to -240um wafer bow heights. To minimize the within-wafer CD distribution induced by wafer warpage, carefully tailoring the film stack and thermal budget in the process flow for locating the wafer shape at CDU friendly range is indispensable and using PR materials with less PEB temperature sensitivities is also suggested. In addition, DoseMapper compensation is also an alternative to greatly suppress the within-wafer CD non-uniformity but the photo-resist profile variation induced by across-wafer PEB temperature non-uniformity attributed to wafer warpage is uncorrectable, and the photo-resist profile variation is believed to affect etch bias uniformity to some degree.

9778-126, Session PSWed

## Process window and defectivity monitoring using high-throughput e-beam hot-spot inspection, guided by a novel, design-aware, scanner control interface

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Due to continuously shrinking design rules, device patterns have become sensitive to sub-10nm size excursions. Defectivity and yield are now increasingly dominated by systematic patterning defects. SEM imaging combined with smart sampling is required for reliable defect characterization in a manufacturing environment. At the same time, hotspot process window monitoring applications requires high throughput inspection capabilities to achieve sufficient statistical significance across the wafer for a specific product and layer. In particular, post-etch wafer level fingerprints need to be reliably detected.

In this paper, we explore the capabilities of a novel, high-throughput e-beam hot spot inspection tool, SkyScan 5000. We guide the e-beam tool to relevant defects locations with a high-resolution, design-aware hot spot detection scanner interface, Process Window Optimizer (PWO) [Ref.1]. This experimental study uses a state-of-the-art back-end-of-line (BEOL) triple lithography-etch process for patterning of 2D logic features, arranged in a dense full-chip layout. Results will include wafer maps of various hot spot types as function of process variations.

PWO, a holistic lithography solution, is used to identify the location of multiple hotspot types linked to different defect mechanisms, such as variations of focus, effective dose, overlay, or other process fingerprints. SkyScan 5000 uses a vector scan mode and GDS-assisted beam center correction to provide high throughput hot-spot inspection. With a sampling plan that groups multiple nearby patterns of interest (POI) across the full wafer, the tool is capable of inspecting well above >105 points per hour while maintaining high resolution at 3nm pixel size. The inspection provides detailed coverage of both a wide range of pattern types and wafer level spatial fingerprint.

In HVM, the high throughput capabilities of SkyScan 5000, combined with the powerful design-aware detection capabilities of PWO can enable effective hotspot process window monitoring to detect yield-impacting process drifts, optimizing productivity and e-beam tool utilization.

9778-127, Session PSWed

## An analytical method for the measurement of reduced sulfur AMC

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Sulfur containing, airborne molecular contamination (AMC) can affect photolithographic processes and equipment. Neither the ITRS roadmap, the SEMI AMC standard or OEM requirements specifically contain sulfur containing compounds other than SO2. Gases investigated are H2S, DMS, COS, CH3SH, DMDS and CS2, all of which have a variety of natural and industrial sources and can be found up to several tens of ppb. None of the compounds is easily removed from air based on their volatility and lack of acidic/basic properties. We developed an analytical method for the offline sampling and detection of these compounds at the low parts per trillion level.

9778-128, Session PSWed

## Holistic, model-based optimization of edge leveling as an enabler for lithographic focus control: Application to a memory use case

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No Abstract Available

9778-129, Session PSWed

## Study the effect of materials and pore size selection on metals reduction in propylene glycol methyl ether acetate

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The trend in microelectronics fabrication is to produce nano-features measuring down to 10 nm and finer. The PPT levels of organic and inorganic contaminants in the photoresist, solvents, and cleaning solutions is

becoming a major processing variable effecting the process capability and defectivity. The photoresist usually contains gels, metals, and particulates that could interfere with the lithography process and cause microbridging. Nano filters of 5 nm polypropylene, 5 nm polyethylene, and 10 nm nylon were used to filter propylene glycol methyl ether acetate PGMEA containing 100 ppb of Na, Mg, Al, Ca, Cr, Mn, Fe, Cu, Zn, and Pb. It was shown that the 10 nm nylon filter was significantly more effective in removing metals than 5 nm polypropylene and polyethylene. All filters were effective in removing trivalent Al, Cr, and Fe metals indicating the mechanism for their removal as mechanical sieving. However, the nylon was also very effective in removing the divalent metals showing adsorptive properties. Furthermore, the metal removal of the nylon membrane was studied as a function of pore size. Nylon membranes having pore size of 5, 10, and 20 nm were tested and found that the finer pore size is more effective in metal removal. In addition, the effect of charge on nylon was studied and found that the metal removal can be improved by increasing the charge capacity of the nylon membrane. Moreover, the photoresist residence time with the nylon membrane was studied by varying the flow rate. It was found that lower flux rate would result in more effective metal removal.

9778-130, Session PSWed

## Electrical defects detection with SEM based review tools in semiconductor production mode manufacturing

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Abstract – In the semiconductor manufacturing process, electrical defects occur due to a marginal process window that often affects the lithography and etch process which results in bridging patterns and overlay issues. These consequently cause electrical shorts and partially etched vias ending with electrical opens. Ebeam tools are typically used to find electrical failures through voltage contrast techniques, based on charge control differences between different areas on the wafer. These results shorten time to resolution for electrical failures when compared to using probe results. However, due to eBeam inspection having still a high COO, customers which process older technology nodes have a motivation to obtain similar results through a higher throughput with reduced cost of ownership. One potential alternative for some eBeam applications is using conventional review SEMs with Image to golden reference image inspection capabilities in Automatic Process Inspection (API ) mode to conduct electrical inspections of die features. In API mode the customer identifies high risk areas for fail and the tool will automatically navigate to these locations, by using Auto Defect Redetection (ADR) with comparison to golden reference, resulting in detection of the VC defects. This paper will detail several case studies of using a SEM review tool to detect systematic electrical defects. This methodology can prove beneficial while monitoring, and developing patterning techniques for a specific design rule by catching electrical shorts and opens that are more visible at a lower resolution inspection used in process monitoring. Outcomes of this effort show that conventional review SEM techniques, using known areas prone to process inconsistencies derived from features pushing the design rule, have the capability to effectively and efficiently emulate eBeam inspection results when implemented in a production setting at process node of 100nm - 200 nm. This paper is collaboration between Applied Materials and Microchip Technology Inc.

9778-132, Session PSWed

## Recipe creation for automated defect classification with a 450mm surface scanning inspection system based on the bidirectional reflectance distribution function and polystyrene latex spheres

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This study explores the feasibility of Automated Defect Classification with a Surface Scanning Inspection System. The defect classification will be based upon scattering sensitivity sizing curves created through Bidirectional Reflectance Distribution. The Bidirectional Reflectance Distribution Function will allow for the creation of Surface Scanning Inspection System sensitivity/ sizing curves based upon the optical properties of both the filmed wafers and the optical properties of the Surface Scanning Inspection System.

The elimination of Polystyrene Latex Sphere (PSL) and/or process particle deposition on both filmed and bare Silicon wafers prior to Surface Scanning Inspection System (SSIS) Automated Defect Classification recipe creation creates a challenge for light scattering surface intensity based defect binning This study will explore the theoretical maximal Surface Scanning Inspection System sensitivity based on native defect recipe creation in conjunction with the maximal sensitivity derived from Bidirectional Reflectance Distribution Function modeling recipe creation.

Maximal sensitivity SSIS scan results from bare and filmed wafers inspected with recipes based upon Bidirectional Reflectance Distribution Function modeling will be created to determine the Automatic Defect Classification binning accuracy of the native defect SSIS recipe creation methodology . Following SSIS recipe creation, initially targeting maximal sensitivity, each recipe will be optimized to classify Crystal Originated Pits, particles, area defects and scratches.

A statistically valid sample of defects from each Surface Scanning Inspection system recipe results for each bare wafer/filmed substrate will be reviewed post Surface Scanning Inspection System Automatic Defect Classification processing on a Defect Review Scanning Electron Microscope. Native defect images will be collected from each statistically valid defect bin category/size for Scanning Electron Microscope Review.

The data collected from the Defect Review Scanning Electron Microscope will be utilized to determine the statistical purity and accuracy of each SSIS defect classification bin.

This paper explores both the commercial and technical considerations of the elimination of Polystyrene Latex Sphere deposition as a precursor to Surface Scanning Inspection System recipe creation targeted towards Automated Defect Classification. Successful integration of Surface Scanning Inspection System Automatic Defect Classification in conjunction with recipes created via Bidirectional Reflectance Distribution Function modeling has the potential to dramatically reduce the workload requirements of a Defect Review Scanning Electron Microscope.

9778-135, Session PSWed

## Focus measurement method by SEM image analysis of circuit pattern

Shinichi Shinoda, Hitachi, Ltd. (Japan)

We have developed a new focus measurement method based on analyzing SEM images that can help to control a scanner.

In advanced semiconductor fabrication, rigorous focus control of the scanner has been required because focus error causes a defect.

Therefore, it is essential to ensure focus error are detected at wafer fabrication.

In the past, the focus has been measured using test patterns made outside of the chip by optical metrology system.

Thus, present focus metrology system can't measure the focus of an arbitrary point in the chip.

The new method enables a highly precise focus measurement of the arbitrary point of the chip based on a focus plane of a reference scanner.

The method estimates the focus amount by analyzing side wall shapes of circuit patterns of SEM images.

Side wall shapes are quantified using multisliced contours extracted from SEM-images high accuracy.

By using this method, it is possible to measure the focus of the arbitrary circuit pattern area of the chip without a test pattern.

We believe the method can contribute to control the scanner and to detect hot spots which appear by focus error.

This new method and the evaluation results will be presented in detail in this paper.

9778-136, Session PSWed

## Surface profile measurement of highly reflective silicon wafer using wavelength tuning interferometer

Yangjin Kim, Naohiko Sugita, Mamoru Mitsuishi, The Univ. of Tokyo (Japan)

In phase-shifting Fizeau interferometers, the phase-shift error and multiple-beam interference are the most common sources of systematic error affecting high-precision phase measurements. The nonsinusoidal waveforms can be minimized by applying synchronous detection with more than 4-sample. However, when the phase-shift calibration is inaccurate, these algorithms cannot eliminate the effects of nonsinusoidal characteristics. Moreover, when measuring the surface profile of highly-reflective samples, the calculated phase is critically determined not only by the decrease in the fringe contrast but also by the coupling error between the harmonics and phase-shift error. In this presentation, the phase errors calculated by several conventional phase shifting algorithms were estimated by considering the coupling error between the higher harmonics and phase-shift miscalibration. It was shown that the 4N–3 algorithm gives the smallest phase error among the conventional phase-shifting algorithms listed in Table 1. Finally, the surface profile of a 4-inch silicon wafer was measured using a wavelength-tuning Fizeau interferometer and the 4N–3 algorithm. The repeatability measurement errors of 4N–3 algorithm was better than any other algorithms listed in Table 1 even though the phase shift miscalibration is 30%.

9778-138, Session PSWed

## Automatic pattern localization across layout database and photolithography mask

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Advanced process photolithography masks require more and more controls for registration versus design and CDU. The distribution of the measurement points should be distributed all over the whole mask and may be more dense in areas critical to wafer overlay requirements. This means that some, if not many, of theses controls should be made inside the customer die and may use non-dedicated patterns. It is then mandatory to access the original layout database to compare the drawn patterns with the etched ones.

Finding some relevant patterns in a database containing billions of polygons may be possible, but matching their physical location on the mask with the original drawing is manually almost impossible. Combining, on one hand, a software expertise in mask databases processing and, on the other hand, advanced skills in control and registration equipment, we have developed a Mask Dataprep Station able to select an appropriate number of measurement targets and their positions in a huge database and automatically create measurement jobs on the corresponding area on the mask for the registration metrology system. In addition, the required design clip is generated from the data base in order to perform the rendering procedure on the metrology system.

This new methodology has been validated on real production line for the most advanced process. This paper presents the main challenges that we have faced, as well as some results on the global performances.

9778-139, Session PSWed

## Prediction of ppm level electrical failure by using physical variation analysis

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No Abstract Available

9778-140, Session PSWed

## Excursion detection using leveling data

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Prior to the actual exposure, every lithography scanner performs a height scan of the chucked wafer surface to make sure that the exposure remains in good focus across the wafer. However, since the scanner exposure is restricted by the exposure slit, which has the width of the exposure field and a finite length in scan direction, it is not possible to fully correct unflatness within the exposure field. Using the leveling data of the exposure tool, it is possible to predict where non-correctable leveling errors will occur.

With the Obsidian module of the OVALiS software, the leveling data of the scanner are automatically downloaded after exposure. These data include both the measured leveling height maps and the correction profiles applied by the scanner. Therefore, it is possible to calculate the non-correctable part, which consists of static and dynamic focus residuals.

Both the leveling height data and the resulting focus residual data can be used for automatic monitoring. The sensitivity of the monitoring method is greatly enhanced by point-wise comparison of the wafer maps to a fixed set of reference wafers, prior to the definition of smart metrics on the difference map. In this way, it is possible to detect process or exposure tool changes that would otherwise go unnoticed.

In this paper, we present a typical variety of monitoring results on production data in a high volume manufacturing (HVM) setting, showcasing the power of the method by stressing the benefits of early drift and excursion detection. Four different use cases are discussed in depth.

In the first use case, smart metrics that are sensitive to unusual leveling behavior are used for detection of scanner and process excursions at the wafer edge. In the second use case, chuck drift is monitored to determine when the chucks must be cleaned, including an assessment of the post-clean improvement.

Correlations between wafer edge leveling residuals and overlay performance are made, based on sensitive key numbers and verified by comparison of leveling wafer maps with overlay vector plots. This reveals a clear correlation between wafer edge wafer warpage and overlay issues. Finally, we used signature recognition metrics to determine non-litho process drifts or excursions, using wafer height maps corrected for chuck fingerprints.

9778-142, Session PSWed

## Improving reticle defect disposition via fully automated lithography simulation

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Most advanced wafer fabs have embraced complex pattern decoration which creates numerous challenges during in-fab reticle qualification. These OPC techniques tend to create assist features that are very close in size and shape to the main patterns as seen in Figure 1. A small defect on an assist feature will most likely have little or no impact on the fidelity of the wafer image whereas the same defect on a main feature could significantly decrease yields. In order to properly disposition these defects, operators need an efficient method that separates main features from assist and predicts the resulting defect impact on the wafer image.

Past work has shown that reliable defect impact on the wafer data can be produced using the ADAS™ defect simulation system[1]. Up until now, using ADAS simulation was limited to engineers due to the various settings that are needed to be manually entered / adjusted in order to create an accurate result. A single error in entering one of these values can cause erroneous results therefore, full automation is necessary. In this study, we propose and test a new method where all needed simulation parameters are automatically loaded into ADAS. This is accomplished in two parts. First we have created a scanner parameters database that is automatically identified from mask product and level names. Second, we automatically determine the appropriate simulation threshold by using a new reference image (provided by the inspection tool) that contains a known measured value of the reticle critical CD. This new method automatically loads the correct scanner conditions, sets the appropriate simulation threshold, and automatically measures the %CD change caused by the defect. This streamlines qualification and reduces the number of reticles being put "on hold" waiting for engineering review. In this study, we present data showing the consistency, accuracy and repeatability of the new method along with the impact on the efficiency of in-fab reticle qualification.

9778-144, Session PSWed

## Highly resolved dimensional control of line gratings by ultra-small angle x-ray scattering

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Fabrication of nanostructures by lithography requires new tools to characterize their shape, size and organization. In fact, the continuous minimization of the nanostructure sizes pushes the conventional techniques, such as scanning electron microscopy (SEM) or atomic force microscopy (AFM), to their limits. Scatterometry methods offer an attractive approach but require an optical model to calculate the response of the system. SAXS (small angle X-ray scattering) or GISAXS (SAXS in grazing incidence) are characterization techniques considered promising for dimensional control by the ITRS roadmap [1]. Actually, several analytical models and experimental approaches have been developed, during the last years around the CD-SAXS technique [2, 3].

In this project, we evaluated to their limit the CD-SAXS capabilities. At this end, we measured several structures (line gratings with different periodicity, line width and profile) on a U-SAXS setup and performed advanced data reduction to quantify the sensitivity of this approach on the investigated parameters. The measured structures are: i) Tungsten lines gratings and ii) Si-ARC (Silicon Antireflective Coating) lines gratings both deposited onto a thin silicon membrane (100 nm thick) [4]. The membrane diameter is 1 mm. Period range of the line gratings is between 100 and 200 nm, sidewall angle of the lines varies between 0 and 12 degrees, lateral roughness amplitude and period varies between 10 and 20 nm, and 30 and 100 nm respectively...

Measurements were performed on a Rigaku smartlab diffractometer equipped with a Cu rotating anode (8.05 keV). Primary optic includes a parabolic multilayer mirror and a two bounces Ge (220) monochromator. The ultra-small angle X-ray scattering (USAXS) configuration is achieved by Bonse-Hart type channel cut collimators. The measurements are performed in transmission (across the membrane thickness). The beam size at the sample position is of few mm?, i.e., much larger than the membrane diameter. The surrounded bulk Si plays so the role of internal slits. We defined as z the direction of the normal to the surface, x the direction perpendicular both to z and to the line gratings, and y the direction along the line. Samples can also be finely tilted around the y axes (0 to 45° by step of 1°). Finally, detector scans allow measuring large (qx,qz) reciprocal space maps (RSM) with a high resolution configuration. Position, intensity and broadening of the Bragg peaks, due to the superstructure, were extracted from the RSM and their variation along the qx and qz axes were plotted and analyzed. Thanks to reverse Monte Carlo simulations, the line periodicity and line width were extracted and revealed to be in good agreement with the one obtained by CD-SEM and CD-AFM. Sidewall angle was extracted and compared to cross sectional SEM images. Stitching effect was also detected and its period was determined. Peak broadening with peak order is discussed in terms of period dispersion and cumulative roughness. Finally, on an another setup (ESRF-BM02 beamline) equipped with a 2D detector, (qx,qy) RSM are also measured. Amplitude and periodicity of the lateral roughness is determined. A very low amplitude roughness, not detectable with conventional technique (~3 nm) is quantified.

9778-145, Session PSWed

## Best practices for monitoring humidity in emersion scanner reticle environments to reduce reticle haze effects

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Emersion technology scanners are adversely affected by a phenomenon called "Haze" when proper measures are not taken to measure and control it. There are three areas that need to be controlled to reduce this haze effect on reticles, one of which is controlling humidity. Reticle haze is accelerated when H2O is present.

There are several limitations with the current reticle environment RH measurement methods, for example, hand-held RH sensors are inconvenient, they can compromise the reticle environment and many areas are inaccessible by hand-held RH sensors and in-situ RH sensors can be impractical.

Additionally, the importance of particle, leveling, vibration and relative humidity control has rarely been considered in reticle environment. However, the need to maximize both yields and tool uptimes in reticle mask environments requires best-in-class practices.

Whether for diagnostics, qualification or preventative maintenance, equipment engineers need to efficiently and effectively make measurements and adjustments to the tools. Legacy particle, vibration, leveling and RH measurement methods are typically cumbersome, non-representative, not real time, compromise the production environment and are costly with downtime required to take the tool offline for these tasks. By contrast, best practice methods involve collecting and displaying data in real-time, speeding equipment alignment or set-up. Real-time data also speeds equipment diagnostic processes saving valuable time and resources. Equipment engineers can also make the right adjustment time after time with objective and reproducible data that essentially enhances process uniformity.

This discussion will review the advantages of using a wireless, real-time,

reticle-like device (AMSR/APSRQ) for key measurement applications in reticle mask environments that delivers on three compelling bottom lines – saving time, saving expense and improving yields.

9778-146, Session PSWed

## Net tracing and classification analysis on e-beam die-to-database inspection

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With pattern shrinking down in the advanced semiconductor nodes, systematic defects from optical proximity correction (OPC) becomes an important yield bottleneck, especially in the beginning of new products tape-out. E-Beam voltage contrast (VC) die-to-database (D2DB) inspection

A novel classification methodology is constructed for E-Beam die-to-database (D2DB) inspection results on via layers. It is a design guided defects classification flow which helps to pin-point true defects from a big amount of false alarm defects. The die-to-database E-beam inspection has remarkable features can help find systematic defects such as: Damaged Via, Missing Via; which will be reported as DVC (Dark Voltage Contrast) defects. However, the D2DB result usually reports millions of defects that lie on both 'active via' and 'floating via', the former being defect-of-interest (DOI), and the latter being of little significance. The indiscriminant mixture of DOI (on active vias) and nuisance (on floating vias) is a challenge in the use of D2DB for finding systematic via defects. In this flow, we adopted the Net Tracing and Classification feature of Nanoscope-Hotspot Pattern Analyzing (HPA) to classify all of the reported DVC defects as being either DOI or non-DOI. We do this by overlaying the E-beam defect location onto the design layout file (GDS or OASIS) and tracing the path of the via to determine whether or not it connects to the active or diffusion layer. This separates active via from floating Via and allows all reported via defects to be classified. Net Tracing Classification is an enhanced application of design based pattern search. This classification needs to involve multiple interconnected process layers. In the new process flow, net tracing will separate DVC defects into three groups: (1) Real DVC defects, in which the net down to active layer; (2) False DVC type 1, in which the net trace down to gate (which is always dark); (3) False DVC type 2, in which the net traces down to floating metal (which is always dark as well). This enhanced defect classification is greatly helpful on separating real DVC via defects from false alarms. It has a secondary benefit of reducing the total number of defects, which is significant for future in-depth data analysis. In addition, the verified real DVC locations can be used to generate care areas for E-Beam die-to-die (D2D) inspection, which can effectively improve throughput and reduce the turn-around-time (TAT). In this paper, we will discuss a use case at the Vx layer.

9778-54, Session 12

## Proposed approach to drive wafer topography for advanced lithography

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Wafer topography measured prior to shipment to device manufacturers has a long history of enabling next generation process integration. For example, nanotopography (NT) was established as a new wafer measurement requirement when film thickness variation after chemical-mechanical polishing (CMP) for shallow trench isolation (STI) was linked to incoming wafer front surface topography. Even then (~1999) the link of NT to lithography was hypothesized as being "more important than to STI CMP."

In this talk we explore the fundamentals of nanotopography measurement of bare and epitaxial silicon wafers to predict substrate suitability for advanced lithography. Here we assume the wafer topographic data is acquired during high volume manufacturing (HVM) of the 300 mm diameter substrates currently used in device manufacturing that require advanced lithography. We further assume that the substrates qualify for 193 nm immersion lithography requiring multi-patterning at the front-end of line (FEOL).

These substrates for multi-patterned FEOL layers already face a gauntlet of extremely tight dimensional specifications. However, in HVM the key is to maintain yield while preventing escape of substrates that impact yield further downstream. Multi-patterning combined with the growing presence and importance of diffraction-based overlay (DBO) has made overlay more sensitive to substrate nanometer-scale topographic features than previous generations. Added to this many device designs combine vertical integration arrays with planar logic within each die, creating spatially non-uniform film stress, wreaking havoc on corrections per exposure (CPE) for near edge die.

We present our proposal for preventing escape of nanometer-scale topographic features during wafer HVM using a new type of topographic filtering and data processing. We call this approach "litho-NT" as opposed to the previously mentioned "STI-CMP-NT" that is already well accepted in the industry. Our proposal is based on double-sided full-wafer interferometry currently used to measure dimensional properties of these wafers, such as flatness and shape, with high precision. We believe that enabling our proposed filtering and data processing on these tools will help drive HVM wafer manufacturing to new levels of excellence for next generation devices requiring advanced lithography.

9778-55, Session 12

## Assessments of image-based and scatterometry-based overlay targets

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Having a well designed overlay metrology target is one of the ways to improve on-product overlay performance. The traditional screening method in which multiple targets types are added to successive reticle tape outs and then evaluated by trial-and-error may not suffice for the 7nm node and beyond. For instance, although segmentation of image-based overlay target has been reported by many as a means for improving overlay measurement, we find that segmentation does not guarantee improvement. In fact it can be undesirable. Fundamental understandings of metrology and wafer process are required to properly design the targets and carefully optimize them for a given process stack involving multi-level measurement. This paper investigates the Blossom, AIM, and scatterometry targets at the FEOL, MOL, and BEOL patterning levels in 7nm node to gain knowledge needed in order to comprehensively map out the overlay target solutions for future nodes.

9778-56, Session 12

## Lithography-aware overlay metrology target design method

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The semiconductor industry has been successfully moving toward shrinking the device sizes because of the impressive improvements in lithography scanner technologies, together with advanced resolution enhancement techniques. At the same time, overlay metrology systems, methods, and tool performance have been also dramatically improved to catch up with the gradually decreasing overlay budget. These impressive successes have motivated a renewed interest in the development of new lithography-aware overlay target design methods to maximize the overlay target performance for given scanner illumination and dynamic lens aberration under the several

target design constraints.

Metrology target design is becoming critically important for advanced nodes especially using multiple patterning schemes including self-aligned double patterning (SADP) and triple Litho-Etch (LELELE) patterning, and the traditional target design scheme may not be suitable anymore. In general, overlay metrology targets are required to accurately represent the relative placement between device features in different layers. However, it is known that the presence of optical aberrations in the exposure tool may induce pattern placement errors (PPE), which vary depending on the spatial characteristics of the features and the shape of illumination, as shown in Fig.1. The optimized scanner illumination with relatively small filling ratio has become standard to improve the imaging resolution, however such an illumination can easily boost the placement error sensitivity to scanner aberrations compared to a source with bigger filling ratio. Any discrepancy between the spatial characteristics of the device versus those of the metrology target are therefore likely to induce a bias between metrology results and the actual device edge placement, which is sought in order to provide control correctable back to the lithographic exposure tool.

In addition to PPE, another important overlay target design criteria is maximizing target process window (PW), where the overlay targets must have large enough PW to make it robust toward process variations. The illumination in high NA=1.35 immersion lithography systems is typically optimized to maximize the printability performance of the device; therefore the target designer only has limited choices of usable pitch for segmenting overlay targets. Importantly, not fully optimized target design can easily lead to serious patterning issue as clearly demonstrated in Fig. 2, which shows the target printability performance corresponding to one of challenging memory layer using SADP process to print the diagonal pattern, illuminated by the rotated dipole illumination. For these reasons, the overlay targets must be co-optimized based on metrology performances (i.e., Accuracy and contrast) and lithography performance (i.e., PW and PPE) to maximize accuracy, contrast, and PW, while minimizing PPE bias between the overlay target and the actual device.

Throughout this work, we will present a new metrology target design (MTD) method by co-optimizing lithography performance based on scanner exit pupil analysis and metrology performance based on accuracy metric, as described in Fig.3. We will demonstrate how the optimized target can improve target printability while maintaining good metrology performance for rotated dipole illumination, particularly optimized for the diagonally orientated device in the memory active layer. We will also discuss remaining challenges for existing tradeoffs between the metrology and lithography performance from the target design point of view.

9778-57, Session 13

## Material analysis techniques used to drive down in-situ mask contamination sources

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Background ASML relevance

ASML is developing EUV lithography to enable high volume manufacturing. The resolution that is printable with EUV lithograpy requires the feature size on mask to shrink further than with DUV lithography, this shrinks the critical defect size in the system below micron resolution. To prevent yield loss due to particle defects, there are tight controls on the number and size of particles added to the NXE scanner. It is crucial to understand the root cause of any added particle on surfaces, as small as they might be.

Particles on substrate

As in many semiconductor application materials, the particles of interest are on a substrate, more specifically on a test reticle suitable for loading into ASML NXE scanners. These substrates are multilayer with multiple background elements present. Using SEM-EDS analysis on small (< 200 nm) particles is challenging, especially on a substrate with multiple background elements present. Traditional SEM-EDS settings (10 kV and 15 kV beam accelerating voltage) will not yield enough detail to identify potential source bulk materials of small (<200nm) particles. Often only the major component of the potential source is visible in the spectrum, if there is any signal other than the background elements.

Solution part 1: low voltage EDS analysis

We have built a methodology with SEM-EDS that uses an acceleration voltage of 5 kV. This greatly reduces the interaction volume of the electrons in particle and substrate, allowing for higher signal to noise ratio. When applying this technique, the microscope resolving power is also limiting. We will explain how imaging quality of the SEM is connected to getting more contrast between particle and substrate in the EDS analysis.

Within the spectral range below 5 keV, we expect a signal of all relevant elements. The lack of K lines of electron shells of heavier elements is compensated by the presence of L and even M lines of those elements. We will show how using all available information on spectral lines can eliminate the need for higher acceleration voltages. In addition, Monte Carlo simulations are used to confirm that a signal is originating from the particle not the substrate.

Solution part 2: improving statistics in EDS

The traditional way of increasing spectral contrast is to gather more counts by longer dwell time, using a higher electron beam current, using a larger detector area or a combination of these. We will outline a focus on spectral resolution and solid angle. By using a Silicon Drift Detector (SDD) with a spectral resolution of 121 eV @ Mn K ?, spectral resolutions of < 40 eV are reached near the Carbon K ? peak. This allows the usage of the L and M lines of heavier elements in the < 5 keV domain.

Solution part 3: Use elemental mapping to use all available data

To use all available spectral data we use elemental mapping that stores all spectral information per pixel of the area mapped. By selecting the full particle in the map, all spectral information of the particle is used. When using traditional spot or area collection, you often miss parts of the particle or include additional signal from the substrate background.

When elemental maps are used also small inclusions or inhomogeneities in the material can be made visible even below the 100 nm size range.

9778-58, Session 13

## Scanning differential-CDI for EUV actinic photomask inspection

Istvan Mohacsi, Patrick Helfenstein, Yasin Ekinci, Paul Scherrer Institut (Switzerland)

Extreme ultraviolet (EUV) lithography is widely considered as the successor of DUV immersion lithography for technology nodes below 10 nm. One of the major challenges in EUV lithography lies in the fabrication of defect-free photomasks. Hence, mask inspection and mask review are crucial steps in mask production, aimed towards locating, characterizing and fixing mask defects. For these purposes, actinic imaging and inspection methods are essential part of mask metrology.

We present scanning coherent diffraction imaging as an attractive candidate for actinic mask inspection. In the proposed scheme, the sample is being scanned across a coherent illumination, while its scattered diffraction patterns are recorded on a high-speed detector without the use of imaging optics. From these patterns, iterative methods can recover the aerial image of the mask with a resolution that is only limited by the numerical aperture of the detector. Moreover, the difference of the measured and calculated diffraction patterns or comparison of die-to-die or site-to-site measured diffraction patterns allows the direct detection of both amplitude and phase defects. The latter method is particularly intriguing for mask inspection, as it not only provides high resolution an sensitivity but by using a continuously moving “on-the-fly” mask blank, it also offers the throughput required for mask inspection by high-volume manufacturing. Furthermore, as part of the RESCAN project, using finer sampling, the very same tool used for mask inspection can also perform mask review, making it a versatile, cost-effective and high-throughput solution for EUV actinic mask metrology.

9778-59, Session 13

## Simulation of AIMS measurements for ILT masks

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Aerial image measurement system (AIMS™) has become one of the standard tools for wafer level inspection of mask performance and mask defects. There are two methods reported for the inspection flow: die-to-die (D2D) and die-to-database (D2DB). The D2D approach compares measured images from two identical dies and tries to detect any defect in it. This approach can only be applied to patterns which repeat in different dies. The D2DB approach compares a measured image to a simulated image. For patterns that do not repeat in another die, only the D2DB approach is applicable. Patterns generated by inverse lithography technology (ILT) may have indistinguishable aerial images but different mask structures. In this case, the D2DB method is necessary for mask inspection. The D2DB method requires accurate simulation of AIMS measurements for bona fide defect detection.

In the simulation, an optical vectorial model is needed to depict the mask diffraction effect. For mask patterns with dimensions close to or smaller than the 193nm wavelength of ArF excimer laser, conventional vectorial Kirchhoff model (thin mask model) is insufficient to describe the electro-magnetic field (EMF) scattering from the mask surface. To accurately simulate the imaging results, a rigorous EMF model is needed to correctly take account of the EMF scattering induced by the mask topography, which is usually called the mask 3D effect. We have used rigorous coupled-wave analysis (RCWA) as a mask 3D model to calculate the diffraction fields from a single plane wave incidence on the mask. Total mask diffraction fields from the partially coherent illumination source in optical lithography can be accurately computed using an Abbe model together with RCWA. A hybrid Abbe-Hopkins model with RCWA can be used to calculate the EMF diffraction at a desired accuracy level while keeping the computation time practical. The calculation speed of the hybrid Abbe-Hopkins model is improved by orders of magnitudes.

Previously, we have reported simulation of AIMS measurements on two-dimensional rectangular structures with various pitches. By floating the parameters in the Mask 3D model including pattern sidewall angle, film stack thickness, film optical properties, and pattern distortions, we were able to match the simulations and measurements. As ILT gradually being adopted in advanced lithography nodes, simulation capability of aerial images of curve linear patterns is needed. In this paper, we will report our simulation results of AIMS measurements on post-ILT mask patterns, whose original targets are simple geometry shapes.

The fitting of measurements is therefore more challenging for AIMS than CD-SEM since AIMS measurements provide full images on the wafer plane. These measurements contain more information than the conventional CD-SEM measurements, which only provide critical dimensions (CDs) or resist contours in some occasions. The CDs or contours merely convey the intensity information near the threshold level. By accurately simulating the AIMS measurements on curve linear mask patterns, it provides a necessary tool to perform the inspection of ILT masks using the D2DB approach and to accurately predict the mask defects.

9778-61, Session 14

## Modeling metrology for calibration of OPC models

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Optical proximity correction (OPC) requires the use of predictive models of lithography, meticulously calibrated to specific manufacturing processes. Both model accuracy and flexibility require these models to be as physically based as possible, given the real-world constraints of computation time for full chip simulation. In very early versions of OPC models, many phenomena were lumped into a generic and empirical "resist model" with enough flexibility to match experimental data, so that the resist model in fact modeled non-ideal properties of the mask, the source, the optics, as well as the resist. Over time, OPC models have become more sophisticated and modular, with a mask model that attempts to capture all of the systematic variation in lithographic results caused by the mask, rigorous optical models that include measured source shapes and aberrations, and a resist model that focuses on known resist mechanisms rather than as a catch-all for remaining systematic variations.

Still, one systematic variation has not yet been separated out from the resist model, and is critical since OPC models are tuned to measured data from the fab: metrology bias. Metrology bias is the systematic deviation between the measured linewidth and the actual feature size. If metrology bias varies with feature size, pitch, and feature type, then this bias will be built into the calibration data used to calibrate the OPC model. These biases are then effectively built into the resist model.

In this work, the analytical linescan model (ALM) [1] is used to predict the metrology bias as function of resist feature size and shape for the case of CD-SEM metrology. By adding this metrology simulation to the OPC model, the compartmentalization of models into physically-based components continues, allowing the resist model to represent only resist effects. A study will be performed to determine if the addition of a metrology model to the OPC model during a calibration flow results in lower calibration RMS and/or more predictive OPC modeling.

References:

[1] Chris A. Mack and Benjamin D. Bunday, "Analytical Linescan Model for SEM Metrology", Metrology, Inspection, and Process Control for Microlithography XXIX, Proc., SPIE Vol. 9424, p. 94240F (2015).

9778-63, Session 14

## Process window limiting hot spot monitoring for high-volume manufacturing

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As the process window for cutting edge DUV lithographic layers continues to shrink, the impact of systematic defects on final yield increases. Finding process window limiting hot spot patterns, and monitoring them in high volume manufacturing (HVM) is increasingly challenging with conventional methods, as the size of critical defects can be below the resolution of traditional HVM inspection tools.

We show a computational method of finding hot spots patterns by full chip simulation and a method of guiding high resolution review tools by predicting the state of the hot spots for all exposed wafers. This hot spot state prediction is based on scanner exposure information and high-throughput Yieldstar metrology. Main process parameters that are estimated from the exposure and measurements are focus and "effective dose" and these are used in a computational model to estimate a probability state for thousands of locations on the wafer. We employ diffraction based focus metrology targets with excellent precision for focus and regular dense line/space patterns to construct an "effective dose" wafer map.

On Imec SuperNova2 10nm metal layer we demonstrate good prediction accuracy by verification of the predicted hot spots defect probability distribution over the wafer.

A large number of critical locations that this methodology allows to be monitored and verified is enabled by an automated way of working. We implement this by collecting contours in GDS format from CD-SEM images using Hitachi High-Technology's DesignGauge contour extraction algorithm, which delivers a result well matches to the regular CD-SEM measurement data that are commonly used for litho model calibration.

For all 2D inspection points, the measured contour and the target design layout are collected in GDS format, which is input to Tachyon verification for defect detection and quantification. This defect detection can use same the detector algorithms that are used to discover design hot spots and connect the defect criteria on wafer to the defect criteria in the computational lithography domain. This approach enables an automated way of collecting high quality information on selected hot spots, where the prediction model helps to sample the most critical important locations that define the edges of the process window.

By utilizing the review data we can also further improve the accuracy of defect prediction for the hot spots by updating the prediction model. From a FEM wafer we collect the data from a large number of hot spots and additional patterns of interest through the entire Process Window. The results are used to update the prediction model. We show that we can monitor and predict the actual state of hot spots this way both in resist and after etch with a similar performance.

9778-137, Session 14

## OPC optimization techniques for enabling the reduction of mismatch between overlay metrology and the device pattern cell

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Aberration sensitivity matching between overlay metrology targets and the device cell pattern has become a common requirement on the latest DRAM process nodes. While the extreme illumination modes used demand that the delta in aberration sensitivity must be optimized, it is effectively limited by the ability to print an optimum target that will meet detectability and accuracy requirements. Therefore, advanced OPC techniques are required to ensure printability and have optimal detectability performance while maintaining sufficient process window to avoid patterning or defectivity issues.

In this paper, we have compared various mark designs with real cell in terms of aberration sensitivity under the specific illumination condition. The specific illumination model was used for aberration sensitivity simulation while varying mask tones and target designs. Then, diffraction based simulation was conducted to analyze the effect of aberration sensitivity on the actual overlay values. The simulation results were confirmed by comparing the OL results obtained by diffraction based metrology with the cell level OL values obtained using design based metrology.

9778-64, Session 15

## 3D-profile measurement of advanced semiconductor features by reference metrology

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A novel method of sub-nanometer uncertainty for the 3D-profile measurement using TEM (Transmission Electron Microscope) and CD-SEM (Critical Dimension Scanning Electron Microscope) images is proposed to standardize 3D-profile measurement through reference metrology. The proposed method has been validated for profile of Si lines and photoresist features in our previous investigations. In this article, we apply the methodology to line profile measurements and roughness measurement of advanced-FinFET (Fin-shaped Field-Effect Transistor) features. The FinFET features are sliced as thin specimens of 100 nm thickness by FIB (Focused Ion Beam) micro sampling system. Cross-sectional images of the specimens are obtained then by TEM. The edges were estimated by using a threshold level of 50% on the intensity profile across the edge of the features. The profiles of fin, hardmask and dummy gate of FinFET features are evaluated using TEM images. The width of fin, the length of hardmask, and the length of dummy gate of FinFET features are measured and compared to CD-SEM measurements. Moreover, we demonstrate a novel on-wafer-3D-profile metrology with CD-SEM measuring a slope cut by FIB (Focused Ion Beam). The results will be used to implement TEM and CD-SEM reference metrology for 3D-profile measurement.

9778-65, Session 15

## Resist 3D model based OPC for 28nm metal process window enlargement

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28nm metal 90nm pitch is one of the most challenging processes for patterning as the resolution is close to the DUV scanner limit. The design rules allow bi-directional multi-pitch multiple CD with high variety of design. Routing algorithms have to handle many constraints in addition to patterning and can thus automatically produce very complex patterning layouts. At this level of complexity three dimensional effects due to the mask as well as three dimensional effects in the resist itself are the main process window limiters. On one side top loss leads to metal shorts and on the other side, line end shortening leads to open via's.

Reference production OPC using two dimensional lithography models cannot predict and thus not correct three dimensional effects. The two dimensional model is based on bottom CD SEM measurement of one dimension and two dimensional structures. Those measurements don't characterize top loss effect or line end footing. We have used a 3D AFM tool to characterize and model the resist profile. This model has been combined with the classical 2D model calibrated using SEM top CD measurement to obtain a 3D resist model [Ref.1]. The prediction capability of this resist 3D model has been validated using KLA 2915 PWQ. The most relevant AI locations of the 3D model have been selected based on their prediction capabilities.

Associated to chosen models we have determined CD limits beyond which post hard mask critical hotspot may appear at process window conditions. The OPC algorithm then uses these models and thresholds to resolve process window conditions. The OPC we have developed uses four process window models. At such levels of constraints for the process window solver algorithm, it is key to carefully set the tradeoff between nominal condition and process window condition. A good tradeoff is obtained when process window conditions triggers edge placement changes for critical hotspots only.

OPC R3D capability to produce a mask without any critical R3D hotspots have been validated on several full chip 28nm designs. The split between classical 2D process window OPC and R3D OPC has demonstrated process window enlargement after HM etch. This gain has been confirmed through yield results from an energy and focus matrix. Reliability has also shown that R3D OPC demonstrates higher via to metal TDDB than a reference OPC. The next challenge will be to use a simpler resist 3D characterization techniques than AFM 3D in order to easily deploy R3D OPC on other critical levels and nodes.

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9778-66, Session 15

## Assessing e-beam direct-write and optical lithography with a multi-beam scanning electron microscope

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Electron optics can assist in the fabrication of semiconductor devices in many challenges that arise from the ongoing decrease of structure size. Examples are augmenting optical lithography be electron beam direct write strategies and high-throughput imaging of patterned structures with multiple beam electron microscopes. We use multiple beam electron microscopy to compare the imaging of semiconductor wafers processed by optical lithography with wafers processed by electron beam lithography.

9778-134, Session 15

## Scatterometry-based metrology for SAQP using virtual reference

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Advanced technology nodes employing multi-patterning techniques for pitch reduction pose new process and metrology challenges in maintaining consistent positioning of structural features. Compounding effects from successive Reactive Ion Etch (RIE) and spacer depositions patterning are difficult to discriminate by a singular evaluation at a specific process step. Figure 1 shows the process flow for Self Aligned Quadruple Patterning (SAQP) to define the small Fin pitch. It is very challenging to examine the pattern using a reference metrology like Transmission Electron Microscopy (TEM). Figure 2 shows an example TEM image in which we are not able to distinguish between the 3 pitches (α, β & γ) coming from SAQP patterning. We cannot validate scatterometry read-out for pitch walking based on TEM images09778-141, Session 15

## Holistic overlay control for multi-patterning process layers at the 10nm and 7nm nodes

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No Abstract Available

9778-143, Session 15

## Challenges in LER/CDU metrology of DSA structures: pitch roughness and cross-line correlations

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In the metrology of nanostructures fabricated on surfaces by nanotechnology methods, two critical challenges are a) the definition of metrics (parameters and functions) which quantify the uniformity of feature sizes and the sidewall roughness (or more generally the shape) of each feature (line or hole edge roughness) and b) the characterization of their positional randomness by appropriately defined metrics. Up to date, the relevant metrological interest in optical and EUV lithography has been focused on the first challenge (CDU/LER/LWR studies) due to their top-down approach, where the position of features is defined with accuracy by the use of photomasks. On the other hand, DSA lithography is a bottom-up self-assembled process which do not guarantee the accurate determination of feature positions, bringing to the litho-metrology scene the second challenge for the characterization of position (placement) errors and correlations of nano-features (lines and holes).

In this paper, we propose an extension of LER metrology of DSA line patterns including both the above mentioned challenges and apply it for the characterization of LER/LWR/pitch statistics of DSA lines (PS-PMMA) with 28nm pitch fabricated by LiNe chemoepitaxy process before and after pattern transfer to Si substrate. First, we examine the impact of DSA peculiarities on the conventional LER characterization methodology (rms, correlation length, roughness exponent, power spectrum, correlation function) and pinpoint the systematic differences with the results from top-down lithographies (see Fig. 1). Secondly, we elaborate pitch metrology and propose the definition of the pitch map form which the pitch roughness along lines and the pitch uniformity across lines can be calculated. The relationship of these quantities with the so-called line placement error and roughness is discussed (see Fig. 2). Thirdly, motivated by the observation that LER in DSA lines is not only an edge phenomenon but more a pattern effect, we focus on the measurement of correlations across lines and propose a generalization of c-factor between edges to a c-factor correlation function between lines to quantify the cross-line correlations. By this function, a new correlation length is defined to characterize the extent of pattern correlations across lines and their impact on LER (see Fig. 3).

The application of the proposed enlarged LER metrology to LiNe DSA patterns shows that pattern transfer leaves almost invariant pitch uniformity to very small values (<3%) but degrades the higher CD variability of PS lines due to etch process stochasticity. In both line patterns (PS and Si lines), LWR parameters are found smaller than LER ones due to strong line edge correlations (DSA footprint). Power spectrum analysis reveals that LWR drop comes from the reduction of high frequencies in line-width fluctuations. Cross-line correlations measured by the newly defined c-factor correlation length seem to extend to almost four pitches horizontal distance for PS lines and are slightly reduced to Si pattern. The effect of guide line roughness on pitch and c-factor metrology is also analyzed while theoretical relationships among the above metrics and parameters are measured. The final aim of our work is the definition of a protocol for the dimensional, positional and roughness metrology of DSA nanostructures based on enlarged methodological tools, statistical tests and well-established theoretical results.

# Conference 9779: Advances in Patterning Materials and Processes XXXIII

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9779-1, Session 1

## Moore or less? The map grows increasingly complex as materials and processes abound *(Keynote Presentation)*

Peter Trefonas III, Dow Electronic Materials (United States)

We are fortunate to be living in the Age of Information, an exciting time of discoveries and continuous process improvements that have driven 50 years of exponential growth. The electronic sector directly has an annual value of about $1.5 trillion, or about 2% of the planet's GNP. Indirectly, its value is far higher as its power, transportation, food production and heath care systems are all dependent on electronics. Its foundation, semiconductor production, is valued at about $350B annually. To maintain this vital engine, as scientists we must continue to discover enabling materials and as engineers we must innovate to reduce the complexity and costs of processes to make them profitable.

This presentation will cover several of the fundamental challenges underpinning successful lithography: using chemistry to accurately locate the edge of a sinusoidal aerial image and then create an acceptable pattern, managing shot noise and other origins of stochastic effects, to understanding and minimization of defectivity. New tools have been brought to resist design, such as high throughput screening, fast-AFM and new polymerization techniques. Resist design has evolved towards a modular polymer approaches with designer monomers, exquisitely designed photoacid generators and quenchers, and even the ability to control, at least in the z-direction, the spatial locations of the molecules in the films. Further control of deterministic location of polymers in the film has led to directed self-assembly (DSA) of block copolymers and even vertically aligned bottle brush polymers.

As technology challenges delayed implementation of EUV lithography, and 193nm exposure tools had to be extended again and again, the lithographic processes have increased in complexity, with a plethora of layers introduced to go below and above the resist film, materials to enable post-process adjustment of the pattern dimensions and roughness and collapse, and then a variety of schemes to frequency multiply. We will review the many schemes and their chemistry with a particular eye on their necessity, potential and impact. With the increased costs and process introduction times to get these complicated flows into production is it time to consider a change from "Moore" to "Less"? How can we simplify the lithographic process without sacrificing resolution or process window, and maintain the march of progress onwards? Will EUV simplify the process? Will DSA have a role?

9779-2, Session 1

## Extending Si, beyond-Si, to beyond-CMOS: Perspectives on logic nano-electronics scaling for the next decade and beyond *(Keynote Presentation)*

Aaron Thean, IMEC (Belgium)

A new information super-structure is emerging as we move into the era of Internet of Everything (IoE). With the orders of magnitude increase in connected devices, future networks are expected to evolve differently from today's internet. As our information infrastructure evolves through the next decade, data centers, smart mobile devices, and sensor nodes will demand a variety of energy-efficient electronic systems that can satisfy a myriad of performance, form-factor, and cost needs. Thus, giving rise to new and mounting challenges for performance, power, cost, and density scaling for nano-electronics. On the other hand, overcoming these new challenges will bring exciting innovations in process capability, material integration, device architectures, and system design. In this talk, we will examine some of the current logic scaling trends, review what are the possible paths forward for process technologies for 7nm, 5nm and beyond. We will also look into how they will have to couple closely to new system strategies. In the process, we will review some of IMEC's on-going advanced Logic R&D activities and innovations targeting upcoming technologies. This will include the processes for multi-gate devices beyond FinFETs, beyond-Si channel devices, and other emerging Beyond-CMOS device-circuit architectures.

9779-3, Session 2

## Metal oxide EUV photoresist performance for N7 relevant patterns and processes

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Inpria continues to leverage novel metal oxide materials to produce high resolution photoresists for EUV lithography with high optical density and etch resistance. Our resists have previously demonstrated 13 nm line/space patterns at 35 mJ/cm2, with extendibility to 10nm half-pitch. We continue to improve photospeed and will provide an update on imaging performance. Since practical patterns for EUV layers will be more complicated than line/space patterns, we also expand on our previous work by demonstrating 2D resist performance using N7 (7 nm node) contact and block mask patterns on small field tools and full field scanners (Figure 1). We will examine the process window, RLS, end-to-end, tip-to-tip, tip-to-line, and LCDU, including the effect of mask bias and track process optimization. A resist model has been created and comparisons between patterned resist features and predictions from this model are discussed. Based on this physical model, the impact of shot noise will be examined in relation to realistic 2D features. Preliminary data on the effect on OPC of using a non-chemically amplified resist will also be presented.

9779-4, Session 2

## Positive tone oxide nanoparticle EUV (ONE) photoresists

Mufei Yu, Emmanuel P. Giannelis, Christopher K Ober, Cornell Univ. (United States)

Extreme ultraviolet lithography (EUVL) has attracted increased attention as an increasingly likely technology, capable resolving sub-10nm half-pitch (hp) features and thus following the roadmap of Moore's Law. New photoresist materials are one of the key drivers for further size shrinkage, which can be developed to support simultaneous improvement in sensitivity, resolution and line edge roughness. Hybrid nanoparticle photoresists stand out from other resist candidates because of the formulation homogeneity, small molecule size, high EUV absorbance and sensitivity as well as high etch resistance due to the inorganic component. Nanoparticles with a variety of organic/inorganic combinations have been investigated and negative tone (NT) patterning has been characterized with EUV, among which the zirconium methacrylate (ZrMAA) nanoparticles showed sensitivity with EUV exposure at 4.2 mJ/cm2 with a resolution as high as 22 nm, and LER of 5.6 nm.

However, the versatility of a NT resist is typically limited due to line swelling

during development in aqueous alkaline developer and only organic developer are preferred. In industrial applications, in the selection of the photoresist system, positive-tone (PT) resist is often more compatible for contact holes and small trenches than a negative tone resist[5]. To date, several PT resists has been reported with minimal L/S feature size in the range of 40nm-150nm with e-beam lithography. However, the dual-tone patternability of a photoresist with e-beam exposure has not been explored in depth, which possesses significant potential if extended into EUV lithography.

Based on the unique dual-tone nature of the organic/inorganic nanoparticles, we have further extended the PT working performance of ZrMAA with deep UV and e-beam lithography. By modifying the NT working process, application of appropriate PEB conditions and using aqueous tetramethylammonium hydroxide (TMAH) as the developer we have induced image reversal. Utilizing 2,2-dimethoxy-2-phenylacetophenone (DPAP) as the primary photo-radical initiator has increased the PT working performance. In our latest research, the minimal line-space feature sizes were 20nm(1:2 L/S) and 30nm(1:1 L/S) with a dose of 55 ?c/cm2 at 100keV accelerating voltage. The resulting trench height varies inversely with pattern density. To further understand and monitor the dual-tone ZrMAA photoresist, we are studying the tone switch mechanism, by adjusting the post-exposure bake (PEB) conditions and the TMAH developer concentration. The elongated PEB time has shown important impact on increasing the solubility contrast and thus switching the working tone.

This study has yielded some interesting insights into the dual-tone photoresist and shown resolution better than 30nm L/S patterns with e-beam exposure. We have shown that PEB has a significant impact on both the solubility change and working tone, with promising indications that the solubility contrast can be further enhanced by adjusting the PEB conditions. The good PT patterning performance with e-beam exposure encourages further extension into EUV characterization.

9779-5, Session 2

## Characterizing and modeling the electronic response to light in metal-based EUV photoresists

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Alternative photoresist platforms are being developed with the goal of meeting resolution, roughness and sensitivity requirements for EUV lithography. Metal-based resists are appealing due to increased etch resistance and absorption compared with organic resists, and resolving power as demonstrated with 13.5nm exposures using synchrotron light.

Recently imec has started a new project to look into novel materials for EUV lithography with particular attention to Metal Containing Resists (MCR) to explore alternative approaches that can offer superior characteristics in photoresist imaging and etching performances which have shown comparable results with more mature Chemically Amplified Resists (CAR) systems. In order to model these MCR it is mandatory to understand both the optical properties and the electronic response to photon absorption. Following previous experiments carried out on organic materials, some of the optical material properties can be experimentally found by merging analysis from high-energy electron scattering models, X-ray Absorption Spectroscopy (XAS), and DUV spectroscopic ellipsometry. In Figure 1 the dispersion curves of a tin-oxide based photo condensable resist are reported . The absorption spectrum (left) is split in 3 regions, upon the different techniques used: modeling up to 41nm ? by using the database of the Center for X-Ray Optics, Electron-Energy Loss Spectroscopy (EELS)/ XAS between 41 and 150nm, and ellipsometry for the longer wavelengths. Dispersion curves can be used to calculate inelastic and elastic mean-free path; convolved to the expected spectrum at wafer level it is possible to estimate electron yield and the secondary electron blur of the analyzed photoresist. All these materials properties can be then combined to modify the physical models currently in use for calibrating organic CARs when using computational lithography software. A detailed description on how to use the dispersion curves experimentally obtained to modify the physical model is reported and discussed in this paper.

9779-6, Session 3

## Negative-tone single component molecular resist based on cationic polymerization

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As the performance requirements for photoresists become more challenging, there has been an increased interest in non-traditional resist designs. Molecular glass resists have been of particular interest as it is thought that their reduced pixel size will improve LER and decrease PAG inhomogeneity. Polymer-bound PAG resists have also been developed in order to further reduce the diffusivity of photoacids. A third approach has been to develop molecular resists that directly contain the PAG functionality, termed single-component molecular resists. This class of resists offer a number of potential advantages including high sensitivity due to the increased PAG loading (as every resist molecule contains a group capable of producing a photoacid), reduction of photoacid diffusivity, and total resist homogeneity. Our group has previously developed a positive tone onium salt based single-component molecular resist (TAS) based on a well-established triphenylsulphonium salt PAG (TPS-SbF6) which was capable of resolving 50 nm lines at a reasonable LER and sensitivity, but was ultimately resolution limited due to photoacid diffusion.1 Since this photoacid diffusion was inherent to the traditional de-protection based positive tone CARs that this single-component resist was based on, we looked to other resist types for inspiration. In negative tone resists based on the cationic homo-polymerization of epoxides however, the photoacid exists as an active species for a much shorter time before protonating an epoxide group and initiating polymerization. Once this occurs the active species is the growing chain end whose diffusion length decreases rapidly as polymerization proceeds. These resists are also of particular interest as they produce a cross-linked polymer network in exposed regions with superior pattern collapse behavior when compared to positive tone polymeric resists. Therefore, a new single component resist has been synthesized which combines the design approach of single-component resists with the superior diffusion and pattern collapse behavior of polymerizable negative tone resists. This resist (TAS-3Ep-SbF6, shown in Figure 1) is similarly based off the onium salt PAG TPS- SbF6 but is further functionalized with epoxide moieties which allow it to act as a negative tone resist without any additives. While TAS-3Ep-SbF6 has been made with the SbF6 anion due to its weak nucleophilicity, the relatively simple three step synthetic scheme used can yield almost any desired anion allowing for the facile synthesis of other epoxide functionalized PAGs or polymerization control additives. In this paper, we will compare the lithographic performance of TAS-3Ep-SbF6 to the positive tone TAS. This study will provide a new example of a single-component molecular resist and will allow for further development of this class of resists.

9779-7, Session 3

## Novel high-sensitivity EUV photoresist for sub-7nm node

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Extreme ultraviolet (EUV) lithography has been recognized as a promising candidate for the manufacturing of semiconductor devices as CH & LS pattern for 7 nm node and beyond. One of the most key performances in the successful EUV resist is how precious EUV dose is utilized realizing ultrahigh resolution and low line edge roughness at the same time. Hereby we describe novel type of chemically amplified resist (CAR) system to achieve 14 nm hp resolution. We found that sensitivity was substantially improved maintaining resolution and line edge roughness. EUV lithography evaluation results obtained for new CAR on EUV interference lithography (EUV-IL) and NXE3300 system are described and the fundamentals are discussed.

9779-8, Session 4

## Acid generation efficiency: EUV photons versus photoelectrons

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The adoption of EUV lithography as a semiconductor manufacturing technology is largely dependent on the ability to produce more powerful and efficient EUV radiation sources. Presently, EUV sources can reach 100W intensity, while the target is 250W. Furthermore, reflective loss during image propagation is significant and reduces the number of EUV photons incident on the imaging layer. For chemically amplified resists, a photospeed-LER-resolution tradeoff is also operative which concurrently limits the attainable image quality if faster resists with higher photoacid generator (PAG) loadings are utilized. The EUV photoacid generation efficiency has been described primarily in terms of the EUV photon absorption by the PAG or the resist matrix and the production of low energy photoelectrons, which are reported as being ultimately responsible for the high quantum efficiencies informed (>1). Such observation led to recent studies by several groups of PAGs with variable electron affinity (EA) and reduction potential (Ered) presumably conducive to a differential photoelectron harvesting efficiency. However, such studies either did not disclose the PAG chemical structures, replaced the EUV source by an e-beam source or lacked a fundamental discussion of the underlying physical mechanisms behind EUV PAG decomposition. In this work, we report the EUV photospeed of a methacrylate-based resist formulated with a battery of openly disclosed isostructural sulfonium PAGs covering a wide range of EA's and Ered's, to unveil any preferential photoelectron scavenging effect. In parallel, several iodonium PAGs are also tested in order to compare the direct EUV photon absorption route to the photoelectron-based decomposition path. Contrarily to what has been widely reported, we have found no direct correlation whatsoever between photospeed and the calculated EA's or experimental Ered's for the isostructural sulfonium PAGs studied. Instead, we found that iodonium PAGs make more efficient use of the available EUV power due to their higher photoabsorption cross-section. Additionally, we determined a cation size effect for both PAG groups, which is able to further modulate the acid generation efficiency. Finally, we present a formal explanation for the unselective response towards photoelectron harvesting based on the stabilization of the PAG cation by bulky substituent groups, the spatial and temporal range of the transient photoelectron and the differences in electron transfer processes for the different systems studied.

9779-9, Session 4

## Investigation of low-energy electron mean free path and energy delivery in EUV resists

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Low energy (<80 eV) photo-electrons and secondary electrons play a crucial role in the exposure chemistry of a chemically amplified EUV resist, however the mechanisms by which they interact in the material are currently not fully understood. In this paper, we present estimates for the inelastic mean free path and energy delivered by electrons in the <80 eV range. Inelastic mean free path is calculated by using the dielectric properties measured using electron energy loss spectroscopy (EELS), while the energy delivery question is investigated by using a low energy electron microscope (LEEM).

The universal curve for inelastic mean free path is well known in the literature, and it quantifies the rate at which an electron directly triggers ionization events in the material [1, 2]. The curve suggests that the scattering mean free path increases indefinitely with decreasing energy for energies <50 eV. This is likely not a fully accurate model, and several authors have suggested that for energies <20 eV, electron-phonon scattering mechanisms are an important channel for inelastic interactions and need to be accounted for [1, 3]. Here, we model the electron-phonon scattering mean free path by using the analytical expressions presented by Dapor [1]. The electron-electron scattering mean free path is calculated by using the dielectric properties of a leading chemically amplified EUV resist measured using EELS, and applying the techniques for the mean free path calculations well established in the literature [2, 4]. Details of the EELS experiment were previously described [5]. The resist absorption spectra obtained after appropriate background subtraction process was used to extract Im[-1/?] by using the normalization techniques described by Egerton [6]. Kramer's-Kronig relationships [6] were then used to obtain the complex refractive index (n+jk) which was then compared with the results from CXRO database which provides values in the >30 eV range. A close match is observed between the EELS measurements and the database values. The results show that electron-electron scattering mean free path trend agrees qualitatively with the universal mean free path trend. The electron-phonon scattering rate however increases with decreasing electron energy, which results in the combined mean free path curve decreasing as a function of decreasing energy for electrons with <10 eV of energy. The physical significance of the local maximum in the mean free path observed at 10 eV will be investigated further.

For studying the relative importance of electrons at various energies from an energy delivery standpoint, large area features were patterned by exposing the resist to electrons in the 3-80 eV energy range with the LEEM tool. Features patterned with electron energies <15 eV were found to not print at the doses used. For the patterns that did print, contrast curve measurement was performed on the post-develop resist profiles to obtain the dose to clear mean free path amount of resist thickness, where the mean free path values calculated above were used. Preliminary results show that the energy delivery efficiency increases non-linearly with electron energy. For instance, the dose to clear a mean free path amount of resist for an 80 eV electron is 156x lower than that required for a 15 eV electron, and 7.2x lower than that required for a 25 eV electron.

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9779-10, Session 4

## Cross sections of EUV PAGs: influence of concentration, electron energy, and structure

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Optimizing the photochemistry of extreme ultraviolet (EUV) photoresists should provide faster, more efficient resists which would lead to greater throughput in manufacturing. The fundamental reaction mechanisms in EUV resists are believed to be due to interactions with energetic electrons liberated by ionization. Identifying the likelihood (or cross section) of how these photoelectrons interact with resist components is critical to optimizing the performance of EUV resists. Chemically amplified resists utilize photoacid generators (PAGs) to improve sensitivity; measuring the cross section of electron induced decomposition of different PAGs will provide insight into developing new resist materials.

To study the effect of photoelectrons generated by EUV absorption photoresists were exposed to electron beams at electron energies between 80 and 250 eV. The reactions between PAG molecules and electrons were measured by using a mass spectrometer to monitor the levels of small molecules produced by PAG decomposition that outgassed from the film as shown in Figure 1. This methodology allowed us to determine the number of PAG molecules decomposed per incident electron. Combining this result with the average depth an electron causes chemistry at a given energy, the effective cross sections of PAG molecules were determined for energies ranging between 80 to 250 eV (Figure 2). Comparing the cross sections of a variety of PAG molecules can provide insight into the relationship between chemical structure and reactivity to the electrons in their environments. This research is a part of a larger SEMATECH research program to understand the fundamentals of resist exposures to help in the development of new, better performing EUV resists.

9779-11, Session 4

## Quantification of the resist dissolution process: an in situ analysis using high-speed atomic force microscopy

Julius Joseph S. Santillan, Motoharu Shichiri, Toshiro Itani, EUVL Infrastructure Development Ctr., Inc. (Japan)

The research of resist processes (conventional / alternative) are continuously being pushed forward in line with targets set for the most advanced patterning techniques such as extreme ultraviolet (EUV) lithography. Resist development i.e. dissolution is one significant part of these processes as it is the step where physical patterns are initially formed from the resist film state.

Focusing on this process step, the authors have proposed using an in-liquid high-speed atomic force microscope (HS-AFM) which allows the in situ analysis of material dissolution [1]. Earlier reports have discussed on; the application of this method in analyzing the pattern formation during dissolution not only in conventional alkali-based developer solutions (2.38wt% tetramethylammonium hydroxide) but also organic solvent types (e.g. normal-Butyl Acetate) for negative tone development [2]. In recent reports, the authors have also proposed the application of this method in the analysis of edge roughness (e.g. LER) and line bridging / pinching formation as it occurs in pattern formation during dissolution [3].

This time, an investigation was made on the quantification of what we refer to as "dissolution unit size" or the basic units of patterning materials as it dissolves in the developer solution. Preliminary experiments with actual patterning materials were done using a positive-tone EUV model resist composed only of polyhydroxystyrene (PHS)-based polymer with a molecular weight (MW) of 2,500. The material was utilized at a 50nm film thickness with post application bake of 90°C/60s. The resulting film is soluble in the alkali-based developer even without exposure.

Figure 1 shows a part of the dissolution unit size analysis results for the PHS-based material with images obtained through the HS-AFM (image size: 500x500 nm, resolution: 400x400 pixels, speed: 2 s/image). Analysis was done by first taking the difference between two successive images i.e. two temporal states of the resist surface during dissolution (fig. 1a) which will result in a differential image representing the change in the resist surface at a given time (fig. 1b). This differential image is then analyzed for dissolution unit size estimation (fig. 1c) where statistical results can be obtained (e.g. histogram of dissolution unit sizes as shown in fig. 1d).

Figure 2 show the dissolution unit size trend (temporal) of the PHS-based material as it dissolves in the alkali-based developer solution. In this result, two prominent trends stand out; (1) a small unit size (~2nm) constantly dissolving all throughout the dissolution process and (2) a gradually increasing unit size (from ~2nm) that roughly remains constant (~6nm) after a certain dissolution time (>10s) until the end of the dissolution process. (1) is assumed to be the fundamental dissolution unit size of the PHS-based material. This suggests that (2) is the occurrence of "polymer clustering", which gradually increases in size but remains constant after dissolution reaches a certain film thickness below the initial surface.

During the conference, comparative studies on various resist material platforms / formulations using this method will be reported. Moreover, results and discussions on the effect of dissolution unit size on pattern quality will be presented.

9779-12, Session 4

## Study on stochastic phenomena induced in chemically amplified poly(4-hydroxystyrene-co-t-butyl methacrylate) resist (high-performance model resist for extreme-ultraviolet lithography)

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Chemically amplified resists are an indispensable technology for high-volume production of semiconductor devices. The resolution of chemically amplified resists has been steadily improved during three decades since the birth of its concept. The fabrication of 16 nm half-pitch line-and-space patterns was demonstrated in 2011. The resolution has been further improved and reached 15 and 13 nm half-pitch in 2014 and 2015, respectively, owing to the intensive efforts of resist makers. With the progress in the

resolution, the feasibility of sub-10 nm half-pitch fabrication has recently attracted much attention from the viewpoint of the extendibility of extreme ultraviolet (EUV) lithography. Toward sub-10 nm half-pitch, the stochastic phenomena is a significant concern. Line edge roughness (LER) rapidly increases in the sub-10-nm-half-pitch region of resist processes. Also, the stochastic defect (pinching and bridges) generation is a problem for the high resolution patterning with high throughput. Understanding of the details of stochastic phenomena is important for their suppression. In this study, the stochastic effects were investigated using a model resist with disclosed contents. The model resist consists of poly(4-hydroxystyrene-co-t-butyl methacrylate) (PHSBM), triphenylsulfonium nonafluorobutanesulfonate (TPS-Nf), and tri-n-octylamine (TOA). Using the model resist, line-and-space patterns with 20-60 nm half-pitch were fabricated in the exposure dose range of 15-25 mJ cm-2. The dependences of line width and LER on half-pitch and exposure dose were calculated, using a Monte Carlo method on the basis of the sensitization and reaction mechanisms of chemically amplified EUV resists. On the basis of the analysis of exposure results, the suppression of stochastic effects is discussed from the viewpoint of material design.

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9779-13, Session 4

## Studying electron-PAG interactions using electron-induced fluorescence

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In extreme ultraviolet (EUV) lithography, 92 eV photons are used to expose photoresists. Currently, common EUV resists are chemically amplified using photoacid generators (PAGs). These PAGs produce acid in exposed regions of resists, thus catalyzing many solubility-changing reactions. In EUV lithography, photo- and secondary electrons (energies of 10 – 80 eV) play large role in PAG acid-production. There are several proposed mechanisms for electron-PAG interactions, e.g. direct ionization of PAG molecules, hole-initiated chemistry, and electron trapping.

The aim of this study is to explore another mechanism – internal excitation – in which a bound PAG electron can be excited by receiving energy from another energetic electron. It is possible for such an excitation to weaken the atomic bonding within a PAG and cause it to decompose and release an acid.

This paper explores the mechanism of internal excitation through the analogous process of electron-induced fluorescence, in which an electron loses energy by transferring that energy to a molecule and that molecule emits a photon rather than decomposing. We will show and quantify electron induced fluorescence of several fluorophores in polymer films to mimic resist materials, and use this information to refine our proposed mechanism. Relationships between the molecular structure of fluorophores and fluorescent quantum yield may aid in the development of novel PAGs for EUV lithography.

9779-14, Session 5

## Characterization of metal resist for EUV lithography

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Extreme ultraviolet (EUV) lithography is one of promising candidates for next generation lithography.[1] EUV resist materials continue to be one of the most critical challenges for EUV lithography technology implementation. [2-4] Metal oxide-based nanoparticle photoresists ('metal resists') have recently emerged as a potential alternative to chemically amplified resist. [5, 6] High-EUV absorbing metals provide resists with high sensitivity in EUV lithography. Although the brighter light source is ideal to reduce line-edge-roughness (LER) of resist patterns, high sensitive resist materials are very attractive for compensating the week intensity of EUV light sources and accelerating the mass production with EUV lithography. Metal resists show also the high dry-etching resistance, which is very useful for the thin thickness of EUV resist materials. However the stability and reaction mechanism of metal resists are not clear. Therefore we have developed a new metal resist which shows good sensitivity to EUV light. We have investigated and provided the key insights to further understanding the molecular structure and reaction mechanism of the metal resists. In this paper, our metal resist was characterized using various experimental methods such as Fourier transform infrared spectroscopy (FT-IR) combined with the Infrared-Free-Electron Laser (IR-FEL) [7], X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), X-ray-absorption fine-structure spectroscopy (XAFS), light scattering and so on.

The metal resist is composed of a metal-oxide core and an organic shell. FT-IR spectra of metal resists were measured. Three peaks of carboxylic vibrational modes were recognized at the wavenumbers of 1240, 1432, and 1554 cm-1 in FT-IR spectra of an organic shell. Each vibrational mode was selectively excited by IR light with the wavenumber of 1554 cm-1 from IR-FEL. The IR irradiation changed the IR spectrum of the metal resist. The irradiation decreased the peak intensity at 1369 cm-1. The irradiations with the other wavenumbers did not change any IR spectra of the metal resist. The results suggest organic molecules in the shell have various characteristics in the structure and reactivity, which closely relates to the stability of metal resists. The structure of the metal core and the morphology of the metal resist will be also discussed at the conference.

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9779-15, Session 5

## Metal containing material processing on coater/developer system

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Metal containing materials are attracting attention in extreme ultraviolet (EUV) lithography. These materials, such as metal oxide based photoresist and organic based metal containing photoresist are expected to be next generation materials for advances in resolution, pattern collapse mitigation, etch durability and sensitivity.

Metal containing materials are considered not only for EUV lithography, but also ArF immersion lithography. Spin on metal hard-mask(MHM) is one of the metal containing materials. MHM enables an alternate hard-mask material for higher selectivity, enhanced EUV sensitivity, and various processes such as image reversal process and gap filling process.

Challenges of processing these metal materials need to be addressed in order apply this technology to manufacturing. Behavior of metal containing

materials on coater/developer process including coating process, baking process, developer process and tool metal contamination is studied on CLEAN TRACKTM LITHIUS ProTM Z (Tokyo Electron Limited; TELTM).

This paper reports the progress of metal containing materials process on Coater/Developer system.

9779-16, Session 5

## Characterization of inorganic resists using temperature programmed and electron stimulated desorption

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Inorganic resists are of interest for nanomanufacturing due the potential for high resolution, low line width roughness, and high sensitivity. The combination of high absorption coefficient elements and radiation sensitive ligands can improve inorganic resist sensitivity while still allowing high contrast. As an example of this concept, is the inorganic resist with the general formula, Hf(OH)4-2x-2y(O2)x(SO4)y?qH2O (HafSOx). HafSOx has both high absorption coefficient elements (Hf) and radiation sensitive ligands (peroxides). In this presentation we discuss the characterization of HafSOx dehydration using temperature programmed desorption (TPD) and the interaction of low energy electrons with HafSOx using electron stimulated desorption (ESD). Both TPD and ESD allow us to characterize the key desorption species through thermal and radiative processes that occur while patterning. ESD results indicate that the peroxo species are very radiation sensitive, even for low energy electrons that approximate secondary electrons from EUV exposures. The primary desorption products from HafSOx are O2 and H2O, and the time evolution suggest much faster kinetics for O2 desorption. Recently we have extended ESD and TPD approaches to investigate tin-based organometallic resist materials, which can have a higher EUV radiation absorption cross-section than the Hf-based systems. For the tin-based system both alkyl and carboxylic acid species are found to decompose through both radiative and thermal processes. Initial ESD measurements indicate that the tin-alkyl bond has a much higher desorption cross-section than the tin-carboxylate bond. These data provide insight into the radiation-induced changes responsible for the solubility transition upon exposure and patternability during development, and the role of secondary electrons in these processes.

9779-17, Session 5

## Systematic investigation of the synthesis, characterization and switching mechanism of metal oxide nanoparticle resists

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The International Technology Roadmap for Semiconductor (ITRS) estimates that a feature size of < 20 nm would be needed to fulfil the requirements of the semiconductor manufacturing industry within the next two years. This has created an urgent need for new materials and processes in photolithography technology. In recent years, metal oxide nanoparticle resists have emerged as a new class of photoresist materials. It has been demonstrated that the combination of an inorganic core surrounded by organic ligands and a photoacid generator could offer smaller feature sizes, higher etch resistance, higher imaging quality and appropriate light absorption, which makes them very promising for extreme ultraviolet lithography (EUVL). This presentation will focus on a thorough synthesis and characterization study of the metal oxide nanoparticles, the ability of the nanoparticle resist materials to produce ~20 nm features, and will provide an insight into the insolubilization mechanism of nanoparticle resist.

We have synthesised small size (≤ 5 nm) metal oxide nanoparticles stabilized with isobutyrate ligand (ZrO2-IBA and HfO2-IBA) via a hydrolysis-condensation reaction. Various characterization methods have been used including dynamic light scattering to measure the nanoparticle size, transmission electron microscopy to observe the nanoparticle structure, attenuated total reflectance Fourier transform infrared spectroscopy to detect ligand binding, and thermogravimetric analysis to examine the composition of the nanoparticles. In addition, solid state nuclear magnetic resonance has been used to monitor the shelf-life of the metal precursor zirconium isopropoxide, check the reaction conversion and check the stability of the nanoparticles product over time and storage condition.

Negative-tone patterning of ZrO2-IBA and HfO2-IBA nanoparticle photoresists can be obtained by development in organic solvents, and we found that the amount of photoacid generator compound (PAG) added in the system could influence the solubility change, and thus the development condition. The nanoparticle resist sensitivity has been tested by EBL; critical dimension (CD) of ~20 nm can be achieved by the ZrO2-IBA + PAG system (line dose 900 pC) and HfO2-IBA + PAG system (line dose 1000 pC).

Moreover, we have used small angle X-ray scattering (SAXS) to observe changes in the nanoparticle size as a function of dose. Similar results were obtained for both the control nanoparticle and the nanoparticle and PAG system, in which we observed a higher tendency for nanoparticle aggregation with increasing dose. This nanoparticle aggregation was observed under scanning electron microscopy (SEM) with the overexposed patterns for the PAG system. The SAXS and SEM results suggest that the insolubization mechanism may not only be governed by the ligand displacement of the isobutyrate ligand with the sulfonate group from PAG compound, but also as a result of nanoparticle aggregation.

9779-18, Session 5

## Comparative study of line roughness metrics of chemically amplified and inorganic resists for EUV

Roberto Fallica, Michaela Vockenhuber, Yasin Ekinci, Paul Scherrer Institut (Switzerland)

Line roughness of a photoresist is of crucial technological importance in lithography process because it directly impacts Line width roughness (LWR) of a photoresist is of crucial technological importance in lithography processes because it directly impacts the performance of the device. Though commonly represented by a single number, the raw roughness amount, LWR is fully characterized by also looking at the frequency content. Characteristic length scales approaching or exceeding the gate length are of particular relevance as variance over shorter length scales are averaged and make a minimal contribution to the effective critical dimension. This is especially important when comparing resists systems that do not share a common chemical platform. Post-processing techniques to reduce LWR must also be evaluated with this in mind.

In this work, we compare the roughness of various photoresists patterned by extreme ultraviolet (EUV) interference lithography in densely packed lines/space of half-pitch 50 to 22 nm. The figures of merit Rq, ?, and H (total roughness, correlation length, and roughness exponent respectively) are measured by analysis of top down SEM images using two approaches: the power spectral density (PSD) and the height-height correlation function (HHCF). Errors induced by measurement tool and statistics are taken into account. The exposure were performed at the XIL beamline (PSI), which is well suited to isolating the resist component of the measured LWR as the interference pattern contributes little roughness at the frequencies of interest.

We examine the following photoresists: hydrogen silsesquioxane (HSQ), poly-methyl methacrylate (PMMA); three chemically amplified EUV resists,

and two non-chemically amplified metal oxide based EUV resists. This choice of photoresists provides a variety of photochemical interactions.

HSQ and the non-chemically amplified EUV photoresists achieve the lowest total LWR, below 3 nm, attributed to the small molecular size and lack of acid diffusion. PMMA shows the highest roughness (≈ 6 nm), ascribed mainly to agglomeration-induced roughness due to the large molecular size. Two of the three CAR resists yield LWR of ≈ 3 nm; the third CAR shows a LWR of ≈ 6 nm.

We then extract the correlation length: it is found that all the CARs have a ? above 10 nm while the metal oxide based resists achieve ? of ≈ 7.5 nm. HSQ yields the lowest correlation length at 5 nm. These results indicate that, although the total LWR variance can be reduced significantly by specific formulation of CAR resists, the low-frequency contribution to roughness is consistently higher in CAR resists than in non-CAR, and will therefore have a greater impact on device variation. This effect is attributed to the more complex chemistry of CAR resists, which involves photo-acid generation, diffusion and quenching. As a result, we find that the acid diffusion is the most relevant contribution to both the overall LWR and to the large correlation length. Finally, we use a numerical model based on the acid diffusion of molecules at the line edge and we compare the relationship between diffusivity and ? to our experimental results.

9779-19, Session 6

## Dielectric properties of spin-on metal oxides and their applications for 2D semiconductor devices

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The spin-on metal oxides have been proposed to replace silicon or metal containing hard mask materials which can be deposited by chemical vapor deposition (CVD) or atomic layer deposition (ALD) since they have better etch resistance, wet removability and gap fill ability in high aspect ratio contacts or trenches than CVD or ALD films.

Recently, in addition to applications of spin-on metal oxides as hard mask materials, their applications as dielectric materials are drawing semiconductor industry's attention not only because of their wet removability and gap fill ability as mentioned as advantages over CVD or ALD materials but also because of suitable dielectric and low leakage properties of spin-on metal oxide materials.

It is also reported that the growth of ALD or Molecular beam epitaxy (MBE) dielectrics on 2D materials (such as graphene, MoS2) is very challenging due to uniformity, pinhole issues, and interface defect density while spin-on metal oxides can be coated on 2D materials without such issues.

In this contribution, the dielectric and leakage properties of spin-on metal oxides such as TiOx and HfOx will be reported and their possible applications for advanced 2D semiconductor device patterning and fabrication will be discussed.

9779-20, Session 6

## Contact/via placement management for N7 logic and beyond

Kenichi Oyama, Shohei Yamauchi, Sakurako Natori, Arisa Hara, Masatoshi Yamato, Kyohei Koike, Tokyo Electron AT Ltd. (Japan); Hidetami Yaegashi, Tokyo Electron Ltd. (Japan)

We will focus on hole placement error budget rather than overlay error.

Through the litho and etching process, we will discuss about hole placement mitigation including some kinds of process approaches.

9779-21, Session 6

## 3D-ICs created using oblique processing

D. Bruce Burckel, Paul J. Resnick, Bruce L. Draper, Paul S. Davids, Sandia National Labs. (United States)

The term three-dimensional integrated circuits (3D-ICs) usually implies stacking planar 2D die by using through silicon vias (TSVs) to provide electrical connectivity from die to die. Recent research has also pursued performing seeded regrowth of silicon after processing the first layer of devices, creating a monolithic 3D-ICs. Both of these approaches perform the front-end-of-line processing using planar CMOS process equipment, performing all operations in a top-down, vertical approach, resulting in devices in which the plane of the active region is parallel to the wafer surface. The purpose of this paper is to demonstrate that it is possible to create devices that are 3D at the device level (i.e. with active channels oriented in each of the three coordinate axes), by performing standard operations at an angle to the wafer surface into high aspect ratio silicon substrates. This approach requires only minimal fixturing changes to standard CMOS equipment, and no change to current lithography. Eliminating the constraint of 2D planar device architecture enables a wide range of new interconnect topologies which could help reduce interconnect resistance/capacitance, and improve performance.

Fabrication of CMOS devices requires "blanket" process steps such as oxidations and CVD/ALD depositions, as well as directional steps such as ion implantation, dry etching and metal deposition. Since most blanket steps such as oxidation, and CVD /ALD deposition can be performed conformally, demonstration of oblique versions of ion implantation, dry etching and metal deposition enables fabrication of MOSFETs in high aspect ratio silicon topography. The key to achieving oblique processing is membrane projection lithography (MPL), a technique which creates suspended inorganic membranes patterned with the desired pattern over 3D topography etched in single crystal silicon using standard CMOS equipment. After membrane formation directional processes are performed obliquely through the patterned membrane. All lithography of the membrane occurs on a CMP-flat surface so that high NA immersion steppers may be used. We have previously demonstrated oblique metal deposition to create micron-scale 3D structured electromagnetic materials. Oblique plasma etching is accomplished by combining the MPL process flow with a Faraday cage in order to orient the plasma etching at an angle with respect to the wafer surface, and oblique ion implantation is a process which is already in high volume manufacturing for halo implants.

In this paper we will show proof-of-concept devices fabricated using on 150 mm wafers, using 248 nm optical lithography at Sandia National Laboratories. Each of the directional steps will be demonstrated following the MPL approach. While the examples shown depict single unit cells and/or MOSFETs this approach to fabrication of 3D-ICs is more compelling when each face of the unit cell contains entire modules, or many transistors to gain areal density. Furthermore, this fabrication approach does not preclude either TSV-centric or monolithic structures employing regrowth to engage the usual 3D-IC approaches.

Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

9779-22, Session 7

## Challenges for immersion lithography extension based on negative-tone imaging (NTI) process

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With the delay of extreme ultraviolet lithography (EUVL) application to high volume manufacturing (HVM), several attempts for the extension of ArF immersion lithography have been widely studied. Among the numerous candidates, NTI (Negative Tone Imaging) process now occupies an important position for HVM of the 20 nm and 14 nm nodes devices. NTI process is a method for obtaining a negative-tone reversal pattern by developing with an organic solvent. NTI process allows a good lithography performance at specific patterns such as narrow trenches and contact holes because of the high optical contrast with bright mask. Lower risk of defects due to the fact that NTI process does not use any cross-linking reaction is also one of the factors that it has been applied to HVM.

Given the situation that EUVL is facing difficulties towards the HVM yet, further extension of NTI process is desired for below 10nm nodes devices. Two main problems that NTI extension must solve are a breakthrough of scaling limit and process cost down. In this paper, we will describe our challenges for these problems.

Last year, we reported ACCEL (Advanced Chemical Contrast Enhancement Layer?technique that can enhance dissolution contrast of NTI process. In fact, lithographic performances such as exposure latitude and DOF improved by about 20% by applying ACCEL to a conventional NTI resist. This year we will show the challenges for further scaling using ACCEL with other shrink techniques.

According to the progress of down scaling technologies, number of processes increases and the cost of ownership (CoO) can not be neglected. Especially, the number of lithography steps and etching steps has been expanded by the combination of processes, and it has come to occupy a large portion of total manufacturing cost. DTD (Dual Tone Development) process is one of the simplest pitch split process which can reduce exposure steps as we reported last year. In this paper, we will propose other cost effective processes using NTI. KrF-NTI will be effective for cost down of exposure tools. Furthermore, new stack techniques which can simplify the conventional tri-layer process are also demonstrated.

9779-23, Session 7

## Novel DDR process and materials for front-edge NTD process

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We developed the novel process and material which can prevent the pattern collapse issue perfectly. The process was Dry Development Rinse (DDR) process, and the material used in this process was DDR material. DDR material was containing siloxane polymer which could be replaced the space area of the photo resist pattern. And finally, the reversed pattern would be created by dry etching process without any pattern collapse issue.

We newly developed DDR material for NTD process. Novel DDR material was consist of special polymer and it used organic solvent system. So, new DDR material showed no mixing property with NTD photo resist and it has enough etch selectivity against NTD photo resist.

Image tone reverse was successfully achieved by combination of NTD and DDR process keeping good pattern quality. Tone reverse pattern below hp 18nm was obtained without any pattern collapse issue, which couldn't be created by just using normal NTD process.

9779-24, Session 7

## Fundamental characterization of shrink techniques on negative-tone development based dense contact holes

Kaveri Jain, Scott L. Light, Micron Technology, Inc. (United States)

Enormous advances have been made in recent years to design sub 40nm dense contact hole pattern with local CD uniformity (LCDU) that the process can tolerate. Negative tone development process (NTD) on 193nm photoresists has achieved this to a large extent without the requirement of additional processing steps on the patterned layer.

With further shrinking of size of the subsequent nodes, the demand to produce smaller holes with wider process window, low defectivity, and improved LCDU is increasing, and reaching beyond what can be achieved through NTD alone. Placement capability of these holes in a litho-etch-litho-etch scheme puts additional onus on creating holes with least compromise on LCDU. A number of techniques are in practice today and new schemes are continuously being developed to achieve this. Most notably, implementation of a collar of Atomic Layer Deposition technique (ALD) on photoresist or substrate has been disclosed lately. However, in recent years, a number of electronics material suppliers have provided a spin-on flavor of this process to achieve similar results as ALD. A variety of material properties and constitution of these materials determine their potential in achieving the desired results in terms of defectivity and attachment capability. In this paper, we will provide fundamental characterization of these techniques such as shrink via application of spin-on agents (organic as well as aqueous) on the post-imaged pattern; application of ALD collar; and other dry etch techniques. We will compare them for their shrink and rework capacity, throughput improvement, defect tendency, dry etch capability and ease of implementation in the process flow. In addition, we will also provide recommendations on which technique is suitable for a given set of process prerequisites.

9779-52, Session PS1

## Planarization of topography with spin-on carbon hard mask

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Spin-on carbon hard mask (SOC HM) has been used in semiconductor manufacturing since 45nm node as an alternative carbon hard mask process by chemical vapor deposition (CVD).

For the hard mask processes, wiggle resistance and etching rates are important for fine pitch pattern etching with good CD uniformity. High thermal stability is necessary to avoid outgas contamination during vacuum process without temperature restriction.

As advancement of semiconductor to 2X nm nodes and beyond, more complicated device structure (FinFET, DRAM) is used and planarization of topography become more important and challenging ever before.

Previously we reported syntheses and performance of high carbon polymers for advanced SOC and demonstrated pattern transfer of resist into substrate down to CD 40nm without pattern deformation or wiggling [1, 2].

In order to develop next generation SOC, one of focuses is planarization of topography. This paper presents planarization performance of SOC with different concepts, the influence of thermal flow temperature, crosslink, film shrinkage, baking conditions on planarization and filling performance.

9779-53, Session PS1

## Colloidal nanocrystal assemblies based nanolithography without optics

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Colloidal nanocrystals are synthesized by wet chemistry and are dispersed

in a solvent, so that they be solution processed. They are capped by organic molecules, which keep them colloidally stable, and can be deposited on any surface to form films. However, the organic fraction of these films is detrimental for their physical and electronic properties, but required for their liquid processability. To remove organics from CNAs, calcination or ligand exchange are the approaches used in the community. Both processes have limitations. Calcination lead to carbonization, particles growth, and the method is substrate dependent (cannot use heat sensitive substrates like plastic). Ligand exchange methods are solution based, they do rarely remove all the organic fraction and they compromise the structural integrity of the CNAs. Furthermore, removing the organics causes large volume losses, which leads to cracking in the film. This problem is amplified when particle size is reduced.

Nanocrystals Plasma Polymerization (NPP) efficiently etches the capped molecules leaving neither residues nor signs of nanoparticle growth. NPP employs low-pressure, room temperature, partially ionized plasma to etch the organic molecules deep into the films. This “cold” plasma processing is a “green”, environmentally friendly process, it yields homogenous processing, is routinely utilized in semiconductor processes, is compatible with heat sensitive substrates, is highly reproducible, and does not harm or change significantly the functional inorganic fraction of the film.

We are working to understand the process of NPP on CNAs to use them as patterning template (e.g., DSA). In order to understand the capacity of NPP, we have plasma processed ~300nm-thick film of ZrO2 nanocrystals (~3.5nm dia) capped by trioctlyphosphine oxide (C24H51OP). The preliminary data from Rutherford Backscattering Spectroscopy (RBS) analysis shows that oxygen plasma ([C] reduced from 30 at% to <1 at%) is more efficient in organic removal than helium plasma (~3at % after processing). However, longer processing time may reduce the gap. TEM images and XRD analysis confirms no change in particle size after plasma treatment. This is particularly encouraging, since size related properties are preserved. Our findings suggest that cracks are linked with the initial ordering of the nanocrystals assemblies. Ordering of the CNAs can be controlled by choosing the appropriate self-assembly conditions.

The NPP-based patterning process is pivoted to the solubility of CNAs. The plasma etch the capping ligands from the exposed area. During the development step, the unexposed area of CNAs are solubilized leaving behind the patterned area. The resolution of NPP-based lithography is ideally limited by the size of the nanoparticles because etching is caused by active gas species. Our preliminary data on NPP-based lithography shows that we can transfer the pattern on >200nm ZrO2 CNAs by using 200mesh Cu TEM grid as a hard mask. The whole process of patterning took less than 3mins (30secs to make the coat + 30secs of plasma processing + ~1min for development & drying).

9779-54, Session PS1

## Development of heat resistant polyphenol compounds applied to the spin-on carbon hardmask

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We have already reported developing the xanthendiol derivative, like NF0197 which is characterized by high carbon content and high heat resistance. The small etching rate, and the good potential for Spin-On Carbon Hardmask of NF0197 was assumed to be due to its chemical structure of rigid xanthene skeleton .

Herein we report the development of a new polyphenol applied to the Spin-On Carbon Hardmask and the thermosetting property. We synthesized the new polyphenol, NF7177, by the condensation of 4,4’-biphenol and biphenyl-4-aldehyde. NF7177 showed the superior solubility for the coating solvents, like PGMEA and PGME, and good heat resistance at 400 degrees Celsius without rigid xanthene skeleton like NF0197. NF7177 is hardened by heat treatment without any cross-linking agents in spite of its low molecular weight of 536 g/mol, and then becomes insoluble in organic solvents.

On the other hand, polyphenols synthesized by changing 4,4’-biphenol to 2,6-dihydroxynaphthalene (BisN) and o-phenylphenol (BisOPP-BP) had poor heat resistance and thermosetting property.

These features could be related to biphenol skeleton of NF7177. Because no phenol component containing OH group was detected from 30 to 400 degrees Celsius in the TG-MS measurement of NF7177, on the other hand, phenol components were detected in the case of BisN and BisOPP-BP. The thermosetting properties seem to be depended on the number and position of OH group. It was indicated that the heat resistance of NF7177 was due to cross-linking based on dehydration reaction.

We also evaluated the etching rate of NF7177 after 400 degrees Celsius cure. It showed 15% smaller than that of Novolac. And also the 30wt% PGMEA solution viscosity of NF7177 showed much smaller value than that of Novolac. The low solution viscosity is effective to gap filling and planarization for topography. Therefore, we considered that NF7177 could be applied to Spin-On Carbon Hardmask better than Novolac.

9779-55, Session PS1

## Enhancing the Novolak resin resist resolution by adding phenol to fractionated resin

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Novolak-based resists are widely used for manufacturing semiconductor, flat panel display (FPD) and MEMS devices. In FPD, the pixel size is becoming smaller in a high-precision model. We have been trying to improve performance of novolak-based resists.

In this paper, we report our results on our investigation on the effects of low molecular weight phenolic compounds addition to fractionated novolak-based resists to improve resolution capability.

9779-56, Session PS1

## Development of spin-on carbon hardmask materials for planarization coating on topographic substrate

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Spin-on carbon (SOC) hard mask process plays a very important role for fine pattern transfer from exposed photoresist to the substrate. With the device shrink and new devices complexity increases (FinFET, 3D integration, and so on), SOC is required a lot of properties such as wiggle resistance, etch controllability, thermal resistance, planarization, and gap filling. Especially, planarization on topographic patterned substrate is being important more and more for SOC materials. In this work, we focused on the investigation of SOC which shows good planarization performance. The relationship between material properties and planarization performance are discussed. Furthermore, we will also discuss the material design enabling flat coating on topographic substrate.

9779-57, Session PS1

## Positive-tone, molecular glass resist based on acid-catalyzed depolymerization

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Current, positive-tone polymeric resists suffer from a variety of performance-limiting issues, including photoacid blur and low mechanical strength, that will only become worse as feature sizes continue to shrink. Molecular glass resists that are crosslinked offer potential solutions to these problems by offering higher mechanical strength and lower photoacid diffusion due to their higher glass transition temperatures. Previously, our group reported the synthesis and e-beam patterning of DPA-2VE, a carboxylic acid containing molecule, as an example of a positive-tone, acid-sensitive, depolymerizable resist. DPA-2VE operated by polymerizing during a post-apply bake (PAB) to create acetal linkages between alkenes and carboxylic acids that, when exposed to photogenerated acid and heated, depolymerized to generate base-soluble small molecules that could be developed in aqueous TMAH solution. DPA-2VE resolved 40 nm features under e-beam patterning, however, it exhibited some dark loss, attributed to small amounts of photogenerated acid that were sufficient to induce depolymerization during the PAB. Trioctylamine (TOA) was included to neutralize the acid present at low doses, but TOA reacted with the carboxylic acids on the resist molecule, resulting in a time delay between when the solution was created and patterning performance. Alkenes and hydroxyl groups on adjacent molecules were also reported to react with each other in solution at room temperature. A potential solution to this problem is to simply use a phenol instead of a carboxylic acid. Using a phenol is expected to reduce or eliminate both dark loss and thus the need for TOA and also the -OH and alkene side reactions. A comparison of phenols and carboxylic acids in polymeric depolymerization resists revealed that phenolic polymers required higher doses to depolymerize and develop in aqueous TMAH solution, suggesting that use of a phenol will likely reduce dark loss. This expected difference in performance can be attributed to the different acidities of phenols and carboxylic acids (the latter is on average 100,000 times more acidic), making the carboxylic acids easier to deprotonate and solubilize in aqueous TMAH developer solution. The synthesis of these resist molecules is relatively straightforward and can be completed in one step, followed by silica gel chromatography to isolate the resist with the desired number of alkenes. This paper will compare the effect of replacing a carboxylic acid with a phenol and also the effect of altering the ratio of alkenes to phenols on patterning performance of acid-sensitive depolymerizable resists. This study will offer a new example of a depolymerizable, positive-tone resist while also providing insight into factors that influence the patterning performance of these types of resists.

9779-58, Session PS1

## Spin-on metal oxide materials with high etch selectivity and wet strippability

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Metal oxide or metal nitride films are used as hard mask materials in semiconductor industry for patterning purposes due to their excellent etch resistances against the plasma etches. Chemical vapor deposition (CVD) or atomic layer deposition (ALD) techniques are usually used to deposit the metal containing materials on substrates or underlying films, which uses specialized equipment and can lead to high cost-of-ownership and low throughput. We have reported novel spin-on coatings that provide simple and cost effective method to generate metal oxide films possessing good etch selectivity and can be removed by chemical agents. In this presentation, new spin-on Al oxide and Zr oxide formulations of hard masks will be reported. The new metal oxide formulations provide higher metal content compared to previously reported material of specific metal oxides under similar processing conditions. These metal oxide films demonstrate ultra-high etch selectivity and good pattern transfer capability. The cured films can be removed by various chemical agents such as developer, solvents or wet etchants/strippers commonly used in the fab environment. Therefore, these novel AZ® spin-on metal oxide hard mask materials can potentially be used to replace any metal, metal oxide, metal nitride or silicon-containing hard mask films in 193 nm or EUV process.

9779-59, Session PS1

## Novel silicon hardmask for collapse margin improvement

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The line collapse margin for resist has become more critical as the pitch and dimension of the lithography pattern continues to shrink. Negative tone development (NTD) is a viable approach to achieve good patterning for 20nm node and beyond. NTD patterns are generated over resist/ hardmask/ bottom layer stack by keeping the exposed region on the hardmsk while removing the resist in the unexposed region. The increase of polarity in the resist has created a mismatch in terms of interface property between NTD resist pattern and conventional silicon hardmask used for PTD and pattern collapse has been observed over NTD resist patterns.

In this paper, we present a novel silicon hardmask incorporating a new floatable polymer as an additive to reduce the polarity mismatch between exposed resist and silicon hardmask. Such additive contains acid-labile group for polarity switch once in contact with to acid in the exposure area. The new silicon hardmasks with floatable, and polarity switchable additive provide 7nm wider collapse margin compared to the conventional silicon hardmask. In addition, the detail lithography factors for the new silicon hardmasks including MEF, DOF, and LWR will be investigated. The defect level will also be shown in this paper.

9779-80, Session PS1

## New resist materials based on polyacetal main chain scission

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No Abstract Available

9779-60, Session PS2

## Metal reduction at point-of-use filtration

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As semiconductor manufacturing heads towards 1X nm pattern fabrication nodes, stringent requirements for metal reduction are being placed on lithography process chemicals. These requirements are due to concerns for deteriorating performance of the semiconductor device due to lithography process induced defects[1,2]. Although many lithography chemicals can be supplied with sufficiently reduced metal concentrations[3], the chemicals can also become contaminated by metal components in the flow path between the chemical delivery system and the wafer.

Ion exchange filters are typically used for metal reduction in semiconductor process fluids. These filters make use of strong acid ion-exchange groups which provide good metal removal efficiency and high ion-exchange capacity[4]. However, ion exchange groups also have a tendency to adsorb the ionic additives such as quenchers and onium salts (ionic photoacid generators) present in chemically amplified photoresists (CAR). For this reason, ion-exchange filters are less suitable for lithography formulations which need to be filtered for metal and particle contaminations prior to spin coat them on Si wafers in lithographic process tracks.

In this study, we explored the metal removal efficiency of nylon 6,6 and high density polyethylene membrane based filters, in solvents of varying degree of polarity such as Cyclohexanone and 70:30 mixture of Propylene glycol methylether (PGME) and Propylene glycol methylether acetate (PGMEA). In a typical experiment, first the metal challenge solution was made by adding 1 ppb of metal analytical standard to the test solvent. Using the test stand shown in Figure 1, filtration was conducted under steady flow by adjusting inlet pressure while monitoring the flow rate of 0.5 ml/sec which is common in lithography solvent dispense systems. Influent and effluent metal concentrations were measured using standard ICP-MS analytical tools. The results are summarized in Figures 2 and 3. In all the solvents tested, nylon 6,6 membrane filtration was found to be significantly more effective in removing metals than HDPE membranes, regardless of their respective membrane pore sizes. This paper will address the mechanistic details of metals removal processes in conjunction with membrane chemical structures / properties.

9779-61, Session PS2

## Integrating nanosphere lithography in device fabrication

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This paper discusses the integration of nanosphere lithography (NSL) with other fabrication techniques, allowing for nano-scaled features to be realized within larger microelectromechanical system (MEMS) based devices. Nanosphere self-patterning methods have been researched for over 3 decades, but typically with smaller objectives and not always for use as a lithography process. Only recently has progress been made towards integrating many of the best practices from these publications and determining a process that yields large areas of coverage, with repeatability and precise placement of nanospheres relative to other features. Discussed are two of the more common self patterning methods used in NSL (i.e. spin-coating and dip coating) as well as a more recently conceived variation of dip coating. Recent work has suggested the repeatability of any method depends on a number of variables, so to better understand how these variables affect the process a series of test vessels were developed and fabricated. Commercially available 3D printing technology was used to incrementally alter the test vessels allowing for each variable to be investigated individually. The results from these test vessels were then applied to develop a vessel for full wafer depositions. With this full vessel, NSL was then used in conjunction with other fabrication steps to integrate features only achievable with NSL in conjunction with other more common lithography steps, in the overall fabrication process of larger MEMS devices. Various combinations of NSL self patterning along with photoresist based lithography are evaluated to address various design objectives, and fabrication methods which could be used to reach these objectives.

9779-62, Session PS2

## CD control based on edge placement error analysis

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Amid the ongoing miniaturization of semiconductor devices, multi patterning processes like litho-etch-litho-etch (LELE) and self-aligned multi patterning (SaMP) techniques have become main stream. An increasing number of publications report that edge placement error (EPE) control is required for further improvements in patterning precision [1, 2, 3, 4, 5]. However, no direct analysis method has been proposed to date to evaluate EPE by wafer inspection means. In this paper, EPE values obtained from a geometric model simulation and actual integrated patterns inspection will be presented.

Overlay is believed to be the major component of EPE, but pitch-walking occurring in SaMP processes also has an impact on EPE. This can be explained by considering geometrical models as presented in Figure 1. If perfect grid and block patterns are ideally placed as in case 1, EPE will be zero. However, even with perfect overlay and non-zero pitch-walking as in case 2, EPE will not be zero. Therefore, in order to satisfy EPE requirements after integration, significant process control at each manufacturing step is crucial. In this work, we present a method for calculating the EPE for a given process by combining process simulation and experimental pattern evaluation results.

9779-63, Session PS2

## Metal assisted chemical etching for silicon micromachining

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INTRODUCTION

Metal Assisted Chemical Etching (MACE) is a simple and low-cost method used to fabricate Si nanowires and nanoporous silicon1. The challenge for this fabrication technique is to etch pattern of different size (from nano- to micro-scale) with the control of the vertical direction for high aspect ratio. Charge balancing structures2 or magnetic fields3 were applied in order to solve these issues.

Here, a self-assembly gold nanostructuring by a simple de-wetting process is combined to MACE4, resulting into a resolutive vertical control for a robust and cheap micromachining method, able to produce high aspect ratio silicon microstructures (80 μm deep) with very dense patterns (2 μm features) such as the one for X-ray diffraction gratings.

EXPERIMENTAL

A photoresist layer on a Si substrate was patterned with a grating structure (pitch in the range of 2-5 μm) by using conventional UV Photolithography. Then, a thin Au film was evaporated on the whole wafer and the photoresist was subsequently lifted-off. The Au patterned sample was dipped in an etchant solution of H2O2, H2O and HF. The molar ratio and dipping time were optimized as a function of the Au thin film morphology. Gratings were characterized by Scanning Electron Microscopy (SEM) in cross section and plan-view. The Au catalyst structure and morphology has been investigated by Rutherford Backscattering Spectrometry, high resolution SEM and Atomic Force Microscopy.

RESULTS AND DISCUSSION

Au film was used as a catalyst and its morphology was varied by using different deposition conditions and post-deposition thermal annealing, in order to affect the Au clustering. Fig.1 (top left) shows the typical morphology of the Au catalyst cluster structure containing cracks and pores, at these locations preferential etchant diffusion takes place. The Si etching occurs at higher speed under the Au catalyst pattern, however our study indicated that the process strongly depends on Au film morphology. The Au morphological data were correlated (cluster size, roughness and etching parameters) in order to optimize the etching performances. An example of a grating obtained in 40 min etching is shown in Fig.1 (bottom right). The

vertical control is lost without the Au nanostructuring (Fig.1, bottom left), resulting into undercut due to the catalyst movement during etching.

The sample size was 4" wafer but the scale limit depends only on the size of the Photolithographic pattern. As seen in Fig.1b vertical control of the etching direction can be achieved, which makes the MACE process feasible for robust and inexpensive large scale microfabrication.

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9779-64, Session PS2

## Considerations for fine hole patterning at 7nm node

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The objective of this work is to study the process variation challenges and resolution in post-processing for the CD-bias control to meet sub-20nm diameter contact hole. Another pattern modulation is also demonstrated during post-processing step for hole shrink. With the realization that pattern fidelity and pattern placement management will limit scaling long before devices and interconnects fail to perform intrinsically, the talk will also outline how circle edge roughness (CER) and Local-CD uniformity can correct efficiency. On the other hand, 1D Gridded-Design-Rules layout (1D layout) has simple rectangular shapes. Also, we have demonstrated CD-bias modification on short trench pattern to cut grating line for its fabrication.

9779-65, Session PS2

## Line-space bridge defect reduction via increased contact time at BARC point-of-use filtration

Michael S. Sevegney, Eric Ellis, Benjamin Kolodzie, Brian Beakley, SAMSUNG Austin Semiconductor LLC (United States); Michael Mesawich, Amarnauth Singh, Rao Varanasi, Pall Corp. (United States)

Bridge-type patterning defects continue to challenge yield performance of photolithographic processes at advanced technology nodes. It is well known that applying point-of-use filtration to pattern stack chemicals prior to dispense is effective for overall defect reduction. Moreover, filters built around fine polymeric nylon membranes have been especially effective for reduction of bridge-type defects, which are driven by amorphous, gel-type contaminants. In a sub-20nm LSI technology HVM environment, the Pall P-Nylon EX filter was evaluated against a conventional 10-nm rated nylon membrane filter for 193 nm immersion BARC dispense applications in both FEOL and BEOL segments. Flow configuration of the membrane tortuosity path within the P-Nylon EX filter results in an increased amount of contact time between the influent and the asymmetric Nylon 6,6 membrane matrix, which enhances the efficacy of contaminant capture and retention via adsorptive mechanisms. The P-Nylon EX filter also offers a more favorable differential pressure flow characteristic, which can impact filter start-up and defect performance. Significant reductions in single-line bridge defects were observed in a positive tone imaging line/space pattern process. Also, significant reductions in both single-line and multi-line bridge defects were observed for negative tone imaging line/space pattern processes, which utilize the same BARC chemical and point-of-use filter.

9779-66, Session PS2

## Line-space bridge defect reduction via enhanced filter cleanliness at resist point-of-use filtration

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Nanoscale patterning defects continue to challenge yield performance of photolithographic processes at advanced technology nodes. It is well known that applying point-of-use filtration to pattern stack chemicals prior to dispense is effective for overall defect reduction. The criticality of point-of-use filtration is two-fold: 1) ability to remove and retain contaminants from process fluids, and 2) cleanliness of filter materials of construction from which process fluids may leach various contaminants. Historically, trace metallic impurities have been identified as key contributors to the formation of amorphous, gel-like contaminants, which can manifest as bridge-type defects if dispensed into the patterning chemical stack. A new cleaning technology has been developed to help meet the demanding defectivity performance targets of state-of-the-art semiconductor manufacturing applications. When applied to filtration, this so-called UltraClean (UC) technology reduces trace metal, particle shedding and non-volatile residue (NVR) contaminants. In a sub-20nm LSI technology HVM environment, a 5nm UC filter was evaluated for a FEOL 193 nm immersion photoresist dispense application. In a head-to-head evaluation against a 5nm-rated polyethylene membrane filter, significant reductions in single-line bridge defects were observed in a positive tone imaging line/space pattern process. It was concluded that enhanced cleanliness of the UltraClean point-of-use filter contributed significantly to overall reduction of critical line/space layer bridge defects.

9779-67, Session PS2

## Chemical trimming overcoat: an enhancing composition and process for 193nm lithography

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As the critical dimension of devices is approaching to the resolution limit of 193nm photo lithography, multiple patterning processes have been developed to print smaller CD and pitch. Multiple patterning and other advanced lithographic processes often require the formation of isolated features such as lines or posts by direct lithographic printing. The formation of isolated features with an acceptable process window, however, can pose a challenge as a result of poor aerial image contrast at defocus. Herein we report a novel Chemical Trimming Overcoat (CTO) process as an extra step after lithography that allows us to achieve smaller feature size and better process window.

9779-68, Session PS3

## Novel neutral underlayer materials to enhance the photolithography performance and defectivity for chemo-epitaxy process

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Directed Self-Assembly (DSA) process with the block-co-polymer (BCP) is one of the attractive processes for creating the very fine pitch pattern.

These BCP pattern are changing the ratio of polymerization unit. Since alignment of BCP is affected by surface energy of the under layer, it is important to control the surface energy of the neutral under layer (NL) to get the perpendicularly alignment pattern. BCP pattern on the flat NL shows random alignment like the finger-print. Therefore, we need to perform the several processes to get target pattern like Line or Contact hole. There are 2 type flows in these processes that are Grapho-epitaxy flow and Chemo-epitaxy flow. Photo-lithography is applied in both flows; for the guide pattern in Grapho-epitaxy flow, and the etching mask of NL or cross-linkable polystyrene layer (XPS) in Chemo-epitaxy flow. In generally, Grapho-epitaxy flow is used to shrink the contact hole pattern and Chemo-epitaxy flow is applied to make the line and space pattern. To get smaller aligned pattern of BCP, it is necessary to apply very fine guide pattern and etching mask. And, BCP pattern is aligned along the guide pattern. In these flows, photoresist is coated on the NL or XPS. From these reason, these under layers are necessary to get the good photo-lithography performance of the photo resist.

In this study, we will report the specially designed NL materials which have the capability to enhance the photo-lithography performance for the good alignment performance of BCP and reduce the defectivity after chemo-epitaxy process. In order to enhance the photo-lithography performance, we made the new polymer that is contained the chromophore to controlled the n/k value and adhesion unit with the photo resist. The surface energy of this material was the neutral for BCP by controlling the ratio of chromophore and adhesion unit. The defectivity was reduced by optimized materials. We can control the n/k value to reduce the reflectivity from the resist bottom and achieve good adhesion with the photo resist pattern. The surface energy of this new material keeps neutral property for BCP. Since this material has the above properties, it shows good perpendicularly alignment pattern of BCP and photo-lithography performance.

## 9779-69, Session PS3

## Phase field mapping for accurate, ultrafast simulations of directed self-assembly

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Block copolymer thin films are a versatile platform for nanoscale patterning. By selecting parameters such as confinement shape and size, wetting conditions, and polymer composition variables such as chain architecture, molecular weight and block fractions, copolymer systems can self-assemble into a wide variety of 10 nm scale ordered structures. Exploring this expansive design space is key to a number of applications. In particular, in directed self-assembly (DSA), block copolymers are used in tandem with conventional lithography to increase the resolution of features in semiconductor devices.

A wide range of models and simulation techniques have been applied to the study of block copolymer assembly. Of these, self-consistent field theory (SCFT) is among the most successful and shows strong agreement with experimental results. Although SCFT is accurate, it is computationally expensive; parameter sweeps and accessible system sizes are limited by the availability of high performance computing resources. There is a significant need for a faster, but still accurate, coarse-grained model.

Phase field (PF) models are a promising approach. Because they numerically resolve only d spatial dimensions rather than the (d+1) dimensions of SCFT, PF simulations can potentially enable a speedup of two orders of magnitude relative to SCFT. Well-known PF models for diblock copolymers include the Landau-Brazovskii (LB), Ohta-Kawasaki (OK) and generalized Ohta-Kawasaki (gOK) models. These models express the system's free energy as a functional of the local species density through an asymptotic expansion about the disordered state. This expression is an approximation of SCFT; however, controlling the validity of the approximation is presently more of an art than a science. We have shown previously that when the segregation strength ?N exceeds 15 or so, existing PF models exhibit both quantitative and qualitative failures in their predictions.

To address these issues, we introduce a force- and stress-matching procedure to systematically map an "exact" model (SCFT) onto an optimized phase field (OPF) model. The optimized models resolve important shortcomings in their predictions. In particular, Figure 1 shows that the domain spacing predicted by our optimized model is a marked improvement over the original across a wide range of segregation strengths. We further present evidence that defect states and energies in bulk block copolymers are also accurately predicted by the OPF models.

In copolymer films in confined templates, we compare the predictions of the OPF models with SCFT for commensurability effects, defect states and energies. We further explore the transferability of a bulk OPF model with optimized parameters determined by a single bulk SCFT simulation into a confined DSA template using no additional parameters. Timing results are presented for side-by-side SCFT and OPF simulations conducted on large templates in the same code base. Thanks to these significant improvements, we anticipate that OPF models are quickly approaching a state suitable for accurate, rapid prototyping of large and geometrically complex DSA templates.

## 9779-70, Session PS3

## Filtration on block copolymer solution used in directed self-assembly lithography

Toru Umeda, Nihon Pall Manufacturing Ltd. (Japan); Shuichi Tsuzuki, Nihon Pall Ltd. (Japan)

Directed self assembly lithography (DSAL) is studied actively as a candidate for next generation lithography. Since materials employed in DSAL are considerably different from conventional chemically amplified resists, an independent study on the filtration should be conducted. We have investigated the block copolymer (BCP) filtration in terms of its impact on the polymer characteristics and gel/metal reduction[1-3]. As shown in Table 1, molecular weight of the block copolymer used in DSAL resist is substantially larger than conventional chemically amplified resists (CAR). It can be anticipated that aggregated gels of low solubility molecules should be produced easily with the high molecular weight polymer due to its limited solubility. In fact, gel particles are reported as the predominant defects in BCP layer in a DSAL processes [4]. In photoresists, removal efficiency for the gels is known to highly depend on the filtration materials [5]. We have examined this dependency on the BCP solution and will report in this paper.

Using a static pressure filtration test-stand shown in Figure 1, effluents of the 1.5% PS-b-PMMA (Mw=35000-b-37000) BCP in propylene glycol monomethyl ether acetate (PGMEA) were collected. The "test filters" used are 2 nm rated high density polyethylene (HDPE) filter, 10 nm rated nylon 6,6 filter and 20 nm rated poly tetra fluoroethylene (PTFE) filter. To evaluate the cleanliness of the obtained effluents, the collected effluents were filtered using a "standard filter", which is a track etch membrane with 30 nm pores. The clogging of the standard filter should depend on the amount of gels in the test filter effluents. Then, a resistance coefficient in the Darcy's law is calculated as a degree of clogging for the standard filter. Equation (1) is the Darcy's law, which is a fundamental relationship among each component in filtration.

dP=k?Q/A (1)

Where: dP=differential pressure of the filter(Pa), k=flow resistance coefficient(m-1), ?=fluid viscosity(Pa?sec), Q=flow rate(m3/sec) and A=filter area(m2)

Figure 2 shows resistance coefficient of the standard filter vs. throughput. Smaller k indicates lower degree of standard filter clogging, i.e. small amount of gels are in the test filter effluent.

As a result, 10 nm rated Nylon 6,6 filter best reduced gels. Since filter ratings such as 2 nm and 10 nm indicate sieving performance of the filter without adsorption, the better gel removal efficiency of the 10 nm filter than the 2 nm filter may indicate gel removal in the BCP solution is enhanced with some adsorption by the Nylon 6,6 filter material.

Based on the results, Nylon 6,6 filter is found to be a good filter for gel removal in the PS-b-PMMA BCP solution. For this BCP solution, filter rating is not the only indicator of the filtration performance but also an adequate membrane material selection should provide significant defect improvement.

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9779-71, Session PS3

## Contrast enhanced diffusion NMR (CEDOSY): quantifying impurities in block copolymers for DSA

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Block-copolymers offer a method to meet the demands of next generation lithographic materials as these materials can self-assemble into scalable and tailorable nanometer scale patterns. In order for these materials to find wide spread adoption many challenges require attention including reproducible self-assembled patterns, for which the purity of block copolymers is critical. Despite the well-controlled reactions used to access block copolymers the reaction conditions used to generate these materials may also introduce homopolymer impurities from a variety of sources and will lead to dramatic impacts in directed self-assembled patterns. Detection of these homopolymer impurities can be challenging for traditional methods of polymer characterization such as gel permeation chromatography (GPC) and 1H-NMR or tedious for more specialized methods of characterization like adsorption based high performance liquid chromatography (HPLC). We will discuss a straight forward NMR based method for the detection of homopolymer impurities in block copolymers – contrast enhanced diffusion NMR (CEDOSY). Conventional diffusion NMR methods, while effective at resolving chemical mixtures, experience difficulties in resolving polymeric mixtures when the resonances of polymer impurities overlap or the impurities are of a similar size to the block copolymer. By taking advantage of the chemically distinct blocks the formation of micelles (or aggregates) can be promoted for the block copolymer by the addition of a co-solvent that allows the impurity to remains as a unimer in solution. This greatly enhances the contrast between the diffusion coefficients of the homopolymer and block copolymer in mixtures and enables the resolution of homopolymer impurities. This technique was found effective at resolving impurities in both first generation poly(styrene)-b-poly(methyl methacrylate) (PS-b-PMMA) systems as well as second generation high ? systems. CEDOSY studies of PS-b-PMMA contaminated with PMMA homopolymer found the limit of detection was below 0.25 wt.% (Mw=2000 PMMA) and this method was effective over a range of PMMA molecular weights. Furthermore, studies that systematically varied the amount of impurity found that calibration curves could be generated to determine the amount of impurity at a given molecular weight. Additional efforts are focused on determining the molecular weight of the impurity a priori.

9779-72, Session PS4

## Gold-polymethylmethacrylate (Au-PMMA) composite resist system: novel bottom up approach for direct write micro/nano-scale gold structures by electron beam lithography

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This paper reports a novel Gold- Polymethymethaceylate (Au-PMMA) composite resist system, for direct write gold micro/nano-patterns using electron beam lithography technology. Composite resist was synthesized for the 10 and 15wt % of Gold precursor (HAuCl4: 3H2O) and PMMA in Ethyl Lactate. Resist composition and its structure were evaluated using FTIR, UV-Vis, and XPS technique. Elemental analysis of the resist films are carried out for the estimation of gold percentage in the resist film. Lithographic evaluation of the resist is carried out using E-Beam writer at 10 kV electrons by varying does from 100 to 900 μC/cm2. The presence of atomic gold at the e-beam exposed region after development is confirmed by Energy Dispersive X-ray Analysis. AFM investigations of the e-beam exposed pattern clearly indicated the minimum dose required for the formation of ~ 20 nm thin gold continuous structures is 700 μC/cm2.

9779-73, Session PS4

## Benzophenone doped PDMS composite resist: high-energy pulsed electron-beam lithography application

Madhushree G. Bute, Sanjay D. Dhole, Vasant N. Bhoraskar, Suresh W. Gosavi, Savitribai Phule Pune Univ. (India)

Electron beam lithography is an important technique in integrated circuit manufacturing, especially for making lithography mask of micron and submicron dimension. It cannot be used efficiently for mass production because of its low throughput. In order to increase throughput of this technique, scientist are engage in improving the sensitivity of resist material and/or improving the lithographic exposure system using multielectron beam lithography approach for pattern transfer. On the contrary multielectron beam lithography system has got its limitation due to e-beam current to get sufficient dose, therefore more attention has been given on development of high sensitivity self developable resist.

Very few groups around the world are engage for the development of dry resist using plasma processes. Even though high sensitivity self developable resist is well reported, so far these processes are not commercialized. Therefore, more emphasis has been given on improved wet resist with high resolution and sensitivity. Various methodologies such as copolymerization and doping of electronegative group (sensitizer) in host polymer matrix have been suggested.

In the recent past PDMS materials has got technological importance, and mainly explored for microfluidics and Lab-On-Chip (LOC) applications. A well developed soft lithography technology is mostly used for transferring the microstructure in PDMS, wherein the master mould is prerequisite. Long processing time and requirement of state-of-art microfabrication facility, to fabricate master mould introduces the technological limitations on fast prototyping.

Since the technique introduced and used for the present case is independent of the master mould, fast prototyping can be achieved with an advantage of fast response to requirement of changing geometries in the desire application. The technique demonstrated in the present work would be another parallel approach for mass production using large area high energy unconventionally used e-beam system.

In the present case a fast single step 6 MeV e-beam lithography process is developed for the micropatterning of the doped PDMS. This is the first report of “e-beam lithography in normal ambience”. We have successfully demonstrated the microstructure fabrication on the PDMS using this technique in 5 minutes. A freestanding metal mask of 500 μm thickness, containing desired pattern which is an array of 200 μm diameter holes having spacing of 100 μm in between them, is positioned over the doped PDMS sample in direct contact mode and 6 MeV e beam is used with the dose in the range of 64-640 μC/cm2 which is less than the previously reported 100 μC/cm2 to 20 mC/cm2. The optimization of the benzophenone concentration in PDMS is formulated on the basis of surface roughness and optical transparency of the fabricated microstructure. The benzophenone concentration and dose are the governing factors of the roughness. The optimum concentration of benzophenone is observed to be 3%. Further for this optimized benzophenone concentration doped PDMS; the effect of dose variation on the morphology of microstructure is also investigated.

9779-74, Session PS4

## mr-PosEBR: a novel positive-tone resist material for high-resolution electron-beam lithography

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Electron-beam lithography (EBL) evolved to one of the most important nanofabrication techniques as it enables the reliable generation of arbitrary two-dimensional patterns with lateral resolution down to the nanometer scale [1]. One of the most widely used high resolution EBL resist materials is high molecular weight poly(methyl methacrylate) (PMMA) [2]. However, PMMA only provides limited performance in terms of sensitivity and etch resistance. The resist's low sensitivity results in higher doses and concomitantly in longer exposure times which is unfavorable for high throughput and large area applications. The low plasma etch resistance of PMMA is the second main disadvantage, hampering the efficient pattern transfer into the underlying substrate by a subsequent plasma etch process. Alternative positive tone EBL resists either suffer from supplying difficulties, prices in constant increase or resist residues after development [3].

Herein, we present the results of a systematic material development study carried out in order to obtain a positive tone resist for high resolution EBL that circumvents the aforementioned obstacles. Several acrylic copolymer materials with different mass fractions of the comonomers, different molecular weights and similar molecular weight distributions were synthesized and – as resist solutions – evaluated in terms of EBL performance such as sensitivity, resolution and etch resistance. The resist material exhibiting the best combination of the desired properties, mr-PosEBR, is two times more sensitive than PMMA and performs comparably to the known high resolution resist ZEP-520A [4]. For example, a grating pattern with single pixel lines with a period of 100 nm could be lithographically generated into films of mr-PosEBR with an area dose of 100 μC/cm2 (line dose 250 pC/cm , film thickness 320 nm, acceleration voltage 30 kV). In terms of resolution, single lines (Cr/Au) of only 35 nm width could be fabricated via lift-off using 100 kV EBL. Furthermore, the dry etch stability of mr-PosEBR in a CF4/SF6 process is similar to the one of ZEP-520A (etch rates mr-PosEBR: 190 nm/min, ZEP-520A: 150 nm/min, silicon: 440 nm/min). Consequently, high resolution nano patterns in mr-PosEBR could be smoothly transferred into the underlying Si substrate with high fidelity.

Hence, mr-PosEBR is a promising novel positive tone resist for electron-beam lithography because it is highly sensitive, can be patterned with high resolution on the nanometer scale, and exhibits a significant dry etch resistance.

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9779-75, Session PS5

## Process integration of metal oxide based photoresist

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Inpria continues to pioneer a novel approach to EUV photoresist, incorporating high EUV absorbing metal oxide centers in an organic matrix. Inpria Gen2 photoresist are capable of 10nm half-pitch resolution and exhibit high etch resistance arising from conversion to metal oxide during processing. The solutions are cast in common organic solvents and we have previously demonstrated basic compatibility with CLEAN TRACKTM LITHIUS ProTM-EUV coater/developer systems (Tokyo Electron Limited). In this paper, we extend the collaboration further to more deeply address contamination concerns. We demonstrate reduction in trace metal contamination and particles in solution, leading to greatly improved defectivity on wafer. Concerns about process module contamination are also addressed. In addition, we discuss data on film thickness uniformity and etch selectivity.

9779-76, Session PS5

## Spin-on-carbon hard masks utilizing fullerene derivatives

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Spin-on-Carbon (SoC) hardmasks are an increasingly key component of the microchip fabrication process. Progress in lithographic resolution has made the adoption of extremely thin photoresist films necessary for the fabrication of "1x nanometre" linewidth structures to prevent issues such as resist collapse during development. While there are resists with high etch durability [1], ultimately etch depth is limited by resist thickness. A possible solution is the use of a multilayer etch stack. This allows for considerable increase in aspect ratio. For the organic hard mask base layer, a carbon-rich material is preferred as carbon possesses a high etch resistance in silicon plasma etch processes. A thin silicon topcoat deposited on the carbon film can be patterned with a thin photoresist film without feature collapse, and the pattern transferred to the underlying carbon film by oxygen plasma. This produces high aspect ratio carbon structures suitable for substrate etching. In terms of manufacturability it is beneficial to spin coat the carbon layer instead of using chemical vapor deposition [2], but the presence of carbon-hydrogen bonds in typical spin-on-carbon leads to line wiggling during the etch (a significant problem at smaller feature sizes). We have previously introduced a fullerene based SoC and reported on material characterization [3,4,5]. The materials low Ohnishi number provides high etch durability and the low hydrogen level allows for high resolution etching without wiggling.

The use of the materials in such etch stacks is demonstrated (figures 1-3). A 20nm thin silicon film was sputtered on top of the carbon layers. Resist patterns are defined by e-beam, and in the case of figure 2, EUV lithography and transferred to the silicon thin film using SF6/CHF3 etch chemistry. The carbon layer was then etched by O2 plasma using the silicon mask and finally the pattern was transferred into the silicon substrate using the same process used to etch the topcoat.

Recent advances in material development and work towards commercialization of the materials will be reported.

Some results from external evaluations of the original 100 series will be presented, together with recent developments with the newer 200 and 300 series formulations (offering improved thermal stability and etch durability).

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9779-77, Session PS5

## Helium ion beam lithography using inorganic HafSOx resist

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Due to the negligible proximity effect benefited from the weak spatial scattering of Helium ions, Helium ion beam lithography (HIBL) has become a promising alternative lithography technique with the capacity of fabricating high-resolution and high-density patterns. Nevertheless, hindered by its limited accessibility?only limited work, including the resist development has been done to optimize the whole lithographic system. HafSOx, as a negative-tone inorganic resist for applications in both e-beam lithography (EBL) and extreme ultraviolet lithography (EUVL), has been demonstrated with high resolution, moderate sensitivity (~400 μC/cm2 for EBL and ~10 mJ/cm2 for EUVL) and low line-edge roughness (LER). HafSOx thin films can be easily deposited by spin-coating a cluster-based solution prepared by simply dissolving HfOCl2, H2O2 and H2SO4 into water at a certain ratio. In this study, the helium ion beam (30keV) was used to test the performance of the HafSOx resist. A sensitivity of 4 μC/cm2 at D50 has been achieved and it stands as one of the best sensitivity for negative-tone resists using HIBL as shown in Table 1. Compared with its EBL and EUVL sensitivity, we found a Helium ion is 50 times and 10 times more efficient than electrons and EUV photons respectively in terms of activating the HafSOx resist. Overdosed patterns have been observed with the substantial inflation of the thickness due to possible Helium bubble formation mechanism after Helium ions obtaining electrons produced inside the resist. The critical dimension has also been tested with sub-15 nm lines achieved. Thickness, stoichiometry and density information has been collected from ellipsometry, atomic force microscopy (AFM) and Rutherford backscattering spectrometry (RBS). Supported by those data, a theoretical simulation, using SRIM (the Stopping and Range of Ions in Matter), of Helium ion interaction with the HafSOx resist has been implemented and we found the ionization accounts for the 93% energy loss and one Helium ion can roughly produce 260 secondary electrons with the assumption of 5 eV as the average secondary electron energy.

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9779-78, Session PS5

## Fundamental aspects of a new process of high-resist sensitization by the combination lithography of EB/EUV pattern exposure with UV flood exposure of photosensitized CAR and non-CAR

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In EUV lithography (EUVL), the most critical issue has been low intensity of the EUV light source.

Light-source intensity and resist sensitivity have a complementary relationship. Therefore, the sensitization of EUV resist is very important to compensate the low intensity of the EUV light source.

However, dramatically improving the resist sensitivity of chemically amplified resist (CAR) is very difficult because of so-called trade-off relation among the resolution, line-width roughness, and sensitivity. Therefore, we propose a very new process: high resist sensitization by the combination lithography of EUV pattern exposure with UV flood exposure (PF combination lithography). The present paper describes the fundamental aspect of detailed reaction mechanisms and patterning of a new process of high resist sensitization by PF combination lithography for high volume manufacturing. The relation of resist sensitization with resolution and roughness including photon shot noise problem will be discussed based on experimental results and reaction mechanisms in comparison between CAR and non-CAR. Especially a very severe problem about the relation of very high resist sensitization with photon shot noise for the high resolution contact hole patterning less than 20 nm will be discussed based on experimental results and reaction mechanisms of CAR and non-CAR.

9779-79, Session PS5

## EB and EUV lithography using inedible cellulose-based biomass resist material

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An inedible cellulose-based biomass resist material instead of alpha-linked disaccharides in sugar derivatives that compete with food supplies was developed by replacing the hydroxyl groups in the beta-linked disaccharides with EB sensitive 2-methacryloyloxyethyl groups. The 75 nm line and space width, and little footing profiles of Cellulose-resist on hardmask and layer were resolved at the doses of 19 μC/cm2. The resolution of line pattern in Cellulose-resist with beta-linked polysaccharide was improved compared with the referenced water-developable resist material derived from sugar derivatives with alpha-linked polysaccharide.

9779-25, Session 8

## Toward sub-20nm pitch FinFET patterning and integration with DSA

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Directed Self Assembly (DSA) has gained increased momentum in recent years as a cost-effective means for extending lithography to sub-30nm pitch, primarily presenting itself as an alternative to mainstream 193i pitch division approaches such as SADP and SAQP. Towards these goals, IMEC has excelled at understanding and implementing directed self-assembly based on PS-b-PMMA block co-polymers (BCPs) using LiNe flow [1,2]. These efforts increase the understanding of how block copolymers might be implemented as part of HVM compatible DSA integration schemes.

In recent contributions, we have proposed and successfully demonstrated two state-of-the-art CMOS process flows which employed DSA based on the PS-b-PMMA, LiNe flow at IMEC (pitch = 28 nm) to form FinFET arrays via both a ‘cut-last’ and ‘cut-first’ approach. [3,4] Therein, we described the relevant film stacks (hard mask and STI stacks) to achieve robust patterning and pattern transfer into IMEC’s FEOL device film stacks. We also described some of the pattern placement and overlay challenges associated with these two strategies.

In this contribution, we will present materials and processes for FinFET patterning and integration towards sub-20 nm pitch technology nodes. This presents a noteworthy challenge for DSA using BCPs as the ultimate resolution for PS-b-PMMA may not achieve such dimensions. Our paper will emphasize patterning approaches, wafer alignment strategies, the effects of DSA processing on wafer alignment and overlay, as well as the resulting CD uniformity of our FinFET arrays.

9779-26, Session 9

## Integration of SIS smoothed DSA line patterns: challenges, solutions and impact on defectivity

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Directed self-assembly (DSA) of block copolymer (BCP) systems can be used to form patterns useful in lithography, especially lines and spaces with lamellar phase systems and vias/pillars with cylindrical phase systems. However, most BCP systems with attractive pattern formation capabilities have limited plasma etch contrast between the polymer domains. One potential solution to greatly enhance this etch contrast is a technique called sequential infiltration synthesis (SIS). In SIS, organometallic (OM) precursor vapours and oxidants are sequentially introduced into self-assembled block copolymer systems in multiple cycles. Thus, the polymer pattern is transformed into a metallic mask with much enhanced plasma etch contrast. We have previously reported that such a block-selective SIS of alumina in lamellar phase PS-b-PMMA can be used to control line width and also significantly smoothen the line edge roughness (LER) and line width roughness (LWR) of the BCP lines [1].

In this work, we report our results with transferring these smoothed alumina lines into silicon using various BARC/hard mask stacks and the impact on line roughness during the pattern transfer process. In particular, we address the unique challenges associated with integrating SIS with chemo-epitaxial DSA and how process choices and material selection may be used to tackle these challenges. Finally, we investigate the impact of the SIS process on pattern defectivity.

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9779-27, Session 9

## Directed self-assembly of PS-b-PMMA with ionic liquid addition

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Directed self-assembly (DSA) of block copolymers is a promising candidate to address grand challenges towards new generations of low-cost, high-resolution nanopatterning technology. Over the past decade, poly(styrene-b-methyl methacrylate) (PS-b-PMMA) has been the most popular block copolymer applied in this area. However, further scaling towards pitches below 20 nm is hindered by its relatively low segregation strength between constituent blocks, characterized by a low Flory-Huggins interaction parameter, $\chi$ ( ~ 0.038 for PS-b-PMMA at r.t). To reach sub-10 nm feature dimensions, many high-$\chi$ block copolymer materials and processes are currently being studied. For many such systems, moving to processing strategies that are less manufacturing friendly than thermal annealing with a free surface is required, for example solvent annealing or thermal annealing with a top coat. Here we investigate the DSA of PS-b-PMMA with blended ionic liquid (IL) on chemically-patterned substrates via thermal annealing with a free surface. This materials system is attractive because with low volume fraction IL it exhibits a substantially higher–$\chi$ than the pure block copolymer, yet the change in surface and interfacial properties are manageable in the sense that poly(styrene-random-methyl methacrylate) brushes may be used to control substrate wetting behavior, and the blend could be assembled using thermal annealing with a free surface. In other words, PS-b-PMMA/IL may serve as a high-$\chi$ drop-in replacement for PS-b-PMMA. In this work, we assess the thermodynamics and kinetics of assembly of PS-b-PMMA/IL blends, and pattern transfer, for two complementary purposes: 1) to delineate the impact of $\chi$ on line-edge roughness by comparing the assembly of PS-b-PMMA with and without IL addition, and 2) to provide key DSA results to determine if PS-b-PMMA/IL blends would offer a solution for sub-10 nm lithography.

9779-28, Session 10

## An improved method for characterizing photoresist lithographic and defectivity performance for sub-20nm node lithography

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The overall quality and processing capability of lithographic materials are critical for ensuring high device yield and performance at sub-20nm technology nodes in a high volume manufacturing environment. Insufficient process margin, high line edge roughness and mask error enhancement factor cause poor manufacturing control, while high defectivity causes product failures.

In this paper, we will focus on the most critical layer of a sub-20nm technology node LSI device, and present an improved method for characterizing both lithographic and post-patterning defectivity performance of state-of-the-art immersion photoresists. Multiple formulations from different suppliers were used and will be compared.

Photoresists will be tested under various process conditions (e.g. thickness, bake temperatures), and multiple lithographic metrics will be investigated (depth of focus, dose latitude, line edge roughness, MEEF, bridging margin, collapse margin, etc.). Results were analyzed and combined using an innovative approach based on advanced software, providing clearer results than previously available. This increased detail enables more accurate performance comparisons among the different photoresists. Post-patterning defectivity was also quantified, with defects reviewed and classified using state-of-the-art metrology tools.

Correlations were established between the lithographic and post-patterning defectivity performances for each material, and overall ranking were established among the photoresists, enabling the selection of the best performer for implementation in a high volume manufacturing environment.

9779-29, Session 10

## Research on topcoat-less photoresist characteristics for high scan speed ArF immersion exposure tool

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Topcoat-less photo resist is getting popular to reduce process step and material cost at below 20nm memory device.

The compatibility between topcoat and ArF immersion can be ignored by using topcoat-less photo resist, therefore it has the benefit to improve process margin, line width (edge) roughness and etch selectivity easily.

There are a lot of parameters, which have been investigated on, to develop the topcoat-less photo resist such as leaching, dynamic contact angle, defectivity controllability and even scan speed of wafer stage in ArF immersion exposure tool. However, optimum dynamic contact angle hasn't been defined yet for high scan speed immersion tool, ≥ 800mm/sec, to increase throughput.

It's well known that receding angle of topcoat-less resists should be

72-75˚for ArF immersion tool which has 600mm/sec scan speed. But there is no suitable suggested contact angle for more than 800mm/sec scan speed.

In this paper, we have tried to find out optimum parameters, like static contact angle, advancing contact angle, receding contact angle, etc for high scan speed immersion tool and show our results to improve line width(edge) roughness of topcoat-less resists.

9779-30, Session 10

## CD-bias control on hole pattern

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Gridded design rules is major process in configuring logic circuit used 193-immersion lithography. In the scaling of grid patterning, we can make 10nm order line& space pattern by using multiple patterning techniques such as self-aligned multiple patterning (SAMP) and litho-etch- litho-etch (LELE). On the other hand, Line cut process has some error parameters such as pattern defect, placement error, roughness and X-Y CD bias with the decreasing scale. Especially roughness and X-Y CD bias are paid attention because it cause cut error and pattern defect. In this case, we applied some smoothing process to care hole roughness. Each smoothing process showed different effect on X-Y CD bias.

In this paper, we will report the pattern controllability comparison of trench and block + inverse. It include X-Y CD bias, roughness and process usability. Furthermore we will discuss optimum method focused on X-Y CD bias when we use additional process such as smoothing and shrink etching .

9779-31, Session 10

## High-speed AFM studies of 193 photoresist during TMAH development

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In this paper we investigated the dynamic process of resist development in real time. Using High Speed – Atomic Force Microscopy (HS-AFM) in dilute developer solution, changes in morphology and nanomechanical properties of patterned resist were monitored. The Bruker FastScan AFM was applied to analyzed acrylic-based polymer resist in developer. HS-AFM operated in PeakForce mapping mode allowed for concurrent measurements of resist stiffness, adhesion to AFM probe and deformation during development. HS-AFM data revealed detailed information about initial resist morphology, followed by a swelling process and eventual dissolution of the exposed resist areas. Each image capture presents data of the physical state for both exposed and unexposed regions of the resist. Such a visual observation of the actual pattern formation of resists during development (chemical effects) will help advance in resist chemistry and design. HS-AFM showed potential for tracking and understanding development of patterned resist films and can be useful in evaluating the dissolution of different resist designs.

9779-32, Session 10

## LER and LWR smoothing by ion implantations from post-litho to post-etch

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The line edge roughness (LER) is a critical yield-limiting factor in the fabrication of semiconductor devices. For the success of the 10-nm technology node and below, LER should be mitigated as much as possible. There are many methods for the mitigation of LER, such as ion implantation, etch trim, resist reflow, etc [1-3]. Among these methods, ion implantation shows promising LER reduction results, with up to 30% LER reduction and minimal CD loss [1]. However, some metrics were absent in Ref. [1], for example, tip-to-tip, tip-to-side, corner rounding, cross-section analysis, etc.

The purpose of this paper is to further investigate the LER smoothing capability of the ion implantation technique. The ion implantation will be tested on the optical LELELE and SADP processes. A comprehensive evaluation including litho to etch, line and space, tip-to-tip, tip-to-side, corner rounding, and cross-section image will be conducted.

As shown in Fig. 1, 19% LER and 16% LWR reduction for the line and space pattern from post litho to post ion implantation has been achieved. Fig. 2 shows the post litho and post ion implantation CD-SEM images for a cross target. It is clear that there is no significant change in terms of corner rounding. Other data is in progress.

9779-33, Session 11

## High-chi block copolymer DSA to improve pattern quality for FinFET device fabrication

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Directed self-assembly (DSA) with block-copolymers (BCP) has been proposed as a lithography extension technique to continue semiconductor scaling below the resolution limits of 193 immersion or extreme ultra-violet lithography. Sub-30nm pitch pattern generation with PS-b-PMMA DSA has been widely studied and FinFET device fabrication with DSA-patterned fins has been demonstrated [1, 2]. Recent progress with BCP material development has even extended the pattern-transferred pitch to the sub-20nm range [3].

Pattern quality for DSA features, such as line edge roughness (LER), line width roughness (LWR), size uniformity, and placement, is one of the key questions for DSA manufacturability. Continued scaling with PS-b-PMMA becomes more challenging as the polymer chain length approaches the

lower limit for phase separation. Switching to higher chi BCP systems promises stronger phase separation and, therefore, sharper material boundaries. However, processing, DSA, and etch transfer of such higher chi BCP systems can lead to more complex processing and/or even higher LER/LWR due to lack of a robust etch transfer process compared to PS-b-PMMA.

In this work, we compare pattern quality between DSA line-space patterns formed using various BCP systems. Line-space grapho-epitaxy results at 24nm pitch confirm good DSA quality and improved low frequency LER/LWR. Figure 1 shows a comparison of line-space patterns at 24nm pitch with one phase of the BCP removed and subsequently etch-transferred into a thin hard mask layer. The high-chi polymer at 24nm pitch yields superior line quality compared to PS-PMMA. Figure 2 shows the LER and LWR power spectral density of the images in Figure 1 and confirms that patterning with high chi polymer reduces low frequency components for both LER and LWR. Silicon containing BCPs are promising material candidates for scaling below 20nm pitch. Figure 3 shows pattern transfer of a PS-PDSS (poly-styrene-blockpentamethyldisilylstyrene) fingerprint pattern at 20nm pitch, demonstrating the potential of low LER/LWR patterning with good etch-transfer budget.

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9779-34, Session 11

## High-chi block copolymers based on chemical modification of poly(t-butyl acrylate) containing block copolymers

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The development of new block copolymer (BCP) materials with higher chi-parameter and narrow polydispersity is critically needed for the advancement of directed self-assembly (DSA) applications. Our approach is to chemically convert the poly(t-butyl acrylate) (PtBA) containing block in PS-PtBA block copolymer (BCP) precursors to increase the chi-parameter of BCPs. We took the advantage of the narrow molecular weight distribution of the PS-PrBA BCP precursors for the preparation of the well-defined BCP materials with high and tunable chi values. A wide range of fluorinated alcohols were investigated to introduce a fluorinated acrylate-block to the PS-block for the enhancement of the BCP chi-parameter. It is important to mention that the issues of neutral surface become even more problematic than the PS-PMMA system, since the surface energy difference between the two blocks becomes more pronounced when the chi-parameter of BCP materials increases. The parallel orientation of block copolymers for those BCPs with high chi is thermodynamically favored, because there exists much stronger tendency for the low surface energy block trying to cover the surface (i.e. interface between air and polymer films.) Therefore, it is desirable to consider and develop a “PS-PMMA like” high and tunable-chi block copolymer material approach, because industry is already familiar with the implementation of the DSA process on a wafer-scale platform.

A PS-PtBA was first synthesized to design a well-defined “mother” BCP with narrow molecular weight distribution via sequential anionic polymerization of styrene and t-butyl acrylate in tetrahydrofuran (THF), which was performed at ?78 °C under purified argon. A sec-butyllithium was used as an initiator. The chemically functional t-butyl units in the BCP can be exchanged to alcoholic units when the trans-alcoholysis reaction is optimized with an acid catalysis, and our chemical modification of the BCP was targeted at the PtBA block with fluorinated alcohols for the synthesis of PS-poly(fluoroalkylate). We discuss the synthetic route and characterization of the modified BCP consisting of PS and fluorinated polyarylate. The equilibrium period (or interlamellar spacings, L0) of the BCP was evaluated by the Small-angle x-ray scattering (SAXS) for a thermally annealed film, and the structural feature in thin films was measured by grazing incidence small-angle x-ray scattering (GISAXS). It was possible to tune the interaction parameter not only by choosing different fluorinated alcohols, but also by controlling the degree of substitutions of t-butyl groups with the fluorinated alcohols for the preparation of PS-partially fluorinated polyacrylate block copolymers. This clearly offers the flexibility and controllability of tailoring the interaction parameters while maintaining the narrow molecular weight distribution of the BCP materials for the advanced lithography applications.

9779-35, Session 11

## Carbohydrate-based block copolymer self-assemblies: sub-10nm highly nanostructured thin films and DSA patterning

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Current knowledge in modern molecular science allows for the preparation of a myriad of tailored nanomaterials, which play important and multifaceted roles in nanoscience and technology. Among the bottom-up strategies, self-assembly is an incredibly powerful concept in macromolecular engineering that offers an invaluable tool for the preparation of 2D and 3D discrete nanostructures, ranging from materials science to molecular biology, which are often not accessible by any other fabrication process. Indeed, the self-assembly paradigm in science has matured over the past two-decades to a point of sophistication that one can begin to exploit its numerous potentialities in nanofabrication. Using self-assembly as a synthetic tool, powerful chemistry and physico-chemistry protocols can be developed that are capable of organizing organic and inorganic building-blocks into unprecedented structures and patterns, over several length scales to create novel and innovative materials.

On the other hand, the constant desire of size reduction of integrated electronic devices, leads the semiconductor industry to develop processes, able to pattern materials at the nanometer scale. In this context, self-assembling copolymers are promising materials offering an alternative method to ArF immersion multiple pattering, EUV (Extreme ultraviolet) or e-beam lithography. However, to provide a competitive process, it is necessary to provide a full class of copolymers able to self-organize in a wide range of patterns size. Currently, one of the major challenges in this field is to find copolymers that could address sub_10 nm pattern size. The main challenge in this area is to reduce the copolymer chain length in order to bring the pitch below 15 nm, without losing the network self-organization. In this context and during the last decades, block copolymers (BCP) systems have received considerable attention as a promising platform for preparing nanometer-scale structures and materials due to their self-assembling nature into periodic domains whether in solution or solid states.

To date, numerous studies have been focused on the self-assembly of

petroleum-based BCPs for potential applications1 in multidisciplinary fields, such as nanoparticles for drug delivery, or nano-organized films for biosensors, or nanolithography, etc. Such materials are derived from fossil resources that are being rapidly depleted and have negative environmental impacts. In contrast, carbohydrates are abundant, renewable and constitute a sustainable source of materials. This is currently attracting much interest in various sectors and their industrial applications at the nanoscale level will have to expand quickly in response to the transition to a bio-based economy. The self-assembly of carbohydrate BCP systems at the nanoscale level via the bottom-up approach, has allowed only recently the conception of very high-resolution patterning (thin films with sub 10nm resolution)2-4 (see figure 1) as well as very high transistor memory performance5,6 that has never been attained to date by petroleum-based molecules and provides these new materials with novel properties.

We will in this paper present new and recent results on the self-assemblies of oligosaccharide-based block copolymer (particularly PI-MH, Polyisoprene-Maltoheptaose) leading to highly nanostructured thin films (sub-10nm resolution) using DSA approach in combination of solvent and/or thermal annealing (see figure 2).

9779-36, Session 11

## Design of new block-copolymer systems to achieve thick-films with defect-free structures for applications of DSA into lithographic large nodes

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The self-assembly of block-copolymers (BCP) is now established to be a straightforward technology to further decrease dimensional limits currently achievable by conventional lithographic tools. Indeed, the capabilities of these materials to form various self-assembled structures of different shapes and features of small sizes, make them very attractive for low-cost microelectronic patterning at high resolution.1

Due to several key-advantages of BCPs self-assembly properties for microelectronic applications (short bake times for the self-assembly process, scalable dimensions..), an early introduction of this technology into lithographic large nodes could be appealing for example in VIA interconnects patterning. In this particular case, the early industrialization of BCPs would require large periods/high molecular weights, like periods exceeding 50 nm. At this mesoscopic length-scale, some limitations for the self-assembly process appear due to the high molecular masses involved, leading to poorly-ordered structures for classical systems (miss-oriented features, highly defective films..). Moreover, aside of this specific behavior, the self-assembly step of the material should be kept within a reasonable process-window, i.e. below few minutes, to overcome a potential throughput issues of wafers. Additionally, the BCP's film-thickness (FT) with perpendicular features should also be sufficient enough2,3 (>50nm) to ensure a good control over the dry-etch transfer of the polymeric mask in the substrate. Taken together, these various conditions are extremely challenging to fulfill, and since even PS-b-PMMA BCPs -Polystyrene-block-poly(methyl methacrylate)- cannot overcome simultaneously the ones on both period and film-thickness (Figure 1), new systems and strategies must be developed to satisfy the whole set of requirements.

Among different approaches envisioned to solve this problem, it was shown that blending PS-b-PMMA BCPs with well-chosen additives can be a first answer to enlarge their accessible process-window and reach the specifications.4,5 However, it would be suitable to design new pure BCPs systems fulfilling naturally the targeted requirements, and benefiting the know-how processes and some of the properties of PS-b-PMMA BCPs.

In this contribution, we will present our studies on new BCPs systems based on PS-b-PMMA architecture synthesized thanks to Arkema's proprietary technology. These new materials are specifically designed to overcome the issues faced for early lithographic nodes. First, we will demonstrated that these systems present the same typical process-flow than classical PS-b-PMMA (same chemistry of neutral layer, no need for a top coat..). Afterward, we will show how these systems present structures with less defects than the ones achieved with the classical pure PS-b-PMMA (Figure 2), fulfilling thus the whole set of conditions specified for the targeted high-dimensions. Eventually, we will highlight through graphoepitaxy approaches as well as critical dimensions uniformity measurements and defects correlations, that the self-assembly properties of these new systems are better by far than the ones exhibited by classical pure PS-b-PMMA BCPs.

9779-37, Session 11

## Directed self-assembly materials for high-resolution beyond PS-b-PMMA

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Since the concept of directed self-assembly (DSA) emerged as an alternative patterning approach in semiconductor device fabrication, Poly(styrene-b-methyl methacrylate) (PS-b-PMMA) has been proven a relatively mature material platform in block copolymer patterning. A variety of DSA flows of both graphoepitaxy and chemoepitaxy schemes have been designed to form guiding structure for block copolymer to grow upon. As good examples of chemoepitaxy scheme, LiNe and SMART™ flows using PS-b-PMMA are widely investigated.[1-2] However, there have also been intensive discussions on its technical challenges (line edge roughness, and extendibility to resolution below 10nm half pitch, etc.), where further technical advance beyond PS-b-PMMA system is required in supporting the continuous scaling in IC device fabrications.

To address the challenging material requirements, we introduced a newly developed material platform of organic high-c block copolymers (AZEMBLY™ EXP PME-3000 series).[3] Without employing a topcoat and delicate solvent vapor annealing, vertically oriented polymer domains were successfully demonstrated with lamellae-forming high-chi block copolymers (L0 17 ~ 26 nm) in a reasonable time frame of self-assembly. It is notable that our in-house PS-r-PMMA underlayers (AZEMBLY™ EXP NLD series) are applicable for the high-chi block copolymer series, and subsequent pattern transfer can be achieved on widely adopted trilayer stacks as well. More importantly, L/S features of sub-10nm half pitch were successfully implemented with chemoepitaxy scheme, which confirmed that the high-chi block copolymers were highly compatible with the existing DSA flows enabled by 193i lithography and standard protocols.

Leveraging the process-friendly package of novel materials, we are striving to extend the potential of the high-chi block copolymer system as well as to improve the performance of existing DSA materials and processes. In this paper, a variety of high-chi block copolymers with lamellar and cylindrical morphologies covering a broad range of L0 are discussed, with improved etch selectivity and patterning performance beyond the scaling of PS-b-PMMA platform.

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9779-38, Session 11

## Access to 5nm features with DSA topcoat system

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New high ? block copolymers containing silicon in one block (Si-BCPs) have been synthesized and characterized. These materials can be oriented under process friendly conditions (annealing below 200˚C for ca. 60 sec.) using the top coat techniques previously described. Several systems that form lamella with differing pitch were synthesized by living polymerization initiated by sec-butyl lithium. The polymers were characterized by size exclusion chromatography and by small angle X-ray scattering (SAXS). Of particular interest are systems that generate crisply defined lamella forming lines and spaces of nominally 50 angstroms in line width. The ? value of this Si-BCP was extracted from scattering profiles by fitting to Leibler's mean-field theory. The measured ? value is 0.25, which is 5 times that of poly(styrene-b-methyl methacrylate) (PS-PMMA). This Si-BCP has high etch contrast due to the silicon containing block, which has enabled transfer of these very small images into an inorganic layer by reactive-ion etching (RIE).

9779-39, Session 11

## Formation of microphase-separated structure with half-pitch less than 5.0nm formed by multiblock copolymers for nanolithographic application

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It is well-known that block copolymers (BCPs) consisting of incompatible components form regular self-assembled structure, so-called microphase-separated structure. The phase-separated domains obtained by BCP self-assembly corresponds to the size of the polymer (degree of polymerization), which can be controlled during the synthesis of the constituent blocks. By using these characteristics of BCPs, the BCPs are considered to be utilized in many fields, e.g. material for bioscience, electric devices, chemical processing devices and lithography.

BCP nanolithography, also known as directed self-assembly (DSA), is an essential technology for next generation lithography to achieve the micro- and nano-patterning with low cost. A microphase-separated structure with the half pitch pattern formation around 10nm has been already accomplished to combine DSA with conventional lithography technique. The size and the resolution of the pattern are closely related to the size and chemical composition of the BCPs. The next target for the microscopic patterning using BCPs is to form the microphase-separated structure with the half pitch less than 10 nm.

We have successfully synthesized diblock copolymers with low molecular weight, and the obtained block copolymer has formed the definite microphase-separated structure with the half pitch of 5.5nm. However the formation of the microphase-separated structure with the half pitch less than 5.0nm by the same diblock copolymers should be difficult. Because since the interaction parameter, chi ($\chi$), of two blocks is relatively low, the BCPs tend to become miscible. So we suggested to synthesize BCP consisting of very strong segregated components and furthermore to use multiblock copolymers such as ABA-type and ABAB-type instead of the simple AB diblock copolymer to solve the problem.

Two kinds of BCP systems with very strong segregated components (high $\chi$) were used in this study, that is, polystyrene(S)-poly(4-hydroxystyrene)(H) system and poly(4-trimethylsilylstyrene)(Si)-poly(4-hydroxystyrene)(H) system. As multiblock copolymers, two kinds of BCPs were prepared, such as HSH triblock, SHSH tetrablock, and HSiH triblock copolymers, and so on. For example, a HSiH triblock copolymer with Mw=8,000, Mw/Mn=1.09 with composition of S, S=0.5, and SHSH tetrablock copolymer with Mw=27,000, Mw/Mn=1.02 with S=0.6 were synthesized. From the TEM observation of the casted film of the HSiH triblock copolymer and the SHSH tetrablock copolymer, alternating lamellar structures were clearly observed. Furthermore the period of the alternating lamellar structures of the SHSH tetrablock copolymer was estimated from SAXS measurements as 10.8nm (that means the half pitch of the lamellar structures is 5.4nm) .

In this study, multiblock copolymers with high $\chi$ with narrow molecular weight distribution were prepared using advanced large-scale living anionic polymerization technique, and using the BCPs the formation of the microphase-separated structure with the half pitch less than 5.0nm was observed by TEM and SAXS.

We will discuss further advancement of evaluation of multi block copolymers.

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9779-40, Session 12

## Novel pattern trimming and shrink material (PTM (PTD) and PSM (NTI)) for ArF/EUV extension

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In recent years, as next-generation lithography, various exposure techniques have been studied such as Extreme Ultraviolet Lithography (EUVL), Directed Self Assembly (DSA) and multiple patterning processes. In particular, EUVL is the most promising candidate for HVM below N7 node. However, there are many problems to be solved such as materials, through put of exposure tool and Mask defect. With respect to the DSA, the fine patterning with Block copolymer has been studied. But DSA process also has the several problems such as the complicated process flow in chemo process, quality of the Block copolymer and defect. On the other hand, although the multiple patterning has been applied device manufacturing for several years, there are some problems such as significant increase in cost due to increasing of the process steps and the overlay accuracy at the multiple process steps. Therefore, Pattern trimming materials (PTM) and Pattern shrink materials (PSM) were developed for miniaturization using the current exposure technology. PTM is applied on a resist pattern produced in a positive tone process and trim the resist pattern. PTM is possible to control the trimming amount by changing the formulation and the baking process. It has been confirmed that effectiveness of the PTM is not only for the LS patterns, but also for 2D pattern like dot pattern. At the same time, it is confirmed that PTM can improve the LWR and LCDU. On the other hand, PSM is applied on the pattern prepared in a negative tone developed process and then it can shrink the resist pattern after baking. We adopted new concept for pattern shrinkage process which dramatically improved LCDU with hole shrinkage. In this paper, we demonstrated L/S and dot pattern trimming by PTM and C/H shrink by PSM with immersion ArF condition and EUV condition. In the future, PTM and PSM are expected to be applied in not only ArF im patterning process but also in EUVL patterning process.

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9779-41, Session 12

## Trilayer rework optimization to overcome advanced technologies challenges

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The recent tendency to integrate analog Bipolar, Flash memory or photonics devices with a CMOS chip results in wafer surface with a vastly irregular topography. To overcome the problem of the resulting high planarization constraints and thin resist masking budgets, the use of trilayer within the lithography stack becomes necessary to enable this challenging pattern transfer. This trilayer is based on an organic planarizing layer (OPL), a Si-containing anti-reflection coating (SiARC) and a thin photoresist. The well-known benefit consists in the introduction of a Si-rich layer in-between the top photoresist and a carbon-rich OPL. It plays both roles of the anti-reflective and of the masking material to selectively etch the OPL under layer. During etching, OPL material thickness has to remain sufficient into non open areas to protect high topology structures such as memories, bipolar emitters or photonics devices. This requirement of maintaining sufficient OPL thickness is also the same for any trilayer rework applications. The preferred rework scenario is the removal of the entire trilayer with successive steps to sequentially strip off each layer selectively to the underneath etched material. Photoresist removal step uses a N2H2 based plasma to minimize impact to SiARC layer, especially with regards to material oxidation. To remove SiARC material, a fluorocarbon based chemistry is used with high temperature, RF power and pressure conditions. To strip OPL material, various chemistries can be used with O2 or N2 gas, depending on challenges to remove residues without damaging the underlying etched layer. These successive process steps are performed with a Lam GxT system with Multi-Station Sequential Processing architecture (see Figure 1). This system allows independent control of temperature, RF power and chemistry, enabling a lower cost option for sequential processing of a trilayer rework operation. In this paper, we investigated SiARC/OPL ashing selectivity and optimizing several process parameters (RF power, plasma chemistry, pressure, time per station). We show that the OPL profile, at the end of SiARC removal step, can be highly modified (see Figure 2). Hence without proper process optimization, higher topology structures could be dangerously uncovered by OPL and therefore damaged by the CF4 based plasma (see Figure 3). Moreover, it could lead to disturbing wafer non-uniformity in term of residues, oxidation or consumption of the underneath material to etch. Increasing process selectivity can be done at this step but the user must take care as this can lead to some parasitic effects. First, during processing a white “smoke” like discharge is generated above the wafer. A second observed effect is a white powder that gradually accumulated on the process chamber base and lid, requiring regular cleaning maintenance. Generated particles have been identified through FTIR and defectivity analysis and the two phenomenon have been demonstrated to have no correlation. This paper details both process and hardware solutions that have been investigated and characterized to have successfully overcome the parasitic effects of trilayer high selectivity rework process.

9779-42, Session 12

## Evaluation of water-based intelligent fluids for resist stripping in single wafer cleaning tools

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The usage of phase fluid based stripping agents to remove photoresists from silicon substrates was studied. Although the use of resists is very common, their successful integration often depends on the ability to remove the resist after certain processing steps. On the one hand the resist chemistry is changing during subsequent process steps that can cause a thermally activated cross-linking which increases the stripping complexity. Resist removal is also challenging after the formation of a hard polymer surface layer during plasma or implant processes which is called skin or crust. On the other hand the choice of stripping chemistry is often limited due to the presence of functional materials such as metals which can be damaged by aggressive stripping chemistries.

An alternative phase fluid based stripping chemistry known as lisoPUR© was investigated regarding its cleaning efficiency and material compatibility on 300mm silicon wafers in a fully automated CMOS environment at Fraunhofer IPMS-CNT. Phase fluids are liquid-liquid-based complex fluids based on micro emulsions. They are built up from dynamic and flexible plasmicells. The globular shapes of the fluid interact with each other and tend to change their forms within some milliseconds. Therefore phase fluids offer a new and innovative working principle: they are penetrating layers through smallest openings and lift off the material from the surface. The fluids have a high water share, work in a neutral pH range, are biodegradable and do not consist of aggressive ingredients which offers additional benefits in total cost of ownership.

In a previous evaluation the contamination behavior of the fluid itself and the proof of concept of this new working principle were investigated. Based on these results next steps were done to implement this new material into a state-of-the-art CMOS manufacturing pilot line. Implementing new materials requires high purity chemicals (VLSI grade) to reduce the contamination of particles and metal cations to a minimum. Additional purification steps in the fabrication of phase fluids have been developed to reduce metallic and ionic impurities to ppb level and release the new cleaning fluids for cleanroom handling. This was proven by analyzing the material itself and a 300mm bare Si wafer which was dispensed with lisoPUR© and a subsequent DI water rinse using an AMAT Raider SP. TXRF and vapor phase decomposition (VPD, IC-PMS) results show that required specification are fulfilled. Additionally, the authors show that a 450nm thick positive tone, chemically amplified resist (post coat, post development, and post etch) was able to remove with lisoPUR©. Therefore, a rinse sequence was developed based on a combination of water and SC1 which was subsequently applied to the phase fluid resist stripping step. Particle measurements using a KLA Tencor Surfscan SP2 and a randomly selected particle review using an AMAT Review SEM were done to evaluate the cleanliness of the wafer surface. Further investigations on the compatibility to different functional materials like copper, alumina and titan nitride were done to show the none aggressive behavior of intelligent fluids in applications such as stripping of resist from Cu seed layers.

9779-43, Session 12

## Novel ArF immersion extension technology by dry development rinse materials (DDRP) and materials (DDRM)

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ArF lithography is still the major process to develop N7/N5 devices. Especially in resist materials, DOF, roughness and CD uniformity are the biggest key parameters in fine pitches. To improve these issues, we newly propose to apply Dry development rinse process (DDRP) & materials (DDRM) as the ArF extension approach. In EUV lithography, DDRP has been widely investigated as one of the approaches to achieve the high

resolution. However, the performance of DDRP for ArF lithography was never demonstrated in detail. In this paper, we especially focus to improve DOF, CD uniformity and LWR by applying DDRP for the pattern of ArF immersion condition. For example, we succeeded to achieve 300% wider DOF, 170% wider EL and 20% better CER in 50nm dense C/H patterning compared with recent standard NTD process by applying DDRP. This new DDR technology can be the promising approach for ArF extension stages in N7/N5 and beyond.

9779-44, Session 12

## Additive chemistry and distributions in photoresist thin films

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The lithographic performance of photoresists is a function of the vertical distribution of formulation components, such as photoacid generator (PAG) molecules, in photoresist thin films and how these components undergo chemical modification and migrate within the film during the lithography processing steps. This presentation will discuss how GCIB-SIMS depth profiles were used to monitor the PAG and quencher base distributions before and after exposure and post-exposure bake processing steps for different PAG/photoresist formulations. The authors will also highlight the lithographic performance of Negative-tone Develop (NTD) resists and the correlation with vertical distribution of resist components. Also acid diffusion lengths will be extracted from the acid distribution before and after post-exposure bake. The figure below illustrates the PAG and quencher distributions in an NTD resist film.

9779-45, Session 12

## PVD prepared molecular glass resists for scanning probe lithography

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As semiconductor industry is in search of beyond CMOS devices with clear structures in the sub-10 nm range, scanning probe lithography (SPL) as well as extreme-UV and electron beam lithography (EBL) stand out as some of the most promising techniques for their manufacturing.1 These techniques require the fabrication of well-defined, amorphous and defect and pinhole-free films in a likewise nanometer thickness range. The use of classical polymeric photoresists however sets limits to the achievable resolution due to their large molecular size and polydispersity.2 An alternative resist material class are the so called molecular glasses (MG). These materials are organic molecules defined by a stable or metastable glassy state at room temperature. In comparison to polymers, they show a well-defined structure and a small molecular size as well as higher vapor-pressures and lower viscosities above their respective Tg.3 The patterning resolution can theoretically reach the size of molecular building blocks which are around one to two nanometer. However, the achievable resolution is dominated by the confinement of the lithographic reaction, defined by the applied patterning technique, patterning parameters, and additives, as well as film formation, glass temperature, etch resistance, etc.4 Recently published literature highlights the potential of MG but also addresses the need for additional research.2,5 As one of only few compounds, Calix[4] resorcinarene, has been intensively investigated as photoresist material. Positive tone patterning with closed-loop electric field SPL has shown high-resolution capability with sub-5nm patterns. Moreover, the combination of SPL with EBL in a mix and match type patterning process showed promising results.6-8 Using phenolic MG resists and thermal SPL, the realization of complex high-resolution patterns and even the realization of three dimensional shapes are demonstrated.9,10 However, tailoring resist materials towards required properties is one of the key factors to control the resolution of future lithography and nanomanufacturing.

In this work we demonstrate the film forming behavior of tailored synthesized MG resists prepared by spin-coating and physical vapor deposition (PVD). On the one hand promising fully aromatic resist materials show limited dissolution behavior in typically used spin-coating solvents and offer a high tendency to crystalize during solvent evaporation. On the other hand high thermal and chemical resistance of these materials makes them ideal for film preparation by PVD. Typically PVD prepared films of small organic molecules show a higher tendency to form amorphous films during the evaporation. But recrystallization occurs in the case of a given unstable amorphous state with time. To overcome this issue we used coevaporation of two structure related resists to prepare stable amorphous thin films. The relation is necessary to suppress demixing and to allow a random stable co-arrangement to form the amorphous state. In our work we show e.g. a 1:1 mixture of tris-substituted twisted resist materials, where the distinct molecular difference is given by one more or less tri-fluoromethyl group in the outer benzene rings. The concurrent single molecule by molecule coevaporation offered a stable amorphous film with high force sensitivity to thermal SPL. Thus high resolution patterns with 20 nm HP are demonstrated.

9779-46, Session 13

## Molecular simulations and evolutionary computing to reconstruct the block-copolymer morphology from x-ray scattering

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Directed self-assembly of block copolymers (BCP) on chemical patterns is proven to be a suitable candidate to complement conventional lithography processes for patterning of small feature sizes. Three-dimensional metrology of the assembled films over large surface areas remains an important challenge. Imaging techniques e.g SEM and TEM can provide the top-down and through-film information of the morphology respectively and characterize local defects with limited field of view. In contrast, X-ray scattering techniques like Critical Dimension Small Angle X-Ray Diffraction (CDSAXS) probe large areas of thin BCP samples providing information on the underlying morphology. Analysis of scattering data is an inverse problem that relies on calculating the intensity based on a proposed structure and comparing to recorded data. A potential agreement between the calculated and experimental intensities provides support for the hypothesized morphology. In the opposite case, state-of-the art optimization methods are often employed to manipulate the structural characteristics of the proposed morphology with an ultimate aim to reproduce the experimentally measured data. Nevertheless, the increasing complexity of the morphologies sought renders the previously approach challenging.

In this work, we present a methodology to directly compare the experimentally observed scattering profiles of polystyrene-b-polymethymethacrylate (PS-PMMA) with the outcome of molecular simulations. A set of thermodynamic and boundary conditions are

introduced as an input to well-established Theoretically Informed Coarse Grained model1. The trajectories recorded from simulations are contrasted to the experimental data. We resort to an optimum combination of the simulation parameters, by using the Covariance Matrix Adaptation Evolutionary Strategy (CMA-ES) resulting in faster convergence compared to traditional random search2. We will discuss the effect of polymer asymmetry, geometry and the type of chemical pattern on the block copolymer morphology and hence the scattering intensity profile. The analysis discussed presents a unique approach to evaluate the underlying physics that drive self-assembly and optimize structure by tuning the molecular characteristics of the systems studied.

9779-47, Session 13

## Directed self-assembly of diblock copolymers in mutli-VIA configurations: effect of chemopatterned substrates on defectivity

Corinne L. Carpenter, Kris T. Delaney, Glenn H. Fredrickson, Univ. of California, Santa Barbara (United States)

Directed self-assembly (DSA) of block copolymers has gained much attention for its potential as a low-cost, high-throughput patterning tool to supplement existing lithographic techniques, and in particular for its ability to easily pattern vertical interconnect accesses (VIAs). Single-hole shrink has been extensively explored, but the continued push towards higher-resolution patterns requires more efficient, less space-consuming techniques. The lithographic resolution limits the minimum distance between two features, and the single-hole templates take up valuable real estate on the wafer. To accommodate denser features and relax the resolution requirements of the lithographic techniques, it is prudent to move to multi-VIA configurations in which two or more features are assembled in a single guiding template (such as an ellipse, a peanut, or a rounded rectangle). This allows considerably denser feature patterning, but comes at the cost of more plentiful and complicated defect modes than those found in single-hole shrink features. Most systems contain persistent horizontal structures (eg. rings, U-defects, or bars) that prove detrimental to the etch process and yield undesirable configurations. Chemically selective patterning may prove useful in eliminating these defects if applied correctly to the system substrate. In this study, we use three-dimensional self-consistent field theory (SCFT) simulations to investigate the equilibrium and metastable defective configurations of diblock copolymer DSA systems in the presence of chemically selective template sidewalls and preferentially attractive striped substrates. We identify the chemopatterning scheme that maximizes defect energies, including sidewall interaction strength and chemical preference. In addition, we discuss chemopatterning schemes that are ultimately detrimental, creating even more complicated and persistent defective modes such as horizontal half-cylinders on the system substrate.

9779-48, Session 13

## Surface affinity role in directed self-assembly of lamellar block copolymers

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Directed Self Assembly (DSA) of block-copolymers (BCPs) is a low-cost, time-saving and versatile complementary technique to the 193nm immersion lithography. This complementary lithographic process can be successfully used for the sub-10nm node for both via [1] and line/space patterning [2]. For line/space application a substantial amount of results were reported in the last couple of years on the chemoepitaxy approach. Nevertheless, several challenges such as line roughness, placement error control or low multiplication factor still need to be assessed. Thanks to the physical constrains coming from the guiding patterns, the graphoepitaxy approach could be the solution for higher multiplication factors. Moreover, by tuning surface properties, one can expect to dissociate template roughness from block copolymer domains roughness.

In this work we are focusing on the graphoepitaxy approach for line/space application. Using the 300mm pilot line available in LETI and Arkema's advanced materials [5], we investigate process optimization of DSA line/space patterning of a 38nm period lamellar PS-b-PMMA BCP (L38). As surface affinity is a key parameter in self-assembly of BCP [3, 4], CD uniformity, defectivity and roughness are studied with respect to the BCP guiding patterns affinity and self-assembly parameters.

Wafers with fingerprint patterns were generated and statistical defectivity analysis monitored. Thus the number of end-line, branches and single domain are counted from CD-SEM top view images by using homemade software (see figure 1A). Several parameters characterizing the self-assembly flow such as neutral layer composition, polymer film thickness annealing time and temperature, were finely tuned in order to identify the best process and anticipate process window for a graphoepitaxy approach (see figure 1B).

Furthermore a graphoepitaxy process is implemented: the BCP is self-assembled inside organic hard mask guiding patterns (SiARC/SOC layers), generated by dry 193nm lithography. Different "template affinity" are benchmarked using sidewall and/or bottom grafted polymers: such as fully PS-affine or PMMA-affine trench that can also have a neutral bottom with either PS or PMMA affine sidewalls. As an example for a PS affine process results are reported in figures 2 and 3. Several density multiplication factors are demonstrate up to 5 as illustrated by top-view CD-SEM images (figure 2). Moreover statistical analysis of line edge roughness (LER) and line width roughness (LWR) is reported. For example, for the PS affine process, the measured LWR is 2.5nm (3?) and the LER is 4.5nm (3?) (see figure 3A). In addition, SEM cross-sections reveal the polymer in-depth morphology inside the guiding pattern (figure 3B) and confirm that the PS domain distribution is compatible with integration requirements (in film perpendicular domains, no "onion like" structures). Moving forward into integration, additional process step such as BCP planarization (over coating and plasma recess) are needed in order to accommodate several density for templates on the same wafer [6]. Planarization impact on the process window stability is studied with regard to the initial block copolymer film thickness and plasma recess parameters.

Overall, this work further illustrates the great compatibility of DSA with conventional integration for CMOS technology and offers a few ways to quantify and reduce defectivity.

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9779-49, Session 13

## Influence of template fill in grapho-epitaxy DSA

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Directed self-assembly (DSA) of block copolymers (BCP) is considered a promising patterning approach for the 7 nm node and beyond. Specifically, a graphoepitaxy process using cylindrical phase BCPs (at imec known as templated DSA) may offer an efficient solution for patterning randomly

distributed contact holes with sub-resolution pitches, such as found in via and cut mask levels. In templated DSA, conventional lithography is used to create a topographical pre-pattern in which, after a surface energy optimization step, a cylindrical BCP is deposited and allowed to phase separate. Finally, the minority block is removed which should result in one or multiple sub-resolution holes within each template.

It has been previously reported that templated DSA shows a dependence on template pattern density. Commonly reported defects such as missing and merging contact holes can occur due to respectively over- or underfilling of the template. A potential solution to counteract the influence of template pattern density is to use sub-DSA-resolution assist features (SDRAFs).

In this work, the template fill (defined as the local BCP film thickness within the template) is experimentally shown to depend on template pattern density, solution viscosity, coating spin speed, and pre-pattern surface energy. Understanding the relationship between these parameters and the resulting fill is crucial for successful implementation of templated DSA. An empirical formula describing this relationship is proposed and discussed. Afterwards, experimental findings are presented concerning the influence of template fill on the resulting DSA morphology and the transfer of the DSA pattern into an underlying stack.

9779-50, Session 13

## Application of resonant x-ray scattering to high-chi polymers

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The semiconductor industry is pushing the limits of conventional optical lithography. According to the ITRS roadmap, new lithographic methods will be required to economically produce the smaller patterned features of future processing generations. Technologies being evaluated to produce these finer feature sizes include extreme ultraviolet (EUV) lithography, multiple-beam electron beam lithography, multiple exposures, and directed self-assembly (DSA) of block copolymers (BCPs). BCP lithography uses a template to direct the self-assembly of the block copolymer. If the template is an integer multiple of the BCP natural repeat distance, the pattern frequency can be multiplied and result in a much smaller pitch than the original lithography method could obtain.

One of the critical questions remaining for BCP lithography is the buried structure and potential 3D defects not visible with surface characterization methods such as CD-SEM and AFM. By combining critical-dimension small-angle x-ray scattering (CD-SAXS) with resonant soft X-rays we are able to determine the buried structure of the two blocks, the interfacial roughness, and the pitch uniformity in native BCP films.1 These measurements were performed on samples with a wide range of template structures. We found samples that had similar top surface structure often had substantial variations in their buried structure. We also found that lamella on a neutral surface could have considerable differences from the lamella on the guiding lines. We will show how these insights into the 3D structure of the block copolymer interface validates computational simulations of the directed self-assembly process of line-space pattern gratings.

In addition to the structure of the patterned samples the interfacial width between the two blocks is expected to play a role in determining the line edge roughness (LER). Soft X-ray reflectivity on BCP lamella oriented parallel to the surface was used to probe the interface width between the lamella. The interface width is connected to the interaction parameter (?) between the two BCP components. By blending a selectively associating additive with the BCP ? can be enhanced and the interfacial width reduced.2

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# Conference 9780: Optical Microlithography XXIX

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9780-1, Session 1

## Patterning challenges in the sub-10 nm era *(Keynote Presentation)*

Moshe E. Preil, GLOBALFOUNDRIES Inc. (United States)

In the 40 years of SPIE conferences on lithography, most of the progress driving the steady decline in feature sizes has been achieved through improvements in the three basic parameters which define resolution according to the Rayleigh equation: wavelength, numerical aperture (NA) and k1 factor. Over the past decade, however, there has been almost no improvement in any of these three parameters. The wavelength has not changed since the adoption of 193 nm ArF excimer laser sources, the maximum NA of 1.35 (0.93 * the index of refraction of water) has been reached, and the k1 factor is already at the lowest practical value of ~ 0.30. Despite this, progress in increasing pattern density has continued by developing new processes such as multiple patterning, either by sidewall deposition or litho-etch-litho-etch double patterning. In many respects, the resist pattern itself no longer directly defines the final device pattern. The limiting feature sizes are now being defined by deposition and etch processes rather than by the optical patterning step. Despite progress bringing EUV lithography to a level where it can support serious research programs, this trend will continue for at least the next several process nodes.

The emphasis on patterning rather than just printing has created new pressures in other parts of the overall process, beginning with the design itself. It is no longer feasible to print random, 2D patterns. The most critical layers are restricted to unidirectional patterns with a limited range of critical dimensions (CD) and pitch. Multiple patterning has put greater stress on total overlay (OL) budgets. The traditional breakdown of lithographic error budgets into CD and OL tolerances has given way to total edge placement error (EPE) budgets where CD, OL and edge roughness, as well as film and etch variations, must all be controlled to meet the required tolerances. Contact hole and cut mask placement have likewise been tightened to single digit EPE budgets.

The drive for better patterning has led to such novel processes as directed self-assembly (DSA), selective deposition and etch. Development must focus not just on individual parts of the process but on design-process co-optimization (DTCO) to produce manufacturable parts. Selective deposition and etch may well improve overlay tolerances by growing or removing materials only in specific areas, but they must be developed together with design and layout constraints that do not increase die size. Similarly, while DSA reduces the CD variation of traditional top-down processing, the placement of the self-assembled patterns can degrade overlay performance. DSA is also suited only for very restricted sets of patterns, requiring tighter coupling between design and process.

There are also significant new challenges to be addressed. New “gate all around” (GAA) architectures will require vertical selectivity as well as horizontal patterning. While the exact GAA configuration is not yet settled, both nanowire and nanosheet options may be needed, and new methods of connecting laterally rather than vertically will present new process and metrology challenges. Finally, improvements in resist and other materials must take into account the stochastic nature of patterning processes at such small dimensions. Improved materials and simulation tools are needed to develop processes which produce uniform, predictable results in a domain where molecular level variations take place over a significant fraction of the feature size.

9780-2, Session 1

## Inverse design and implementation of compact and efficient nanophotonic circuits *(Keynote Presentation)*

Jelena Vuckovic, Alexander Piggott, Jesse Lu, Jan Petykiewicz, Stanford Univ. (United States)

By completely opening the parameter space in design of nanophotonic circuits, new functionalities and better performance relative to traditional optoelectronics approaches can be achieved. We have recently developed such inverse approach to design nanophotonic structures only based on their desired performance. Moreover, constraints including structure robustness, fabrication error, and minimum feature sizes can be incorporated in design, without need to have an optics expert as a designer. Finally, such structures are fully fabricable using modern lithography and nanofabrication techniques. Examples of demonstrations of devices including ultra-compact and efficient wavelength splitters on the silicon platform will be presented.

9780-3, Session 2

## Expected innovations of optical lithography in the next 10 years *(Invited Paper)*

Soichi Owa, Noriyuki Hirayanagi, Nikon Corp. (Japan)

In the past 10 years, immersion lithography has been the most effective high volume manufacturing method for the critical layers of semiconductor devices. Today, it is the recognized technology to be used for the 10 nm node in combination with multiple patterning techniques, and it may even be the technology used for the 7 nm node and beyond. To achieve the performance and accuracy needed for these nodes, the projection for the next 10 years is to continuously enhance the immersion scanner system, including throughput. This total productivity, however, can be upgraded by not only continuous improvements, but also by larger innovations which might happen in the optical lithography. In this paper, we will discuss the possibilities and the impossibilities of potential lithography future innovation ideas.

9780-4, Session 2

## Computational process modeling and correction in a multipatterning era *(Invited Paper)*

Chris Spence, ASML Brion (United States)

Since the 28nm node, the resolution of ArFi lithography tools has been limited by the fixed Numerical Aperture of the scanners (1.35) at approximately 40-45 nm half pitch. As a consequence, the shrink cadence identified by Moore’s law requires more and more complex patterning flows such as multiple Litho-Etch (LE) steps as well as spacer techniques (Self-Aligned Double Patterning (SADP)). To ensure yield it is necessary to optimize the total Edge Placement Error, a combination of Overlay, Global CDU, LCDU, OPC errors after processing is completed.

In this presentation we will discuss some of the ways that these contributors can be measured, modeled and corrected as part of a Holistic Lithography methodology. These techniques can be combined with EUV lithography to continue Moore’s law down to final pattern dimensions of 5-6 nm half pitch

9780-5, Session 2

## Lithographic qualification of high-transmission mask blank for 10nm node and beyond

Yongan Xu, IBM Corp. (United States); Tom B. Faure,

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In this paper, we discuss the lithographic qualification of high transmission (High T) mask for contact hole applications in 10nm node. First, the simulated MEEF and DoF data will be compared between the 6% and high T PSM masks with the transmission of high T mask blank varying from 12% to 20%. The 12% High T blank shows significantly better MEEF and larger DoF than those of 6% PSM mask blank, which are consistent with our wafer data. However, the simulations show no obvious advantage in MEEF and DoF when the blank transmission is larger than 12%. From our wafer data, it will be also seen that the common process window from High T mask is 40nm bigger than that from the 6% PSM mask. In the elongated bar structure, the 12% High T mask shows significantly less develop CD pull back in the major CD direction at different print bias. The optimized illumination condition for 6% PSM shows MEEF improvement but almost no improvement in the DoF through pitch. In addition, by using the High T mask blank, we have also investigated the SRAF printing and the resist profile through cross sections, and no patterning risk has been found for manufacture. As part of this work new 12% High T mask blank materials and processes were developed, and a brief overview of key mask technology development results will be shared. Overall, it is concluded that the High T mask, 12% transmission, provides the most robust and extendable lithographic solution for 10nm node and beyond.

9780-6, Session 2

## Ultimate intra-wafer critical dimension uniformity control by using lithography and etch tool corrections

Michael Kubis, Liesbeth Reijnen, Katja Viatkina, Melisa Luca, Charlotte Chahine, Jan Mulkens, Mircea V. Dusa, ASML Netherlands B.V. (Netherlands); Richard J. Wise, David Hellin, Benjamin Kam, Daniel Sobieski, Johan Vertommen, Girish A. Dixit, Nader Shamma, Lam Research Corp. (United States); Patrick Jaenen, Philippe Leray, IMEC (Belgium)

With shrinking design rules, the overall patterning requirements are getting aggressively tighter and tighter. For the 7-nm node and below, allowable CD uniformity variations are entering the Angstrom region. Optimizing inter- and intra-field CD uniformity of the final pattern requires a holistic tuning of all process steps.

In previous work, CD control with either exposure tool or etch tool corrections has been discussed. Today, we present the ultimate holistic CD control approach, combining the correction capability of the etcher with the correction capability of the exposure tool.

State-of-the-art scanners and etch tools offer high-order correction potential of CD uniformity fingerprints. In the ArF scanner (NXT:1970Ci), freeform dose correction across slit and along scan can be used for every field to tune the CD uniformity, using LithoInsight® solutions.

In the latest etch tools (Kiyo® E and Kiyo® F Series) proprietary Hydra® technology can be used to tune for optimum CD uniformity.

The study is done on 10-nm logic node wafers, processed with a test vehicle stack patterning sequence. We include wafer-to-wafer and lot-to-lot variation and apply optical scatterometry (YieldStar S-250) to characterize the fingerprints. Making use of all available correction capabilities (lithography and etch), we investigated combinations of feedforward and feedback loops to reach the lowest CD uniformity. Results of the final pattern uniformity based on this co-optimization technique are shown.

We conclude on the application of this holistic lithography and etch optimization to 7nm High-Volume manufacturing, paving the way to ultimate within-wafer CD uniformity control.

9780-7, Session 3

## The impact of lower light source bandwidth on patterning performance

Paolo Alagna, Cymer LLC (Belgium); Gregory A. Rechtsteiner, Will E. Conley, Cymer LLC (United States); Vadim Timoshkov, ASML Netherlands B.V. (Netherlands); Patrick Wong, IMEC (Belgium); Jan Baselmans, ASML Netherlands B.V. (Netherlands)

Patterning solutions based on ArF immersion lithography are the fundamental enablers of device scaling. In order to meet the challenges of industry technology roadmaps, tool makers in the DUV lithography area are continuously investigating all of the interactions between equipment parameters and patterning in order to identify potential margins of improvement. Cymer, a light source manufacturer, is fully involved playing a crucial role. As demonstrated by Cymer's recent studies, a significant improvement to multiple patterning solutions can come by leveraging the light source capabilities. In particular, bandwidth is a key knob that can be leveraged to improve patterning. While the previous publications assessed contrast loss induced by increased bandwidth, with this work the authors will expand the research in the opposite direction and will investigate how patterning can be affected by improved image contrast achieved by bandwidth reduction. Preliminary analysis performed on simulated and experimental data show encouraging potential margins improvements.

9780-8, Session 3

## Intra-lot wafer by wafer overlay control using integrated and standalone metrology combined sampling

Young-Sin Choi, Donghan Lee, Jae-il Lee, YoungSun Nam, Young Seog Kang, Se-Yeon Jang, Jeong-Heung Kong, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

Tight overlay margin of DRAM with device shrinkage is requiring wafer level correction. From this reason, intra-lot drift control has been already applied by lens and reticle heating control technologies. And photo scanner recently released has the capability for reducing the wafer to wafer overlay variation with extended correction potential. Nonetheless there still exist high residual that classified correctable error per wafer. In general, in order to control intra-lot overlay variation such as wafer by wafer correction, it requires several times of overlay measurements.

Recently by using integrated-metrology tool, it was successful to measure intra-lot overlay variation. It is expected to improve APC overlay performance by correction of intra-lot overlay variation measured by integrated-metrology. In this paper, intra-lot wafer to wafer correction using data coming from integrated and standalone metrology will be tested and discuss about the gain of overlay performance. Using the specific layer of 2X nm node, measure several wafers and budget break out correctable parameter. Finally we get encouraging results through feed forward by wafer with this experiment.

9780-9, Session 3

## Reduction of wafer-edge overlay errors using advanced correction models, optimized for minimal metrology requirements

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In order to optimize yield in DRAM semiconductor manufacturing for 2x nodes and beyond, the (processing induced) overlay fingerprints towards the edge of the wafer need to be reduced. This can be achieved by acquiring denser overlay metrology at the edge of the wafer, to feed field-by-field corrections. Although field-by-field corrections can be effective in reducing localized overlay errors, the requirement for dense metrology to determine the corrections can become a limiting factor due to a significant increase of metrology time and cost. Moreover, frequently updating field-by-field corrections adds a risk of adding some level of lot-to-lot or wafer-to-wafer noise into the corrections being applied.

In this study, a more cost-effective solution has been found in extending the regular correction model with an edge-specific component. This new overlay correction model can be driven by an optimized, sparser sampling especially at the wafer edge area, which also allows for a reduction of noise propagation. Lithography correction potential can be maximized, with significantly less metrology needs. Evaluations have been performed to show the benefit of edge models in terms of on-product overlay performance. We show here improvements of wafer-edge overlay combined with sparse metrology.

Optimized sparse metrology, while still meeting on-product performance requirements, enables integrated metrology. The ultimate goal is to drive down overall metrology fab footprint and lithography cycle time.

9780-10, Session 3

## Overcoming low-alignment signal contrast induced alignment failure by alignment signal enhancement

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Overlay is one of the key factors which enables the extension of optical lithography to the 1X node in DRAM manufacturing. It goes without saying that good wafer alignment is a prerequisite for good overlay. However, alignment failures or misalignment are commonly observed in the Fab. There are many factors which could induce alignment problems.

Low contrast in the alignment signal is one of the main issues. The contrast can be degraded by opaque stack materials or due to processes like CMP. This becomes critical in the case mark sub-segmentation is combined with double or quadruple spacer process.

The contrast in the alignment signal can be improved by applying new material or process optimization, which could lead to adding another costly process. However, if we would be able to amplify the position signal and reduce the background signal, we would be able to improve the alignment performance without the need for any process change. In this paper we use ASML's new alignment sensor (SMASH MK3.3) on special wafers containing 'low contrast marks' to demonstrate a significant alignment & overlay improvement.

9780-11, Session 3

## Pattern edge placement errors at 10nm integrated circuit design node

Jacek K. Tyminski, Julia A. Sakamoto, Shane R. Palmer, Steven S. Slonaker, Stephen P. Renwick, Nikon Research Corp. of America (United States)

Use of 193nm immersion-based (193i) lithography at current and future lithographic nodes requires extensive use of multiple patterning. Previously, imaging quality was described largely by CD control and overlay. Now, these metrics have become strongly linked and the overall figure of merit is edge placement error (EPE).

One of the key contributions to EPE is attributed to layout design, corrected for optical proximity effects, interacting with optimized setups of the imaging tools1. Other contributions to pattern EPE are directly linked to the exposure tool alignment and overlay performance2. Finally, imaging-driven pattern displacements and exposure defocus and dose variations occurring during imaging tools operation also contribute to pattern EPE3.

To unify all edge placement contributions into a common, integrated environment, we have developed an EPE model combining contributions from layout designs and OPC interacting with optimized projector setup, scanner overlay performance, and optically driven image displacements. This EPE model can be used to conduct scanner-specific analysis of the impact of various layout designs and imaging strategies on pattern placement at various IC layers.

In this report, EPE model and its components for advanced immersion ArF scanners will be presented. Examples of pattern EPE budgets, representative of 10 nm IC design node, will be discussed. Statistics of across-wafer and intra-field EPE of 10 nm node patterns will be presented. Conclusions on the edge placement performance of the current generation of the lithography tools patterning 10nm and more advanced node designs will be presented.

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9780-12, Session 4

## Pattern size based process window variation comparison between NTD and PTD

Doyoun Kim, SK Hynix, Inc. (Korea, Republic of)

In this paper, we have explored the trend of both NTD and PTD patterns in various environments. We have analyzed process window variation of both NTD and PTD according to pattern types, sizes and pitch. As well, the process window of a layer with various pattern types and sizes tends to decrease due to specific size and type. As a result, guidelines for using NTD and PTD will be proposed.

9780-13, Session 4

## Ultimate 2D resolution printing with negative-tone development

Martin Burkhardt, IBM Thomas J. Watson Research Ctr. (United States); Yongan Xu, IBM Corp. (United States); Hsinyu Tsai, IBM Thomas J. Watson Research Ctr. (United States); Alexander Tritchkov, Joerg Mellmann, Mentor Graphics Corp. (United States)

The printing of contact holes using positive tone development typically requires the interference of more than the 0th and 1st diffracted orders. In the 2d case and cQuad illumination, if (0,0), (±1,0), and (0,±1) are exclusively present, the contrast can in the best case not rise above 0.33, which is typically insufficient for a good process window. And this maximum value can only be achieved if the (0,0) and (±1,0) orders are matched to give a perfect sine wave of perfect contrast in y while the (0,0) and (0,±1) orders yield perfect contrast in x. In reality, the contrast is quite a bit lower. On the other hand, for negative tone development we are interested in the minima of the intensity–the dark locations in the image–and if we can manage to reduce the intensity in the minima we can achieve a high contrast image. Through a choice of RET and illumination, we manage to achieve a resolution for contact holes in 2d at k1 values that can otherwise be achieved only for 1d imaging.

Earlier work has been done on double exposures that exposed in the same resist a horizontal grating with x-dipoles and subsequently a vertical grating with y dipoles, without intermediate process steps. This yielded a high contrast image in resist at k1 <0.3 (Truffert 2009). We show that an equivalent result can be achieved in a single exposure with a single mask, at admittedly high dose. We investigate the process parameters and the related mask tolerances, and find a non-intuitive result for the mask pattern that yields an optimized image at given mask specifications. Finally, we investigate the extension of this technique to EUV through simulations and (hopefully) experiments.

9780-38, Session PTue

## Sub-100nm periodic structures fabricated by proximity i-line mask-aligner lithography (and self-aligned double patterning)

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I-line mask-aligner lithography is a well known method for the printing of micrometer sized features, and it´s thus particularly used for the fabrication of MEMS devices. In spite of a theoretical resolution in the range of half of the illumination wavelength, the feature size remains five to ten times higher than this value especially if the proximity exposure mode is used. By using a binary diffraction grating as photo-mask and illuminating it close-to-normal incidence, the latter generates only the + and – 1st transmitted diffraction orders if the grating structure is properly optimized (period, duty-cycle, depth, and material). The interferences generated in the overlapping area of these two propagating orders create a high-contrasted sinusoidal intensity distribution with a long depth of focus. This allows to use the proximity exposure mode and thus avoid the unwanted use of contact lithography, which degrades the mask after some exposures. With such a technique, the period of the interferogram is half of the one of the phase-mask, and we present here the transfer of a grating with a period of 350 nm by placing the photoresist coated wafer 10 μm away from the 700 nm period mask. By using the method known as Self-Aligned Double Patterning (SADP), it´s then possible to reduce the printed period by a factor of two, and produce 175 nm periodic structures from the 350 nm periodic ones, and thus reach the 90 nm node with i-line proximity mask-aligner lithography. The fabrication method consists in transferring a 350 nm period grating, fabricated according the method described above into a sacrificial polymer layer. A metal layer (Aluminum) is then deposited over the polymer structure by evaporation. Afterwards the metal is removed from the horizontal surfaces leaving only metal on the side wall of the grating trench. The last step consists in removing the sacrificial polymer layer and then obtains a 175 nm period metal grating. The final metal grating can be used as etching mask for the transfer of a high resolution grating in the substrate or directly used as optical component. As a practical application we have used the fabricated 175 nm aluminum grating as wire grid polarizer. The optical characterization shows that the fabricated component work for a large wavelength range (from 400 nm to over 1 μm) covering the visible part of the electromagnetic spectrum, with a transmission of the TM polarized light over 30 % and an extinction ratio above 35 for wavelengths above 450 nm. The result demonstrates that proximity i-line mask-aligner lithography can be an alternative method for the production of large area sub-wavelength optical components, usually made by e-beam lithography.

9780-39, Session PTue

## Innovative method to suppress local geometry distortions for fabrication of interdigitated electrode arrays with nano gaps

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In this paper we present a method to optimize the lithography process for the fabrication of interdigitated electrode arrays (IDA) for a lift-off free electrochemical biosensor. The biosensor is based on amperometric method to allow a signal amplification by redox cycling. By decreasing the gap between the electrodes the cycling efficiency can be increased compared to the conventional amperometry[1], [2]. Different fabrication techniques are used to build the electrode arrays with gap distances in the nanometer range but requires more advanced technologies such as e-beam, DUV projection lithography or nano imprint lithography [3]–[5]. However these processes are more expensive and require a lift-off process afterwards. We demonstrated a method to fabricate IDAs with nano gaps with conventional mask aligner lithography and two subsequent deposition process. This process sequence even eliminates the lift-off process which is a critical step for electrode fabrication. With mask aligner lithography an initial structure with a critical dimension of 1 μm line and space (l/s) is fabricated. The linewidth variation of this finger structures is critical due to the fact that the elevated resist pattern is increasing during the subsequent deposition processes and consequently the distance between the structures is decreasing. By decreasing the distance down to the nanometer range the linewidth variation is becoming the most critical factor and can result in a short circuit of the electrodes.

Therefore, the light propagation and the resist pattern of the mask aligner lithography process are simulated to optimize the lithography process. Analyzing the light propagation of the IDA pattern for different distances of mask and wafer indicate an intensity reduction due to Fresnel diffraction at the outer finger structures of the electrode array. The area with the periodical structures show equal intensity distribution for the gaps whereas the gap for the outer finger structures (where the periodic ends) the intensity decreases. The result is a larger finger structure at the IDA end region. Consequently, the width of the electrode fingers has to be equal to prevent a short circuit (grow together) during deposition process where the distance between the structure decrease. To optimize the outer finger structure assistant features (AsFe) were introduced. The AsFe allow an optimization of the intensity distribution at the electrode fingers. Hence, the periodicity is expanded and the outer structure of the IDA is practically a part of the periodic array. The better CD uniformity can be obtained by adding three assistant features which generate an equal intensity distributions for the complete finger pattern. Considering a mask optimization of the outer structures would also be feasible [4]. However, due to the strong impact of the gap between mask and wafer at contact

lithography it is not practicable. The better choice is to create the same intensity distribution for all finger structures. With the introduction of the assistant features large areas with electrode gap sizes in the sub 100 nm region are demonstrated.

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9780-40, Session PTue

## Coherence management in lithography printing systems

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Proximity lithography is a widely used printing technique in production lithography. Its main advantages are a high throughput and the fact that the mask is better preserved as compared to contact printing. But when using such a printing technique, the resolution is limited by diffraction and interference effects and decreases with the increase of the gap, which is usually of 30 to 200 um. Different methods have been developed to reduce as much as possible these diffraction effects. More specifically, it has been shown that, influencing on the coherence of the illumination, by modifying the angular spectrum, will directly impact on the quality of the prints.

With coherence effects being of such importance on the resulting prints, it is therefore of interest to study the coherence in various illumination systems and have a way to compare them. The results presented in this work will especially focus on a specific production system. It is a so-called MO Exposure optics, which has been developed by Süss Microtec. It is an improved version of a standard lithography illumination system, where two subsequent Köhler integrators are used instead of one and more channels are introduced (over 10000 channels). Such a system was developed in order to allow variations of the angular spectrum of the illumination, by placing various Illumination Filter Plates (IFP). These plates are placed just before the second Köhler integrator. They are a quick and easy way to customize the illumination spectrum. It has been shown that it results in noticeable differences in the prints, but the coherence of such systems has never been studied. Our aim is to study the coherence in more detail to find ways of an effective coherence management with the MO Exposure optics.

To measure the coherence at the limited space available in the machine, we use a Young double slit experiment. In such experiments the spatial coherence of a quasi-monochromatic source directly determines the contrast of the fringes in the interference pattern obtained in the far-field. An extended source will have a decreased contrast. Therefore, by imaging the interference pattern of a double-slit, it is possible to compare the coherence of different illumination systems. We could here for the first time, measure the coherence of mask aligner illumination system under various conditions.

In practice, the mixing of the different samplings present in the system (microlens array, IFP) makes it more difficult to interpret the results. The aerial images of a structure with 4um features was taken with a microscopic setup. They present some variations in intensity level and homogeneity depending on the filter plate used. The interference pattern measurements also show differences in the coherence of the illumination. A combined knowledge of both aerial images and coherence properties allows to extract important information about the illumination light. In our contribution we will discuss the interdependence between illumination, coherence and structure geometry by presenting several examples including proximity correction structures.

9780-41, Session PTue

## Fabricate large area and defect free periodic structures with advance achromatic laser interference lithography

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Laser interference lithography (LIL) is a great way to produce micro and nano scale periodic structures. The principle of LIL is that two or more coherent laser beams overlap with each other and form a standing wave in the space which can be recorded by the photoresist. Comparing with the traditional optical lithography, it has many advantages such as simple optical design, maskless, inexpensive, infinite depth of focus, and large area patterning with single exposure. LIL has bright future in the field of period structure application such as light-emitting diode (LED), grating, photonic crystals, and etc.

However, due to the principle of LIL, exposure result is very sensitive to the light source, especially in large area exposure. Regular defects occurs in large area exposure result when the laser source has multiple longitudinal mode or mode hopping. Because different mode of laser source interference with each other, and form a beat wave. The electric field distribution of beat wave and the chemical reaction in the photoresist cause the regular defects in large area exposure result. The simulation result match with the experiment result. Therefore, this paper design and build up an advanced achromatic interference lithography system to solve this problem. The principle of achromatic interference lithography is to separate the coherent laser beam by grating and use two parallel mirror to recombine the laser beam, then form a standing wave for exposure. Due to the principle of achromatic interference lithography, the exposure result is no longer relative to the wavelength of the laser source, and the pitch of the periodic structures is half of the grating pitch. As a result, achromatic interference lithography is able to eliminate the regular defects. But traditional achromatic interference lithography system is not very efficient because transmission lost and only first order light is used. This paper build up an advanced achromatic interference lithography system with two reflective blazed gratings. Because of the principle of the reflective blazed grating, we can improve the efficiency of our achromatic interference lithography system. In this paper, 20 mm2 of large area periodic structures with 420nm pitch and 180 nm linewidth have been successfully fabricated without any defects.

In conclusion, this paper design and build up an advanced achromatic interference lithography system which is able to eliminate the regular defects produce large area defect free micro and nano scale periodic structures.

9780-42, Session PTue

## Optimizing the lithography model calibration algorithms for NTD process

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As patterns shrink to resolution limits of up-to-date optical lithography technology, negative tone development (NTD) process has been an increasingly adopted technique to enable superior imaging quality through employing bright-field (BF) masks to print the critical dark-field (DF) metal and contact layers. However, from the fundamental materials and process interaction perspectives, several key differences exist between NTD process

and the traditional positive tone development (PTD) system, especially the horizontal shrinkage and horizontal development depletion, hence the traditional resist parameters developed for the typical PTD process have no longer described well in NTD process modeling. In order to cope with the inherent differences between PTD and NTD processes and get improvement on NTD modeling accuracy, several NTD models with different combinations of complementary terms were built by accounting for the NTD-specific horizontal shrinkage, horizontal development depletion and large wafer CD jump induced by sub threshold assistance feature (SRAF) effect. Each new complementary NTD term has its definite aim to deal with the NTD-specific phenomena. In this study, the modeling accuracy was compared for the different models and the specific patterning characteristics were evaluated among various feature types. Multiple complementary NTD terms were finally proposed to solve all the NTD-specific behaviors simultaneously and further optimize the NTD modeling accuracy. The test results of new algorithms on our critical dark-field layers demonstrated consistent model accuracy improvement on both calibration and verification.

9780-43, Session PTue

## Source mask optimization using 3D mask and compact resist models

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Source Mask Optimization (SMO) has played an important role in technology setup and ground rule definition since the 2x nm technology node. While improvements in SMO algorithms have produced higher quality and more consistent results, the accuracy of the overall solution is critically linked to how faithfully the entire optical system is modeled, from mask down to substrate. Fortunately, modeling technology has continued to advance to provide greater accuracy in modeling 3D mask effects, 3D resist behavior, and resist phenomena.

Specifically, the Domain Decomposition Method (DDM) approximates the 3D mask response as a superposition of edge-responses. The DDM can be applied on sectorized illumination source based on Hybrid-Hopkins Abbe approximation, which provides an accurate and fast solution for the modeling of 3D mask effect and has been widely used in OPC modeling. The implementation of DDM in the SMO flow, however, is more challenging because the shape and intensity of the source, unlike the case in OPC modeling, is evolving along the optimization path. As a result, it gets more complicated. It is accepted that inappropriate pupil sectorization results in reduced accuracy in any application, however in SMO the required uniformity and density of pupil sampling is higher than typical OPC and modeling cases.

In this paper, we describe the novel method to implement DDM in the SMO flow. The source sectorization is defined by following the universal pixel sizes used in SMO. Fast algorithms are developed to enable computation of edge signals from each fine pixel of the source. In this case, each pixel has accurate information to describe its contribution to imaging and the overall objective function. A more continuous angular spectrum from 3D mask scattering is thus captured, leading to accurate modeling of 3D mask effects throughout source optimization. This method is applied on a 2x nm middle-of-line layer test case. The impact of the 3D mask model accuracy on the source profile and corresponding lithographic performance is studied in detail. Furthermore, the impact of using a compact resist model in SMO is also investigated by using the same test case. The improvement in lithographic performance by employing accurate 3D mask models and compact resist models is further justified by simulation from rigorous models.

9780-44, Session PTue

## Layer aware source-mask-target optimization

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Source-mask optimization (SMO) has been used extensively to enhance the resolution of lithography with low k1 factors for logic 2x nm and below nodes. As design target co-optimization becomes a critical part of the technology development, design targets are added as additional variables into the SMO frame work, thus enabling the co-optimization of the targets together with the illumination source and mask shapes. Since the SMO cost function is designed for lithographic process window maximization, the optimization of design targets is based on lithographic metric and does not take into consideration the impact of the etch process. As a result, the lithography targets optimized via conventional SMO may not lead to optimum post-etch final targets.

To address the post-etch process requirement, we developed the methodology and flow of layer aware source-mask-target optimization. In this approach, the target co-optimization in SMO is performed by considering the inter-layer constraints. Fig. 1 illustrates a test case by showing an integrated critical pattern cell for the metal layer. To maximize the process window of the tip-to-tip (T2T) feature, a large T2T lithography target is preferred. However, with the increase of the T2T spacing, the post-etch metal to via overlap margin is reduced. In the layer-aware source-mask-target optimization flow, a geometry constraint for the T2T lithography target is defined by considering metal to via enclosure rule as well as the etch bias. The T2T target is then co-optimized with the source and mask under this constraint. The optimum target resulting from this flow is the best solution that gives the largest possible lithographic process window while maintaining inter-layer requirements at the post-etch stage. Fig. 2(a) shows the Exposure Latitude (EL) vs. Depth of Focus (DOF) plot for the test case described in Fig. 1. With the conventional SMO flow, the overlapping DOF at 5% EL is 66 nm, which is mainly limited by the T2T structures. By co-optimizing the target during SMO, the overlapping DOF is improved significantly to 83 nm. With the implementation of layer-aware source-mask-target optimization, a reasonably good overlapping DOF of 79 nm is still achieved. At the same time, sufficient metal to via enclosure margin is maintained, as shown in Fig. 2(b). This approach can also be extended to the multiple patterning SMO solutions by considering the inter-color constraints.

9780-45, Session PTue

## Resist profile aware source optimization and application in N28 full chip OPC

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Aggressive design rules for contact and back end of line (BEOL) device layers continue to drive the need for effective full chip patterning optimization. Resist top loss is one of the major challenges for 28 nm and below technology nodes. Resist top loss can leads to post-etch

hotspots which are difficult to predict and degrade the process window significantly. With ASML's advanced programmable illuminator (FlexRay) and the Tachyon SMO platform, resist aware source optimization can be achieved which can greatly improve the imaging contrast, enhance focus and exposure latitude, and minimize resist top loss. In this paper, we demonstrate a full chip SMO methodology. It includes: pupil optimization based on robust pattern coverage, validated pupil coverage with excellent lithography performance, and compare standard and resist profile aware (R3D) OPC and lithography manufacturing check (LMC). Results include verifying the most computationally efficient flow to achieve best patterning optimization. We apply this methodology using a real full chip design. Verification results show that an optimized freeform source (FFS) improves DOF, EL, MEEF and best focus shift by 24%, 45%, 25% and 50% respectively. Moreover, the worst resist top CD is improved from 0 nm to 33 nm. This improvement is verified on silicon. A new focus exposure model was calibrated with the FFS, and the full chip OPC recipe was retuned. Wafer data was exposed with the optimized FFS, resulting in a common process window qualification (PWQ) window of 85 nm DOF @ 5% EL without any top-loss hot-spots.

9780-46, Session PTue

## A novel full chip process window OPC based on matrix retargeting

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Introduction

In traditional PVBAND based PWOPC, PVBAND was used to represent process variations. The process variations normally include dose/focus variations. PVBAND was generated by XOR all the simulation contours at different dose/focus corners. Pinch/Bridge related constraints were defined for inner and outter of PVBAND. The PWOPC process moves fragments in such a way not only to make simulated nominal contour to achieve target, but also trie to meet the pinch/bridge constraints defined for inner/outter band.

In advanced technology node, however, the situation becomes more complicates. For example, For Metal layer in 28nm and below, more complicated models may be needed in PWOPC such as TOPLOSS model. So another criterion is needed to constrain the bridge based on TOPLOSS model simulation. Also it is not unusual to define contact/via related enclosure constraints for metal layer. All those constraints were defined by user based on experience, sometimes those constraints were aggressive thus it is not easy to find optimal solution. In extreme case those constraints may push certain dense fragments in conflict direction. The performance is also a concern when multiple process condition related simulations were involved in PWOPC.

In this paper a new PWOPC was developed to solve those challenges. The matrix retargeting based PWOPC had several steps: (i) Define constraints for each process window condition, for example one criterion for pinch and one for bridge, one for toploss, one for via enclosure; (ii) Calculate violations based on mask simulation for each fragment; (iii) Generate matrix based on violations of fragments; (iv) Find optimal position of each fragment that will minimize the violations by solving the matrix; (v) Record and treat the optimal position as new target (vi) Traditional nominal OPC was used to converge to that new target.

Experiment results showed on several chips that by using matrix retargeting all the constraints will be considered and optimal solution will be found in a larger scope of dense area.

9780-47, Session PTue

## Model based OPC/ORC accounting for non-planar topography effects in implant layer

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From 28nm technology node and below, Optical Proximity Correction (OPC) needs to take into account light scattering effects from prior layers when bottom anti-reflective coating (BARC) is not used, which is typical for implant layers. Reflective surfaces with topography can cause overexposure in some areas in the photoresist, resulting in undesired critical dimension (CD) variations in the printed patterns. This phenomenon is expected to be attenuated by the use of anti-reflecting coating, but it causes complexity of process, and increased manufacturing costs and time.

In this paper, wafer topography aware OPC/ORC modeling flow taking into account non-planar topography effects for Implant layers is presented. This approach can be effective in delivering improved CD control for complex sub-layouts, and represents only a small impact to full-chip correction runtime. CD-SEM review were used to confirm the validity of the sub-layer aware model on wafer.

9780-48, Session PTue

## Simple method for decrease of wafer topography effect for implant mask

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Controlling critical dimension (CD) of implant blocking layers during photolithography has been challenging due to reflection caused by wafer topography. Unexpected reflection which comes from wafer topography makes severe CD variation on mask patterns of implnat layer. Using bottom anti-reflective coatings(BARCs) can reduce the topography effect, but it could also damage wafer surface during BARCs dry etching. Developable BARCs(D-BARCs) could be alternative solution for wafer topography effect. However there are some issues that should be considered in D-BARCs process such as sensitive temperature control and managing defects. There are also papers introducing model based topography aware OPC as a solution for wafer topography effect implant layer. But building topography aware OPC model is very complex and it takes too much time to build.

In this paper, we will introduce experimental results of wafer topography effect using various test patterns and propose a simple method that could effectively reduce wafer topography effect.

9780-49, Session PTue

## Native conflict awared layout decomposition in triple patterning using bins based library matching method

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As technology nodes further scales down in very large scale integration, triple patterning (TP) lithography is widely recognized as a promising solution for sub 14/10 nm technology. Similar to double patterning (DP) lithography, the key challenge of TP lithography is the layout decomposition. When the distance of two features in a layout is less than a critical value, the two features are regarded as conflicted ones and should be assigned to different masks to achieve pitch relaxation. In order to make the layout decomposable, stitches are inserted to split one continuous feature shape into segments that would be printed in different masks. Unfortunately, even with stitches, not all the patterns can be directly decomposed into three masks due to the "native conflict (NC)", which cannot be resolved by stitch insertion. Detecting a NC in DP lithography is equivalent to odd cycle checking in a layout graph which can be resolved in linear time

using a breath-first-search. But in triple patterning, the NC detection is not straightforward and finding a 4-clique is even NP-complete. Therefore, existing triple patterning layout decomposition methods focus on minimizing number of conflicts and stitches. However, minimizing the number of conflicts may not be optimal in practice since the existence of conflict will reduce layout re-design/modification. To alleviate the designers' work, an efficient method to detect the NC is necessary.

Upon this work, we combine the bin based segmentation with graphs library matching together to detect and report the NCs in triple patterning. In this scheme, isomorphs-free graph generation method is adopted to construct a graph library that contains all bi-connected graphs with four, five, six and seven nodes. The degrees of these nodes are all not less than three. Totally, there are 172 graphs, which are pre-assigned to different colour or NC highlighted. When a layout is loaded, we divide it into overlapping bins according to the density of the layout. A layout graph is constructed in each bin, and iterative vertex removal is applied to remove vertices with degree less than three. The sub-graph obtained will match the graphs in the library using the graph isomorphism algorithm in polynomial time. Once it is matched, we can simply do colouring and NC reporting concurrently by mapping the colours according to the nodes in the library.

Fig. 1(a) presents that part of a layout divided into two overlapping bins within the light-salmon dash. As shown in the figure, the boundary of bins is extended to include fractional parts of polygons in next bins. For example, parts of P6 and P10 are also added into the left bins to construct a conflict graph, so does the polygon P5. However, only the colouring results of polygon within a bin can be accepted. Isomorphism-free graphs with four and five nodes in the library are presented in the Fig 1(b). The NCs are highlighted in a light-salmon dash box, and each node in the graph we obtained gets the degree not less than three. Once the sub-graph matches one in the library, the native conflict can be located and highlighted quickly, and the color of the polygons can be mapped from the corresponding graph in the library directly. In Fig. 2, the layout decomposition and NC highlighted results are shown. The modified c1sim benchmark is tested with our method. Three NCs added in the layout can be highlighted in mustard efficiently and the enlarged partial views of NC area are shown in the three bins.

9780-51, Session PTue

## Means to improve light source productivity: from proof of concept to field implementation

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The availability of large data sets as well as the effective control and management of field activities creates potential for a more reliable understanding of tool behavior in a production environment. By analyzing these large data sets, natural and expected variations from tool to tool, fab to fab, or field personnel / customer ways of working can be identified and minimized. The findings guide the conceptualization and development of new solutions that can in turn help customers increase productivity. We will demonstrate how Cymer has learned from its large install base of ArF immersion light sources to and analyze data to better understand chamber behaviors both in short term and throughout the chamber life time while reducing variations in early chamber qualification. We will illustrate how the team has developed, tested and implemented solutions that improve equipment availability and predictability. Results of productivity gains achieved without any adverse impacts on tool performance or increasing in facilities' consumption (power and gases) will also be presented.

9780-52, Session PTue

## Neon reduction program on Cymer ArF light sources

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Cymer understands that neon supply has been severely impacted and is responding with a multi-part plan to support our customers. Cymer's primary objective is to ensure that reliable system performance is maintained while minimizing gas consumption. Gas algorithms were optimized to ensure stable performance across all operating conditions.

The Cymer neon support plan contains four elements: First: Gas reduction program to reduce neon by >50% while maintaining existing performance levels and availability. Second: Short-term containment solutions for immediate relief. Third: Qualification of additional gas suppliers and fourth: Long-term recycling/reclaim opportunity. The Cymer neon reduction program has shown excellent results when compared to standard gas use versus the new >50% reduced neon performance for ArF immersion light sources. Testing includes stressful conditions such as repetition rate, duty cycle and energy target changes. No performance degradation has been observed over typical gas lives.

9780-54, Session PTue

## The next-generation ArF excimer laser for multiple-patterning immersion lithography with helium free operation

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Multiple patterning ArF immersion lithography has been expected as the promising technology to satisfy tighter leading edge device requirements. A new ArF excimer laser, GT64A has been developed to cope with the reduction of operational costs, the prevention against rare resource shortage and the improvement of device yield in multiple-patterning lithography. GT64A provides the sophisticated technologies which realize the narrow spectral bandwidth with helium free operation and improve further spectral bandwidth stability.

A helium gas purge has usually been employed due to the low refractive index variation with temperature rises in laser shooting within the line narrowing module(LNM). The unique property of helium gas has been increasing the demand in the worldwide industries, but is causing inflation of the price in the market over the years. Nitrogen gas with an affordable price has been used as an alternative purge gas of helium on the restrictive condition of low thermal loads. However, the refractive index variation of nitrogen gas is approximately ten times more sensitive to temperature rises than that of helium. This caused the considerable wavefront distortions of a laser beam in the high duty cycle operations with the higher thermal load, and broadened a spectral bandwidth.

The ingenious LNM configuration in GT64A enables the thermal wavefront deformation of a laser beam to reduce without helium gas purge within LNM. Even without the helium gas purge, the spectral bandwidth becomes equal to that with the conventional helium purge, because the incident beam divergence on a grating is suppressed. The helium free operation saves operational costs in the processes and contributes to support green operations.

In our laser system, a spectral bandwidth is controlled by adjusting the wavefront of a laser beam using a two-lens optical system within a resonator. The bandwidth has deviations by themal history with laser operations. It should be always controlled tightly even after a quiescent interval, such as wafer loading. The spectral bandwidth control algorithm has already been developed to compensate the deviations. Spectral bandwidth stability is improved further by developing the actuator with high response speed. The improvement in spectral bandwidth stability contributes to the further reduction of CD variation.

GT64A is the distinguished light source that offers higher device yield and lower operational costs for chipmakers. In the presentation, the latest development status on GT64A will be discussed.

9780-55, Session PTue

## Rare resource supply crisis and solution technology for semiconductor manufacturing

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There are growing concerns over future environmental impact and earth resource shortage throughout the world and in many industries. Our semiconductor industry is not excluded. “Green” has become an important topic as production volume become larger and more powerful. In this article, recent global supply issue of rare resources, especially Neon gas, and solution to support semiconductor industry will be discussed.

Because of its inertness and extreme chemical stability, the rare gases are widely used in semiconductor manufacturing. One major component of an Excimer laser system is Neon. It is used as a buffer gas for Argon (Ar) and Krypton (Kr) gases used in deep ultraviolet (DUV) lithography laser systems. Since Neon gas accounting for more than 96% of the laser gas mixture, a fairly large amount of neon gas is consumed to run these DUV lasers. However, due to the country’s ongoing crisis in Ukraine, the main producer of neon gas today, supply reduction has become an issue and is causing increasing concern. This concern is not only based on price increases, but has escalated to the point of supply shortages in 2015. This poses a critical situation for the semiconductor industry, which represents the leading consumer of neon gas in the world.

To address this issue, Gigaphoton, Inc., has started to provide a “Neon Gas Rescue Program” for their DUV lasers, a comprehensive package consisting of three programs that include: the rapid qualification of new gas vendors; a limited-time, free-of-charge implementation of Gigaphoton’s eTGM technology for reducing neon gas usage; and the accelerated introduction of “hTGM” the company’s newest gas recycling technology. This program was developed to provide customers with immediate assistance in addressing the growing challenges in supply and cost of Neon gas, for sustaining a stable high-volume manufacturing environment.

The amount of Neon gas that needs to be injected will depend on the amount of impurities generated during the electrical discharge. The eTGM system employs new gas control algorithms that monitor laser performances to determine the Neon injection parameters. This allows injection volume and timing of Neon gas to become more flexible, that enables to reduce Neon consumption into half amount compared to conventional systems.

Further, the next generation green technology that can recycle Neon gas is under development. This system called hTGM, collects exhausted gas and then removes impurities such as Water, Oxygen and Hydrogen Fluoride by filter. Gigaphoton’s various solutions that enable green manufacturing, are now expanding to world’s fabs and employed to minimize overall cost of operation.

9780-56, Session PTue

## Spatial conversion of excimer laser beam

Alexsandr S. Grishkanich, ITMO Univ. (Russian Federation)

An optical shaper of excimer laser beam that enables the transformation and optimization of spatial characteristics of a coherent UV beam was studied in experimental setting. Experiments revealed that rectangular 3 x 20 mm laser beam with 2 x 5 mrad divergence attained a square shape of 20 x 20 mm and 5 x 5 mrad divergence in orthogonal directions after passing the beam shaper. It is shown that the application of a beam shaper in installations for material microprocessing simplifies optical layout of the illumination module, allows to obtain an optimal homogeneity of sample illumination (under 2%) upon the reproductive image on the processing plane of the sample with submicron precision and to mitigate the radiation load on optical elements via the elimination influence of “hot” spots.

9780-57, Session PTue

## Progress on glass ceramic ZERODUR enabling nanometer precision

Ralf Jedamzik, Clemens Kunisch, Johannes Nieder, Thomas Westerhoff, SCHOTT AG (Germany)

The Semiconductor Industry is making continuous progress in shrinking feature size developing technologies and process to achieve 7 nm feature size. The required Overlay specification for successful production is in the range one nanometer or even smaller. Consequently, materials designed into metrology systems of exposure or inspection tools need to fulfill ever tighter specification on the coefficient of thermal expansion (CTE). The glass ceramic ZERODUR® is a well-established material in critical components of microlithography wafer stepper and offered with an extremely low coefficient of thermal expansion, the tightest tolerance available on market. SCHOTT is continuously improving manufacturing processes and it’s method to measure and characterize the CTE behavior of ZERODUR®. This paper is focusing on the “Advanced Dilatometer” for determination of the CTE developed at SCHOTT in the recent years and introduced into production in Q1 2015. The achievement for improving the absolute CTE measurement accuracy and the reproducibility are described in detail. Those achievements are compared to the CTE measurement accuracy reported by the Physikalische Technische Bundesanstalt (PTB), the National Metrology Institute of Germany. The homogeneity of the CTE is of highest importance to achieve nanometer precision on larger scales. Additionally, the paper presents data on the CTE homogeneity and its improvement in the last two years. The data presented in this paper will explain the capability of ZERODUR® to enable the extreme precision required for future generation of lithography equipment and processes.

9780-58, Session PTue

## Optimal design of wide-view-angle waveplate used for polarimetric diagnosis of lithography system

Honggang Gu, Hao Jiang, Chuanwei Zhang, Xiuguo Chen, Shiyuan Liu, Huazhong Univ. of Science and Technology (China)

For hyper-NA immersion lithography, it is necessary to control and diagnose the polarization effects in the illumination and the projection lenses to improve the imaging quality. Waveplates are basic and indispensable optical elements in such polarimetric diagnosis tools to modulate and analyze the polarization state of the polarized light. A conventional waveplate is usually designed for collimated light at normal incidence, whose retardance varies greatly with the incident angle of light. Since the light beam in a hyper-NA imaging system illuminates the waveplate with a large incident angle, the conventional waveplate is not suitable to be used any more. It is therefore important to design wide-view-angle waveplates to meet the requirements in the applications of polarimetric diagnosis for a lithography system.

In this paper, we present an optimal design method for the wide-view-angle quarter waveplate by combining two positive waveplates made from magnesium fluoride (MgF2) and two negative waveplates made from sapphire, using the simulated annealing algorithm. We derive general formula for the retardance calculation of the birefringent crystal waveplate at arbitrary incident angle based on the theory of wave propagation. Experimental results have confirmed the validity of the retardance calculation theory. To ensure the design process repeatable and reliable, a method to approximate the initial design parameters of the wide-view-angle waveplate is proposed. Further we apply the simulated annealing algorithm to obtain the optimal design of the wide-view-angle waveplate around the initial design parameters. A wide-view-angle quarter waveplate used for polarimetric diagnosis of the 193nm immersion lithography system is optimized using the proposed method as an example. The results demonstrate that the variation in the retardance of the wide-view-angle waveplate is less than ± 0.4° for a wide-view-angle range of ± 20°.

9780-59, Session PTue

## Confocal position alignment in high-precision wavefront error metrology using Shack-Hartmann wavefront sensor

Jiani Su, Zengxiong Lu, Yuejing Qi, Guangyi Liu, Qingbin Meng, Academy of Opto-Electronics (China) and Beijing Excimer Laser Technology and Engineering Ctr. (China)

The aberration inspection of Shack-Hartmann of lithographic lens has reached the nanometer inspection accuracy. Collimator as the key element of the system, the accurate positioning of itself is one important factor for the inspection accuracy. Based on the wavefront reconstruction with Zernike polynomials, in this paper, an optical alignment method for positioning adjustments of the collimator is presented. A sensitivity matrix is obtained from the equation that describes the correlation between Zernike coefficients and the multi-degree-of-freedom misalignment, and the positioning adjustments of collimator are acquired thereof. For the aberration inspection with Shack-Hartmann method, an engineering model of 193nm NA 0.75 projection lens is established in commercial simulating software (ZEMAX). For 0.5nm RMS aberration inspection accuracy, the positioning accuracy of collimator is analyzed and plotted with independent single freedom degree and mutual correlation with combined three freedom degrees. These analysis indicate the proposed method is a viable tool for aligning confocal position of collimator.

9780-60, Session PTue

## SEM signal emulation for 2D patterns

Evgenii Sukhov, Synopsys SPb, LLC (Russian Federation); Thomas Muelders, Ulrich Klostermann, Weimin Gao, Mariya Braylovska, Synopsys GmbH (Germany)

The application of accurate and predictive physical resist simulation is seen as one important use model for fast and efficient exploration of new pattering technology options, especially if fully qualified OPC models are not yet available at a early pre-production stage.

Practically, a resist model is considered as qualified, if no systematic error signatures with respect to experimentally measured wafer CD is observed. The methodology of using a top-down CD-SEM metrology to extract the 3D resist profile information, such as the critical dimension (CD) at various resist heights, has to be associated with a series of presumptions which may introduce such small, but systematic CD errors. Ideally, the metrology effects should be carefully minimized during measurement process, or if possible be taken into account through proper metrology modeling. Typical artifacts are related to resist shrinkage, electron charging effects or simply the CD extraction method from an SEM scan-line, whose signal form is the result of complex interactions of the electron-beam with the resist profile and its neighborhood.

In this paper we discuss the application of a fast SEM signal emulation describing the later phenomena, i.e. SEM image formation. The algorithm is applied to simulated resist 3D profiles and produces emulated SEM image results for 1D and 2D patterns. It allows estimating resist simulation quality by comparing CDs which were extracted from the emulated and from the measured SEM images.

Moreover, SEM emulation is applied for resist model calibration to capture subtle error signatures through dose and defocus. Although more degree of freedom are being added in terms of modeling parameters, the study indicates that the application of CD SEM emulation allows to generate more predictive models than the conventional method of using CDs extracted from simulated profiles.

Finally it should be noted that our SEM emulation methodology is based on the approximation of physical phenomena which are taking place in real SEM image formation. This approximation allows achieving better performance compared to a fully physical model. This approach is essential for deployment of SEM emulation within a resist model calibration process.

9780-61, Session PTue

## Source mask optimization study based on latest Nikon immersion scanner

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The 2x nm logic foundry node has many challenges since critical levels are pushed close to the limits of low k1 ArF water immersion lithography. For these levels, improvements in lithographic performance can translate to decreased re-work and increased yield. Source Mask Optimization (SMO) is one such route to realize these image fidelity improvements. In SMO, critical layout constructs are intensively optimized in both the mask and source domain, resulting in a solution for maximum lithographic entitlement. From the hardware side, advances in source technology have enabled so-called programmable illumination. The approach allows highly customized illumination, enabling the practical application of SMO sources. The customized illumination sources can be adjusted for maximum versatility. In this paper, we present a study on a critical layer of an advanced foundry logic node using the latest ILT based SMO software, paired with state-of-the-art scanner hardware and intelligent illuminator. Both simulation and on-silicon measurements are used to confirm the performance of the studied layer meets established specifications.

9780-62, Session PTue

## CDU budget breakdown as a diagnostic method for imaging sensitivity in HVM

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As leading edge lithography moves to advanced nodes, CDU requirement relatively increased with technologies 14nm/20nm and beyond.

In this paper, we want to introduce the methodology to offer an itemized CDU budget such as Intra-field, Inter-field, wafer to wafer as well as scanner contributors vs. non-scanner contributors (including detailed analysis of reticle contributors like CD, absorber thickness and SWA variation) through Top-Down CDU and Bottom-Up CDU budget breakdown and deliver sources of CD variation with measureable value so that we can estimate CDU gain from them. Test vehicle being used in this experiment is designed based on 14nm D/R basis. Measurement structures are densely located at slit/scan direction on the reticle for the data collection plan. Hence, we can expand on this methodology to build up the tool reference fingerprint when we release new tool fleet.

The final goal will be to establish a methodology for CDU budget breakdown to be used to draw conclusion on the root causes of the observed CDU, propose its improvement strategy and estimate the gain

9780-63, Session PTue

## Inverse polarizer on mask

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The inverse polarizing effect of Sub-Wavelength Metallic Gratings (SWMGs) is employed to improve the lithography performance by controlling the polarization. The SWMGs are intentionally created on the top surface of mask. Its polarization selectivity is deliberately designed according to the bottom mask patterns. To achieve the best lithography performance of two-beam interference, the grating period of SWMGs is chosen to allow only zero-order diffraction to reach bottom mask patterns. A series of simulations and optimizations on SWMG structures can be done to achieve better image quality by enhancing the contrast.

9780-64, Session PTue

## Line-edge roughness frequency analysis for SAQP process

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The self-aligned quadruple patterning (SAQP) is an emerging multi-patterning technique for the semiconductor technology node 10 nm and below. The self-aligned scheme in SAQP greatly reduces the overlay issue comparing with other multi-patterning techniques like litho-etch-litho-etch. However, the line edge roughness (LER) is still a challenge, especially for the case when wiggling exists.

In this paper, the LER transfer in a SAQP process is shown for the first time. All of the three LER characterization methods, including conventional standard deviation method, power spectral density (PSD) method and frequency domain 3-sigma method, are used in the analysis [1]. The wiggling is also quantitatively characterized for each SAQP step with a wiggling factor. This will benefit both process optimization and process monitoring.

Figure 1 shows the CDSEM images for each SAQP step. Figure 2 shows the LER and LWR transfer for each SAQP step, characterized by standard deviation, PSD and frequency domain 3-sigma methods. The largest LER and LWR reductions are from litho to etch step, especially in the middle frequency region. After etch step, LER is kept on the same level while LWR keeps decreasing. The reason for the inconsistence on the LER and LWR reduction is due to wiggling. Although the wiggling is not visible on the CDSEM images, it does exist at a small extent that cannot be detected visually. This is probably due to residual stress.

The wiggling factor is designed to characterize wiggling extent quantitatively. If there is no wiggling, the wiggling factor should be one. The wiggling threshold is set to be 0.9 which is 90% of the maximum value of wiggling factor. In practice case when wiggling factor is larger than this wiggling threshold, wiggling can be believed to disappear. If wiggling starts to increase, wiggling factor changes from one to negative value. The smaller wiggling factor corresponds to larger wiggling extent. The detailed information on wiggling factor can be found in Ref. [1].

Figure 3 shows wiggling factor for each SAQP step. It is a clear trend that wiggling factor reduces from 0.8 to 0.55 from litho to final SAQP step. There is no wiggling factor data for the step from etch to 1st spacer deposition, since there is almost no change for the low frequency LWR in this step. The wiggling factor from Fig. 3 shows that wiggling becomes worse during LER transfer in this SAQP process.

The result from Fig. 3 will greatly benefit process optimization and make the further LER reduction possible, since it is never revealed with the conventional visual inspection method. The wiggling factor and frequency domain 3-sigma method may also help the process monitoring in semiconductor manufacture.

9780-65, Session PTue

## Fabrication of dual-wavelength diffractive beam splitters using maskless optical lithography based on a digital micromirror device

Jun Amako, Toyo Univ. (Japan); Shinozaki Yu, Toyo Univ., Kawagoe (Japan)

We demonstrate a dual-wavelength diffractive beam splitter to be used in parallel laser processing. This novel splitter formed in a transparent material generates two beam arrays at different wavelengths and allows them to overlap at the process points on a workpiece. The splitter has a complex and deep surface profile and needs to be large enough to allow application of expanded laser beams. These requirements constrain the selection of the resist patterning method.

The splitter was stochastically designed using a simulated annealing algorithm by considering the splitting performance, wavelengths, and material dispersion. As an example, for the selected wavelengths of 1064 and 532 nm with 5 splits each, 22 levels were used for a depth of 6.8 ?m and 40 pixels for a period of 1 mm in order to achieve splitting efficiencies greater than 80% and splitting uniformities higher than 0.90. The levels had equal heights, and the pixels had unequal widths. This performance was very sensitive to profile errors: sampling error and depth error. Sampling errors were due to rounding off pixel locations, and depth errors existed in the resist patterning. Fourier analysis simulations showed that tolerances for sampling and depth errors were 1% and 0.5%, respectively.

Fabrication of the proposed splitter requires high resolution, grayscale capability, and high throughput. We therefore selected maskless exposure based on a digital micromirror device (DMD). In a proof-of-principle experiment, the photoresist (AZ P4620, Electronic Materials) was spin-coated to a thickness of ~8?m on a fused silica substrate of diameter 100 mm, and after pre-baking, the resist was patterned using a maskless exposure system (DL-1000, NanoSystem Solutions) equipped with a UV-LED light source and a DMD to form multi-level patterns over a 10 mm ? 10 mm area by scanning the resist substrate in the XY directions. The pattern data for the 5-fan-out-splitter was displayed on the DMD with a resolution of 1024 ? 768 pixels and was projected onto the resist with a 1?m sampling width. The non-linearity in the gamma characteristics of the resist was corrected to minimize depth errors.

The splitter formed in the resist was evaluated using a 3D laser microscope (OLS 4000, Olympus) to profile the surface and using two low-power lasers operating at 1064 and 532 nm to obtain two arrays of 5 split beams. The surface roughness was found to be smaller than ±100 nm, and the efficiency and uniformity were measured to be 76% and 0.58 at 1064 nm and 65% and 0.64 at 532 nm. These results were not satisfactory compared to the theoretical results: 80% and 0.97 at 1064 nm and 82% and 0.94 at 532 nm, and these differences were mainly due to the roughness of the resist surface. This roughness was attributed to luminance variations across the DMD and can be reduced by appropriately mapping them out. This issue is currently under investigation.

Through this study, we showed the feasibility of a diffractive beam splitter that functions at two different wavelengths and clarified the issues remaining to be addressed.

9780-66, Session PTue

## OPC for curved designs in application to photonics on silicon

Bastien Orlando, Vincent Farys, STMicroelectronics (France); Sergei V. Postnikov, Patrick Schiavone, Céline Tranquillin, ASELTA Nanographics (France)

No Abstract Available

9780-67, Session PTue

## Pixel-based mask optimization via particle swarm optimization algorithm for inverse lithography

Lei Wang, Sikun Li, Xiangzhao Wang, Chaoxing Yang, Feng Tang, Shanghai Institute of Optics and Fine Mechanics (China) and Univ. of Chinese Academy of Sciences (China)

No Abstract Available

9780-68, Session PTue

## A physical resist shrinkage model for full-chip lithography simulations

Peng Liu, ASML Brion (United States)

The semiconductor manufacturers are increasingly adopting the negative tone development (NTD) process in their leading-edge lithography applications due to its superior imaging quality compared to the conventional positive tone development (PTD) process [1-2]. While this adoption is critically needed in order to achieve the required process window for the ever-shrinking device feature sizes, it imposes an emerging challenge on the computational lithography tools in terms of model accuracy, especially in full-chip applications such as optical proximity correction (OPC) and verifications where the compact resist models are generally employed. The engineers often find the model forms that have been working very well with the PTD process suddenly perform very poorly on the NTD process, because the resist behaves quite differently in NTD as opposed to PTD, much more than just the reverse tone in the development rate. While the final resist profile in a PTD process is generally dominated by optical effects, it is not true anymore in a NTD process. A very distinctive effect observed in NTD is the resist shrinkage induced by the de-protection reaction during the post-exposure bake (PEB). This effect is not visible in PTD because the resist volume having a high level of de-protection (and therefore shrinkage) is removed by the developer and therefore can be safely ignored in the lithography model [3]. But it is what's left in a NTD process and must be taken into account in NTD resist simulations [4-5].

In this work we present the development of a physical resist shrinkage model for full-chip lithography simulations. It consists of model elements for all essential physical mechanisms that govern the resist shrinkage process as shown in Figs. 1-3. One of the model elements is a resist shrinkage function that models the local resist shrinkage ratio as a function of the local exposure energy in a stress-free or homogenous environment. The typical form of this function is shown in Fig.4. For a given resist, its shrinkage function can be constructed from the experimental data of resist thickness as a function exposure dose [6]. In the simulation, it is used to compute the initial strain distribution in the resist induced by the de-protection reaction in PEB. Another model element is based on the theory of elasticity [7]. It solves the resist deformation problem under the stress caused by the initial strain. Combined with other full-chip lithography models we have developed for the rest lithography processes [8], this physical resist shrink model enables us to significantly improve the model accuracy for full-chip computational lithography applications in NTD.

9780-14, Session 5

## Chronicles of compact lithographic modeling *(Invited Paper)*

Yuri Granik, Mentor Graphics Corp. (United States)

The basic ideas of lithographic modeling come from the seminal papers of Rick Dill, and were realized by Oldham and Neureuther in the SAMPLE simulator.

The necessity for fast compact lithographic models arose in the late 90th along with the emergence of OPC as a "killer application", a technological enabler to print IC features on target.

At that time, fast aerial image methods were being advanced by Neureuther, Barouch, Axelrad, Mack, et. al.

The breakthrou came in 1994 when Pati and Kailath from Stanford and then Cobb from Berkeley proposed to approximate transmission cross-coefficients using either EVD or SVD decompositions (SOCS decomposition).

These methods reduce machinery of optical simulations to a simple series of of convolutions and squarings. As a result, the full-chip optical simulations became attainable in reasonable amount of computer time.

In the same breakthru year, attacking the problem from a different direction, Stirniman and Rieger adapted Gabor filters to model mask-to-wafer pattern transfer an information channel. Aerial image simulations can be viewed as the special case of this filtering method. This "informational" model was the first in the class of so-called "compact process model" that attempted to capture not only optical diffraction, but also other distortion effects originated by the resist processing and etching.

The next round of modeling evolution was prompted by certain limitations of the "informational" model. In particular, it follows from a very general theoretical considerations that the shift-invariant mask-to-wafer transfer operator can be expanded into a Volterra series from which the Gabor filtering and the "informational" model follow. The first term of this expansion is convolution with the mask, and can be utilized for optical flare, or resist fogging modeling. The second term is a bilinear convolution similar to the SOCS model.

The high-order terms become more and more computationally combersome.

And though they suppose to capture weak non-linearities, similar to the Taylor series expansion, it is hard or impossible to accuratly reflect strong non-linear effect that are pertinent to lithographic processing.

The seeding idea of higly non-linear "variable threshold resist" (VTR) model was born in Neureuther's group in Berkeley, and then adapted for OPC by OPC Technology startup. Later more parameters were introduced into this model to capture 2D effects of line-end shortening and microloading.

The first compact model to deal with etch-specific effects, such as aspect ratio dependent etching and microloading, were published by Granik in 2001. The main innovation was intorduction of "visibility" kernels that trace particle fluxes and account for shielding effects of trench walls. In the same publication, we introduced into circulation the term and the concept of a "compact process model" by analogy with the more common collocation "compact device model".

When around 2005-2006 Brion and Mentor OPC simulation engines adopted dense sampling strategies, the shortcomings of VTR model became obvious. The new, "dense" resist model, have to be developed. Taking roots in ideas from Fukuda papers on acid/base interactions during post-exposure baking, Mentor modeling team came up with CM0 and shortly thereafter with CM1 resist models. Novadays, "dense" resist models similar to CM1 are adopted by all major OPC providers, and serve as workhorses of full-chip simulations.

Fastforward to present times, it is hard to name a lithographic effect or process that has not been taken into account by compact models.

Especially challenging appears to be "optical" complications such as accounting for wafer topography during imaging of implantation layers, and thick mask effects.

One of the standing problems is to accurately and quickly model directed self-assembly (DSA). In this presentation, we update on the progress in the development of compact DSA models, and their ability to predict phase transition regimes.

9780-15, Session 5

## Effects of lithography model physics on model-based assist feature placement

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Assist feature (AF) has been widely used in optical proximity correction(OPC) to increase the lithography process window. With the technology nodes continuously shrinking, conventional rule-based AFs are unable to delivery sufficient process window. Many works has been reported using model-based assist feature (MB-AF) placement to further improve the process window needed in advanced nodes. Traditional MB-AF placement approaches use an optical model to place AFs as a tradeoff between productivity and performance. However, as the resolution continues to push downward, a simple optics system is insufficient to describe wafer behaviors. As a result, including more physics in the lithography model, such as the electromagnetic scattering induced by mask 3D topography and the behaviors of photoresist, is a key to successfully enhancing the process window using MB-AF. It would be of lithography engineers' interest to study how these physics terms affect MB-AF placement.

Since limited research addresses this question either theoretically or experimentally, this study investigates how different lithography physics terms impact the effectiveness of MB-AF placement. The model-based placement approach we use is to build a placement map using pixel flipping techniques. With this map, AFs can be heuristically generated to enhance the process window. Among various MB-AF placement approaches that have been reported in the literature, the pixel-based MB-AF placement approach is capable of including various effects of physics (such as the mask 3D effect) in the simulation.

The physics terms concerned in this study are mainly mask 3D effects and chemical resist reactions. The mask 3D effect is attracting much R&D effort because of its importance on large phase assignment and focus variations. To accurately optimize the lithography mask, effects of mask 3D aware model-based AF placement are worth to study. Similarly, in advanced technology nodes, chemical resist effects are widely present and cannot be neglected. Resist terms are developed to predict different characteristics on wafer in terms of feature size, type, or range. Considering an appropriate resist terms for MB-AF placement could be effective to improve process window.

We will report the results of MB-AF placement for structures with simple geometric shapes. The impacts of different physics terms on the accuracy of placement will be studied. By analyzing the effectiveness of MB-AF placement with different physics terms, lithography engineers are able to understand the roles that those model terms play in generating MB-AFs for process window enhancement.

9780-16, Session 5

## Machine learning (ML)-guided OPC using basis functions of polar Fourier transform

Seongbo Shim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of) and KAIST (Korea, Republic of); Suhyeong Choi, Youngsoo Shin, KAIST (Korea, Republic of)

As layout feature size shrinks down, a widely used model-based OPC requires much more time due to higher pattern density and larger simulation time. A few studies have addressed a mask bias prediction method built through machine learning (ML) using some geometry parameters. Typically, a local pattern density around a measurement point of line segment is used as a parameter. It is however not an ideal one because unnecessarily large number of parameters (some hundreds) are required as pattern density increases.

We propose to employ basis functions of polar Fourier transform (PFT) to construct parameters in ML-guided OPC. A basis function is multiplied with a local layout to yield a PFT signal; a set of PFT signals then becomes the input of machine learning process. Inputs are propagated through multi-layer perceptron (MLP) network, while the values are multiplied with some weights assigned on the edges; the output corresponds to the predicted mask bias of line segment. Edge weights are determined in advance through training a number of test segments. The rationale for using PFT basis functions is threefold:

• Efficiency of parameters: Basis functions are orthogonal. Therefore, there is little redundancy in PFT signals, implying that smaller number of parameters (compared to using local pattern densities, for instance) can be used for the same accuracy.

• Ease of implementation: A commercial OPC package usually has internal optical simulator, which uses PFT basis functions. This allows us to implement our method on top of commercial OPC tool with ease.

• Accuracy: PFT basis functions are widely used to model optical diffraction and interference because a light on a wafer is concentrically distributed due to the circular pupil of scanner imaging system. A mask bias is determined by layout's optical characteristic, so it is natural to use PFT basis functions in OPC.

The accuracy of our method is determined by how comprehensive test segments are used for constructing MLP network. We propose efficient segment sampling method. A PFT signal is extracted from each segment in test layouts and arranged as a vector; vectors of all segments are marked in n-dimensional space; we divide the space into grids, and pick only one vector (i.e. one segment) for each grid. Each chosen segment (red dot) is a representative of each grid, so we eventually cover the whole parameter space with smaller number of test segments. In addition, we may apply principal component analysis (PCA) to reduce the dimension of space, which allows further reduction in the number of test segments.

The proposed method is implemented on top of Proteus, which is commercial OPC package available from Synopsys. Our method requires only one lithography simulation (as opposed to multiple simulation runs in conventional OPC), which outputs a set of PFT signals that are used to extract trained mask bias. We compare our method to a few state-of-the-art in terms of runtime and accuracy (e.g. EPE) by using a few industrial memory and logic layouts.

9780-17, Session 5

## Bayesian inference for OPC modeling

Andrew Burbine, Mentor Graphics Corp. (United States) and Rochester Institute of Technology (United States); David Fryer, John L. Sturtevant, Mentor Graphics Corp. (United States); Bruce W. Smith, Rochester Institute of Technology (United States)

The modern use of optical proximity correction (OPC) demands increasingly accurate models of the photolithographic process. Model building and inference techniques in the data science community have seen great strides in the past two decades which make better use of available information. This paper aims to demonstrate the predictive power of Bayesian inference as a method for parameter selection in lithographic models by quantifying the uncertainty associated with model inputs and wafer data. Specifically, this combines the model builder's prior information about each modelling assumption with the maximization of each observation's likelihood as a Student's t-distributed random variable. Through the use of a Markov chain Monte Carlo (MCMC) algorithm, a model's parameter space is explored to find the most credible parameter values. During parameter exploration, the parameters' posterior distributions are generated by applying Bayes' rule, using each model's likelihood and the priors imposed on them. The MCMC algorithm used, the affine invariant ensemble sampler (AIES), is implemented by initializing many walkers which semi-independently explore the parameter space. The convergence of these walkers to global maxima of the likelihood volume determine the parameter values' highest density intervals (HDI) and reveal champion models. We show this method of OPC model parameter selection is more robust to errors in mask and wafer input parameters than traditional methods for lithographic models.

9780-18, Session 5

## OPC recipe optimization using genetic algorithm

Abhishek Asthana, William Wilkinson, Dave Power,

GLOBALFOUNDRIES Inc. (United States)

Due to multiple parameters that need tuning and their correlation, the task of optimization of OPC recipes is not trivial. Usually, no standard methodologies exist for choosing the initial recipe settings, and in the keyword development phase, parameters are chosen either based on previous learning, or to resolve specific problems on some test designs. Such approaches fail to holistically quantify the effects of parameters on other or possible new designs, and to an extent are based on developer's intuition. In addition, when a quick fix is needed for a new design, numerous customization statements are added to the recipe, which make it more complex.

The present work demonstrates the application of Genetic Algorithm (GA) technique for optimizing OPC recipes. GA is a search technique that mimics natural selection and has applications in various science and engineering disciplines. In this case, GA search heuristic is applied to two problems: (a) an overall OPC recipe optimization with respect to selected parameters (b) application of GA to improve printing and via coverage at line end geometries. As will be demonstrated, the optimized recipe significantly reduced the number of ORC violations for case (a). For case (b) line end for various features showed significant printing improvement.

9780-19, Session 5

## Impact of bandwidth variation on OPC model accuracy

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Over the years, Lithography Engineers continue to focus on CD control, overlay and process capability to meet current node requirements for yield and device performance. Reducing or eliminating variability in any process will have significant impact, but the sources of variability in any lithography process are many. The goal from the light source manufacturer is to further enable capability and reduce variation through a number of parameters. (1, 2, 3, 4)

Recent improvements in bandwidth control have been realized in Cymer's XLR® light source platform with Cymer's DynaPulse™ control technology. This reduction in bandwidth variation translates in the further reduction of CD variation in device structures5. The Authors will review the methodology in determining the impact that bandwidth variation has on CD through bias, pitch, dose and focus which is required to build a dynamic model. Figure 1 demonstrates CD change for specific pitches for a target CD of 45nm vs bandwidth with variation of 75fm. Understanding the impact that bandwidth variability has on the accuracy of the Source and Mask optimization and the overall OPC model will be reviewed and demonstrated on leading edge Memory and Logic device structures.

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9780-20, Session 6

## Design technology co-optimization assessment of directed self-assembly-based lithography *(Invited Paper)*

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The majority of DSA research has been focused on demonstrating process and material issues through 1D L/S and 2D hole arrays only. One of the industry's mostly raised question on DSA is "Whether DSA can be applied on real VLSI designs" and the answer is not clear.

DSA is a new patterning concept and how to best use it is not well understood. Should we design for established DSA or we design a new DSA process to suit our design?

We attempt to give a preliminary answer by conducting a quantitative DTCO study for finding an optimal DSA process-design combination for 7nm logic node and beyond. We demonstrate a quantitative DTCO by using our in-house computational Lithography toolset and DSA simulation tools [1, 2], and verified by wafer data if possible.

This work was performed by the Research and Development Alliance Teams at various IBM Research and Development facilities.

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9780-21, Session 6

## An integrated source/mask/DSA optimization approach

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With a view to establish it as a cost-efficient alternative to extreme ultra-violet lithography (EUVL) or pattern multiplication techniques, the directed self-assembly (DSA) of block copolymers (BCPs) has become a subject of intense research and development. Currently, the introduction of DSA for lithography is still obstructed mainly by an insufficient understanding of defect formation, the non-availability of suited materials for smaller features sizes and the lack of a comprehensive computational platform. This work presents an approach to jointly optimize the lithography/DSA co-process by taking a lithography-centric view, tightly embedding the DSA simulation into the conventional lithography process computation flow.

For that purpose, we have devised a direct source/mask/DSA optimization (SMDSAO) method, which incorporates standard lithographic metrics and figures of merit such as the maximization of the process window. While related approaches commonly divide the problem into two stages—(1) the search for an optimum guide pattern and (2) a source/mask optimization to obtain that pattern, the approach proposed here considers only the final result of the entire co-process. This technique is demonstrated for a contact doubling example, assuming grapho-epitaxy-DSA. To retain a feasible runtime of the procedure, a reduced, two-dimensional interface Hamiltonian-based DSA model is employed: Given a confinement, the model seeks a phase interface—of the inner cylinder, in the context of contact holes—that minimizes the free energy. The model is highly efficient but only approximates the shape and the position of the profile in a strong segregation regime, completely neglecting thermal effects. To conveniently infer the free energy, a Legendre polynomial representation is chosen, which—using polar coordinates—proved well-suited in the case of contact holes.

The general flow of the proposed routine can be broadly outlined as follows:

Each candidate solution consists of an optimizer-generated source and mask setting. The corresponding bulk images or the resist profiles are computed. If the pattern severely fails to meet elementary fidelity criteria (for example, if no pattern is generated), the solution is rejected. Otherwise, a side-lobe printing risk is determined, and the candidate is penalized accordingly.

Afterward, the Legendre polynomial representation is extracted from the lithography pattern. The shape of the inner cylinder is determined by the interface Hamiltonian model. The profile is evaluated in terms of placement and x and y-CDs. To enable a full-fledged process window optimization, the lithography steps are conducted for different focus and dose settings, leading to the usual process window, however, for CDs obtained after DSA. Specifically, the ultimate optimization goal is to maximize the process window due to x and y CDs. As an optimization routine, a multi-objective evolutionary algorithm is employed. For verification, the final result is evaluated using two additional models: a continuum model using the Ohta-Kawasaki formulation and a coarse-grained particle approach (single chain mean field). The feasibility of this approach is demonstrated through several results and their comparison with the more exact DSA models.

9780-22, Session 6

## Multi-layer VEB model: capturing interlayer etch process effects for self-aligned via in multi-patterning process scheme

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Self-Aligned VIA (SAV) process is commonly used in back end of line (BEOL) patterning. As the technology node advances, tightening CD and overlay specs requires continuous improvement in model accuracy of the SAV process. Traditional single layer Variable Etch Bias (VEB) model is capable of describing the micro-loading and aperture effects associated with reactive ion etch (RIE), but it does not include effects from under layers. For the SAV etch, a multi-layer VEB model is needed to account for the etch restriction from the metal trenches. In this study, we characterize via post-etch dimensions through pitch and through metal trench widths, and show that VEB model prediction accuracy for SAV CDs after SAV formation can be significantly improved by applying a multi-layer scheme. Using a multi-layer VEB, it is demonstrated that the output via size changes with varying trench dimensions, which matches with silicon results. The model also reports via shape post-etch as a function of trench environment, where elliptical vias are correctly produced. The multi-layer VEB model can be applied both multi-layer correction and verification in full chip flow. This paper will also suggest that the multi-layer VEB can be used in other FEOL layers that have similar interlayer etch process effects, such as gate cut, to support the robustness of new model.

9780-23, Session 6

## Mask defect printability in the self-aligned quadruple patterning (SAQP) process

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The half pitch (HP) of lines and spaces (L/S) patterns for fabricating fine metal layers becomes less than 20nm in accordance with the shrinkage of semiconductor devices. Unfortunately, Immersion exposure technique using 193-nm immersion scanners with hyper NA (1.35NA) lenses cannot resolve the under-20nm HP patterns. Self-aligned quadruple patterning (SAQP) process is one of the most suitable techniques for the fabricating of under-20nm HP lines and spaces patterns because the process cost is relatively low due that the process needs only one lithography step. In the SAQP process, It is possible to form a 1/4 HP pattern of the pattern of the core material by repeating the fabrication of sidewall spacer two times. One of the most serious problems for applying the SAQP process to the real devices is the printability of the defects of the photomask to wafer, because the effect of the mask defects may be enlarged when the defects are transferred to the spacer pattern. Our group showed that in the self-aligned double patterning (SADP) process, where 32nm L/S patterns were made, the effect of mask defects was suppressed at the spacer pattern due that the defect size became small at the fabrication of the spacer pattern [1].

In the present study, we evaluated the printability of the mask defects to wafer at the SAQP process in order to clarify the limit size of defects of the photomask. We made ~60nm HP lines and spaces patterns by using an ArF immersion scanner. At the lithography, a special mask which had several kinds of programmed defects (both opaque and clear type) was used. After the development, the resist L/S patterns was transferred to a hard mask by RIE. Then the first spacer pattern, whose HP was ~30nm, was made at the both sides of the hard mask pattern. After the hard mask was removed, the first spacer pattern was transferred to the second hard mask by RIE. Then the second spacer pattern, whose HP was ~15nm, was made at the both sides of the second hard mask pattern, and the second hard mask was removed. Then the mask defect printability was investigated by measuring the defect sizes of the programmed mask defects at lithography, at the fabrication of the first spacer, and at fabrication of the second spacer. We found that the defect sizes became smaller when sidewall spacer process proceeds. For instance, the printed size of one of the programmed mask defects at lithography, at the fabrication of the first spacer, and at the fabrication of the second spacer was 5.0%, 4.3%, and 3.8% of resist HP, respectively. This means that the defect size becomes smaller not only at the fabrication of the first spacer pattern but also at the fabrication of the second spacer pattern, which indicates that the effect of the mask defects in the SAQP process is smaller than expected. Therefore, the mask defects can be controlled and the SAQP process can be applied to the real devices.

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9780-24, Session 7

## Standard cell pin access and physical design in advanced lithography *(Invited Paper)*

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No Abstract Available

9780-25, Session 7

## Incorporating photomask shape uncertainty in computational lithography

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Uncertainties exist broadly in lithographic systems and have a significant influence on lithographic modeling and optimization. Previously, the uncertainty regarding dose and focus is investigated to measure their impact on the imaging quality. The maximization of process window which measures the tolerable exposure and dose variation under a given critical dimension (CD) error is an important objective in lithographic optimization. The uncertainty of other parameters, such as the wavelength, numerical aperture (NA), and photomask parameters is also explored to evaluate the accuracy of using lithographic modeling to predict the performance of imaging systems.

This work focuses on the shape uncertainty of the photomask and considers the uncertainty in computational lithography. Due to manufacturing and measurement errors of the photomask, shape uncertainty is usually unavoidable. The uncertainty includes line-width error such as CD bias and line-edge roughness. Simulations using rigorous electromagnetic field theory are conducted to evaluate its influence on the lithographic processes and the results show that the image quality is sensitive to such uncertainties. The profile of the photomask patterns is characterized with single-frequency method or Fourier transform algorithm to model the line-width bias and edge roughness. However, few studies have been done to consider this uncertainty in computational lithography since it is usually computationally intractable to incorporate the shape uncertainty in inverse lithography.

In this paper, the shape uncertainty of the photomask pattern is explored within a level-set mask representation framework, which is commonly used in inverse lithography. The level-set function is represented by a random field, which is a statistical process to represent multi-dimensional vectors. The Karhunen-Loeve (K-L) expansion method is introduced to represent the random field with the eigenfunctions and eigenvalues of random field's covariance function. With this method, the shape uncertainty can be characterized with only several random variables, which make it possible to be incorporated in inverse lithography. Then, a min-max algorithm is used to optimize the mask pattern to further reduce the computational complexity. Simulations are performed to model such shape uncertainties, and inverse lithography is conducted to show the effectiveness of such methods.

The shape uncertainty is shown in Fig. 1, where we can see the representation using the proposed method is quite effective. Several nanometers' differences are shown among the different realization of contours. However, the process windows of the perturbed mask changes obviously according to the mask. Inverse lithography considering the shape uncertainty is performed, and the result is shown in Fig. 2. For a given pattern, the optimization is performed using both the traditional ILT and the proposed ILT with shape uncertainty. The values of cost function over a random space are depicted in the figure. It is shown that in most cases, the values considering the uncertainty is smaller than the ones without accounting the uncertainty. The results obviously show that optimization can effectively increase the robustness of the optimized mask to the shape uncertainty.

9780-26, Session 8

## Alternative high-resolution lithographic technologies for optical applications *(Invited Paper)*

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Compared to the lithographic realization of nano-structures for micro-electronics the demands of optical applications on the lithographic fabrication technologies are different. This relates to the lateral shape of the structures as well as to their three dimensional surface profile. On the other hand optical nano-structures are often periodic which allows for the use of dedicated lithographic exposure principles not applicable for the structuring of IC pattern.

In the presentation an overview of some actual lithographic technologies will be given specially developed for the realization of high resolution optical nano-structures. This includes a special electron-beam lithographic exposure technique for high-quality and high resolution sub-wavelength pattern generation and the diffractive mask aligner lithography for cost-effective fabrication of large area 3-dimensional optical nano-structures.

Electron-beam lithography using the Variable Shaped Beam (VSB) writing principle is a suitable and very flexible fabrication technique to address the needs of optical applications. It is based on an exposure with extended geometrical primitives like rectangles or triangles of flexible size. In case of periodic pattern as they are found in optical elements like photonic crystals or meta-materials, the VSB writing principle can be further extended by a so called character projection where complex exposure pattern are coded in a stencil mask and exposed with a single shot. Resulting shot-count and thus writing time reductions can be in the order of about 100...10000. The realization of numerous kinds of elements on larger areas becomes possible only with such a highly parallel writing strategy. The flexibility for generating arbitrary pattern is maintained by a specially developed diaphragm stage offering to combine more than 500 different exposure characters in a single layout.

The second technique to be discussed in more detail is the mask aligner lithography utilizing diffractive photo masks. It has opened a way towards a cost-effective fabrication of high resolution nano-structures with feature sizes below 200nm. This approach thus overcomes the typical limitations of conventional shadow printing mask-aligner exposures and moves its resolution limit by at least one order of magnitude. In the last few years we have demonstrated the huge application potential of diffractive mask-aligner lithography by the realization of different micro- and nano-structures with demanding quality criterions such as highly efficient pulse compression gratings, wire-grid polarizers for wavelengths down to 400nm, plasmonic absorbers, or non-periodic pattern with micrometer resolution.

In the contribution we will show what could be the necessary next development steps for further improving the diffractive mask-aligner technology, especially towards the realization of three-dimensional surface profiles. For this purpose we have implemented two additional changes in the mask-aligner. First, the conventional Mercury arc-lamp has been replaced by a specially designed laser illumination. It includes dedicated means for an effective speckle reduction and homogenization as well as a computer controlled scanning system. The second extension is a piezo-controlled lateral alignment between mask and substrate which allows performing multiple exposures with lateral shifting the mask by a given distance in between the single exposures. In combination with the pattern transfer by diffraction effects both modifications can be used generate locally varying exposure intensities and thus a three-dimensional surface profile after the resist development process.

Examples of micro-structures generated by the novel exposure techniques will be shown.

9780-27, Session 8

## Optical lithography on a V-grooved substrate for 3D nanofabrication

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Semiconductor fabrication is currently rapidly extending towards three-dimensional (3D) integration. State-of-the-art integrated circuits are already highly multi-layered and effectively represent a 3D structure. Nevertheless, each layer within the stack is fabricated by planar technology and therefore overlay is a central concern in such a layer-by-layer approach. To solve this issue, first steps were accurately taken to fabricate 3D nanostructures with only one alignment step [1]. We present an original method to use conventional deep-UV lithography in combination with a pre-structured substrate to pattern monolithic 3D nanostructures in only one step, with ensured out-of-plane alignment [2].

The novel method overcomes overlay issues by starting the fabrication from a pre-structured wafer that already contains a three-dimensional structure. For a proof-of-concept experiment we use a Si wafer structured with V-shaped trenches. The trenches are etched using anisotropic KOH etching of silicon. We spin coat a back anti-reflection coating (BARC) and a photoresist layer on the wafer using an optimized recipe that provides a homogeneous covering of the trench slopes over at least 1.5 micron depth. We managed to control photoresist thickness over the wafer by fabricating trenches with a different width. After the photoresist is applied, multiple UV exposures are performed to achieve a sufficiently large depth of focus and obtain resist exposures over a slope. We demonstrate resist development on a slope of V-trenches on a Si wafer, and we show first photonic band gap crystals mask with this method.

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9780-28, Session 8

## High dynamic grayscale lithography with an LED based microimage stepper

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We developed a novel LED projection based direct write grayscale lithography system for the fabrication of freeform surfaces such as micro-lenses, diffusors and diffractive optics. We show the benefit of this new technology concerning high dynamic control of the dosage, which is realized by a combination of an exposure intensity control within the micro image in and a variable exposure dose. The image generation is realized by a LCoS micro-display which is illuminated by a 405nm UV High Power LED, which can be controlled in power and exposure time. The Image on the display is demagnified with an exchangeable lens with ratios between 5x to 100x.

The presented technique enables a highly dynamic dosage control. Together with an accurate calibration of the resist response this leads to a superior low surface error of the fabricated profiles (<0.2% RMS). The exposure concept allows a high structure depth of >100µm and a spatial resolution below 1µm as well as the possibility of very steep edges in the profiles of (>80°). Another benefit of the concept is a high patterning speed up to 100cm?/h which allows the fabrication of large scale optics and microstructures. The micro-display can be moved in the XY-direction and can be rotated for precise alignment. The substrate is brought into position with an air bearing stage with an accessible area of 500x500mm? and the accuracy of the positioning is <100nm. As the exposure setup can also be moved in the z-direction the system also allows a layer-wise exposure of curved substrates. In the presented publication we will describe the setup and show examples of micro-structures. We demonstrate the performance of the system with the fabrication of a refractive freeform array, where the RMS surface deviation does not exceed 0.2% of the total structure depth of 50µm. Further we show that this structuring technology is suitable to generate diffractive optical elements as well as freeform optics and arrays with a high aspect ratio and structure depth showing a superior optical performance. Last we demonstrate a multi-height-level diffraction grating on a curved substrate.

9780-29, Session 8

## Firefly: an optical lithographic system for the fabrication of holographic security labels

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This paper introduces Firefly, an optical microlithography origination system that has been developed at Combustion Ingenieros S.A.S, Bogotá-Colombia in order to produce holographic masters of high quality. The lithographic maskless system has a resolution of 500 nm half-pitch, and generates holograms (holographic masters) with the optical characteristics required for security applications of level 1 (visual verification), level 2 (pocket reader verification) and level 3 (forensic verification). The holographic master constitutes the main core of the manufacturing process of security holographic labels used for the authentication of products and documents worldwide.

Additionally, the Firefly is equipped with a software tool that allows for the hologram design from graphic formats stored in bit maps. The software is capable of generate and configure basic optical effects such as animation and color, as well as effects of high complexity such as Fresnel lenses, engraves and encrypted images, among others.

The Firefly technology gathers together arts, optical lithography, image digital processing and the most advanced control systems, making possible a competitive equipment that challenges the best technologies in the industry of holographic generation around the world. In this paper, a general description of the origination system is provided as well as some examples of its capabilities.

9780-30, Session 8

## Phase analysis of binary mask structures

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Printing industry needs solutions for printing structures with desired structure features. The current ways to improve resolution are phase shifting mask (PSM), optical proximity correction (OPC) and off axis illumination (OAI). A cost effective solution to do the printing would be using binary mask with simple correction structures and operate in proximity. The amplitude or intensity characteristics of the structure in a binary mask at different proximity gaps has been analyzed extensively for many industrial applications. But the phase evolution from the binary mask having OPC structures is not considered so far. But it is the phase which will allow particular high resolution structures through design of darkness at phase singularities. In this paper we provide a detailed analysis of the phase evolution from a corrected structure. The aim is to understand underlying principles and find practical rules to be used in design.

The analysis has been done with an instrument called High Resolution Interference Microscopy (HRIM), a Mach – Zehnder interferometer which gives access to phase and amplitude of aerial images behind photomasks. The source of illumination for phase measurements is a wavelength stabilized Laser (Toptica Topmode laser with CHARM control) having a wavelength of 405nm. The wavelength simulate the wavelength regime of proximity printing industry. The mask under observation is placed in the

object arm and measurement are done by scanning from focus (mask plane) to different proximity gaps with a high resolution objective (Leica HCX APO, 50X/ NA 0.9). For each distance an interferogram is recorded by a camera (Scion Corporation, CFW1312M camera with SONY ICX205AK). The phase profiles are evaluated using the Schwider – Hariharan algorithm with the help of a moving mirror in reference arm.

The current paper emphasis on the phase measurement of different optical proximity correction structures and especially for corners on a binary mask. The corner structures represent a two dimensional problem which is difficult to handle in with simple rules of phase masks design and therefore of particular interest. The additional correction structures are simple squares and rectangles which will help to print the corners more precisely. The structures are designed for a proximity gap of 30 μm. It is known that phase shifting mask giving rise to phase singularities which lead to better structure definition. The use of small amplitude correction features to simulate sharp phase features is not yet discussed in literature. Here we want to explore the potential of such an approach.

As an example we show results for an OPC structure that is composed out of 3 squares around a corner. Amplitude and phase measurement at 0, 15 and 30 micron are presented as well as a profile of intensity phase in the propagation direction at a specific position. One recognizes already sharp propagating phase changes in the x-z profile and specific phase humps at the square positions in the x-y phase images. In our contribution we will discuss in detail the influence of different correction structures on amplitude and phase and draw conclusions for lithography proximity printing application.

9780-31, Session 9

## Patterned wafer geometry (PWG) metrology for improving process-induced overlay and focus problems *(Invited Paper)*

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Prime silicon wafers are ideal substrates for lithographic patterning, with tight flatness specifications for focus control. Process engineers are painfully aware that in-process product wafers can substantially depart from this ideal substrate. Wafer processing can induce non-flatness leading to focus problems, or distort the wafer leading to overlay issues. Thus processes from outside the lithography sector can impact yield by ruining lithographic pattern quality.

Double-sided optical interferometric metrology is the standard method to assess the flatness of blank silicon wafers. In the last several years, a similar Patterned Wafer Geometry (PWG) metrology tool is able to measure in-process patterned wafers. This paper will survey some of the applications of PWG data to characterize and mitigate process-induced yield problems. The apparent surface seen by the interferometer may be different than the true top or bottom surface, due to transparent thin films, a discrepancy that we call “false topography”. The paper will include modeling of such effects, along with some experimental data using an opaque film to reduce the problem.

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9780-32, Session 9

## Improvement of unbalanced illumination induced telecentricity within the exposure slit

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Telecentricity is an important parameter for wafer alignment and overlay in the lithography process. Normal (geometric) telecentricity, which is induced by illuminator misalignment, induces translation of the aerial image through focus and has no pitch dependency. However, telecentricity (energetic) also can also be induced by pupil imbalance.

The exposure slit of the scanner can show pupil variation across the slit. In general the pole balance reduced at the edge of the slit compared to the middle of the slit. Recently, ASML implemented pupil balance improvements across the slit. With this new method, pupil balance variation is improved and telecentricity at the edge of the slit is reduced significantly.

9780-33, Session 10

## High-order aberration control during exposure for leading-edge lithography projection optics

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High throughput with high resolution imaging has been key for the leading-edge microlithography. However, to simultaneously achieve high throughput and high resolution, management of thermal aberrations due to lens heating during exposure becomes a critical issue. Thermal aberrations cause CD drift and overlay error, and these errors lead directly to edge placement errors (EPE). The use of off-axis illumination and/or freeform illumination for resolution enhancement increases the probability of high order aberrations due to strongly-localized lens heating. One of the most severe exposure conditions for thermal aberrations is the thin dipole illumination condition, which localizes light energy in the lens pupil. In this case, we usually have a considerable amount of thermally induced uniform astigmatism. This astigmatism includes not only the Z5 Zernike polynomial wavefront term, but also Z12, Z17 and even higher order terms: the ratio depends on the dipole shape. Finer and finer pattern generation in semiconductors requires further aberration reduction of the projection lens due to higher error sensitivity for imaging performance. Therefore, management and control of high order thermal aberrations is a critical requirement.

We have developed a new thermal aberration control system. It consists of a multi-drive-axis dynamic deformable mirror (MDDM) and thermal aberration adjuster across the field (TAAAF). The MDDM is integrated into the projection optics with a deformable mirror and high-accuracy piezo-driven hardware. This unit can work to control the high-order wavefront shot-by-shot with high-response. The dominant component of thermal aberrations under all illumination conditions is the wavefront error distributed uniformly across the image field. The MDDM can control this error up to the 28th Zernike polynomial. The TAAAF can control the non-uniformly-distributed wavefront across the field. The magnitude of the distributed wavefront errors is not so large but has a high impact on overlay error; in particular, odd-order components of the residual aberrations increase sensitivity of measured overlay mark shift to small variations of the off-axis illumination.

Thus we have developed TAAAF for overlay enhancement.

In this paper, we will show practical performance of the lens heating with dipole and other typical illumination conditions for finer patterning. We confirm that our new control system can reduce the high-order aberrations and show critical-dimension uniformity CDU and overlay enhancement during the exposure.

9780-34, Session 10

## DUV light source technologies for 10nm and 3D NAND

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Deep UV light sources continue to be extended into 10nm node applications through the use of multi-patterning techniques as well as vertically integrated devices used for 3D NAND applications. While 3D NAND devices rely more heavily on earlier-generation 248nm light sources, the 10nm logic and DRAM devices continue to drive advanced ArF immersion patterning techniques to achieve high resolution lithography. This paper will cover recent advances in light source technologies such as tighter bandwidth control to support larger focus budgets, lower bandwidth to improve image contrast and support enhanced optical proximity correction techniques[1,2], as well as lower running costs needed to offset the complexities of increasing number of patterning layers. Recently, several studies exploring the impact of bandwidth on imaging performance have suggested that reducing light source bandwidth variability[3] can expand the focus budget as it is equivalent to reducing blur in imaging and ultimately critical dimension uniformity. Additionally, lowering the absolute bandwidth target has enabled contrast improvements that also improve CD uniformity[4]. In the case of 3D NAND devices, cost-effective solutions are achieved through the creation of vertical devices that require more 248nm lithography layers and these in turn drive the need for increased throughput for further cost efficiencies. This paper will also report on recent improvements in 248nm light source technology where the output power has been increased from 40 to 50W, enabling higher throughput and lower cost per layer that is leveraged in the production of 3D NAND devices.

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9780-35, Session 10

## The ArF laser for the next-generation multiple-patterning immersion lithography supporting green operations

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Multiple patterning ArF immersion lithography has been expected as the promising technology to satisfy tighter leading edge device requirements. One of the most important features of the next generation lasers will be the ability to support green operations while further improving cost of ownership and performance. Especially, the dependence on rare gases, such as neon and helium, is becoming a critical issue for HVM process. The new ArF excimer laser, GT64A has been developed to cope with the reduction of operational costs, the prevention against rare resource shortage and the improvement of device yield in multiple-patterning lithography.

Based on the field-proven injection-lock twin-chamber platform, GT64A has advantages in efficiency and stability and this leads to cost-effective green operations while improving performance. The first is the reduction of gas usage. One is neon. More than 96% of the gas used in the lasers is neon. Another gas that requires attention is helium. Recently the unstable supply and the shortage supply of neon and helium became a serious worldwide issue. To cope with this situation, Gigaphoton is developing lasers that support reduction of neon usage and completely helium-free operations. The injection-lock twin-chamber platform has capability to execute a new advanced gas control algorithm in which parameters, such as input power and gas pressure are closely monitored during operations and fed back to the injection/exhaust gas controller system. By introducing this new gas control to twin-chamber platform, the laser gas consumption can be reduced by up to 50%.

And newly designed Line Narrowing Module can realize completely helium free operation. Even without helium gas purge, the spectral bandwidth becomes equal to that of the conventional helium purge. Narrower spectral bandwidth enhances image contrast and therefore enables the excellent CD control for device manufacturers.

Other basic improvement applied to the GT64A is spectral bandwidth stability. Gigaphoton originally developed the control method using optical components for the variable bandwidth. The combination of optical components and actuator allows control of the spectrum. The spacing between these two optical components can be adjusted to make the spectrum variable. The new spectral bandwidth control algorithm has already been developed to compensate the offset due to thermal change during the interval such as the period of wafer exchange operation. Spectral bandwidth stability will be improved further by developing the actuator with high response speed. The improvement in spectral bandwidth stability contributes to the further reduction of CD variation.

Finally, from the system point of view, REDeeM Cloud™, new monitoring system for managing light source performance and operations, is on-board and provides detailed light source information such as wavelength, energy, E95, etc.

These technologies and the detailed properties of GT64A will be discussed in detail.

9780-36, Session 10

## NXT:1980Di immersion scanner for 7nm and 5nm production nodes

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Immersion scanners remain the critical lithography workhorses in semiconductor device manufacturing. When progressing towards the 7nm & 5-nm device nodes, pattern-placement and layer-to-layer overlay requirements keep progressively scaling down and consequently require system improvements in immersion scanners. The on-product-overlay requirements are approaching levels of only a few nanometers, imposing stringent requirements on the scanner tool design in terms of reproducibility, accuracy and stability.

In this paper we report on the performance of the NXT:1980Di immersion scanner. The NXT:1980Di builds upon the NXT:1970Ci, that is widely used for 16 and 14nm high-volume manufacturing. We will discuss the NXT:1980Di system- and sub-system/module enhancements (e.g. more accurate machine calibration, reduced disturbance levels) that drive the scanner overlay (DCO/MMO), focus (LVT) and productivity performance. Overlay, focus, and productivity data will be presented for multiple tools.

To further reduce the on-product overlay system performance, alignment sensor improvements (contrast) as well as active reticle temperature

conditioning are implemented on the NXT:1980Di. Both developments are instrumental in extending the application range of reticle usage, and in extending the registration-robustness of alignment markers towards the effects of the various post-litho steps, enlarging the solution space of process integration of semiconductor device manufacturing.

NXT:1980Di productivity scanner design modifications raised productivity levels from 250wph to 275wph, providing lower layer costs for customers using immersion technology.

In concert with these scanner advancements, integrated metrology and computational lithography will remain necessary to supplement & maintain the performance of the state-of-the-art immersion machines in high-volume manufacturing.

9780-37, Session 10

## Next-generation immersion scanner optimizing on-product performance for 7nm node

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The semiconductor technology roadmap suggests that multiple patterning techniques will be used at the 7nm node, and continuous improvements in on-product accuracy and yield will be required. The final lithography accuracy is determined by what is known as the “on-product” performance, which includes projection lens heating, illumination condition variations, product wafer-related errors, and long-term stability. It is evident that on-product performance improvement is imperative now, and will become even more crucial in coming years. Today, the cutting-edge Nikon NSR-S630D immersion lithography scanner is demonstrating high performance at a number of manufacturing facilities worldwide. In order to continue to meet customers’ future requirements, Nikon has developed the next-generation lithography system focusing on optimizing the main factors impacting on-product performance.

The first essential advancement involves the next-generation scanner’s projection lens, which is equipped with a newly developed thermal aberration control system. This control system consists of the Multi-drive-axis Dynamic Deformable Mirror (MDDM), as well as the Thermal Aberration Adjuster Across the Field (TAAAF). This sophisticated system can reduce high order aberrations, and thereby improve CDU and overlay, without any adverse throughput impacts. The second critical area of innovation is the FIA alignment microscope that provides enhanced alignment mark measurement repeatability. This is due to changes in the FIA image sensor as well as the FIA water cooling system. The new FIA light source also increases the light intensity substantially. As a result of these numerous advances, FIA alignment is expected to deliver better measurement precision for product alignment marks that are typically more challenging to detect.

Several other subsystems on the next-generation scanner have been redesigned as well to provide heightened on-product performance. In addition, the total scanner management system based on the Plug & Play Manager (PPM) introduced at SPIE AL 2015 has been operating successfully at a number of customer sites. The Nikon turnkey solution includes the PPM as well as Zeroing functions that improve overall scanner performance and productivity, and also reduce operator workload. The Zeroing functions provide automatic overlay and focus compensation, enabling increased long-term scanner stability.

There is little doubt that these vital new developments coupled with the mature Streamlign platform will help customers achieve their aggressive accuracy and productivity requirements. In this presentation, we will introduce the details of the next-generation Nikon scanner and provide supporting performance data.

9780-50, Session 10

## Investigation of systematic CD distribution error on intrafield

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As feature size shrinks, better critical dimension uniformity (CDU) is highly demanded in aspects of device characteristics. Intra field CDU is one of main contributor in total CD variation budget. Especially systematic CD distribution in shot, bank and MAT boundary should be strongly considered to minimize repeated error to guarantee high yield even though it is not prominent in overall CDU value.

In this paper, we investigated the several factors to affect systematic CD distribution error on intra field. First of all, localized mask CD variation caused by electron-beam scattering over local region, development loading and etch loading effect directly printed in wafer. Appropriate mask fabrication suppress CD variation at boundary region. Secondly, chemical flare effect is expected to make CD gradient at boundary region. Photo acid concentration change by sub-resolution assist feature (SRAF) can reduce the CD gradient. We demonstrated SRAF size dependency in positive tone develop (PTD) and negative tone develop (NTD) case. Thirdly, out-of-field stray light due to adjacent exposed field causes CD gradient at field boundary. Exposure dose reduction is expected as a solution in this case. Even though we perfectly control CDU at boundary region after mask patterning, other process issues such as etch and CMP loading effect also make worse the CD distribution at boundary region.

Through the consideration of above factors, we optimized systematic CD distribution error at boundary region before etch. Furthermore we compared several techniques to compensate post-etch systematic CD distribution.

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9781-1, Session 1

## Toward the 5nm technology: layout optimization and performance benchmark for logic/SRAMs using lateral and vertical GAA FETs *(Invited Paper)*

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The scalability of thin-body devices like FinFETs at the 5nm node and beyond technologies is in question if the subthreshold slope (SS) and short-channel effects (SCEs) need to be maintained. GAA nanowire transistors (LFET) can offer a superior control of the gate over the fully-depleted channel and allow to further scale the gate length to 15 nm with the nanowire (NW) diameter of 4-7 nm. However, in a conventional 2D layout, the gate length, sidewall spacers and source/drain contacts will compete for space within the devices' pitch. Additionally, an ultra-thin channel could also potentially degrade the carrier mobility due to a strong quantum confinement. To overcome these challenges, a more disruptive architecture called vertical GAA FETs (VFET) is being considered as a promising candidate for sub-5nm nodes. In VFETs, the gate length is defined by the thickness of the high-k/metal-gate and is not confined by the device's footprint. In VFET layouts, the freedom in the ordering of the devices could enable a further layout optimization for improving routing resources and area density.

SRAM area are always used as a metric for benchmarking technology platforms. The required density scaling of SRAMs has forced an aggressive metal pitch (MP) and gate pitch (CGP) and demanded multiple EUV exposures to meet the tip-to-tip constraints. Meanwhile, the CMOS scaling has placed SRAMs into the regime where it is substantially hard to meet the performance, energy and density requirements. The 2X density scaling trend has made SRAMs more prone to process variability and difficult to compromise read and write margins. Consequently, the ability of SRAM scaling will rely on the co-optimization of lithography solutions, novel device architectures and circuit techniques.

In this paper, we present a layout and performance analysis of logic and SRAM circuits for vertical and lateral GAA FETs using 5nm design rules. EUVL processes are exploited to print the critical features (32 nm MP and 24 nm CGP). Patterning compromises for enabling the 5nm node will be discussed in details. Process variability (PV) bands are simulated to assess the robustness of different layout choices. A distinct layout architecture for vertical FETs is proposed and elaborated for the first time. The proposed layout construct can improve the port accessibility significantly, which helps to reduce routing congestions at PnR level. For a high performance standard-cell library, the advantage of the vertical architecture is diminished due to the strong drive current constraint. Using an assumption of two vertically-stacked layers of nanowires for LFETs, the standard-cell area delivered by the VFET and LFET architectures is equivalent. A BSIM-CMG model has been built and calibrated with TCAD simulations, which account for the quasi-ballistic transport in the nanowire channel. The resulting simulations show that the vertical SRAMs outperform the lateral SRAMs. At iso-performance, the standby leakage of vertical SRAMs is 2.6X lower than LFET-based SRAMs. Using the same design rules, the vertical bitcells are 20-30% denser than lateral bitcells. Without assist circuit techniques, the 122 bitcell will become the high-density (HD) bitcell and simplify the cut mask requirements for the NW layer.

9781-2, Session 1

## Structural design, layout analysis and routing strategy for constructing IC standard cells using vertical gate-all-around nanowire MOSFETs

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As optical lithography and conventional transistor structure are approaching their physical limits, 3D vertical gate-all-around (GAA) nanowire MOSFETs is widely considered as a promising device candidate for post-FinFET logic scaling owing to its superior gate control and scaling potential. However, source and drain of a vertical nanowire MOSFET are oriented in the vertical direction. Consequently, structural design of IC devices/circuits, layout arrangement for high-density vertical nanowires/interconnects, and routing strategy are non-trivial challenges. In this paper, we shall discuss these critical issues for constructing standard cells using 3D vertical GAA nanowire MOSFETs.

A conceptual GAA nanowire MOSFET device structure with local interconnects is illustrated in Fig. 1. In this structure, the metal gate is surrounding the nanowire column and sandwiched between two oxide layers. Contact holes will be etched through the top and bottom oxide layer and filled with interconnecting metal. Such a gate and metal connecting manner suggests that the wires should be routed on two layers, e.g., called T-layer and B-layer (see Fig. 6). In a routing layout design, gates may be connected to metal wires on T or B layer (Fig. 2). Specifically, if the gate is connected to metal wires in T and B layers simultaneously, such a device can be used as a via to connect the metal wires at two layers, as illustrated in Fig. 2. Similar to row-based standard cell layout in a conventional layout, the proposed cell layout (Fig. 6) is also designed with a fixed height so that a number of cells can be abutted side-by-side to form multiple rows stacked vertically to complete a row-based cell layout. The power and ground rails run parallel to the upper and lower boundaries of the cell. The NMOS transistors are placed closer to the ground rail while the PMOS transistors are placed closer to the power rail. Like source-drain sharing in a conventional layout, the gate regions of multiple NMOS (or PMOS) devices can be merged to save space (Fig. 3) if their gates are connected together (as T5 and T6 in Fig. 5).

Next, we shall discuss the routing algorithm for the standard cell layout. Since the wires can be routed on T or B layer, we should determine first which layer to route a wire. To reduce the more difficult intra-cell interconnects (which are often across different levels), we suppose that all the input and output pins are located on the same T-layer (Fig. 7(b)). For the other wires, we group them into three types according to their locations: T-type (a terminal located at the top active area of PMOS/NMOS), B-type (a terminal located at the bottom active area of PMOS/NMOS) and G-type (a terminal located at the gate), as illustrated in Fig. 7(c). If a device's drain terminal is T-type, its source terminal will be B-type, and vice versa. The wires will be routed based on their terminal types, following below rules. 1) if all the terminals of the wire are T-type/B-type, the wire will be routed on T-layer/B-layer; 2) if all the terminals are G-type, the wire can be randomly routed on T-layer or B-layer; 3) if the terminals are T-type/B-type and G-type, the wire can be routed on T-layer/B-layer; 4) if the terminals are T-type and B-type, the wire needs to be divided into two parts and both of them will be routed on T-layer and B-layer separately (as the 5th wire in Fig. 7(d)), while a redundant device acting as a via should be assigned to connect them; 5) if the terminals are T-type, B-type, and G-type, we can use a G-type terminal to divide the wire into two parts, both of which are routed on T-layer and B-layer separately, as the 1st wire in Fig. 7(d).

In general, the wires routed on T-layer contains all T-type terminals and some G-type terminals, while the wires routed on B-layer contains all the B-type terminals and the rest G-type terminals. The wires in two layers can

be routed independently. For each layer, a negotiated congestion algorithm (e.g., famous "Path-finder") is utilized to rout all the wires. After routing process is completed, the 2-D patterns of each layer will be decomposed and synthesized using the (alternating-material) self-aligned multiple patterning and stitching processes. As an example, we redesign some standard cells in NangateOpenCellLibrary using 3D vertical GAA nanowire MOSFETs, and the test results are shown in Table 1 to verify the functionality of our method.

9781-3, Session 1

## Directed self-assembly aware restricted design rule and its impact on design ability

Yulu Chen, Ryoung-Han Kim, GLOBALFOUNDRIES Inc. (United States)

Directed self-assembly (DSA), the epitaxial alignment of block copolymers to minimize the system free energy, is prone to defects that are random and difficult to eliminate, as highlighted in prior work. In creating fins for FinFET device, the defect density is known to be a strong function of guide template CD. We propose the use of restricted design rules (RDR) that limits the guide template CD to achieve low defectivity and also report its impact design-ability of logic, I/O, and SRAM, and overall chip area. The restricted design rule in defining guide template CD is extracted from empirical data. Design rule check (DRC) is applied to GLOBALFOUNDRIES' 20nm technology chip design to estimate the penalty of DSA specific RDR.

9781-4, Session 1

## Integrated routing and fill for self-aligned double patterning (SADP) using gride-base design

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Self-aligned double patterning (SADP) or self-aligned quadruple patterning (SAQP) have been proposed as an alternative patterning solution for sub-10nm technology.

Many studies on SADP have focused on the size and orientation of mandrels for a given main design.

In current practice of SADP, once main design is complete, line and space style of dummy fills are inserted. A large buffer space is required around the main design because no further verification of main design (in presence of fills) is performed. This causes irregular pattern density, which becomes a source of process variations.

We propose integrated routing and fill, in which main design (routing, to be specific) and fill insertion are performed together. grid-based dummy arrays are first assumed; as a main design is introduced, array patterns are cut where needed to identify main routing as well as fills. This approach can be compared to post fill as follows.

- Buffer space can be kept smaller, e.g. in typical metal pitch. This is because main design and fill insertion are done together, and the impact of fills on design can readily be verified through PEX or even lithography simulations. Buffer space in post fill however should be kept larger, e.g. 2 or 3 times of metal pitch. Even some fills that are missing in post fill can now be introduced due to smaller buffer space.

- Both designs and fills are on the grid, so less regions are unoccupied, which also helps pattern regularity.

Since fills are inserted while regular metal pitch is maintained, mandrel can be determined without any conflicting point; unnecessary spacers are removed by cutting process; the remaining spacers are etched to the substrate, which leaves the final metal wires. A key in SADP is to make various mandrel width as uniform as possible, and our grid-based design helps in this regard.

The proposed design flow is compared to post fill design flow. The line and space array of dummy fills is first generated; main design is then introduced and overlapped with the dummy; dummy patterns within a certain distance from the main design are removed (called array cut); merged layout of the dummy and main design is then submitted to the subsequent process, such as verifications (e.g. schematic check, DRC, PEX, and density check); if there is an error, we revise the array cut and main design until no error is discovered. The verification in conventional fill flow does not involve fills, which is important difference.

Both design flows are implemented and compared in terms of uniformity of pattern density, capacitance increment due to fills as well as other impacts on main design, etc.

9781-5, Session 1

## Integrated layout based Monte Carlo simulation for dense design scaling

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Design rules (DR) are created to communicate to designers process limitations in form of geometric constraints. Certain design rules are calculated based on wafer fail mechanism (FM) with process assumptions (PA), including process dimensions and variability. In the past, design rules are always set to guard-band worst case design/process scenario to maintain design efficiency. However in advanced technology nodes the dimensional variability has became more and more layout dependent. As processes are being pushed to their physical limits, scaling has become increasingly difficult to maintain, making it a priority to remove all design-rule-slack without introducing yield risk.

Dense design also often involves "Design ARC", a collection of design rules, the sum of which equals critical pitch defined by technology. In a design ARC, moving a single edge can lead to chain reaction of other rule violations. In current DR guided design flow, when a design rule violation occurs, we either fix design or re-examine rule value for that particular layout. However with design ARC this flow is often iterative and futile. Also since design rules only pass or fail, it is difficult to make quantitative tradeoffs between competing rules.

Layout based Monte Carlo simulation (LBMCS) is a new DR calculation tool we developed that does Monte-Carlo (MC) simulation directly on top of layout. It generates complex checks according to wafer FM using pseudo-contours. In this paper we propose a multi-rule optimization approach enabled by LBMCS. We start with a layout that followed design rule as much as possible. Then we identify the failed design rules in this seed layout, as well as those passing rules that are linked to the failed one(s) within design ARC. For all these rules we revisit the fail mechanisms behind them and enable their fail rate calculations in the integrated LBMCS. The interactions of these rules, or fail modes, are linked together through the layout, enabling us to go beyond single rule optimization. Based on the fails in the seed layout, we make layout adjustment to generate DOEs. The results of LBMCS runs are detailed fail rates for each fail mechanisms enabled in the run, so in the end an informed decision can be made.

In this paper we use the example of SRAM word line contact optimization to explain this methodology. Our results show how we pick a candidate with evenly distributed FM failure measures to pass all checks, even though it's not design rule clean.

In summary, in order to achieve best possible scaling, we cannot follow the single rule approach but have to spread out the design rule slack among all the rules forming a design ARC. We demonstrated a methodology based on LBMCS for the example of word line contact. We believe this methodology can be generalized to optimize any critical pitch limited design scaling or special constructs. This methodology may not be possible to squeeze

everything in any tight pitch, but for a given technology node and given PA we can optimize the layout to achieve the best possible scaling for a specific design layout.

9781-6, Session 1

## Impact of EUV patterning scenarios on different design styles and their design rules for 7nm-node BEOL layers

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In the paper we focus on various EUV patterning scenarios for the critical BEOL layers, including metal and via, that are designed according to 1D and 2D metal 1 design styles. Standard test layouts with baseline design rules (mainly metal pitch and tip-to-tip distance) are prepared for the design styles. Imaging performance of the test layouts created for the different patterning scenarios is verified through simulations with predicted resist process capability and scanner error budgets, and then compared by looking into certain key metrics including depth of focus (DOF), CDU, mask error enhancement factor (MEEF), edge placement error (EPE), and line edge roughness (LER), and so on. The test layouts are then shrunk by tightening the design rules. Imaging performance of the tighten layouts are evaluated to clarify shrink capability of the design rules. We demonstrate image fidelity, CDU, and EPE variability with the proposed patterning scenarios for 30nm and 32nm 2D designs as well as 28nm and 30nm pitch 1D designs, respectively. The EUV capability for the 1D/2D designs with the associated patterning scenarios is summarized. The EUV single exposure for the cut pattern offers the best design rule shrink capability for the 1D design.

The 'EUV for cut pattern' scenario is likely the most attractive solution for the 1D metal designs. EUV imaging performance is sensitive to size and relative location of the cut features, i.e., the line ends. The cut feature size is determined by the metal pitch and the number of adjacent metal line ends while the cut feature location is related to the design intent. As a result, the cut pattern style could be very different among the layouts from different designers. Pros and cons of selected cut pattern styles are estimated through comparison of imaging performance, design rule, and cell size. Additionally, dark-field imaging and bright-field imaging for the patterns are compared in terms of imaging performance and dose requirement (throughput).

For the most critical via layer, via size is generally enlarged to increase image contrast. However, corner-to-corner distance of a via pair in the retargeted layout may become small for the EUV imaging. We introduce a custom OPC treatment that uses removed close corners as a guide pattern to prevent the corners from being bridged over. Nowadays, a self-aligned process is widely adopted for the via layers in the industry. Because certain via edges are bounded by metal edges, location of those via edges can be adjusted properly for improving image contrast. It indicates that optimization of the via target is required. We demonstrate image result of the optimized via target and then compare with that of the original square via design. Scalability of the designs with the different via shapes is clarified. Finally, we attempt to come up with suggested design style and design rules associated with the best pattern scenario for the 7nm-node metal and via layers.

9781-7, Session 2

## Methodology for analyzing and quantifying design style changes and complexity using topological patterns *(Invited Paper)*

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In order to maximize yield, design companies spend a lot of effort up front to analyze what types of design styles are needed and used in their layouts (standard cells, macros, routing layers, and so forth). One important goal is to reduce the types and complexity of design patterns in use, while establishing and understanding what sets of patterns are necessary for designers. Further, over time design styles can and do change and therefore it also important to be able to identify when new patterns have being introduced and what they are. As the semiconductor industry continues to move towards smaller and smaller feature sizes, having an understanding of what patterns are actually needed and used becomes increasingly important for both designers and their foundry partners. This type of analysis requires two basic capabilities. First is a methodology for analyzing the "known pattern" space: namely to measure the types and quantities of patterns that are being used in a design, including with a metric for pattern complexity. Second is the ability to measure and track what has changed between designs to identify the "unknown pattern" space.

This paper introduces a novel methodology for full chip high performance topological pattern analysis (figure 1) and the applications of this methodology towards analyzing design styles in order to quantify and measure design changes and the degree of layout regularization. This methodology has a pattern capture phase where a full analysis of the "known pattern" space is performed to build a database of all known patterns along with corresponding metadata (such as dimensions and pattern relationships). In the pattern compare phase, a new design can be compared to this pattern database to identify the "unknown pattern" space.

Previous approaches have required knowing up-front what patterns to focus on, whether hotspots or specific interesting constructs (such as line end enclosures) [1][2][3]. This new approach allows engineers to perform a full profiling across all patterns that exist in design and without needing to explicitly specify what patterns to analyze.

This paper will use this topological pattern analysis methodology to analyze and compare differences in design styles across successive design nodes. Trends regarding pattern regularization and complexity will be measured and described. Further, within a specific process node, this paper will describe how differences in successive revisions of the same design can be measured.

Early in the design cycle, the design of high yielding standard cells is critical for design companies. This is often done before the process and related litho models and rules have fully matured. An understanding of what patterns are common and which patterns are unique helps provide process-agnostic guidance to designers looking for ways to improve their design robustness. This paper will also relate how this pattern analysis methodology can be applied to the process of correlating pattern usage and cell usage to help designers understand what patterns are important and to suggest where and how patterns can be improved to increase layout regularization.

9781-8, Session 2

## Methodology to extract, data mine and score geometric constructs from physical design layouts for analysis and applications in semiconductor manufacturing

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At advanced technology nodes (sub-22 nm), design rules become very complicated as interactions between multiple layers become more complex,

while the number of design elements within the optical radius increases. As a result, one may possibly encounter novel yield limiters in the 2D/3D design space with every new product taping out to the fab. Key to fast yield ramp is identifying novel constructs that may become yield detractors, and to address the challenge in the DFM space before actual Silicon is run. A comprehensive methodology to find such geometric constructs is proposed. This work uses a method to deconstruct physical design layouts into unit geometric design constructs with optimal context [1, 3]. These geometric basis elements are a comprehensive cover of the known physical design space. Further, a scoring model is proposed to prioritize the captured design features depending upon the end application requirements. The proposed method is computationally fast to be able to classify and deconstruct the chip level design layout with or without prior anchoring [2] (comparable to that of the industry standard DRC runtimes). For prior filtering, "new" design constructs found with respect to the yielding baseline design can be used (figure 1). A "new" design construct is defined as either one that is topologically distinct or one which has dimensions outside of the range of what has been seen before. The scoring model is a weighted function of annotated properties of classified geometric design constructs (figure 2). These properties (feature vector) span design metrics like usability, complexity, and variability associated with extracted design constructs in a given layout. More metrics based on process window and sensitivity analysis can be included in the proposed scoring method.

The output of such a flow is a pattern library that can be easily plugged into pattern matching flows to feed into the end application. Flow for one such application is shown in figure 1 along with a schematic for scoring model shown in figure 2.

9781-9, Session 2

## By using pattern enumeration methodology to accelerate process development and yield ramp up

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This paper will present a novel method of how to generate test key patterns which contain most possible design styles that a designer can draw based on particular design rules. The enumerated test key patterns also contain critical design structures which are allowed by a particular design rule. The pattern enumeration method can migrate process weak patterns from older technology nodes to the new technology node in order to help foundries check process detractor patterns at the development stage.

A layout profiling method is used to do design chip analysis in order to find potential weak points for new incoming products before fab processing and take preemptive action to avoid yield loss. Yield loss can be prevented by comparing different products and leveraging the knowledge learned from already manufactured chips to find possible yield detractors.

9781-10, Session 2

## Optimization of self-aligned double patterning (SADP)-compliant layout designs using pattern matching for 10nm technology nodes and beyond

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Pattern-based methodologies for optimizing Self-Aligned Double Patterning (SADP)-compliant layout designs are developed based on identifying lithography hotspots and replacing them with pre-characterized, manufacturing-friendly fixing solutions. Multi-patterning has become the key enabler for technology scaling, and SADP is one of the competitive solutions for 10nm technology nodes and beyond. Its pitch-splitting sidewall imaging method offers advantages compared to quadruple litho-etch decomposition in terms of mask costs and variability control, such as overlay requirements. Despite its many benefits, SADP also introduces new design and manufacturing challenges. On the design side, the SADP-compliant layout designs are difficult to visualize as the drawn layout designs no longer completely represent the mask layers used for manufacturing. i.e., the mandrel (non-mandrel) and the block masks. Thus, automated layout optimizations that have been traditionally applied to the drawn layers need to be adapted so that they are applicable to the mask layers. On the manufacturing side, the printing of contact-like block masks that are used to form the line ends of dense pitch metal lines pose a significant lithographic challenge. These lithography hotspots increase the likelihood of line end bridging on the routed metal layers, in which the uni-directionality and high-regularity make them suitable for the SADP manufacturing process.

An automated pattern-based matching and replacement methodology optimizes line ends to improve block mask manufacturability. By identifying the line end topologies in SADP decomposed layout designs and opportunistically replacing them with consistent predetermined fixes on the block mask, the number of lithography hotspots is reduced, and the design manufacturability is improved. This proposed methodology requires a topology-based library of lithography hotspots to be built a priori, in which each topology is associated with a predetermined fixing solution. A pattern matching engine then searches for matching topologies from the library in the SADP decomposed layout designs. If a match were found, the engine would replace the existing hotspot with the predetermined fixing solution. These fixings are opportunistic because only the design rule check-clean replacements are preserved.

The methodology was demonstrated on a 10nm SADP decomposed routed block with an area of 200 x 200 um2 on the metal 2 layer. Optical rule checks (ORC) detected ~2500 line end bridging hotspots. A pattern classification engine was used to classify the hotspots to unique classes. Using exact pattern classification and a 96 nm classification radius, 2500 hotspots reduced to 880 unique classes. Then, a small library containing four line end topologies was built (see Fig. 2). For each topology, a corresponding manufacturing-friendly fix on the block mask was predetermined and stored in the library. Using a topology-based pattern matching and replacement engine, the predetermined fixes were opportunistically applied to the SADP decomposed layout design. The four topological-based fixes resolved all the lithography hotspots.

9781-11, Session 3

## ILT application beyond 10nm

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The purpose of OPC is to assist lithography for achieving the correct photo mask shape and printing the pattern with correct on-wafer contour [1]. However facing the challenges of lithography resolution limited by 193nm immersion exposure tools and the design rule shrunk down to 7nm and beyond, the traditional OPC approach often delivered a solution close-to-target,[2] while not close-to-contour, as shown in Fig. 1. The targeted width and length could be well-achieved in OPC. However, for 2D features like corner or tip, ILT provided better close-to-contour performance [3]. Contrast to traditional OPC that approximates photo mask shape by inputting various mask shapes/sizes to find a solution closest to desired pattern contour, ILT calculates the correct photo mask shape from the desired contour (Fig. 2) to provide more accurate lithography printing and consequently more robust process. Fundamentally, reversely solving the lithography printing equations from desired contour is the core concept of ILT (Inverse Lithography Technology) [4]. For 7nm and beyond, 193nm immersion single patterning needs to be push further to support upcoming multiple patterning needs. Tip-to-tip design on single patterning below 25nm and line-end pull-back control needs to be 20% better than previous node are essential design rule to be supported.

Experimental Results

The direct ILT on a full chip process is a very costly process in terms of numbers of CPU needed and CPU run time needed.[5] To reduce CPU numbers/run time, we have integrated ILT HSF (hot spot fix) method into our OPC flow, as shown in Fig. 3. The ILT HSF is to conduct ILT process only on the weak patterns that could cause yield failure. Current design for 10nm and 7nm nodes are processed with both ILT and OPC, and then the mask house has been using customized data preparation process to reduce mask writing time and state-of-art e-beam writer to generate much finer jog patterns on masks. In this work, the lithography printing and post-etch patterns have been verified, using in-line CDSEM for top-down inspection, yield maps, and electrical tests for the characterization of ILT and OPC performance. The lithography is targeting bi-direction 80nm resolution with post-CMP tip-to-tip spacing down to 25nm.

9781-12, Session 3

## Hybrid hotspot detection using regression model and SOCS kernels

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As minimum feature sizes shrink, resolution enhancement techniques (RETs) such as high coherent illumination and complex sub-resolution assist features (SRAFs) are required to print features using 193nm immersion lithography. However, the side effect of these techniques is that optical contrast of some patterns decreases. Lower contrast patterns are likely to result in hotspots after etching process due to process variations. Unexpected hotspots still appear on wafers. Therefore, it is important to detect and fix these hotspots at the design stage to reduce the development time and manufacturing cost. Currently, as the most accurate approach, lithography simulations are widely used to detect the precise locations of hotspots. However, it is known to be time-consuming. Although several fast hotspot detection methods such as machine learning and pattern matching have been proposed, those proposed methods have a fundamental problem that their prediction accuracy highly depends on the training data and classification algorithm. In addition, optical simulations are often still needed to identify the exact locations of hotspots, resulting in an increase in calculation time.

In this paper, we propose a hybrid hotspot detection framework based on a regression model and sum of coherent source (SOCS) kernels to accurately identify those exact hotspots. It is able to produce results as accurate as full lithography simulations with much less computational cost. The key point of speed-up is how to reduce optical computation times. As shown in Fig.1, firstly we predict optical aerial images for all area with regression model which is very fast. When a hotspot is detected from the results, there is a possibility of misjudgment because the prediction accuracy of optical aerial image calculated with regression model is not high. To solve this problem, we calculate optical aerial image using SOCS for the limited areas where patterns having misjudgment possibilities exist. Since the locations of hotspots are identified based on optical intensity, we can detect hotspots without misjudgment. Furthermore, computational time is reduced by calculating optical aerial images with the minimum number of SOCS kernels. Therefore, our proposed method is able to produce results as accurate as full lithography simulations with much less computational cost. In our presentation, we will discuss the details and effectiveness of the proposed flow with comprehensive experimental results.

9781-13, Session 4

## Variability-aware compact modeling and statistical circuit validation on SRAM test array

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It is widely recognized that, in nano-scale CMOS technology, variation in manufacturing process has emerged as a fundamental challenge to IC design. While foundries are working hard to mitigate process variability, the design houses are asking for accurate and appropriate models to handle statistical circuit performance evaluation. Variability-aware compact transistor models can enable statistically optimized designs by capturing device variations in a concise, yet physically accurate way, and they are relatively easy to integrate with existing CAD tool flow. In addition, these compact transistor models require customized test structure designs as well as proper statistical characterization procedures. In this work, we have extracted variability-aware compact transistor models based on electrical measurements from carefully designed SRAM array test structures. We have also built a custom Monte Carlo simulation platform to utilize these compact transistor models in the IC design flow. Our collaborating team has designed bit-transistor accessible SRAM array test structures, as shown in Figure 1, using foundry's 28nm FDSOI technology. This design enables high-volume transistor I-V measurements as well as cell DC characteristics measurements. We have collected I-V measurement data [1] of the pass-gate transistor within each SRAM cell across 5 rows and 512 columns of the test structure array. These I-V curves are then used for compact variability model characterization. Meanwhile, we have also measured the DC write-noise margin characteristics of those SRAM cells. These unit circuit performance data will later be compared with our custom MC simulation results to demonstrate the validity and efficacy of these variability-aware compact transistor models. Of particular interest is to show predictive ability at the far "tails" of the performance distribution. As discussed in [2], properly selecting model parameters for statistical characterization is essential for compact variability modeling. We have proposed and implemented a stepwise parameter selection procedure to obtain an optimal model parameter set for both model extraction and custom MC simulation. Based on the test structure design, we have chosen the industry standard PSP 103.1 model with nominal parameter values from a foundry's default model. As depicted in Figure 2, the final four-parameter-set has clear physical property representations in the model equation, reasonable I-V curve model fitting error and far simpler statistical correlation structure. The various components of variability observed in these model parameters are extracted and added to the model cards for statistical circuit simulation. Figure 3 shows the comparison of direct measurements (top) vs. custom MC simulations using extracted model parameters (bottom). The middle row of "standard" MC simulations based on the default design kit, is added for complete comparison and clear visualization. Our results to this stage demonstrate that the far simpler statistical structure, represented by only the four physical parameters that were selected, matches the full MC results. In the immediate future we will focus on exploiting the simple statistical structure of the extracted parameters shown in Figure 2, in order to capture the non-linear correlations and the non-Gaussian distributions through appropriate parametric transformations. The goal is to demonstrate that important non-normality in the measured data can be predicted by our simplified model. Such non-normality is often evident at the tails of the performance distributions, and capturing that is necessary for the statistical modeling of inherently high-yielding IC designs. We will also attempt to leverage via machine learning techniques the apparent clustering made visible in the simplified scatterplot matrix in order to identify faulty measurements or faulty devices in large sets of test patterns.

9781-14, Session 4

## Impacts of process variability of alternating-material self-aligned multiple patterning on SRAM circuit performance

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Process variability induced circuit performance degradation is a major concern as FinFET devices are scaled down to sub-10 nm. In another paper, we propose a novel approach to significantly reduce the edge-placement-error (EPE) effect in complementary lithography (and consequently improve the cut-process patterning yield) by combining selective etching and alternating-material self-aligned multiple patterning (altSAMP) processes.

The line arrays fabricated by an altSAMP process will be made of two different materials (e.g., A and B). As shown in Fig. 1, an alternating-material self-aligned quadruple (altSAQP) patterning or a self-aligned sextuple (SASP) patterning process can produce the A-B or A-B-B type of line array, respectively. As illustrated in Fig. 2, we can decompose the holes over the lines made of material A into one mask and the holes over the lines made of material B into the other mask. The targeted line density for each decomposed mask is half of the original array and a following highly selective etching process to cut the targeted lines (ideally) will not attack the neighboring non-targeted lines, therefore more severe EPE can be tolerated.

Compared with the conventional SAQP process wherein no multi-modality of the final (single-material) spacers is present, the altSAQP line features show a bi-modality characteristic. Similar statistical signature can be observed in a SASP process. This raises a critical question about the random fluctuation of SRAM circuit performance if an altSAQP or SASP process becomes an inevitable solution to tackle the EPE issue in the future. In this paper, statistical TCAD simulations are carried out to examine SRAM circuit performance in the presence of altSAQP/SASP process variability. If fabricated by an altSAQP/SASP process, the line CDU and LWR will contain the bi-modality variations (see Tables 1 & 2) due to the varying statistical characteristics of lines A and B. We assume that gates and fins are fabricated by the same type of process as mixing two different processing techniques will drive up the manufacturing costs. As shown in Fig. 3, if an altSAQP (or SASP) process is adopted in SRAM fin/gate fabrication, it can result in two (or five) types of SRAM cells based on their material choices. A 6-transistor SRAM circuit shown in Fig. 4 is studied in our simulations and the static noise margin (SNM) is used to analyze the SRAM circuit performance.

SNM characteristics of the mentioned seven types of SRAM circuits are obtained from TCAD simulations for the 10-nm half pitch (HP=10 nm) and shown in Figs. 5-7. The ratio of SNM standard deviation to mean value ($\delta/\mu$) ($\mu$: mean value of SNM, ?: standard deviation of SNM) is adopted to measure the SNM stability. From Fig. 6, we can see SRAM curcuits fabricated by an altSAQP process is more stable than by a SASP process when the half pitch reaches 10 nm. Moreover, if a SRAM cell fabricated by a SASP process is symmetric regarding its fin/gate types, its SNM stability will be the optimal (see Fig. 6 (f)). Fig. 7 shows the simulation results of (?-6?)/Vdd (Vdd: supply voltage), which is a commonly used index to estimate the SRAM yield. It indicates that altSAQP or SASP process fabricated 6-T SRAM circuit design meets the six-sigma yield requirement when the half pitch is scaled down to 10 nm. Despite the altSAQP/SASP process variability and the related SNM degradation (compared with SRAM circuits fabricated by the single-material SAMP process), the induced fluctuation of SRAM circuits is still controllable. We shall further discuss 7-nm and 5-nm circuit performance and optimization in our paper.

9781-15, Session 4

## Modeling interconnect corners under double patterning misalignment

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Interconnect parasitics are important as they account for increasing portion of circuit delay. Manufacturing variations on interconnect are modeled by interconnect corners, which are combinations of extreme resistance (R) and capacitance (C) values. For example, Cmax is a corner in which metal wire is patterned wider and thicker so C becomes larger and R becomes smaller. In double patterning technology (DPT), in particular with litho-etch-litho-etch process, mask misalignment in the same metal layer is another manufacturing variation that should be considered in interconnect corner modeling.

Assuming that three parameters, such as metal width, thickness, and ILD height, are random variables following respective Gaussian distribution, probability density function (PDF) of total capacitance, which includes both coupling (Cc) and ground component (Cg), can be obtained. Conventional Cmax and Cmin corners without misalignment correspond to 3-sigma of this PDF and are denoted by CM and Cm, respectively. To account for misalignment, we obtain new values of total capacitance CM' and Cm' while the extent of misalignment is set to its own 3-sigma value.

If all four random variables are considered together, a new PDF of total capacitance is obtained. Interconnect corners from this PDF, marked as CM'' and Cm'', are located much tighter. Since Cg is invariant under misalignment, we determine the coefficients of Cc in these interconnect corners:

CM'' = Cg + k1Cc, (1)

Cm'' = Cg + k2Cc. (2)

Let us assume that three wires are located and center wire may be misaligned; this is the configuration where actual interconnect corners are modeled. If center wire is misaligned to the right, its coupling capacitance to the left wire decreases while that to the right wire increases; the total capacitance therefore almost does not change. We therefore want to obtain the coefficients of ground capacitance such that total capacitance remains invariant, i.e.

Cmax = k3Cg + k1Cc, (3)

Cmin = k4Cg + k2Cc, (4)

where Cmax and Cmin are corners without misalignment.

The proposed method is implemented using the industrial 14-nm technology in Matlab. We demonstrate the method for various circuits in terms of capacitance, signal and crosstalk delays, compared to the worst case analysis and the Monte Carlo simulation.

9781-16, Session 4

## Model-based CMP aware RC extraction of interconnects in 16nm designs

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Traditional RC extraction flows mostly consider interconnect thickness variations caused by etch and CMP processes in a way of rule-based approach where a form of tables or polynomials is used. While such rule-based approaches are easily incorporated into design flows, they are not inevitably accurate since table-look-ups in rules are inherently taking simple (mostly one dimensional) typed patterns. Moreover, rules fail to account for the length scale and cumulative effects in both etch and CMP, thereby making them less accurate compared to physics-based models. In this paper, we introduce a model-based CMP aware RC extraction flow that uses the results of thickness simulations from CMP modeling tools. We apply the proposed model-based CMP aware RC extraction flow to several blocks in a 16 nm design, and compare the results of the proposed model-based flow with those of a traditional rule-based RC extraction flow. This paper also notes that running the model-based flow in conjunction with the traditional rule-based flow should cover the full range of RC variation along critical nets, and ensure faster timing closure.

9781-31, Session PSWed

## Design space exploration for early identification of yield limiting patterns

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In order to resolve the causality dilemma of which comes first, accurate design rules or real designs, this paper presents a flow for fast exploration of the layout design space to early identify problematic patterns that will negatively affect the yield at the process development early stage.

A new random layout generating method is reported in this paper, which generates realistic design-like layouts without any design rule violation. Model-based Lithography simulation is then used on the generated layout to discover the potentially problematic patterns (hotspots). These hotspot patterns are further explored by randomly inducing feature and context variations to these identified hotspots. Simulation is then performed on these expanded set of layout clips to further identify more problematic patterns. These patterns are then classified into design forbidden patterns that should be included in the Pattern Library checker for design illegal patterns detection that need better optimized design layout and handed in the RET recipes and processes.

Summary:

For simultaneous development of designs and process, designers need design rules early in the design cycle to early define what the allowed (and forbidden) design constructs are. On the other hand, complex patterning issues cannot be easily extrapolated from known process physical limitation, and the traditional test sites are not sufficient to cover the complex 2D patterning variations that can potentially exist in real designs.

In order to resolve this causality dilemma of which comes first, accurate design rules or real designs, this paper presents a flow for exploration of the layout design space to early identify problematic patterns that will negatively affect the yield. The design space exploration flow is composed of three stages.

1. Layout Schema Generator (LSG)

A new random layout generating method is reported in this paper which generates realistic design-like layouts without any design rule violation. The randomness of the generation is implemented by applying Monte Carlo method while inserting unit patterns in a grid. Design rules are applied as constraints during the generation of the layout.In this paper, we will demonstrate how this method can effectively generate random layouts for single mask and multiple patterning technologies. The layout generator can generate 50,000 layout clips in less than an hour. The randomly generated layout can be classified into 220,000 unique patterns.

2. Simulation

Lithography simulation is then used on the generated layout to discover the potentially problematic patterns across process window (hotspots).

3. Hotspot Variation (HSV)

The hotspot patterns identified from the previous step in addition to other patterns that are already known to be yield limiters are further explored. The patterns are varied by randomly inducing feature and context variations to these identified patterns. Simulation is then performed on these expanded set of layout clips to further identify more problematic patterns. These patterns are then classified into design forbidden patterns that should be included in the design rule checker and legal patterns that need better handling in the RET recipes and processes.

We demonstrated how using the DSE can early identify good and bad patterns to print by applying the design space exploration (DSE) flow on an advanced node

9781-32, Session PSWed

## Design technology co-optimization for 14/10nm metal1 double patterning layer

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Design and technology co-optimization (DTCO) is a new technology method, which takes the manufacturing process limitations, mainly lithography into account during the early design stage. DTCO has become the most efficient scaling strategy when developing the products below 14/10nm because the traditional pure lithography technology is no longer up to the challenges. Based on the both design limitations and process concerns, DTCO can combine the various design rules with the related corresponding lithography techniques. What's more, an inappropriate decision at the beginning may lead to costly adjustment in the later period of the whole manufacture procedure. Therefore, it is evident that the DTCO can play an efficient role for the final success of products. Generally, DTCO covers a broad scope of research directions, which may involve the power consumption, multiple exposure patterning, hotspots characterization and grouping, design rule refinement and so on. This paper demonstrates a newly developed optimization algorithm under the term of DTCO to make double patterning technology (DPT) more compliant when used as the photolithographic solution.

The double patterning technology (DPT) becomes necessary to extend the ArF water-based immersion lithography to keep up with Moore's Law before the EUV technology. However, the existence of the imperfect DPT solutions, such as the stitch boundaries and conflict defects has a bad effect on the yield even though several rounds of the fine tune of the optical proximity correction (OPC) are coming into use. Hence the DPT-compliant DTCO can be achieved to re-optimize the DPT- related design rule and improve the robustness of design rule using the guidance from the analysis and evaluations of the DPT-conflicts resolving.

In this paper, the methodology of DPT-compliant DTCO is applied to a 1.3x routed-metal layer from the 14nm node. To start a design-like layout including plenty variations is generated with the guidance of a set of design rule. Next, the layout pattern is decomposed into two masks, simultaneously the color conflicts will be found and analyzed. The hotspots will be classified by the degree of the similarity of the geometries. So the DPT related hotspots library will be formed. The different DPT hotspot library units can be defined and used in the following research of the effective retargeting and the design rule re-optimizing. After the analysis, the solutions of eliminating the hotspots can be created for the limited number of the hotspot library units. Then the DPT-aware design rules can be re-optimized systematically by adding the analysis from the DPT hotspot library. Finally, we can generate the random large-scale layout with the new optimized DPT-aware design rule which can print more robustly.

The approach described here has one strong advantage of optimizing the design rule which can accord with the practical manufacture requirements and become more manufacture friendly from being fixed early. The demo results show that the algorithm proposed in this paper is an efficient solution for refining the 14/10 nm tech node Metal1 layer design rule, which can update the design rule and avoid later design rework.

9781-33, Session PSWed

## An integrated design-to-manufacturing flow for SADP

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Self-Aligned Multi-Patterning (SAMP) is a potential technology for metal layers in N10 and beyond nodes. One of the main advantages of SAMP over (LELE) multi-patterning is better Mask overlay control. In addition, SAMP results in better process tolerance and lower Line-Width Roughness. One of the main approaches of SAMP fabrication is SID (Spacer is dielectric). In this approach, we have a mandrel mask which has patterns with double or quadruple the required pitch. Side walls are grown on both sides of the mandrel lines to define the width of spacers between metal lines. Line-end cuts approach can be used to define the final printed pattern. In this paper, we propose a full manufacturing flow for SAMP including layout decomposition, retargeting, source optimization, OPC, and verification. We highlight important design and technology aspects that must be considered for creating a manufacturable SAMP flow.

9781-34, Session PSWed

## Using pattern analysis methods to do fast detection of manufacturing pattern failures

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For debugging silicon failures, DFT diagnostics can identify which nets or cells caused the yield loss. Normally, it needs a long time and many resources to identify which failures are due to one common layout pattern or structure. This paper will present a new yield diagnostic flow that shows, based on preliminary EFA results, how pattern analysis can more efficiently detect systematic defects within the manufacturing environment. This pattern analysis and tracking helps to increase visibility on product design failures and allows for yield loss estimations.

9781-35, Session PSWed

## Electron-beam lithography with character projection exposure for throughput enhancement with line-edge quality optimization

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VLSI Design and Education Center (VDEC), the University of Tokyo, is running an open-use nanotechnology research facility for universities, research institutes, and companies in Japan with support from Ministry of Education, Culture, Sport, Science & Technology in Japan. We have class 1, 100, and 1000 clean rooms with leading-edge fabrication and measurement instruments. Among them, electron-beam lithography (EBL) tools are attracting many users for both mask fabrication and direct wafer/chip writing. Currently, we have two EBL instruments, ADVANTEST F5112+VD01 and ADVANTEST F7000S-VD02 systems, which are capable of both variable-shaped beam (VSB) and character projection (CP) exposure schemes.

VSB is a high-speed lithographic technique based on variable-size rectangular beam, while CP realizes high-speed exposure by shooting arbitrary figures with one EB shot, if the target figures are prepared as a character on a stencil. These methods are considered to be suitable for small-featured VLSI fabrication with regularly-arranged layouts like standard-cell logics and memory arrays.

On the other hand, most VDEC clean room users are aiming for non-VLSI applications like photonics, MEMS, MOEMS, and so on. Such devices can still receive the high-speed benefit of VSB over the conventional Gaussian-beam exposure, but not the full utility of CP capability due to the wide variety of layout patterns. In addition, the stepwise edge shapes by VSB strips to approximate oblique or curved edges of the target layout patters often cause intolerably-rough edge conditions, which possibly degrade the resultant device characteristics. Such roughness is also in a tradeoff relation with the exposure speed that depends on the number of the divided VSB figures.

Our goal in this research is to provide an overall EBL methodology from layout design to development utilizing VSB and CP schemes. The key technique in our methodology is layout data conversion of arbitrary patterns into VSB and CP shots, where our own software tool decomposes curved or oblique edges in the layout into CP characters (Fig. 1). The remaining portion is redefined as inner polygons that are composed of perpendicular edges. They are further decomposed into rectangle VSB shots using a commercial tool (Fig. 2). EB shot count of a CP-bordered layout is less than a half of the corresponding VSB-alone layout in our optical-waveguide TEG for negative resist EBL, typically. CP conversion condition like CP character variety, CP placement strategy, inner polygon parameters, and so on, may affect EB exposure speed, edge quality, and resultant device characteristics.

We use Hydrogen Silsesquioxane (HSQ) negative resist and tetramethylammonium hydroxide (TMAH) developer in our experiments because they are known as a high-resolution EBL solution. Top-down and angled SEM images of developed HSQ resist on Si substrate are shown in Figs. 3 and 4, respectively. They show edge and side wall conditions of curved waveguides by VSB and CP exposure. The small (100nm) CP case shows the most smooth edge profile, which implies that the optimum CP condition could be found for each edge quality target. Further details of the tunable design and exposure parameters and the optimization results will be discussed.

9781-36, Session PSWed

## Rapid recipe formulation for plasma etching of new materials

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In nanomanufacturing, the creation and optimization of tool recipes is one of the largest contributors to time and expense during a product development cycle. These costs are especially significant in dry etching processes, where very little is well understood about processing conditions and the produced feature layout. Dry etching is one of the most challenging fabrication steps to optimize due to its large number of process variables and the complexity of the gas chemistry and surface kinetics taking place in the reactor where hundreds of physical and chemical reactions occur in parallel. Many feature and reactor scale plasma etch models and software exist for dry etching. Nevertheless, these models are cumbersome to use in practice due to their inability to adapt to new materials and gas chemistries, to capture local variations in etch rate due to complex pattern densities, their significant parameter input requirements, and their lengthy simulation times.

Current optimization schemes for etching often rely on a trial and error approach. Qualitative relationships based on experience are used to “tune” etch parameters for existing recipes, however this approach does not provide for extrapolation to new processes. Other schemes include design of experiment (DOE) methods like full or fractional design to determine relationships between process inputs, but these approaches do not take into account prior knowledge about the system physics or the past process recipes. Prior research has demonstrated the success of Bayesian experimental design and inference in making more precise parameter estimates with limited data in a variety of fields helping improving model predictions for biochemical pathways, chemical kinetics, and material properties.

In this study, we focus on building a fast and inexpensive process creation and optimization scheme for etching using flexible continuum models and Bayesian statistics. We are particularly interested in developing etch recipes for MgO because of its potential application in STT-RAM devices and the challenges it poses for pattern transfer. We predict bulk etch rates using a steady-state model with volume-averaged plasma parameters and classical Langmuir surface kinetics. Applying single component Metropolis Hastings methods, we model plasma particle and surface kinetics within a global plasma framework using limited data. The accuracy of these predictions is evaluated with synthetic and experimental etch rate data for magnesium oxide in an ICP-RIE system. Finally, we compare this approach with the models generated from JMP, a software frequently employed for recipe creation and optimization.

9781-37, Session PSWed

## Expanding the printable design space for lithography processes utilizing a cut mask

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## Conference 9781: Design-Process-Technology Co-optimization for Manufacturability X

The utilization of a cut-mask in semiconductor patterning processes has been in practice for logic devices since the inception of 32nm-node devices, notably with unidirectional gate level printing. However, the microprocessor applications where cut-mask patterning methods are used are expanding as Self-Aligned Double Patterning (SADP) processes become mainstream for 22/14nm fin diffusion, and sub-14nm metal levels. One common weakness for these types of lithography processes is that the initial pattern requiring the follow-up cut-mask typically uses an extreme off-axis imaging source such as dipole to enhance the resolution and line-width roughness (LWR) for critical dense patterns. This source condition suffers from poor process margin in the semi-dense (forbidden pitch) realm and wrong-way directional design spaces. Common pattern failures in these limited design regions include bridging and extra-printing defects that are difficult to resolve with traditional mask improvement means. This forces the device maker to limit the allowable geometries that a designer may use on a device layer.

This paper will demonstrate methods to expand the usable design space on dipole-like processes such as unidirectional gate and SADP processes by utilizing the follow-up cut mask to improve the process window. Traditional mask enhancement means for improving the process window in this design realm will be compared to this new cut-mask approach. The unique advantages and disadvantages of the cut-mask solution will be discussed in contrast to those customary methods.

9781-38, Session PSWed

### Characterization of shallow trench isolation CMP process and its application

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Chemical mechanical polishing (CMP) has been a critical enabling technology in shallow trench isolation (STI), which is used in current integrated circuit fabrication process to accomplish device isolation. Excessive dishing and erosion in STI CMP processes, however, create device yield concerns. This paper proposes characterization and modeling techniques to address a variety of concerns in STI CMP. In the past, majority of CMP publications have been addressed on interconnect layers in back-end-of-line (BEOL) process. However, the number of CMP steps in front-end-of-line (FEOL) has been increasing in more advanced process techniques like 3D-FinFET and replacement metal gate, as a results incoming topography induced by FEOL CMP steps can no longer be ignored as the topography accumulates and stacks up across multiple CMP steps and eventually propagating to BEOL layers. In this paper, we first discuss how to characterize and model STI CMP process. Once STI CMP model is developed, it can be used for screening design and detect possible manufacturing weak spots. We also work with process engineering team to establish hotspot criteria in terms of oxide dishing and nitride loss.

As process technologies move from planar transistor to 3D transistor like FinFet and multi-gate, it is important to accurately predict topography in FEOL CMP processes. These incoming topographies when stacked up can have huge impact in BEOL copper processes, where copper pooling becomes catastrophic yield loss. A calibration methodology to characterize STI CMP step is developed as shown in Figure 1; moreover, this STI CMP model is validated from silicon data collected from product chips not used in calibration stage. Additionally, wafer experimental setup and metrology plan are instrumental to an accurate model with high predictive power.

After a model is generated, spec limits and threshold to establish hotspots criteria can be defined. Such definition requires working closely with foundry process engineering and integration team and reviewing past failure analysis (FA) to come up a reasonable metrics. Conventionally, a potential STI weak point can be found when nitride residues remains in the active region after nitride strip. Another source of STI hotspots occurs when nitride erosion is too much, and active region can suffer severe damage.

9781-39, Session PSWed

### Advanced DFM application for automated bit-line pattern dummy

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This paper presents an advanced DFM application for automated methodology used for Bit Line Pattern Dummy (BLPD). The application on dynamic random access memory (DRAM) takes advantage of dummy shapes alignment to memory functional bit lines to ensure consistency and reliability across the memory chips. This paper will present how dummy shapes insertion according to space available resulted reduced manufacturability variations across memory bit-lines.

9781-40, Session PSWed

### Wafer hotspot prevention using etch aware OPC Correction

Dave Power, Ayman Hamouda, Mohamed Salama, GLOBALFOUNDRIES Inc. (United States); Ao Chen, GLOBALFOUNDRIES Singapore (Singapore)

As the Semiconductor technology development advances into deep-sub-wavelength nodes, multiple patterning is becoming more essential to achieve the technology shrink requirements. Recently, Optical Proximity Correction (OPC) technology has proposed simultaneous correction of multiple mask-patterns to enable multiple-patterning awareness during OPC correction. This is important to prevent inter-layer hot-spots during the final pattern transfer. In state-of-art literature, multi-layer awareness is achieved using simultaneous resist-contour simulations to predict and correct for hot-spots during mask generation. However, this approach assumes a uniform etch shrink response for all patterns independent of their proximity, which isn't sufficient for the full prevention of inter-exposure hot-spot, for example different color space violations post etch or via coverage/enclosure post etch.

In this paper, we explain the need to include the etch component during multiple patterning OPC. We also explore a new approach for Etch-aware simultaneous Multiple-patterning OPC, where we include the combined resist and etch simulations during the correction. Adding this extra simulation condition during OPC is suitable for full chip processing from a computation intensity point of view. Also, using these models during OPC to predict and correct inter-exposures hot-spots is similar to previously proposed multiple-patterning OPC, yet our proposed approach more accurately corrects post-etch defects too.

9781-41, Session PSWed

### Building block recipe style recipes for productivity improvement in OPC, RET and ILT flows

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Traditional rule-based OPC, model-based OPC and rule-based RET methods have been the workhorse mask synthesis methods in volume production for logic and memory devices for more than 15 years. With continuous technical enhancements, these methods have proven themselves robust, flexible and fast enough to meet many of the technical needs of even the most advanced nodes. ILT methods are well known to have strong benefits in finding flexible mask pattern solutions to improve process window for the most advanced design locations where traditional methods are not sufficient. However, advanced node OPC/RET requirements have also

changed radically in the last 15 years beyond just technical requirements, the volume of engineering work to be done has skyrocketed. The number of device layers which need OPC/RET can be 10X higher than in earlier nodes. Additionally, with multiple patterning common, the number of mask layers per device layer is often 2 or more times higher. Finally, the # of design features to correct per mask layer has increased exponentially with node progression. These factors have led to a large increase across the industry of the number of OPC engineers needed to develop the many new complex OPC/RET recipes for advanced nodes.

In this paper, we describe new developments which significantly improve the productivity of OPC engineers to deploy OPC, AF, and ILT recipes in current and future manufacturing nodes. In addition to technical improvements such as ILT hot-spot fixing necessary to support correction needs, we have re-architected the entire flow based on how engineers now develop OPC/RET recipes for modern device nodes. This work will describe the improvements in OPC/RET development methodology which include: specifically targeted advanced new technical functions; new types of modular structures for much faster reuse of customizations; and new interfaces to flexible programming capabilities to enable easier development and integration of deep customizations for the most challenging technical needs. We show examples of complex mask data correction flows utilizing these concepts and quantify the benefits for overall productivity gains for development engineers of traditional and advanced processes.

9781-42, Session PSWed

## Hybrid pattern based sub-resolution assist feature

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A hybrid multi-step method for Sub-Resolution Assist Feature (SRAF) placement in a random logic layout using ArF immersion Lithography is presented. We are proposing a novel, pattern matching based approach to place SRAFs. The new approach is compared to traditional rules and model based SRAF placement strategies. Optimizing the process window of square or rectangular target features is done by considering optical and resist effects. The process window improvement is measured by comparing process variation bands (PVbands). Due to the complexity of building a complete Rule Based SRAF (RBSRAF) solution and the performance limitation of the Model-Based SRAF solution (MBSRAF), the hybrid pattern based SRAF reduces the complexity and improves performance.

Achieving a full coverage of a rules-based SRAF solution requires an enormous effort and time to optimize the assist features dimension and placement. Rules-based SRAF placement is highly dependent on engineering experience and often fails in random and complex logic layouts. In contrast, model based SRAF insertion tends to have a good SRAF coverage without much code complexity but it needs vast computational capacity, also it may add mask complexity. Additionally, the model based SRAF insertion could introduce non-consistent solutions [1]. A pattern based insertion is simultaneously used with a rule based approach to correct the non-optimized SRAF insertion on a 28nm node technology. This includes introducing missing SRAFs, and optimizes SRAF placement and dimensions. In the proposed algorithm the Optical Rule Checking (ORC) result is used to populate a library of limited process window patterns caused by wrong SRAF insertion. The process window coverage of random layouts is greatly improved vs. traditional rules based approaches, and the runtime is decreased vs. the model based approach. Overall, the stability of the methodology increases and new designs are less likely to show process window problems due to missing SRAF coverage.

9781-43, Session PSWed

## Multiple patterning CD bias offset study by overlay

Chia-Ching Lin, Gary Ch Wang, En Chuan Lio, Howard Chen, United Microelectronics Corp. (Taiwan)

As device design rule has been made pattern size shrink, LELE (Litho-Etch-Litho-Etch) process is used in advance pattern process more and more. The CD control is one of the most critical factors for semiconductor manufacturing. However, the number of current in-line measurement points are not sufficient for the whole wafer CD monitoring. It's the goal to increase inline monitor capacity without suffering process cycle time. To generate an innovation pattern to reach the goal is the purpose for the advance pattern process.

This paper is going to introduce the detection of CD variation by using overlay metrology in LELE process. The target mark was designed from AIM (Advanced Imaging Metrology) overlay mark. By placing Layer 1 and Layer 2 AIM pattern side by side, CD variation will cause related position changed. And it is able to be detected by overlay tool. On the other hand, overlay shift will not influence this model. It has an advantage over the conventional CD measurement tool. First, the overlay tool throughput is 5~10 times faster than traditional CDSEM and the measurement time is saved. Second, we are able to measure CD and overlay at the same time. Both CD/AA performance are considered and the throughput is also gained.

9781-44, Session PSWed

## Incorporating effective etch bias model into multipatterning OPC process-window solver

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Multiple patterning approaches continue to play an increasing role in the lithography of leading edge semiconductor devices. With the use of Litho-Etch-Litho-Etch (LELE) and Litho-Etch-Litho-Etch-Litho-Etch (LELELE) patterning it has become feasible to pattern pitches roughly one half to one third of the pitch resolvable by the most advanced immersion scanners. This pitch-splitting multipatterning approach places special demands on Optical Proximity Correction (OPC). Critical components of modern OPC solvers such as process-window OPC (PWOPC), which works to ensure minimum line width and space are achieved throughout a given range of process variations (mask CD, exposure dose, defocus), must be enhanced in the multipatterning case. To ensure minimum space is achieved among polygons from different exposures (masks), the PWOPC solver must recognize spaces among polygons from different exposures, and treat their correction differently from same exposure spaces. The effects of a non-constant etch bias, particularly an etch bias that has fairly large negative values (e.g. an "etch shrink"), further complicates the PWOPC problem because the non-constant etch bias needs to be included in the calculation of inter-color spaces if the PWOPC solver is to be able to enforce a given post etch minimum inter-color space through the range of given process variations.

In this paper we present a newly enhanced Multi-Patterning PWOPC solver including model-based non-constant etch bias compensation simulation during OPC correction iterations. A triple-patterning layer is used as the test case for this functionality.

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9781-17, Session 5

## Automatic layout feature extraction for lithography hotspot detection based on deep neural network *(Invited Paper)*

Tetsuaki Matsunawa, Shigeki Nojima, Toshiya Kotani, Toshiba Corp. (Japan)

Lithography hotspot detection in the physical verification phase is one of the most important techniques in today's optical lithography based manufacturing process. Although hotspot detection using lithography simulation is widely used, it is also known to be time-consuming. To detect hotspots in a short runtime, several machine learning based methods have been proposed. However, it is difficult to realize highly accurate detection without false-alarm increase because an appropriate layout feature that represents geometrical characteristics of hotspots and non-hotspots accurately is undefined. This paper proposes a new method to automatically extract a proper layout feature from a given layout for further improvement in detection performance of machine learning based method. Our approach consists of two phases, a pre-training and a fine-turning. In the pre-training phase, layout clips are used as a training data set and layout feature is automatically extracted through several neural networks. Auto-encoder, which is one of the dimensionality reduction techniques in machine learning, is used to learn parameters of each neural network. In the fine-tuning phase, based on the trained neural networks, hotspot detection model is built with the training data including given labels, which consist of -1 for non-hotspots and +1 for hotspots. By using the extracted layout feature and trained model, high accurate detection with lower false-alarm is achieved. Experimental results show that using deep neural network can achieve better performance than other frameworks using manually-selected layout features and detection algorithms, such as conventional neural network or support vector machine.

9781-18, Session 5

## Patterns-based DTCO flow for early estimation of lithographic difficulty using optical image processing techniques

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Estimating and predicting lithographic difficulty during early stages of node development have always been a challenge to the design and patterning communities. Traditionally, design rule checking is evaluated by validating drawn geometries against predetermined rules and model-based validation techniques that unlikely to be mature enough to capture all the patterning challenges in early development stages.

In this paper, we introduce a fast and reasonably accurate methodology to determine patterning difficulty based on the fundamentals of optical image processing techniques along with Monte Carlo based random pattern generator to analyze the frequency content of the design shapes that determine the patterning difficulty via a computational patterning transfer function. In addition, we use this flow to generate a set of difficult patterns that can be used to evaluate the design ease-of-manufacturability via scoring methodology as well as to help in the optimization phases of post-tapeout flows.

In the early stages of the design cycle, the proposed flow does not require highly sophisticated models from the fab, yet it is based on the fundamentals of image processing techniques which make it fast and reliant on theoretically accurate principles that are independent of the details of the patterning process in the fab. This flow offers combined merits of scoring-based criteria and model-based approach for early designs. The value of this approach is that it provides to designers early prediction of potential problems even before the rigorous model-based DFM kits are developed. Moreover, the flow establishes a platform for interaction between the design and the manufacturing communities based on geometrical patterns.

9781-19, Session 5

## A random approach of test macro generation for early detection of hotspots

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Multiple-Patterning Technology (MPT) is still the preferred choice over EUV for the advanced technology nodes, starting the 20nm node. Down the way to 7nm and 5nm nodes, Self Aligned Multiple Patterning (SAMP) appears to be one of the effective multiple patterning techniques in terms of achieving small pitch of printed lines on wafer, yet its yield is in question. Predicting and enhancing the yield in the early stages of technology development are some of the main objectives for creating test macros on test masks. While conventional yield ramp techniques for a new technology node have relied on using designs from previous technology nodes as a starting point to identify patterns for Design of Experiment (DoE) creation, these techniques are challenging to apply in the case of introducing an MPT technique like SAMP that did not exist in previous nodes.

This paper presents a new strategy for generating test structures based on random placement of unit patterns that can construct more meaningful bigger patterns. Specifications governing the relationships between those unit patterns can be adjusted to generate layout clips that look like realistic SAMP designs. A via chain can be constructed to connect the random design of experiment (DoE) of SAMP structures through a routing layer to external pads for electrical measurement. These clips are decomposed according to the decomposition rules of the technology into the appropriate mandrel and cut masks. The decomposed clips can be tested through simulations, or electrically on silicon to discover hotspots.

The hotspots can be used in optimizing the fabrication process and models to fix them. They can also be used as learning patterns for DFM deck development. By expanding the size of the randomly generated test structures, more hotspots can be detected. This should provide a faster way to enhance the yield of a new technology node.

9781-20, Session 5

## Hotspot detection and removal flow using multi-level silicon-calibrated CMP models

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As we move to more advanced technology nodes the number of Chemical Mechanical Polishing (CMP) steps used in manufacturing a chip is increasing rapidly. At the same time, the feature scale, within chip and across wafer planarity requirements for said CMP steps are becoming more stringent. The complex pattern dependencies inherent in CMP processes, and the cumulative nature of the topography generated by these processes make it very difficult to meet the stringent uniformity requirements for the variety of designs produced. This causes manufacturing and yield related hotspots on

the designs. Accurately predicting hotspots and providing guidelines to fix them are therefore critical for CMP process development, yield ramp up and shorter design and manufacturing cycles.

In this paper we present a hotspot detection and removal flow. The flow uses Cadence Design System's manufacturing modeling methodology that accurately predicts feature scale, within chip, and wafer level topography. The modeling methodology takes into account etch depth, deposition and CMP variations across multiple levels in the design, and also across multiple process steps within a given design level. The modeling methodology predicts hotspots and generates fixing guidelines to fix/remove them. We demonstrate the hotspot detection and removal flow's application using manufacturing data from product designs.

9781-21, Session 5

## Migrating from older to newer technology nodes and discovering the process weak-points

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This paper will present a novel methodology for how to enumerate initial test patterns based on other technology node products. With this novel methodology, DRM development and process capability verification can be sped up rapidly compared to a traditional way. At the same time, the process weak-points can be migrated from the older technology nodes to new technology node. This will help the foundry catch process detractor patterns at new technology development at an early stage.

9781-22, Session 6

## Triple/quadruple patterning layout decomposition via novel linear programming and iterative rounding *(Invited Paper)*

Yibo Lin, Xiaoqing Xu, The Univ. of Texas at Austin (United States); Bei Yu, The Chinese Univ. of Hong Kong (China); Ross Baldick, David Z. Pan, The Univ. of Texas at Austin (United States)

As feature size of the semiconductor technology scales down to 10nm and beyond, multiple patterning lithography (MPL) has become one of the most promising candidates for lithography, along with other emerging technologies such as extreme ultraviolet lithography (EUVL), e-beam lithography (EBL) and directed self assembly (DSA). Due to the delay of EUVL and EBL, triple and even quadruple patterning are considered to be used for lower metal and contact layers with tight pitches. In the process of MPL, a layout is split into various parts and manufactured by different masks. e.g. in triple patterning lithography (TPL), three masks are used so the layout needs to be divided into three parts, which is also called layout decomposition. Similarly in quadruple patterning lithography (QPL), it is necessary to decompose a layout into four parts.

For any pattern pair, if two patterns are very close to each other, they should be split into different masks; otherwise, a conflict is introduced and it is not possible to manufacture them. In layout decomposition, each pattern can be viewed as a vertex in a graph. If two patterns are too close to be manufactured in the same mask, a conflict edge is introduced to connect corresponding vertices. Vertices that share the same conflict edge must be assigned to different masks, or labeled with different colors. Then the layout decomposition problem can be formulated into a graph coloring problem, shown as Fig. 1. i.e. TPL can be formulated to 3-coloring and QPL can be formulated to 4-coloring. The minimum distance to insert a conflict edge between two patterns is named as coloring distance.

Graph coloring is known as an NP-complete problem for color number larger than two. A layout may exist native conflicts such as 4-clique (K4) structure that is not 3-colorable. In Fig. 1(c), vertex a, b, c and d form a K4 structure, so at least four masks are needed. The main objective of layout decomposition is to minimize the number of conflicts. For metal layers, stitching is usually allowed to resolve conflicts; i.e. a pattern can be split into touching parts such that they can be labeled with different colors. But stitches are forbidden for contact and via layers. While layout decomposition is still different from traditional graph coloring, the NP-completeness still holds.

Previous work has studied the graph model formulation for layout decomposition problem and various algo- rithms have been proposed including integer linear programming (ILP), semidefinite programming (SDP) and other heuristic approaches.1–6 While it is true that ILP can solve the problem optimally, it suffers from ex- ponential runtime. SDP and other heuristic approaches are introduced to speedup the decomposition process with tradeoffs between runtime and solution quality. In order to improve the pattern uniformity on each mask, density balance is also introduced as a secondary optimization target during decomposition.7,8 For row based layout structures, even faster approaches have been proposed with the guarantee of optimality.9–12

In this paper, we focus on the application of layout decomposition where stitching is not allowed such as for contact and via layers. We propose an iterative rounding and linear programming (LP) solving technique to reduce the number of non-integers in the LP relaxation problem. The boundary vertices of feasible polyhedron space for LP are studied and an odd cycle based technique is developed to effectively reduce non-integer solutions. Given a layout with either rectangles or polygons where stitch insertion is forbidden, our goal is to provide high quality decomposition results efficiently while introducing as few conflicts as possible.

9781-23, Session 6

## Design strategy for integrating DSA via patterning in sub-7nm interconnects

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In recent years, major advancements have been made in the directed self-assembly (DSA) of block copolymers (BCP), and insertion of DSA for IC fabrication is being seriously considered for the sub-7nm nodes. At these nodes the DSA technology could alleviate costs for multiple patterning and limit the number of masks that would be required per metal layer. One of the most straightforward approaches for implementation would be for via patterning through templated DSA (graphoepitaxy), since hole patterns are readily accessible through templated confinement of cylindrical phase BCP materials [1].

Our studies show that decomposition of interconnect via layers in realistic circuits below the 7nm node would require more than six colors (multiple patterning steps) using 193nm immersion lithography. Even the use of EUV might require double patterning in these dimensions since the minimum via distance would be smaller than EUV resolution. The grouping of vias through templated DSA can resolve local conflicts in high density areas. This way, the number of required multi-patterning steps can be significantly reduced.

For the implementation of this approach, DSA-aware mask decomposition is required. In this paper, the imec design approach for via patterning in sub-7nm nodes will be discussed. We introduce a new methodology for efficient via grouping, and we propose options to expand the list of DSA-compatible

via patterns (DSA letters). Based on the alphabet approach, as described by Yuelin Du[2], we define letter cost formulas together with evaluation functions, and we develop a program which automates the via grouping process and gives the optimal coloring solutions. The tentative flowchart of this program is shown in Figure 2 of the supplemental file. The ultimate objective of this research is to test the methodology in a fully routed processor at sub-7nm node.

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9781-24, Session 6

## Enablement of DSA for VIA layer with a metal SIT process flow

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Among next-generation lithography techniques, directed self-assembly (DSA) of block copolymers (BCP) has received considerable attention. The main advantage of this method is cost reduction, thanks to the reduced number of lithographic steps. Meanwhile, the associated mask correction had to account for the introduction of this new technique maintaining a high level of accuracy and reliability.

In order to create a Vertical Interconnect Acess (VIA) layer, graphoepitaxy DSA is the main candidate. The technique relies on the creation of a confinement guide using optical microlithography methods, in which the BCP is allowed to separate into distinct regions. The resulting patterns are etched to obtain an ordered VIA layer. For technologies beyond 10 nm, 1D gridded designs are commonly used especially in a Self-Aligned Double Patterning (SADP) metal process: VIAs connecting metal line layers are placed along a discrete grid thus limiting the number of VIA pitch.

Guiding pattern variations impact directly the placement of the target and one must ensure that it does not interfere with the circuit performance. To prevent flaws, design rules are set. In this study, for the first time, an original framework is presented to find a consistent set of design rules for enabling the use of DSA in a production flow using SADP for metal line layer printing.

In order to meet electrical requirements, the collection area (the intersecting area) between VIA and metal lines must be sufficient to ensure correct electrical connection. This collection area is driven by both VIA placement variability and metal line printing variability. Based on a 10 nm node process assumptions, the Monte Carlo method is used to set a maximum threshold for VIA placement error.

In addition, to determine a consistent set of design rules, representative test structures have been created and tested with our inhouse placement estimator: the topological skeleton of the guiding pattern [2]. Structures with deviation above the maximum tolerated threshold are considered as infeasible and the appropriate set of design rules is extracted. In a final step, the design rules are checked with further test structures that are randomly generated using percolation in order to emulate a P&R standard cell block.

9781-25, Session 6

## Layout decomposition for a modular technology to solve the edge-placement challenges by combining selective etching, direct stitching, and alternating-material self-aligned multiple patterning processes

Hongyi Liu, Ting Han, Jun Zhou, Yijian Chen, Peking Univ. (China)

Although 1-D layout has shown significant advantages for leading-edge IC design and manufacturing, there exists a prohibitive barrier for its future success: edge-placement errors (EPE) in the cut and via patterning steps. To overcome the EPE challenges, we propose a modular patterning approach by combining layout stitching, selective etching, and alternating-material self-aligned multiple patterning (altSAMP) processes. By adopting this novel approach, we can potentially achieve higher processing yield and more 2-D design freedom for continuous IC scaling down to 5 nm.

Unlike the conventional single-material SAMP processes, the line arrays fabricated by an altSAMP process consist of two different materials which allow highly selective etching processes to remove one material (ideally) without attacking the other. For example, a line array arranged in an alternating order A-B-A-B..., as illustrated in Fig. 1, can be formed by alternating-material self-aligned quadruple/octuple patterning (altSAQP/ altSAOP) process, while a line array arranged in a quasi-alternating order A-B-B-A-B-B... (Fig. 2) can be fabricated by a self-aligned triple/sextuple (SATP/SASP) patterning process. To reduce the EPE effect, we decompose the holes over the lines made of material A into one mask and holes over the lines made of material B into the other mask, as illustrated in Fig. 3. After printing the cut holes using one mask, a following highly selective etching process will cut the targeted lines, (ideally) without attacking the exposed non-targeted lines (made of a different material). When two separate cutting steps are completed, the resultant 1-D patterns can be transferred to an underneath hard-mask layer for continuing the processing steps. Since the targeted-line density for each decomposed cut mask is half of the original array, the cut-hole patterning process can tolerate more severe EPE effect.

Next, we shall discuss several key features of cut-hole layout decomposition and synthesis algorithm. 1) The target layout is decomposed into two parts. Fig. 4 shows how to decompose the original cut-hole layout into two parts using A-B or A-B-B type of grating arrays. The holes over lines A are collected into part I, while the holes over the lines B are collected into part II. 2) To generate a cut-hole mask with the maximum patterning yield, we should optimize two parameters: margin and overhang as illustrated in Fig. 5. The margin space is to ensure that a misaligned cut hole will not lead to a miscut of the line ends. The overhang is to ensure a complete cutoff of the targeted lines with the minimum impact on the adjacent non-targeted lines. 3) When generating a conflicting graph for each decomposed mask as illustrated in Figs. 6(c) and (e), a node represents a cut hole, and an edge between two nodes indicates that these two holes are spaced within a threshold distance (determined by the minimum resolution). In general, generating the cut holes in one part (Figs. 7(c-d)) can be formulated as a coloring problem. Any two nodes connected by an edge represent a conflict and they should be assigned different colors. If only one mask (e.g., using EUVL) is designed for each part, we can merge those holes with the tightest pitch or redistribute their locations (see Fig. 7) to remove the edges/ conflicts. If two masks (e.g., using 193i) are designed for each part (Figs. 6(e-f)), the decomposition algorithm can be formulated as a two-coloring problem. If odd circles exist in coloring operation, we can merge/redistribute the holes or divide a cut hole into two small cut holes (Fig. 7) and assign them to two masks.

Similar to a SAMP+stitching process proposed before to avoid the via EPE issue, we can also use altSAMP+stitching process to pattern 2-D features. Such a concept to form 2-D layout is illustrated in Fig. 8. We first form the features in one (e.g., X) direction by an altSAMP process. After depositing a thin film, we continue to form the features in the other (e.g., Y) direction by another altSAMP process. Finally, the features in X and Y directions are combined and transferred to the same layer. In this patterning scheme,

the altSAMP process offers the functionality of density scaling while the stitching process creates 2-D design freedom and multiple-CD/pitch capability.

IC fabrication typically contains three types of critical layers: fin/gate, contact, and metal. According to the varying characteristics of each type of layer, different design/manufacture methods are explored. For the fin/gate layer, the 1-D features are highly regular, thus we can form them by an altSAMP process to reduce the cut-hole EPE effect. For 2-D metal layers, they can be manufactured by altSAMP+stitching process to avoid the via EPE issue. We evaluate our layout decomposition/synthesis techniques based on 15nm-node standard cells and the experimental results are shown in Tables 1 & 2, which verify the functionality of our method.

9781-26, Session 7

## Interlayer design verification methodology using contour image

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Memory industry has been pursuing endless shrinking technology which increases fabrication complexity. It poses problems between adjacent layers as well as within a single layer. Especially, patterning bridge and misaligned contact failures between two layers are so difficult to verify during the process inside fabrication line. For that reason, until now, we carry out electrical measurements and examine vertical structures using VSEM(Vertical SEM) on fab-out wafers. However, it requires a pretty long time to analyze the process after fab-out and importantly, we are not able to obtain reliable amount data due to limited sampling points. Also, in case of VSEM, it is a destructive examining process.

In order to overcome the difficulties of the problems mentioned above, we have developed the interlayer design verification methodology using contour image. Our methodology is comprised of 4-steps: preparation, measurement, data-processing, and design verification. In the 1st step, preparation, we define measured regions(or points) and prepare GDSII file for measured patterns. It is very important since it affects measurement step and design verification step. The 2nd step, measurement, is measuring the patterns of wafers. After measuring of patterns, we extract the contour images of the measured patterns using NGR (Nano Geometry Research) equipment. The 3rd step, data-processing, is to overlap each measured contour images onto the intended layout designs. Through this process, we are now able to extract the relation (like overlap, space, etc) between interlayer. We use our in-house developed tool to merge images and to extract data. (Fig. 1) The 4th step, design verification, is to analyze the extracted relation (overlap, space, etc) and verify the interlayer designs. A large amount of data can be collected and shows normal distributions which enable us to analyze the data statistically. We verify the interlayer design by specific criteria. (Fig. 2) The criteria is determined by fabrication, electrical characteristic, and other elements. Through this verification, we check on the margin of current interlayer design and give feedback on weak points and the amount of deficiency. (Fig. 3)

Our methodology makes it possible to verify interlayer design by extracting the contour image from the real patterns. So we can confirm the relation of interlayer visually from the real patterns. And we can verify interlayer design even during the fabrication process and conduct a non-destructive inspection. Also this methodology provides a large amount of measurement data. As previously stated, the statistical analysis of the extracted data enhances the degree of completeness and realizes the difference of process induced by different design environment. Through this methodology, we can calculate the margin of current interlayer design and suggest the requirement of design. And we will improve the interlayer design.

9781-27, Session 7

## The innovative PWQ method for accurate weak point extraction in DRAM

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In a sub 2Xnm node process, the feedback of pattern weak points or the possible issues is more and more significant. Therefore, the method of Process Window Qualification (PWQ) is very serious and essential these days. However, conventional method has critical problems. If comparison and control group have same problem, the issue patterns are not detected by current defect detecting approach. To overcome these problems, our company adapts die to data base matching PWQ process. Even though new method compares real pattern to layout, our margin decision process is based on image shape. Therefore, it has some problems.

First, inspection result analysis time is too long, so these long analysis time increases the developing period of new device. Moreover, because of the limitation of time and capability of reviewer, we cannot increase the inspection point or scan the large area. Consequently, the result of PWQ weak points cannot represent the all the possible defects. Finally, since the PWQ margin is not decided by the mathematical value, to make the solid definition of killing defect is impossible.

To overcome these inconvenience and problems, we have established an accurate and solid PWQ method.

The overall atmosphere of our new method is as follows. Firstly, before the inspection start, the layout is predefined so that we can measure the places where we want to observe. Next, the measuring results are classified according to pattern shape. Finally, we extract the certain statistical values from the classifying data, such as median, standard deviation, dispersion, etc. And it shows the possible issue points which are based on previously extracting values. The biggest advantage of this method is that we can extract the pattern weakness by the quantitative analysis.

As a result, it is possible to see the genuine margin of the critical pattern issue which we cannot see on our conventional PWQ inspection; hence we can enhance the accuracy of PWQ margin.

9781-28, Session 8

## Verification and application of multi-source focus quantification

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The concept of the multi-source focus correlation method was presented in 2015 [1, 2]. A more accurate understanding of real on-product focus can be obtained by gathering information from different sectors: Design, short loop scanner monitoring, scanner leveling, on-product focus and topography.

This paper will follow up by showing that we can predict across chip topography from reticle data in terms of density and perimeter density, including experimental proof. In order to visualize the potential applications of this different pixel sizes will be used to perform the correlation, in-line with the minimum resolution, correlation length of CMP effects and scanner level sensor spot size. Potential applications of the topography determination will be evaluated, including optimizing scanner leveling by ignoring non-critical parts of the field, and without the need for time consuming offline measurements.

**Conference 9781: Design-Process-Technology Co-optimization for Manufacturability X**

9781-29, Session 8

## A comparative study on the yield performance of via landing and direct stitching processes for 2D pattern connection

Jun Zhou, Yijian Chen, Peking Univ. (China)

As leading-edge IC design and manufacturing made their way through the technical barrier of optical scaling, non-scalable edge-placement errors (EPE) present in the cut and via patterning steps seem to be prohibitive challenges. There exist two 2-D layout design methodologies for current and future IC scaling. The first approach (see Figs. 1(e-h)) is to decompose random 2-D patterns into two layers and each layer contains unidirectional 1-D dense arrays which are patterned with a SAMP or DSA process followed by multiple cut steps to form the desired circuit patterns. The features decomposed into different layers are physically located at two levels and connected through vertical vias. This is often called 1-D gridded design, which involves via landing accuracy between two lines (e.g., metal 1) located at different levels. To avoid the via EPE challenges, we proposed a direct stitching technique (see Figs. 1(a-d)) to form random 2-D patterns. In this approach, the 2-D target layout is also decomposed into two components, and each component contains one or multiple sets of unidirectional patterns which can be patterned by a SAMP+cut process. However, the final 2-D patterns are formed by directly stitching two components together without using connecting vias, which can potentially achieve higher processing yield and more 2-D design freedom. Therefore, a quantified and comparative study on the yield performance of via landing and direct stitching processes for 2-D pattern connection is critical to understand and evaluate their technical merits and limitations.

As shown in Fig. 2(a), various types of process variations (e.g., misalignment, line/space and via CD variation) can cause the yield loss of via landing. Similarly, as shown in Fig. 2(b), the direct stitching technique suffers from these process variations as well. In our previous papers, the yield models of the hole landing (on one single line) and direct stitching were developed based on the concept of POF (probability of failure) or POS (the probability of success, POS=1-POF). Nevertheless, the yield model of via landing is more complicated as it needs to consider the impacts of its overlay accuracy with respect to both top and bottom lines. Moreover, as shown in Fig. 3, the neighboring features can cause further yield loss of via landing if an undesired feature contact occurs. Our preliminary calculation results (see Fig. 4) show that via landing yield performance is more sensitive to ? (standard deviation of the overlay errors) compared with the direct stitching process. We also found that in many cases, yield performance of the direct stitching technique is significantly better than the via landing process (which is required by 1D gridded design). In this paper, we shall extensively investigate the possible conditions and mechanisms that can degrade the yield performance of both via landing and direct stitching processes, and identify the most valuable approach for continuous IC scaling down to 5 nm.

9781-30, Session 8

## Estimate design sensitivity to process variation for the 14nm node

Guillaume Landie, Vincent Farys, STMicroelectronics (France)

Looking for the highest density and best performance, the 14nm technological node saw the development of aggressive designs, with design rules as close as possible to the limit of the process. Edge placement error (EPE) budget is now tighter and Reticle Enhancement Techniques (RET) must take into account the highest number of parameters to be able to get the best printability and guaranty yield requirements. Overlay is a parameter that must be taken into account earlier during the design library development to avoid design structures presenting a high risk of performance failure.

This paper presents a method taking into account the overlay variation and the Resist Image simulation across the process window variation to estimate the design sensitivity to overlay. Areas in the design are classified with specific metrics, from the highest to the lowest overlay sensitivity. This classification can be used to evaluate the robustness of a full chip product to process variability or to work with designers during the design library development. The ultimate goal is to evaluate critical structures in different contexts and report the most critical ones.

In this paper, we study layers interacting together, such as Contact/Poly area overlap or Contact/Active distance. ASML-Brion tooling allowed simulating the different resist contours and applying the overlay value to one of the layers. Lithography Manufacturability Check (LMC) Detectors are then set to extract the desired values for analysis.

Two different approaches have been investigated. The first one is a systematic overlay where we apply the same overlay everywhere on the design. The second one is using a real overlay map which has been measured and applied to the LMC tools. The data are then post-processed and compared to the design target to create a classification and show the error distribution.

We finally explore the different solutions available to help optimizing the design. For this, we have evaluated a tool called Design Rule Optimization (DRO) that will look for the best design configuration to limit the failure risk and offer the biggest Process Window Exposure Latitude.

# Conference 9782: Advanced Etch Technology for Nanopatterning V

Monday - Tuesday 22–23 February 2016

Part of Proceedings of SPIE Vol. 9782 Advanced Etch Technology for Nanopatterning V

9782-1, Session 1

## Advanced patterning techniques: Etch opportunities and responsibilities *(Keynote Presentation)*

Richard Schenker, Intel Corp. (United States)

No Abstract Available

9782-2, Session 1

## EUV for sub-10nm logic *(Keynote Presentation)*

Anthony Yen, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

No Abstract Available

9782-3, Session 1

## Etch technologies for 7nm and 5nm nodes *(Invited Paper)*

Akihisa Sekiguchi, Tokyo Electron Ltd. (Japan)

No Abstract Available

9782-4, Session 2

## Atomic layer processing for nanopatterning *(Invited Paper)*

Erwin Kessels, Technische Univ. Eindhoven (Netherlands)

The realization of nanoscale devices is increasingly relying on nanopatterning approaches that go well beyond conventional lithography. Atomic layer processes such as atomic layer deposition (ALD) are gaining considerably in importance. In self-aligned double and quadruple patterning (SADP and SAQP) atomic layer deposition is used to conformally deposit spacer materials and these patterning schemes have become indispensable in present day technology nodes. However to scale devices to 7 nm and beyond, new breakthroughs will be required. Atomic layer etching (ALEt) is considered necessary in advanced plasma etch technology due to the need for tight control of etch variability. In this contribution the status and prospects for ALEt will be discussed as well as other novel nanopatterning paradigms relying on atomic layer processing. The chemical and physical principles underlying the atomic layer processing methods will be highlighted.

9782-5, Session 2

## Paths toward low-damage etching of highly porous organo-silicate low-k dielectrics *(Invited Paper)*

Jean-François de Marneffe, Liping Zhang, Mikhail R. Baklanov, IMEC (Belgium); Koichi Yatsuda, Tokyo Electron Ltd. (Japan); Kaoru Maekawa, TEL Technology Ctr., America, LLC (United States); Mike Cooke, Andy Goodyear, Oxford Instruments Plasma Technology Ltd. (United Kingdom); Christian Dussarrat, Air Liquide Labs. (Japan); Remi Dussart, Thomas Tillocher, Floriane Leroy, Philippe Lefaucheux, Group de Recherches sur l'Energétique des Milieux Ionisés (France); Mitsuhiro Watanabe, IMEC (Belgium)

Integration of ultra-low-k dielectric becomes more challenging as technology nodes move to smaller dimensions. Amongst the various steps involved in interconnects fabrication, plasma etching is particularly damaging, mainly due to reactive radicals and VUV photons [1]. In the present paper, various options towards low-damage patterning of low-k materials will be exposed, from the concept to the approaches and methods. For the ULK to remain unaffected by plasma exposure, radical as well as VUV damage need to be minimized. A temporary material densification by sacrificial filler is the most promising concept nowadays [2]. ULK densification can occur through various approaches, where temperature is the key factor. Methods, depending on the approach used, require major changes in the interconnect flow with little change at etch level, or more stringent etch hardware modifications to achieve low temperature or cryogenic temperatures [3]. The protection mechanism will be discussed [4,5]. An alternative route is pore sidewall passivation or 'carpeting' with a permanent coating agent. Pore carpeting is more difficult, since it combines both material and processing challenges: protection against plasma radicals and low dielectric permittivity. Finally, VUV damage and mitigation strategies will be addressed [6].

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9782-6, Session 2

## Etch transfer of sub-20nm half pitch patterns printed using thermal scanning probe lithography *(Invited Paper)*

Armin W. Knoll, Colin Rawlings, Heiko Wolf, Urs Dürig, IBM Research - Zürich (Switzerland)

Thermal Scanning Probe Lithography (tSPL) is an AFM based patterning technique, which utilizes heated tips to locally evaporate a thermally sensitive polymer. The method allows for sub 10 nm half pitch patterning in the thermally sensitive resist, linear speeds of cm/s, and precise 3D relief patterning. Similar to other techniques, high resolution is accompanied with a limited patterning depth, which poses challenges on the transfer of the written structures into useful devices.

We have developed an etch transfer process based on a three layer transfer

stack which allows us to process the patterns of about 10 nm depths reliably into the substrate or to perform metal lift-off processes [1]. The key ingredient in the transfer stack is an ultrathin evaporated SiO 2 hardmask layer. The hardmask is used to amplify the pattern into a 50 nm thick polymeric transfer layer. The transfer layer subsequently serves as an etch mask for transfer into silicon or for metal lift-off processes.

During the past years we have optimized the transfer stack and improved the achievable half pitch density after pattern transfer from 28 nm [2] to 13.8 nm.

Patterns written at 18.3 nm [3] and 13.8 nm half pitch were successfully transferred into silicon (see figure). The line edge roughness (3?) was evaluated to be approximately 3 nm both in the transfer layer and in silicon.

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9782-7, Session 2

## DC superimposition in CCP etchers for advanced patterning

Mingmei Wang, Vinayak Rastogi, Hongyun Cottle, Andrew W. Metz, Alok Ranjan, TEL Technology Ctr., America, LLC (United States)

A negative DC superposition on top of a CCP chamber was investigated using Hybrid Plasma Equipment Model (HPEM) simulation and experiment. By applying a high negative DC voltage on top electrode, a strong negative DC sheath is formed. Due to ion/electron bombardment of top electrode surface, secondary electrons are generated and accelerated by the negative DC sheath. Those secondary electrons with high energy can traverse through bulk plasma and reach wafer surface during negative RF cycle. The high energy electron (HEE) beams are capable of modifying surface material properties, modulating bulk plasma densities, changing wafer surface electron energy distribution functions (EEDFs), and neutralizing positive charges deep in features etc.

Gas chemistries such as Ar, H2, N2 and hydrofluorocarbon plasmas have been tested by applying a negative DC voltage on the top electrode. EEDFs, HEE fluxes, plasma densities, will be discussed for aforementioned chemistry. Experiments are conducted on 193 and EUV photoresist (PR) to investigate how these conditions will impact the resist properties, such as LER/LWR, etch resistivity, thickness etc. A typical tri-layer stack (Resist/ ARC/Planarizer Layer) has also been used to investigate critical patterning issues including X/Y shrink ratio and high aspect ratio soft material (e.g. OPL) wiggling. HEEs are capable of reducing charge effects in narrow structures and help improve shrink ratio in, e.g., contact etch. HEEs can penetrate deep into OPL to produce crosslinking which makes the material harder and decreases wiggling during etch. Impact of system parameters and trends will be discussed regarding chemistries under consideration.

9782-8, Session 3

## Patterning challenges in advanced device architectures: FinFET to nanowire *(Invited Paper)*

Naoto Horiguchi, IMEC (Belgium)

No Abstract Available

9782-9, Session 3

## 193nm trilayer negative-tone development process for patterning magnetic tunneling junctions *(Invited Paper)*

Qinghuang Lin, Sebastian U. Engelmann, Armand Galan, Steve Holmes, Gen Lauer, Nathan Marchack, Janusz J. Nowak, Eugene O'Sullivan, Yu Zhu, Eric A. Joseph, Anthony J. Annunziata, IBM Thomas J. Watson Research Ctr. (United States)

Spin-transfer torque (STT) magnetic random access memory (STT-MRAM) is a leading candidate to replace dynamic random access memory (DRAM) when DRAM scaling approaches its physical limits. STT-MRAM bits are pillar-shaped magnetic tunnel junction structures, which must be patterned into large arrays with a very uniform pillar diameter distribution. Since pillar structures are not normally found in CMOS logic applications, new lithography and etching processes must be developed. In this paper, we present a 193 nm trilayer negative-tone development (NTD) process for patterning magnetic tunneling junction pillars. This 193nm trilayer NTD process has significantly improved critical dimension uniformity (CDU) in comparison to a 193nm positive-tone development (PTD) process. Moreover, we have used this process to demonstrate structural yield of magnetic tunnel junction pillars down to < 10 nm critical diameter.

9782-10, Session 3

## Plasma etch patterning of EUV lithography: balancing roughness and selectivity trade off

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EUV based patterning is one of the frontrunner candidates enabling scaling for future technology nodes. However it poses the common challenges of 'pattern roughness' and 'etch resistance' aspect which are getting even more critical as we work on smaller dimension features. Continuous efforts are ongoing to improve resist materials and lithography process but the industry is slowly moving to introduce it at high volume manufacturing. Plasma Etch processes have the potential to improvise upon the incoming pattern roughness and provide improved LER/LWR downstream to expedite EUV progress.

In this work we will demonstrate the specific role of passivation control in the dual-frequency Capacitively Coupled Plasma (CCP) for EUV patterning process with regards to improving LER/LWR, resist selectivity and CD tunability for line/space patterns. We will draw the implicit commonalities between different passivation chemistry and their effectiveness for roughness improvement. The effect of relative C:F and C:H ratio in feed gas on CFx and CHx plasma species and in turn the evolution of pattern roughness is drawn. Data that shows the role of plasma etch parameters impacting the key patterning metrics of CD, resist selectivity and LER/LWR will be presented.

**Conference 9782:**
**Advanced Etch Technology for Nanopatterning V**

9782-11, Session 3

## Plasma etching processes for the integration of III-V materials with Si for CMOS and photonic applications

Erwine Pargon, Maxime Bizouerne, Guillaume Gay, Camille Petit-Etienne, Laurent Vallier, LTM CNRS (France); Pauline Burtin, Mélisa Brihoum, Sébastien Barnola, CEA-LETI (France)

III-V semiconductor compounds such as InGaAs, InAlAs, InGaP are known for their unique optical and electronic properties and are today widely used for optoelectronic and high-frequency applications (LED, laser...). In recent years, the progress in molecular wafer bonding technology [1] allows to seriously consider integrating III-V materials with Silicon. If successful, the integration of III-V materials with Si paves the way for a wide range of novel device designs for optoelectronic, microelectronic and photovoltaic applications. Such integration takes advantages of both III-V materials properties and the maturity and scale of Si processing. For instance, hybrid photonic integrated circuits proposes to elaborate passive components (waveguides, filter..) in the Silicon On Insulator (SOI) substrate and to use III-V materials for specific functionality such as light emitter [2] (cf. Figure1). As the scaling of conventional CMOS technology approaches fundamental quantum limits, III-V integration with Si could also provide an effective and practical solution for high speed and high density circuit application for sub-10nm technological node (cf. Figure 2). For all these future technologies, development of industrial processes for III-V materials dry etching is necessary. In the present study, we investigate the etching mechanisms of III-V materials and especially In based compounds (such as InP and InGaAs) with the objective to develop plasma etching processes allowing their integration on SOI wafers for advanced CMOS and photonic devices. In photonics, high etch rates, high selectivity over the SOI, and pattern anisotropy are the main process requirements and could be obtained using assistance of wafer heating during the plasma process. In CMOS, the main key issues are the patterning of the III-V material with a nanometric control and without any plasma induced damage. In this study, we provide some insights to fulfill the process specifications for both applications by correlating XPS, ellipsometry, and AFM surface analyses. Etching experiments have been carried out on 200mm industrial etching platform from AMAT composed of two ICP chambers, whose one is equipped with a hot cathode. An XPS analyses chamber is connected via transfer chamber to the reactors in order to characterize quasi in-situ the surface of the III-V materials surface after etching and to bring some fundamental understanding of the plasma surface/interaction.

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9782-12, Session 4

## Self-aligned-quadruple-patterning for N7/N5 silicon fins *(Invited Paper)*

Efrain Altamirano-Sánchez, Tao S. Zheng, IMEC (Belgium)

The continuous increment of pattern density with the aim of following Moore's law has brought many challenges to the integration processes involved in the manufacturing of integrated circuits (IC). For example, fins specifications for N7 and N5 technologies are very tight and difficult to imagine few years ago but possible to reach thanks to the technological progress on plasma deposition and etching tools. The specifications for N7/N5 on pitches ranging from 18 to 24 nanometers are as follow. Critical dimension (CD) after etch is required to be about 7nm with a CD uniformity (CDU) control of 0.5nm (3sigma). The LWR and LER should be in the sub nanometer range if we consider that the LWR has to be 10% of CD. Among all the challenges to comply with the latter specification, a major challenge relies on metrology, which has to have the resolution to determine the roughness of such small features. In order to rely on the CDSEM values, we have been working on multi-metrology package (CDSEM, 3DAFM and planar TEM). Another specification is the fin height and the profile, which is set to 120 nm and 89-90 deg on the top 50 nm.

In this study, we developed a self-aligned-quadruple-patterning that has the potential to deliver N7 and N5 fin requirements, keeping an eye on the cost. The patterning stack is composed of Pad oxide (SiO2) and Pad nitride (SiN); these layers are required for further fin process integration like oxide fill, CMP and oxide recess. Thus, these layers are not determined by the SAQP patterning strategy. Two layers are definitely required for the quad pattern formation, aC and aSi which are the cores. The DARC (SiOC) and BARC are require for lithography reflectivity control. Thus in this SAQP scheme we just need a couple of layers and two spacer depositions (both SiO2 low temperature ALD) to develop a process capable to comply with N5/N7 specifications. Compared to SAQP schemes where the mandrels are only aSi, our approach is about 20% lower in cost. This mainly due to the use of aC core and the elimination of etch-stopping-layers. We will show results of the full SAQP development where the fin CD is about 7 nm and the depth is about 110 nm.

In this contribution, each step for the quad pattern formation will be discussed: from lithography to the fin patterning. We will show the metrology challenges and full map 300 mm wafer evolution step by step. Pitch walking optimization, which is still ongoing, will be as well discussed.

9782-13, Session 4

## Optical metrology for advanced process control: full module metrology solutions *(Invited Paper)*

Cornel Bozdog, Nova Measuring Instruments Inc. (United States); Igor Turovets, Igor Turovets, Igor Turovets, Nova Measuring Instruments Ltd. (Israel)

No Abstract Available

9782-14, Session 4

## Self-aligned quadruple patterning integration using spacer on spacer pitch splitting at the resist level for sub-32nm pitch applications

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Multiple patterning integrations for sub 193nm lithographic resolution are becoming increasingly creative in pursuit of cost reduction and achieving desired critical dimension. Implementing these schemes into production can be a challenge. Aimed at reducing cost associated with multiple patterning for the 10nm node and beyond, we will present a self-aligned quadruple patterning strategy which uses 193nm immersion lithography resist pattern as a first mandrel and a spacer on spacer integration to enable a final pitch of 30nm. This option could be implemented for front end or back end critical layers such as Fin and Mx. Investigation of combinations of low temperature ALD films such as TiO, Al2O3 and SiO2 will be reviewed to determine the best candidates to meet the required selectivities, LER/LWR and CDs. Several challenges arise with spacer on spacer pitch splitting such as first spacer shape impact on second spacer deposition profile and final etch profiles as well as pitch walking control.

In this presentation we will highlight the unique etch challenges associated with spacer on spacer SAQP patterning strategy and summarize our efforts in optimizing the patterning stack, etch chemistries and process steps

to provide a viable alternative to other conventional multiple patterning schemes. We will compare this new integration scheme with previously presented SAQP flows and show the benefits / disadvantages of pursuing this new strategy in terms of LER/ LWR performance, CD targeting, final etch profiles and cost benefits.

9782-15, Session 4

## PMMA removal selectivity to PS using dry etch approach: Mechanism understanding and sub-10nm patterning application

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For sub-10nm patterns, the semiconductor industry is facing the limits of conventional lithography to achieve narrow dimensions. Among the different approaches investigated Directed Self-Assembly (DSA) of Block Copolymers (BCP) is one of the most promising solutions due to its simplicity, its low cost of operation and its capability to design high density patterns (with cylinder or line shapes). Today, PS-b-PMMA is a well-developed block copolymer for these applications. One critical challenge for their integration is the PMMA removal selectively to PS. In the first approach, the benefits of using an acetic acid have been presented in previous papers for contact applications, but the major drawback is the risk of pattern collapse for line application. Therefore the etch plasma approach appears as the most promising as mentioned in the literature for contact or line applications.

This paper is dedicated to PMMA removal selectively to PS using dry etch approach. We have screened different oxidizing and reducing plasma chemistries. Using CO gas provides a PMMA:PS infinite selectivity at 5s thanks to the deposit on PS and the PMMA etching. However after few seconds of process, a saturation etching phenomenon is observed on PMMA preventing its removal. CO impact on PS and PMMA has been determined with X-ray Photoelectron Spectroscopy (XPS). According to these analyses, it has been proved that a carbon-oxide layer is formed onto the polymer and increases with the process time on each material helping the deposit above PS and causing the etch stop phenomenon on PMMA. By combining CO with dihydrogen or xenon gas, this saturation phenomenon can be avoided but the selectivity will be lower than for CO only.

In this paper, we proposed two strategies to remove PMMA with a very high selectivity to PS (>20:1). Based on the characterized phenomena involved by CO chemistry, a CO-based chemistry has been developed to avoid PMMA etch stop phenomenon conserving the non-PS etching. An oxygen-free chemistry has also been proposed. By controlling the polymerization of fed gas on the polymers, PMMA removal can be achieved without consuming PS with this oxygen-free chemistry.

These chemistries have been applied on cylindrical and lamellar patterns. They have been studied in terms of selectivity and pattern fidelity. It has been proved that they provide a full PMMA removal with a selectivity of 8:1 to PS. According to this, the PS pattern thickness has been perfectly conserved and the dimensions not impacted by the PMMA removal.

To evaluate the new developed chemistries, PS patterns have been transferred into dielectric layers for cylindrical and lamellar patterns. These transfers are a proof of the good PMMA removal because patterns are successfully transferred into sublayers while conserving initial dimensions. Finally, these chemistries have been applied for block copolymers into a DSA grapho-epitaxy integration scheme.

9782-16, Session 5

## Evaluation of ALE processes for patterning *(Invited Paper)*

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Atomic layer etch processes have gathered much interest recently. Alternating cycles of deposition and etching are applied to the plasma process, eliminating some of the tradeoff behaviors typically associated with conventional plasma processes.

Patterning processes require the utmost control on critical dimension (CD), line edge roughness (LER) and line width roughness (LWR). Maybe one of the most crucial issues during manufacturing is the pattern transfer from a soft mask (carbon based) material into a hard mask material. A very characteristic phenomenon is that mechanical failure of the soft material may be observed and/or severe LER/LWR evolution as well as CD change. As such, atomic layer processes with the promise of control at the atomic scale may provide new pathways for patterning multilayer stacks. However understanding of atomic layer processes is still lacking on a fundamental level.

Nevertheless, the impact of ALE-like (cyclic) patterning processes on LER/ LWR evolution have been evaluated. The impact of different process gases as well as patterning stacks will be discussed in detail.

9782-17, Session 5

## Edge roughness characterization of advanced patterning processes using power spectral density analysis (PSD) *(Invited Paper)*

Shimon Levi, Applied Materials, Ltd. (Israel)

No Abstract Available

9782-18, Session 6

## Atomic precision etch using a low-electron temperature plasma *(Invited Paper)*

Shahid Rauf, Applied Materials, Inc. (United States)

No Abstract Available

9782-19, Session 6

## Interactions between plasma and block copolymers used in directed self-assembly patterning *(Invited Paper)*

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The directed self-assembly (DSA) of block copolymers offers a promising route for scaling feature sizes below 20 nm. At these small dimensions, plasmas are often used to define the initial patterns. It is imperative to understand how plasmas interact with each block in order to design processes with sufficient etch contrast and pattern fidelity. Symmetric lamella forming block copolymers including, polystyrene-b-poly(methyl

methacrylate) and several high chi silicon-containing and tin-containing block copolymers were synthesized, along with homopolymers of each block, and exposed to various oxidizing, reducing, and fluorine-based plasma processes. Etch rate kinetics were measured, and plasma modifications of the materials were characterized using XPS, AES, and FTIR. Mechanisms for achieving etch contrast were elucidated and were highly dependent on the block copolymer architecture. For several of the polymers, plasma photoemissions were observed to play an important role in modifying the materials and forming etch-resistant protective layers. Furthermore, it was observed for the silicon- and tin-containing polymers that an initial transient state exists, where the polymers exhibit an enhanced etch rate, prior to the formation of the etch-resistant protective layer. Plasma developed patterns were demonstrated for the differing block copolymer materials with feature sizes ranging from 20 nm down to approximately 5 nm.

9782-20, Session 6

## A route for industry compatible DSA oh high X PS-PDMS diblock copolymers *(Invited Paper)*

Olivier Joubert, LTM CNRS (France)

No Abstract Available

9782-21, Session 6

## 450mm etch process development and process chamber evaluation using 193i DSA guided pattern

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During 450mm etch development, challenging feature sizes at the 14nm node and below are needed for process development and chamber performance evaluation. Traditional techniques such as sidewall image transfer (SIT) require multiple film deposition steps and etch steps to achieve small feature sizes in the etch transfer or hardmask pattern. This approach requires the readiness of many film deposition tools, such as atomic layer deposited (ALD) SiN, which are not yet available on 450mm equipment platforms. These upstream processing gaps could delay the actual etch application work a year or more. Additionally, the SIT approach itself requires etch process development, such as sidewall spacer etch and mandrel removal at larger pitch, which could add an extra six months to one year.

In the Global 450mm Consortium (G450C), a 193nm immersion guided directed self-assembled (DSA) pattern has been used to create challenging patterns. Block copolymer (BCP) material was coated directly onto a patterned tri-layer 193nm immersion exposed wafer and baked. As a result, smaller line/space patterns were formed between photoresist lines. Only one litho pass is needed. The first guided DSA patterned wafer was produced, refined, and ready for etch process development within a month of the G450C's first 193i patterned wafer availability.

Using 193i guided DSA patterns, a 28nm pitch STI stack and a 40nm pitch M1 BEOL stack were created. The initial etch baseline processes were scaled up from 14/10nm advanced node capabilities on the 300mm platforms to their respective 450mm platform. The STI stack includes BCP, neutral layer, SiARC, an amorphous carbon layer (ACL), SiN, SiO2, and Si etches. The BEOL stack includes BCP, neutral layer, SiARC, ODL, TiN, SiO2, low-K and SiCN etches. Flow and power scaling factors were obtained. The process results including etch rate, etch uniformity, CD, and etch profile (across-wafer; up to 1.5mm-3.0mm from the wafer edge) were studied. All etch tools in the SUNY Polytechnic Institute's G450C fab facility are included in this work.

During the process development, the process parameters were varied. The effects of various process knobs, including ESC temperature, gas injection, coil current ratio, and power pulsing were investigated to fine tune each etch step. Process window was investigated and compared to current 300mm etch chambers.

Using the developed baseline processes, a Passive Data Collection of ten wafers (blanket wafers with 144 measurement points each) was performed on each chamber. Within wafer, wafer-to-wafer and run-to-run variations were analyzed and tool process stability data was obtained. Excellent process stability results were shown for all current etch chambers.

Although the initial DSA layers contained a higher than desired dislocation density, the G450C Etch team was able to use DSA guided wafers for initial process development. The G450C Lithography team is currently working on reducing defects and providing additional patterning capabilities (contact, overlay, etc). Through these developments, the Etch and Lithography teams are able to provide needed structures for downstream process development including metal/dielectric deposition, post-etch cleans, CMP, and electrical testing.

9782-22, Session PS1

## Predicting LER and LWR in SAQP with 3D virtual fabrication

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The continued scaling of transistor and interconnect feature size and the introduction of 3D structures such as FinFETs and 3D NAND into CMOS process technology has brought significant challenges to process control of key structural variation sources such as line-edge roughness (LER) and line-width roughness (LWR). In this work, process impact on LER and LWR in a SAQP flow has been investigated, for the first time, through predictive 3D virtual fabrication. Deposition and etch effect on LER and its frequency response has been systematically studied.

This work makes exclusive use of Coventor's SEMulator3D virtual fabrication software platform for predicting intricate process interactions in integrated technologies. The initial LER is applied through lithography. In the random line generation algorithm, noise of multiple characteristic wavelengths and amplitudes are superimposed to form exposure edges with the expected LER. Figure 1 shows an example of random LER edge that matches realistic LER generated by 1-D Fourier synthesis technique. The SAQP model is implemented through predictive modeling of each process step in the SAQP flow. LER and LWR extraction is conducted using advanced virtual metrology.

Line edges involved in SAQP flow are categorized into 4 functional edges: edge 1 is created after lithography; edges 2 is created from edges 1 after

the 1st spacer deposition; edges 3 and 4 are created from edges 1 and 2 respectively after the 2nd spacer deposition. Figure 2 illustrates the four functional edges in the final structure and the evolution of each edge through SAQP flow.

LER is plotted against each critical process step in SAQP flow following the introduction in lithography, and grouped by functional edges. It is shown that spacer deposition reduces LER by creating new functional edges, while etch has minimal impact in this effect. The post-lithography and final LWRs are shown in Figure 4. There are four resulting LWRs in SAQP flow, labeled by the source edges. The inset shows the evolution of all edges through SAQP flow. The LER of the initial two edges (1A and 1B) are randomly generated and are uncorrelated, indicated by the different outlines in the inset of Figure 4. Spacer deposition creates new edges that are correlated to its original edge: for example, edge 2A is generated from 1A through 1st spacer deposition. This study shows: LWR of 1A2A and 1B2B are small due to correlated edges; LWR of 3A3B is unchanged because of high LER of the uncorrelated edges, and LWR of 4A4B is improved due to low LER of individual uncorrelated edges.

Design of experiments has been conducted where LERs with four different wavelength has been individually applied, and the LER through SAQP process has been analyzed (Figure 5). LER reduction from etch and deposition are extracted (Figure 6). It shows that etch effectively reduces high frequency LER while deposition improves LER across a wider frequency range.

Frequency-dependent etch and deposition effect on LER in SAQP flow has been studied by conducting design of experiments and virtual metrology through SEMulator3D virtual fabrication. Factors impacting final LWR have also been analyzed. Spacer technology creates correlated edges, significantly reducing LWR. Further LWR reduction can be achieved by optimizing LER.

9782-23, Session PS1

## Etch proximity correction through machine-learning-driven etch bias model

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Due to etch proximity e?ect, a design layout should be modified through etch proximity correction (EPC) to compensate for etch bias before it is submitted to OPC and subsequent optical lithography. The extent of etch proximity effect, called etch bias, is a?ected by the amount of particles (e.g. ions or radicals) that collide with substrate surface together with their incidence angle and direction. Accurate prediction of etch bias in full chip level is thus not feasible, so EPC often relies on empirically obtained rules or models. A rule-based EPC has been adapted for years over several technology nodes, but simple rules alone cannot accurately correct various patterns; it is expected that, in 10-nm technology, on-chip variation (OCV) is still up to 28% beyond the tolerance after rule-based EPC is applied. In model-based EPC, a few empirical parameters such as density-, visible-, and blocked-signals are used to predict etch bias; but post-EPC OCV is still not satisfactory enough.

Our approach to EPC is guided by artificial neural network (ANN). A set of polygon edges, called segments, is identified from a sample layout. For each segment, a number of parameters (local densities and image slope) are extracted by examining nearby segments. These parameters become the inputs of ANN, which outputs predicted etch bias of a segment; in other words, each segment is trained through ANN for its etch bias while nearby segments are involved in training process. This is repeated for each segment and for a number of sample layouts, so that a variety of trained segments are prepared beforehand. During actual EPC, the parameters of each segment are identified and used to extract the predicted etch bias.

The accuracy of output etch bias from the network is determined by chosen parameters and a set of test segments used for training. A local pattern density is measured at a few positions along concentric circles, whose centers coincide with the center of a segment; the density value corresponds to the amount of etching particles, and the measurement position is associated with the incidence angle and direction of the particles. An intensity slope is also included as a parameter to take account of a side wall angle of the resist, which a?ects etch bias. Local densities and image slope model etching phenomena better than the parameters in conventional model-based EPC in physical point of view. Test segments are prepared as follows: for each segment in sample test layouts as well as from synthetic test patterns, parameters are extracted and arranged as a vector; each segment is thus identified as a point in n-dimensional space; nearby points are clustered and we pick only one point from each cluster. In this way, we maintain a small number of test segments, while they still represent a variety of segments in the space.

The proposed EPC is implemented on top of Proteus, which is commercial OPC and EPC package. It is compared to both rule- and model-based EPC that Proteus supports in terms of prediction accuracy and runtime.

9782-24, Session PS1

## RIE challenge for fabrication of half-pitch sub-10nm lines and spaces pattern using directed self-assembly

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Recently, Directed Self-Assembly (DSA) has attracted semiconductor device manufacturers' attention. By combining micro-phase separation of block copolymers (BCP) with lithographically defined pre-patterns, sub-10 nm patterning becomes feasible using 193 nm lithography or EUV lithography. In order to realize sub-10nm patterning, high level polymer-polymer interaction is required. These BCPs are known as high-chi BCP. The chi is a Flory-Huggings interaction parameter which gives a measure of the interaction of the polymer-polymer interaction.

A Silicon-containing BCP is one of the promising high-chi materials for semiconductor manufacturing. The Silicon-containing BCP has not only a high polymer-polymer interaction but also can realize a high Reactive Ion Etching (RIE) endurance during a dry development and pattern transfer to an under-layer. Polystyrene-b-polydimethylsiloxane (PS-b-PDMS) is known as high-chi material with a potential for sub-10 nm patterning. [1] However, the lines can be obtained from the parallel oriented PDMS cylinders. Poly (polyhedral oligomeric silsesquioxane methacrylate)-b-poly(trifluoroethyl methacrylate) PMAPOSS-b-PTFEMA that has a great potential to fabricate half pitch (HP) sub-10 nm lines and spaces pattern. PMAPOSS-b-PTFEMA can form a vertical oriented lamellar structure on various substrates. [2] Because after the development a mask thickness is higher than the cylinder structure, the vertical oriented lamellar structure has an advantage in high precision pattern transfer process.

In this work, we fabricated sub-10 nm patterns by DSA with lamellar structure high-chi BCP. And we evaluated dry development and pattern transfer to the under-layer by RIE. An extreme optimization of stacked layers and RIE conditions such as gas chemistry and RF power are required to realize the sub-10 nm pattern transfer to a substrate.

Figure 1 (a) shows the post phase separation fabricated by a lamellar structure PMAPOSS-b-PTFEMA. Figure 1 (b) shows the results of dry development, and figure 1 (c) shows pattern transfer to spin-of-carbon (SOC) layer. Figure 2 shows cross-sectional SEM images of Half Pitch (HP) 8 nm lines and spaces pattern fabricated by lamellar structure PMAPOSS-b-PTFEMA.

At the upcoming conference, we will discuss about the details of pattern fabrication of HP sub-10 nm lines and spaces pattern.

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9782-25, Session PS1

## LER improvement for sub-32nm pitch self-aligned quadruple patterning (SAQP) at back end of line (BEOL)

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Critical back end of line (BEOL) Mx patterning at 7nm technology node and beyond requires sub-36nm pitch line/space pattern in order to meet the scaling requirements. This small pitch can be achieved by either extreme ultraviolet (EUV) lithography or 193nm-immersion-lithography based self-aligned quadruple patterning (SAQP). With enormous challenges being faced in production readiness of EUV lithography, SAQP is expected to be the front up approach for Mx grid patterning for most of industry. In contrast to the front end of line (FEOL) fin patterning, which has successfully deployed SAQP approach since 10nm node technology, BEOL Mx SAQP is challenging owing to the required usage of significantly lower temperature budgets for film stack deposition. This has an adverse impact on the material properties of the as-deposited films leading to emergence of several challenges for etch including selectivity, uniformity and roughness.

In this presentation we will highlight those unique etch challenges associated with our BEOL Mx SAQP patterning strategy and summarize our efforts in optimizing the patterning stack, etch chemistries & process steps for meeting the 7nm technology node targets. We will present comparison data on both organic and in-organic mandrel stacks with respect to LER/LWR & CDU. With LER being one of the most critical targets for 7nm BEOL Mx, we will outline our actions for optimization of our stack including resist material, mandrel material, spacer material and others. Finally, we would like to update our progress on achieving the target LER of 1.5 nm for 32nm pitch BEOL SAQP pattern.

9782-26, Session PS1

## Gate patterning challenges of vertically stacked gate-all-around Si nanowire MOSFET devices for 10nm and beyond nodes

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Relentless scaling of advanced MOSFET devices is extremely challenging using non-planar device architectures such as Finfet and nanowire. The top-down fabricated, gate-all-around architecture with a Si nanowire channel is a promising candidate for 10nm and beyond nodes technology generations. The gate-all-around structure enhances the electrostatic control and hence gate length scalability. Nanowire represents the next evolution from Finfet where the gate surrounds the channel. The fabrication of the novel device will introduce many new challenges due to complex topography and geometry characteristics. Fabrication of vertically stacked Si nanowire arrays and gate etch are two of the most challenging steps.

In this work, we will mainly focus on the investigations of gate patterning challenges encountered during etch processes development. A vertically stacked gate-all-around Si nanowire is firstly fabricated on a bulk substrate by using the deep reactive-ion etching process known as the Bosch process. Dummy gate stack including thermally grown gate oxide and poly-silicon gate material will be formed around the stacked nanowire arrays, respectively. The gate patterning process is originated from 14nm Finfet devices, in which ?-Si/SiO2 multilayer is used as an etch mask. Although, the dummy poly gate etch is very similar to Finfet device gate etch, topography effect makes gate etch extremely challenging. On one hand, the vertical gate etch profile with high aspect ratio will be critically required to meet subsequently stringent requirement from metal gate last process. At the same time, no significant damage occurs on the gate oxide for vertically stacked nanowire arrays, or some nanowires may be easily broken with etch processing. On the other hand, enough over etch is needed to clear the gate materials from bulk Si substrate side wall and among different nanowire arrays for vertical and horizontal directions. Consequently, a very high etch selectivity is necessarily required between poly-silicon and gate oxide in order to remove all gate materials.

In this paper, we will discuss some of the approaches that we have investigated to achieve the best etch process to enable an effective gate patterning strategy to meet the requirement of vertically stacked gate-all-around Si nanowire MOSFET devices for 10nm and beyond nodes.

9782-27, Session PS1

## Silicon nitride etching by light ion implantation: a comprehensive study of layer modification and selective removal

Olivier Pollet, Vincent Ah-Leung, Maxime Garcia Barros, Nicolas Posseme, MINATEC (France)

For technology nodes beyond 14nm silicon nitride spacer etching has become a major challenge. Conventional plasma etching techniques based on CHF3/O2 cannot achieve thorough nitride removal on horizontal surfaces without inducing either CD loss or Si/SiGe source/drain recess. This leads to either gate leakage increase or poor raised source/drain epitaxy. An original etching approach has been reported which consists in modifying the silicon nitride through H2 ion implantation by plasma (ICP or CCP) and then selectively removing the modified fraction of the layer thanks to chemical etching (hydrofluoric acid dip, HF) [1]. Layer modification depth is controlled thanks to plasma parameters (bias voltage and process time). This unconventional technique was demonstrated on 14nm FDSOI logic device and showed less than 1nm spacer CD loss, less than 0.6nm SiGe recess which enabled defect-free source/drain epitaxy [1].

To etch silicon nitride in order to build spacers by using this novel process, the modified SiN must be removed selectively to pristine SiN but also to SiO2 (gate hardmask, STI) and Si/SiGe (source/drain). Several removal options were investigated amongst which hydrofluoric acid and NF3/NH3 remote plasma showed efficient modified SiN removal. However with this type of process SiO2 is etched whatever the process conditions used, thereby limiting their application to spacer etching [2].

Based on this study we developed an HF optimized process demonstrating high selectivity to SiO2 and pristine SiN, above 30 in both cases. This optimized HF process involves a post-treatment in order to remove the reacted fraction of the layer.

In this presentation we propose to understand etch mechanisms to remove the modified layer thanks to ATR, MIR and XPS analyses. We will demonstrate that reaction of implanted layer with optimized HF leads to the formation of (NH4)2SiF6 salts which has also been previously reported to form during plasma etching of SiN [3]. Efficiency of this optimized process on patterned wafers will be shown.

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