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7969-01, Session 1

Printability and inspectability of defects on the EUV mask for sub-32-nm half-pitch HVM application

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The availability of defect free masks remains one of the key challenges for inserting extreme ultraviolet lithography (EUVL) into high volume manufacturing (HVM). Among the defects on the final EUV masks, 75 % of those are originated from the blank level. However, commercial state-of-the art inspection tools cannot meet the requirements for HVM. Therefore, accomplishment of defect free masks will depend on the timely development of defect inspection tools which cover both mask-blank and pattern inspections. In this paper, defect printability and inspectability are studied using 2 kinds of EUV mask with programmed pit defects and natural defects, respectively.

First, programmed pit defects on the multilayer are evaluated to set-up the required defect sensitivity of blank inspection tool. Our preliminary results show that programmed pit defects with 28.3nm SEVD (Sphere Equilibrant Volume Dimension, Width : 40.5nm, depth : 3.4nm) could be printable on the resist images on the wafer while those with 17.1nm SEVD (32.3nm, depth : 2.0nm) were captured in the aerial images from SEMATECH-LBNL AIT (Actinic Inspection Tool) in 35nm HP (half pitch) L/S patterns. This means that this value of SEVD should be detected with blank inspection tool for EUV high volume manufacturing.

Second, a full field EUV mask is fabricated to characterize printability and inspectability of various types of natural defects on the final EUV mask. Exposure works are performed using the EUV ADT (Alpha Demo Tool) at CNSE in Albany. After the exposure, both mask and wafers are inspected with mask and wafer inspection tools, respectively. According to the AFM (Atomic Force Microscope) analysis, profiles of natural defects are quite different from those of programmed blank defects. Thus, studies on the natural defects are very essential. Finally this paper will present how to define the defects induced from the mask blank level.

7969-02, Session 1

Modeling the transfer of line-edge roughness from mask to wafer

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Contributions to line-edge roughness (LER) from EUV masks have recently been shown to be an issue of concern for both the accuracy of current resist evaluation tests as well the ultimate LER requirements for the 22-nm production node. More recently, it has been shown that the power spectral density of the mask-induced roughness, is markedly different than that of intrinsic resist roughness and thus potentially serves as a mechanism for distinguishing mask effects from resist effects in experimental results. But the evaluation of stochastic effects in the resist itself demonstrate that such a test would only be viable in cases where the resist effects are completely negligible in terms of their contribution to the total LER compared to the mask effects. On the other hand the results presented here lead us to the surprising conclusion that it is indeed possible for mask contributors to be the dominant source of LER while the spatial characteristics of the LER remain indistinguishable from the fractal characteristics of resist-induced LER.

7969-03, Session 1

EUV secondary electron blur at the 22-nm half-pitch node

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Because of the excitation mechanism in EUV lithography the photo-acid is not expected to be generated at the exact location where the EUV photon is absorbed in resist. This so-called secondary electron blur has thus far proven to be very difficult to access experimentally. This is because the secondary electron blur is expected to be small (<10nm) and because it is difficult to separate from other blur terms such as acid diffusion.

In this paper the Arrhenius behavior of the combined blur parameters upon EUV exposure will be investigated through variation of the PEB temperature. In this way thermally activated parameters that contribute to blur (such as acid/base diffusion) can be separated from non-thermally activated parameters (such as secondary electron blur). The experimental results will be analyzed in detail using resist modeling in order to verify whether the secondary electron blur is a significant contributor to the total blur at the 22nm half pitch node. This approach should allow to experimentally determine (or at least put an upper limit on) the magnitude of secondary electron blur, which is believed to define the ultimate resolution limitation of EUV lithography.

7969-04, Session 2

Development status of EUV resist materials and processing at Selete

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Extreme Ultra-Violet (EUV) lithography is the leading candidate for semiconductor manufacturing of the hp 22-nm technology node and beyond. One of the critical issues facing EUV lithography is resist performance, because of the stringent requirements for resolution limit, sensitivity and line edge roughness. To achieve the targets, Selete have evaluated more than 700 EUV resists (from various resist suppliers) using the small field exposure tool or SFET which is linked with a coater & developer track system under chemically controlled environments.

We previously reported on the lithographic performance of Selete standard resist 4 (SSR4) and improvement of resist process. (1, 2) It was especially discussed how LWR reduction and pattern collapse prevention were achieved through improved resist processes. The aqueous developer solution of tetrabutylammonium hydroxide (TBAH) was found to be most effective in the prevention of pattern collapse of SSR4.

The Selete R&D program covers the evaluation of manufacturability for the EUV lithography process. Here, we have begun a yield analysis for hp 3x nm and 2x nm test chips using EUV1 (Nikon) full field exposure tool.

A higher yield on hp 3x nm test chip was achieved through the application of various resist materials and improvement of resist processes. However, relatively lower yield was observed for on hp 2x nm test chips. (3)

One of the causes for lower yield is insufficient pattern transfer ability. A higher aspect ratio of resist pattern and improvement of dry etching durability of resist materials are viewed as possible solutions.

In this study, we will report on the improvement of resist materials and processes for hp 2x nm evaluations. We will also present the lithographic

performance of our newly resist materials (SSR-X). Furthermore, application of under layer, alternative developer solution and rinse solution will be discussed.

A part of this work is supported by New Energy and Industrial Technology Development Organization (NEDO)

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7969-05, Session 2

Comprehensive EUV lithography model

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As EUV lithography nears pilot-line stage, photolithography modeling becomes increasingly important in order for engineers to build viable, production-worthy processes. In this paper, we present a comprehensive, calibrated lithography model that includes optical effects such as mask shadowing and flare, combined with a stochastic resist model that can predict effects such as line-edge roughness. The model was calibrated to CD versus pitch data. 2D line-end shortening structures are used for verification of the accuracy of the model. We then use this model to investigate several issues critical to EUV: first, we examine the trade-off between LWR and photospeed by changing PAG loading and quencher loading in the photoresist model. Second, we compare the predicted resist contribution to CDU for different line-end shortening test structures as the flare is reduced from 16% (the level in the current alpha tools) to 8% (the level expected in the beta tools).

7969-06, Session 2

Additive-loaded EUV photoresists: performance and the underlying physics

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The incorporation of silica and other nanoparticles into resist systems has been shown to increase image resolution, but the mechanisms and structure-property relationships necessary for optimization have not been characterized.1, 2 Here, we identify mechanisms behind additive induced enhancements in resolution for EUV based copolymers of hydroxystyrene and tert-butyl acrylate (ESCAP resist), and apply this knowledge to the development of multi-functional additives that can lead to substantial performance enhancements.

The incorporation of nanoparticles within amorphous resists can lead to a decrease in photoacid mobility by occupying voids and reducing excess free volume. We propose that substantial improvements in line edge roughness (LER) can be realized through incorporation of additives that exhibit strong, non-covalent, multipoint interactions with the resist chain segments that yield substantial reductions in photoacid diffusion due to a slowdown in the resist chain mobility and reduction in the overall free volume of the as applied resist as shown in Scheme 1. We incorporate chemically protected additives which blend with the protected polymer resist and undergo deprotection along with the polymer resist to generate strongly interacting groups in the exposed regions. This scheme allows for the compatibility of the additive with the polymer before and after deprotection.

Various molecular glasses (MGs) protected with tert-butoxylcarbonylmethyl groups that deprotect to form carboxylic acid groups capable of hydrogen bonding were employed as additives for incorporation in ESCAP resist. While all MGs decrease the dark loss by imparting solubility inhibition as also observed by Ito, Ueda and coworkers,3 our results indicate that MG additives deliver the additional function of reducing photoacid diffusivity, which is important to achieve lower critical dimension (CD). Thus, optimization of the additive molecular structure, size and composition was performed to lower CD and LER. Acid diffusion length measurements using the method of bilayers developed at NIST4 also show differences in the acid diffusion lengths for photoresist blends with different MGs additives. Simultaneously, optimization of the type and loading of PAG and base quencher was also carried out.

The disadvantages of using neat small molecule resists, namely, poor film forming attributes and insufficient glass transition temperatures are offset by the polymeric resist component present in the blend. On the other hand, incorporation of additives allows reductions in dark loss, and more importantly reductions in acid diffusivity to achieve better resolution. Additionally, it is expected that small molecules of appropriate molecular architecture and size should pack well within the polymeric matrix and thus lead to smaller LER.

Optimizations to date have resulted in 25 nm resolution at a large depth of focus (0.5 microns) using SEMATECH EUV micro exposure tool at Albany, which represents a significant performance enhancement relative to the neat resist. We continue to optimize the formulations and processing conditions to achieve even better resolution and LER while maintaining sensitivity.

To understand and characterize the structure-property relationships the photoresist blends were also characterized to correlate their physical properties with their performance. Next, positron annihilation lifetime spectroscopy will be carried out to correlate the photoresist blend performance with reductions in the free volume upon incorporating various MGs.

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7969-07, Session 3

100W 1st generation laser-produced plasma source system for HVM EUV lithography

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Since 2002 we have developed CO2 laser produced Tin plasma EUV source (CO2-Sn-LPP) which is the most promising solution as the 13.5nm high power (> 200W) light source for high volume production extreme ultraviolet lithography (EUVL). Because of its high efficiency, scalability and spatial freedom from plasma, we believe the CO2-Sn-LPP scheme is most promising candidate. One of the technical challenges is the requirement of high average in-band power at the intermediate focus1, together with the cleanness of the plasma chamber. Theoretical2 and experimental3 data have clearly demonstrated the advantage of the combination of a CO2 laser wavelength with Tin plasma to achieve high conversion efficiency from laser pulse energy to EUV in-band energy. High average laser power due to high amplification efficiency and superior beam quality is readily available by a short pulse CO2 laser technology.4 The CO2 drive laser is based on industrial high average power cw CO2 laser modules.Up to now we have reported progress of the each component technology.

From 2009 we have been constructing system demonstration device: ETS -- “Engineering Test Stand” for the purpose of performance demonstration with all of component technologies integrated. In this paper we introduce latest performance of the 1st generation Laser-Produced Plasma source system “ETS” device for EUV lithography is under development. We report latest status of the device which consists of the original concepts (1) CO2 laser driven Sn plasma, (2) Hybrid CO2 laser system that is combination of high speed (>100kHz) short pulse oscillator and industrial cw-CO2, (3) Magnetic mitigation, and (4) Double pulse EUV plasma creation. Maximum power is 104W (100kHz, 1mJ EUV power @ intermediate focus), laser-EUV conversion efficiency is 2.5%, duty cycle is 20% at maximum (table 1). In the background we have steady progress on the CO2 laser produced Tin plasma method for HVM EUV light source, high duty operation of pulsed CO2 laser without any degradation of fine beam quality. Also improved stability of the Tin droplet injector enables continuous plasma creation. Magnetic field collects the injected Tin ions and guides them into a Tin collector. Continuous operation time so far is 3 hours. Debris is efficiently suppressed by pre-pulse plasma formation and magnetic field mitigation system. Long-term performance is now under investigation. Also future plan is updated.

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7969-08, Session 3

Development of spectral purity filter for CO_2 laser-produced plasma (LPP) based on magnetized plasma confinement of absorbing gases

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There is an urgent need to develop spectral filters for infrared absorption that can withstand high heat loads with minimal EUV transmission loss. Reports on spectral measurements of current CO2 laser-produced plasma (LPP) extreme ultraviolet (EUV) sources reveal that the light propagating to the intermediate focus (IF) is dominated by 10.6 μm photons.1 The transmission of this light causes thermal load issues on the masks and optics. A spectral purity filter which uses a confined gas that absorbs the unwanted CO2 laser light is being developed. SF6 gas is of tremendous interest because it absorbs preferentially at 10.6 μm based on its infrared active vibrational mode which coincides with some of the CO2 laser wavelengths. The absorption coefficient of SF6 is documented in literature at some CO2 laser lines.2,3 Below is a table showing the absorption cross section at room temperature reported by Cantrell.4 An optical system has been configured to determine the full extent of the absorptive properties of SF6 at various CO2 laser wavelengths and under various experimental conditions such as very low temperatures while ensuring minimal EUV transmission loss. Of particular interest is the multi-photon absorption in SF6 prior to vibrationally induced fragmentation. In addition, a magnetized hollow cathode arc discharge has being built to measure the SF6 diffusion at different pressures in order to determine the confinement properties of the system. SF6 is inert under normal conditions, but it is expected that the EUV photons will ionize the molecules which potentially poses a concern to optics if allowed to interact with their surfaces. The ultimate goal is a configuration that will allow easy integration into a CO2 LPP source system with the ability to withstand high heat loads with minimal EUV transmission loss and no diffusion of the infrared absorbing gas toward the optics.

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7969-09, Session 3

Cooled EUV collector optics for LPP and DPP sources

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For several years SAGEM has invested in technologies and engineering to develop innovative solutions for collecting optics for LPP and DPP EUV sources. Among the technological challenges for collecting mirrors, thermal control is a very important issue to avoid degradation of reflectivity performance due to the heating of the reflective surface. Sagem proposes solutions based on a metallic mirror with embedded cooling circuits inside the substrate to stabilize the temperature of the mirror during source operation. Results of simulation as well as first technology validations obtained on prototypes will be shown to demonstrate the performance of the cooled mirror design. Another critical performance about the collector is the high quality roughness of the surface for limiting scattering and the reflectivity losses. Thanks to specific polishing process, very performing roughness performances (HSFR) below 2 Angstroms have been achieved on demonstration metallic parts even on high departure asphere. Reflectivity measurements made after coating of these parts will confirm that the obtained polishing quality is compliant with EUV standards. Next developments in EUV collectors will be lastly presented.

7969-10, Session 3

Enabling the 22-nm node via grazing incidence collectors integrated into the DPP source for EUVL HVM

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Media Lario Technologies has adapted its proprietary technology for space applications to successfully develop and manufacture grazing incidence collectors for the XTREME technologies Sn-fueled DPP source, enabling the 22 nm node.

Media Lario Technologies’ grazing incidence collectors have enabled every DPP source delivered by XTREME technologies. We present thermal and optical performance on grazing incidence collectors integrated onto the Sn-fueled DPP source under operating conditions that are representative of the requirements of EUVL scanners for the 27 nm node. The grazing incidence collectors are produced with custom reflective layers that perform within XTREME technologies’ debris mitigation strategy, enabling a 1-year lifetime of the source-collector module. With a point-source collection efficiency greater than 24% and integrated thermal control for an absorbed power of 6 kW, the grazing incidence collector enables the source power roadmap for the 22 nm node and beyond.

Combining the thermal and absorbed power data measured on existing collectors with simulation, we are able to show the feasibility of extending the performance of the current collector to satisfy the scanner throughput roadmap.

7969-11, Session 3

High-brightness LPP source for actinic mask inspection

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EUV actinic mask inspection requires a cost effective, high brightness light source. Adlyte Corporation has developed a reliable, compact and cost-effective EUV source for inspection applications with plans to extend the product for scanner High Volume Manufacturing application. The EUV source will generate high brightness EUV of up to 1 kW/mm2Sr. The EUV target is a high frequency tin droplets combined with an industry proven high power Nd:YAG laser which can deliver up to 1.6 kW of power at short pulse. For extended operational lifetime and with high reliability, the collector integrates two methods to mitigate ionic and neutral debris, and actively manage of the thermal load. Latest operational data will be presented.

7969-12, Session 3

Combined effects of pre-pulsing and target geometry on efficient EUV output from laser-produced plasmas experiments and comparison with modeling

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Laser produced plasmas (LPP) is currently the promising source of an efficient EUV output for advanced lithography. Optimum laser pulse parameters with adjusted wavelength/energy/duration ablating simple planar or spherical tin target provides 2 - 3 % coefficient efficiency (CE) in the laboratory experiments and in agreement with modeling results. Additional effects such as ablation of target with complicated geometry or tin-doped targets including pre-pulsing technique can significantly increase CE. Recent investigations showed that such LPP system improvements allow reducing laser energy loses by decreasing photons transmission (third or more harmonic of Nd:YAG laser) or photons reflection (for CO2 laser). Also optimization of target heating using pre-pulses or ablating low-density and nanoporous tin oxide can improve LLP source by creating efficient plasma plume and as a result increase CE, the most important parameter for EUV sources. Second important challenge in the developing LPP devices is decreasing fast ions and target debris to protect the collecting system and increase its lifetime.

We investigated the combined effects of prepulsing with different parameters and various target geometries on increasing EUV signal and on the energetic ions production. The much higher reflectivity of CO2 laser from a tin target leads to two ways for system optimization using pre-pulses - complicated targets or shorter laser wavelengths for the initial pre-pulse.

We utilized our unique combination of experimental facilities (CMUXE Laboratory) and advanced computer simulation (HEIGHTS package) for detail investigation and optimization of LPP sources with various lasers and target parameters and geometries and optical collection system. Comparisons of experiments/modeling results were discussed and detailed plasma characteristics of optimum LPP sources with different geometries were analyzed.

7969-13, Session 4

Replicated mask surface roughness effects on EUV lithographic patterning and line-edge roughness

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International Technology Roadmap for Semiconductors (ITRS) has set the current limit on LER in resists to be less than 1.2nm (3 LER) at the 20nm half-pitch resolution. Under such constraints, it has been shown that mask contributors to LER play a significant role. For the EUV mask, the phase coherent roughness that propagates from layer to layer, termed replicated surface roughness (RSR), is considered to be significant. Furthermore, modeling studies have shown that this RSR must be limited to 50 picometers to meet current LER targets for the 22 and 16-nm half-pitch lithography nodes [1].

For EUV, this brings into question the suitability of top-surface roughness analysis methods such as Atomic Force Microscopy (AFM) for RSR characterization. Because phase coherent roughness related speckle in the aerial image will contribute to LER, it is crucial to understand the relationships between bottom (substrate) surface roughness, top surface roughness, EUV scattering, and aerial image speckle for developing accurate mask specifications and suitable roughness metrics.

In order to quantify the roughness contributions to speckle, a programmed roughness substrate was synthesized with a number of areas having different roughness magnitudes. The substrate was then multilayer coated. AFM surface maps were collected before and after multilayer deposition. At-wavelength reflectance and total integrated scattering measurements are also completed. The mask was then imaged at-wavelength for the direct characterization of the aerial image speckle using the SEMATECH Berkeley actinic inspection tool (AIT) [2]. Modeling is used to test the effectiveness of the different metrologies in predicting the measured aerial-image speckle. The extent to which the various metrologies can be utilized for specifying tolerable roughness limits on EUV masks is determined.

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7969-14, Session 4

Requirements of electron-beam defect repair process for EUV mask application

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Mask defect repair using electron beam induced processing is one of the most promising technologies for EUV mask fabrication as well as optical mask fabrication. Fundamentally, electron beam induced processing is governed by electron induced reaction with a precursor gas and electron scattering process with a substrate material and gas reaction with a substrate material. Currently, EUV blank mask consisted of Ta-based absorber material and thin Ru-capping layer which protects multi-layer. Also it is known that Ta-based absorber material shows spontaneous reaction with a precursor gas which is XeF2 and Ru-capping layer should be well protected during repair process. In addition, electron scattering with substrate stack might be able to produce unwanted electron reaction where electron beam radiation was not applied. We will discuss some of experimental results which show electron/gas, electron/substrate and gas/substrate reaction during EUV mask repair process and suggest criteria of electron beam induced mask defect repair process to meet defect requirements of EUV mask.

7969-15, Session 4

AIMS EUV: the actinic aerial image review platform for EUV masks

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The EUV mask infrastructure is of key importance for a successful

introduction of EUV lithography into volume production. In particular, the manufacturing of defect free masks is of the essence and requires a printability analysis ("review") of potential defect sites. Based on such a review decisions about the need to repair and judgements about the success of a repair can be taken. For this purpose Carl Zeiss and the SEMATECH EUVL Mask Infrastructure consortium started a development programme for an actinic aerial image metrology system (AIMS) for which the concept study phase is currently ongoing. The AIMS EUV will emulate the aerial image of EUV-lithography scanners at 13.5nm wavelength. Thereby, it generates and measures an enlarged version of the scanner's aerial image emulating the scanner's illumination conditions. Accordingly, the AIMS EUV tool ensures to capture the defect's effect in the real exposure process. In this paper, we will present the key results of the concept study, explain the chosen system concept and discuss the expected system performance.

7969-16, Session 4

SEMATECH's infrastructure for defect metrology and failure analysis to support EUV mask defect reduction program

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Mask blank defects have been one of the top challenges in the commercialization of extreme ultraviolet (EUV) lithography. To determine defect sources and devise mitigation solutions, detailed characterization of defects is critical. However, small defects pose challenges in metrology scale-up. SEMATECH has a comprehensive metrology strategy to address any defect larger than a 20 nm core size to obtain solutions for defect-free EUV mask blanks.

This paper will outline metrology challenges with current defects in EUV mask blanks and metrology issues that arise with increasingly smaller defects. Further, we will illustrate SEMATECH's approach to and existing capabilities for defect metrology, including a state-of-the-art metrology toolset that is required to analyze EUV mask blank defects. This capability includes, but is not limited to, Auger spectroscopy and high resolution transmission electron microscopy (TEM) analysis, which enables SEMATECH to analyze nanoscale defects. The newly established Auger tool at SEMATECH, which can run a standard 6-inch mask blank, is already providing important information about sub-100 nm defects on EUV blanks. The operation on a complete 6-inch mask allows samples to be analyzed without glass cutting, which contaminates the blank and makes sample navigation and determination of defect position difficult. . Recent results show demonstration and identification of defect sources such as small carbon particle down to size of 30 nm. (See Figure 1 for sub 50 nm carbon particle on EUV mask blank). The paper compares the capability and challenges of Auger electron spectroscopy (AES) for EUV metrology. Using AES to characterize defects on EUV substrates is particularly challenging due to the insulating nature of substrate, which causes high charging. The characterization technique and data analysis were enhanced to remove the effects of charging, which poses serious issues for the defect characterization EUV substrates. The AES can also help characterize the multilayers and deposition system to identify elemental constituents and deposition rates within the deposition system.

Complementary to Auger analysis, TEM provides ultimate resolution in the defect imaging of sub-nanometer structures. Crystallinity, elemental, and phase information can be readily collected, providing details about the origins of mask blank defects. Figure 2 represents one of the crystalline Si defects, originating from a Si target, which disrupted a multilayer stack in an EUV mask blank. The high resolution imaging of the core of the defect and of its effect on the multilayer can precisely determine the total phase change at the defect location. Hence, high resolution TEM imaging can provide comprehensive information for simulating the printability of defects and can further aid in determining the critical size of printable defects. SEMATECH's TEM capabilities are enhanced with other analytical electron microscopy techniques including energy dispersive x-ray spectroscopy (EDS) and electron energy loss spectroscopy (EELS) in conventional and scanning TEM (STEM) modes. These methods provide superior analytical power compared to similar techniques in traditional secondary electron microscopy (SEM). Comprehensive characterization results using analytical TEM and STEM methods on EUV mask blank defects will be presented.

7969-17, Session 4

Evaluation of EUV mask defect using blanks inspection, patterned mask inspection, and wafer inspection

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Extreme Ultraviolet Lithography (EUVL) is promising technologies for the fabrication of ULSI devices with 22nm half-pitch (HP) and beyond. Mask plays a key role as an integral part of a lithographic system. For the EUV mask, it is required to exhibit high lithographic performance, such as higher image contrast, smaller shadowing effect caused by oblique illumination, lower thermal expansion of substrate material, better flatness control, etc. Our earlier works on the improving lithographic performance of EUV mask had demonstrated that by thinning down LR-TaBN absorber with EUV light-shield area, the shadowing effect could be reduced without any loss in printability. On the other hand, one of the key challenges is to achieve defect-free masks. There are three main categories of mask defects: phase defects embedded in the multilayered blank, absorber pattern defects generated during mask pattering and particles during blanks/mask fabrication or resulting from mask handling. It is important to identify the root cause of defects in order to realize defect-free masks and it is also necessary to set suitable specifications of mask defects for the production of ULSI devices. Selete has been developing EUV mask infrastructures such as full-field actinic blank inspection tool and 199nm wavelength patterned mask inspection tool in order to support the reduction of EUV mask defect.

In this paper, we evaluate printability of mask blank defects and mask pattern defects exposed by full-field scanner EUV1, using full-field actinic/non-actinic blank inspection tool, 199nm wavelength patterned mask inspection tool and wafer inspection tool. And based on a series of results of natural defect analysis, we clarify the current status of EUV mask defectivity.

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7969-18, Session 5

A new and unique NIST facility for EUV photoresist witness-plate testing

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Before being tested for print quality in scanners, extreme ultraviolet (EUV) photoresists must undergo stringent tests to ensure that they do not contaminate the scanner's optics or environment. Worldwide, there are very few of these witness-plate testing facilities, thus making the tests expensive with long lead times. At the National Institute of Standards and Technology we have designed and constructed a high-throughput beamline on the Synchrotron Ultraviolet Radiation Facility (SURF III) in order to help the resist community meet their contamination testing needs. The set-up allows very high intensity broadband irradiation of the multilayer witness sample and EUV exposure of the resist. A critical benefit of these new conditions is that they allow scaling of the test results to the EUV scanner situation.

The beamline uses broadband radiation of 5 nm to 20 nm collected and

focused by a rhodium-coated toroidal mirror. This configuration provides a peak intensity on the sample of over 50 mW/mm2. The sample is a capped MoSi multilayer, which reflects light onto a second multilayer. From the second mirror the light is reflected to the resist-coated wafer. During exposure the wafer is rotated and translated to ensure uniform illumination over the surface. The system can provide a clearing dose of in-band radiation on a 200 mm wafers in about an hour. Diagnostics in the sample chamber include an ion gauge and a residual gas analyzer to monitor vacuum quality, calibrated photodiodes to measure power on the sample and wafer, and a null-field ellipsometric imaging system to provide a real-time in-situ monitor of contaminant-layer growth. A second branch of the beamline can also make dose-to-clear measurements to ensure proper exposure of the resist.

In our contribution we will describe the design as well as performance metrics such as power and spot size at the sample and wafer. Furthermore, we will present the interesting, new insights obtained by tests on pure gases as well as photoresists.

7969-19, Session 5

Influence of environments on the footprint of particle contamination on EUV mask

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The lifetime of the EUV mask is one of the most important issues for extreme ultraviolet (EUV) lithography. There are many open questions to be solved to keep the mast surface clean and prolong its lifetime. Several types of defects including bumps on and pits in either the multilayer or the mask blank were observed. Those defects might be printable.

For storage of EUV mask different environments can be considered such as high and low vacuum, or air can be considered. Particle contamination can occur from manipulating, loading or unloading, or storing the mask. Particle on the surface is one source of defects. Dedicated cleaning can be performed to remove such particles. On wafer cleaning it has been demonstrated that pits can be formed as a result of megasonic cleaning. Also on mask blanks pits have been observed after removing particles. In this study we show that even if particles are removed still a residue or “footprint” is left behind. Such a footprint may in itself be large enough to become a printable defect.

Particle contamination and particularly the removal using an AFM tip have been studied. This method allows for subsequent inspection of the location from where the particle has been removed and residues have been observed. More specifically we investigate the influence of storage time, humidity, and environment on EUV mask surface by measuring footprint of contaminants and its removal forces in order to understand how EUV mask surface is sensitive to environment.

Silica and PSL (polystyrene latex) particles with diameters below 100 nm were used as model contaminations to be deposited on Si and Ru surfaces, respectively. These samples were aged for 2, 5, and 10 days at 0, 40, and 100% relative humidity (R.H.) in air and N2 environments at room temperature. The changes of particle height under these storage conditions were measured to define the contact area of the particles on the surfaces. The aged particles were pushed away from the surface by using atomic force microscope (AFM) and then the footprints of the particles were measured. Particle removal forces also were measured while the AFM probe pushed away the particles. The effect of particle size on the footprint was also investigated.

When silica and PSL particles were aged on a Si surface at different level of humidity and ageing times, the removal forces for silica particle increased as a function of ageing time and increasing humidity. On the other hand, higher removal forces were measured for PSL which were aged at 0% R.H. compared to those for an aged particle at higher humidity. This result shows that the water meniscus formed at the particle/surface interface for hydrophylic particles might be a source of the higher bonding force for silica and the weaker bonding for PSL. In order to explain this result, residue which left as a footprint after the particle was pushed away was observed. The size and height of residues changed at different storage conditions as shown in Figure 1. These residues might be printed on wafer as defects on the wafer later on.

According to the results, the size of the particle footprint changed under different environment conditions and footprints might induce a killer defect in EUV lithography. This study could help to improve the understanding of particle adhesion on EUV mask and might help to improve mask life time.

7969-20, Session 5

Optics contamination studies in support of high-throughput EUVL tools

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As the new generation of extreme-ultraviolet lithography tools attain higher throughput, it is important to establish the scaling laws required to extend the existing data on optics contamination to regimes of higher intensity, greater pulse-repetition rates and varying bandwidths. The EUV optics contamination program at the synchrotron facility of the National Institute of Standards and Technology (NIST) has ongoing efforts to investigate these scaling laws to improve the utility of our expanding database ranking the contamination risks posed by various species.

We have found that the contamination rates for different species can scale quite differently with intensity. The rates for some species, such as benzene at modest pressures of 2E-8 mbar and below, become largely independent of intensity starting at intensities as low as ≈1 mW/mm2, while the rates for other species, such as tert-butylbenzene even at pressures below 1E-9 mbar, continue to scale approximately linearly with intensity up to the highest attainable 4 mW/mm2. (See Figure 1.) We believe that the observed intensity saturation occurs at intensities such that the total rate of EUV-induced reactions (including cracking which leads to C deposition and photon-stimulated desorption which does not) for a given organic species overwhelm the thermal desorption rates for that species. In this limit every molecule of that species adsorbed onto the optic surface is either cracked or photo-desorbed with an intensity-independent branching ratio. So increasing the intensity further does not increase the contamination rate. We will discuss the applicability of this simple model to recent data acquired using a newly commissioned beamline with intensities up to 50 mW/mm2.

The various programs studying optics contamination around the world utilize different EUV sources, which vary from low-rep-rate pulsed sources to quasi-CW synchrotrons. To connect these various data sets and use them to predict contamination risks under high-volume production conditions, NIST is investigating the dependence of contamination rates on the bandwidth and time structure of the EUV light. Initial results of these studies will be presented and predictive models discussed.

It is also important to utilize and correlate different surface analysis techniques to ensure reliable quantification of carbon deposition rates as well as to improve detection and identification of species from resist outgassing or from the native vacuum environment that might be resistant to carbon cleaning methods. NIST relies primarily on x-ray photoelectron spectroscopy and spectroscopic ellipsometry to characterize the EUV-induced contamination. We will report on the correlation of these two techniques over a wide range of exposure conditions. We will also show results form a new null-field ellipsometric imaging system which provides real time, in situ, high-spatial-resolution imaging of carbon growth with sub-nanometer sensitivity.

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7969-21, Session 5

A simple modeling of carbon contamination on EUV exposure tools based on contamination experiments with synchrotron source

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Contamination control of optics is one of critical issues for EUV lithography. EUV irradiation under an environment with organic or carbon-containing gas compounds causes carbon contamination on mirror surfaces.

In past experiments with relatively high EUV intensity (2~20W/cm2), contaminating rate during EUV irradiation depends on EUV intensity. However, the actual transmittance degradation of optics in EUV1, a full-field EUV exposure tool, is faster than estimated from experimental results if contaminating rate is proportional to intensity. In the existing EUV1, fluorocarbon compounds have been detected as one of residual gasses in the vacuum chamber. We then investigated and compared the contaminating rates of decane (C10H22, one kind of normal hydrocarbons or alkanes) and perfluorohexane (C6F14, one kind of normal fluorocarbones or fluoroalkanes). Their contamination growth behavior was quite different. Decane's contaminating rate increased proportionally with EUV intensity, showing a clear dependency on EUV intensity. However, perfluorohexane's contaminating rate was almost constant against EUV intensity, showing a poor dependency on EUV intensity, and was larger than decane's contaminating rate.

We then investigated also at much lower EUV intensity of several mW/cm2, similar to that in the illumination optics in EUV1. Perfluorohexane's contaminating rate was almost constant at EUV intensity down to ~10 mW/cm2. Apparently perfluorohexane's contaminating rate was much larger than decane's contaminating rate in the range of EUV intensity around ~10 mW/cm2. A lower EUV intensity gives a higher contaminating rate per dose. These results qualitatively coincide with the degradation of transmittance due to carbon contamination observed in EUV1.

To explain the behavior, we assumed a simple model: contamination reaction occurs when photons are supplied onto contaminants which are supplied and adsorbed on mirrors, and the lesser of their supplying rates determines contaminating rate. At a lower EUV intensity, since contaminants are sufficiently supplied, photon supply determines contaminating rate. If EUV intensity is low enough, contaminating rate of any contaminants will be proportional to EUV intensity up to an intensity where supplying rates of photons and contaminants balance, taking into account a reaction probability or a quantum yield which means how many molecules one photon can make react. Under such a condition, contaminating rate will not change even if contaminant partial pressure varies as far as contaminants are sufficiently supplied, and surplus contaminant molecules will be desorbed after mean stay time. On the other hand, at a higher EUV intensity, since photons are sufficiently supplied, contaminant supply determines contaminating rate which is independent of EUV intensity and depends on contaminant's partial pressure.

We applied this model to an existing EUV1. The transmittance degradation history agreed well with the calculation based on this model.

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7969-22, Session 5

Cleaning of carbon contamination on EUV masks and optics

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Contamination of projection optics and the mask in EUV exposure tool is still a key issue on keeping productivity. The intense illumination in high volume manufacturing machine (HVM) may affect on not only the deposition rate but also the characteristics of the contamination film. We found that once carbon contamination film is deposited, it will be transformed into more carbon-rich and rigid substance, gradually under continuous EUV irradiation. In the HVM, this effect may be notable. On the other hand, we studied the coverage of carbon contamination on patterned mask. The results from coverage evaluation show that carbon contamination on the patterned mask is not uniform and could not be cancelled by an increasing dose.

Thus we have developed and evaluated cleaning techniques so far. Here we present comprehensive evaluation results for conventional and alternative carbon contamination cleaning techniques, for example, sulfuric peroxide mixture (SPM) cleaning, UV/ozone cleaning, hydrogen (H)-radical cleaning, novel alkene gas assist pure-ozone cleaning .

At first, we evaluated the removal rates of carbon contamination. Figure 1 shows an example of removal rate evaluation. The sample is rather rigid electron-beam chemical vapor deposited carbon patches. The thicknesses of the patches are measured with an atomic force microscope. The figure shows that the patches are removed by the rate of 90 nm/min with pure-ozone cleaning. This rate is markedly faster than other cleaning techniques. As other assessment items, the damages of the masks are particularly analyzed. The cleaning residue and accumulative degradation with multiple cleaning is also examined. In addition, we examined the effect of silicon on cleaning process using EUV deposited contamination and sputter-deposited silicon doped carbon films because it is often reported that the EUV deposited carbon contamination contains silicon.

The results are summarized as below:

1. SPM removes weakly-bound contamination but it seems hard to be applied to rigid carbon film.

2. Both of UV/ozone and H-radical removes carbon film by the rate of few nm/min.

3. Alkene gas assisted pure-ozone cleaning removes rigid carbon film by the rate of a hundred nm/min.

4. All cleaning techniques evaluated here is safe for silicon capping layer with native oxide.

5. It needs some tuning for ozone-based two cleaning techniques to apply ruthenium capping layer.

6. Silicon containing decelerates cleaning rate dramatically but somewhat better for H-radical cleaning.

In the conference, putting together these results, we will show the bases for application of above mentioned cleaning techniques from practical viewpoint.

7969-23, Session 6

Development of EUV lithography tools in Nikon

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Extreme ultraviolet (EUV) lithography is the ultimate lithography technology for semiconductor- device manufacturing after ArF immersion lithography. In the early 1990s we have demonstrated high resolution of EUV lithography down to 50nmL/S using a synchrotron light source at SORTEC and Schwarzschild optics. Since then, we have continuously improved fundamental technologies for EUV lithography such as multilayer-mirror coatings, polishing and metrology of aspheric mirrors. Based on these technologies, EUV exposure tools equipped with full-field projection optics with numerical aperture (NA) of 0.25 were developed. The most important unit of exposure tools is projection optics, in which the wavefront error of 0.4nmRMS and the flare of 6% were achieved. EUV1 is now used by Selete and the other customers for the development of EUV lithography process integration of hp 3x nm-node and hp 2x nm-node semiconductor devices.

Contamination is one of the big issues for EUV lithography. As for EUV1, we faced rapid degradation of transmittance of illumination optics due to the serious carbon contamination at the beginning. In order to understand the mechanism of contamination growth, exposure experiments using a synchrotron source and modeling study of the contamination growth have been conducted. Using these results in-situ mitigation system of EUV1 was optimized. After that, the carbon contamination growth on optics has been completely suppressed. In the other hand, oxidation of optics is a potential issue for HVM EUV exposure tools, because the intensity of EUV radiation on the mirror surface is much higher than EUV1. To solve this issue, new capping layer materials, which have high durability to exposure induced oxidation and protect multilayer mirrors, have been developed.

At the beginning, our target insertion timing of EUV lithography was hp 32 node. However, double patterning technology of ArF immersion becomes in practical use. It may possibly cover hp 22nm node. Though EUV lithography with NA of 0.25 can cover hp 22nm node, higher NA is required to cover next generation. For HVM EUV exposure tools NA of projection optics will be increased. Optical design of projection optics with NA of 0.35 has already been completed. Now further increase of NA is under investigation. In parallel to the optical design, aspheric mirror polishing, metrology and multilayer coating technologies applicable for the manufacturing of high-NA projection optics are continuously under development.

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7969-24, Session 6

Resolution capability of SFET with slit and dipole illumination

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Extreme-ultraviolet lithography (EUVL) is a promising candidate for the fabrication of ULSI devices with a half pitch (hp) of 22 nm and beyond. Double-patterning technology is another candidate for the hp 22-nm node, but it is difficult to use for the hp 16-nm node. We installed the EUV small-field exposure tool (SFET) in 2007 to facilitate the development of EUV resists and EUV masks. Since the SFET has a high numerical aperture (NA = 0.3) and low aberration & flare, it should be able to resolve fine line-and-space (L/S) patterns for the hp 22-nm & 16-nm nodes. In this study, we evaluated the resolution capability of the SFET using two types of off-axis illumination, namely, x-slit & x-dipole.

The EUV light source of the SFET is Xe-fueled discharge-produced plasma. There are 6 shells in the collector mirror, and the maximum sigma of the illumination optics is 0.7. The wafer size is 300 mm. The stability of the resist process is excellent because an in-line wafer track is connected to the SFET. The wavefront error measured with an interferometer was 0.76 nm RMS (Annular Zernike 5-37) at the center of the field. The measured flare was 11%. The synchronization error between mask and wafer stage was less than +/- 1 nm. Dose uniformity in the exposure field (600 um x 200 um) is about ±10-15%; but it is about ±3-5% in the central area of the field (200 um x 200 um). For resist evaluation, we usually use this central area. Because of this good dose uniformity, it is easy to observe cross sections of printed resist patterns.

Figure 1 shows the calculated image contrast of L/S patterns for x-slit and x-dipole illumination. The simulations took aberration and flare into account. X-slit illumination (sigma = 0.3/0.5) was designed for hp 22-nm L/S patterns. It provides a high image contrast for pattern sizes of hp 20-30 nm. X-dipole illumination (sigma = 0.5/0.7) was designed for hp 16-nm L/S patterns. The contrast is quite high for pattern sizes of hp 16-23 nm. However, it is quite low for pattern sizes of hp 26-55 nm because of the effect of central obscuration.

To verify these simulation results, we performed exposure experiments using SMR569 resist (40-nm thick). The EUV mask had fine L/S patterns with sizes down to 75 nm, which corresponds to 15 nm on wafer. Figure 2 shows an SEM image of 16-nm L/S patterns printed with x-dipole illumination; the modulation is clear. We think that the SFET has the capability of resolving hp 16-nm L/S patterns with x-dipole illumination.

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7969-25, Session 6

The SEMATECH Berkeley MET: extending EUV learning down to 16-nm half pitch

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As experience with EUV alpha tools grow and delivery of pre-production tools approaches, the emphasis for microfield exposure tools is quickly moving towards 16-nm half pitch and below. This trend is clearly evident in the research activities on the SEMATECH Berkeley MET tool. At a numerical aperture (NA) of 0.3, however, conventional illumination limits us to a resolution of approximately 22 nm. Breaking this limit requires the use of aggressive resolution enhancement techniques such as dipole illumination and phase shift masks. The fabrication of strong phase shift masks for EUV, however, is not a simple process. To get around this limitation we have employed a method we refer to as pseudo phase-shift mask. Using this process, the Berkeley MET can in principle attain 12-nm half pitch resolution. We note however, that in this mode the system acts very much as an interference lithography tool limiting its utility for general purpose EUV learning. We use the pseudo phase shift method to test the ultimate resolution limit of a variety of resists with the best performing resist supporting on the order of 16-nm lines and spaces.

In addition to the resolution limits, we also summarize a variety of research activities on the SEMATECH Berkeley MET, including the effect of repetitive mask cleaning on mask-induced LER, the effects of out of band radiation on printing results, and the correlation between resist resolution limits and LER. The latter is particularly important since it suggests that our current LER limits may in fact be primarily driven by resolution limits.

Finally, we will turn the discussion to the future detailing plans for the development of the SEMATECH Berkeley 0.5-NA MET. This tool would address the needs of generalized EUV development at the 16-nm node and beyond. The tool will support an ultimate resolution of 8 nm half-pitch and generalized printing using conventional illumination down to 12 nm half pitch. As with the current MET, the new tool will support a fully programmable pupil fill. To be constructed on a newly optimized branch at the Advanced Light Source synchrotron facility, the system will also support improved optical throughput.

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7969-26, Session 6

Investigation of EUV tapeout flow issues, requirements, and options for volume manufacturing

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Although technical issues remain to be resolved, EUV lithography is now a serious contender for critical layer patterning of upcoming 2X node memory and 15nm Logic technologies in manufacturing. If improvements continue in defectivity, throughput and resolution, then EUV lithography appears that it will be the most extendable and the cost-effective manufacturing lithography solution for sub-78nm pitch complex patterns. EUV lithography will be able to provide a significant relaxation in lithographic K1 factor (and a corresponding simplification of process complexity) vs. existing 193nm lithography. The increased K1 factor will result in some complexity reduction for mask synthesis flow elements (including illumination source shape optimization, design pre-processing, RET, OPC and OPC verification). However, EUV does add well known addidtional complexities and issues to mask synthesis flows such as across-lens shadowing variation, across reticle flare variation, new proximity effects to be modeled, significant increase in pre-OPC and fracture file size, etc.

In this paper, we investigate the expected EUV-specific issues and new requirements for a production tapeout mask synthesis flow. The production EUV issues and new requirements are in the categories of additional physical effects to be corrected for; additional automation or flow steps needed; and increase in file size at different parts in the flow. For example, OASIS file sizes after OPC of greater than one TeraByte can be expected to be common, which will place significant stress on post-processing methods, OPC verification, mask data fracture, file read-in/read-out, data transfer between sites (e.g., to the maskshop), etc. With current methods and procedures, it is clear that the hours/days needed to complete EUV mask synthesis mask data flows would significantly increase if steps are not taken to make efficiency improvements. Therefore, we also analyze different options for reducing or alleviating the EUV specific issues mentioned above and the expected cost/benefit tradeoffs associated with these options. The options include understanding the accuracy vs. run-time benefit of different rule-based and model-based approaches for several correction issues; predicting the implications and improvements expected with different flow automation options; and estimating possible productivity improvements with different flow parallelization choices. Optimal combinations of options and accuracy/effort/runtime results can be seen to enable EUV lithography tapeout flows to achieve equal or better total time when compared to current 193nm lithography tapeout flow times.

7969-27, Session 6

EUV flare and proximity modeling and model-based correction

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The introduction of EUV lithography into the semiconductor fabrication process will enable a continuation of Moore's law below the 22nm technology node. EUV lithography will, however, introduce new and unwanted sources of patterning distortions which must be accurately modeled and corrected on the reticle. Flare caused by scattered light in the projection optics is expected to result in several nanometers of on-wafer dimensional variation, if left uncorrected. Previous work by the authors has focused on combinations of model-based and rules-based approaches to modeling and correction of flare in EUV lithography. Current work to be presented here focuses on the development of an all model-based approach to compensation of both flare and proximity effects in EUV lithography. The advantages of such an approach in terms of both model and OPC accuracy will be discussed. In addition, the authors will discuss the benefits and tradeoffs associated with hybrid OPC approaches which mix both rules-based and model-based OPC. The tradeoffs to be explored include correction time, accuracy, and data volume.

7969-28, Session 6

EUV OPC for the 15-nm node

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For the logic generations of the 15 nm node and beyond, the printing of pitches at 64,nm and below are needed. For EUV lithography to replace ArF-based multi-exposure techniques, it is required to print these patterns in a single exposure process. The k_1 factor is roughly 0.6 for 64 nm pitch at an NA of 0.25, and k_1~0.52 for 56 nm pitch. These k_1 numbers are of the same order at which model based OPC was introduced in KrF and ArF lithography a decade or so earlier. While we have done earlier work that used model-based OPC for the 22 nm node test devices using EUV [1], we used a simple threshold model without further resist model calibration. For 64 nm pitch at an NA of 0.25, the OPC becomes important, and at 56 nm pitch it becomes critical. For 15 nm node lithography, we resort to a full resist model calibration using tools that were adapted from conventional optical lithography. We use a straight shrink 22 nm test layout to assess post-OPC printability of a metal layer at pitches of the 15 nm logic generation and use this information to correct 15 nm test layouts.

In this paper, we discuss the work flow from drawn design to the finished mask, with emphasis on the model-based optical proximity correction.

7969-29, Session 7

Phase-defect printability and actinic dark-field mask-blank inspection capability analyses

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Detecting printable phase defect on an EUVL (Extreme Ultraviolet Lithography) mask blank is important for the development of practical defect-free EUVL mask fabrication processes. We have developed an actinic EUVL mask blank inspection tool which has a potential of detecting all critical phase defects on EUVL mask blank. So far, we demonstrated >99% capture rate of detecting programmed phase defects of 60 nm in width and 1.5 nm in height in spite of a large pixel size of 500 nm. Small sized native defects down to 20 nm in FWHM at multilayer surface were also successfully detected with this tool.

Understanding the impact of phase defects on the printed pattern size variation is essential to clarify the critical defect. To evaluate a phase defect printability, a new test mask which includes absorber line patterns and programmed phase defects with finer sizes (as small as 30 nm) compared to those presented in the previous work (minimum size: 60 nm) was prepared. The absorber L/S patterns with half pitch of 128 nm - 96 nm on the mask were exposed using an EUV exposure tool (EUV1), and the multilayer defect printability for varying location of the multilayer phase defects relative to the absorber line patterns was evaluated. Simulation of projected images was also conducted using FDTD (Finite Difference Time Domain) method. Furthermore, the effects of multilayered internal structure on the inspection signal and on the defect printability were analyzed. This analysis was performed because in the previous work the small sized native defect signals were found to be much larger than the signals estimated by surface defect volume measured by AFM. It is found from the simulation that some internal structure plays a key role in the impact on projected patterns on wafer.

On the other hand, the actinic inspection tool at Selete was upgraded by replacing the CCD camera with an improved TDI (Time Delay and Integration) operation and by introducing a noise reduction algorithm. To confirm inspection capability, the new test mask was used for inspecting small sized programmed phase defect arrays formed on the clear area on

the mask. In addition, dark-field inspection signals as functions of FWHM and height of the phase defect were simulated using FDTD method. Using these results, the relationship between inspection sensitivity limits, pixel size, and illumination energy was analyzed. Through these signal analyses, extendibility of the current actinic dark-field inspection to beyond 22 nm hp will also be discussed.

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7969-30, Session 7

EUV masks under exposure: practical considerations

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Extreme Ultraviolet Lithography (EUVL) is slowly emerging as a manufacturing solution to enable the semiconductor roadmap. Printing features on wafers using EUV exposure tools and EUV masks has become routine. Manufacturing considerations and concerns exist, but remain largely unquantified. This paper focuses on the practical side of EUV mask metrology and use. Mask metrics such as film thickness, material properties, feature profile, critical feature size, line edge/width roughness (LER/LWR), image placement (IP) and defect levels will be measured and monitored on the mask. A key enabling technology is scatterometry. This technique is fast, non-destructive and provides a wealth of film, CD and profile information to supplement the more traditional metrology methods like CDSEM and cross-sectional TEM.

After completing a suite of pre-measurements, the mask will be exposed on an ASML ADT EUV exposure system and the printing quality assessed on wafer. Lithographic metrics to be evaluated include defect levels, contrast, mask error enhancement factor (MEEF), wafer LER/LWR and depth of focus. The change in both mask and wafer metrics as the mask is exposed and cleaned will be studied to identify mask lifetime limiters. These limiters in turn define mask requirements and underscore gaps in development. This EUV-specific effort is required to determine how close EUVL masks are to meeting manufacturing requirements and whether there are areas of development that require additional focus from the industry.

7969-31, Session 7

Contamination removal, inspection, and pattern repair on EUVL reticles

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In order for EUVL to work it is necessary to have defect free reticles and the reticles should stay defect free during their life time. Defects can be categorized as particles or as molecular. It has been known that the EUV photons cause carbon growth on the reticle. This occurs on the absorber and on the reflective parts of the reticle. The carbon growth on the reflective parts causes a change in CD due to the sidewalls being covered with absorbing carbon [1]. We have shown in earlier investigations that the Shielded Microwave Induced Remote Plasma (SMIRP) process doesn't impose damage to capped multilayer mirrors and that carbon removal rate is relatively high [2].

In our present research we focused on the carbon removal rate of our SMIRP process inside the trenches and on top of the absorber of a EUVL dummy mask. The dummy mask consists of a LTEM substrate with a Si top layer, the mask pattern consists of a SiO2 buffer layer and TaN absorber. We used the Carl Zeiss Helium Ion Microscope (HIM) in our facility for the imaging of the lines and spaces of the dummy mask and for carbon deposition on the absorber and inside the trenches. After exposure to the plasma the mask was again imaged using the HIM to check the carbon removal and XPS analysis was performed to investigate possible damage to the absorber due to the exposure of the plasma.

Next to carbon contamination particles on the reticle contribute to possible risks of yield and throughput. Within our research we also investigated the removal rate of organic particles on the reticle with our SMIRP process. For this research we deposited PSL spheres on the dummy reticle and exposed the reticle to the plasma. After exposure the reticle was imaged with the HIM and the removal efficiency was determined.

As a final step the reticle was imaged in the HIM and the ion beam was used to etch away a part of the absorber. This in order to mimic a potential reparation scheme for EUVL reticles. During etching carbon is deposited and the carbon is removed with the plasma process. Finally the reticle is imaged to check the results of the etching process and XPS analysis is performed to check for possible damage to the underlying Si cap layer.

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2. N.B. Koster et al, "Shielded plasma for cleaning of EUV mirrors", EUVL symposium 2008, Lake Tahoe, http://www.sematech.org/meetings/archives/litho/8285/pres/CP-03-Koster.pdf

7969-32, Session 7

Feasibility of EUVL thin absorber mask for sub-32-nm half-pitch patterning

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EUV lithography is the leading candidate for sub-32nm half-pitch device manufacturing. EUV Pre-Production Tool (PPT) is expected to be available at the end of 2010. As EUVL era comes closer, EUVL infrastructure has to get mature including EUVL mask stack.

To reduce CD error by mask shadowing effect, thin mask stack has been considered. We presented that EUVL mask with 58nm absorber height shows same printing performance with conventional EUVL mask with 80nm absorber height. CD error and pattern damage at the shot edges due to light leakage from the neighboring fields was also demonstrated in our previous work.

In this paper, optimal mask stack which shows lower H-V CD bias than conventional structure using 70-nm-thick absorber is proposed. To find minimized absorber height for sub-32nm pattering experimentally, printing result of conventional mask and thin mask stack with 1:1 L/S and island patterns will be compared.

Further-on, we demonstrate the printing result of the reticle which is designed to minimize CD error at the shot edges due to OD effect by reducing reflectivity from the absorber.

All the wafers are exposed at ASML Pre-Production Tool, and S-litho EUV is used for simulation.

7969-33, Session 7

Current status of EUV mask blanks and LTEM substrates defectivity and cleaning of blanks exposed in EUV ADT

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The defectivity of EUV mask blanks remains one of the key challenges in EUV lithography. Mask blank defects are a combination of defects or particles added on the substrate, added during MoSi multilayer deposition, and during handling.

A recent upgrade to the Lasertec M7360 at SEMATECH has enabled us to detect new defects (sub-30 nm SEVD) on the substrate that were not previously detectable. In this paper, we report our recent investigation

of defects on low thermal expansion material (LTEM) substrates and their creation and removal. Data obtained with atomic force microscope (AFM) imaging of defect topography, scanning electron microscope/ energy-dispersive spectroscopy (SEM/EDS), and Auger characterization of defect composition will be presented.

Cleaning of particles added by handling in a clean room environment with an EUV alpha demo exposure tool (ADT) with and without static EUV exposure will be discussed. . Particle contamination on the backside of EUV masks can impact overlay or focus during exposure. We have developed cleaning processes capable of removing backside defects without contaminating the front side of the masks. Backside defects will be characterized by AFM and SEM/EDS, and their topography and composition will be presented.

Finally, we will present our latest results on the effect of storing EUV mask blanks and a method of protecting EUV masks during storage and handling.

7969-34, Session 7

An EUV Fresnel zoneplate mask-imaging microscope for lithography generations reaching 8 nm

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We present the potential capabilities of a low-cost, next-generation EUV mask-imaging microscope, based on the proven optical principle of the SEMATECH Berkeley Actinic Inspection Tool (AIT), but surpassing it in every performance metric. The new tool design would enable research on multiple generations of EUV lithography technology, down to 8 nm or beyond, reaching to the year 2025's design rules.

Owing to the wavelength-specific reflective properties of EUV reticles, imaging with EUV light is the only faithful way to understand the physical response of defects, repairs, and pattern optical proximity corrections. The wavelength-specific properties limit the effectiveness of all non-EUV inspection technologies, and the differences between EUV and non-EUV measurement technologies are likely to increase in future nodes. Therefore, the prolonged unavailability of an EUV microscopy tool could hamstring the commercialization of EUV lithography, and impede research into future nodes.

As a high-magnification all-EUV Fresnel zoneplate microscope, the AIT has been in the vanguard of high-resolution EUV mask imaging for several years. The AIT's measurement of mask architectures, blank and pattern defect imaging, defect smoothing and printability, and recently, direct, quantitative aerial image phase measurement, has expanded our collective understanding of EUV masks and shaped the course of current mask development. A new tool could greatly surpass the capabilities of the AIT by overcoming many of its current limitations.

Our studies show that in a new system design, the photon efficiency can be improved by 200x by streamlining the illuminator (removing two mirrors) and reengineering the nanofabricated zoneplate structure. Combined with an xyz mask stage and vibration isolation for nm-scale stability, the system throughput could be increased relative to the AIT, from two to ten through-focus measurement series per hour, with 2x higher signal-to-noise ratio and improved illumination uniformity. A lossless, custom-coherence illuminator, implemented with scanning mirrors, can mimic arbitrary, future steppers and prototypes. The illuminator design can accommodate an adjustable angle of illumination from 6 to 9° enabling 4x-NA values up to 0.625. An array of zoneplate lenses, similar to the current AIT, gives the flexibility to implement various discrete NA values, with a low-magnification mode for rapid pattern navigation.

We will present detailed analysis of the NA and focal length dependence of the imaging field of view, showing that Strehl ratios above 0.95 and CD uniformity measurements with 3 sigma values in the 2-6 nm range are possible across a circular, aberration-corrected sweet-spot several microns diameter. Relative to high-magnification reflective lenses, zoneplates are simple to use and align, and they can be produced inexpensively, with diffraction-limited quality and demonstrated flare below 3%. Despite narrow illumination bandwidth requirements, a zoneplate-based system could be used with emerging coherent EUV sources, with some design trade-offs.

We believe that an EUV aerial image microscope system such as this could be brought online in 2012, well in advance of commercial tool availability, and would be ready for advanced research on future EUV lithography generations.

7969-35, Session 8

Understanding EUV resist dissolution characteristics and its impact to RLS limitations

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Over the past decade, significant efforts to further progress the insertion of Extreme Ultraviolet (EUV) lithography have generally resulted in EUV entering development and pre-production phases. Given that further work is still needed to bring EUV technology to a manufacturing phase, lithographers explore potential solutions as well as research to gain fundamental understanding of the issues pertaining to resolution, line-width roughness and sensitivity (RLS). The RLS trade-offs continue to be a significant topic for exploration in EUV lithography.

In this work we present insights into RLS limitations by combining experimental data mining and resist modeling and simulation techniques with a development rate monitor (DRM). A DRM provides experimentally-determined dissolution characteristics for a given resist process and potentially be used to produce a more accurate model description of the process. This work presents experimentally-determined dissolution characteristics for ultra-thin EUV resist films as a function of material type and developer conditions and their impact to RLS trade-offs. Resist models are created with DRM data for its dissolution characteristics and used in subsequent simulations to gain fundamental understanding of EUV lithographic performance. In addition to typical lithographic quality metrics (exposure latitude, DOF), the interaction of resist properties (ie, de-protection kinetics and dissolution) with processing techniques are also discussed. Finally, a description of the RLS limitations with respect to resist properties and process conditions is discussed.

7969-36, Session 8

Impact of polymerization process on LWR of an EUV resist

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Line Width Roughness (LWR) is critical to 193 and EUV lithographic processing. Several approaches have been used to minimize LWR in advanced resists. Various polymer and matrix properties, such as polymer molecular volume and free volume fraction [1], polymer dissolution and the impact of activation energy of the de-protection reaction [2], and the distribution of small molecules in the polymer matrix [3] have been shown to influence the functional behavior of the resist. The interdependence of resolution, LWR, and sensitivity (photo speed), as shown in Figure 1, is generally acknowledged in ArF and EUV lithography. Thus, optimization of any one property may lead to limitations among the other two in this RLS trade-off. EUV photo resists have achieved sub-30nm resolution in part by limiting photo acid diffusion by means of

tethering PAG molecules to the polymer backbone. The concentration and distribution of tethered PAG within any single polymer chain is expected to have a significant impact on LWR. We have developed polymerization methods to improve the incorporation and homogeneity of monomers, including PAG monomer, for an EUV resist polymer. Further, we report on the correlation between an improved polymerization process with respect to polymer homogeneity, swelling of the partially exposed film, and improved LWR, as shown in Figure 2. Additionally, LWR improvement was achieved without sacrificing resist photo speed and resolution.

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2.J. Foucher, A. Pikon, C. Andes, J. Thackeray, “ Impact of Acid Diffusion Length on Resist LER and LWR measured by CD-AFM and CD-SEM,” Proc. SPIE 6518, 65181Q-651812Q (2007).

3.D. van Steenwinckel, J. Lammers, T. Koehler, R.L. Brainard, P. Trefonas, “Resist effects at small pitches,” J. Vac. Sci. Technol. B 24(1) pp.316-320 (2006).

7969-37, Session 8

Line-width roughness control and pattern collapse solutions for EUV patterning

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Line width roughness (LWR) control is a critical issue in extreme ultraviolet lithography (EUVL). The difficulty of controlling LWR and the need to minimize it have grown as the sensitivity of materials and resolution in the resist patterning process have improved. Another critical feature that has become difficult to control in EUVL and 22 nm half-pitch systems is pattern collapse. The increase of aspect ratio that comes from further scaling promotes the onset of pattern collapse. Both pattern collapse and LWR are easily observed in EUVL and leading-edge ArF immersion lithography.

This paper will demonstrate recent gains in LWR control using track-based processes, etch-based improvements, and the results of combined techniques in leading EUV films. Also the use of a newly developed EUV-specific FIRM rinse chemistry to reduce pattern collapse will be discussed along with future development activities and industry requirements for both LWR and pattern collapse.

7969-38, Session 9

Out-of-band radiation effects on resist patterning

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The extreme ultraviolet lithography (EUVL) resists are derived from existing molecular structures that were developed for deep ultraviolet/ ultraviolet (DUV/UV) lithography. Some of these resists that are currently being utilized for EUV patterning studies have been shown to be many times more sensitive to specific wavelengths in the 150-300nm DUV/UV region as compared to the sensitivity to the EUVL exposure wavelength of 13.5nm [1,2]. This is of significant concern since the plasma based EUV light sources are known to produce quantifiable emission in this region along with the required source bandwidth. Moreover, a part of these extra out_of_band (OOB) emissions from the source is expected to reach the wafer level resulting in the unwanted background exposure of the resists (flare) causing reduced image contrast in patterning.

Our previous works estimated the expected OOB flare contribution at the wafer level assuming that there is a given amount of OOB at the collector focus [1]. We found that the OOB effects are wavelength, resist and pattern dependent. Flare tests from the alpha demo tool, which uses a plasma EUV source finds the flare contribution from out_of _band (OOB) light at the wafer level to be between 3-4% of the EUV light [3].

In this paper, patterning results with rigorous and complete experimental evaluation of multiple resists using the SEMATECH Berkeley 0.3-NA MET and controlled OOB radiation is presented. Performances above the resolution limit and at the resolution limits are presented. The results show an impact on LER and on process performance after the OOB exposures. Figure 1 and 2 give examples of imaging completed. Figure 1 shows that the LER (24nm half-pitch) is worse for a resist after OOB exposures, and figure 2 shows results for another resist where LER (24nm half-pitch) and resolution to be better after OOB exposures. Repeat measurements were completed for reproducibility of these results on all resists evaluated.

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2.Roberts, J. M. Bristol, R. L., Younkin, T. R., Fedynyshyn, T. H., Astolfi, D. K., and Cabral, A., “Sensitivity of EUV resists to out-of-band radiation,” Proc. SPIE 7273, 72731W (2009).

3.Flare evaluation of ASML alpha demo tool, Hiroyuki Mizuno, Gregory McIntyre, Chiew-seng Koay, Martin Burkhardt, Bruno La Fontaine, and Obert Wood, Proc. SPIE 7271, 72710U (2009.

7969-39, Session 9

Directly patterned inorganic hardmask for EUV lithography

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Inpria is developing a directly patternable, inorganic hardmask platform for EUV lithography. The approach is based on photosensitive metal oxide sulfate films deposited from aqueous solutions. The films are atomically smooth, dense, and amorphous, providing the basis for high-fidelity patterning. For example, we have recently described a resolution of 10 nm half-pitch and LWR of 1.6 nm at 30 nm half-pitch via electron-beam lithography(1). In initial exposures on the LBNL EUV MET(2), sub -20 nm half-pitch resolution was readily demonstrated. Recent improvements in patterning performance will be presented. We demonstrate that the high EUV absorbance of the films and the efficient exposure chemistry, provide a path to the sensitivity required for commercial introduction of EUVL. In addition, because the exposure process does not rely on chemical amplification, especially low resist blur is observed. By using the contact-hole blur metric(3) a value of < 8 nm (the lower bound of the metric) has been realized. This feature is apparent from the 2-D image fidelity, low LWR, and high ultimate resolution, cf., Fig. 1. We also note that ultra-thin (20 nm) imaging layers can be employed since film integrity is readily retained at these thicknesses and the material itself performs as a very highly selective etch mask. Pattern collapse is thereby mitigated in the system.

(1) Telecky et al, EIPBN 2010

(2) Naulleau et al, SPIE 2010

(3) Anderson et al, SPIE 2008

7969-40, Session 9

Novel resolution enhancement layer for EUVL

H. Kim, H. Na, C. Park, C. Park, S. Kim, C. Koh, K. S. Mayya, I. Kim, H. Cho, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

EUV resists have been developed to be able to print sub-30nm L/S features with EUV alpha DEMO tool (ADT) having 0.25NA. However, a lithographic performance of EUV resist is not comparable to that of DUV resist. At same process constant (k1), the imaging capability of EUV resist is poor than that of DUV resists. Out of band radiation (OOB) is regarded as one of the sources which aggravate imaging quality of EUV resist. Although the exact spectrum of out of radiation is not open, LASER produced plasma (LPP) type source and discharge produced plasma (DPP) type source is believed to have the OOB radiation. Therefore to improve pattern fidelity and LWR of EUV resist, the mitigation of OOB radiation impact is required. New material which can mitigate the OOB radiation impact is developed. This material is applied as an additional layer on a conventional EUV resist film. It shows no intermixing. Process window is not changed by applying this layer. The filtering ability of OOB radiation is explored. Furthermore the change of OOB radiation impact is compared and will be discussed in this paper.

7969-41, Session 9

A new model for chemically amplified EUV photoresists

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A new model for chemically amplified EUV photoresists is presented in detail [in final abstract, more specific details will be included in this first sentence.]. This new model predicts several previously-unexplained, experimentally observed phenomena including inside-to-outside corner rounding bias[1], footing on the resist profile, resist top loss, line end shortening, and a peculiar distortion of certain patterns such as jogs and elbows. The new model also appears to provide insight into line edge roughness and the vertical striations reported by George et al.[2].

[paragraph to give details about how the new resist model matches experimental data. Currently the new resist model shows good agreement with existing data (Tom Wallow's distorted patterns, Chris Anderson's corner rounding data, XSEM evidence of footing, and top-loss).]

[There are two test masks being made - one by Global Foundries and another by LBL. The test masks have circles, jogs and line-ends all in both polarities and various sizes, shapes. We expect to nail down the resist parameters for the new model with the circles and jogs, and then show that this model can predict the line-end shortening on the line-end patterns. We expect plenty of data by SPIE and we expect good agreement.]

[a paragraph to discuss other details of the physics of the new model, interpret other observations]

[perhaps a paragraph or sentence to discuss implementation of model]

[possibly a paragraph to discuss relation of new model to roughness and vertical striations]

The new model predicts that certain patterns cannot be effectively corrected with OPC and therefore should be avoided unless resist formulations are improved. [other ways to mitigate the problem]

7969-42, Session 9

LWR and resist collapse improvement in EUV resist process

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Extreme ultraviolet lithography (EUVL) is the most effective way for sub 30nm HP manufacturing. EUV resist showed a fair progress of resolution and sensitivity for pilot-line implementation of sub 32nm HP patterning. However, resist LWR does not meet the requirement of ITRS specification, and resist collapse is one of critical issues for sub 30nm HP manufacturing.

Many researches have been made for the improvement of resist LWR and resist collapse with various kinds of approaches. Rinse material is the most effective technique to address both critical issues. LWR improvement in rinse process is largely dependent on both resist platform and the type of rinse material used. Resist LWR has been improved in a large portion with rinse process, but there has been little study on how much LWR improvement with rinse material can be maintained after etch process. In this paper, we will characterize the resist LWR and resist collapse improvement with two major promising resist platforms using various kinds of rinse materials and demonstrate how much LWR improvement with rinse material could be achieved after etch process.

Resist LWR specification is 2.2nm for 32nm HP based on ITRS 2009, but EUV LWR below 3.5nm after etch process has not been demonstrated yet. The demonstration of below 3.0nm LWR after pattern transfer is important in EUVL and needs to be pursued using all kinds of available technical approaches. We will report results on this kind of activity on LWR improvement with useful techniques.

7969-43, Session 9

Stochastic exposure kinetics of EUV photoresists: a simulation study

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Unlike the direct photon absorption mechanism of exposure for 248-nm and 193-nm photoresists, EUV resists are exposed via photo-ionization: a high-energy photon absorbed in the resist ionizes the polymer, generating an electron, which in turn can generate several secondary electrons. These electrons then scatter through the resist losing energy and, occasionally, interacting with a photoacid generator (PAG) to generate an acid. Monte Carlo simulation of these events leads to a prediction of acid concentration as a function of exposure dose for a given set of resist parameters. Repeated simulations using such a Monte Carlo model can lead to a prediction of both mean acid concentration and its standard deviation. Both results are important in understanding EUV exposure kinetics and in predicting the impact of those kinetics on the line-edge and linewidth roughness of final lithographic images.

In this paper, the Stochastic Resist Model of PROLITH X3.1 is used as the Monte Carlo simulator to predict the number of acids generated within a given resist volume as a function of EUV exposure dose and a set of resist parameters. By repeated simulations, both the mean and standard deviation of the number of generated acids can be determined. Examining the mean acid concentration as a function of exposure dose, the exposure kinetics were found to be first order, and an effective exposure rate constant C was defined. Each determination of C required 10,000 simulations of an open-frame exposure of a 50X50X10nm volume of resist. By varying a wide range of input parameters to the Monte Carlo simulator, an approximate model of how C varies with these parameters was found to predict the actual value of C as determine from PROLITH stochastic simulations to within a few percent over a wide range of parameter values.

Such open-frame exposure simulations also allowed the calculation of the standard deviation of the acid concentration, an important quantity that greatly influences the line-edge roughness (LER) in EUV lithography. A semi-empirical expression was found to predict the standard deviation calculated from the PROLITH stochastic resist model to within a few percent over a wide range of parameter inputs.

The results of this study, semi-empirical expressions for the mean and standard deviation of the acid concentration resulting from the EUV exposure of a chemically amplified resist, are quite significant. They show how acid variance can be reduced for a given exposure dose and by how much:

- Increase PAG loading,

- Increase absorbance, α

- Increase photoelectron generation efficiency, ϕe
- Increase exposure rate constant, C

Further, this model for EUV exposure can be used as a component of a comprehensive model for LER currently being developed.

7969-44, Session 10

Modeling growth of defects during multilayer deposition of EUV blanks by level set method

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Reducing defects on extreme ultraviolet (EUV) masks is one of the most critical issues to be addressed for commercialization of EUV lithography. The defect core, namely the pit or particle, can originate either on the substrate, during multilayer deposition or on top of the multilayer stack. The printability of the final defect will depend on the phase change and the amplitude change in a given position. The net phase change and/or amplitude change adds to the intrinsic effect of the core defect and its influence on the growth of the multilayer stack during deposition. Therefore, identifying this influence is critical. Level set methods are used to simulate defect growth during multilayer deposition. How the shape, profile, and position of the core defect and the growth conditions impact the dimensions of the final defect is discussed. Simulations of defect shape and growth during multilayer deposition take into account the nature of the defect (pit or bump) and direction and incident flux of the material. This paper further discusses and outlines the simulation results for shadow effects due to the directional flux of material. Further, the modeling of the defect growth was improved by including the rotation of the substrate, which is commonly done during deposition to attain better uniformity. In the end, the simulation results considering deposition conditions are compared with the transmission electron microscopy (TEM) characterization of the native defects on EUV mask blanks deposited under similar conditions.

7969-45, Session 10

Demonstration of defect-free EUV mask for 22-nm NAND flash contact hole layer using electron-beam inspection system

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Fabrication of defect free EUV masks including their inspection is the most critical challenge for implementing EUV lithography into semiconductor high volume manufacturing for 22nm half-pitch (HP) node and beyond. NAND flash device, especially the contact hole (C/H) layer, is likely the first device that EUV lithography will be employed for manufacturing due to the aggressive scaling and the difficulty for making the pattern with the current ArF lithography. Furthermore, the C/H layer is assumed the most suitable layer for EUV lithography because of not only the difficulty to resolve pattern but also the low pattern density. The low pattern density makes it easy to cover multi-layer phase defects by absorber film and change it to non-printable defect.

To assure the defect free EUV mask, we used electron beam inspection (EBI) system eXplore 5200 developed by Hermes Microvision, Inc. (HMI) [1]. As one knows, the main issue of EBI system is the low throughput. To solve this challenge, a function called Lightning scan has been recently been developed and installed in the system. The lightning scan mode allows the system to inspect only the C/H pattern area while ignoring the blank area between the C/H, thus sharply reduced the overhead time and enable us to inspect NAND C/H EUV mask with significantly higher throughput.

In this paper, we will demonstrate the possibility of defect free EUV mask fabrication and the inspection using the EBI system with lightning scan mode for the C/H layer of 22nm NAND flash device.

7969-46, Session 10

Development of new FIB technology for EUVL mask repair

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The technology that is used for photomask repair has been evolved to achieve more precise process with the shrinkage of design rules. Recently, most of defects on high-end masks are repaired with electron beam (EB) or focused ion beam (FIB). Since EUVL masks will be applied to hp22nm and beyond, those pattern sizes will be smaller than 88nm. However, the minimum repairable size of the current state-of-the-art repair systems is about 20-30nm. From the viewpoints of the pattern sizes and the minimum repairable size, development of a new repair technology is expected to satisfy requirements for EUVL masks.

We are developing a new FIB technology which is expected to be one of solutions to EUVL mask repair. Conventional FIB systems use gallium ions (Ga+) from a liquid metal ion source (LMIS), but the new FIB system uses hydrogen ions (H2+) or helium ions (He+) from a gas field ion source (GFIS).

In the etching and deposition process induced by EB and the new FIB, secondary electrons play an important role. The region where EB generates secondary electrons is not small, because incident electrons scatter near the surface of masks. On the other hand, the region where the new FIB generates secondary electrons is small, because incident ions (H2+, He+) penetrate into the depths of masks. Therefore, the process region with the new FIB is smaller than that with EB. Furthermore, the diameter of the new FIB is theoretically estimated to be smaller than that of EB. Those advantages suggest that the new FIB technology is a promising solution of repairing EUVL masks of hp22nm and beyond.

We have made a repair system by implementing the new FIB technology and evaluated its performance, such as beam diameter, scan damage and minimum repairable size for the feasibility study. The latest results of our evaluation are reported in this paper.

7969-47, Session 10

Inspectability of mask phase defects in EUV lithography

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EUV mask defects, especially those buried defects under the multi-layered mirror (MLM), are regarded as one of the most critical issues for successful introduction of EUV lithography in the mass production of semiconductor IC's. To prepare the capability to characterize and handle such defects, we fabricate a programmed-defect mask. Both bump and pit defects of various dimensions are created on the same mask by E-beam patterning and various heights or depths of these defects are generated through several cycles of low-thermal-expansion material (LTEM) substrate etching. The smallest bump and pit defects achieved are 20 nm and 40 nm, respectively. The substrate is then deposited with MLM and absorber, forming phase defects for patterns on the absorber. Patterns on the absorber include line/space and hole features of various pitches and are designed to allow for various relative distance with respect to these phase defects.

The mask can be used to define the size specification of allowable defects on the substrates, according to their printability. More, the mask can be used to qualify a mask defect inspection tool, according to the inspectability of defects that are printable. In this paper, we will focus on the mask process for realizing programmed-defect masks and their preliminary inspection results.

7969-48, Session 10

Compensation for EUV multilayer defects within arbitrary layouts by absorbers pattern modification

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Multilayer defect compensation, enabled by fast, three-dimensional, electromagnetic, extreme ultraviolet (EUV) mask simulation, will be demonstrated for arbitrary multilayer defects within arbitrary absorber patterns. The goal of multilayer defect compensation is to transform an EUV mask blank, which is unusable due to multilayer defects, into a mask which can be used to print the desired image on the wafer, by modifying the absorber pattern near the defect. This is a fundamentally difficult problem because multilayer defects primarily modulate the phase of the reflected light, while the absorber pattern primarily modulates the amplitude. So, the effect of the defect must be compensated for by the absorber without modifying the phase of the reflection directly. The problem is also difficult for practical reasons, such as determining the geometry and location of the defect before generating a compensation pattern, and designing compensation patterns that are manufacturable. This work will primarily focus on designing and studying manufacturable compensation patterns with simulation, assuming the multilayer defect geometry is known.

The compensation method described in this work is iterative, and each iteration requires one three-dimensional mask simulation with the current absorber pattern. With standard rigorous simulation methods, developing a compensation pattern for a single defect would take days.

But, in this work the fast simulation software Defect Printability Simulator (DPS) is used to produce compensation patterns in minutes.

Compensation experiments with simulation and wafer print have been performed before, but none of these has attempted to improve the image through focus or compensated for a defect in an arbitrary pattern.

This work uses an edge based algorithm that is valid for arbitrary designs. Multiple through focus images are used in each iteration to determine the compensation pattern, which improves the final compensation pattern through focus.

Simulation makes the rapid study of many practical effects possible.

In this work, the effects of the errors in the assumed defect geometry and repair tool or mask writer are investigated. Also, the effects of off-axis illuminations on the effectiveness of compensation are explored.

7969-57, Poster Session

Comparison between ADT and PPT for 2X-DRAM patterning

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Extreme Ultra-Violet (EUV) lithography is almost only solution reachable for next-generation lithography below 30nm half pitch with relative cost competitiveness. In this study, we investigate the feasibility of EUV lithography for applying below 3X nm dynamic random access memory (DRAM) patterning.

Very short wavelength of 13.5nm adds much more complexity to the lithography process. To understand for challenges of EUV lithography for high volume manufacturing (HVM), we study some EUV specific issues by using EUV full-field scanners, alpha demo tool (ADT) at IMEC and pre-production tool (PPT) at ASML.

Good pattern fidelity of 2X nm node DRAM has been achieved by EUV ADT, such as dense line and dense contact-hole. But CD uniformity of 3X nm dense contact-hole by EUV is very challenging, even compared to ArF immersion lithography with litho-freezing-litho-etch (LFLE) technology. In the previous study, such poor CD uniformity was mainly caused by intra-field CD uniformity, especially in slit CD uniformity. In this paper, we will report on CD uniformity and process window of 2X nm node DRAM layers with both ADT and PPT. Then we investigated the contribution of each factor that is known to influence the CD fingerprint in EUV lithography such as shadow effect, flare effect, slit intensity uniformity, reticle CD error, image plan focus deviation and lens aberration (in particular, astigmatism aberration).

7969-58, Poster Session

Shadowing effect modeling and compensation for EUV lithography

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EUV lithography is one of the leading technologies for 16nm and smaller node device patterning. One patterning issue intrinsic to EUV lithography is the shadowing effect due to oblique illumination at the mask and mask absorber thickness. This effect can cause CD errors up to several nanometers, and, consequently, needs to be accounted for in OPC modeling and compensated accordingly in mask synthesis. Because of the dependence on the reticle field coordinates, shadowing effect is very different from the traditional optical and resist effects. It poses challenges to modeling, compensation, and verification that were not encountered in tradition optical lithography mask synthesis: 1) information of chip placement on the reticle and how the reticle is scanned is needed; 2) correction has to be instance based instead of cell based; 3) asymmetric correction may be needed even for 1D patterns; and 4) ideally, model-based correction should be employed so that it is more verification friendly.

In this paper, we present a systematic approach for shadowing effect modeling and model-based shadowing compensation. Edge based shadowing effect calculation with reticle and scan information is presented. Model calibration and mask synthesis flows are described. Experiments are performed to demonstrate the effectiveness of the approach.

7969-59, Poster Session

Convergence study for lines, spaces and holes

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As the OPC scripts become more and more complex for advanced technology nodes, the number of parameters used to control the convergence increases drastically. This paper does not aim to determine what a "good convergence criteria" is but rather to review the efficiency of the existing OPC solutions in terms of accuracy and parameter dependence, to solve simple design layouts. Three different OPC solutions, including a "standard algorithm", a "local convergence OPC" and a more holistic OPC, are compared on different structures containing lines, spaces and holes. A cost function is used to determine the quality of the convergence for each structure. Resulting number of iterations required for convergence is reported for each OPC solution as a map of convergence (OPC solution vs iterations).

7969-60, Poster Session

Particle qualification procedure for the TNO EUV reticle load port module of the HamaTech MaskTrackPro cleaning tool

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Co. KG (Germany)

During transport/handling of EUV reticles the risk for particle contamination is high. HamaTech is developing the first EUV reticle automation tool; used in combination with the MaskTrack Pro cleaning tool close to the EUVL tool. TNO has developed the Load Port for EUV reticles. To demonstrate that the Load Port functions sufficiently particle free (particles ≥50nm), TNO has developed a particle qualification procedure. At the SPIE Advanced Lithography 2011, the qualification procedure will be evaluated and the latest particle cleanliness results of the Load Port will be presented.

7969-61, Poster Session

EUVL dark-field exposure impact on CDs using thick and thin absorber masks

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EUV lithography can support 15 nm logic manufacturing and beyond. As critical feature sizes shrink, it is desired to reduce the EUV mask absorber thickness in order to minimize 3D mask effects as well as accommodate the incident angles required by the PO design for future generation (higher NA) EUVL toolsets.

When compared to a thick absorber mask, the thin absorber EUV mask is expected to have a comparable process window, a reduced shadowing effect, and lower MEEF. However, regardless of the mask absorber thickness, the dark-field in EUV lithography is never 100% dark. Using the same absorber stack composition, EUV masks with thinner absorbers have inherently higher leakage due to the background transmission propagating through the absorber stack. While this does act to improve resist sensitivity or throughput, the leakage reduces the image contrast and can cause CD degradation in “double” exposed regions at the edge of adjacent fields.

In this study, we present EUVL lithographic benchmarking of both thin and thick absorber masks on the Intel MET and the ASML ADT at IMEC. We have experimentally quantified the process window, EL, LWR, MEEF, Esize, ultimate resolution, and impact of dark-field background exposures on CDs for both thin and thick absorber masks. We discovered there are additional issues when field edges overlap with adjacent fields and will discuss mitigation strategies for EUV leakage emanating from dark-field regions.

7969-62, Poster Session

Particle detection on flat surfaces

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Since 2006, EUV Lithographic tools have been available for testing purposes. This gave a boost to the development of fab infrastructure for EUV masks. The absence of a pellicle makes the EUV reticles extremely vulnerable to particles. Therefore, the fab infrastructure for masks must meet very strict particle requirements. It is expected that all new equipment must be qualified on particles before it can be put into operation. This qualification requirement increases the need for a low cost method for particle detection on mask substrates.

TNO developed its fourth generation particle scanner, the RapidNano. The RapidNano is capable of detecting nm sized particles on flat surfaces. The detection is based on dark field imaging techniques and fast image processing. The tool was designed for detection of a single added particle in a handling experiment over a reticle sized substrate. Therefore, this tool is very suitable for the validation of particle cleanliness of equipment and processes. During the measurement, the substrates are protected against particle contamination by using a protective environment. All stages and other possible particle sources are placed outside the protective environment. The imaging takes place through a window. The geometry of the protective environment enables large flexibility in substrate shape and size. Particles can be detected on substrates varying from 152 x 152 mm mask substrates to wafers with a diameter up to 150 mm.

Programmed chromium defects on silicon were used for determination of the sensitivity of the RapidNano. Particles of 50 nm and larger were detected automatically. Results on capture efficiency for particles in the range between 30 nm and 400 nm according to the standard SEMI M50-0307 will be presented.

7969-63, Poster Session

Impact of mask line-edge roughness on exposed resist lines in extreme-ultraviolet lithography

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Resist Line Edge/Width Roughness (LER, LWR) are two of the most critical aspects in Extreme Ultraviolet Lithography (EUV) for the 32 nm technological node and below. In order to achieve the International Technology Roadmap for Semiconductors (ITRS) specifications for resist LER and LWR, different methods are being explored: resist composition, speckle contribution, mask line/surface roughness, and post-litho smoothing processes.

In this paper mask LER/LWR and resist LER/LWR have been characterized and compared by using spatial and frequency analyses on top-down Scanning Electron Microscopy (SEM) images. It was found that Low Frequency (LF) mask roughness is well correlated with the Power Spectral Density (PSD) of the resist edges. High Frequency (HF) resist roughness resulted to be less critical than the LF LWR, smoothened by the cut-off of the EUV optical system which acts as a Low Pass filter during the exposure process (Table 1 A).

Experimental data for both mask and resist were subsequently implemented in the Prolith stochastic simulator in order to quantify the mask LER/LWR contribution to the final resist roughness: a comparison between the stochastic physical resist modeling and deterministic physical resist modeling confirmed the significant contribution to the overall resist LER/LWR in the LF range (Table 1 B). HF roughness component was obviously absent in the deterministic simulation.

7969-64, Poster Session

Fast and accurate EUV mask simulation with new modular simulator

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A new fast and accurate simulator, called LAIPH EUV Defect Printability Simulator or DPS, is presented which can accurately simulate the wafer image generated by an extreme ultraviolet (EUV) lithography mask with a buried defect three to four orders of magnitude faster than rigorous methods. The simulator has been built by taking the concepts developed at the University of California - Berkeley for the simulator RADICAL and presented in [1], making improvements where necessary, and combining them with the technology already in place at Luminescent Technologies to produce a full featured simulator for EUV mask research, development, and inspection. DPS achieves its speed with a modular design that utilizes different simulation methodologies specifically designed for each component of the EUV mask. The outputs of each simulator within DPS are linked by converting the electric field output of one into a set of plane waves to be input into the next.

The absorber is modeled by the propagated thin mask model first proposed in [2] and described in detail in [1]. This model starts with a simple thin mask transmission. A point source, for one-dimensional patterns, or a line source, for two dimensional patterns, is added to the thin mask transmission at the edges of the absorber. Finally, this whole field is propagated by a fraction of the total absorber height to account

for the thickness of the absorber. The value of the point source and the propagation distance must be calibrated from rigorous simulation. Unlike the method in [1], which required manual pre-calibration of the point sources and propagation for each new type of absorber, the LAIPH EUV Defect Printability Simulator has automatic calibration, using rigorous coupled wave analysis (RCWA), built-in. This leads to more flexibility and better accuracy.

The other major component of DPS is the multilayer simulator. Two options are available to simulate EUV masks with buried defects. One is the advanced single surface approximation presented in [1]. This is appropriate for simulations where only the top surface profile of the mask is known or the layers below the surface are uniform. A slightly slower, but more general multilayer simulator will also be available within DPS. This new multilayer simulation method can accurately predict the reflection from non-uniform layers below the surface of the multilayer. It uses a different algorithm than the ray tracing method developed by Lam and included in [1]. This new algorithm has comparable accuracy to that ray tracing method, but is faster and more flexible.

The speed and accuracy of this new simulator will be demonstrated by comparisons to rigorous simulations using methods such as RCWA and the finite difference time domain (FDTD). Several specific applications to demonstrate the flexibility of the simulator will also be shown.

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[2] M. C. Lam, et al., “Simplified model for absorber feature transmissions on EUV masks”, Proc. of SPIE, Vol. 6349, (2006).

7969-65, Poster Session

Evaluation results of a new EUV reticle pod having reticle grounding paths

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A new SEMI standard E152-0709 “Mechanical Specification of EUV Pod for 150 mm EUVL Reticles” has been published in July 2009. In the standard, reticle grounding requirements are mentioned as related information: an electrical connection between the front and back sides of EUVL reticles as well as the electrical connection to the reticle backside from outside the outer pod may be needed and specified in future. Reticle grounding is very important for reticle protection not only from ESD damage but also from particle contamination. We reported particle adhesion on charged substrates during pumping down and venting cycles1. It is obvious that an EUV mask has to be grounded during shipping, storage and tool handling to prevent particle adhesion. Canon, Nikon and Entegris have jointly developed a new EUV pod “cnPod/ESD” which has electrical connections to the reticle from outside the outer pod by modifying a SEMI compliant EUV pod “cnPod” 2. In order to have an electrical connection between the reticle backside and the outer pod, a cantilever is installed inside the inner pod cover. The cantilever touches the reticle backside just inside 146mm x 146mm which is specified as the minimum conductive layer area in SEMI P37 “Specification for Extreme Ultraviolet Lithography Substrates and Blanks”. In order to have an electrical connection between the reticle front side and the outer pod, though it is not required in E152, an electrical conductive material is used for the reticle supports on the inner pod baseplate.

We will show various evaluation data of the new ESD pods from particle contamination point of view and will discuss the necessity of the reticle grounding in this meeting. We used CrN coated substrates for the evaluation instead of real EUV masks, because LR-TaBN films which are in common use for an absorber has a dielectric layer, TaBO, on the top. The dielectric layer is a strong obstacle to ground the reticle from the supports on the baseplate. In addition, the film area on the reticle front side is not specified in SEMI P37. Reticle grounding is very important for reticle protection not only from ESD damage but also from particle contamination and MIRAI-Selete has confirmed the effectiveness of reticle grounding using a new EUV pod “cnPod/ESD”. However, modification of P37 is needed to make a universal EUV pod which has an electrical connection between the reticle front side and the outer pod.

This work is supported by NEDO.

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[2] “Evaluation Results of a New EUV Reticle Pod based on SEMI E152”, Kazuya Ota, Masami Yonekawa, Takao Taguchi and Osamu Suga, Proc. of SPIE Vol. 7636 76361F (2010).

7969-66, Poster Session

Repeat mask cleaning effects on EUV lithography process and lifetime

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The reflective, multilayer based, mask architectures for extreme ultraviolet (EUV) lithography are highly susceptible to surface oxidation and contamination. As a result, EUV masks are expected to undergo cleaning processes in order to maintain the lifetimes necessary for high volume manufacturing. For a mask cleaning process to be practical, negligible negative impact on mask performance after repeated cleaning is a requirement. Mask surface damage and the increased LER that may result from repetitive cleaning still remains a concern.

For this study, the impact of repetitive cleaning of EUV masks on imaging performance was evaluated. Two, high quality industry standard, EUV masks are used for this study with one of the masks undergoing repeated cleaning and the other one kept as a reference. The SEMATECH Berkeley 0.3 NA micro-field exposure tool (MET) patterned 40 nm and 36nm equal lines and spaces are evaluated for process changes. Exposure data from these two masks with the same architectures were collected using the same resist and exposure conditions prior to the start of the cleans. Lithographic performance, in terms of process window analysis and line edge roughness, was monitored after every two cleans and compared to the reference mask performance. Moreover, mask surface is monitored by atomic force microscopy (AFM) and reflectivity changes are monitored by x-ray reflectometry.

The initial results from these studies, was reported recently [1]. After a total of eight cleans of the mask, minimal degradation is observed in the lithographic performance. Critical dimension (CD) matched LER curves for all cases is near 4.0 nm in the best dose and focus region of the process. The variations in LER are shown to be less than the process uncertainty determined for this resist at ±0.4nm. Exposure latitudes calculated also show similar results, where it remains within the process error for the eight cleanings completed. Furthermore, surface analysis by AFM did not show changes in the mid-spatial frequency roughness measured after each clean as can be seen from the data tabulated in table 1. We conclude that the cleaning cycles completed to this point did not damage mask multilayer or absorber structures. The cleaning cycles are continued until significant loss in imaging fidelity is found. In this paper, we outline the results for the total duration of these studies spanning nearly a year.

1.S. A. George, L-M. Baclea-an, P. P. Naulleau, R. J. Chen, T. Liang, EUV mask surface cleaning effects on lithography process performance, J. Vac. Sci. Technol. B (manuscript #40692, accepted August 2010).

7969-67, Poster Session

Quantitative evaluation of mask phase defects from through-focus EUV aerial images

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Mask defects inspection and imaging is one of the most important issues

for any pattern transfer lithography technology. This is especially true for EUV lithography where the wavelength-specific properties of masks and defects necessitate actinic inspection for a faithful prediction of defect printability and repair performance. In this paper we will present a technique to obtain a quantitative characterization of mask phase defects from EUV aerial images. We apply this technique to measure the aerial image phase of native defects on a blank mask, measured with the SEMATECH Berkeley Actinic Inspection Tool (AIT) an EUV zoneplate microscope that operates at Lawrence Berkeley National Laboratory. The measured phase is compared with predictions made from AFM top-surface measurements of those defects.

While amplitude defects are usually easy to recognize and quantify with standard inspection techniques like scanning electron microscopy (SEM), defects or structures that have a phase component can be much more challenging to inspect. A phase defect can originate from the substrate or from any level of the multilayer. In both cases its effect on the reflected field is not directly related to the local topography of the mask surface, but depends on the deformation of the multilayer structure.

Using the AIT, we have previously showed that EUV inspection provides a faithful and reliable way to predict the appearance of mask defect on the printed wafer; but to obtain a complete characterization of the defect we need to evaluate quantitatively its phase component.

While aerial imaging doesn't provide a direct measurement of the phase of the object, this information is encoded in the through focus evolution of the image intensity distribution. Recently we developed a technique that allows us to extract the complex amplitude of EUV mask defects using two aerial images from different focal planes.

The method for the phase reconstruction is derived from the Gerchberg-Saxton (GS) algorithm, an iterative method that can be used to reconstruct phase and amplitude of an object from the intensity distributions in the image and in the pupil plane. The GS algorithm is equivalent to a two-parameter optimization problem and it needs exactly two constraints to be solved, namely two intensity distributions in different focal planes. In some formulations, adding any other constraint would result in an ill posed problem. On the other hand, the solution's stability and convergence time can both be improved using more information. We modified our complex amplitude reconstruction algorithm to use an arbitrary number of through focus images (see fig. 1) and we compared its performance with the previous version in terms of convergence speed, robustness and accuracy.

We have demonstrated the phase-reconstruction method on native, mask-blank phase defects and compared the results with phase-predictions made from AFM data collected before and after the multilayer deposition. The method and the current results could be extremely useful for improving the modeling and understanding of native phase defects, their detectability, and their printability.

7969-68, Poster Session

Physical and geometric optics models for mask roughness induced LER

B. M. McClinton, P. P. Naulleau, Lawrence Berkeley National Lab. (United States)

Collective understanding of how both the resist and line-edge roughness (LER) on the mask affect the final printed LER has made significant advances. What is poorly understood, however, is the extent to which mask surface roughness couples to image plane LER as a function of illumination conditions, NA, and defocus. Recently, a simplified model approach to mask roughness induced LER has been proposed which offers a faster and less cumbersome alternative to the traditional method of full 2D aerial image simulation modeling. The implementation of that simplified model is described here in detail. One step in the implementation of the simplified model is the scaling of speckle by the intensity at the line-edge, which has certain implications for printing isolated lines versus isolated spaces. For small critical dimensions (CDs), the intensity in the middle of an isolated space is damped compared to the intensity maximum reached in the clear-field surrounding an isolated line. This provides a benefit in damping the intensity-scaled speckle at the line-edge, and consequently the mask roughness induced LER as well. Simulation data is presented for an aberration-free imaging system with NA = 0.32, both 22-nm and 50-nm isolated lines and spaces, on a rough mask with replicated surface roughness (RSR) 50 pm, for a range of correlation lengths and a variety of disk illumination conditions. We also investigate the LER behavior at long correlation lengths of surface roughness on the mask. We find that for correlation lengths greater than approximately 3 /NA in wafer dimensions and CDs greater than approximately 0.75 /NA, the simplified model, which remains based on physical optics, converges to a "geometric regime" which is based on ray optics and is independent of partial coherence. In this "geometric regime", the LER is proportional to the mask slope error as it propagates through focus, and provides a faster alternative to calculating. Data is presented for both an NA = 0.32 and an NA = 0.5 imaging system for CDs of 22-nm and 50-nm horizontal-line-dense structures.

7969-69, Poster Session

LER aberration sensitivity and extended dipole illumination

B. M. McClinton, P. P. Naulleau, Lawrence Berkeley National Lab. (United States)

Here we conduct a mask-roughness-induced line-edge-roughness (LER) aberrations sensitivity study on the printing of features using potential illumination candidates for both the 22-nm and 16-nm half-pitch nodes respectively in extreme-ultraviolet lithography (EUVL). Full 2D aerial image modeling for an imaging system with NA = 0.32 was done for features on a rough mask with a replicated surface roughness (RSR) of 100 pm and a correlation length of 32 nm. As the ideal RSR value for commercialization of EUVL is 50 pm and under, and furthermore as has been shown elsewhere, a correlation length of 32 nm of roughness on the mask sits on the peak LER value for an NA = 0.32 imaging optic, these mask roughness values and consequently this aberrations sensitivity study presented here, represent a worst-case scenario. The illumination conditions were chosen based on potential candidates for the 22-nm and 16-nm half-pitch nodes, respectively. In the 22-nm case, a disk illumination setting of = 0.50 was used, and for the 16-nm case, crosspole illumination with = 0.10 at an optimum offset of dx = dy = .67 in sigma space. In addition, we consider an alternate source shape that is a dipole extended into a strip, properly displaced for the 16-nm node. Surprisingly, while increasing the length of the dipole, and thus decreasing the illumination coherence in the direction orthogonal to the lines, has no impact on LER. Furthermore, the LER found from the extended dipole is the same as that found for 16-nm lines and spaces under crosspole illumination with = 0.10 and an optimum offset of dx = dy = .67 in sigma space. It is shown that this surprising result is a direct consequence of the 'geometrical regime' found for LER, as presented elsewhere at this conference. Thus, while the extended dipole illumination maintains roughly the same LER control through focus as the crosspole, preliminary results show it has an added benefit in improving imaging quality, in terms of ILS, NILS, and contrast.

7969-70, Poster Session

Absorber height effects on SWA restrictions and 'shadow' LER

B. M. McClinton, P. P. Naulleau, Lawrence Berkeley National Lab. (United States); T. I. Wallow, GLOBALFOUNDRIES Inc. (United States)

As extreme-ultraviolet lithography (EUVL) moves towards commercialization and pushes to ever smaller critical dimensions (CDs), 3D effects of mask absorber patterns become increasingly important. Specifically, the limit to which side-wall-angle (SWA) needs to be controlled to maintain the required 10% CD tolerance is as yet not well known. In addition, how shadowing caused by the necessary off-axis illumination onto the multilayer mirror mask pattern with mask absorber LER effects the transferred LER to the aerial image is also not well

understood. In this study, we look at these 3D effects of absorber height on mask patterns and their implications for EUVL. We first consider the extent to which side-wall-angle (SWA) constrains the process window for an NA = 0.32 aberration-free imaging system with 4X demagnification. Preliminary results show that the nominal SWA has no effect on the process window size, at least for the three SWA cases we investigated: 80, 85, and 88 degrees SWA. Data also seem to show that for 88-nm lines and spaces measured-to-size at the top of a 70 nm absorber (in mask dimensions), a disk illumination with = 0.50 with a nominal SWA of 85 degrees requires that the SWA must remain within ± 0.25 degrees in order to maintain the 10% CD tolerance, after optimizing the process window. In addition, CD tolerance sensitivities are minimal as a function of nominal SWA. Secondly, we also consider how off-axis illumination of 4 degrees on mask absorber pattern line-edge-roughness (LER) effects the resulting aerial image LER through shadowing. We discretely sample a 4-nm amplitude mask LER over a wide range of spatial frequencies for both 22- and 50-nm lines and spaces for an NA = 0.32 aberration-free imaging system with 4X demagnification. So far, data suggests that shadowing causes slight differences between the left- and right-side LER. Data was gathered using the commercial software applications Panoramic and EM-Suite.

7969-119, Poster Session

EUVL alternating phase-shift mask

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Extreme ultra-violet Lithography (EUVL) alternating phase shift mask (APSM) or other optical enhancement techniques are likely needed for 16nm half pitch (HP) technology generation and beyond using EUVL due to resolution and process window limitations. The fabrication of EUVL APSM is more difficult than either EUVL binary mask or conventional optical APSM fabrication. In the case of EUVL APSM, the phase difference in the two regions (0 and 180-degree phase regions) is created by a phase step in the substrate before multilayer (ML) coating as illustrated in Fig. 1. The step height that induces 180-degree phase mismatch in the ML is determined by [/(4cos 2m+1), where m are integers (0, 1, 2, ...). In the experiment, we targeted for a step height with m=1. The same mask design also contains the standard binary structures so that a comparison between the EUVL APSM and the EUVL binary mask can be performed under the same illumination and wafer process conditions. The EUVL APSM is exposed on a full-field 0.25NA Nikon EUV1 scanner. The wafer level results showed higher dense line resolution for EUVL APSM as compared to that of EUVL binary mask for equivalent illumination conditions (conv. 0.3). This result is given in Fig. 2. Resolution down to 22nm HP with modulation down to 16 nm HP was demonstrated. APSM also showed improved line width roughness (LWR) and depth of focus (DoF) as compared to the best EUVL binary results obtained with OAI (C-Dipole).The wafer CD resolution improvement obtained by APSM in the experiment is partially limited by the resist resolution and the mask phase edge spread during ML deposition. We believe that wafer CD resolution can further be improved with improved resist resolution and a phase fabrication process. In the presentation, we will discuss in detail the mask fabrication process, wafer level data analysis, and our understanding of EUVL APSM related issues.

7969-71, Poster Session

Relationships between EUV resist outgassing and contamination deposition at Selete

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The development of high-performance EUV resists is still one of top three critical issues in EUV lithography. In addition resist outgassing is a specific issue for EUV resist. Many researchers have investigated EUV resist outgassing by use of pressure-rise method and quadropole mass analyzer (Q-MASS). These method, however, have some weak points evaluating the relation-ship between contamination deposition on optical elements (projection optics mirrors and masks) and a specific resist outgassing molecule because pressure-rise method only measures total pressure from resist outgassing and Q-MASS method shows fragmentation of resist outgassing molecules. Therefore we introduced gas chromatography mass spectrometry (GC-MS) to measure exactly EUV resist outgassing species [1].

This presentation summarizes the systematic evaluations of EUV resist outgassing by GC-MS and witness sample to obtain the relationships between resist outgassing and contamination deposition. We will discuss the resist outgassing species of EUV model resists determined by GC-MS and contaminated materials on optical elements (witness samples) by EUV irradiation.

This work is supported by New Energy and Industrial Technology Development Organization (NEDO).

[1] Hiroaki Oizumi, Kazuyuki Matsumaro, Julius Joseph Santillan and Toshiro Itani: Proc. SPIE 7636 (2010) 76362w.

7969-72, Poster Session

Interaction of benzene and toluene vapors with Ru(0001) surface: relevance to MLM contamination

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We report studies of the interaction of benzene and toluene vapors with the Ru(0001) surface, a model cap layer for multilayer mirrors (MLMs), using temperature programmed desorption (TPD), X-ray photoelectron spectroscopy (XPS), low energy ion scattering (LEIS), electron stimulated desorption (ESD) and scanning tunneling microscopy (STM). A tunable broad-beam low energy electron source (0-200 eV) is used to simulate EUV-radiation-induced surface reactions. We have bombarded the entire sample with a defocused electron beam while exposing it to a hydrocarbon vapor from a capillary array doser. The experimental TPD results indicate that bonding of adsorbed hydrocarbons is dissociative on Ru(0001). On clean Ru we find for these molecules that a fraction of a monolayer (ML) dissociates almost completely. Performing repeated adsorption/desorption cycles of these gases without cleaning the sample surface between cycles leads to a stepwise increase in the surface carbon coverage and buildup a self-limited carbon monolayer. Desorption of molecular hydrogen due to decomposition of hydrocarbon molecules at T > 300 K, with a multiple-peak TPD spectrum, is the only reaction product observed from the sample surface. Graphene monolayer and bilayer formation on Ru by hydrocarbon pyrolysis or by carbon segregation from the sample bulk is examined as a possible way to reduce the surface contamination rate. Graphene buildup has been confirmed by the presence of corresponding superstructures in LEED patterns and STM images. The binding energy of the hydrocarbon molecule is found to be smaller on a graphene layer than on disordered carbon. Electron bombardment of the Ru surface in the presence of gas phase hydrocarbons leads to C-buildup whose thickness depends on pressure and temperature. Carbon layer thickness was evaluated from the attenuation of the Ru 3d5/2 XPS peak. The comparison of electron-induced carbon growth rate for clean Ru surface with that for graphene-precovered Ru is presented. Electron bombardment of fractional ML of hydrocarbon molecules yields H+ as the only ionic desorption product. A quadrupole mass spectrometer (QMS) with its ion source turned off was used for mass analysis of positive ions produced by electron impact on the adsorbed hydrocarbon layer. The total cross section for electron-induced dissociation of hydrocarbons on clean and C-covered Ru can be determined from the decay of H+ ion current as a function of time.

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7969-73, Poster Session

EUV reflectivity studies of CO2 and YAG LPP contaminated Ru mirrors

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To maintain the incremental development of semiconductors governed famously by Moore's Law, new lithography techniques must be developed. Current visible and ultraviolet light imprinting methods have reached their maximum limitations and the extreme ultraviolet (EUV) region has been selected as a possible successor. While EUVL offers a solution to extend Moore's Law, several problems persist pursuant to large-scale industrial application. Laser produced plasmas (LPP) from tin have been demonstrated to emit EUV radiation (13.5 nm light) with a reasonably acceptable conversion efficiency, although debris accumulation on the collector optics is still a major issue.

Our recent results have shown that CO2 produced laser plasmas emit less debris compared to Nd-YAG LPP.1-3 However, CO2 LPP ions are more energetic compared to YAG LPP ions. The dissimilarity in debris features are explained due to nearly 2 orders of magnitude difference in critical density of the pump beam as well as variation in the laser energy deposition in these plasmas. This article investigates further the debris emission from CO2(35 ns, 10.6 micron) and Nd-YAG (6 ns, 1.06 micron) laser produced tin plasmas, focusing specifically on the changes in the EUV reflectometry of the collector optics. Both YAG and CO¬2 LPP contain distinct atomic and ionic debris distribution and hence damages caused by the debris affect the mirror reflectivity differently. Sputter deposited Ruthenium mirrors are placed at various angular positions throughout a stainless steel vacuum chamber and act as witness plates to the YAG and CO2 plasma debris. The contaminated mirrors are then transported to the IMPACT facility for EUV reflectivity studies. The EUV reflectivity set includes a 13.5 nm light source (Phoenix EUV sem|20 source) and EUV photodiodes. Differences in EUV reflectivity of mirrors exposed to YAG and CO2 laser produced tin plasma debris at various angles will be reported.

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7969-74, Poster Session

Dependence of contamination rates on key parameters in EUV optics

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Optics contamination remains one of the challenges in extreme ultraviolet (EUV) lithography. Current plasma sources used in EUV exposure tools emit a wide range of out-of-band (OOB) wavelengths in addition to the desired wavelength near 13.5 nm (EUV). We present results from the study of surface charging effects and interaction of ions from the source with the surface relating to EUV contamination. We also present experimental results of contamination rates of EUV and OOB light using a xenon plasma source and a deuterium arc lamp and filters. The results indicate that contamination rates with some OOB radiation wavelengths are higher than with EUV radiation. The fact that radiation near and beyond 190 nm (below 7eV photon energy) can contaminate optics is reported in literature [1]. The angle of illumination of the optics is important. At shallow angles, the contamination rate is faster because of higher surface area being exposed, and the effect of that contamination on the reflectivity of the optics is greater. Also at shallow angles there is a mechanism that increases the surface roughness of the contamination layer, causing scattering from the contaminated optics. The temperature of the optic has a significant effect on the contamination rate. Reducing the temperature of the optic by about 10 degrees, the contamination can be more than doubled. Selected species were tested to help understand the cause of the contamination mechanism and the effect of the contamination due to resist outgassing components when exposed near high volume manufacturing (HVM) intensities. Results show that diphenyl sulfide poses a risk of contamination when outgassing from photoresists.

7969-75, Poster Session

Bandwidth control of Mo/Si multiyear-based EUV high reflectors

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Mo/Si multilayer is one of the most frequently used material combinations for high reflective coatings at extreme ultraviolet (EUV) wavelengths. A reflectance greater than 70% at 13.5nm could be designed with an alternation of quarter-wave Mo/Si multilayers. A typical bandwidth of 0.6nm at full-width-half-maximum (FWHM) can be realized with a Mo/Si structure with 50 bilayer periods. It is possible to narrow the spectral bandwidth by optimizing the Mo/Si multilayer design. Various narrowed bandwidths of EUV high reflectors were calculated by changing the ratio of Mo thickness to the Mo/Si bilayer period and the total number of the periods. A Mo/Si based multilayer EUV mirror designed at 13.5nm and 10o angle of incidence was measured by scanning grazing angles from 0o up to 85o. Measured data will be compared to the designs.. The difference between the measured and designed peak position and reflectance will be discussed in terms of film microstructure, interface and thickness evolution from substrate surface to the outermost layer revealed by high resolution transmission electron microscopy (HRTEM), glazing angle X-ray reflectivity (GIXR) and atomic force microscopy (AFM) measurements.

7969-76, Poster Session

Experimental and theoretical study on asymmetric carbon contamination coverage observed on SFET-exposed mask

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EUV mask contamination has a strong, negative impact on both throughput and printing performance in extreme ultraviolet lithography (EUVL). Our previous study using optical simulation analysis revealed that the impact depends on the optical characteristics of the contaminant layer and on the type of coverage (conformal or not)1). So we have to determine the nature of the carbon film and its coverage on an actual exposed mask to accurately evaluate the impact of contamination on lithographic performance.

We analyzed a mirror that was exposed for long time in the Small-Field Exposure Tool (SFET) to determine the nature of the carbon film. We used many surface analysis techniques, such as ellipsometry, microbeam X-ray diffraction, TEM, XPS, RBS(Rutherford backscattering spectroscopy), ERDA (elastic recoil detection analysis, and so on. The results showed that the contaminant film was amorphous-like carbon containing a large amount of hydrogen.

We also examined the carbon film coverage of an SFET-exposed mask by using CD-SEM and 3D-AFM (Veeco InSight 3DAFM). CD-SEM images of clean and contaminated masks revealed not only that contamination growth increased the line width, but also that the image of the contaminated mask had asymmetric features, i.e., the white band was wider on the sunshine side than on the sunshade side. 3D-AFM profiles support the CD-SEM observations such as increase of pattern width and pronounced top-corner-rounding on the sunshine side than on the sunshade side.

Clear asymmetry of carbon coverage was observed in our recent work of TEM observation in the case of perpendicular illumination: The contaminant film is thinner on the sunshade side than on the sunshine side. In addition, the sunshade side has an overhang shape. On the other hand, the coverage is almost conformal when the illumination is parallel to the mask pattern, although there tends to be a small overhang.

To understand how asymmetric growth originates, we constructed a theoretical model of carbon growth on a patterned mask. The model involves three calculation steps: (1) The electric field strength in the near field of the mask pattern is calculated based on electromagnetic field theory. (2) The growth rate is calculated based on the assumption that it is proportional to the electric field strength at each surface point. (3) The change in the surface profile is calculated using a string model. When Step 3 is finished, we go back to Step 2 and calculate the growth rate on the new surface. Repeating this procedure yields the time-wise change in the contaminated surface.

The results of above calculation reproduce the TEM observations such as asymmetry and overhang shape in sidewall carbon coverage when the illumination is perpendicular to the mask pattern, and also almost conformal coverage and slight overhang structure in parallel illumination. Quantitative comparison between theory and TEM experiment will be discussed in the presentation.

Based on the above knowledge, we examined the lithographic impact of this asymmetric coverage by using EM-Suite simulation.

7969-77, Poster Session

Damage testing of EUV optics using focused radiation from a table-top LPP source

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As a consequence of the steadily increasing EUV powers and radiation doses, damage and degradation testing of EUV optical elements has become an important issue. In this contribution we report on first damage tests on optics and detectors for the wavelength of 13.5nm using a high fluence micro-focus from a laboratory-scale EUV source. The setup consists of a laser-generated plasma from a pulsed gaseous Xenon jet or a solid Au target, respectively. In order to obtain a small focal spot resulting in a high EUV fluence, a modified Schwarzschild objective consisting of two spherical mirrors with Mo/Si multilayer coatings is adapted to the source, simultaneously blocking unwanted out-of-band radiation. By demagnified (10x) imaging of the Au plasma an EUV spot of 5 µm diameter with a maximum energy density of ~1.3 J/cm² is generated at a wavelength of 13.5 nm and a pulse width of 8.8 ns.

We demonstrate the potential of this integrated source and optics system for damage testing on EUV optical elements and sensoric devices. As an example, single pulse ("1-on-1") and multiple pulse ("S-on-1") damage thresholds were determined for Mo/Si multilayer mirrors, using both on-line optical microscopy, interferometry and atomic force microscopy for damage detection. The data are compared with in-situ measurements of the reflectivity change at 13.5nm. Moreover, thin metal coatings (Gold) used as grazing incidence mirrors were irradiated. Threshold energy densities for damage and film removal were determined, showing a linear dependence on the film thickness [1]. Furthermore, EUV-to-VIS quantum convertors (Ce:YAG crystals, phosphor coatings) employed for beam characterization were investigated in terms of linearity, saturation behavior and conversion efficiency.

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7969-78, Poster Session

Plasma-assisted cleaning by metastable atom neutralization (PACMAN): a plasma approach to cleanliness in lithography

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The Plasma-Assisted Cleaning by Metastable Atom Neutralization (PACMAN) cleaning technique being developed in the Center for Plasma-Material Interactions (CPMI) at the University of Illinois at Urbana-Champaign is a dry-non-contact vacuum-based removal technique. The PACMAN process uses a high density helium plasma (ne ~ 1017 m-3, Te ~ 2 eV) to achieve removal of organic contaminants on optical masks, EUV masks, silicon wafers, and optics material used in integrated circuit manufacturing. The PACMAN process is successful at removing both hydrocarbon particles as well as carbon layers by utilizing the high-energy helium metastables in the plasma. The helium metastables, with ~ 20eV of energy, are used to break the bonds of the particle allowing for volatilization or desorption of the atoms/hydrocarbon chains of the particle to achieve an etching-like removal method without using traditional etchant process gasses. With ion energies of ~ 10eV, damage such as surface roughening or surface erosion to the underlying structures being cleaned are avoided. Also, film densification (the removal of hydrogen from a hydrocarbon resulting in a dense carbon layer at the surface of the particle) is avoided in the PACMAN technique due to the absence of high-energy ions which would preferentially sputter hydrogen out of the particle matrix. Preliminary results for the removal of polystyrene latex nanoparticles in the range of 30 nm to 500 nm have shown removal rates of ~ 40 nm/min without damage to silicon wafers. Also, carbon films on silicon wafers have been removed with the PACMAN technique at a rate of ~ 11 nm/min. Current results of cleaning various particle types from surfaces through the PACMAN process will be presented in addition to a theoretical model of the removal process.

7969-79, Poster Session

Broadband spectrophotometry on non-planar EUV-multilayer optics

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Adapted characterization facilities play a major role in the development of optical components for EUV-lithography. In addition to precise measurement techniques of large-scale research centers, especially laboratory-scaled instrumentation gains of importance for a flexible and efficient optimization of multilayer based optical systems in the production line. Although, numerous characterization methods in the EUV spectral region have been established, the spectrophotometric characterization of curved multilayer optics within broad spectral intervals is still a challenging task.

In the present contribution, a reliable and compact EUV-spectrometer adapted for the analysis of curved EUV-optics for near normal incidence applications will be described. Using a specific design for the specimen holder, the limits of both types of samples, convex and concave, can be verified. The capability of the device is confirmed by investigations in the spectral reflectivity of a single EUV-multilayer mirror deposited on a silicon wafer. Its radius of curvature is continuously adjustable, providing a direct comparison of the detected peak reflectivity, peak location and spectral bandwidth in dependence on its curvature. The range of curvature applied is in compliance with optics specifications of current projection systems for EUV-lithography.

The accurate spectral measurement of optics with radii of curvature even smaller than 300mm is achieved by applying a polychromatic approach for the spectrometer. In this new concept, the entrance slit of the spectrograph unit coincides with the focal point of radiation exactly on the sample surface. Aiming for a high spectral resolution, this virtual entrance slit must be preferably small. Using a beam shaping unit based on the Kirkpatrick-Baez principle, the diameter of the focused radiation on the sample surface can be adjusted to the order of just a few tens of microns. Therefore, curvatures of common EUV-optics have a marginal influence on the beam divergence which can be easily compensated by the adaptation of installed apertures. In addition, the small beam diameter even allows for detailed surface mappings which are necessary for an assessment of significant imaging properties, for instance concerning the lateral homogeneity of coatings of EUV optical components.

7969-80, Poster Session

Development of an in-situ Sn cleaning method for extreme-ultraviolet light lithography

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The development of a successful extreme ultraviolet light source for lithography relies on the ability to maintain collector optic cleanliness. Cleanliness is required to maintain the reflectivity of the collector optic thus maintaining the light power output at the intermediate focus. In this paper, an in-situ method is explored to remove Sn from a contaminated collector optic. Hydrogen plasma is used to promote Sn etching while maintaining the integrity of the collector optic's multi-layer structure. The removal rate of Sn is investigated as a function of various operational parameters including chamber pressure, plasma electron density, as well as plasma electron temperature. Initial results are presented using an external RF-plasma source. The use of the collector optic as a RF-antenna is also investigated to optimize the etching rate of the hydrogen plasma. Initial plasma parameter measurements reveal electron densities on the order of 1011-1012 cm-3, with electron temperatures on the order of 1-3 eV. An optimized etch rate of ~125 nm/min off of Si was observed using 1000 W, 80 mTorr, and a flow rate of 50 sccm of H2. These initial measurements are used as a basis for optimizing the etching rate off of the collector optic. Such results are important in allowing the long-term usage of a single collector optic to minimize operating costs involved with replacing the optic, as well as tool downtime.

7969-81, Poster Session

Removal of carbon and tin contamination with low-power downstream plasma cleaning using different gases

G. Morgan, R. Vane, XEI Scientific, Inc. (United States)

In order for extreme ultraviolet (EUV) lithography to make the transition to high volume manufacturing, safe and effective in situ methods for cleaning EUV optics and maintaining vacuum chamber cleanliness must be developed. In last year's Advanced Lithography conference, low power downstream plasma cleaning was shown as an effective candidate for in situ removal of carbon from EUV optics (Proc. SPIE, Vol. 7636, 76361Q (2010); doi:10.1117/12.846386). Room air was flowed past the low power RF plasma, creating oxygen radicals which were then carried by convection to the contaminated optic. The radicals removed the carbon contamination on the optic producing CO2, CO and H2O, which are pumped out of the vacuum chamber.

There is concern that removal of carbon contamination by oxidation may damage the capping layers of the optics. In particular, ruthenium capping layers may be susceptible to reaction with oxygen radicals. The previous experiments with low power downstream plasma were done on silicon capped EUV optics. Also, there is a need to remove tin deposits from EUV optics. Tin deposits contaminate collector optics for EUV Sources and will not be removed by oxygen radicals.

Preliminary data shows that hydrogen radicals can be created using the same low power RF source. These radicals can also remove carbon contamination, although at a slower rate than oxygen radicals. Additionally, plasma with a CF4/O2 gas mixture can also be created by the low power source. This plasma creates fluorine radicals, which may provide a way to remove tin.

This paper will explore the effectiveness of these non-oxygen plasma sources as a means to remove carbon and tin deposits from EUV optics without damage. Cleaning effectiveness will be measured by using a silver coated quartz crystal microbalance (QCM) with an extra layer of carbon on top. The QCM is a sensitive tool for measuring mass changes on a surface. Changes in frequency in the QCM are proportional to the changes the mass on its surface; these changes can be used to determine what chemistry is occurring on the QCM. The combination of silver and carbon coatings should provide a precise means of measuring both the cleaning and oxidizing activity of the downstream plasma process. The QCMs can also be coated with gold and an extra tin layer on top for determination of tin removal by the downstream plasma cleaning process. Additionally, a ruthenium coating layer on the QCM may also be used to test whether or not the cleaning process is harmful to the ruthenium cap found on EUV optics.

7969-82, Poster Session

Narrow spectral bandwidth EUV multilayers: fabrication and performance

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Multilayer films are critical to EUVL optical systems and have many applications in other EUV technologies. For 13.5 nm radiation, Molybdenum and silicon (Mo/Si) multilayers are used ubiquitously because of their high relative reflectivity and good stability. However for applications using high-harmonic sources (plasma-based EUV lasers), for zone-plate based EUV microscopes, a narrower bandwidth is required than is normally achieved with a typical Mo/Si multilayer.

To address the issue of narrower bandwidth requirements, we have investigated two approaches for fabricating multilayers using DC magnetron sputtering. One approach is to reduce and optimize the thickness ratio of molybdenum to silicon in Mo/Si multilayers, and another is to use the second order reflectance from a multilayer with approximately double the standard period. Figure 1 is a performance comparison between two 45 degree Mo/Si multilayers, one coated with typical parameters and the other optimized for narrow band. A factor of 3.5 better bandwidth response has been achieved by reducing the thickness ratio of molybdenum to silicon. Figure 2 shows the reflectivity curves for two Mo/Si multilayers designed for near-normal (85o) reflection. Spectral bandwidth has been reduced from 4.5% to 2% by using the second order, without greatly sacrificing reflectivity. In addition to the methods discussed here, multilayers using other materials suitable for narrow-band EUV have also been investigated.

7969-83, Poster Session

Application of flash-lamp post-exposure baking for EUV resist processing

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EUV lithography (EUVL) is the leading candidate for the manufacture of devices with 22nm node and beyond. However, many challenges remain for the industry to understand clearly and to overcome before EUVL will be ready for application in volume production. Efforts have been made to improve the various critical components of EUVL, such as light source, exposure tool, mask, resist material, and so on.[1] Among these, resist materials are considered as one of the most critical issues in realizing EUVL. For EUV resist materials, the main development issue is how to concurrently achieve high sensitivity, minimal resolution limit and low line width roughness (LWR) in the required fine patterns. At present, sensitivity and resolution continue to be improved through advances in EUV resist material research. However, LWR remains a difficult issues.[2] Thus, the investigation of LWR-reduction from the point of view of resist processing has became necessary.[3] In recent years, some groups have reported resist process enhancements for post-application bake (PAB), post-exposure bake (PEB) in vacuum, and alternative rinse and developer solutions as possible methods for LWR reduction.[2-4] Depending on the type of resist material used in these aforementioned methods, a difference in the resist lithographic performance was observed. Another method for LWR reduction that is being considered is shortening the acid diffusion length of the photo-acid generator (PAG) through the application of PEB processes. This has been shown feasible with the utilization of

sub-millisecond PEB technologies, as reported elsewhere.[5]

In this paper, an investigation on the potential of flash-lamp (FL) PEB process for EUV resist processing is reported. Here, a wafer-heating process utilizing a Xe lamp was applied for instantaneous and full-wafer baking. PEB times as short as few milliseconds are expected with the FL PEB.[6] During the conference, the latest lithographic results obtained with this alternative technology will be discussed.

7969-84, Poster Session

Availability of underlayer application to EUV process

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EUV lithography is one of the most promising technologies for the fabrication of beyond 40nm HP generation devices. It has various advantages including shorter manufacturing turn around time, higher k1 process factor and process extendibility to subsequent generation devices relative to double patterning technologies. However, it is well-known that EUV lithography still has significant challenges. A great concern is the change of resist material for EUV resist process. The resist thickness is below 100nm to avoid pattern collapse and increase resolution. But thin films in this thickness range have a significant impact on etch-process capability. It is well-known that multi-layer film structure is a potential solution. Also, EUV resist material formulations will likely change from conventional-type materials. As a result, substrate dependency needs to be understood.

TEL has reported that the simulation combined with experiments is a good way to confirm the substrate dependency. In this work the application of HMDS treatment and SiON introduction, as an under-layer, are studied to cause a footing of resist profile. Then, we applied this simulation technique to Samsung EUV process. We will report the benefit of this simulation work and effect of underlayer application.

Regarding the etching process, underlayer film introduction could have significant issues because the film that should be etched off increases. For that purpose, thinner films are better for etching. In general, thinner films may have some coating defects. Therefore, we evaluated the coating performance of ultra thin film. We will report the coating coverage performance, defectivity and material consumption capability of thin film coating. Finally, we confirm the resist process performance using an actual EUV resist process. These results are also reported.

7969-85, Poster Session

Development of underlayer material for EUV lithography

T. Endo, R. Sakamoto, R. Ohnishi, B. Ho, Nissan Chemical Industries, Ltd. (Japan)

For the next generation lithography (NGL), several technologies have been proposed to achieve the 22nm-node devices and beyond. Extreme ultraviolet (EUV) lithography is one of the candidates for the next generation lithography. However the high power EUV light sources, defect less multilayer EUV masks and EUV resists with RLS trade-off (R: Resolution, L: LER/LWR, S: Sensitivity) are still the key issues for EUV lithography.

For lithography processes, LWR and resist pattern collapse are the most critical issues because of the small target CD size and high aspect ratio. If we only optimize the formulation of photo resist to solve these issues, it will face to the limitation of improvement. But we apply the EUV under-layer (UL) material and investigate the new process, for example the post patterning rinse, they could have the option to over come these issues. The requirements for UL material shall have the good coating property with thin thickness (< 20nm) on various substrate, the high adhesion with photo resist, the universal resist compatibility, minimize LWR and the enhancement of photo resist sensitivity.

In this study, we design the new concept of EUV UL material to meet these requirements and study the impact of functional group for pattern collapse behavior by using EB/EUV exposure tool. In the same time, the absorbance effect of EUV UL material for lithography performance was also investigated.

7969-86, Poster Session

Study of post-develop defect on typical EUV resist

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This study reports on post-develop defect for EUV resist process. Presently, research and development of EUV resists are continuously being carried out in terms of resolution, sensitivity, LWR.[1] However, in the preparation of EUV lithography for mass-production, research on the reduction of pattern defects, especially post-develop defect is also necessary. As observed during the early stages of resist development for the various lithographic technologies, a large number of pattern defects are commonly coming from the resist dissolution process.

As previously reported, utilizing an EUV exposure tool, we have classified several EUV specific defects on exposed and un-exposed area. And also we have reported approaches of defect reduction.[2]

In this work, using some types developer solution (TBAH, TBAH+, etc) comparing with current developer solution (TMAH), EUV specific defects were evaluated. Furthermore, we investigated the defect appearing-mechanism and approached defect reduction by track process. During the conference, based on these results, the direction of defect reduction approaches applicable for EUV resist processing will be presented.

7969-88, Poster Session

Study of ion implantation into EUV resist for LWR improvement

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Today, application of EUV Lithography (EUVL) for mass-production is considered for the memory devices of 2x nm half pitch. Through the continued efforts to improve the performance of EUV resist, recently many resists show the resolution of less than 25 nm half pitch(1) and breaking the wall of 20 nm is the specific concern.

On the other hand, the progress in line width roughness (LWR) is slower than the expectation. The gap between the current top level resist's LWR performance of ~3 nm and the required value of less than 1.5 nm 3s in ITRS(2) roadmap is large. It is suggested that the post-processes after resist imaging is necessary to achieve better LWR(3). The post-processes such as solvent smoothing, baking, UV cure give the great reduction of LWR(4). But the LWR of the pattern is important after etching rather than after the resist development, so the effectiveness of post-process should be judged after pattern transfer. One of the well known ways to improve the resist etching resistance is the ion implantation(5) .Recently the LWR reduction by the low energy ion implantation for EUV resist is reported(6). However, in those investigations the comparison of LWR only between before and after ion implantation is reported.

In this paper, the authors have performed the ion implantation for the EUV resist patterns followed by pattern transfer. The LWR at each step were measured and compared. The dense line patterns with the half pitch of 32 nm were replicated by the EUV resist with the residual thickness of about 50 nm. The substrate was SiO2 as the transfer film. Ar ion implantation was performed with 30keV of incident energy and with the dose of 1.0E15/cm2. It was found that the etching resistance was improved by the ion implantation and the effectiveness of LWR reduction was larger after etching rather than after ion implantation.

- portion of this work was performed at the IBM Alliance Albany Site.

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7969-89, Poster Session

Development of EUV resist for 22-nm half-pitch and beyond

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Extreme ultraviolet (EUV) lithography is one of the most promising candidates for next generation lithography (NGL), which can achieve 22nmhp lithography and beyond. In order to implement EUV technology, resists are one of the critical items that require significant improvement in overall performance. In order to achieve these improvements, many research groups are developing new materials such as molecular glass (MG), polymer bound photo-acid generator (PAG), high quantum yield PAG, sensitizer and high absorption resin.

In this study, we explored new materials to break the trade-off relationship among resolution, line width roughness (LWR), and sensitivity (further discussions reference the term RLS) and investigated mechanisms to achieve improvements.

7969-90, Poster Session

Acid diffusion measurements based on extreme-ultraviolet resist outgassing

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Critical requirements for resolution, sensitivity and line edge roughness (LER) must be achieved as Extreme Ultraviolet (EUV) resists are developed for High Volume Manufacturing (HVM) lithography. Information on methods to optimize acid diffusion in chemically amplified resists will facilitate the progress towards this resist development. During exposure of these resists to EUV radiation, the photoacid generator (PAG) decomposes to generate an acid which deprotects the polymer. Molecular outgassing of the components originating from the protection group in these photoresists during EUV exposure can reveal vital information about the diffusion of the acid present. The diffusion capability of the acid will influence the rate of deprotection even below the post exposure bake (PEB) temperature. Hence, the rate of outgassing of the protection group component can be correlated to the acid diffusion during and after EUV exposure on different time scales. A set of EUV resists based on PAG's capable of generating acids of different sizes will be tested on system equipped with an EUV source (Energetiq EQ-10M) and an Extrel mass spectrometer. The deprotection from each acid released during the PAG decomposition will be captured by the measured signal from mass spectrometer. Various base loadings will be added to the resist formulations to directly impact the quenching of the acid and thus affect its diffusion length in the polymer. The influence of film thickness on the rate of outgassing of these components will be studied as well. Figure 1 below shows an example of diffusion rates being captured by a mass spectrometer of two species escaping from the photoresists immediately after the EUV source was turned off. The component diffusing faster shows a faster decay rate than the slower diffusing component.

7969-91, Poster Session

EUV lithography for 22-nm half-pitch and beyond: exploring resist resolution, LWR, and sensitivity trade-offs

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The International Technology Roadmap for Semiconductors (ITRS) denotes Extreme Ultraviolet (EUV) lithography as a leading technology option for realizing the 22nm half pitch node and beyond. Readiness of EUV materials is currently one high risk area according to recent assessments. The main development issue regarding EUV resist has been how to simultaneously achieve high sensitivity, high resolution, and low line width roughness (LWR). This paper describes the strategy and current status of EUV resist development at Intel Corporation. Data collected utilizing Intel's Micro-Exposure Tool (MET) is presented in order to examine the feasibility of establishing a resist process that simultaneously exhibits ≤22nm half-pitch (HP) L/S resolution at ≤12mJ/cm2 with ≤3nm LWR. Application of post-processing techniques to reduce LWR will also be discussed.

7969-92, Poster Session

Unraveling the effect of resist composition upon EUV optics contamination

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EUV lithography is the most promising new technology for the next node of semiconductor devices. Unfortunately, the high energy photons are likely to generate more contamination than observed with ArF or KrF light which would reduce the transmission of the EUV optics. Resist outgassing is an important contamination source. However, not enough is known about the way a resist composition influences the contamination growth rate, while this information is crucial to guide the development of EUV resists.

To reduce the knowledge gap, Fujifilm Electronic Materials (FFEM), IMEC and ASML a started a joint effort aimed at systematically exploring the contribution of the different resist components and at understanding the effect of chemical modifications of the different components on the contamination tendency of resists.

The project focuses on:

1. identifying the volatile components outgassing from resist,

2. create an initial correlation between the contamination rate and resist composition,

3. the composition of contamination remaining on the optics surface after cleaning.

The outgassing components are assessed by RGA analysis, the contamination rate is quantified by witness plate testing and the non-cleanable contamination is explored by surface analysis using XPS. Contamination growth is explored using both EUV and e-beam exposures and the results obtained by both these techniques are compared.

To explore the effect of the resist composition upon contamination growth, the following resist components are individually varied:

- polymer matrix and blocking groups,

- quencher,

- and PAG.

In this way the total contamination of a resist can be divided into the separate contributions of the different resist components upon the contamination growth rate, which is a huge step forward in the understanding of optics contamination due to resist.

The Contamination growth dependence upon polymer chain length is

studied in more detail, as it is expected that longer chains will result in less outgassing and therefore less contribution to contamination. As it was already observed that PAG is a major contributor, the effect of PAG on the contamination growth is more extensively explored. The effect of PAG loading, different PAG anions and cations and PAG fixation by polymer binding upon contamination growth is explored. A few examples of results obtained are given below (Figure 1).

The combined results of this investigation will form a solid basis regarding the relation between resist composition and its contamination potential and is therefore very valuable for the development of good resists EUV that do not contaminate much.

7969-93, Poster Session

Acid proliferation to improve the sensitivity of EUV resists

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Extreme ultraviolet (EUV; 13.5 nm) lithography has attracted great attention as a promising next-generation lithography with resolution down to sub-30 nm. Highly sensitive EUV resists are strongly needed to compensate for the low productivity of EUV lithography due to the low power of the EUV light source. Acid amplifiers give additional acid generation through the autocatalytic decomposition in the presence of a strong acid and were recently applied to EUV resists. Herein we report the efficient acid generation by the control of acid proliferation processes in order to improve the sensitivity of EUV resists.

Thin polymer films of poly(4-hydroxystyrene-co-tert-buthylacrylate) (UV3) containing pinanediol-monotosylate (PiTs), -monotriflate (PiTf), or -monomesitylate (PiMe) as an acid amplifier were employed. Irradiation of these films was performed by using EUV radiation (Energetiq Technologies EQ-10M). The films were then baked at 100 – 130 °C and developed in an aqueous 2.38% Me4N+ OH–. Thermal stability of the acid amplifiers in the film was evaluated by UV-vis spectrophotometric titration of pH indicator dye, employing here coumarin 6 (C6). The red shift from C6 to protonated C6-H+ occurs with increasing annealing time, indicating that acid amplifiers self-decomposed by the annealing to give corresponding acid. The PiTs, PiTf, and PiMe were stable up to 110 °C, 90 °C, and 120 °C for at least 90 s, respectively. The contrast curve of the UV3 film containing PiTs after development was examined. Increasing acid amplifier loading leads to improve sensitivity of the resist; the dose to clear (E0) values for 5, 10, 20 wt% of PiTs loading were 1.8, 1.3, and 0.5 mJ cm-2, respectively. It is suggested that the PiTs decomposed autocatalytically in the presence of acids generated from acid generator to give corresponding acids; subsequently, the tert-butyl group was cleaved effectively by the acids. The similar trend was observed with PiMe. Next, the E0 values for the UV3 film containing 10 wt% of PiMe after development were 2.5, 1.8, and 1.1 mJ cm-2 with a post exposure bake (PEB) at 100 °C, 110 °C, and 120 °C, respectively. Such an enhancement of sensitivity indicates the importance of the control of acid proliferation during PEB. EUV lithography imaging studies of the acid amplifying resist are in progress.

7969-94, Poster Session

Studies of acid diffusion of anionic or cationic polymer bound PAG

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As the feature critical dimensions decrease, higher and more requirements are being made of photoresist materials for fabrication of nanostructures. EUV lithography is one of the most important candidates for half-pitch 22nm node device manufacturing and beyond. The main issue for developing EUV resist is to satisfy the ITRS target of sensitivity, line-width roughness(LWR), and resolution simultaneously. However, Resist researchers have difficulty in EUV resist development because they are tradeoff relationships each other. Among them, LWR is closely related to acid diffusion length of photo acid generator. Researchers have tried to accomplish uniform distribution and diffusion minimization of PAG in photoresist film in order to improve LWR. They are mainly using two kinds of method for PAG introduction for uniform distribution and diffusion minimization. One is using sulfonium salts having ultra bulky anion or cation for the acid diffusion suppression, the other is direct incorporation of the PAG into the polymer backbone. In that regard, we have pursued development of a variety of 193nm and EUV CARs that contain photoacid generator(PAG) units covalently bonded directly to the resin polymer backbone. When we consider polymer bound PAG, there can be anionic polymer bound PAG resist, cationic polymer bound PAG resist and nonionic polymer bound resist. In this work, we will discuss diffusion length and line edge roughness(LWR) of these polymers. Acid diffusion length(Ld) and diffusion coefficient(D) were calculated by according to the modified Fick,s equation. As a result of this measurements we knew that diffusion length of general PAG using ArF photoresist was range from a several thousand nm to a several ten nm and PAG diffusion length having bulky anion and cation is range from a several ten nm to a several nm,

In case of polymer bound PAG these values showed under 10nm of diffusion length. We have synthesized a series of polymer bound PAG with different cation size in order to investigate effects of LWR, sensitivity and resolution. Based on these results we show you the data and look into the trend of line edge roughness.

7969-95, Poster Session

Deep ultraviolet out-of-band contribution in extreme-ultraviolet lithography: predictions and experiments

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Extreme ultraviolet lithography (EUVL) sources emit a broad spectrum of wavelengths ranging from EUV to IR. The IR part of the spectrum is filtered by a spectral purity filter (SPF). The DUV contribution mostly filtered by the optics, but a small portion reaches the wafer and will affect imaging performance by exposing the photoresist. Hence it is critical to determine the amount of out of band (OoB) in DUV present in a EUV lithography tool, as well as its effect on the printed features on the wafer.

In this study we investigate the effect of OoB in EUV. A model is developed in order to be able to quantify the DUV/EUV ratio at wafer, and all the input parameters required are estimated in the range from 140 to 400nm, as well as in EUV. The transmission of the optical system was estimated based on the optical design and reflectivity measurements of the mirrors. The mask reflectivity for multilayer (ML) and absorber was measured down to 140nm. The sensitivity in EUV and DUV for a variety of resist platforms was measured at 13.5, 157, 193, 248 and 365nm. The source spectra were measured or estimated from theory. Our results allowed estimating of the DUV/EUV ratio for two ASML tool configurations, the EUV Alpha Demo Tool and the NXE 3100.

The modeling results were compared to experiments on EUV ADT by introducing a methodology able to measure the EUV/DUV ratio at wafer level. To this aim an aluminum coated mask was fabricated and qualified in EUV as well as in DUV. The analysis of dose to clear exposures of a reflective and an absorbing mask in EUV gives an indication of the DUV/EUV ratio. This methodology, apart being used to validate the quality of the modeling, is also used to benchmark the DUV sensitivity of different resist platforms in a simple and effective way as well as to monitor DUV OoB.

7969-96, Poster Session

Understanding the behaviour of laser-produced tin plasma by time-resolved spectroscopy and simulation of their spectra

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Laser-Produced Plasmas (LPP) of tin have been recently proposed as one of the best extreme ultraviolet (EUV) sources for the next generation of EUV lithography in semiconductor industries that requires an intense source within 2% bandwidth of 13.5 nm wavelength. This paper discusses the behaviour of tin LPP from its temporal evolution as well as simulations of the unresolved-transition array (UTA) spectra responsible for the peak EUV emission. A Nd:YAG laser of 1064 nm wavelength, 7 ns FWHM output, operating at 10 Hz was focused on a tin slab target of 3.2 mm thick housed in a stainless steel vacuum chamber evacuated down to ~ 10-6 Torr. An ISAN spectrograph with a 600 lines per mm grating which covers the wavelength range from 10 to 30 nm and a digital camera were employed to record the EUV emission. The tin spectra were captured by a Stanford Research System (SRS) delay generator at times ranging from -15 to +10 ns relative to the laser peak while the MCP detector was gated for a 10 ns window and the tin target was exposed for 5 shots at each time delay to avoid errors associated with laser drilling. The theoretical spectra of the SnVI - SnXIV were calculated by the Cowan suite of codes from which the oscillator strengths and wavelengths (gf,) were used as input to the collisional-radiative (CR), steady state model of Colombant and Tonon, which calculated the fractional ion densities in the plasma. In the Cowan code calculations the scaling factors were chosen to be between 69 to 85 while in the CR model the calculated UTA were weighted according to ion fraction (as a function of electron temperature and density) to simplify the steady state plasma modelling. A wide range of electron temperatures from 20 eV to 50 eV were simulated to fit the experimental results for each time delay in the early stages of the EUV emission after being convolved with Gaussian broadening of 0.53 nm to compensate for the instrumental broadening. The quality of fit was evaluated by a least square analysis. The experimental results show that the development and collapse of the UTA closely match the behavior of laser pulse over time which conforms with our previous results using a shorter wavelength laser. The UTA in-band intensity is found to increase over time while the brightest spectrum is observed around the peak of the laser pulse. In the early stages of the EUV emission (t = -6 ns to t = -1 ns relative to the EUV peak) the electron temperatures are theoretically estimated to be between 35 - 40 eV. The spectra broaden toward longer wavelengths as the plasma cools down which indicates that lower ion stages contribute. This trend gives rise to the self-absorption features near the end of the plasma which, based on the theoretical calculations, are due to SnVI - SnXI. The emission duration from the UTA, determined from the integrated emission over time is found to be ~7 ns. The theoretical calculations also show that the satellite lines which originate from multiply excited electrons slightly broaden the spectra and increase the features at longer wavelengths though they are not obvious in the experimental results primarily due to relatively poor spectrograph resolution.

7969-97, Poster Session

Laser-produced plasma EUV source around 6.7 nm as future EUV source

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In recent years, laser-produced dense plasmas have been focused on as a high efficient and high power source of extreme ultraviolet (EUV) radiation. The EUV emission with a wavelength less than 10 nm has found much interest. This wavelength shorter than 10 nm is especially useful for next generation semiconductor lithography toward the final stage after 13.5-nm EUV source and other applications, such as material science and biological imaging near the water window. In particular, EUV emission at the relevant wavelength is coupled with a Mo/B4C multilayer mirror with a reflective coefficient of 40% at 6.5-6.7 nm.

A Q-switched Nd:YAG laser at 1064 and 532 nm produced a maximum pulse energies of 2 and 1 J with a pulse duration of 10 and 8 ns (full width at half-maximum (FWHM)), respectively. The laser was perpendicularly focused on a planar Gd and Tb targets with a thickness of 1 mm by use of a lens with a focal length of 120 cm. The focused intensity was change ranging from 1010 to 1013 W/cm2 with focal spot sizes from 30 to 300 micron to compare the electron temperature effect at high laser intensity with the plasma hydrodynamic expansion loss effect at large spot diameter. A flat-field grazing incidence spectrometer was used. The time-integrated spectra were obtained by a thermoelectrically cooled back-illuminated x-ray CCD camera.

We observed various spectra of the Gd plasmas at different focal spot diameter and the laser intensities to compare low electron temperature effect and the plasma hydrodynamic expansion loss effect. The laser wavelength was set at the fundamental wavelength of 1064 nm with the laser energy of 2 J. The laser intensity was verified by moving the distance between the focal lens and the target. To achieve the high emission intensity, the focal spot diameter requires the increase larger than 300 micron to reduce the plasma expansion loss. The efficient multi charged ions for 6.5-6.7 nm, on the other hand, should be produced for the electron temperature of 170 eV. These parameters are traded off. The in-band emission at 6.7 nm ± 1% at the spot diameter of 35 micron was observed to be lower than that of at 210 micron. At the spot diameter of 35 micron, the dip around 6.7 nm was appeared. The typical time-integrated EUV emission spectra between 5.5-10 nm Gd ions produced strong broadband emission around 6.7 nm. The spectral in-band emission at 6.7 nm ± 1% was maximized when the focal spot diameter of 210 micron at the balance of two effects. As a result, the spectral in-band emission at 6.7 nm ±1% was maximized when the focal spot diameter of 210 μm (FWHM) at the laser intensity of 4 × 10^11 W/cm^2 at the balance of two effects. As a result, the in-band emission strongly depends on the plasma volume with the low plasma hydrodynamic expansion loss effect. Temporally and spatially integrated electron temperature of the Gd plasma was observed to be 45 eV at this laser intensity. An electron temperature higher than 50 eV was also reproduced in the CR model. We would show and discuss the wavelength dependence on the spectral behavior, conversion efficiency, etc.

7969-98, Poster Session

Counter-facing plasma focus system as an efficient and long-pulse EUV light source

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Recent advances in the field of extreme-ultraviolet (EUV) lithography enhanced expectations for next-generation chips and nanotechnologies; thus, the light source should play a vital role in constructing and inspecting microstructures. Because they are cost effective and simple, EUV light sources based on high-energy-density discharge plasma are advantageous compared to laser-produced plasma and synchrotron light sources. However, despite recent efforts in developing a discharge-produced EUV plasma source, an efficient and stable light source remains to be realized.

Conventional discharge-produced plasma sources emit photons around 13.5 nm 1% (in-band range) through capillary discharges, hollow cathode z-pinches, gas-jet z-pinches, vacuum spark discharges, and plasma focus devices. The extraction of debris-free light is the greatest challenge due to the electrical dissipation into the discharge components, which causes a huge heat load on the electrodes and to high repetition exhausts of plasma. Thus, damages of electrodes and correction mirrors

prevent to realize an efficient and stable light source.

In fast pinching plasma, heating and ionizing the plasma in the early stage of the discharge consume most of the input energy. Because the conventional z-pinch discharge scheme used for EUV plasma is basically one dimensional, the compressed plasma should expand immediately. It cannot confine the plasma for more than a microsecond. In addition, the estimated thermal velocity of EUV plasma is 1 cm/ s. Plasma moving at this velocity tend to move away from the hot region, which prematurely ends a sub-millimeter size EUV plasma in as little as 100 ns. The plasma conversion efficiency (PCE) of a conventional EUV source is dominated by the transient nature with a very short lifetime of EUV plasma. It has been estimated that PCE approaches the spectrum efficiency when the lifetime reaches several microseconds. A recent study indicated that the low conversion efficiency is largely due to the transient nature of the plasma, and that magnetic confinement of the high energy density plasma may realize an efficient EUV source. Therefore, two-dimensional (axial and radial) confinement is required to prolong the lifetime of EUV plasma. Herein a plasma focus device, which is composed of a pair of counter facing coaxial plasma guns, is investigated as a candidate for an efficient and highly repetitive EUV light source.

The prototype plasma focus system consisted of a pair of Mather-type plasma guns. The coaxial electrodes were stainless steel and composed of outer-electrode cylinders with an insider diameter of 10 mm and inner-electrode rods with a diameter of 5 mm. The guns faced the counter electrodes with 4 mm gap spacing. Insulators placed between the cylindrical electrodes provided the initial breakdown currents. The current sheets launched from the insulators advanced axially toward the center gap where they interact with each other. The length between the insulator surface and the top of center electrodes were selected to be 10 mm such that the plasma reached the center of electrodes when the discharge currents were maximized at tpeak. They were driven by pulse power drivers [2 (C=0.8 F, capacitors +L=0.5 H inductors)] with opposite polarities. The outer electrodes were grounded to a common aluminum plate, while the center electrodes received applied high voltages with reversal polarity. The charged voltage were nominally 15 kV, which drove the sinusoidal current pulse with approximately 15 kA peaks and a 1.0 s rise time.

We made thin films of Li or Li compounds on the insulator surface by vacuum evaporation as ionized and light emission materials.

In the conference presentation, we show the experimental results for the maximum PCE and EUV emission plasma size.

7969-99, Poster Session

Development of the reliable 20-kW class pulsed carbon dioxide laser system for LPP EUV light source

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Extreme Ultra Violet (EUV) light source is expected to be used for next generation lithography. For the recent several years the source has been the most critical issue. In addition especially Laser Produced Plasma (LPP) method EUV light source system is expected to provide higher output power (>250 W) in order for scanners to obtain higher throughput. To realize performances such as higher power and high reliability required for industrial use, the main driver laser is one of the key components. Our LPP EUV light source system uses a high power pulsed carbon dioxide (CO2) laser as the main drive laser.

Our approach is a MOPA system based on a small average power pulsed master oscillator and a chain of some power amplifiers. The current MOPA system cannot provide more than 25% of overall operation efficiency. The main reason is an insufficient power level at initial amplifier stages. Also the thermal managements and dynamic stabilities are very important factors to realize the mass-production level reliable laser output.

In this presentation, some of the pressing technical challenges of the LPP laser driver, such as efficiency and stability of operation, are shown.

A new master oscillator system and a pre-amplifier system based on a novel configuration of an RF-excited CO2 laser are the key to high efficiency. Energy efficiency over 40% and multi-kW output from 100W input are predicted and verified in our experimental pre-amplifier. Feasibility of a >20 kW pulsed CO2 laser system is shown by numerical modeling and preliminary test results.

The total length of this laser beam path is longer than 50 meters and the number of optics in the main beam path is more than 100. To operate this laser for mass-production level, there are two major critical items. One is the optical cavity stabilities. The operation pattern is burst mode such as 1000 msec on and 500 msec off for die exposure, also several second off for cassette change. To stabilize these intermittent operation mode, laser cavity and optics thermal distortion need to be suppressed within the required level. All mirrors are made by low thermal expansion coefficient materials and windows are made by low dn/dT materials. Also some compensation optical systems are equipped inside the beam path. At the same time, the dynamic stabilities have to be considered for obtaining stable beam performance. There are many vibration sources in the system itself and outside the equipment. All mechanical components have to be designed under these conditions to avoid the sympathetic vibration. As pointed out above, to realize the industrial ready pulsed CO2 laser system, all functions should be worked together. Initial performance and long time operation date are shown based on test results.

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7969-100, Poster Session

Characterization and optimization of tin particle mitigation and EUV conversion efficiency in a laser-produced plasma EUV light source

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An extreme ultraviolet (EUV) light source of 13.5 nm has been developed for next generation lithography. A promising method to generate in particular the required high output power of over 250 W is a laser-produced plasma (LPP) with a tin droplet target and a pulsed CO2 laser.

A tin plasma is an efficient generator of 13.5 nm EUV light. On the other hand, deposition of tin particles which strongly affects EUV mirror lifetime is a critical issue for long-term stable operation of the high-power EUV light source. Tin particles, also called “debris”, consist of energetic plasma ions and neutrals, and fragments. We have demonstrated effective guiding and mitigation of charged particles generated from tin plasma in a strong magnetic field. In this configuration, a high ionization degree of the tin particles enhances the guiding. An effective way to obtain high ionization and therefore high mitigation performance is to supply smaller droplets with a diameter of 10 micrometer. However, there is a possible risk that the EUV conversion efficiency (CE) decreases for smaller droplets. In order to maintain a high EUV CE, precise control of laser irradiation conditions is required.

A compact EUV generation system is employed for basic investigation of

EUV light generation and tin particles mitigation. This system simulates the same conditions, for example pulse width and pulse energy of a CO2 laser, tin droplet size and magnetic field, as the high-power EUV light source we develop except for the pulse repetition rate. Because of the compactness of the system it is easy to measure and optimize many irradiation parameters. These basic measurements contribute to the development of the high-power production machine and to the basic design for further EUV power scaling together with theoretical calculations.

The compact EUV system mainly consists of a short-pulsed high-energy CO2 laser with a repetition rate of 10Hz, a tin droplet generator and a EUV vacuum chamber with a solenoid magnet. Tin ions, neutral atoms and fragments can be measured separately. A highly sensitive tin particle measurement technique is needed to determine the optimum mitigation condition. For this reason a laser induced fluorescence (LIF) system is installed to measure the rarefied tin neutrals. Characterization of EUV light is also possible simultaneously with EUV detection and imaging tools in the chamber. In this conference we will report details of experimental results and discuss the optimization of particle mitigation and EUV CE.

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7969-101, Poster Session

Development of debris-mitigation tool for HVM DPP source

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Debris-mitigation tools (DMTs) have been used in DPP sources and the performance has been well proven in alpha sources. In beta and HVM sources, requirement to the DMT is increasing to fulfill the power and lifetime requirements simultaneously. In order to bring DPP technology into HVM level, a high-performance DMT has been developed. It has high mitigation performance for both neutral and ionic debris, large collection angle of the collector having high optical transmission, and withstand large thermal input from the discharge source head. Experiments were carried out using mirror samples and proved sufficient performance with which no sputtering and deposition were observed.

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7969-102, Poster Session

The effect of pre-pulses on EUV and ion debris emission from laser-produced Sn plasmas

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The current method of optical lithography as a technique for semiconductor fabrication is soon to be replaced by the extreme ultraviolet (EUV) lithography technique, which operates at a peak wavelength of 13.5 nm with a 2% bandwidth. Laser-produced plasmas (LPP), the generation of plasmas by the intense laser irradiation of a target material, are considered a leading candidate for the EUV light sources. Among various target materials evaluated, Sn has demonstrated the best conversion efficiency of laser energy to in-band EUV light. However, Sn plasmas also generate a great amount of ionized and atomic debris that can impede the reflectivity of the expensive collector optics in the EUV lithography system through ion/atomic deposition and implantation. An in-depth characterization of this debris is a much-needed first step in the development of effective debris mitigation systems without much loss of EUV photons. The pre-pulsing of a LPP typically provides a higher x-ray and EUV yield. We investigated the EUV and ion emission features from reheated Sn LPP. Planar slabs of pure Sn were irradiated with either 10.6 micron, 35 ns CO2 laser or 1.06 micron, 6 ns Nd:YAG laser, to create plasmas which are then reheated by CO2 or Nd:YAG laser pulses to prolong the EUV emission. We studied the optimized delay time between the production and the reheating beams in order to maximize the conversion efficiency of the EUV output, in orthogonal and collinear reheating schemes. A Faraday cup is used to determine the ion flux and the kinetic energy distribution of the ionized Sn debris.

7969-103, Poster Session

Sn film and ignition control for performance enhancement of laser-triggered DPP source

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A laser-triggered DPP source is being developed and showing considerable progress toward HVM. Performance, in terms of power and lifetime, of DPP sources has been proven by long-term usage in lithography development fields. Since high-performance debris-mitigation tools are used in DPP sources, collector lifetime is not an issue. However, it is worth developing the technology to enhance overall lifetime of the collector module. In order to suppress both neutral and ionic debris, two technologies, which can be simultaneously used in a DPP source, have been developed. First, a precision control of trigger laser leads to significantly low amount of fast ions which could cause sputtering of the collector. Second, an active control of liquid tin layer, which acts as a fuel material and cooling medium, reduces particle debris and lowers the load on a debris-mitigation tool. Implementing these technologies is considered to provide enhancement of the lifetime of the collector module. In addition, it supports power scaling toward HVM level because it enables increase of pulse repetition frequency and conversion efficiency as well.

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7969-104, Poster Session

Stable tin droplets for LPP EUV sources

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The leading candidate technology for the manufacturing of the next generation semiconductor devices is extreme ultraviolet lithography (EUVL). The 13.5nm radiation (2% bandwidth) can be generated from a Laser-Produced Plasma (LPP). Tin-based LPPs formed using a high power (kW) laser, are highly emissive in this wavelength window.

A key component of EUV LPP sources is the droplet generator. Small tin droplets are mandatory for long-term operation, as they form a regenerative target. Tin droplets present high conversion efficiency (CE) and can be synchronized with the pulsed lasers used for EUVL. EUV sources are required to have stable emission. The overall source stability directly correlates with the stability of the fuel delivery system.

The main requirements for a tin droplet generator are reproducible droplet size and circularity, controllable droplet speed, droplet train stability, as well as long-term operation. Small tin droplets minimize the amount of debris by only delivering the number of radiators needed for EUV emission to the target irradiation site. The CE of an EUV source directly depends on droplet stability. Droplet stability is statistically assessed in time and space: the vertical jitter between droplets, the mean droplet train drift, as well as the deviations from the droplet train mean are studied. The long-term operation is achieved by the tin conditioning system, including refilling.

This paper provides an overview of the main characteristics of the droplet generator, which is a fully in-house developed system. The tin conditioning and dispensing units are described. Then the generator performance is detailed using multiple diagnostics. One of the applied instruments is a macroscopic lens, which, combined with a high speed flash lamp, allows single droplet resolution, see Fig.1. Droplet size and circularity distributions, as well as droplet velocity distributions are mapped for different operating conditions, together with the droplet train stability at the target irradiation site. During operation, the main input parameters are the excitation function and repetition rate, the reservoir backpressure and the generator temperature. Additionally different ranges of vacuum level, nozzle orifice diameter and distance nozzle- irradiation site are studied. The droplet quality is derived at each operating point. Then the obtained results are assessed in the context of the droplet generator requirements for use in an EUV source, with a focus on the implications for source stability. As a conclusion, the resulting generator performance meets the EUVL source requirements for metrology as well as lithography applications.

7969-105, Poster Session

EUV brightness, stability and contamination measurements at the intermediate focus module

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The manufacturing technology for the next generation semi-conductor devices will be based on extreme ultraviolet lithography (EUVL) using a laser produced plasma (LPP) as a candidate 13.5nm light source. EUV sources must be stable, energy efficient and meet the power requirements at intermediate focus. Additionally the plasma debris load must be minimized without compromising the radiation intensity. One challenge of EUVL is the development of a source with contamination-free intermediate focus (IF) that fulfills the required stability, brightness and number of operating hours.

In the first part of the present work, the brightness of the EUV source is calculated from the measured power and the measured spot dimension. The central challenge in this part of the work is to optimize the stability and the brightness of the EUV signal coming out of the source. This challenge is addressed in experiments conducted in the plasma science facility at ETH Zurich. The LPP is formed from the interaction of a Nd:YAG laser and tin target inside a spherical vacuum chamber of inside diameter 800 mm. The EUV intensity and average radiation fluxes can be simultaneously acquired in the facility. The time dependent EUV intensity is collected with a EUV power-meter. A quadrupole mass spectrometer together with ion detectors are used to monitor target ions (Sn species) and to measure kinetic energy distributions. Within the vacuum chamber, due to the modular design of the facility a collecting system or a number of supports for witness plates can be installed; thus it is possible to characterize, in an angular-resolved manner, phenomena including LPP-surface interaction, debris deposition and heat loads.

The stability is measured over a 1 hour period and over a 1s, and 0.4s period. A parametric study is conducted varying the laser power and the droplet dimension for both the stability and the brightness measurements. The dimension of the spot, instead, is measured with a CCD camera sensible in the EUV range, and it is compared with the results of a ray tracing software.

In the second part of the present work, the contamination after the IF is measured and compared with the contamination before IF. The measurements are taken to prove that the intermediate focus module can work as an interface between the EUV source and the next stage. The contamination is measured and monitored over 1 hour running periods in different positions of the module.

7969-106, Poster Session

Characterization of the Sn-droplet EUV source at the LEC, ETH

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Extreme Ultraviolet Lithography (EUVL) is a leading candidate for the future development of smaller and faster microchips with feature sizes of 32 nm or less. Tin laser-produced plasmas (LPPs) are the most promising source of in-band radiation for EUV lithography and inspection applications. However, ions emitted from these LPPs may cause significant damage to components, specifically the collector optics. Tin-droplet targets have the ability to supply the minimum mass required to generate the EUV radiation, leading to substantial decrease in the amount of generated debris. Metrology applications require a compact laser-plasma source that will generate broad EUV radiation at minimum cost.

At the Laboratory for Energy Conversion, ETH Zurich we have developed a high brightness, low etendue and high irradiance EUV source. Absolute intensity measurements of the EUV radiation formed using the droplet target have been recorded. The measurements were recorded over 2 pi steradian with respect to the plasma. The droplet generator, a fully in-house developed system (Figure 1), was synchronized with a Nd:YAG laser (operating at the fundamental frequency) at a frequency of up to 20 kHz. A laser triggering system has been developed to trigger the laser pulse for each individual droplet.

The laser pulse was focused to a power density of 1E11 W/cm2 to maximize in-band emission. The EUV detector employed was a calibrated energy monitor, mounted on a custom built robotic arm (Figure 2). This enabled the recording of the EUV emission from the plasma over a full hemispherical region. The spatial profile and stability of the plasma were measured at a range of angles with respect to the plasma. A comprehensive study of the out-of-band (OOB) radiation from the source has also been carried out using a Phystex Energy Monitor, a calibrated filter/photodiode detector.

In summary, the data presented shows a full 3-dimensional distribution of the EUV emission and conversion efficiency from the tin droplet source, the spatial profile of the plasma in the EUV and OOB wavelength regions, the angular distribution of the OOB radiation in the 200 to 1000 nm range and the stability of the source.

7969-107, Poster Session

Improvements in the EQ-10 electrodeless Z-pinch EUV source for metrology applications

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Now that EUV lithography systems are beginning to ship into the fabs for next generation chips it is more critical that the EUV infrastructure developments are keeping pace. Energetiq Technology has been shipping the EQ-10 Electrodeless Z-pinchTM light source since 1995[1]. The source is currently being used for metrology, mask inspection, and resist development[2,3,4]. These applications require especially stable performance in both output power and plasma size and position.

Over the last 5 years Energetiq has made many source modifications which have included better thermal management as well as high pulse rate operation [5]. Recently we have further increased the system power handling and electrical pulse reproducibility. The impact of these modifications on source performance will be reported.

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7969-108, Poster Session

Investigation on the interaction of long-duration Nd:YAG laser pulse with Sn plasma for an EUV metrology source

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A several-watt EUV source with high average brightness is required for EUVL metrology to perform actinic inspection of masks, photo-resists, and wafers with sub-nanometer spatial resolution. Because of the requirements of small emitter size (smaller than 30 μm) to achieve high brightness, laser-produced plasma with a tiny focal spot provides an ideal EUV metrology source. A laser with pulse duration less than 1 ns, e.g. 100 ps, is most commonly considered as the laser driver for a metrology source in order to avoid expansion of the EUV source due to thermal expansion of the EUV plasma, which is believed to be proportional to pulse duration. However, sub-ns lasers suffer the following limitations when operated at the kW level: (1) high cost of ownership, (2) poor laser beam quality due to nonlinear effects, and (3) no industrial experience operated with high duty factor. In addition, the intense spike of EUV light due to the short laser pulse duration limits the maximum average EUV power applied to the mask and photo resist, etc. We present efforts to clarify the feasibility to apply a long duration Nd:YAG laser to a metrology EUV source.

It was found that an almost constant conversion efficiency is obtained from Sn plasmas irradiated with a Nd:YAG laser with pulse durations from 10 to 30 ns. We also showed that CE is constant with pulse durations from 130 ps to 15 ns. It was found that Sn ions with much less kinetic energy were observed with a 30 ns laser pulse as compared with that of a 7 ns pulse due to the lower laser intensity and the longer rising laser slope. The measurement on the in-band EUV imaging showed that EUV source size depends on laser intensity instead of pulse duration and small EUV size is still possible with pulse duration as long as 40 ns.

This research shows that an efficient and bright EUV source is feasible with a long pulse duration Nd:YAG laser. The lower peak intensity of EUV emission due to the long pulse duration makes the EUV source more suitable for EUV metrology. Moreover, the application of long duration (longer than 30 ns) Nd:YAG laser has several important advantages as compared with sub-ns laser, (a) lower cost due to the simpler laser structure, (b) better laser beam quality due to the smaller B-integral, which is proportional to laser intensity, (c) more reliable operation with high duty factor, and (d) more efficient reduction in target debris from the plasma.

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7969-110, Poster Session

Lifetime of EUV optics under pulsed source

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One of the most promising technologies for next generation device manufacturing is extreme ultraviolet lithography (EUVL), which uses 13.5 nm wavelength radiation generated from free-standing plasma-based sources. Degradation of EUVL optics due to radiation induced carbon growth and surface oxidation in vacuum systems is a well-known effect that not only reduces system throughput through the associated reduction in EUV reflectivity but also introduces wavefront aberrations that compromise the ability to print uniform features. In this paper we present several potential solutions towards an improvement of optics lifetime such as the selection of optimal capping layers for oxidation protection, the mitigation of carbon growth and the development of efficient cleaning techniques that do not degrade the multilayer surface.

Radiation induced carbon growth on surfaces of Mo/Si multilayers with different capping layers (TiO2 and Ru) has been studied under EUV-exposures in a tert-butyl benzene (TBB) atmosphere in a pressure range of 10-8 - 10-6 mbar at the Exposure Test Stand (ETS) using a pulsed Xe-discharge source. The simultaneous exposure of two samples (TiO2 and Ru) with a maximum peak intensity of 1 mW/mm2 and a large exposed area (> 15 mm2 on each sample) was suitable for a detailed surface study by conventional characterization techniques (Fig. 1, left). The carbon growth rate for various partial pressures of TBB was extracted from EUV-reflectivity losses (Fig. 1, right), SE- and XPS-data. The carbon growth rates under pulsed versus quasi-continuous synchrotron sources with similar exposure conditions (intensity and partial pressure) will be compared and analyzed.

Radiation-induced carbon contamination and removal experiments on Ru- and TiO2-capped Mo/Si multilayer mirrors have been conducted at the ETS. Carbon contamination layers with thickness of > 5 nm (Fig. 2) were created by low-dose exposure (~ 5 J/mm2) in TBB-atmosphere at a pressure of 3x10-3 mbar. EUV exposures with a radiation intensity of 0.25 - 1.0 mW/mm2 in different atmospheres (H2, O2...) were used for both: mitigation of carbon growth and surface cleaning of previously contaminated multilayer mirrors. The effect of the EUV-intensity, the cleaning-gas, and the capping-layer material on the degradation and cleaning mechanisms will be discussed.

Special efforts were focused on the investigation of surface cleanability by EUV-exposure in a high-pressure hydrogen atmosphere. It will be shown that the TBB-cleaning rate under EUV-exposure with an intensity up to 1.0 mW/mm2 and a hydrogen pressure up to 1.0 mbar is extremely low and insufficient for practical application. To enhance the cleaning efficiency of hydrogen it was suggested to use a mixture of hydrogen and inert gas (He, Ne and Xe) which has a considerably higher absorption cross section than hydrogen and is therefore much easier excited by the EUV radiation. The first results of this study will be presented and discussed.

This work is supported by Intel.

7969-111, Poster Session

Next-generation of Z* modelling tool for high-intensity EUV and soft x-ray plasma sources simulations

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In the practical requirements for EUV sources for lithography HVM the average EUV power at IF is demanded higher than presently available. At the same time, for actinic mask blanks, patterned mask and in-situ inspection tools, EUV sources of moderate power but very high brightness are required. In practice, the complicated plasma dynamics and self-absorption of radiation limits the in-band EUV radiance of the

source plasma, and the etendue constraint limits the usable power of a conventional single unit EUV source. Under those conditions one of the primary goals in the development of EUVL is the modelling of plasma-based light sources created by intense lasers and high-current pulsed discharges. The 2-D computational code Z* and its commercially available version Z*BME were designed by EPPRA to model multicharged ion plasmas in experimental and industrial facilities using a radiative magnetohydrodynamics (RMHD) approach; however, 3D electromagnetic field, recent advances in atomic physics and the need for spectral and angle-resolved 3-D analysis of radiation and fast particle emission have restricted its use. A new generation of the computational code Z* is currently developed under international collaboration in the frames of FP7 IAPP project FIRE for modelling of multi-physics phenomena in radiation plasma sources, particularly in EUV band, to include improved atomic physics models and full 3-D plasma simulation to evaluate plasma dynamics, spectral emission and the generation of fast charged particles, neutrals. Such modelling can be the key factor in EUV source optimization and will considerably contribute to solving current EUVL source problems as well as extending their application to subsequent nodes (16nm and beyond) and shorter wavelength radiation applications. The radiation plasma dynamics, the spectral effects of self-absorption in LPP and DPP and resulting conversion efficiencies are discussed. The generation of fast electrons, ions and neutrals is considered. Conditions for the enhanced radiance of highly ionized plasma in the presence of fast electrons are evaluated. The modelling results are guiding a new generation of multiplexed sources being developed at NANO-UV, based on spatial/temporal multiplexing of individual high brightness units with fast micro-plasma pulsed discharge, to deliver the requisite brightness and power for both actinic metrology and lithography applications.

7969-112, Poster Session

Laser-produced plasma lightsource for EUVL

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EUV Lithography is the front runner for next generation critical dimension imaging after 193 nm immersion lithography for layer patterning below the 32 nm node; beginning in 2013 according to the International Technology Roadmap for Semiconductors (ITRS). NAND Flash devices are expected to have the need for this manufacturing technology as soon as 2011, with pilot line system introduction starting this year (2010). The availability of high power 13.5 nm sources has been categorized as high risk and ranked as critical with other technologies requiring significant developments to enable the realization of EUV lithography. High sensitivity photoresists with good line-edge-roughness (LER) and line-width-roughness (LWR) are needed to keep the required source power within reasonable limits. Photoresist sensitivity and other light absorbing elements are the basis to derive EUV source power requirements within the usable bandwidth (BW) of 2 %. Scanner manufacturers are requiring clean EUV power close to 200W at the intermediate focus (IF) to enable > 100 wph scanner throughput assuming 10 mJ/cm2 photoresist sensitivity. The need for a Spectral Purity Filter (SPF) increases the requirements for Raw EUV Power even higher. Clean EUV Power is calculated by taking the Raw EUV power and subtracting the losses associated with the Spectral Purity Filter (SPF) and dose control, for initial sources these losses are estimated to be 35% and 20% respectively. A scalable EUV source architecture is needed to enable the evolution of EUV lithography during the life cycle of the technology. Laser-produced-plasma (LPP) sources are expected to deliver the necessary high power for critical-dimension high-volume manufacturing (HVM) scanners for the production of integrated circuits in the post-193 nm immersion era.

7969-113, Poster Session

Tabletop coherent EUV source for mask metrology

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As EUV lithography advances towards production, EUV sources for metrology applications such as actinic mask inspection will be required. Coherent EUV metrology sources have the advantage that they can be used both for interferometric and imaging inspection techniques. In the case of imaging, coherent sources can exploit the exciting potential of lensless imaging techniques that can achieve diffraction-limited spatial resolution in a simple, robust, geometry.

KMLabs' XUUS is a recently-developed coherent EUV source that fits on a tabletop. It is based on high harmonic upconversion (HHG) of a near-infrared (IR) ultrafast laser such as Ti:sapphire to generate EUV wavelengths. HHG is an extreme version of 2nd, 3rd etc. harmonic generation in crystalline materials. To reach EUV wavelengths around 13.5 nm, the 61st harmonic of the fundamental Ti:sapphire laser (800 nm) must be produced. In XUUS, HHG occurs inside a custom gas-filled waveguide structure.

Two engineering advances have enabled KMLabs to advance XUUS from a basic physics curiosity to brightness levels for practical imaging and metrology applications. These are the development of commercial high average power tabletop ultrafast drive lasers with push-button cryogenic cooling, and the process of phase-matching in gas-filled hollow waveguides to efficiently generate in-band EUV light. These two engineering breakthroughs that are embodied in the XUUS EUV source: it comprises a state-of-the-art 20 fs-class ultrafast Ti:sapphire laser amplifier system, coupled with the XUUS phase-matched HHG capillary system. Figure 1 shows the interior of the compact, packaged, XUUS system. It can be used with various gases including krypton, xenon, argon, helium, and hydrogen to access different wavelengths in the 13 to 50 nm range. Conversion efficiencies from the 800 nm drive laser to EUV wavelengths are around 10-4 to 10-6. These values seem modest when compared to tens of % efficiency that can be obtained for conversion to 2nd - 4th harmonic in crystals. But, nonetheless, the XUUS can generate fully coherent light with a useful flux of 1012 photons per second at 40 - 60 eV; a brightness comparable to that from a synchrotron source.

Current efforts to further increase the EUV flux will be discussed. In exciting recent research, the XUUS wavelength range was extended to < 3 nm, using mid-infrared lasers to drive the HHG process. Finally, applications in nanoscale heat transport, nano-imaging and magnetics will be highlihghted.

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7969-114, Poster Session

Overlay accuracy of EUV1 using compensation method for nonflatness of mask

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Extreme-ultraviolet lithography (EUVL) is a promising candidate for the fabrication of ULSI devices with a half pitch of 22 nm and beyond. Since

EUVL uses a reflective mask, image placement (IP) errors arise when a mask is not flat; that is, EUVL requires super-flat mask substrates. However, it is difficult to fabricate mask blanks that have both good flatness and a low defect density. One way to mitigate the flatness requirement is to correct the pattern data for the EB mask writer to compensate for IP errors caused by the nonflatness of a mask. In this study, we used the EUV1 full-field scanner to evaluate the effectiveness of this compensation method.

The EUV1 was installed at Selete in 2007. The maximum field size is 26 mm x 33 mm. The EUV light source is Xe-fueled discharge-produced plasma (DPP). EUVL masks consist of a 51-nm-thick LR-TaBN absorber layer, a 10-nm-thick CrN buffer layer, a 40-pair Mo/Si multilayer, a mask substrate of low-thermal-expansion material (LTEM), and a backside conductive layer. We made two EUVL masks using the compensation method called grid matching correction for thickness variation (GMC-TV), which was developed by NuFlare Technology; and we used the EUV1 to evaluate the resulting overlay accuracy. One mask was quite flat, with the flatness variation of both surfaces being less than 100 nm. The other was non-flat, with the variation being greater than 200 nm. Since the reproducibility of the flatness of a chucked mask is better than 30 nm in the EUV1, the intra-field overlay errors without linear components are less than 2 nm (3s) for the same mask. In contrast, the errors were about 3 nm (3s) for the two masks. The main cause of this degradation in overlay accuracy might be the difference in mask flatness. Using overlay patterns corrected by a method that compensates for mask nonflatness reduced the overlay errors to about 2.5 nm (3s). Although the change was small, the compensation method was found to improve the intra-field overlay accuracy of the EUV1.

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7969-115, Poster Session

EUV processing investigation on state-of-the-art coater/developer system

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In order to further understand the processing sensitivities of the EUV resist process, TEL and imec have continued their collaborative efforts. For this work, TEL has delivered and installed the state of the art, Clean Track, LITHIUS Pro for EUV coater/developer to the newly expanded imec 300mm cleanroom in Leuven, Belgium. The exposures detailed in this investigation were performed off-line to the ASML Alpha demo tool. As EUV feature sizes are reduced, is it apparent that there is a need for more precise processing control, as can be seen in the LITHIUS Pro for EUV. In previous work from this collaboration, experiments were performed on an ACT12 coater/developer. The initial investigations from the ACT12 work showed reasonable results; however, certainly hardware and processing improvements are necessary for manufacturing quality processing performance. To understand the current level of the LITHIUS Pro for EUV, evaluations for critical dimension uniformity and defectivity were performed on the imec baseline resist as well as investigations into the reduction of line width roughness and pattern collapse.

7969-116, Poster Session

Holographic Fourier-synthesis custom-coherence illuminator suitable for 0.5-NA extreme-ultraviolet micro-field lithography

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Synchrotron radiation is a coherent, debris-free radiation source suitable for extreme ultraviolet (EUV) microfield exposure tools (METs). There are two basic challenges when dealing with coherent light for general imaging applications: achieving uniform illumination and obtaining the desired pupil fill (partial coherence factor). This paper describes a two-stage system meeting both of these criteria that is suitable for use in a 0.5 numerical aperture (NA) EUV MET employing synchrotron radiation.

The first stage of the illuminator is uniformity stage, designed to create a uniform illumination footprint across the entire field from an arbitrary input intensity profile. Shown in Figure 1 (optics 1 and 2) , the uniformity stage is comprised of a square-wave-carrier phase-only EUV holographic optical element (HOE) [1] implemented as a programmed diffuser and a collection optic to redirect the +1 and -1 diffraction orders from the HOE towards the second stage of the illuminator. To eliminate fringes in the far-field overlap region, one branch of the collection optic is offset by the 500-nm illumination coherence length, ensuring that fringes from different spectral elements (colors) are spatially shifted enough to make the net fringe contrast vanish.

The second stage of the illuminator (optics 3 and 4) is a two-axis scanning galvanometer that manipulates the angle that the incoming radiation strikes the object during the exposure [2]. Mutual incoherence of the various angles is ensured through the scanning process by virtue that none of the angles coexisting in time. By varying the illumination angle during the exposure, any desired pupil fill can be achieved. In addition, the scanning mirror is imaged to the object to ensure stationarity of the pupil fill across the field. This work was funded in part by SEMATECH and supported by the Director, Office of Science, of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231.

7969-117, Poster Session

Lateral shearing interferometry for high-resolution EUV optical testing

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Next generation EUV optical systems are moving to higher resolution optics to accommodate the smaller length scales targeted by the semiconductor industry. As the numerical apertures of the optics become larger, it becomes increasingly difficult to characterize aberrations, which broaden the point-spread function and thus limit the resolution of an optical system. Conventional interferometric techniques such as point-diffraction interferometry (PDI) are difficult to realize experimentally because of the small spatial filters which are nearly impossible to fabricate and have poor photon throughput.

Lateral shearing interferometry (LSI) provides an attractive alternative to PDI because of its experimental simplicity, stability, relaxed coherence requirements, and ability to theoretically scale to high numerical apertures2. LSI is a type of common-path interferometry whereby the test wavefront is incident on a low spatial frequency grating which causes the resulting diffracted orders to interfere on the CCD. LSI eliminates the need for a high quality spatially coherent reference wave by interfering the test wavefront with a shifted (sheared) copy of itself. The reconstructed phase approximates the derivative of the wavefront in the direction of the shear.

LSI has been used at lower numerical apertures with great success. However, moving to higher numerical apertures presents new challenges. Wavefront distortion from the diffraction grating creates systematic aberrations that have no simple analytic model. The large spectrum of angles makes carrier-frequency based interferogram analysis extremely difficult which may force a phase-shifting approach to the analysis. High numerical apertures create stricter tolerances for the alignment of the optical elements.

In this paper, a new analytic method is presented based on a holographic construction of the LSI setup. Historically difficult to perform in simulation, numerical computations of high numerical aperture propagation are made feasible by an 80-core supercomputer that verify the validity of the analysis. A visible light mockup is created to confirm the results of the simulation.

7969-118, Poster Session

Extensibility of extreme-UV lithography

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Extreme-UV (EUV) lithography is regarded as one of the most promising candidates for the mass production of logic integrated circuits beyond the 20-nm generation. As pursuers of this promising technology, we want to ensure its extensibility so that all investments on its infrastructure are rewarded and Moore's law extended for more than one or two generations. By simulation and experimental evidence gathered so far, we conclude that soon-to-be-available EUV exposure tools with NA=0.32 are capable of delineating features down to the 32-nm minimum pitch. Since the next-generation exposure tools are still in the design phase, we would like to identify their optimal numerical aperture (NA) by considering requirements from not only resolution but also the lithographic process window.

By process window, we mean EL, DOF, and MEEF. If we start with the nominal NA=0.45, then for the minimum pitch of 22 nm, the process window of horizontal lines is very small, accompanied by high MEEF. This results from the shadowing effect due to the chief ray angle of incidence at the object side (CRAO) being not equal to zero, and cannot be resolved by simply biasing the dimension on mask (DOM) of these features. If we increase the NA, MEEF can be reduced and EL can be increased. However, these improvements saturate beyond NA=0.55~0.60. This is because when we increase the NA, the CRAO needs to be increased accordingly, resulting in a more severe shadowing effect. If we reduce the absorber thickness, MEEF can be reduced. However, EL is correspondingly reduced due to an increase in residual reflection from the absorber. Besides, we find that acid diffusion length in resist plays an important role in the MEEF.

In this paper, we will discuss the optimal NA for the 22-nm minimum pitch by taking into account all these factors, and possible methods to enlarge the process window.

7969-49, Session 11

Performance validation of ASML's NXE:3100

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With the shipment of the NXE:3100 to Semiconductor Manufacturers, we enter the next phase in EUVL implementation for IC manufacturing. Since 2006 process and early device verification has been done using the two Alpha Demo Tools (ADTs) located at Leuven, Belgium at IMEC and Albany, New York, USA. With the shipment of the NXE3100 to IC manufacturers, the focus will shift to the integration of EUVL exposures tools into a manufacturing flow, preparing high volume EUVL manufacturing expected to start in 2012.

The NXE is a multi-generation TWINSCAN platform with an exposure wavelength of 13.5nm, and features reflective optics and dual stages operating in vacuum. The NXE:3100 is the first generation of the NXE platform. With 0.25 NA projection optics, a planned throughput of 60WpH and dedicated chuck overlay of 4nm, it is targeted at EUV implementation for 27nm hp and below. The second and third generation 0.32NA NXE tools, include off-axis illumination for high volume manufacturing of resolutions down to 16nm hp and a throughput of >150WpH.

While last year's NXE:3100 paper focused on module performance including optics, leveling and stages, this years update will, in detail, assess imaging, overlay and productivity performance of completed systems. Based on data obtained by our own development program and in joint work with customers we will assess the readiness of the system for process integration at 27nm hp and below. Imaging performance with both conventional and off-axis illumination will be evaluated. Although single exposure processes offer some relief, overlay requirements continue to be challenging for exposure tools. We will share the status of the overlay performance of the NXE:3100.. Source power is a key element in reaching the productivity of the NXE:3100 - its status will be discussed as well. We also will review the reliability performance of this 1st generation for the NXE platform after its first period of operation.

Looking forward to high volume manufacturing with EUV we will update on the design status of the NXE:3300B being introduced in 2012 with a productivity target of 125wph.. Featuring a 0.32NA lens and off-axis illumination at full transmission, a half pitch resolution from 22nm to 16nm will be supported. In order to ensure a solid volume ramp-up the NXE:3300B will be built on as many building blocks from the NXE:3100 as possible making optimum use of the NXE platform concepts.

An outlook to even higher NA systems will complete the paper.

7969-50, Session 11

Tin DPP source collector module (SoCoMo) ready for integration into Beta scanner

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For cost-effective high volume manufacturing (HVM) of semiconductor devices, high power EUV light sources are needed to drive industrial EUV (extreme ultra-violet) lithography applications. XTREME technologies and EUVA have jointly developed tin based DPP (Discharge Produced Plasma) source systems during the last two years for the integration of such sources into scanners of the latest and future generations. Goal of the consortium is to enable this EUV source technology for the tool manufacturers on schedule.

A first Beta EUV Source Collector Module (SoCoMo) containing a tin based discharge produced plasma (DPP) source is in operation at XTREME technologies since September 2009. Along side the power increase, the main focus of work emphasizes on the improvement of uptime and reliability of the system using also the years of practical experience with the Alpha sources. Over the past period a EUV dose of several hundreds of MegaJoules of EUV light has been generated at intermediate focus, capable to expose more than a hundred thousand wafers with the right dose stability to create well-yielding transistors. During the last months the entire system achieved an uptime of up to 80 % calculated according to the SEMI standards. This SoCoMo is at the moment of writing the abstract ready for the integration into a beta scanner for first wafer exposures. In this paper we will present the recent status of this system like power level, uptime and lifetime of components.

In the second part of the paper the EUV source developments for the HVM phase are described. The basic engineering challenges are thermal scaling of the source and debris mitigation in addition to the volume claim conditions of the HVM scanners. Feasibility of the performance can be demonstrated by experimental results after the implementation into the beta system. Related models were verified and calibrated with the experimental results. Further efficiency improvement feasibility, which is required for the HVM phase, will also be shown based on experiments. The further HVM roadmap can thus be realized as evolutionary steps from the Beta products.

7969-51, Session 11

LPP source system development for HVM

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EUV Lithography is the front runner for next generation critical dimension imaging after 193 nm immersion lithography for layer patterning below the 32 nm node; beginning in 2013 according to the International

Technology Roadmap for Semiconductors (ITRS). NAND Flash devices are expected to have the need for this manufacturing technology as soon as 2011, with pilot line system introduction starting this year (2010). The availability of high power 13.5 nm sources has been categorized as high risk and ranked as critical with other technologies requiring significant developments to enable the realization of EUV lithography. High sensitivity photoresists with good line-edge-roughness (LER) and line-width-roughness (LWR) are needed to keep the required source power within reasonable limits. Photoresist sensitivity and other light absorbing elements are the basis to derive EUV source power requirements within the usable bandwidth (BW) of 2 %. Scanner manufacturers are requiring clean EUV power close to 200W at the intermediate focus (IF) to enable > 100 wph scanner throughput assuming 10 mJ/cm2 photoresist sensitivity. The need for a Spectral Purity Filter (SPF) increases the requirements for Raw EUV Power even higher. Clean EUV Power is calculated by taking the Raw EUV power and subtracting the losses associated with the Spectral Purity Filter (SPF) and dose control, for initial sources these losses are estimated to be 35% and 20% respectively. A scalable EUV source architecture is needed to enable the evolution of EUV lithography during the life cycle of the technology. Laser-produced-plasma (LPP) sources are expected to deliver the necessary high power for critical-dimension high-volume manufacturing (HVM) scanners for the production of integrated circuits in the post-193 nm immersion era.

7969-52, Session 11

Extendibility of EUV lithography toward 1X-nm hp generation

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To support prosperity of semiconductor businesses, continuous scaling of devices is strongly required. Referring to ITRS roadmap high volume production of 2X nm half pitch (hp) will start in recent years. EUV lithography has a promising potential to fulfill the scaling requirements with considering the cost of ownership. Nevertheless, for further scaling requirements beyond 1X nm hp, some new technique should be introduced to EUVL. There are three candidates for resolution enhancement in EUVL. The first candidate is an exposure tool with higher NA. Several exposure tool vendors announce their roadmaps to release high NA tools (>0.4) after a lapse of several years. Second candidate is enhancing resist resolution by reducing image blur. Image blur is phenomenon of energy diffusion from exposure light to resist absorption intrinsic to chemically amplified resist. The diffusion length will be comparable with target pattern size, so that the reduction of this value is very effective for resolution enhancement. The last candidate is introducing Double Patterning (DP) technique to EUVL. In DUV lithography, DP has already been on high volume manufacturing stage and feasibility of the technique had been evaluated. Of course this technique can be applied to EUVL. By combination of EUVL and DP, 1X nm hp can be achieved with current exposure tools and resist process. We examined DP process to EUV exposed wafer and obtained 1X nm hp pattern below 15 nm. In this paper the evaluated results of those three candidates will be described from various view points, technology readiness, process cost, tool availability and feasibility etc.

Our conclusion is mass production of 1X nm generation can be fulfilled with the combination of EUVL and DP. Moreover, Applying exposure tool with high NA and high resolution resist, EUVL is extendible to 0X nm generation.

7969-53, Session 12

CD correction for half-pitch 2x-nm on extreme ultraviolet lithography

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For high volume manufacturing, we had evaluated manufacturability and applicability on a rule of around hp-35-nm, which corresponds to 19-nm logic node, with fabrications of PL test site and BEOL (back end of line) test chip using EUV1 exposure. Not only accurate critical dimension (CD) and overlay but also electrical properties were demonstrated. We are now moving to evaluate a test chip fabrication for hp-2x-nm. In this paper, we describe the pattern fabrication of wiring and an accuracy of an optical proximity correction (OPC) and a flare variation compensation (FVC). We used SSR4 (Selete Standard Resist 4) with 50-nm thick and a multi-stacked resist process for the BEOL test chip evaluation. The wiring patterns with Cu filling on hp-28-nm and hp-24-nm were successfully fabricated. It will be covered to device fabrications on 16-nm logic node and beyond. For CD corrections, at first, FVC with a rule-base correction was applied to the patterns of 24-nm line-and-space varying pattern densities from 33% to 67% as to evaluate an extendibility of the flare correction concepts based on PSF and a resist blur consideration with dipole illumination. Developed inspection CD was measured from the corner to center on various pattern density areas as shown in figure 1. The correction accuracy of plus or minus 2 nm was obtained. On the contrast, corrections of OPC and FVC with model base were required obtaining accurate CD accuracy in an area of hp-2x-nm due to low k1 lithography. For the modeling, we used several evaluation patterns such as through the pitch and/or linearity of isolated-line and isolated-space. At the each evaluation patterns, flare intensities were calculated by using in-house tool. These flare intensities were considered on model creation by a fitting between an empirical data and EDA tool calculation. The fitting error of 1.15 rms (root mean square) was obtained on the 28-nm pattern. The result suggests that CD accuracy on 16-nm logic node can be satisfied by using the model based corrections.

7969-54, Session 12

Patterning challenges in setting up a 16-nm node 6T-SRAM device using EUV lithography

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Today, 22nm node devices are built using Arf immersion lithography, possibly combined with double patterning techniques. Some stretch till the 16nm node is feasible, using double, triple or even quadruple patterning. Alternatively, Extreme UltraViolet (EUV) lithography is showing promising results, and is considered to be the most likely option for this device node [1-2]. Electrically functional 22nm node devices are already available, where EUV lithography is used for the definition of the back-end layers [3]. Fewer results are published on the patterning of front-end layers using EUV lithography. In this work, EUV lithography is used for the patterning development of all critical layers of a 16nm node 6T-SRAM cell and the different challenges encountered are discussed.

Imec's 16nm node 6T-SRAM cell (0.051um2) has a litho-friendly circuit layout and will be implemented using bulk finfet technology, as this approach is considered to be the most promising one for scaling SRAM devices. The active level (64nm pitch) and the gate level (80nm pitch) are designed uni-directional and perpendicular to each other (Figure 1). The critical contact and the metal1 pitches are determined by these front-end design rules. The contact level uses rectangular local interconnects, besides the regular square contacts. These rectangular interconnects have already proven their benefit in electrical performance [3]. Short metal1 slots, in two directions, connect the transistors with each other. These four critical levels are exposed on the ASML EUV Alpha Demo Tool.

First, a process tuning is needed to set-up the bright field (~30% resist coverage) front-end patterning exercise, as most preliminary work focused on the use of more dark field masks. Initial exposures revealed a resist-dependent sensitivity to flare. This tuning involves the selection of a dedicated resist and possible process optimizations like e.g. the development step. Next to that, our full standard 22nm node integration scheme is revised in view of scaling, and the etch processes needed tweaking, to pattern the new scheme with reduced resist thicknesses. The thinner resist is needed to prevent pattern collapse at the desired

dimensions.

Exposure of a first generation test cell already showed that Optical Proximity Correction (OPC) is needed for the definition of the back-end layers, when scaling the design from the 22nm to the 16nm node SRAM cell. In order to decrease the rounding and the size of the rectangular contact holes with respect to the square contacts, biasing and probably serifs are needed on this contact level. On the metal1 layer, line-end corrections are unavoidable to ensure correct patterning and sufficient overlap with the underlying contacts. For the front-end layers, we verified if the gate level can be created in a single patterning step, because of improved aerial image contrast. Currently, in our 22nm node device, a line cut approach is needed to ensure enough overlap of the gate over the underlying fin [4]. The single patterning validates the ability of EUV lithography for device making as alternative to Arf multi patterning.

7969-55, Session 12

Availability of 2x-nm devices using EUV tool

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Extreme Ultra Violet Lithography (EUVL) has been widely realized as a promising candidate for 22 nm half-pitch device manufacturing and beyond. Selete program covers manufacturability for these devices with a scheme of lithography integration, which consists of exposure tool implementation, resist benchmark and mask technology development.

We have continued to evaluate a process liability of EUVL due to recognize our current status of lithography technology development for 2x nm node. In this study, we describe the critical point of EUVL on an assumption for device manufacturing through wafer processes. We used a full-field step-and-scan exposure tool Nikon's EUV1. A test pattern was designed for yield evaluation and exposed to a stacked multi resist layer. After the resist development, the pattern was replicated to SiO2 film with etching and metal wiring formed by damascine process.

Result of the yield value of the electrical measurement indicates our process maturity; includes resist process performance, tool performance, mask performance. We will discuss about each contribution and our process maturity.

Also tool status will be reported, especially resolution limit using resolution enhancement techniques of the EUV tool will be discussed.

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7969-56, Session 12

Progress of EUV lithography toward adoption for manufacturing

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Extreme Ultra-Violet (EUV) lithography is the leading candidate for semiconductor manufacturing for the 22nm technology node and beyond. Due to the very short wavelength of 13.5nm, EUV lithography provides the capability to continue single exposure scaling with improved resolution and higher pattern fidelity compared to 193nm immersion lithography. However, reducing the wavelength brings new equipment and process challenges.

To enable EUV photon transmission through the optical system, the entire optical path of an EUV exposure tool operates under vacuum, and in addition reticle and optics are reflective. To obtain the required CD and overlay performance, both wafer and reticle front surfaces need to have near-perfect flatness, as non-flatness directly contributes to focus and image placement errors, in the case of the reticle due to non-telecentricity. Traditional vacuum chucks, both for reticle and wafer, cannot be used and are replaced by electrostatic chucks. Any contribution of this new clamping method on CD and overlay control therefore needs to be investigated, including avoidance of particle contamination over time.

This work was performed on ASML's EUV Alpha Demo Tool (ADT). We investigated the different, non-conventional contributions to overlay control on the ADT, with particular attention to the wafer clamping performance of the exposure chuck. We demonstrate that we were able to improve the overlay performance by compensating for the wafer clamping error during the wafer alignment sequence. The impact of different wafer types on overlay was also evaluated. In addition to clamping effects, thermal effects have also been shown to impact overlay and were evaluated by monitoring the thermal behaviour of a wafer during exposure on the ADT and correlating to the resulting overlay.

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7970-01, Session 1

A comparison of maskless technologies

A. Fujimura, D2S, Inc. (United States)

No abstract available

7970-02, Session 1

Nanoimprint lithography

T. Higashiki, Toshiba Corp. (Japan)

No abstract available

7970-03, Session 1

Directed self-oriented self-assembly of block copolymers: bottom-up meeting top-down

T. P. Russell, Univ. of Massachusetts Amherst (United States)

No abstract available

7970-04, Session 2

The comparison of NGLs from a tool vendor's view

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As the conventional optical lithography reaches its limit, we are now facing a huge paradigm shift to new NGL schemes. There exist several candidates, such as Double Patterning, EUV and Nanoimprint for high-volume production, but they have their own new unconventional technical issues. This paper compares these NGL technologies from an exposure tool vendor's view.

The 1st candidate is Double Patterning. It has already been applied to real production in Flash memory production. From the viewpoint of a tool vendor, the self-align technology, such as sidewall image transfer technologies, is a "must", and no other double patterning technology is stable as for overlay. Systematic errors can easily be introduced through the various interactions of an exposure tool and other components. However perfect each component may be, overlay specifications are sometimes difficult to attain. In order to extend the DP technology further, systematic optimization of all the technologies, such as pattern design, exposure tool, reticles and pellicles, is mandatory. The countermeasures and constraints of future DP technology will be discussed in detail.

EUVL, another candidate, is now going to be introduced into pre-production phase. The delay of EUVL to 22nm node, however, is pushing us to adopt higher NA optics and off-axis illumination. This adoption forces us another challenge to finer control of wavefront aberration and the fabrication of large optical elements. We can remember the reduction of residual aberrations in the conventional optical lithography was promoted by the introduction of various resolution enhancement technologies. In addition, we may be obliged to adopt 8-mirror system for higher NA, which requires higher output source power by 2X. We are afraid chemical amplification resist doesn't work in the fine pattern area less than 20nm. The EUV tool challenges, especially in optics, will be clarified in the presentation.

Nanoimprint is the last candidate for volume-production in memory application. It can offer the proven fine resolution and good pattern fidelity. The technology matching between nanopimprint technology and the exposure tool, however, is very critical, because imprint procedure means the direct contact between a tool and a wafer. We have experienced such contact in immersion, but the degree of the mutual interaction is extremely high in imprinting. We will discuss the technical issues to match both technologies, and what will remain as the challenges with special interests to defectivity and overlay.

At present, each candidate has its own issues, and the most suitable answer may differ from customer to customer. We will characterize each technology from a tool vendor's view, considering the severe requirements in the resolution era less than 20nm.

7970-05, Session 2

Step and flash imprint lithography: defectivity and other critical aspects

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Nanoimprint lithography (NIL), in particular step and flash imprint lithography (SFIL), continues to make progress towards meeting high volume manufacturing requirements for semiconductor devices. Demonstrations have shown that NIL meets, or is close to meeting, 22nm node requirements for resolution, critical dimension uniformity, line width roughness, and template pattern placement. Even overlay, once considered a major roadblock, has improved to within a factor of two of the requirement for 22nm flash in the International Technology Roadmap for Semiconductors (ITRS). The ability to faithfully replicate virtually any structure using a simple process will ensure NIL's viability for many patterning applications. However, unlike extreme ultraviolet (EUV) lithography and 193nm immersion double patterning, NIL has not been successful in building an industry-wide collaboration to ready the technology for the 22/16 nm half-pitch ITRS nodes. A key reason for this lack of interest is that even after several years in the spotlight, publicly available data on the issues most often associated with NIL remain sparse. Without this critical information, the semiconductor industry cannot accurately assess the technology.

The goal of this paper is to show the overall status of SFIL with respect to semiconductor high volume manufacturing and, more specifically, to shed light on defectivity, the number one technical challenge. Included are new results gathered off the first 22nm half-pitch template at SEMATECH. SFIL defectivity will be addressed with detailed results from an ongoing project aimed at assessing both process and template defectivity. Data from multiple templates and inspection tools, including a near-production grade template designed to provide comparison data with an EUV process, will also be presented. The various types and sources of defects are characterized, and current and projected defect densities are shown. Plans for electrical testing and a comparison to EUV defectivity are discussed, along with a roadmap for future defect improvements. In addition, an overview of SEMATECH's 22nm imprint process, in-house template fabrication capability in conjunction with the College of Nanoscale Science and Engineering, and other ongoing projects are reviewed.

7970-06, Session 2

Defect reduction of high-density full-field patterns using jet and flash imprint lithography

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Imprint lithography has been shown to be an effective technique for replication of nano-scale features. When the imprint material is a

photocurable liquid, it is possible to perform the patterning process at low temperature and ambient pressure, which enables accurate overlay and reduces process defectivity. The resolution of the imprint approach is strictly dependent on the ability to create a 1X master mask or template, and improvements in resolution can be achieved without new optical systems or photoresist materials. In this sense, imprint lithography is a multi-generational technique that is being used to facilitate device and process prototyping at several upcoming lithography nodes.

Acceptance of imprint lithography for manufacturing will require demonstration that it can attain defect levels commensurate with the requirements of cost-effective device production. Previous work has focused on the inspection of low resolution Metal1-like patterns and the high resolution inspection of sparse sub-32nm features. This work summarizes the results of defect inspections of full field patterns that were imaged using Jet and Flash Imprint Lithography (J-FILTM). Inspections were performed with a KLA-T 2132 optical inspection tool.

A 26mm x 33mm field imprint mask was provided by Dai Nippon Printing. A primary die, consisting of 120nm NAND Flash-like features surrounded by additional metrology, alignment and test cells, was designed to simulate a standard memory gate layer. The die breakdown along with a close up of the primary pattern is shown in Figures 1a and 1b. The primary pattern was sized for compatibility with in-house inspection sensitivity.

Imprinting was performed on 200mm silicon wafers using an Imprio 300. A 2nm adhesion layer was deposited prior to imprinting. The first two imprint runs resulted in an average imprint repeater defect density of 41 defects/cm2. Potential root causes consisted of particles, resist strength, and dispenser contamination. By moving to a clean dispenser and increasing the modulus of the imprinted resist, the defect density was quickly reduced by an order of magnitude (See Figure 2.).

The remaining defects appeared to be mainly a result of particle contamination. Figure 3 depicts two typical repeater defects that were traced back to a particle event. In order to identify the cause of these repeaters, an extended imprint run was done to understand particle adders in the imprint tool. A six thousand imprint run clearly shows a tendency towards higher numbers of particle adders at the beginning of the run (Figure 4). It is interesting to note that after six thousand imprints, the particle adders are reduced to less than one particle per 100 imprints. Work is now underway to identify the cause of the particle adders and further reduce defectivity. The extension of this work to other patterns and feature sizes will also be discussed.

7970-07, Session 2

Nanoimprint lithography of 20-nm half-pitch and metal via pattern for semiconductor applications using polymer replica stamp

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In this study, 20 nm (Half pitch) and metal via 3D pattern in Si wafer was successfully replicated with UV-curable polymeric material. The replica stamp was used for step and repeat nanoimprint lithography (NIL) on 300 mm Si wafers and the pattern quality was evaluated.

The quartz stamp has been generally used for step and repeat UV-NIL due to its high pattern fidelity and durability. But it has some drawbacks such as limited pattern shape and high cost. In contrast, the polymer replica stamp is good to replicate wide variety of pattern in low cost. Hence the replica stamp can be a successful candidate for semiconductor application if some issues in it can be addressed. Among them, this study focused on addressing the issues in resolution limit, durability and defectivity in polymer replica stamp.

20 nm master pattern was fabricated on Si wafer by using the e-beam lithography, dry etching and subsequent release layer coating. The pattern was replicated onto quartz plate which is loadable into step and repeat NIL tool as a stamp. A UV-curable organic inorganic hybrid polymer was used for stamp material and a release layer was applied onto the surface of replica stamp. In step and repeat UV-NIL, the shot field was 15 mm X 15 mm and 188 shots were imprinted on a 300 mm Si wafer. Scanning electron microscope (SEM) and optical inspection tool (pixel size 155 nm) were used for line width measurement and defect counting respectively.

The line width (LW) and line width roughness (LWR) of Si master was 25.4nm and 2.8nm respectively. In case of imprinted pattern, LW=26.1 nm and LWR=1.8 nm were obtained. The result showed good pattern fidelity and enhanced LWR. By using the imprinted resist pattern, the underlying silicon nitride layer was dry etched and it showed LW= 21.4 nm and increased LWR which is due to the insufficient etch margin in resist layer.

Durability of replica stamp (20nm half pitch) was tested on 12 inch Si wafer using step & repeat nanoimprint process and obtained over 400 shots. The 3D metal-via pattern also tested using replica stamp and successfully achieved pattern transfer from nanoimprint pattern on Si wafer to Si wafer by RIE etching process .

The line width trend measured from about 400 shots showed linear decrease in line width. The slope is 0.87 nm/100 shots. It means gradual degradation of the release layer of replica stamp and the resultant LW change in NIL pattern. And this degradation again resulted in the defects in imprinted pattern.

In conclusion, we could replicate and imprint the 20 nm line and space pattern. But release layer of replica stamp showed poor durability and resulted in high defectivity. Thus the self-release material must be considered for better performance of replica stamp.

7970-08, Session 2

Progress in template and mask replication using jet and flash imprint lithography

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The Jet and Flash Imprint Lithography (J-FILTM) process uses drop dispensing of UV curable resists for high resolution patterning. The technology is actively being used to develop solutions for memory markets including Flash memory and patterned media for hard disk drives. It is anticipated that the lifetime of a single template or mask will be on the order of 1E4 - 1E5 imprints. This suggests that tens of thousands of templates/masks will be required. It is not feasible to employ electron-beam patterning directly to create this volume. Instead, a “master” template - created by directly patterning with an electron-beam tool - will be replicated many times with an imprint tool to produce the required supply of “working” templates/masks. In this paper, the ability to fabricate replica templates and masks is demonstrated.

In the case of patterned media, the process starts with the fabrication of a master template. An example of this process, for 25nm bit patterns, is shown in Figure 1. A high resolution electron beam resist, such as ZEP520A is used to define the bit array. After pattern transfer, a final relief image is formed in the mask. Figure 1a depicts 25nm half pitch pillars in the fused silica master. The master pattern is then transferred to a replica blank (Figure 1b). The working replica is then used to print the bit pattern array on a disk (Figure 1c).

An example of a fully patterned discrete track replica is shown in Figure 2a. The replica is a 150mm diameter fused silica wafer. In this example, the pattern includes both the media and the servo patterns (Pictured in Figures 2b and 2c). Patterning starts at a radius of 16.5mm and ends at 31.5mm. Critical dimension (CD) uniformity is generally well controlled, with small variations occurring at the inner and outer radius of the patterned area.

The same replication process is now being adopted for semiconductor memory fabrication. In this case, a 6025 master with a 33 x 26 mm patterned area is used to transfer the relief images into a 6025 replica mask. Initial CD results look very promising. Figure 3a shows 28, 32 and 48nm nm half pitch lines imprinted with the master. Figure 3b shows the same features after the pattern transfer process. Feature size has

been maintained, and the wall profile for all three features is close to 90 degrees. A first look at etch depth uniformity has also produced good results. Eight points within the field were measured and the etch depth of the 48nm half pitch lines was examined using atomic force microscopy. A targeted etch depth of 60nm was achieved with a 3 sigma variation of only 2.4nm.

This paper will review the process and tools used to fabricate the replicas. CD, CD uniformity, and relief image fidelity will also be presented. For the case of semiconductor mask replication, topics including defectivity, alignment strategy and image placement will also be discussed.

7970-09, Session 3

E-beam lithography development, outlook, and critical challenges

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Key advantages of e-beam lithography have been practically limitless resolution and maskless pattern generation capability with probe-forming systems. The evolution started in the 1960s with the SEM-type Gaussian beam systems writing one pixel at a time. However, serial exposure of pattern elements with a scanning beam is a slow process and throughput presented a key challenge from the beginning. To meet this challenge imaging concepts with increasing exposure efficiency have been developed projecting ever larger number of pixels in parallel.

During the 1970s the concept of shaped beams had been developed projecting on average 100 pixels in parallel.

This lithographic technology has originally been implemented in electron beam direct write (EBDW) applications and subsequently became the technology of choice for mask making in the semiconductor industry. But shaped beams have not kept pace with Moore's law so far.

The physics of charged particles impose throughput limitations on e-beam lithography systems: Coulomb interactions between beam electrons cause image blur and consequently limit beam current and exposure speed. Physically separating beam electrons into multiple beamlets to reduce Coulomb interaction led to the development of massively parallel pixel projection techniques in maskless lithography (ML2). Uniquely different concepts are currently pursued in Europe and the US aiming to image from many thousand up to millions of pixels in parallel.

This paper will provide a brief status report based on recent e-beam lithography development results. It also will give an outlook on how the various ML2 approaches will likely be able to meet the critical challenges presented by the exposure requirements in the semiconductor industry. The windows of opportunity for both mask making and EBDW will be discussed.

7970-10, Session 3

MCC8: throughput enhancement of EB direct writer

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Due to the ever-incresing mask cost and its complexity, EBDW as a ML2 (Maskless Lithography) has more attracted a great deal of attention than ever. To overcome relatively lower throughput, which is most serious issue of EBDW, systems using MEB technologies such as multi-column or multi-beam or massive-beam approach are developed and hotly discussed in recent workshops and conferences.

We are developing a high throughput 50kV e-beam direct writer MCC8 that has 8CCs to obtain higher throughput of more than 5WPH. The MCC8 has multi column cell (MCC) technology, character projection (CP) technology with design for e-beam (DFEB) and much higher current density than that of our conventional systems.

As for MCC, we had made a proof of concept (POC) system with 4CCs and presented some realistic and fruitful results in the work of Mask-D2I project of ASET. The MCC technology can shorten the total exposure time by parallel and independent exposure of each CC at its corresponding positions on the wafer. It is not the multi beam approach but the multi column approach.

Also CP with DFEB technology can enhance shot count reduction ratio up to 25x and has been applied in our single beam systems and achieved practical usability. High current density can be brought out due to the cell size decreasing by the technology node progress and other system improvements by way of limiting the shaped-beam size at the first aperture.

The current density of MCC8 is 400 A/cm2 while conventional systems are 20 A/cm2. Limiting beam size means another advantage that the size of CP is smaller and consequently the number of CP increases, i.e. throughput improvement.

By the combination of these proven technologies, MCC8 realizes a throughput of 5WPH at 22nm device node and by clustering several of this system together, over 30WPH can be realized.

In this paper, we will discuss MCC8 with the results of these technologies and how to achieve the throughput enhancement.

7970-11, Session 3

eMET: 50 keV electron multibeam mask exposure tool

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The mask writer is a key tool for the whole value chain of the semiconductor industry and for a number of emerging industrial nanoimprint technologies. In order to extend 193nm immersion lithography to the 22nm hp technology node and possibly beyond, SMO (Source-Mask-Optimization) becomes mandatory leading to the necessity of exposing complicated ILT (Inverse Lithography Techniques) patterns. Such patterns would lead to a writing time explosion for 50 keV electron VSB (Variable Shaped Beam) writers. [1] The enhancement of writing speed is also mandatory for EUVL masks and nanoimprint master templates. [2] These industrial needs can only be fulfilled by adopting multi-beam writing schemes. [3]

At IMS Nanofabrication the development of a 50 keV electron multi-beam Mask Exposure Tool (eMET) was started in 2009, with the aim to fulfill the requirements of the 15nm hp mask and template nodes, and beyond. [3, 4] In the course of this development effort an eMET POC (Proof of Concept) system will be realized until end of 2011. The eMET POC will provide c. 256-thousand programmable 50 keV electron beams of in-situ selectable 20nm or 10nm size. The eMET development is based on proven multi-beam projection technology [4]. CD fine adjustments with dose as well as size correction will be presented which were realized with a 50 keV electron multi-beam test system operating with c. 2500 programmable beams. In addition to these recent experimental results, gray scale redundant multi-beam exposure of ILT test patterns will be shown.

Furthermore, the anticipated eMET POC and eMET Product writing speeds will be explained in detail, specifically addressing the write times for leading-edge complex masks and templates for the 15nm hp technology node and below.

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7970-12, Session 3

Scanning exposures with a MAPPER multibeam system

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MAPPER Lithography is developing a maskless lithography technology based on massively-parallel electron-beam writing with high speed optical data transport for switching the electron beams. In this way optical columns can be made with a throughput of 10-20 wafers per hour. By clustering several of these systems together high throughputs can be realized in a small footprint. This enables a highly cost-competitive solution for either direct patterning or complementary patterning approach, [1, 2].

MAPPER's current systems have 110 parallel electron beams and results at 32 nm half pitch resolution have been shown [3, 4]. These exposures were all done in a static mode. This means that the 300 mm wafer stage was moved to a certain position and deflectors in the electron optics took care of scanning the field. The 300 mm wafer stage was controlled by capacitive sensors which have a high accuracy, but a limited range of about 130 µm.

This paper will describe the results of exposures with a scanning wafer stage. These results are obtained in two steps:

1. Scanning the wafer stage under capacitive sensor control

2. Scanning the wafer stage under interferometer control

At the time of writing this abstract exposures with capacitive sensor control have been performed. Results are shown in figures 1 and 2 for 100 nm half pitch and 45 nm half pitch respectively.

In this presentation we will also discuss the scanning exposure results obtained under interferometer control. The interferometer provides a longer scanning range and we are able for the first time to stitch one electron beam to the other in the same exposure.

How good the results are will depend mainly on two contributions: stage errors and beam position stability errors. We will report on our findings and distinguish the two contributions to the total stitch error.

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7970-13, Session 3

Multishaped beam: development status and update on lithography results

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According to the ITRS [1] mask is a significant challenge for the 22nm technology node requirements and beyond. Mask making capability and cost escalation continue to be critical for future lithography progress. On the technological side mask specifications and complexity have increased more quickly than the half pitch requirements on the wafer designated by the roadmap due to advanced optical proximity correction and double patterning demands. From the economical perspective mask costs have escalated each generation, in which mask writing represents a major portion. The availability of a multi- electron-beam lithography system for mask write application is considered a potential solution to overcome these challenges [2, 3].

In this paper, an update of the development status of a full package high throughput multi electron-beam writer, called Multi Shaped Beam (MSB), will be presented. Lithography performance results, which are most relevant for mask writing applications, will be disclosed. The MSB technology is an evolutionary development of the matured single Variable Shaped Beam (VSB) technology. An arrangement of Multi Deflection Arrays (MDA) allows operation with multiple shaped beams of variable size, which can be deflected individually. [4]

With that evolutionary MSB approach a lower level of risk and a relatively short time to implementation compared to the known revolutionary concepts is associated [3, 5, 6].

Lithography performance is demonstrated through exposed complex pattern, which allow the investigation of resolution, position related parameters, Line Width Roughness (LWR) and pattern fidelity. Further details of the substrate positioning platform performance will be disclosed. It will become apparent that the MSB operational mode enables lithography on the same and higher performance level compared to single VSB and that there are no specific additional lithography challenges existing beside those which have been already addressed [1]. On the basis of real pattern analysis work some throughput simulations will be given. The paper will close with MSB product roadmap outlook.

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7970-14, Session 4

Self-assembly patterning for sub-15-nm half-pitch: a transition from lab to fab

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Directed Self Assembly is an emerging technology, that to-date has been primarily driven by research efforts in university and corporate laboratory environments. Through these environments, we have seen many promising demonstrations including small half pitch (<15nm), registration control, and various layout shape capabilities. Now, the attention turns to integrating these capabilities into a 300mm pilot fab, which can study the directed self-assembly in the context of the semi-conductor fabrication environment and equipment set.

This body of work discusses the status and challenges observed during a 300mm pilot fab implementation study using a 12nm half-pitch, line and space lamella polymer system. We breakdown the study into 3 phases.

Stage 1: Fingerprints patterns

Before focusing on pattern alignment and registration issues, we first focus on the basic 300mm spin-track optimization of the self-assembly process and the dry-etch development process optimization. Here, the bake temperatures, solvent rinsing, substrate affects on orientation, PMMA dry etch, and gross defects are all studied.

Stage 2: Directing with pre-patterns

After creating a baseline process flow with reliable fingerprint patterns, we move towards directing the lamella into line-space patterns using various pre-patterns. We study the direction control process window using an ArF litho test mask with wide CD and pitch design space, and test various 300mm process sequences in order to get the most reliable DSA demonstration. (Figure 1)

Stage 3: Application specific etch demonstrations

Finally, we use the self-assembly materials to conduct various etch demonstrations, such as a basic tri-layer etch demonstration, poly gate, and STI. (Figure 2)

Through this work, we shed more light on the commercialization potential

of directed self-assembly for 15nm half-pitch patterning and below, and gain visibility into the development requirements and time needed to make this ready for mass production.

7970-15, Session 4

Integration of block copolymer directed self assembly with 193i lithography toward fabrication of nanowire MOSFETs

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Integration of block copolymer directed self-assembly (DSA) with 193 immersion lithography is an attractive sub-lithographic patterning approach. Not only can the DSA provide sub 15nm ½-pitch features by multiplying feature density compared to the photoresist guiding patterns, but researchers have also shown that the pattern quality, in terms of LER/LWR, CD control, can be improved. In this work, we demonstrate the fabrication of nanowire field-effect transistors (FETs) using block copolymer DSA with multiple patterning techniques, in which the guiding patterns for DSA are defined lithographically by 193i lithography or EUV interference lithography and then the pattern density is multiplied by DSA process. After proper modification of the chemistry of the guiding patterns, parallel lines are assembled and then transferred into an SOI substrate using plasma etching. Channels with different numbers of nanowires are cut and isolated from the array by optical lithography. Back-gated and top-gated transistors are further fabricated using conventional semiconductor manufacturing processes. Electrical analysis results prove the viability of fabricating devices using DSA multiple patterning technique. Thus, if combined with design for manufacturing, DSA could be considered as an alternative pitch division approach for existing optical lithography methods. The quality of the patterns by DSA, i.e. LER/LWR, will be discussed as well.

7970-16, Session 4

Block copolymer lithography integrated with conventional 193-nm ArF or I-line photolithography

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Block copolymer lithography utilizes the self-assembled block copolymer thin films as a lithographic mask. To date, various directed self-assembly approaches employing prepatterned substrates or external fields have been exploited for the laterally ordered block copolymer lithography. Among them, graphoepitaxy and epitaxial self-assembly are two major successful approaches. A graphoepitaxy utilizes a topographic substrate pattern to direct the self-assembly of block copolymer thin films. The topographic confinement from the side walls enforces the lateral ordering of block copolymer nanodomains within the pattern trenches. However, the maximum area of the laterally ordered morhpology is intrinsically limited by the trench width of the substrate pattern, which usually remains even after pattern transfer. In contrast, epitaxial self-assembly utilizes chemically patterned surfaces. The epitaxial assembly of block copolymers on the topography-free chemical patterns enables a laterally ordered periodic nanodomain array over an arbitrarily large area. However, an ultrafine chemical pattern, that commensurate with the block copolymer self-assembled morphology, is required. Such an ultrafine prepattern generally requires high-cost, serial lithography such as E-beam or scanning probe lithography.

In this presentation, we introduce a cost-effective and truly scalable directed block copolymer lithography synergistically integrating conventional 193 nm ArF or I-line photolithography with block copolymer self-assembly. In the first approach to combine block copolymer self-assembly with ArF lithography, a stripe surface pattern having periodic variation of surface chemistry (pattern pitch: 143 nm) was produced by ArF lithography. An asymmetric block copolymer blend films assembled upon the surface chemical pattern generated highly-ordered, multiple arrays of self-assembled cylinders with a layer pitch 30 to 60 nm, which enhanced the surface pattern density prepared by ArF photolithography by a factor of two or three. In the second approach to combine block copolymer self-assembly with I-line lithography, named as soft graphoepitaxy, the topographic pattern of an organic negative-tone photoresist prepared by conventional I-line photolithography (pattern pitch: 600–1000 nm) successfully directed block copolymer assembly. This simple idea of using photoresist pattern for graphoepitaxy reduces the number of process steps and ensures scalable and parallel processing. More significantly, any trace of the topographic pattern can be completely eliminated by a mild cleaning process after pattern transfer.

7970-17, Session 5

Progress toward 1 Terabit/inch2 bit patterned media

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We will present our recent progress in 1 Terabit/in.2 BPM fabrication. We will report a novel strategy to integrate directed self-assembly of block copolymer (BCP) with nano-imprint lithography for >1 Terabit/in.2 template fabrication. A concentric full track disk template at an areal density of 1 Terabit/in.2 has been demonstrated for the first time. This full-track template with pillar-tone dot features was fabricated on a 6” quartz substrate by combining rotating e-beam lithography with imprint lithography and BCP process. 1 Terabit/in.2 hole-tone resist dot pattern with good size uniformity and position was formed on a disk using UV imprint lithography. A reverse-tone process was used to create the thin hard mask layer that is needed in the following dry etch process to form 1 Terabit/in.2 magnetic dots. We will present the preliminary results on size sigma and positioning accuracy, magnetic sigma, and spinstand recording test. Several key challenges will be addressed, such as defect reduction in the template fabrication, servo pattern integration, and the improvement of magnetic signal uniformity.

7970-18, Session 5

E-beam directed self-assembly and imprint lithography for patterned magnetic media

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Patterned media is a solution to provide data bit thermal stability for future generation disk drives. Patterned bit media is not expected in the disk drive manufacturing until densities of 1 Tb/in2 or greater. If the bits were to be placed on a square lattice, 1 Tb/in2 would correspond to a dot period of 25 nm. The specifications for the patterned media geometry and accuracy are determined by the required magnetic switching field distribution of the magnetic bits and the recording head. One of the major contributors to a wider switching field distribution is a variation in island size. From configurations of today’s write heads, the shape of the future bits may be rectangular rather than square or round. A bit aspect ratio of 2:1, corresponds to a track pitch of 36 nm and a downtrack bit pitch of 18 nm at 1 Tb/in2.

Because of the tighter distribution of island sizes, e-beam lithographically guided self assembly of PS-b-PMMA is shown to narrow the island size distribution and the magnetic switching fields of patterned magnetic bits over bits patterned by e-beam lithography alone. Self assembly allows the multiplication of the density of the patterns to 1 Tb/in2 or greater. In addition, we show e-beam writing strategies to minimize e-beam write

time and exploit the pattern correction of directed self assembly. We also show techniques to address different shape bits. The application of e-beam directed self assembly to fabricating imprint templates and imprinted patterned media is demonstrated at densities up to 1 Tb/in2.

7970-19, Session 5

Nanoimprint process for 2.5Tb/in2 bit patterned media fabricated by self-assembling method

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Bit patterned media (BPM) is a promising candidate for high-density magnetic recording media. The data track area of BPM consists of magnetic bit array and the required bit pitch is less than 20nm for 2.5Tb/in2 and 12nm for 5Tb/in2. To realize such a high-density BPM, directed self-assembling (DSA) technology is a possible solution, and nanoimprint lithography is a promising production process for such a high-density BPM at low cost.

We have reported the application of DSA template as etching mask to form a magnetic dot array.[1] In this paper, we report the fabrication process of a master mold of a 2.5inch BPM disk by the DSA method. The replication of the BPM pattern by the UV nanoimprint process is also discussed.

The master mold is fabricated as follows. The guide pattern to order the diblock copolymer [polystyrene (PS) - polydimethylsiloxane (PDMS)] is formed by the imprint method on a silicon substrate. The prepared guide pattern is provided with a data track area and a servo pattern area. The PS-PDMS is cast into the guide pattern and annealed to form a self-assembled dot array. The dot pitch of the data track is 17nm, which corresponds to the areal density of 2.5Tb/in2. After removing the PS matrix by oxygen reactive-ion etching (RIE), the silicon substrate is etched via the hard mask layer under the PDMS portion. A silicon master mold is obtained by removing the hard mask layer.

The transparent mold is replicated from the silicon master mold. Then, the transparent mold is used to form the BPM etching mask pattern on the magnetic recording medium by the UV nanoimprint process. The critical dimension change from the silicon master mold to the UV imprinted pattern via the transparent mold is investigated.

This work was partly supported by NEDO.

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7970-20, Session 5

High-density patterned media fabrication using jet and flash imprint lithography

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The introduction of patterned media technology is targeted to enable future generations of hard disk drives. Recent work on bit pattern media (BPM) demonstrated that storage densities of 1 Tb/inch2 can be achieved. Implementation of this technology will require industrial-scale lithography at unprecedented levels of feature resolution, pattern precision, and cost efficiency. As an intermediate approach, discrete track recording (DTR), with relaxed resolution and dimensional uniformity requirements, is also being developed. The process experience gained through the development of DTR is valuable for establishing the infrastructure necessary for BPM technology. In this paper, the key process steps for using J-FIL for the fabrication of high density pattern media are reviewed.

Cost efficiency for patterned media requires both process longevity and tooling that operates at throughputs necessary to meet cost of ownership targets. Previous work has demonstrated the viability of the imprint process using fully patterned DTR templates. An example of template lifetime is shown in Figure 1. A series of 350 disks were printed, and defect levels were well below the required defect targets. To address throughput, a Molecular Imprints NuTera HD7000 system, printing at over 350 disks/hour was evaluated using both full field 48nm pitch DTR templates and 27nm pitch BPM templates. Density at these pitches is 1Tb/in2. Figure 2 depicts the HD7000 tool. Jet and Flash Imprint Lithography (J-FIL) [3] is used to print both the front and back side of the disks. Relative to HD2200, throughput of the HD7000 is doubled while occupying half the floor space of the previous generation tool, making it suitable for pilot and volume production applications.

First tests of the HD7000 focused on full field 48nm DTR printing. Throughputs greater than 360 disks/per hour were demonstrated. An example of the feature fidelity is shown in the top down SEM image of Figure 3. On average the lines measured 25.6nm with a critical dimension uniformity of 3nm, 3sigma and a line edge roughness of 4.1nm. The original master template used for these tests had several defects, however in the low defect areas the imprinting was defect free. An example of low defect printing is shown in Figure 4. Pictured is a magnified Candela scan containing both the media (darker area) and the servo tracks. The image is free of bright spots, indicating no defective scattering sites.

As a final test, BPM templates, created using self assembly, was used to imprint 27nm pitch arrays of dots. Figure 5 displays two SEM images of imprinted patterns. This paper will also discuss attributes of the imprint tool as well as the additional processes used to obtain high fidelity low defect imprinting.

7970-21, Session 5

Fabrication of chevron patterns for patterned media with block copolymer directed self assembly

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As block copolymer directed assembly continues to make progress into the fabrication of bit patterned media templates for magnetic recording hard disk drives, the need to demonstrate compatibility of self assembly with servo features and other sector header patterns becomes more compelling. Here we investigated the approach of using block copolymer directed assembly with density multiplication into chevron structures on chemically patterned surfaces to demonstrate the construction of basic building block patterns useful for sector header patterns. We demonstrated that lamellar-phase block copolymers could be directed to assemble into chevron shapes with predefined angles ranging from 20° to 90°. The width of disordered regions at the apex of chevrons can be minimized by optimal design of the guiding patterns. Disordered regions as narrow as one or two periods of the block copolymer pattern have been shown.

7970-22, Session 6

The effect of local segment flexibility mismatch on defects in directed-self-assembly of di-block copolymers

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High resolution patterning is the basis for a number of modern technologies, and in particular the ability to form and continue to scale down patterns on semiconductor devices is a key driver for the

microelectronics industry. However, the challenge is rapidly growing in difficulty as attempts are made to pattern at length scales below 25 nm using conventional lithographic techniques that involve the application of patterned radiation modulated at length scales commensurate with the pattern size scale (i.e. optical lithography and e-beam lithography). Recently, self assembled block copolymer patterning has been shown to be a promising technology for patterning at length scales between 10 to 50 nm. Computer modeling has characterized the conditions under which block copolymers will form patterns, as well as the effect of walls and surface patterns on the formation of order in block copolymers. These computer models typically rely on mean-field interactions between different polymer block segments to induce the phase separation that produces the lithographic patterns. Most of these models use an average energy of mixing between the polymer segments, determined by a Flory-Huggins parameter (chi), and an average compressibility. As the product of chi and the length of the copolymer segments increase the likelihood of phase separation increases and the specific morphology changes. While these parameters determine the phase separation, we hypothesize that the occurrence of defects can at some level be affected by the more subtle mismatch in the segment flexibility of the two polymer segments in the diblock copolymers. Mean-field models include neither of these two effects, so we have applied a more general meso-scale model of standard polymers used in block copolymer patterning techniques including poly(styrene), poly(methyl methacrylate) and poly(dimethyl siloxane) and their derivatives. Rotational Isomeric States (RIS) models of these polymers were used to derive the dependence of the Kuhn segment length of these polymers as a function of both polymer degree of polymerization and temperature. The effect of polymer structure on the Kuhn segment length as a function of length and temperature is significant. For example, the derivative of the Kuhn segment length with respect to temperature actually changes sign depending on the stereochemistry of poly(methyl methacrylate). These characteristics were programmed into a meso-scale NPT molecular dynamics model. After simulation of homo-polymers to confirm that the flexibility characteristics from the RIS models were reproduced, various diblock copolymers were simulated. These simulations showed that a mismatch in the polymer flexibility increases the likelihood of defects in self-assembled patterns of the block copolymers. The simulations also suggest temperature and segment length ranges that can reduce this mismatch and therefore the occurrence of defects.

7970-23, Session 6

Self-assembling block copolymer resist blends for large-area, low-cost etch masks

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Block copolymer films with a thickness of a single domain layer have been shown to be effective etch masks for pattern transfer of features larger than 15 - 20 nm. This work focuses on applying this concept to hydrogen bonded blends of molecular glasses with low molecular weight, triblock copolymer surfactants with the general structure PEO-b-PPO-b-PEO. Although disordered in their neat form, blends of these materials with selective additives create well-segregated block copolymer morphologies with domain sizes less than 10 nm as shown by X-ray scattering. In addition to increasing the copolymer segregation strength, which increases pattern definition, the additives can be selected based on their reactive ion etch performance to enhance the overall etch contrast of the segregated blend. These additives can range from unsaturated aromatic rings to polyhedral oligomeric silsesquioxanes (POSS), both of which can be obtained with hydrogen bond donating functional groups to drive blending and strong segregation. The etch contrast enhancement using aromatic molecular glasses enabled well-defined 6 - 7 nm cylindrical domains to be transferred into an underlying, wafer-supported SiO2 film. As commercially available commodity materials, these blends are being investigated as low cost etch masks for large-area, roll-to-roll manufacturing of porous or patterned media. Additional results with similar, lower molecular weight surfactants suggest that these pattern transfer results may be extended to achieve replication of domains as small as 2 - 3 nm.

7970-24, Session 6

Guided self-assembly of block-copolymer for CMOS technology: a comparative study between grapho-epitaxy and surface chemical modification

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Recent work has shown that Block Copolymer (BCP) lithography emerges as a viable alternative for patterning beyond optical lithography capability (1). Direct self assembly on chemical pre-patterns (2) and graphoepitaxy (3) are two predominant approaches to generate density multiplication of patterned templates using block copolymers. Both approaches have demonstrated sub-lithographic performances.

In this communication, we present a comparison between guiding the self assembly by grapho-epitaxy and by surface chemical modification. Block co-polymers are designed and synthesized on purpose for this study: PS-PMMA of different ratio (50:50, 60:40 and 70:30) and mean molecular weight (from 20k to 150k). They have been synthesized by RAFT (Reversible Addition-Fragmentation Chain Transfer) polymerization in order to efficiently control the molecular weights of each block and to obtain narrow poly-dispersity indexes. Optimal process conditions (thickness, annealing temperature and time, etc) have been obtained in most of the cases.

Pre-patterned structures used in the graphoepitaxy approaches are generated using single exposure 193nm dry lithography with commercial photo resist on the top of a commercial BARC, and than freezed before BCP process. The PS-b-PMMA is spin coated and annealed in order to generate self assembly, than chemical treatment remove PMMA and form a PS mask. The horizontal and lateral order is controlled by tuning different parameters: molecular weight of the polymeric constituents, correlation between a substrate patterns and the intrinsic copolymer period, interaction with the substrate. Figure 1a shows an example of pattern density multiplication by graphoepitaxy using this process. In this case the density of the initial pattern is increase eight times by BCP process.

Guided self-assembly by chemical surface modification is performed by the following process sequence. First, an ultra thin layer of hydroxyl terminated polystyrene as polymer brush is graphed to the silicon substrate. This layer is selectively chemically modified by oxygen plasma, using a PMMA layer which has been deposited on top and patterned by e-beam lithography as a mask. After removing the PMMA, the PS-b-PMMA block co-polymers are spin coated and annealed to obtain the guided self-assembly templates. Finally, the MMA block is selectively removed by reactive ion etching.

Figure 1b shows an example of guided self assembly by chemical surface modification. In this case, the pattern performed by electron beam lithography consists of an array of lines with a pitch of 64 nm. After self assembly, the resulting pattern presents a pitch of 32 nm, indicating a successful density multiplication.

A comparison of both processes and additional results for the two approaches (graphoepitaxy and chemical surface modification) will be presented at the conference. The self assembly process presents different dynamics in both cases. The influence of patterns height, pre-patterned pitch, time and temperature on the final self-assembled pattern will be reported. We conclude that both techniques have demonstrated sub lithographic performances while presenting also specific limitations. In consequence, a care analysis have to be done in order to define the optimal process for CMOS integration.

7970-25, Session 6

Study and optimization of the parameters governing the block copolymer self-assembly: toward a future integration in standard lithographic processes

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Block copolymers thin films are promising materials which can be used to complete new lithographic breakthroughs such as e-beam or EUV. Indeed, their ability to self assemble into various morphologies, if controlled, could be used to access cheap bottom-up nanostructured features as masks for alternative lithography.1

In this paper, we present our studies on polystyrene-b-polymethylmethacrylate (PS-b-PMMA) block copolymer systems with different block molecular weight ratio to produce either lamellar or cylindrical morphologies in thin films. More specifically, we focus on the different accessible parameters to optimize the processing conditions for the self-assembly of those block copolymers, to further integrate those materials in lithographic processes.

First of all, the interface between the copolymer thin film and the silicon substrate has to be neutralized in order to avoid a preferential wetting of the substrate by one block and to allow by this way the perpendicular orientation of the structure. This can be done by the chemical derivatization of the silicon wafers with random copolymers containing the same constituents as the block copolymer used.2 In order to understand how this random copolymer layer will influence the self assembly process, several random copolymers of different molecular weights and various PS/PMMA ratios were synthesized by controlled radical polymerization. The functionalization of the silicon surface with those random copolymers was studied by varying the grafting temperature and time as well as different cleaning procedure (RCA1, oxygen plasma, UV-ozone...) of the surface prior to the grafting. The resulting random copolymer brushes were characterized (thickness, wettability measurements...), and show that the derivatized-surface's properties are intimately linked to the grafting procedure followed (figure 1).

We studied afterwards the self-assembly process of the block copolymer film spin-coated on the different random brushes obtained by varying several parameters such as the film thickness, and the annealing time and temperature. We have shown that the thin-film morphology (in-plane, out of plane or mixed ones) depends critically on those different parameters and that a subtle optimization of them will provide almost defect-free nanostructures. Most importantly, a very good quality of the self-assembled features can be obtained within few minutes, offering thus very attractive conditions for the integration of this kind of systems in a standard lithographic process. We also examined the morphology of the self assembled features as a function of the depth of the block copolymer thin film. This is achieved by progressive Ar/O2 plasma etching of the film after the subsequent removal of the PMMA block structured domain (figure 2). Thanks to this technique, we have shown that the film top-nanostructures can span across the whole film thickness or that the in-plane and out-of-plane features can stack themselves, depending on the conditions used for the self-assembly process.
We also present some results on the block copolymer self-assembly behavior when the above-optimized parameters are combined with graphoepitaxy patterns to organize the film in more useful features for lithography.3 To conclude, results of the transfer of the PS nanostructures in the bulk silicon substrate with several plasma-etching technologies will be presented, both with the film on free-surface or organized with graphoepitaxy approaches.

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7970-26, Session 6

Registration of sub-10-nm features by hierarchical self-assembly of styrene-dimethylsiloxane block copolymers

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Self-assembly of block copolymers can form periodic patterns with smaller feature sizes than can be achieved using conventional lithography process, so it has great promise in nanoscale lithography. Registration of the features is critical for lithographic applications, and becomes more challenging as the feature sizes decrease into the nm regime. In this work, we present a hierarchical strategy for templating of small period (12 - 17 nm period, feature sizes 6 nm and above) block copolymers using a topographical pattern formed from a larger period (34 - 40 nm) block copolymer which can itself be templated using features produced by electron-beam lithography or photolithography.

This process is demonstrated using poly(styrene-block-dimethylsiloxane) (PS-b-PDMS). Block copolymers with a Si-containing block are particularly attractive due to their high etch contrast and high interaction parameter, which leads to a sharp interface between the microdomains. We successfully obtained micro-phase separation and nano-sized line and dot pattern formation from low molecular weights of PS-b-PDMS block copolymer: 16kg/mol, 12.5kg/mol, 8.5kg/mol and down to 6kg/mol. To illustrate double templating, 45.5kg/mol PS-b-PDMS block copolymer (f_PDMS = 0.33) was self-assembled to form a monolayer of in-plane cylinders of PDMS in a PS matrix, aligned with topographical templates made using photolithography. Annealing in a toluene vapor then oxygen etching of the film produced oxidized PDMS topographical grating patterns of period 34 - 40 nm. Alternatively, a perforated lamellar pattern could be produced by annealing in a mixture of toluene and heptane vapor. The 45.5kg/mol pattern was coated with a PDMS brush, then a smaller sized block copolymer, such as 16kg/mol PS-b-PDMS, was spin-coated and annealed. The 16kg/mol PS-b-PDMS has a period approximately half that of the 45.5 kg/mol PS-b-PDMS, and its self-assembled microdomains aligned with the topographical pattern to produce very well-ordered arrays of either cylinders or spheres with period 17 nm (Fig. 1). The morphology was controlled by the solvent anneal conditions: annealing in acetone gave cylinders, whereas annealing in DMF gave spheres.

The defect levels of the pattern were related to the commensurability between the two block copolymers. Defect levels in the templated 16kg/mol pattern were very low when the period of the 45.5kg/mol pattern, which was varied via the annealing process, was within 10% of twice the period of the 16 kg/mol pattern. For larger mismatch, significant defect levels (e.g. >10 defects /um^2) formed. Additionally, the duty cycle of the 45.5 kg/mol pattern was varied. The lowest defect levels in the 16 kg/mol pattern occurred at a duty cycle of around 50%, i.e. equal mesas and trenches. 12 kg/mol and 8 kg/mol PS-PDMS were also templated on the 45.5 kg/mol patterns. The period of these smaller block copolymers is incommensurate with that of the template, and superstructure patterns formed such as two rows of spheres on the mesas and one row in the trenches. 3D-simulation of this double templated self-assembly based on self consistent field theory confirmed the experimentally determined hierarchical morphologies of cylindrical sub-20 nm block copolymers on the larger period templates.

7970-27, Session 7

Approaches to rapid resist spreading on dispensing based UV-NIL

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Nanoimprint lithography (NIL) is a promising technique for nano-pattern fabrication of future magnetic and semiconductor devices. It is recognized that NIL resist spreading time is a determining factor in UV-NIL process throughput. In this study, reduction of the resist spreading time is discussed based on direct observations of resist spreading in the dispensing-based NIL process.

A low volatility resist was newly developed to enable ink-jet coating with small resist droplets and implementation of the imprint process in vacuum. Resist vapor pressure generally increases with deceasing resist viscosity. This dilemma was solved by the molecular design of the acrylate monomer. The newly developed resist was coated on quartz wafers (0.525mm in thickness) by spin coating or ink-jet coating. The coated quartz wafer and the silicon mold were set in the imprint chamber. The resist was imprinted with the mold in nitrogen, helium, or vacuum atmosphere. The resist spreading process was observed through the quartz wafer during imprinting process.

It was found that the resist spreading process is composed of three steps. The first step is observed in the early stage of resist and silicon mold contact. The resist makes capillary bridges. The capillary bridges are pushed back by the silicon mold as the distance between the silicon mold and the quartz wafer decreases. In this step, the resist flows not only in the in-plane direction but also in the vertical direction. In the second step, the resist and residual gas flow in the gap between the silicon mold and the quartz wafer along the pattern direction of the silicon mold. Residual gases merge, producing bubbles. In the third step, the bubbles shrink due to absorption of the residual gas into the resist and quartz. The remaining bubbles form non-fill type defects upon UV radiation. The bubble shrinking speed depends on the solubility of the gas in quartz. In the nitrogen atmosphere, more than a few minutes are required for the bubbles to shrink.

Two issues are examined to improve resist spreading: 1) Ink-jetting of small droplets at high area density to prevent formation of large resist capillary bridges and to reduce the distance between resist droplets. 2) Employing of the vacuum imprint process to prevent bubble formation in the gap between the silicon mold and the quartz wafer. A comparison of 1pl droplets and 10pl droplets showed that smaller droplets at high area density can reduce resist spreading time. It was also demonstrated that bubble shrinking speed can be improved by changing the imprint atmosphere from helium to vacuum. It is expected that UV-NIL throughput will be improved by combining dispensing-NIL with imprinting in vacuum.

7970-28, Session 7

Reactive fluorinated surfactant for step and flash imprint lithography

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One of the major concerns with nanoimprint lithography is separation failure, which causes defects in the imprinted area. These defects result from cohesive failure rather than adhesive failure in the separation process. We have reported that the addition of fluorinated surfactants to the imprint fluid is an effective method of aiding separation and improving template lifetime. This study was focused on the development of reactive fluorinated additives, which function as surfactants, but chemically modify the quartz template surface during the imprint process to preserve the tailored surface energy of the template (the self replenishing concept). Initial material screening indicated that the silazane functional group is suitable for this role and a new perfluoroalkyl silazane (F-silazane) was subsequently synthesized. The F-silazane shows moderate reactivity with the glass surface, as well as acceptable shelf life when mixed with standard imprint fluids. A multiple imprint study was conducted with an Imprio® 100 tool. An imprint formulation containing the F-silazane achieved continuous imprinting longer that the control imprint fluid, thus demonstrating its effectiveness.

7970-29, Session 7

A new releasing material and continuous nanoimprinting in mold replication for patterned media

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Patterned media, Discrete Track recording Media (DTM) and Bit Patterned recording Media (BPM), is one of promising technologies for HDD areal density growth. Groove size for DTM is 15nm in 50nm track pitch, and bit size for BPM is 12.5nm in 25nm tack pitch for 1Tbit/inch2 areal density on 2.5inch HDD media. That is feasibility demonstration target as the first generation of patterned media which all the media and the HDD makers are aiming at. The DTM or the BPM patterns need to be transferred to a wide and large area of a 2.5inch diameter media, with an extremely high throughput of over 1000 media per hour for a large-scale production. Therefore, Nano-Imprint Lithography (NIL) and a mold (imprint mask) are essential. And, mold replication from an EB master is also a key for the production since EB writing takes so much long time then a high cost.

In nano-imprinting, since it is contact printing, there are some difficulties reported in general, such as surface particles and/or UV resist pulling out (lift-off) and sticking, i.e. contamination, to the master mold, as well as a rise in separation force with increasing pattern density. Particularly a higher separation force might cause damages to the master mold and imprinting tool, degradation in pattern quality possibly as well. Those difficulties also work to retard continuous imprinting for the mold replication. Then, we focused on a release material to facilitate clean separation between cured resist (replica) and the master mold.

The release material needs to have PFPE (Per-Fluoro-Poly-Ether) main chain obviously. Then, we looked at terminal-group. We tried to characterize several candidates in contact angle for surface free energy, in force curve and friction curve by AFM for adhesion (release) and friction, in film thickness by XRR, and so on. Then, we found that a release material with hydroxyl terminal-group at one side in molecule showed the best performance in the characterization. We also found that the new release material we chosen showed a higher durability, i.e. less film loss by continuous imprinting especially when a higher temperature baking applied after spin-coating.

We finally carried out continuous nano-imprinting for the mold replication to see a real performance of the new release material, by an EB master mold of 50nm track pitch DTM designed pattern on a 2.5inch full surface. And, we successfully demonstrated over 300 continuous replica imprinting with no mold cleaning at all. Particularly, we found that the new release material prevented from transferring particles from the replica wafer to the master mold. No repeatable imprinting defect was caused by the particles transferring, while the others not.

This paper describes a novel release material we chosen, and continuous nano-imprinting results with it for replica mold fabrication from an EB master for the patterned media application.

7970-30, Session 7

Detection, identification, mitigation, and resolution of defects in roll-to-roll imprint lithography for flexible displays

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Roll to roll imprint lithography has been used successfully to fabricate thin film transistor (TFT) backplanes for flexible displays. The technique used for patterning is Self-Aligned Imprint Lithography (SAIL). This technique developed at HP Labs has been described before and allows for multiple levels to be imprinted in one lithography step. As we have ramped from a laboratory scale to a pilot production mode we have

uncovered systematic defect modes that were not yield limiters when producing smaller backplanes with larger pixel sizes. Materials, tools and techniques used to build these backplanes are designed for flex circuits and other components with design rules 10 to 20 times larger and greater defect tolerance. We are charting new territory in desired defect density from these tools and materials.

We apply semiconductor processing and defect learning methodology to characterize the sources of the defects, both killer and nuisance, as we ramp our roll to roll process. We will show substrate, film deposition, lithography and process induced defects as well as how they were mitigated or resolved.

Finally a request for standardization and development of new tools is proposed in order to enhance the speed of adoption of the technology into high volume manufacturing.

7970-31, Session 7

Step and repeat UV nanoimprint lithography on pre-spin coated films: a promising route for fabrication of nanophotonic chips

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UV Nanoimprint Lithography (UV-NIL) technology is a very attractive technology to reproduce micro/nano-patterns over large area at low cost [1]. The Step&Repeat approach for UV-NIL allows reaching high throughput and is currently in industrial preproduction phase for various applications such as hard disks [2]. One of the highest patterning resolution reported at this time is by Toshiba Corporation using a UV-NIL stepper with 18 nm isolated lines [3]. We present here a method combining the advantages of Step&Repeat technology and the imprinting of spin-coated films.

Thin films of low-viscosity UV-curable polymer resist (mr-UVCur21xp) from Micro Resist Technology are spin coated on 6 inch silicon wafers and imprinted with a UV-NIL steeper (MII Imprio 55). The process is performed at low pressure (P<0.8 bar), no vaccum and short exposure times (120s). The residual layer of imprinted patterns is easily controlled by initial spin coating conditions. The template consists of HSQ (Hydrogen Silsesquioxane) patterns, down to 10 nm minimum feature size, directly written by Electron Beam Lithography on quartz substrate. We have demonstrated the imprinting of gratings 14/40 nm linewidth/picth (Figure 1a) and residual layer thickness down to 2 nm (Figure 2). The very thin residual layers allow an easy pattern transfer by plasma etching of some of the smallest feature sizes reported in the literature (see Figure 1b)

The process has been successfully used to fabricate nanophotonics chips based on digital planar holography (Figure 3), performances exhibit similar results to devices fabricated by electron beam lithography [4]. This work opens a route for low cost fabrication of new kinds of components based on DPH technology.

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7970-32, Session 8

Fast mask writer: technology options and considerations

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No abstract available

7970-33, Session 8

IMAGINE: an open consortium to boost maskless lithography take off: first assessment results on MAPPER technology

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In the latest ITRS roadmap updated last July, Maskless remains as a candidate to address lithography needs for sub-16nm technology nodes. The attractiveness of this solution in terms of cost and flexibility linked to the throughput potential of the massively parallel writing solutions maintain the interest of large scale IC manufacturers, such as TSMC(1) and STMicroelectronics, to push the development of this technology. Nevertheless, the development of multibeam does not reach yet the level of EUV maturity, the other candidate for 16nm technology node. Indeed, technological solutions developed in the US, with the KLA REBL project and in Europe with IMS Nanofabrication (Austria) and MAPPER (Netherlands) are still at the pre-alpha platforms level with limited capabilities with respect to the final ones expected for the high volume manufacturing platform. But even with limited funds and supports, these companies highlighted already the potential of this technology which is now really considered as a real lithography option (2,3).

In parallel to tool development, multibeam needs to rely on a robust infrastructure and for this partnership is essential to keep dynamic and know-how dissemination.. Through its seventh framework program (FP7), from 2008 to the end of 2010, Europe has funded the first multibeam consortium, named MAGIC, where MAPPER and IMS Nanofabrication solutions and multibeam infrastructure were jointly developed.

Starting July 2009, LETI and MAPPER have initiated an open collaborative program IMAGINE focused on the assessment of the MAPPER technology. TSMC and STMicroelectronics already joined this consortium followed by several infrastructure partners on data preparation, resist and processes. This paper will first briefly outline the objectives of this program,.then it will report on the first year tool assessment results, resolution capabilities (see pictures below), stitching performances and technology reliability. Based on all these data directly collected in an industry-like environment, this paper will provide an extensive overview on the maturity degree and the ability of a low energy accelerating voltage multibeam option to answer to the industry needs in the 2015 horizon.

7970-34, Session 8

Influence of massively parallel e-beam direct-write pixel size on electron proximity correction

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E-beam direct writing (EBDW) is one of the potential solutions for multiple nodes for 32-nm half-pitch and beyond. In the past, its throughput limitation curbed EBDW development to mostly mask making, small volume wafer imaging, and prototyping. It has then been proposed to achieve throughput greater than 10 wafers per hour (WPH) by a single column with >10,000 e-beams writing in parallel, or even greater than 100 WPH by further clustering multiple columns within a certain tool footprint by MAPPER.

However with the MAPPER tool, all electron beams are scanning in parallel and synchronized. It looses the flexibility of changing dosage of each individual beam to achieve sub-pixel accuracy. In addition, the required aggregate bandwidth at the data stream module is up to 12 Tera bytes per second (Bps) for a 10 WPH tool with 13,000 beamlets and 2.25-nm writing pixels. Beyond the 32-nm node, sub-nm accuracy for critical dimension and placement accuracy of the features is required. But, using the sub-nm grid in raster scanning will dramatically increase the aggregate bandwidth to over 60 Tera Bps.

In this paper, we demonstrate sub-nm proximity error and pitch accuracy by using the multiple-nm pixel size via shape modification and dithering rules, which can reduce the need of aggregate bandwidth to less than 7.5 Bps onto MAPPER's writer. Furthermore the writing-error-enhanced-factor to quantitatively characterize the impact of CD and pitch accuracy by various resist and focus will be reported.

7970-35, Session 8

Data path development for massive electron-beam maskless lithography

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Electron beam lithography has been used in the production of integrated circuits for decades. However, due to the limitation of throughput it was not a viable solution for high volume manufacturing and its biggest application is the production of semiconductor masks. Due to many considerations it has particularly now become desirable to eliminate the semiconductor mask and introduce maskless lithography for semiconductor fabrication [1]. Massive electron beam maskless lithography (MEBML2) has been proposed as a solution to this problem. The MEBML2 system overcomes the traditional source current limitation of an electron beam system by using many thousands of parallel electron beamlets to write a pattern directly on the wafer [2], [3].

In developing the MEBML2 tool the challenges have shifted and, in absence of the mask, the system data path has emerged as one of the central challenges. The main theme in the data path development is bandwidth. The required raw bandwidth at the patterning beam is determined by throughput and resolution, i.e. pixel size and number of intensity modulation levels. To achieve a production worthy throughput at 10 wafer per hour in a Gaussian-beam-based maskless lithography system, by writing 3.5 nm pixels at 2 levels (on/off) which is required for the 22 nm lithography node, the required aggregate bandwidth at the beam blanker array is up to 45 Tbit/s. [3] This large bandwidth requirement means that the data path architecture is mainly characterized by the bandwidth of the data streams in the system. Compression techniques can be used to reduce the intermediate data stream bandwidth requirements in the system [4]. This technique could lead to simplified design of the system, reducing power consumption and footprint, but comes at the cost of increased data processing complexity and possible limitations on throughput.

In this paper we will show results from the development of a prototype data path for the Gaussian-beam-based maskless lithography system. A new concept for the data processing and storage is presented. This vertex based processing and storage technique is shown to reduce memory usage considerably, with only modest requirements for the hardware resources. It shows that realistically implementable data path systems for high volume manufacturing with a maskless lithography technology are available.

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7970-36, Session 8

EBDW to complement optical lithography for 1D GDR patterning

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The semiconductor industry is moving to highly regular designs, or 1-D Gridded Design Rules (1-D GDR), to improve process latitude, chip size and chip energy consumption.

The fabrication of highly regular ICs is straightforward. Poly and metal layers are rearranged into 1-D layouts. These 1-D layouts facilitate a two-step patterning approach: a line-creation step, followed by a line-cutting step, to form the desired IC pattern (See Figure 1).

The first step, line creation, can be accomplished with a variety of lithography techniques including 193nm immersion or interference lithography, self-aligned double patterning (SADP) and directed self assembly. This step appears to be scalable to at least 7nm, with two applications of SADP for pitch division by 4.

The second step, line cutting, requires an extremely high-resolution lithography technique. At advanced nodes, the only options appear to be 193nm immersion with quadruple patterning, which would be extraordinarily costly, or EUV or EBDW.

This presentation focuses on the requirements for a "cut" pattern exposure tool and simulations of Multibeam's innovative e-beam lithography technology. All of the discussion of "cuts" applies directly to "hole" layers such as contacts and vias.

The "cut / hole" exposure tool needs to meet four major criteria: high 2-D resolution, overlay to underlying layers, high throughput, and cost-effectiveness. Multibeam's technology meets all four requirements.

High 2-D Resolution

Multibeam uses variable shaped electron beams with extremely high 2-D resolution to directly expose cut / hole patterns, extending to the 11nm technology node and beyond. 1-D layouts can be optimized by knowing the shape repertoire of the e-beam litho tool.

Overlay to underlying layers

Multibeam's array architecture consists of multiple columns. Each column has one beam, and each beam has a BSE detector. The BSE detector enables direct alignment of each beam to local alignment marks on a distorted wafer.

High throughput

Multibeam's e-beam "engine" technology consists of a compact array of identical all-electrostatic e-beam columns. Each column produces a high-current density shaped-beam. Each shaped beam is rapidly blanked on-and-off while vector-scanned across the wafer surface. Vector scanning offers a huge throughput advantage for cut /hole patterns, which have low (3-10%) pattern density. By vector scanning, Multibeam skips over empty areas, reduces shot count and data rate, and maximizes beam "on" time. With ~100 columns in each engine and multiple engines in a cluster tool, Multibeam's technology can match production flows at high-volume fabs.

Cost-effectiveness

EBDW eliminates cut / hole masks. This drastically reduces the cost of pattern exposure.

7970-37, Session 8

Model-based mask data preparation and impact on resist heating

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As 20nm logic node approaches, it is now clear that logic devices will be written using 193i lithography with Source-Mask Optimization (SMO) and Optical Proximity-effect Correction (OPC) producing complex mask shapes. At 20nm, Sub-Resolution Assist Features (SRAFs) have sub-60nm shapes in mask dimensions. With electron beam-based writing of masks, short-range blur caused by Coulomb effect, forward scattering, and resist diffusion is 20nm to 40nm for the leading edge. With the size of the shape being written approaching the short range blur, two things occur. Firstly, the rounding aids in reducing the required shot count to write non-orthogonal shapes, if Model-Based Mask Data Preparation (MB-MDP) technique is deployed. Secondly, model-based correction based on shape modification or dose modification become necessary to write the small shapes. MB-MDP takes advantage of its mask-simulation based approach to allow overlapping shots. Overlapped areas are 2X dose (or more) and provide dose modulation in addition to shape correction for added flexibility in model-based correction of small features. This approach, however, causes a theoretical concern for increased resist heating in the overlapped regions potentially causing critical dimension uniformity (CDU) degradation and worse. This paper will present the results of the study that enabled the MB-MDP capability on the NuFlare EBM-7000 and above models, an

7970-56, Poster Session

Scatterometry sensitivity for NIL process

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It is necessary and important to control the residual layer thickness (RLT) in order to keep a high -resolution performance for nano imprint lithography (NIL).

And scatterometry is one of the CD measurement meteorology tools for NIL process (including RLT-measurement).

We reported a first order analysis result about scatterometry sensitivity last year at this conference considering only reflectivity, not phase about scatterometry signal.

In this paper, the scatterometry sensitivity considering phase, up to 45nm HP resin pattern and beyond by using RCWA (Rigorous Coupled Wave-analysis) simulation is described.

The criterion of this analysis is defined as the quantification of the sensitivity comparing with 65 nm HP resist pattern of ArF immersion process.

And this criterion is the sum of the absolute difference of the reflectivity values between the nominal and varied conditions thorough the spectrum, which are used in scatterometry tools.

Furthermore, the simulated result in this analysis can be used to discuss the extendibility of scatterometry.

7970-58, Poster Session

Directed self-assembly of block copolymer on photochemically attached polymer surface layer

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The microdomain structure of polystyrene-polymethylmethacrylate block copolymer (PS-b-PMMA) was directed by a photochemically attached polymer surface layer. The photochemical attachment of neutralization polymer on silicon surface was convenient and effective technique for interfacial energy control to provide the directed self-assembly of block copolymer.

Controlling the interfacial energy between under substrate and block copolymer was required for the direction control of block copolymer self-assembly. Mansky et al. have demonstrated controlling the interfacial energy using the polymer brush with end-functionalized random copolymer. Their method was an effective for precisely controlling the interfacial energy; however the long annealing time (1~3 days) was needed for the polymer brush formation.

In this study, we investigated photochemically attached polymer surface layer for controlling the interfacial energy to direct the block copolymers. It is simple and quickly forming method.

The benzophenone chlorosilane derivative was synthesized and immobilized on the Si wafer surface from toluene solutions using triethylamine as a catalyst. Then the polymers for interfacial controls were spin-coated on the benzophenone-modified surface. The polymer film was irradiated by ArF excimer laser and rinsed with cyclohexanone to form the polymer surface layer. The lamella-forming PS-b-PMMA was spin-coated and annealed to provide the microdomain structure.

As a result, the perpendicular microdomain orientation of lamella-forming PS-b-PMMA on the substrate modified with polymer surface layer. The photochemically attached polymer surface layer was effective for the interfacial energy control for block copolymer. The microdomain structure of PS-b-PMMA film formed on the lithographic pattern of the polymer surface layer was observed and the directed microdomain orientation of PS-b-PMMA was obtained. The new polymer surface layer provides the developing more efficient directed self-assembly lithography.

7970-59, Poster Session

Soft lithography for patterning polymer-carbon nanotube composite

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The development of applications for nanotechnology depends partly on micro- and nanofabrication techniques for the structuring of nano-materials. In this regard, the patterning or structuring of nano-composites based on polymers and carbon nanotubes is of great interest for a variety of applications including biomedical and electronics. We report on the use of soft lithography for the fabrication of functional nano-composite material structures as free-standing components or on flexible substrate. We have successfully structured composites of polyvinyl alcohol (PVA) and multi-walled carbon nanotubes (MWCNT) in the micro-scale dimensions.

Soft lithography involves the use of a stamp or mold typically made from an elastomer such as polydimethylsiloxane (PDMS). The PDMS stamp has patterned relief structures on its surface and is employed to print complementary structures with feature sizes ranging from nanoscale to a few hundred microns. In our work, the PDMS soft mold contains micro-patterns made by molding the PDMS on a complementary silicon master mold fabricated by anisotropic KOH bulk etching. The PDMS soft mold patterns are transferred onto a wet layer of PVA-MWCNT nano-composite by replica molding or microtransfer molding. The nano-composite is prepared by blending MWCNT with an aqueous solution of PVA prepared by dissolving PVA in de-ionized water at 75 °C. The water to PVA ratio is 6: 1 by weight. For eliminating the agglomeration of MWCNT, MWCNT is mixed with acetone with vigorous magnetic stirring at 85°C until the acetone is evaporated completely. The MWCNT is mixed thoroughly with PVA solution at different concentration by a two hour ultrasonic bath treatment. The thorough mixing is very essential to ensure that the CNT is dispersed in the PVA uniformly. Finally, the PVA-MWCNT pre-polymer blend is de-aerated by vacuum treatment for 1 hour. The PDMS soft mold is placed in contact with the wet nano-composite layers on silicon, glass or polyethylene terephthalate (PET) substrates. The features of the PDMS mold are transferred by solidifying the liquid nano-composite material at room temperature in contact with the PDMS

soft mold. The liquid nano-composite conforms to the features of the soft mold, resulting in micro-scale patterns of the nano-composite.

The resulting patterned nano-composite layers exhibited a significant contrast in electrical conductivity between the areas with nano-composite patterns and those with no patterns. The conductivity of CNT films can be conveniently controlled over many orders of magnitude by adjusting the MWCNT and PVA weight ratios. Prior research conducted by other researchers has demonstrated special mechanical and electrical properties of polymer-CNT composite thin films. For instance, the stress in the CNT film is detectable at superfine scale by Raman spectrum shift. The fabrication processes reported here can be conceivably used in thin film devices and flexible microsystems. The soft lithography method is a cost-effective method of fabricating micro- and nano-scale dimension structures of polymer-carbon nanotube composites such as the PVA-MWCNT material in the present case.

7970-60, Poster Session

Direct-write maskless lithography using patterned oxidation of Si-substrate induced by femtosecond laser pulses

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Photolithography is an important technique to fabricate micro and nano photonics, nanoelectromechanical systems (NEMS), microelectromechanical systems (MEMS), microfluidics and lab On a Chip Systems. Generally, photolithography involves either physical or chemical vapour deposition, and then deposited films must be patterned subsequently using a resist and various etching techniques. Photolithography is not well-suited to cost-effective and high-throughput processing since there is several steps involved in fabrication process and this technique requires photomask for replication which its fabrication is normally very expensive and time consuming. Over the past few years, numerous attempts have been proposed for maskless lithography technique such as scanning electron beam lithography (SEBL) focused ion-beam (FIB) lithography, multi-axis electron beam lithography (MAEBL), interference lithography (IL) maskless optical projection lithography, easy soft imprint nanolithography (ESNIL), scanning-probe and dip pen lithography (SPL, DPL), and Tribo Nano Lithography (TNL) based on atomic force microscope (AFM). Although, these techniques have some advantages, they entail time consuming processing steps and employ complex and expensive equipments and systems which are influenced by environment and require well-trained user for their operation, leading to high operating cost and low throughput.

In this research, we reported a direct-write maskless lithography method by a combination of laser oxidation of silicon and wet alkaline etching. To the best of our knowledge we are the first to report direct maskless etch stop writing by oxidation of silicon induced by MHz frequency femtosecond laser irradiation for micro/nano-machining application. Using a high repetition femtosecond laser in megahertz rate enables us to control laser fluence below the ablation threshold which causes crystalline silicon conversion to silicon oxide. The oxidized thin layer of silicon is then used as an etch stop in the following wet chemical etching solution (KOH).

In this work a theoretical and experimental analysis of the effect of the laser parameters such as repetition rate, pulse width and number of pulses on the quality of oxidized area and the size of the fabricated features has been carried out. This proposed method has a potential of fabricating features in micro/nano scale by optimizing etching and laser parameters such as employing a laser beam of shorter wavelength, a higher NA focusing lens and reducing pulse energy.

This technique can lead to a promising solution for maskless lithography since it involves less processing steps and requires simple equipment configuration. Also, this method allows for large-area patterning (in mm-scale) at fast writing speed under ambient conditions. In comparison to systems such as AFM, FIB and Electron Beam, which are employed in other techniques, lasers are much more economical and can be acquired and operated at lower cost which makes it particularly suitable for rapid prototyping and custom-scale manufacturing for a wide variety of applications in MEMS, NEMS, fabrication of semiconductor and Lab On a Chip systems. Scanning Electron Microscope (SEM), a Micro-Raman and Energy Dispersive X-ray (EDX) spectroscopy analyses were used to evaluate the quality of oxide layer and the etching process.

7970-61, Poster Session

Fast and large-field electron-beam exposure by CSEL

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We have developed a Crestec Surface Electron emission Lithography (CSEL) for shrinking the dimensions of semiconductor devices. CSEL system is 1:1 electron projection lithography using surface electron emitter. A resolving power below 10nm is possible because of the property of an electron optics and an electron source of the system. In first report1, we confirmed that a test bench of CSEL resolved below 30 nm pattern over 0.2 um square area. Practical resolution of the system is limited by the chromatic aberration. We improved the resolution of the prototype CSEL system by reducing the initial energy spread of electrons and/or by increasing the electric field intensity. An energy spread of emitted electrons of a nanosilicon planar ballistic electron emitter (PBE) is very small as explained in other report2. After that, the prototype CSEL system exposed sub-micron patterns distributed over 3 mm square area corresponding to 10 times size of sub-field as shown in last report3.

In this study, we examine the prototype CSEL system exposed L/S pattern over full-field for practical use. The experimental column of the system is composed of the PBE and a stage as a collector electrode which is parallel to the electron source. An accelerating voltage of about -5 kV is applied to the electron source with respect to the collector. The target wafer located on the stage and PBE are set between two magnets that generate an vertical magnetic fields of 0.5 T to the surface of the target wafer. A gap between the electron source and the target wafer is adjusted to a focus length depending on electron trajectories in the electromagnetic field in the system. The electron source projects a patterned electron image on the target since the patterned mask was formed on the surface electrode of the electron source. The electrons emits from openings of the mask.

When a pulsed bias voltage is applied to the electron source, the electron source emits a patterned surface electron beam. The beam strikes the resist film coated on the target wafer and make replica of the pattern. We indicate the system exposes 200 nm L/S pattern over 10 mm square area of full-field in 1 sec. An advatage of CSEL is high resolution due to small chromatic aberration, and another advantage is pottentially high throughput because the coulomb blur is small without any crossover in the electron optics. When we get sufficient current from the electron source the throughput can be more than 100 wafers/hour.

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7970-63, Poster Session

Optimization of e-beam landing energy for EBDW

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E-beam lithography is capable of patterning high-resolution shapes. It is widely considered as a complement to extend optical lithography for patterning critical layers.

Most EBDW systems are in development from 5 keV to 50 keV e-beam landing energies. This 10x difference in electron energy has widespread effects on beam shape, LER, CDU, throughput, thermal budget and alignment mark imaging.

Some tradeoffs of high-energy versus low-energy EBDW are well known: high energy results in sharper resolution, low energy reduces thermal impact. Other tradeoffs are either not as well known, or unexamined, despite the importance of electron energy to e-beam lithography performance.

We present a detailed analysis of the tradeoffs of various e-beam landing energies. We use a simple column design with no beam crossovers and high beam currents for all simulations. We examine 5 keV, 7.5 keV, 10 keV, 20 keV and 50 keV.

Simion 8 (from Scientific Instrument Services, Inc.) is used for electrostatic lens analysis and charged particle trajectory modeling.

We examine:

1. Beam shape repertoire (beam profiles)

2. Contributions to LER and CDU (#-of-electrons per shot, beam edge acuity, depth of focus, beam intensity drift)

3. Throughput (beam current)

4. Thermal budget (beam power)

5. Alignment mark imaging (backscattered electron intensity)

Low energy EBDW has advantages in resist sensitivity and thermal control. Its disadvantages include lower beam current, poorer alignment mark image contrast and a requirement for very thin resist.

High energy EBDW has advantages in beam current, alignment mark image contrast and resolution. It's disadvantages include wafer heating and low resist sensitivity.

With set requirements for beam shape, LER, CDU and thermal budget, we report the findings in beam dose (throughput) and alignment mark imaging at various beam energies.

7970-64, Poster Session

Demonstration of lithography patterns using reflective e-beam direct write

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Traditionally e-beam direct write lithography was too slow for most lithography applications. E-beam direct write was limited because maximum blur requirements limits the total amount of allowable current in a single column. Printing small features requires to either significantly reduce the throughput of an e-beam lithography tool, or to significantly increase the number of electron beams in a single tool. Because of today's uncertainty with regards to the lithography roadmap beyond 22nm and novel design concepts which use semiconductor technology to increase e-beam lithography throughput to commercially viable levels, new e-beam direct lithography tools are designed with lithography performance at 22nm and below.

REBL (Reflective Electron Beam Lithography) is being developed for high throughput electron beam direct write mask-less lithography. The system is targeting critical patterning steps at the 20 nm node and beyond at a capital cost equivalent to 0.5 M$/WPH. Reflective Electron Beam Lithography incorporates a number of novel technologies to generate and expose lithographic patterns with throughput and footprint comparable to current 193nm immersion lithography systems. A patented reflective electron optic concept enables the unique approach utilized for the Digital Pattern Generator (DPG). The Digital Pattern Generator is a CMOS ASIC chip with an array of small, independently controllable lens elements, which act as an array of electron mirrors. In this way, the system is capable of generating the pattern to be written using massively parallel exposure by ~1 million beams at extremely high data rates (~ 1Tbps). A rotary stage concept using a rotating platen carrying multiple wafers optimizes the writing strategy of the Digital Pattern Generator to achieve the capability of high throughput for sparse pattern wafer levels. The lens elements on the Digital Pattern Generator are fabricated at imec under imec's CMORE program. The fabricated Digital Pattern Generator contains ~ 1,000,000 lens elements, allowing for 1,000,000 individually controllable beamlets. A single lens element consists out of 5 electrodes, each of which can be set at controlled voltage levels to either absorb or reflect the electron beam.

A system using a linear movable stage and the Digital Pattern Generator integrated in the electron optics module was used to expose patterns on device representative wafers. Results of these exposure tests are discussed.

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7970-65, Poster Session

A lossless circuit layout image compression algorithm for electron beam direct write lithography systems

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Dai and Zakhor (2006) introduced a data delivery system (Fig. 1) with a lossless image compression component to improve the throughput of electron beam direct write (EBDW) lithography systems. By storing the compressed layout image in the processor board memory and decoding it on-the-fly at the decoder circuit which is connected to the lithography writer with on-chip wiring, they were able to significantly increase the throughput of EBDW lithography systems.

The layout image compression algorithm should satisfy the following properties: 1) the compression ratio should be at least (Transfer rate of Decoder to Writer / Transfer rate of Memory to Decoder), and 2) the decoding algorithm has to be simple enough to be implemented within the EBDW lithography writer as a small add-on. This second constraint requires the use of a decoder operating with little memory.

Our work uses the data delivery system framework proposed by Dai and Zakhor (2006), but we have significantly improved the layout image compression component by taking a completely different approach (Fig 1) based on an efficient and specialized transformation.

Since most of the polygons in layout images are Manhattan, simple corner descriptions to represent the polygons like those in the widely used GDSII/OASIS formats are effective for representing layout images. However, layout images may also contain non-Manhattan polygons. Since full rasterization is required to reconstruct non-Manhattan polygons from earlier corner representations this type of encoding will generally be too complex for a low-memory decoder. Our specialized transformation restricts corners to those delimiting horizontal and vertical contours and combines the efficiency of corner representation with fast and low-complexity line-by-line decoding.

Our algorithm also contains a low-complexity frequent pattern replacement component (Fig. 2) to take advantage of repeated patterns within the layout image. Instead of using relatively slow procedures to search the entire image for frequent patterns, we exploit the hierarchical structure already present in most GDSII/OASIS formatted representations for fast frequent pattern searching. In other cases we first apply the algorithm proposed by Gu and Zakhor (2008) to deduce the hierarchical structure of the layout from the GDSII/OASIS representation.

Finally, the image output from our procedure is over a ternary alphabet and the vast majority of pixels are zeroes. To this output image we apply a novel run-length encoding scheme and arithmetic coding to produce our compressed binary representation of the original layout image.

The proposed algorithm achieves three to five times higher compression than Block C4, which is the follow-up algorithm proposed by Liu, Dai, Zakhor, and Nikolic (2008) to the original layout image compression scheme C4 proposed by Dai and Zakhor (2006). Our algorithm has a simpler decoder which can be implemented in VLSI with less on-chip memory than C4 (2006) or Block C4 (2008). It is also about 50 times faster than Block C4 in encoding and about 20 times faster in decoding. (Figures 4-6 offer detailed results for two circuits. JBIG refers to a standard binary image compression algorithm.)

7970-66, Poster Session

Electron-beam-induced freezing of a positive tone EUV resist for use in directed self-assembly applications

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Recently, directed self assembly (DSA) of block copolymers (BCP) through lithography assisted epitaxy and graphoepitaxy has been investigated by a number of groups. This innovation has enabled the possibility of pitch division beyond the resolution of optical lithography. Many groups have reported the use of negative tone resists for the demonstration of block copolymer alignment, because undesired solvent interaction, resist degradation and deformation during polymer depositions can be avoided. Furthermore, the negative tone resists used could withstand the high temperature annealing steps that were required for lamella formation of block copolymers. With few or no commercial negative 193 nm and EUV resists available, resist freezing is a solution that can be incorporated into DSA processing steps that involve commercial positive tone resists.

We present a novel way for freezing of a positive tone EUV resist using electron beam irradiation to yield a material that is compatible with processes used for the DSA of block copolymers. In the experiment a positive-tone open-source EUV resist was used as the template material for graphoepitaxy. Patterned resists were frozen by irradiation with an electron beam to doses that facilitated polymer crosslinking and the frozen resist was found to retain the original pattern after annealing above the Tg of the resist for 3 min (Figure 1). In this paper, the feasibility of using electron beam irradiation for resist freezing will be studied. The effect of CD and LER after resist freezing and BCP deposition will also be discussed.

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7970-67, Poster Session

Corner rounding compensation in photomask writing

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In Electron Beam lithography, proximity effect correction is unavoidable problem. It indicates the behavior that electrons shot by gun colliding with resist molecular and substrate atoms scatter, and expose unintended position. The short range scattering caused by resist molecular is called as forward scattering, and the long range scattering caused by substrate atom is called as back scattering.

In 50keV VSB (Variable Shaped Beam) mask writer, usually used for mask writing, It is assumed that forward scattering is less than 50 nm, and back scattering is approximately 10 um. Actually the forward scattering range is thought as shorter. This figure includes beam blur and “process blur” which means the dimension variation caused by development process. It is difficult and not so beneficial to divide these factors, they are treated as 50nm blur.

The back scattering affects to the dimension variation at this time. Line width become wider in dense area, smaller in sparse area. Proximity Effect Correction has been studied, and its purpose is to correct such line width variation.

Thus, reasonable strategy for proximity effect correction can be like the following.

Firstly, it divides whole chip into 1um or smaller meshes, and calculates densities in each mesh. Secondly, applying Gaussian filter to the density map to obtain effective backscatter intensity. Finally, it calculates optimum exposure intensity for the patterns which belongs the mesh. Low dose to dense area, high dose to sparse area.

On the other hand, the forward scattering has been ignored because its impact to line width variation was very small. But, its effect can be definitely observed in corner and line end. This “corner rounding” effect makes pattern fidelity worse. This means that the mask cannot reflect aggressive OPC result correctly. The smaller the feature size, the more critical “corner rounding” is observed.

To fix this problem, overwrite “corner pattern” at each corner seems to make situation better. But the optimal corner pattern’s specification such as pattern size and dose modulation is required.

We studied about the optimal corner pattern’s specification.

Algorithm to calculate optimal dose for corner pattern will be shown. And its impact is validated by simulation.

7970-68, Poster Session

Fabrication active defect in colloidal crystals by two-photon-induced polymerization

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Colloidal crystals (CCs) are attractive 3D photonic crystals because of easy fabrication and tunable PBG in the UV-Visible-IR range.Although only a pseudo-PBG can be obtained in CCs, there is a distinct L-point bandgap in CCs forbidding light propagation in the (111) direction, which can be utilized to manipulate the spontaneous emission of the light emitters. The optical gain enhancements of the active materials in CC owing to the L-point gap have attracted much attention because of the application in fabricating low-threshold laser. Fabrication of defect in perfect colloidal crystals will introduce defect mode in otherwise forbidden PBG, which makes the emitters embedded in the colloidal crystal emit light at the defect mode wavelength and facilitates gain enhancement of the gain media. However, it is difficult to introduce artificial defect in colloidal crystals by traditional optical lithography method, which is normally useful in 2D fabrication. Two-photon-induced polymerization (TPIP) is an unique method to fabricate artificial 3D features with high resolution, which is proper to introduce defect in colloidal crystals. In this manuscript, we demonstrate the fabrication of active defect in colloidal crystals by TPIP using dye-doped photoresin.

Figure. 1 (a) SEM image of the slice fabricated by TPIP at the edge of the colloidal crystal; (b) Microscopy image of the capital character “A” in colloidal crystal; (c) Confocal laser scanning microscopy image of the dye-doped capital character “A” in colloidal crystal

Colloidal crystal was fabricated by vertical method using monodispersed PS microspheres. Allyl-fluorescein dye molecule was synthesized and doped into commercial photoresin SCR500 to make dye-doped photoresin, in which the dye concentration is about 2 wt%. A mode-locked Ti:sapphire laser (Tsunami, Spectra-Physics) was used as an excitation source, which provided a wavelength of 780 nm and a pulse width of 80 fs at repetition rate of 80 MHz. The laser was tightly focused via a high NA(1.4, oil immersion, Olympus) objective lens, and the focal spot was scanned on the x-y-plane by a two-galvanomirror set (HurrySCAN 14, SCANLAB), and along the z-axis by a piezostage (P-622. ZCL, PI), both controlled by a computer. Fig. 1 (a) shows the SEM image of the polymeric slice at the edge of the colloidal crystal, which is half embedded in the colloidal crystal, and the other part outside the colloidal crystal. The outside part is obviously supported by the embedded part, which demonstrates that feature can be readily fabricated inside the colloidal crystal. Fig. 1 (b) (c) shows the microscopy image and confocal laser scanning microscopy image of the dye-doped capital character “A” in colloidal crystal. From Fig. 1 (b) (c), dye-doped defect was successfully introduced into the colloidal crystal, which paves the way for investigation optical property of the active defect in colloidal crystal

7970-70, Poster Session

High-throughput near-field optical nanolithography by scanning microsphere array

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Optical near-field has been extensively examined as a possible route to overcoming the traditional optical diffraction limit as authors have demonstrated a variety of nanopatterning examples in the optical near-field both in apertureless and apertured schemes.

While the demonstrated results carry a great promise in terms of spatial resolution (up to ~10nm), a direct writing method based on a single scanning probe has limitation in achieving high processing throughput.

In order to tackle the described issue, a parallel near-field optical nanomanufacturing scheme has been developed for arbitrary nanopatterning by authors using the fluidically assembled microsphere arrays incorporated with a DMD (digital micromirror display) array for laser-modulations. Although the optical near-field formed under regularly assembled micro/nano- spheres were previously utilized for periodic lithographic patterning, the microsphere array assembled in orthogonal and discrete manner, allowed truly arbitrary nanopatterning by combining it with the DMD array enabled optical switching and piezo based scanning motion.

In this study, we will report high rate lithographic capability utilizing the massively parallel near-field optical scanning apparatus. Further improvement in spatial resolution will be also demonstrated via nonlinear MPA (multi-photon absorption) processes enabled by coupling ultrashort pulsed laser illumination.

7970-38, Session 9

Nanoelectronic, nanophotonic, and chemical sensing devices fabricated by nanoimprint

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Nanoimprint lithography (NIL)1 is a cost-effective nano-patterning technology based on the mechanical deformation of a resist. It has been used as the enabling technology for nano-science and nano-technology research. At HP labs, NIL enables us to fabricate applications in nano-electronics, nano-photonics and chemical sensing. For example, we fabricated a family of memristor crossbar circuits2,3 and also demonstrated the integration of memrister and CMOS circuits4. We also fabricated various types of optical metamaterials at near-IR and mid-IR using NIL. Those included metamaterials with negative “μ” at 5 μm range5, metameterials with both negative “ ” and “μ” at 1.55 μm range6. Moreover, we also demonstrated the first optical modulation of metamaterial at optical frequency7, the modulation speed record of 0.9 ps8, and the first third harmonic generation using metamaterial at optical frequency9.

Recently, we developed a process to fabricate high-aspect-ratio 3-D nanostructures using nanoimprint lithography,10 and demonstrated two types of surface enhanced Raman Spectroscopy (SERS) chemical sensing devices fabricated using 3-D NIL. By adding Au nano-particles on a 3-D polymer nano-cone array, we made it into a highly sensitive SERS sensor (figure 1). It showed a successful detection of only 200 (0.3 zeptomoles) benchmark molecules, trans-1,2-bis(4-pyridyl)ethylene (BPE). We also demonstrated a molecule trapping and sensing device based on a nano-pillar array11

Tips of the nano-pillars were coated with gold. The working schematics are shown is figure 2a&b). The solution to be detected was first dropped onto the sample. Then the pillar tips were closed under the capillary force (figure 2c&d), while the solvent evaporated. During this process, dissolved molecules were trapped in the gaps between tips, and SERS hot spots (SERS enhancement factor of 2x1010) also formed in the same places. That provides a great platform for low concentration molecule detection.

7970-39, Session 9

Wafer-level fabrication of distributed feedback laser diodes by utilizing UV nanoimprint lithography

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1. Introduction

Nanoimprint lithography (NIL) is an attractive method for fabricating diffraction gratings of distributed feedback laser diodes (DFB LDs). It takes shorter time to fabricate diffraction gratings by using NIL compared with using electron beam lithography (EBL), while NIL has high resolution comparable with EBL. We have studied NIL as a fabrication method of diffraction gratings of DFB LDs on 2-in. InP wafer. We have focused on the accuracy and the controllability of the grating period, which is an essential parameter because they predominantly influence the emission wavelength of DFB LDs.

2. Experiment

We use a reverse-tone NIL process for suppressing the inhomogeneity of residual layer thickness which leads to the variation in the figures of the transferred patterns. After imprinting, spin-coating of Si-containing resin is followed by etch-back to reveal the tops of the imprinted corrugations. Next, the revealed layer is selectively etched through to the substrate, and the formed patterns are used as masks for the subsequent etching in order to transfer the patterns to the substrate. After that, a conventional buried-heterostructure process have been used to fabricate DFB LDs.

The diffraction gratings with the period from 196 to 206 nm have been formed on a 2-in. InP wafer. The grating periods have been verified by measuring the diffraction angles of the incident light to the transferred grating patterns.

Two types of DFB LDs with different grating periods, 195 nm and 202 nm, have been simultaneously fabricated on a 2-in. wafer using this novel process in combination with the conventional fabrication process for DFB LDs. We have evaluated uniformity and stability of the characteristics of the fabricated LDs.

3. Results

We have compared the measured and the designed values of the grating periods. The error between the measured and the designed values has been less than 1%, and the variation of the periods across the wafer is less than 0.2 nm through the 6 wafers.

The oscillation spectra of the LDs with the grating periods of 195 nm and 202 nm have been compared. It is evidently shown that the peak wavelength corresponds to the Bragg wavelength of each grating period, which demonstrates that diffraction gratings are precisely fabricated by the NIL process.

We have compared the characteristics of the LDs fabricated in this study with the conventional LDs fabricated by using EBL. The histograms of the side-mode suppression ratio (SMSR) of the two types of LDs indicate that no significant difference is seen in the variations of the SMSR. The standard deviations of the LDs by NIL and EBL are 2.0 and 1.8, respectively.

We have also investigated the time-dependent change in operation current of LDs with the output power of 10 mW at the ambient temperature of 85ºC. No significant change is seen in operation current up to 5000 hours, indicating the fabricated LDs have high reliability.

4. Conclusion

Nanoimprint lithography has a high potential for the wafer-level fabrication of diffraction gratings of DFB LDs.

7970-40, Session 9

Fabrication of hole pattern for position-controlled MOVPE grown GaN nanorods with highly precise nanoimprint technology

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Nano Imprint Lithography (NIL) is a promising technology that combines low costs with high throughput for fabrication of sub 100 nm scale features. One of the first application areas in which NIL is used is manufacturing of various types of LED's. The wafers used for producing LED's are typically III/V semiconductor materials grown with epitaxial processes. These types of substrates suffer from growth defects like hexagonal spikes, v-pits, waferbowing, atomic steps and surface corrugations on a scale of few 10µm or even large islands of irregularities. The mentioned irregularities are particularly disturbing when NIL based processes are utilized to create patterns onto the wafer surface, see figure 1. The defects can have a height of several µm, which can cause large areas without nano-patterns, substrate breakage or as in the case where the stamp is applied directly onto the substrate, breakage of the stamp itself. Using Obducat's IPS®/STU® manufacturing process circumvents this since no hard materials touch each other during the entire process sequence, see figure 2. The IPS® material is flexible which allows the stamp to adjust to the curvature and roughness of the substrate, thereby giving a uniform residual layer on full wafer scale. Indeed, this is essential for high volume manufacturing where the imprinted nanostructures must have an even quality every time. In addition, this technology makes it possible to produce 8000 imprints from one single stamp.

The nanopatterns created by NIL can be applied to control metal organic vapour phase epitaxy (MOVPE) growth of GaN nanorods (NRs) containing optically highly efficient defect-free quantum discs with tunable emission wavelength [1] or core shell heterostructures [2] to improve high efficiency light emitting devices.

The nanoimprint lithography was performed using a Sindre® 400 by Obducat. A master stamp was manufactured using e-beam lithography on a Si wafer with resist and replicated to a nickel mother stamp by electroplating. The nickel stamp was then coated with an anti-adhesion monolayer of a fluorinated alkyl phosphate. The stamp had several types of patterns, but this work focuses on a pattern of 200 nm with a pitch of 400 nm and a depth of 100 nm. The substrates used were two inch sapphire substrates with a 30 nm SiO2 masking layer deposited by CVD on top a GaN layer. The substrates were spin-coated with 98 nm TU2 resist. The imprint process was optimized to give a residual layer below 20 nm with a structure depth of 97 ± 5 nm. The depth cannot be determined more accurately due to the surface quality of the substrates. An appropriate reactive ion etching (RIE) step opens the desired hole-pattern in this SiO2 layer. Hereby the quality of the subsequent MOVPE grown NRs such as e.g., position, shape, size and defect density, is determined by the highly precise NIL process.

This paper will show that NIL is an excellent and reproducible technology to produce nanopatterned GaN substrates highly suitable to grow defect free arrays of position-controlled nanorods for ultrahigh brightness LED applications.

7970-41, Session 9

Adaptation of roll to roll imprint lithography: from flexible electronics to structural templates

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Imprint lithography techniques developed at HP have demonstrated a diverse range of capabilities. Previous efforts have established methods for processing of electronics materials such as the Self Aligned Imprint Lithography (SAIL) technique for roll-to-roll processing. This approach permits a singe imprint step to create a multi level mask comprising all patterns required for subsequent etching steps, obviating the need for multiple alignment steps. In this paper the imprint lithography technique and aspects of SAIL are reviewed. New work to explore the patterning capabilities of imprint tooling for the generation of structural templates is presented. It is shown that features with aspect ratios approaching 6:1 are well within the capability of in-house methods. Subsequently, we have explored the capability of imprint processing to generate structural templates for fluid containment. Arrays of transparent well structures, formed on a flexible transparent substrate provide the basis for a color display filter matrix that is filled by inkjet deposition of pigmented resins. A particular advantage of this approach is precise color pattern definition. A separation between primary color fields of 4 microns is realized without risk of color mixing or overlap. Components patterned with high absolute precision by imprint lithography were readily integrated with parts from other sources to yield flexible color reflective display demonstrator panels. This work highlights the flexibility of imprint processing and its suitability for use with a wide variety of materials and in differing applications.

7970-42, Session 9

Development and characterization of carbon nanotubes processes for NRAM technology

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NRAM technology, a non-volatile memory based on the use of carbon nanotubes, overcomes the limitations of other memory technology types (including traditional Flash), for sub-40nm nodes, and is currently developed in manufacturing fabs.

The NRAM technology process flow involves the deposition of a film of carbon nanotubes onto silicon wafers at several of the critical layers. The carbon nanotubes, which are available in aqueous solutions, are deposited onto the wafers using spin coating techniques, the residual moisture being subsequently removed by a post apply bake. The quality and reproducibility of the carbon nanotubes layers, across wafer, wafer to wafer and lot to lot, is then of paramount importance for the overall NRAM devices performances.

In this paper, we will present the key steps of the development and characterization of carbon nanotubes processes applied to NRAM technology, focusing on specific deposition techniques, defectivity and thickness control, along with other critical integration parameters.

Traditional spin coating techniques used for polymer based micro-lithographic materials such as photo-resists and Bottom Anti-Reflective Coating (BARCs), are not suitable for aqueous solutions of carbon nanotubes; indeed, they result in excess nanotubes removal from the wafers, which is the opposite of the targeted goal. Therefore, specific spin coat recipes have been developed, consisting in a sequence of critical steps, each of them having a key role for retaining carbon nanotubes on the wafers and for controlling the post coat thickness. Detailed results will be presented, using different types of carbon nanotubes solutions, with a wide range of optical densities. The correlation between the carbon nanotube concentration in liquid (optical density @ 532nm, OD) and the post coat thickness will also be demonstrated.

Defectivity control procedures using state of the art equipment have also been developed to monitor cleanliness and overall post coat quality of the carbon nanotubes layers. Focus has been put on defects characterization: type, origin, size, and density across wafers. Post coat defectivity improvement could eventually be obtained via carbon nanotubes solutions formulation optimization.

7970-43, Session 10

New advances with REBL for maskless high-throughput EBDW lithography

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REBL (Reflective Electron Beam Lithography) is a program for the development of a novel approach for high-throughput maskless lithography. The program at KLA-Tencor is funded under the DARPA Maskless Nanowriter Program. A DPG (digital pattern generator) chip containing over 1 million reflective pixels that can be turned on or off is used to project an electron beam pattern onto the wafer. The DARPA program is targeting 5 to 7 wafers per hour at the 45 nm node, and we will describe extensions to both increase the throughput as well as extend the system to the 32 nm node and beyond.

REBL utilizes several novel technologies to generate and expose lithographic patterns at throughputs that could make ebeam maskless lithography feasible for manufacturing. The DPG will incorporate CMOS on-chip circuitry in order to provide the extremely high data rates without excessive interconnect. The exposure strategy uses a TDI (time delay integration) technique of scrolling data across the DPG in synchronicity with the stage motion, which provides both redundancy for defective pixels as well gray-level exposure control for proximity effect correction and sub-pixel edge placement. The stage will be a rotary mag-lev design that can hold and expose up to 6 wafers at a time. Wafer registration will be based on non-actinic optical metrology of marks placed on the wafers as well as on spokes between wafers.

The talk will focus on three specific areas of REBL technology. First, we have developed a new column technology based on a Wien filter to separate the illumination and projection beams (see figure). The new column design is much smaller, and has better performance both in resolution and throughput than the first column which used a magnetic prism. This column design is the first step leading to a multiple column system. Second, we will describe the rotary stage and platform which is being integrated into a functional rotary stage lithography system. Third, the latest results of a fully integrated DPG CMOS chip with lenslets will be reviewed. We have developed an array of over 1 million micro lenses which is fabricated on top of the CMOS DPG chip. The microlens array eliminates crosstalk between adjacent pixels, maximizes contrast between on and off states, and provides matching of the NA between the DPG reflector and the projection optics.

7970-44, Session 10

Large-scale eRIF implementation for sub-22-nm e-beam lithography

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Electron Beam Direct Write (EBDW) lithography is used in the IC manufacturing industry to sustain optical lithography for prototyping applications and low volume manufacturing. It is also used in R&D to develop the technological nodes ahead of mass production. As microelectronics is now moving towards the 32nm node and beyond, the specifications in terms of dimension control and roughness becomes tighter. In addition, the shrink of the size and pitch of the features significantly reduces the process window of the lithographic tools. In EBDW, the standard proximity effects corrections only based on dose modulation show difficulties to provide the required Energy Latitude (EL) for patterning the structures designed below 45nm node. A new approach is thus needed to improve the process window of EBDW lithography and, therefore, push its resolution capabilities.

In previous papers a new writing strategy based on multiple pass exposure has been introduced and optimized to pattern critical dense lines. This new technique consists in adding small electron Resolution Improvement Features (eRIF) on top of the nominal structures. Then this new design is exposed in two successive passes with optimized doses. Previous studies were led to evaluate this new writing technique and establish rules to optimize the design of the eRIF. Significant improvements have already been demonstrated in terms of Line Edge Roughness (LER), EL, CD Uniformity and Line End Shortening (LES) on SRAM and Logic structures down to the 16nm node. These results were obtained with a tool dedicated to the 45nm node. The next step of this work is thus to automatically implement the eRIF to correct large-scale layouts.

In this paper, a data preparation flow is set up to automatically implement the eRIF on sub-22nm layouts. Specific correction rules are implemented to improve the CD control and the patterning of corners and line ends. This work is done with "INSCALE", the new data preparation software from ASELTA Nanographics. The dose and the shape of the eRIF are automatically tuned to best fit the nominal design. As a result, the control of each dimension of the features is improved compared to the standard dose modulation correction. In other words, resist patterning is much more accurate, even two technological nodes below the specifications of our e-beam tool.

7970-45, Session 10

Demonstration of real-time pattern correction for high-throughput maskless lithography

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MAPPER Lithography is developing a maskless lithography technology based on massively-parallel electron-beam writing with high speed optical data transport for switching the electron beams [1]. In this way optical columns can be made with a throughput of 10-20 wafers per hour. The amount of data for each 26mm x 33mm field is 8 Tbyte. The data rate is approximately 3 Tbyte per second.

In the MAPPER tool each electron beam performs a raster scan. On each point of a 3.5nm grid the beams can be switched ON, or OFF (see figure 1). Because the grid is much smaller than the size of the electron beam, an edge of a feature can be positioned with a better accuracy than the grid size by having an ON-OFF modulation within the beam size (25nm). Also by switching OFF the beam at a few grid points effectively the dose can be lowered. This feature can for instance be used for proximity correction. In an earlier publication [2] we have stated that when proper algorithms are used to calculate the bitmap, the CDu and overlay contributions due to the finite grid size of 3.5nm are smaller than 1nm 3s. In this paper we will describe these algorithms, as well as lithographic simulations in which the CDu and overlay contributions have been calculated.

Many effects can be corrected by modifying the exposed pattern. A typical example is the proximity effect. This effect can be calculated off line because the corrections are identical for all fields and all wafers that are exposed by a certain pattern. However some corrections need to be updated for each field on the wafer. Examples are the corrections to realize overlay such as field size and shape adjustment. For this it is important that the algorithms mentioned above can be executed in real time. We will show the feasibility of real time corrections by disclosing the results of the implementation of the algorithms on an FPGA test board. Based on these experiments the required amount of FPGA resources for 10 wph operation has been determined. We will demonstrate that it is possible to build a cost competitive datapath that allows for real time corrections, and enables high throughput maskless lithography.

[1] M.J. Wieland et al, Proc. of SPIE, Vol. 7637, 76370F, (2010)

[2] M.J. Wieland et al, Proc. of SPIE, Vol. 7637, 76371Z (2010)

7970-46, Session 10

EBPC for multibeams low-kV electron projection lithography

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It is now obvious that the path leading to denser IC has become hazardous since 193nm scanners have been operating beyond their resolution limit. However if the tools that could provide photo lithographers some relief are not in production yet, luckily enough, good progresses were made in developing alternative photolithography techniques. Among them, massively parallel mask less lithography stands out as a serious candidate since it can achieve the required resolution at the right cost of ownership provided targeted throughput performance is reached. This paper will focus on this latter technique and more precisely, will report on part of the development works performed at CEA/LETI using the MAPPER technology inside the open multi-partners program IMAGINE.

Data preparation is certainly not the easiest part in the technology. Indeed, layouts are basically turned into huge bitmap streams containing the information to be sent to the thousands of parallel beams working all together to print the patterns correctly. Addressing the low energy specific case, we will study 4 different ways of performing this step involving geometrical correction with and without dose modulation or even a method using a direct inversion of the layout. We will then look into sensitivity to beam matching, overlay and stitching errors. Based on the results, we will discuss the ability of the technology to print complex logic designs at the 16nm and 11nm node.

These simulation works will be completed by model calibration results on exposed wafers with and without resist model. Then, the resulting models will be used jointly with above mentioned correction scenarios to print verification patterns at the 22nm node.

To summarize, the intention of the paper is to give a clear status towards where E-Beam Proximity Correction (EBPC) performance stands today using current MAPPER pre-alpha tool. It will also provide with some insights about how corrections will be performed on the HVM tool together with expected pattern fidelity performance at the 16nm and 11nm logic nodes.

7970-47, Session 10

Fast characterization of line-end shortening and application of novel LES correction algorithms in e-beam direct write

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For the manufacturing of semiconductor technologies following the ITRS roadmap [1], we will face the nodes well below 32 nm half pitch in the next 2~3 years. Despite being able to achieve the required

resolution, which is now possible with electron beam direct write variable shaped beam (EBDW VSB) equipment and resists [2], it becomes critical to precisely reproduce the complex pattern onto a wafer.

This exposed pattern must meet the targets from the layout in both dimensions. For instance, the end of a line must be printed in its entire length to allow a later produced contact to be able to land on it. Currently, the control of printing patterns such as line ends is achieved by a proximity effect correction (PEC) which is mostly based on a dose modification [3].

We investigated the line end shortening (LES) with a novel approach including an additional geometrical correction to push the limits of this correction and measurement algorithms. The designed LES test patterns, which aim to characterize the status of LES in a quick and easy way, were exposed with negative chemically amplified e-beam resist (nCAR) using a VISTEC SB3050DW e-beam direct writer. Figure 1 shows the designed test pattern with varying gap width, line CD and duty ratio. The evaluation of LES is performed using an Applied Materials VeritySEM4i® with an advanced measurement algorithm (figure 2).

In this paper we will discuss the current status and possible improvements of LES using different advanced correction and measurement algorithms, reaching from currently used dose modification, figure 3b, to an experimental combination of dose and shape correction. Figure 3a demonstrates the principle of how a combined correction could be applied to the line end. Finally, we show exposure results with the novel LES correction algorithms applied to a large production like pattern, figure 4, in the range of our target CDs smaller than 40nm and check its performance.

7970-48, Session 11

Formation of nanochannel silicate networks via nanoimprint lithography

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Nanoimprint lithography (NIL) has been embraced by a number of users as a practical and cost effective means for patterning surfaces. An extensive body of work compiled thus far on NIL has shown its usefulness in producing nanoscale devices and topological platforms for various surface chemistries. This paper focuses on the use of NIL to fabricate air gap and channel networks in silicate layers and demonstrates that the air gap network structures generated have desirable low- dielectric (k) properties as well as the required thermal and mechanical properties suitable for manufacturing environments. The fabrication of the 3-D device level features of the hierarchical structure, specifically buried nanochannels, are enabled through the use of nanoimprint lithography (NIL) to create sacrificial organic templates. The creation of such features is not possible using conventional photolithography techniques.

In our study, a sacrificial template approach, also known as the inorganic-organic nanohybrid technique, was applied to generate air-gaps and nanochannels by a three-step process. First, NIL was used to pattern a sacrificial polymer layer on a silicon substrate. Second, the patterned layer is coated with the silicate precursor material. Finally a high temperature treatment accomplishes complete curing of the silicate layer and concurrent removal of the organic NIL template layer resulting in the formation of a nanochannel network.

Successful fabrication required the identification of suitable organic resins for patterning by NIL. Two systems were studied in detail; a UV curable resin based upon crosslinkable acrylate monomers was developed and imprinted using UV-assisted NIL. Also thermal NIL was successfully employed using a resist composed of poly(hydroxyethylmethacrylate) (PHEMA). In both cases the NIL layer had to be designed so that it was not dissolved by solvents for spin-on-glass silicate precursor material. Two different silicate layer materials were examined, polymethylsilsesquioxane (PMSSQ) and well-ordered mesoporous silica films through the three-dimensional (3-D) replication of phase separated block copolymer templates in scCO2. The resulting nanochannel networks were examined by optical microscopy and cross sectional electron microscopy. Continuous embedded channels with widths ranging from 100 - 1000 nm centimeters in length were formed. The composite dielectric constant of these porous networks ranged from 2.2 to 2.7. Applications in nanofluidics and thin film cooling are currently being explored.

7970-49, Session 11

Self-assembly of nanocrystal superlattice films on a liquid surface

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The ability to assemble nanocrystals (NCs) into periodically ordered

structures on multiple scales and over large areas is important for electronic, optoelectronic and magnetic device applications. Here we present our recent results focusing on the self-assembly of colloidal NCs on an immiscible liquid surface under ambient conditions. First of all, we will report a multiscale periodic assembly approach induced by the rapid drying of a NC dispersion on a liquid surface, enabling the formation of stripe-patterned NC films over square centimeter areas while preserving the local superlattice structure within 15 seconds. The highly periodic stripe pattern forms spontaneously via a new type of contact-line oscillatory instability without the need of any specialized equipment or the application of external fields, with the stripe periodicity tunable on the micrometer scale by varying the NC concentration. This rapid assembly approach is compatible with heterogeneous integration processes, as the liquid-supported patterned films can be readily transferred to arbitrary substrates for characterization and device fabrication. More complicated architectures are also accessible by sequential film transfer. This assembly process is applicable to magnetic, metal, semiconductor, and dielectric NCs with different sizes and shapes, and may be extendable to other systems such as micrometer-sized colloids and polymers. The periodic structure imparts interesting modulation and anisotropy to the properties of such striped NC assemblies. The push to integrate NC films to solid state devices will be accelerated dramatically by the ability to induce order on both microscopic and nanoscopic scales and the opportunity to harness the intrinsic anisotropies in these periodically modulated NC films.

Next, we will describe a novel method to grow centimeter-scale binary nanocrystal superlattice (BNSL) membranes that can be easily transferred to arbitrary substrates. co-assembly of two types of NCs into BNSLs has recently attracted significant attention, as this provides a low-cost, programmable way to design metamaterials with precisely controlled properties that arise from organization and interactions of the constituent NC components. Different from the traditional methods in which BNSLs are exclusively grown on a solid substrate, we have explored self-assembly of multicomponent nanocrystals on a liquid surface. This new assembly strategy represents a significant advance over previous methods, as it not only allows rapid (5-10 min vs. several hours for traditional methods) formation of large-scale BNSLs, but also enables transfer of BNSLs to create unique architectures such as free-standing membranes that have not been accessible previously. Our approach circumvents the limitations (i.e., slow, substrate-sensitive, and low surface coverage, etc) associated with the current methods for growing multicomponent NC superlattices, enabling integration of large-scale BNSLs on any substrate for device applications. Fundamentally, studies of BNSL growth on a liquid surface may also shed light on the mechanisms of multicomponent NC assembly. Our method is general for a variety of nanocrystal combinations and will facilitate exploration of this new and important class of materials.

7970-50, Session 11

Nanopatterning of diblock copolymer directed self-assembly lithography with wet development

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The critical dimension required for logic and memory devices is beyond the resolution limit of 193nm immersion lithography, while next generation lithography technologies including EUV has still a lot of big challenges. Currently several double patterning techniques are most viable candidate for bridge technology, however, it causes higher cost and process complexity than single exposure lithography. Especially for beyond 20nm HP pattern formation, as double patterning scheme flow is more complex like multiple double patterning; it causes higher cost and process complexity.

Directed Self Assembly Lithography (DSAL) is an alternative and non-traditional patterning technique that will be one of the candidates for next generation lithography.

DSAL process has many technical advantageous features such as critical dimension control (5~50nm) and improved line edge roughness (~2nm 3) Furthermore, as DSAL process itself does not use exposure tool, the process cost is much lower. Thus, DSAL has great technical and economical advantages than extension of conventional lithography technologies.

Typical diblock copolymer, poly (styrene-block-methyl methacrylate) (PS-b-PMMA), is assembled during thermal process under low oxygen concentration. And then, the PMMA area is removed by O2 plasma generally. However, O2 plasma attack also etches off PS area simultaneously. As a result, the thickness of residual PS pattern is thinner and it causes degradation of PS mask performance. PS thickness loss in the device integration is not desirable as etching mask role.

In this work, we applied wet development technique which could be higher selectivity to keep PS film thickness after pattern formation. The results show that wet development technique has advantages. In addition, we challenges to apply assist process to improve the tolerance for O2 plasma of PS. We will report the availability of wet development process in DSAL pattern formation.

7970-51, Session 11

Fabrication of novel 3D structures via nano-indentation proximity field nanopatterning (NI-PnP)

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In this symposium, we will present a new fabrication technique known as Nano-Indentation Proximity Field Nano-Patterning (NI-PnP). Nano-indentations are made by first forging a diamond tip in the desired 3D shape, which is then used to make arrays of indents in a photoresist material. The resultant 2D grating is then exposed to some optical field to generate a 3D interference pattern inside the photoresist material, subsequently recorded in the same in the form of a three-dimensionally periodic structure. Since the shape of the generated interference pattern is controlled by the grating and the optical field of exposure, the ability to fabricate any arbitrary multi-level grating opens up significant design room for the fabrication of more complex 3D structures.

To fabricate a multi-level grating or phase mask with a complex 3D topology, a 3D punch in the shape of inverse replica of the unit cell of the grating is first fabricated. This is done by using focused ion beam milling (FIB) on a diamond nano-indenter tip (Fig 1a, 1b). The altered 3D tip is mounted into an AFM with a nano-indenter attachment, and is repeatedly pressed into the surface of the photoresist material (typically SU-8) (Fig 1c). The profile of the punch is replicated with precise control over the lateral position and the indentation depth.

The resultant optical grating can then be exposed to create a 3D interferogram inside the photoresist material. The interferogram and the structure subsequently recorded (Fig 1d) arise as a result of the interference between the different diffracted beams, created as the optical field interacts with the grating. The 3D interferogram created by a grating repeats itself after a set distance, known as the Talbot Distance, a function of the grating geometry, wavelength of exposure and the refractive index of the polymer. For typical binary gratings, the motif of this interferogram is a single hot spot since only a single level is ‘imaged’ inside the photoresist by the optical field of exposure. By using suitably designed multi-level gratings, the shape, size and position of the hotspots can be changed with unprecedented control. The hotspots can also be split to allow for the creation of structures with multi-point basis. This ability to fabricate complicated periodic structures opens significant avenues for the fabrication of novel photonic structures and metamaterials.

7970-52, Session 11

Double and triple exposure with image reversal in a single photoresist layer

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Double patterning has emerged as the likely lithography approach to bridge the gap between ArF immersion lithography and EUV [1]. This paper proposes a new patterning method that combines multiple (double or more) exposures with image reversal in a single photoresist (PR) layer to generate patterns decomposed in separate exposure steps. The principle of this approach consists of applying image reversal PR by first exposing the PR with the 1st mask, performing the reversal bake step and exposing the PR the 2nd time with the 2nd mask. In addition, the PR can optionally be developed after the 1st exposure before the reversal bake to generate a different pattern. The final PR pattern is determined by the properties of the image reversal PR: during the final development, the areas of PR that were never exposed, only exposed during the 1st exposure and exposed twice are insoluble. Crucially, only the PR areas exposed during the 2nd exposure (after reversal bake) are soluble. The final PR pattern after development is a composition of areas of insoluble PR segments. This technique has been extended to triple exposures where the first two exposures are conventional double exposures and the 3rd exposure takes place after the reversal bake. In conventional double exposure patterning, the final small pitch pattern is processed using two separate lithography and etching steps with a hard mask such that only larger pitch patterns are exposed . The proposed method lowers the cost-of-ownership (CoO) of double exposure significantly, since in lieu of two PR layers it uses only one PR layer. Using simple “primitive” mask patterns for the 1st and 2nd (and 3rd) exposures, the method produces complex patterns, that are impossible to obtain in a single PR layer with the double exposure technique. This approach mitigates also the diffraction distortion effects, especially for inside corners present in “+” “L” and “T” shaped pattern structures. In case of triple exposure, the diffraction rounding of the outside corners can be mitigated as well. The proposed method lends itself to a generation of composite masks by overlaying aerial images of simple “primitive” masks in the same PR layer, thus simplifying the mask design. The image reversal technique as the final step can be targeted for the resolution of the smallest features taking advantage of the negative photoresist slopes. This approach can be retrofitted into existing older generation photolithography, obviating in many cases the use of optical proximity corrections (or using OPC for further resolution enhancements) and thus boosting the yields significantly. The method shares the requirement of tight overlay accuracy approaching now 3 nm [2] with extant double exposure methods. This technique is attractive particularly for NAND, NOR, DRAM, and SRAM cell with highly regular lithography patterns. The paper provides examples for photolithography process flow reduction, mitigation of diffraction effects, and mask decomposition. The CoO comparison between the proposed vs the conventional double exposure/patterning method is also discussed in details.

[1] S. Sivakumar, Proc. IEDM, p. 1-4, 2006; K. Ushida, ISSM, p. Iv-Ix, 2006

[2] W. H. Arnold, Proc. SPIE, v. 6924-04, 2008

7970-53, Session 12

The effect of wear of atomic force microscope probes in scanning probe-based nanolithography

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Scanning probe based patterning processes are gaining attention due to the potential for realizing small feature sizes. While these processes are increasingly being used in a range of applications in research and development settings, widespread industrial use has been hampered by a number of factors, including the mechanical degradation and wear of the probe tip. In this work, we examine the wear of atomic force microscope probes and assess the effect of wear on patterning performance.

Specifically, the wear of atomic force microscope probes made of conventional probe materials, including silicon and silicon nitride, and the performance of diamond like carbon coated probes were evaluated experimentally. Mechanics modeling was used to connect the measured wear performance to material properties and scanning conditions. Implications of this work on the implementation of scanning probe based nanolithography processes will be discussed.

7970-54, Session 12

Tunable two-mirror laser interference lithography system for large-area nanopatterning

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Laser interference lithography is an effective, inexpensive, and convenient approach in preparation of large-area uniform nanostructures and photonic materials. By the geometrical configuration of multiple beams combined with single exposure or multiple exposures, interference lithography has been used to fabricate two-dimensional or three-dimensional nanostructures. Two common interferometers that have been used successfully for interference lithography are the Lloyd-mirror and the Mach-Zehnder interferometers. A Lloyd-mirror interferometer consists of a mirror attached perpendicular to the substrate holder, where an angular rotations results in a simple and fast nano-patterning of controlled pattern periodicity. However, the size of patternable area is limited by the coherent length of a laser and the size of a mirror: that with low periods is mainly limited by a coherent length while that with high periods is limited by the size of a mirror. To produce the periodic nano-patterns over a larger sample area, a Mach-Zehnder interferometer has been used. However, it lacks the tunablility of pattern periodicity, requiring laborious optical path reconfiguration to modify the pattern periods. A large optical table is also necessary for the flexibility of the setup and a costly high power laser is required to provide enough power for expanded beams travelling a large distance.

In this work, we have designed, constructed, and tested a novel, compact and tunable interference lithography system featured with both the simplicity of a Lloyd-mirror interferometer and the large-area patterning capabilities of a Mach-Zehnder interferometer. In the new system, a laser beam is split into two beams and a rotational mirror is introduced in the path of each expanded beam. Each mirror can be individually regulated to a specific angle for a designed period, which allows the convenient tunability of pattern periodicity without losing the patternable area. Experimentally, we used a HeCd laser of 325 nm in wavelength as a radiation source, whose effective coherent length is about 10 cm to define interference patterns of the critical contrast of 0.8. The whole setup was currently installed on a small 4’ × 8’ table. By using a square mirror larger than 10 cm in a side, uniform nano-patterns are theoretically obtainable in the sample area larger than 10 cm × 10 cm for a wide range of pattern periods. Various nano-patterns (line, dot, and pit) of resist materials with controlled film thickness were fabricated on a 4” silicon substrate at regulated periods of 250, 500, and 750 nm. Uniform patterns covered the entire surface area for each period, which is in good agreement of the theoretical calculations. This new two-mirror interference lithography system has demonstrated to be a robust, simple and relatively inexpensive approach for large-area nano-patterning with great tunability in pattern periodicity. This unique capability will allow new scientific and engineering applications requiring well-regulated nano-patterns over a large surface area such as photonic devices.

7970-55, Session 12

Solid-immersion Lloyd's mirror as a testbed for plasmon-enhanced high-NA lithography

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We describe a new cost-effective technique to perform high-NA interference lithography based on the Lloyd's mirror that requires only the use of a high index prism, index matching liquid and a coherent laser source.

The method is similar to other two-beam solid-immersion lithography schemes [1-3], but eliminates the need for beam splitters, a beam block and some steering optics.

The system (shown in supplement file), builds upon the traditional Lloyd's mirror by coating one side of a high index prism cube with a reflecting material such as Aluminum, thereby creating a solid-immersion equivalent. The requirements for such a system are that the prism has low index inhomogeneity, low absorbance (high transmission) in the wavelength of interest, low birefringence and be capable of withstanding a specified amount of stress during sample mounting. In our case we have used Yttrium Aluminum Garnet (YAG) as the prism material, which has a refractive index of 1.87 at 365nm and negligible absorption, no birefringence, high durability, transmission in the 250nm to 5um range and easier surface polishing than sapphire. Anti-reflection coatings can be designed to ensure maximum transfer of incident power through the prism sidewalls hence reducing spurious reflections. Although we have designed the system at a wavelength of 365 nm, the idea is easily extended for 193 nm imaging using a Lutetium Aluminum Garnet (LuAG) prism material [2].

The system has been designed to allow measurement of plasmonic assisted improvements to high-NA lithography. One of the improvements that we want to verify is the use of metallic under-layers that enhance the evanescent near-fields giving a better depth of focus under ultra high-NA imaging conditions. For the 365nm proof-of-concept, silver (= -2.7 + 0.23i) can be used as the reflecting under layer and by using a high index matching fluid, a grating pattern can then be imaged into the photoresist with the Lloyd's mirror. The imaging relies on the fact that the negative real part of the permittivity of metal allows reflections that are much larger than unity in the evanescent regime, and examples of the expected intensity profiles in 50-nm thick resist at an NA=1.85 in the system are shown in the supplement file. A high contrast image does not extend all the way into the resist layer with an index-matched bottom layer, but it does with the plasmonic bottom layer added. Ideally we can tune the permittivity of the metal layer to optimize it for individual numerical apertures, however in practicality, silver stands out to be a good candidate in terms of providing a near-uniform reflection for a wide-range of numerical apertures.

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7970-57, Session 12

Soft UV-NIL at the 12.5-nm scale

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Nanoimprint lithography (NIL) has proven its ability for high resolution replication already in the mid 90's by S. Chou's group [1][2]. Still, being a competitive candidate for "next generation lithography" (NGL), nanoimprint lithography has to overcome central limitations such as master lifetime, cost of ownership - and defectivity. One of the biggest advantages of NIL as NGL lithography technology is the resolution capability.

The resolution achievable in the entire nanoimprint technology rises and falls with the master manufacturing process. Resolutions in the sub 15 nm scale requires lithography processes such as electron beam lithography or in this particular case charged particle nano patterning (CHARPAN) [3]. CHARPAN uses massively parallel ion beams either exposing a resist or directly patterning a substrate. Herein silicon wafers with hydrogen silsesquioxane (HSQ) resist are used as master stamp materials. The resist is directly exposed using 10 keV H3+ ions and can be used as master stamp directly after development without any subsequent reactive ion etching. Direct replication with this valuable and time consuming master may cause damage or contaminations. To be able to use this master for direct replication, there is the need of anti sticking coatings to guarantee a reliable, defect free and easy separation between master and cured polymer. Soft UV-NIL [4] [5] is considered to be one of the most promising candidates to overcome these major limitations pushing NIL towards high resolution production solutions for various applications. Soft copies as intermediate stamp dramatically increase the lifetime of the expensive high resolution master and decrease process costs at the same time, as they can be used for multiple imprints without applying anti sticking coatings. We used the NIF-A-10a stamp polymer from Asahi Glass Co. Ltd, which was cast in a puddle on the stamp master and contacted uniformly with a carrier substrate, which was pre-treated with a primer. Central issues in the soft stamp fabrication process are to tune the stamp polymer in such a manner that it can resolve high resolution features and to ensure an easy and defect free release from the imprint resist. On the other hand this low surface energy material should have sufficient bond strength to the carrier substrate for a reliable and continuous operation mode without de-lamination. The obtained soft stamp constitutes a negative of the master with improved surface energy, UV transparency and elastomeric modulus. For the imprint process the commercially available imprint resist mrUVCur06 from Micro Resist Technology was spin coated on a 4" Si wafer, which was treated with an adhesion promoter. Then, the soft working stamp without anti sticking coating is brought into uniform contact with the resist layer and the resist is cured by UV polymerization through the transparent working stamp using a commercial available Nanoimprint tool from EVG. Finally, the working stamp is separated from the imprinted substrate, resulting in an imprinted resist layer which is the negative counterpart of any topography preserved on the stamp surface.

This work demonstrates highest resolution master manufacturing and imprint lithography on 12.5 nm half pitch (hp) features using soft polymeric stamps. It addresses so far unmet needs making NIL a highly interesting candidate for "next generation lithography" regarding resolution, cost of ownership, master lifetime and process reliability.

The work was funded by the Austrian nanoinitiative (www.nanoinitiative.at, FFG and bmvit) through the NILaustria project cluster (www.nilaustria.at).

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7970-69, Session 12

Molecular models for study of directed assembly with copolymers: method and applications

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Recent studies have established that directed assembly with block copolymers can be used to create device-like structures with levels of perfection and registration that warrant their consideration for commercial fabrication processes. A number of applications of block copolymer directed assembly are currently being evaluated, for example for production of high-density storage media. Such applications generally rely on the concept of density multiplication, which includes the creation of a relatively sparse pattern on a substrate and the addition of information to the patterning process by the block copolymer material itself. Applications also rely on the use of complex multicomponent blends and the hierarchical assembly of the relevant materials. The diversity of substrate patterns and materials choices available to block copolymer directed assembly necessitate that molecular-level predictive methods be developed to design effective patterning strategies in-silico. Without these, the parameter space available for examination would be difficult to explore. In this work we will present a formalism that relies on molecular modeling to predict the morphologies and structures that arise in block copolymer directed assembly. The capabilities of the formalism will be demonstrated in the context of several specific examples of industrial relevance. The validity of theoretical calculations will be established by direct comparison to experimental data. These examples will include i) formation of cylindrical structures in density multiplication, ii) a comparison of the effectiveness of topographic and chemical patterning strategies, iii) the formation of spherical phases in honomegenous and non-homogeneous chemical patterns, and iv) studies of the advantages and disadvantages of relying on complex multiblock materials, including triblock and pentablock copolymers.

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7971-01, Session 1

Semiconductor metrology from new transistor and interconnect materials to future nanostructures

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No abstract available

7971-02, Session 2

A holistic metrology approach: hybrid metrology utilizing scatterometry, CD-AFM, and CD-SEM

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Shrinking design rules and reduced process tolerances require tight control of CD linewidth, feature shape, and profile of the printed geometry. Various critical dimension (CD) metrology toolsets like Scatterometry, CD-SEM and CD-AFM are typically utilized individually in fabs. There's no "accurate metrology"; all metrologies differ from each other. Each of these toolsets has its own set of limitations, merits and assumptions in optimization algorithms. For example, correlation between geometric parameters, variation in material properties (n&k), and long model optimization time limits scatterometry metrology. Similarly, the shrinkage phenomenon, charging effect, and profile variations negatively impact measurement performance of the CD-SEM toolset. CD-AFM suffers from issues such as tip wear, tip characterization, low throughput, and inaccuracy in measuring dense structures and at the bottom of the profile. At the same time, these toolsets have their own application set where they perform better relative to others, e.g. direct product measurement (CDSEM), profile metrology (Scatterometry and CDAFM), etc.

Uniting several metrologies into a single result gives a new meaning to the term "metrology". It is an enabler to getting a single combined result from different metrologies. We define "Hybrid Metrology" to be the use of any two or more metrology toolsets in combination to measure the same dataset. Data from one toolset can be exchanged with another toolset and used in a complementary or synergistic way in order to improve the overall measurement performance. A possible example would be using sidewall angle profile measured with CD-AFM/scatterometer to fine-tune the CD measurement algorithm of the CD-SEM.

Here we demonstrate the benefits of the Hybrid Metrology for Scatterometry in two embodiments: Offline during recipe setup and Online during actual measurement. We use as a test vehicle a relatively complex application: the litho anchor structure for 20 nm Optical Proximity Correction (OPC). These anchor structures are traditionally measured using CD-AFM, and play a critical role in OPC modeling and simulations. However, as the design rules shrink and these structures become denser, it has become very difficult for CD-AFM to provide accurate CD and profile data by itself. Scatterometry is called upon to support CD-AFM (and possibly CD-SEM) for this application.

As presented in our previous paper [1], adding more information from different sources like multiple targets, reference data from other toolsets, etc. is the answer to the scatterometry conundrum of improving both accuracy and precision simultaneously. This is the Holistic Metrology approach. As part of this approach, algorithms for Hybrid Metrology allow is to include external measurement data (CDSEM, CDAFM) within the Scatterometry recipe. On one hand, the external measurement data is used during the recipe setup phase. This allows for 1) more accurate modeling and 2) reduction of model optimization time. On the other hand, external measurement data is used during the real-time measurement phase, providing 3) increased recipe robustness and 4) reduced inter-parameter correlation during the actual measurement on the tool.

This paper will cover measurement results obtained using typical BKM as well as those obtained by utilizing the Hybrid Metrology approach. Measurement performance will be compared using various metrology metrics for example total measurement uncertainty (TMU).

7971-03, Session 2

In-situ CD control with spectroscopic ellipsometry

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Thermal processing of semiconductor substrate is common and critical to photoresist processing in the microlithography sequence [1]. As the feature size continue to scale down, the chemically amplified resist (CAR) has emerged as an alternative to the traditional novolak-based resist for DUV lithography. This positions the post exposure bake (PEB) as the most important thermal processing step among all as it activates the acid-catalyzed de-protection mechanism and causes the exposed resist to be soluble during the development process [2].

Earlier works demonstrated the feasibility of spectroscopic ellipsometry in measuring the CD profiles as well as to monitor the changes in the resist film during PEB and extract data for simulation [3]-[6] due to desirable merits: fast, nondestructive, sensitive and easy to integrate into the existing production line. Strong correlation between de-protection induced thickness reduction and amplified chemical reaction in the exposed area of the chemically amplified resist (CAR) during post-exposure bake (PEB) also has been established [7]-[9] and most importantly, the optical properties of the resist film due to the thickness reduction can be detected using a spectroscopic ellipsometer.

In this paper, a confocal ellipsometer based on the rotating polarizer configuration is developed and a proposed control scheme is presented for signature profiles matching to optimize the process control. The load during the process varies due to variations in the initial photoresist thickness prior to PEB and in order to maintain the same thickness reduction ratio, thus the end thickness of the photoresist (set point) varies from wafer-to-wafer. The ellipsometer monitors the de-protection process in real time and the reflected spectrum is used to compute the signature plots, and . The mean square error (MSE) between the measured and the desired signature profiles is computed and based on the magnitude of the MSE, a control signal is generated to alter the bake plate temperature set point. The proposed control scheme is aimed to reduce the statistical error functions derived from the signature profiles.

Figure 1 compares the response of the controlled signature plots with respect to the reference signature profiles. From the figure, it can be seen that without deliberate control, the shift of the signature profiles for the reference wafer is considerably uniformed throughout the entire PEB cycle. With the intervention of active control, the gap between measurements for the signature plots varies accordingly with respect to the elevation of baking temperature. Figure 2 shows that the signature plots for wafers under controlled environment are able to converge in a group within a tighter band. The uncontrolled wafers during PEB depict a more erratic behaviour indicating significant CD variance from wafer to wafer. With the implementation of the proposed control scheme, the improvement of wafer-to-wafer critical dimensions (CD) uniformity is approximately 5 folds.

7971-04, Session 2

Litho process control via optimum metrology sampling while providing cycle time reduction and faster metrology-to-litho turnaround time

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In keeping up with the tightening overall budget in lithography, the metrology requirements have already reached a deep sub-nanometer level. This drives the need for clean metrology (resolution and precision). Authors have already published results of a thorough investigation of a scatterometry-based platform from ASML showing promising results on resolution, precision and tool matching for overlay, CD and focus.

But overall requirements are so extreme that all measures must be taken in order to meet them. In light of this, parallel to above mentioned need for resolution and precision, the speed and sophistication in communication between litho and metrology (feedback control) are also becoming increasingly crucial. An effective sampling strategy for metrology plays a big role in this is.

In this study authors would like to discuss results from above mentioned scatterometry-based platform in light of sampling optimization. For overlay, various sampling schemes (dense / sparse combinations as well as inter and intra field schemes) were used on many production lots and effectiveness of such sample scheme was studied to reveal an ideal sampling scheme that can result in 0.5nm to 1nm gain in overlay control (compare to today's practice). A study was also performed for focus and dose monitoring based on metrology data. Cycle time contribution of metrology (at litho) in overall cycle time of a full process flow was investigated and quantified with the concept of integrated metrology. Results indicated a cycle time reduction per layer (if an integrated concept is used) of 3 to 5 hours, which can easily add up to several days of total cycle time reduction for a fab.

7971-05, Session 2

Mask registration impact on intrafield on-wafer overlay performance

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Improved overlay performance is one of the critical elements in enabling the continuing advancement of the semiconductor integrated circuit (IC) industry. With each advancing process node, additional sources of overlay error and new methods of reducing those errors need to be taken into account. In this work we consider the impact of mask registration or pattern placement errors on intra-field on-wafer overlay performance. Mask shops measure mask registration at rather low sampling rate and this data has historically not been incorporated into the wafer fab overlay data systems. In this work we consider mask-to-mask overlay and point out the importance of high density sampling as well as the potential for improved mask qualification and disposition. We also investigate the correlation of mask registration and wafer overlay including comparisons of both scribe-line dedicated overlay targets as well as in-die device patterns. From these results we suggest possible improved analysis and implementation techniques for improved overlay performance.

7971-06, Session 2

Application of mask process correction (MPC) to monitor and correct mask process drift

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Temporal drift in the mask manufacturing process has been observed in CD measurements collected at different times. Most of this is corrected through global sizing and dose adjustments resulting in small mean-to-target (MTT) residual errors. However, this procedure does not account for a detectable change in the proximity behavior of the mask process. This paper discusses a procedure for detecting and monitoring the proximity behavior of a process using an targeted sampling plan. It also proposes a procedure to correct for drifts in proximity behavior if it is predictable and systematic.

7971-07, Session 3

Subnanometer line width and line profile measurement for CD-SEM calibration by using STEM

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The novel method of sub-nanometer accuracy (uncertainty) for the line width and line profile measurement using STEM (Scanning Transmission Electron Microscope) images is proposed to calibrate CD-SEM line width measurement. In the proposed method, the traceability and reference metrology of line width and line profile are established using Si lattice structures and the uncertainty evaluations.

A specimen of Si line and space is sliced on Si 110 surface as a thin specimen of 100 nm thickness by FIB (Focused Ion Beam) micro sampling system. Then the bright-field and dark-field STEM images of the specimen are obtained by STEM (HD-2700) with accelerating voltage of 200 kV and magnification of x150,000. The high magnification STEM images show Si lattice structures clearly.

From the images, the line profile is detected the following procedure:

1) The STEM image is transformed to the frequency domain image by 2D-FFT (Fast Fourier Transform). The peeks of the frequency domain image indicate the image magnification and inclination angle of the STEM image by the relationship between the Si lattice structure and image pixels.

2) The images are rotated by the inclination angle. Therefore, the positions of Si lattice are on the same line of the image with distances of Si lattice size.

3) The size of image pixel is evaluated comparing with Si lattice size and the uncertainty of the size and image magnification is evaluated.

4) A novel noise reduction method using Si lattice structures is proposed. In the method, the image contrast within Si lattice area is increased and the edge of Si lattice area is clearly recognized.

5) The edge position on the each Si lattice line is defined at the 50% intensity between outside and inside of Si lattice area.

6) The thickness of oxide film of Si line is evaluated. Then the detected line profiles are compared with the measurement results by CD-SEM and CD-AFM.

We applied the above methods to the 45 nm Si line width standard. The edge position on each Si lattice is calculated and the edge positions of line profile are estimated. The standard deviation of the edge positions is less than 0.1 nm. The expanded uncertainty of the line edge positions is evaluated from the uncertainty contributors of repeatability, image magnification, Si lattice counting by edge detection, environmental condition and so on. The contributors of Si lattice counting and image magnification are estimated as the large uncertainty contributors in the case. From these calculation, the expanded uncertainty (k = 3) will be estimated less than 0.5 nm (3 sigma).

In future works, we will evaluate the thickness of oxide film of Si line and compare the line profile by STEM images using the proposed method with the measurement results by CD-SEM images and AFM images on the same line position. Then the detailed estimation of the uncertainty of the proposed method is calculated for establishment of the traceability and the reference metrology of the line width measurement.

7971-08, Session 3

Challenges of SEM-based critical dimension metrology of interconnect

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Semiconductor technology is advancing below 50 nm critical dimensions bringing unprecedented challenges to process engineering, control and metrology. Traditionally, interconnect metrology is put behind high-priority gate metrology; however, considering metrology, process and yield control challenges this decision is not always correct. Optical critical dimension (OCD) diffraction microscopy is working its way to interconnect manufacturing process control, but scanning electron microscopy (SEM) remains the number one critical dimension (CD) metrology for interconnect process engineering and optical proximity correction (OPC) modeling. Recently, several publications have described secondary electron (SE) trapping within narrow high-aspect ratio interconnect structures. In these papers, pre-dosing of the sample helped to extract SE from the bottom of the hole and measure its diameter. Based on current understanding of the phenomenon, one should expect that high-aspect ratio interconnect structures (holes and trenches) with critical dimensions below 100 nm may show signs of SE trapping of various degree. As a result, there may be an uncontrolled effect on SE waveform and, therefore, bias of CDSEM measurement. CD atomic force microscopy (AFM) was employed as a reference metrology for evaluation of uncertainty of interconnect trench and hole measurements by CDSEM. As the data indicates, CDSEM bias shows a strong dependence on pitch of periodic interconnect structure starting from drawn CD of 50 nm. This corresponds to a trench profile aspect ratio of 3:1 which is significantly less than 7:1 for reported earlier contact holes case. CDSEM bias variation for the evaluated set of samples is about 20 nm. The measurement uncertainty of interconnect holes by CDSEM is also in question. Reference CD metrology of holes is a big challenge. TEM measurements of the diameter of the hole may not be accurate enough for several reasons: material shrinkage during sample preparation, difficulty of sample cut positioning, unknown hole-to-hole local variation, and hole sidewall roughness. CDAFM of 50 nm holes is also quite challenging because of finite probe diameter, potential probe bending and sticking to the hole walls. A typical OPC sample consists of both photoresist and etched interlayer materials. Traditionally, many through pitch CD structures are measured to obtain a large enough data set to get an accurate model. For proof of concept, ten pitch structures at constant CD were chosen for measurement. As the AFM data indicates, the hole diameter changes quite significantly with depth and the hole profile varies from one OPC structure to another. So far, our attempts to extract reliable and reproducible bottom hole diameters from the SEM signal have failed. Abe et al. have used a clever way to correlate physical bottom diameter of holes with CDSEM measurements and demonstrated that for their process and dimensions the SEM “top” diameter and physical bottom diameter correlate well. This conclusion can’t be generalized and MU of CDSEM must be evaluated on an individual technology/process basis. A more general approach to improve CDSEM accuracy is necessary which is based upon reproducible CDSEM measurements, modeling and correction. The work is in progress.

7971-09, Session 3

Robust edge detection with considering three-dimensional sidewall feature by CD-SEM

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In the critical dimension scanning electron microscope (CD-SEM) measurement of LSI patters, higher precision is required with the scaling in device size. Signal averaging is often used to improve the precision; however, it cannot be applied in the measurements of local pattern feature such as short line’s CD or two-dimensional pattern shape. Accordingly, the image noise is the largest obstacle in these local measurements. In addition, there is a demand for extraction of the z-coordinate (i.e., the perpendicular direction to the wafer plane) of the obtained pattern-edge.

Pattern edge is usually determined as the position where the CD-SEM signal-intensity equals to the user-defined threshold level. To minimize the image-noise influence, it is recommended to define the threshold as the level where the slope of the signal profile is the steepest. However, it is not practical since the feature of the signal profile varies along the edge and the threshold level of 50% is often used. Regarding z-coordinate of the edge points, several analyses can calculate CD as a function of z from a signal profile, but they need an image with a high signal-to-noise ratio [1, 2].

To solve the above-described problems, we propose an easy method using the threshold-level (T) dependences of bias-free line-edge roughness (LER) and of LER bias [3]. T-dependence of bias-free LER shows similar characteristics with the z- dependence of sidewall roughness. LER bias becomes large where the sidewall is rough or tapered. Taking advantage of these features, we define the best threshold as the level where the bias-free LER is stable and the LER bias is the minimum. By using the obtained best threshold, the influence of the noise on the edge position can be minimized (i.e., achieve the best repeatability) in measurements of other patterns if the patterns fabricated with the same process have the similar T-dependences of bias-free LER and of LER bias.

To confirm the validity of the proposed method, samples of step-shaped silicon lines and resist lines were fabricated. The silicon sample was observed with CD-SEM and AFM. A step on the sidewall was clearly recognized in LER bias graph, and the best thresholds for extracting the edges were found at upper and lower position of the step level. It was confirmed that the best threshold obtained by the proposed method actually gave best repeatability in local line width measurements of resist sample. The repeatability (3sigma) was less 40% of the value obtained by the conventional threshold level, 50%. These results show the possibility of the proposed method in optimization of CD-SEM parameters to achieve high measurement repeatability with considering three-dimensional structure.

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7971-10, Session 3

Tool-to-tool matching issues due to photoresist shrinkage effects

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Photoresist shrinkage is an important systematic uncertainty source in critical dimension-scanning electron microscope (CD-SEM) metrology of lithographic features. In terms of metrology gauge metrics, it influences both the precision and the accuracy of CD-SEM measurements, while locally damaging the sample. Minimization or elimination of shrinkage is desirable, yet elusive. This error source will furthermore be a factor in CD-SEM metrology on such polymer materials, such that learning to work around this issue is necessary.

Tool-to-tool matching is another important component of measurement uncertainty that metrologists must control in high volume manufacturing, and photoresist samples are a most difficult case due to shrinkage effects, as tool-to-tool biases can vary based on the sample or other parameters. In this work, we explore different shrinkage effects and their influence on matching. This will include an investigation of how the photoresist shrinkage rate varies with time from the chemical development of the photoresists, which necessitates that measurements on different tools within a group be performed in rapid succession to

avoid additional error. The differences in shrinkage rates between static and dynamic load/unload cases will also be addressed, as these effects should also influence matching. Finally, various sampling schemes for matching will be explored, through both simulation and experiment, for use with shrinking materials. Included is a method whereby various fleet tools measure different locations, once per tool, within a uniform line/space grating [1]. Finally, we will assess how well matching can be achieved using these techniques.

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7971-11, Session 3

Influence of the charging effect on the precision of measuring EUV mask features

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Precision of measuring EUV mask CD is becoming more important as the adoption of the EUV lithography for high volume manufacturing is expected to be dragged on to 2x nm node and beyond. We reported in BACUS 2007 that the dimensions of EUV mask features continuously measured by CD-SEM gradually varied because of the charging.

The effect of charging on the measured CD variation mainly consists of three factors: 1) shift of the incident points of primary electrons deflected by the surface charge, 2) distortion of the profiles of secondary electron signal intensity caused by the deflection of the secondary electrons, and 3) deviation of the threshold points or the maximum slope points of the secondary electron signal intensity profile due to the variation of the image contrast.

Contribution of each factor to the measured CD variation was analyzed using Monte Carlo simulation considering the charging effects. The region near the mask surface is positively charged as the secondary electrons escape from the sample. The escape depth of the secondary electrons is supposed to be less than a few nanometers. On the other hand, primary electrons penetrate into deeper regions and the regions are negatively charged.

If the capping layer is composed of silicon, the region from the surface to the depth of about 2nm can be considered to be naturally oxidized. The surface of the tantalum-based absorber is also oxidized. The density of positive charge at the absorber surface is supposed to be higher because the secondary electron yield of the tantalum oxide is higher than that of silicon dioxide. However, the electrical field intensity just above the absorber surface is much lower than that of silicon dioxide surface because the permittivity of the tantalum oxide is much higher than that of silicon dioxide.

As a result, high field region just outside the mask surface is distributed in the space between sidewalls rather than the absorber surface. The secondary electrons emitted from the sidewall tend to be more dragged into the capping layer surface by charging. This causes the distortion of the white band and it results in the increase in space CD, and the decrease in line CD. This is the major contribution of the measured CD variation.

The deflection of the primary electrons really exists but its contribution to the measured CD is rather small. It is because the high electric field region is concentrated between the side walls rather than above the absorber patterns.

The deviation of the maximum slope points in the SEM signal profile which determine the pattern edge also has some contribution to the variation of measured CD. It is because the SEM image contrast change affects the positions of the pattern edges determined through smoothing and differentiating procedures. However, this variation can be minimized by using the appropriate weighted average in the smoothing procedure.

For those three factors described above, how the materials constants affect the CD precision measured by CD-SEM is discussed.

7971-12, Session 4

Optical illumination optimization for patterned defect inspection

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We demonstrate performance gains using scatterfield microscopy techniques for die-to-die defect comparison metrology. Scatterfield microscopy enables design-specific bright field optical tools for use in signal-based defect analysis of features with dimensions well below the measurement wavelength. Central to this approach is engineering the illumination as a function of angle and analysis of the entire scattered field. This methodology has been incorporated into simulations that demonstrate improvements in defect inspection for various defect types on the Defect Metrology Advisory Group (DMAG) intentional defect array (IDA) wafers.

Theoretical simulations reported here were carried out using a fully three-dimensional finite difference time domain (FDTD) electromagnetic simulation package. Comprehensive modeling was completed investigating angle-resolved and polarization-resolved illumination to enhance defect detection for the 13 nm line-width logic-poly stack. Oblique incidence is compared against more conventional, normal incidence illumination. Angle and polarization resolved enhancements and defect sensitivity gains are identified and presented in this report.

Comprehensive modeling to investigate a range of illumination wavelengths to enhance defect detection for several defect types was completed. Simulations were performed to evaluate performance gains obtained at wavelengths ranging from 193 nm to 450 nm. The data show that many defects are more detectable when using the shorter 193 nm or 266 nm illumination wavelength. However, identification of an optimum wavelength between 193 nm and 266 nm cannot be determined without consideration of the process stack, materials, defect type and directionality, incident angle, and polarization.

Experimental confirmation of these simulation results is ongoing as of time of abstract submission. The current 193 nm Scatterfield Microscope at NIST has yielded images of the IDA 65 nm logic-poly stack. This instrument represents a substantial effort at a ground up custom tool design and construction. Experimental efforts are focused toward the validation of simulation results, essential for confirming shorter measurement wavelength and oblique illumination performance gains for some process stacks and to provide direction for the extensibility of optical defect detectability.

7971-13, Session 4

Wafer noise models for defect inspection

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The ability to simulate patterned wafer inspection microscopy is important to guide equipment design and development, with defect signal or signal-to-noise being the key output metric. Prior simulation work has focused on system noise, for example detector dark current, as the primary contributor to the noise denominator. With the introduction of aggressively low k1 lithography and other types of pattern processing that induce high local variations either upon the industry or on the near horizon, the contribution of wafer noise, defined loosely as non-yield impacting pattern or process variation, is becoming a significant if not the dominant noise element. Quantitative noise models which accurately represent these local process variations are required to support simulations that seek signal-to-wafer-noise outputs.

The present work develops structural models for line edge roughness (LER) and surface roughness. Line edge roughness is described by the movement of the line center and variation in CD. Correlation length and variation are measured for both of these parameters at a representative lithographic step on best and worst case samples which are fed forward into a random LER generation algorithm that produces example

structures mimicking the correlation length and the variation of the sample's CD and line center undulations. Film roughness models are developed following a similar methodology with the RMS film height and correlation length being the parameters measured from a representative film.

FDTD simulations are performed on the structures generated from the LER model to compute the aerial images of the structures in the image plane of a wafer inspection microscope. The relationship between the various model parameters and defect signal-to-wafer-noise are explored for advanced design rule structures in brightfield and darkfield imaging modes across a range of wavelengths, with conclusions being drawn regarding the wafer inspection sensitivity process window across LER skews.

7971-14, Session 4

Quantitative measurement of voltage contrast in SEM images for in-line resistance inspection of incomplete contact

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SEM inspection using voltage contrast has the capability to detect electrical defects, whose voltage contrast formed in SEM images appears to vary. The authors have already reported that the gray scale of SEM images depends on variation in contact resistance due to incomplete contact between a contact plug and a silicon substrate [1]. However, contact resistances that appear as a difference in gray scale are not quantitatively estimated during conventional in-line inspection. Accordingly, we recently developed an in-line inspection method for partial electrical measurement of contact resistance, which is quantitatively estimated from the voltage contrast formed in an SEM image of an incomplete-contact defect.

In a previous study, we calibrated the contact resistances of an incomplete-contact defect from gray scales of a defective plug deliberately formed on standard calibration wafers for estimating voltage contrast [2]. However, it was difficult to inspect manufactured patterns for various devices, but it was difficult to inspect patterns for test-elementary-groups. This is because the gray scales of normal-contact plugs and defective plugs formed for manufactured devices may vary according to the resistances between the normal contact plugs and the backside wafer. The gray scales of the defective plugs depend on the electrical characteristics of the circuits connected under the plug pattern.

In the present study, we developed a method for estimating defect resistances from the gray scale of voltage contrast formed on manufactured patterns for various devices. This method applies a circuit simulator (which is already reported [3]) that calculates the charging voltage for the patterns and the intensity of the secondary electrons according to an equivalent circuit model. To accurately estimate the resistance of defects formed in a device, the simulator was improved by considering the variation of defect resistance, which strongly depends on the differential voltage between the plug surfaces and the backside wafer. For example, the resistance of the deliberately formed defect was changed from 1E13 to 1E8 Ω, when the differential voltage was varied from 0 to 4 V.

With this method, at first, two I-V characteristics, namely, resistances between the plug surfaces and the backside wafer, are measured by nano-prober [4]. One is the I-V characteristic of the deliberately formed defect on the standard calibration wafers; the other is that of a normal-contact plug formed in the inspected patterns. Next, the calibration curve for the inspected patterns is calculated from the measured resistances obtained from the two measured I-V characteristics.

The inspection method was applied to estimate the resistance of defects formed on an SRAM pattern. The calculated calibration curve is used to accurately estimate the defect resistance (with an accuracy of about an order of magnitude) from the voltage contrast formed on the defects in the inspected SRAM patterns.

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7971-15, Session 4

Characterization of EUV resists for defectivity at 32 nm

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Extreme ultraviolet (EUV) lithography is considered as the leading patterning technology beyond the ArF-based optical lithography, addressing the need for transistor densification to meet Moore's Law. Theoretically, EUV lithography at 13.5nm wavelength can meet the resolution requirements for 1xnm technology nodes. However, there are several major challenges in the development of EUV lithography for mass production of advanced CMOS devices. These include the development of high power EUV light sources, EUV optics, EUV masks, EUV resists, overlay accuracy, and metrology and inspection capabilities. In particular, it is necessary to ensure that effective defect control schemes will be made available to reduce the EUV lithography defectivity to acceptable levels.

This paper presents a study on the defectivity and characterization of patterned EUV resists, with the objective of providing a quantitative comparison between the defectivity of different resist materials and different stacks. Patterned defectivity wafers were printed using the ASML EUV full-field Alpha-Demo Tool at imec (0.25NA). The EUV resist patterns consisted of 32nm Line/Spaces. Several of the most advanced resist types and underlayers were screened experimentally. The different resist types and stacks were inspected using a DUV laser based Brightfield inspection tool (UVisionTM, Applied Materials), followed by SEM defect review (SEMVisionTM, Applied materials) and CD metrology measurements (VeritySEMTM, Applied Materials). The patterns were characterized in terms of defect types and defect density.

We identified the major defect types and discuss factors that affect the defectivity level and pattern quality, such as resist type, and exposure dose and focus. Scattering analysis using DUV polarized light at different polarizations was performed, to indicate on the inspection performance trends for a variety of defect types and sizes of the different resists and stacks. The scattering analysis shows that higher defect scattering is induced using polarized light.

7971-16, Session 4

OPC verification and hotspot management for yield enhancement through layout analysis

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As the design rule shrinks down, various techniques such as RET, DFM have been continuously developed and applied to lithography field. And we have struggled not only to obtain sufficient process window with those techniques but also to feed back hot spots to OPC process for yield improvement in mass production. OPC verification procedure which iterates its processes from OPC to wafer verification until the CD targets are met and hot spots are cleared is becoming more important to ensure robust and accurate patterning and tight hot spot management.

Generally, wafer verification results which demonstrate how well OPC corrections are made need to be fed back to OPC engineer in effective and accurate way. First of all, however, it is not possible to cover all

transistors in full-chip with some OPC monitoring points which have been used for wafer verification. Secondly, the hot spots which are extracted by OPC simulator are not always reliable enough to represent defective information for full-chip. Finally, it takes much TAT and labor to do this with CD SEM measurement. These difficulties on wafer verification would be improved by design based analysis. The optimal OPC monitoring points are created by classifying all transistors in full chip layout and Hotspot set is selected by pattern matching process using the NanoScope , which is known as a fast design based analysis tool, with a very small amount of hotspots extracted by OPC simulator in full chip layout. Then, each set is used for wafer verification using design based inspection tool, NGR2150 . In this paper, new verification methodology based on design based analysis will be introduced as an alternative method for an effective control of OPC accuracy and hot spot management.

7971-17, Session 4

A new methodology for TSV array inspection

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3D integration with TSV (Through-Si-Via) is expected to be a breakthrough technology to enhance values of semiconductor devices, along with design rule shrinkage. Currently, various technologies for TSV are being developed. However, work is still required to find solutions in metrology and inspection for TSV processes. Available methods to check TSV are shape observation by IR-microscope, cross-sectional observation with SEM, and depth measurement by white-light interference. These methods are adequate for analysis, but are not suitable for TSV shape management in production line, since they are point measurement and small area observation, and it will take a long time to cover whole TSV arrays over the wafer. It is important to check whether TSV over the entire wafer are created correctly. In addition, non-destructive and quick methods for such purpose are required.

A new methodology for inspection of TSV process wafers is developed by utilizing an optical diffraction signal from the wafer. The optical system uses telecentric illumination and has a two-dimensional sensor in order to capture the diffraction light from TSV arrays. The diffraction signal is used to modulate the displayed wafer image intensity. Furthermore, the optical configuration itself is optimized. The diffraction signal is sensitive to via-shape variations, and an abnormal via area is analyzed by the signal.

The test wafers have arrays of vias with high aspect ratio on a bare silicon wafer, and they have vias with programmed varied diameter and depth. Experimental results show that (1) the diffraction signal from TSV arrays was captured as the image with high signal to noise ratio, (2) the diffraction signal changed according to via diameter changes, and (3) the diffraction signal was also changed according to via depth changes. The signal change by 1% diameter variation was obviously good enough to be detected. Furthermore, in order to check the sensitivity for other types of shape changes, cross sections of the wafers were obtained and analyzed.

As a result, the new method is effective for the inspection of the diameter, depth and shape changes of via arrays created on the silicon wafer. It is useful for pilot wafers to optimize the process condition of exposure tools and etching tools. Also it is useful for the production wafers with via arrays. This method is applicable for the inspection of the shape of the boundary between silicon and other kind of metals, such as wafers after insulator film deposition or after copper filling. Since information from the diffraction signal from TSV arrays is captured in the two dimensional image of the wafer, the inspection time can be reduced drastically. Thus it is possible to inspect every wafer in production lines.

7971-18, Session 5

Statistical-noise effect on power spectrum of line-edge and line-width roughness with long-range correlation

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Line-edge and line-width roughness (LER and LWR) is one of the origins that cause the increasing challenge of device variability in large-scale integrations (LSIs), notably in future devices. Recent studies revealed that it also causes a dielectric breakdown between neighboring wirings. To characterize the LER/LWR, we need to estimate its correlation length x as well as variance or standard deviation. Excluding spurious LER/LWR caused by the scanning-electron-microscope (SEM) image noise is another task. We achieved these by developing an analytic formula of discrete power spectrum of LER/LWR for use in the PSD fitting. Although the PSDs calculated by this formula excellently agreed with experimental ones, the latter showed a trace of an additional component that had long-range correlation beyond the analysis limit of the aforementioned method. To extend this limit of correlation length, we have recently developed “assembly” method, which virtually assembles lines by repeatedly gathering line segments, which are arbitrarily disposed on a long line or equivalently prepared lines, and randomly changing their combination and order while permitting overlapping of the segments among the assembled lines. Then, we calculate their PSD, considering them as seamless. Additionally, we have succeeded in deriving an analytic formula of these assembled-line PSDs. Its validity was confirmed by the Monte-Carlo (MC) calculations. The assembled-line PSDs exhibit oscillatory structures in the case when x is larger than the length L of line segments. Ideally, the PSDs are obtained by averaging Fourier transforms over an infinite number of samples. However, actually, the number is finite and causes the statistical noise, an irregular variation, in the PSDs. The error of estimated LER/LWR statistics caused by the statistical noise decreases with the number NFT of assembled lines but eventually bottoms at the values determined by the number NL of line segments used to assemble the virtual lines. Naturally, these minima decrease with NL. The error of estimation by the assembly method steadily increases with x in the entire x range of this study. This error is almost independent of the number of gathered line segments in the assembled lines. By contrast, the error by the conventional method markedly increases with x beyond L/(4p), as projected in our previous report, due to missing plateaus of PSDs at small wave numbers. An experimental assembled-line PSD excellently agreed with a result calculated assuming three LWR components that were caused by short-range (1st) and long-range (2nd) correlations, and SEM image noise. x and variance used in these calculations were 35.0 nm and 6.25 nm2 in the 1st component, and 2870 nm and 0.75 nm2 in the 2nd, respectively. The variance of the image-noise component was 1.52 nm2. The experimental PSD exhibited characteristic spikes that were periodically observed as a function of wave number and found to be caused by a systematic width variation that existed in all the line segments in common. Because other previous studies also reported a trace of the long-range-correlation component, this assembly method is indispensable to analyzing most of the conventional and future LER/LWR.

7971-19, Session 5

Reduction of SEM noise and extended application to prediction of CD uniformity and its experimental validation

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For the miniaturization and successful patterning of integrated circuits (IC), a metrology of critical dimension (CD) becomes an important issue to ensure successful verification of patterning. However, as CD becomes smaller, metrology noise becomes a significant source of errors in CD metrology. Furthermore, it may pose significant contribution on

CD Uniformity. Noises in SEM metrology have been analyzed by many investigations, and several approaches were made to reduce the noise already, such as frame averaging, sum-line averaging, and other data treatments.

In this paper, a simple method to extract the noise from SEM images using frequency analysis is introduced. For smaller design node, the absolute amount of the image data to process to get CD will be limited at the same magnification. To cope with this problem, no other data averaging methods was used during analysis to get the maximum out of image. Multiple SEM images of simple Line and Space (L/S) patterns at the design rule of 4x nm were analyzed and a model of frequency profile (Power Spectrum Density (PSD) model) was made using an offline analyzing tool based on Matlab®. The PSD model is analyzed and categorized into White noise and 1/f profile (Fig 1). White noise is not a systematic rather a random noise added during SEM imaging process sequences and needs to be excluded. Noises are eliminated to generate a noise reduced PSD profile to make CD results. The contribution of white noise on CD measurement can be assessed using Line Width Roughness (LWR) measurement. Furthermore, CD uniformity can be also predicted from the modeled noise. This prediction is based on an assumption that CD uniformity is equal to LWR if the inspection area is extended to infinity and appropriate sampling method is applied.

For experimental validation of the CD uniformity measurement, image analysis using simple L/S patterns are performed. For the validation, CD uniformity is measured in two different set of measurement conditions. From the noise model made from image analysis, the results showed that the contribution of white noise on LWR can be up to around 70% (in power) without any noise reduction measures after imaging (sum line averaging) in photo resist image. CD uniformity is predicted for each measurement condition and compared with real measurement. For a result, CD uniformity prediction (3sigma) from noise model shows within 15% in accuracy with real CD uniformity value measured from the photo resist image.

7971-20, Session 5

Sensitivity of LWR and CD linearity to process conditions in active area

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LWR and CD linearity are both a major concern in the interpretation of drawn devices to actual structures on Si, and even more when translating to expected currents (both driven current and leakage current). Both of them have long ago been shown to be sensitive to process (especially lithographic) conditions, but usually not comparatively and, even more seldom are the final (etched) results thus related to the lithography process.

Following our previous work on the sensitivities of LER and LWR to layout, we set out to research whether these sensitivities are themselves sensitive to process changes which tend to affect LER and LWR. As a logical conclusion, we expected that process changes which tend to worsen roughness will increase the dependence of the roughness on layout effects - that the outcome will be addible. Measurements were done in Active Area lay

Initial results show very interesting dependence of roughness and CD linearity (dependence of measured CDs on drawn CDs) of long dense resistors. A process change that tended to make roughness worse (increased PEB, with reduced exposure to match original CD targeting), also had significant impact on the linearity, making it surprisingly more accurate at the low CD regime, but with significantly more variance.

As can be seen in Figure 1, the increase in LWR was as expected, but with an interesting “twist” on CD dependence. If we neglect the under-DR 140 nm measurement, we can see that in the standard process, there is little dependence on drawn CDs (as is known) - the 150 nm lines have slightly higher roughness, but that is all. In the high-PEB version, however, the results are more interesting, showing a considerable increase in roughness as CDs increase.

Even more intriguing is comparison of CD linearity in various structures. While, as discussed above, in the long dense resistors linearity actually improves with the increased PEB, results are different when examining isolated transistors. Here we compare results of two types of transistors - classic and U-shaped. As can be seen in Figure 2, increased PEB has harmed the CD linearity of both types of transistors, despite the fact that at CD-cell, all wafers were targeted the same for both dense and isolated features (at minimum design rules). Next stage in our study will be to complete measurement of roughness in the isolated transistors, and to compare to other structures and other process variations such as other illumination conditions and OPC models.

7971-21, Session 5

High-precision edge-roughness measurement of transistor gates using three-dimensional electron microscopy combined with marker-assisted image alignment

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The scaling-down of semiconductor devices has increased the fluctuation in the threshold voltage of the transistor gates. To discuss this problem, more detailed investigations in dopant distributions and three-dimensional (3-D) information, including edge-roughness as well as the uniformities of the materials which composed the gate structure, are considered to be important. Although scanning electron microscope (SEM) based inspection equipments are widely used today, either the height-direction dependence of the edge-roughness or the internal structure of the gate are difficult to be characterized, since they acquire only top-view SEM images to analyze the gate structures. Thus 3-D observation method based on scanning transmission electron microscope (STEM) is useful for characterizing semiconductor devices; in this method, the interior of a specimen is reconstructed from its projections obtained by STEM at various observation angles (serial images). To enhance the image quality, 3-D analysis holder and “micro-pillar” specimen have been developed, which enabled eliminating “missing wedge” during serial image acquisition [1]. Furthermore, (i) pre-alignment of micro-pillar before serial image acquisition, and (ii) marker-assisted image alignment using various gold nanoparticles formed on the micro-pillar surfaces significantly improved the 3-D image quality, and we have achieved distinguishing the separation of two particles of less than 1 nm, according to Rayleigh standard.

Using this 3-D STEM, we examined a pMOS just after gate etch processing (Sample A). Note that a thin film containing a heavy metal (replica layer) was deposited on the gate to enhance the image contrast on the gate surface, prior to specimen preparation, as shown in Fig. 1(a). After obtaining the 3-D reconstructed images, we extracted the edge-roughness. As shown in Fig. 1(b), both the line edge roughness (LER) and line width roughness (LWR) on the TiN layer were larger than those on the high-k and polisilicon layers. We then performed the 3-D measurements on a pMOS after completing the entire device process (Sample B), and extracted slice images from the 3-D reconstructed images. The image contrasts in the polisilicon and TiN layers were uniform; however, grains around 5 nm in diameter appeared in the high-k layer, as shown in Fig. 2(b). We consider that the grains appearing in high-k layer signified fluctuations in the crystalline orientation and/or irregularities in the composition, Hf and Al, of the high-k layer. Furthermore, the slice images in Sample B also revealed that the width of the high-k layer was locally reduced, which seems to significantly influence the characteristics of the semiconductor device when further scaled-down. Our 3-D

measurements successfully revealed information, such as the edge-roughness, uniformity, and local reduction, on each layer that the gate structure is composed of, which seems very important for characterizing and controlling future integrated devices, but are difficult with other conventional measurement methods, such as cross-sectional STEM and SEM.

7971-22, Session 5

Mueller-matrix ellipsometry of artificial nonperiodic line-edge roughness in presence of finite numerical aperture

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Line edge roughness (LER) represents one of the challenges of today's semiconductor technology process control. With constantly decreasing pitch the importance of LER increases as the ratio between LER and mean line width increases. Optical characterization tools have proven invaluable for fast and non-destructive inline process control and LER monitoring. Theoretical work on the sensitivity of angle-resolved data to the LER [1,2] demonstrated significance of the problem and explored limits of effective medium approximations for the purpose of LER modeling. Recent work on the artificially designed periodic roughness [3] has shown that the sensitivity of the optical methods is very good even with a finite numerical aperture (NA). Two dimensional rigorous coupled-wave analysis (RCWA) was used in order to fully explain effects of the artificial roughness on the measured Mueller matrix spectrum.

Effects of the finite numerical aperture are not negligible, and they have to be considered especially when grating pitch is decreased into sub-wavelength range, due to the "wash-out" effect it has on the measured data. The numerical aperture is now present in many modern optical characterization tools, which focus incident light into very small sub 100 μm spots. Therefore, the sensitivity of optical tools to the LER has to be re-evaluated in order to incorporate effect of NA on the measured data.

We have manufactured a line grating with artificially designed non-periodic LER and pitch of 736 nm in order to study the sensitivity of Mueller matrix ellipsometry to LER. Measured Mueller matrix data are compared with the data taken for an unperturbed line grating, which serves as the reference sample. Both measured Mueller matrix data are fitted using 1D RCWA in order to compare differences coming from model imperfections with changes in data caused by the LER. Finally, changes caused by LER are explained using 1D RCWA model, which is extended with an effective medium layer on the lines' walls. Different approaches to define effective parameters of the layer simulating LER will be discussed. All analyses are done in the framework of multiple azimuth configurations, and the azimuthal dependence of the sensitivity to LER is discussed.

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7971-23, Session 6

A CD-gap-free contour extraction technique for OPC model calibration

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Recently, the demand for high accuracy OPC model calibration is rapidly growing in the lithography field. In particular, many researchers have reported OPC model calibration techniques that use SEM contours, and suggest that using these contours possibly enables significant improvement in complex mask design. However, compared to conventional CD-based calibration, contour-based calibration results in increased errors in 1D features. In fact, our research shows that there is a gap of about 1 nm, which we call "CD-Gap," between CD measurements directly calculated from a SEM image and CD measurements calculated from SEM contours. To achieve accurate calibration, SEM contours must match the corresponding CD measurements. This large CD-gap remains a major issue due to the difficulty of extracting SEM contours from an image during the calibration process.

We have developed a CD-gap-free contour extraction technique in response to this problem. In our technique, the mask edge is classified into three different shape structures, and an optimized SEM contour extraction method is prepared for each shape structure to eliminate the CD-gap. Our contour extraction procedure is divided into three steps.

(i) Mask edge classification

Typically, the shape of the mask edge can be classified in terms of geometry, circuit function, and lithography. In our technique, we geometrically classify the mask edge into three shape structures (LINE, CORNER, and end-of-line (EOL)) for analytical simplicity.

(ii) Shape mapping

First, we find a correspondence between a mask edge and image edge. Next, we map shape structures in the classified mask edge to the corresponding image edge. However, if image quality is poor during the model calibration process, this scheme is not sufficient for estimating an accurate mapping due to increased edge roughness. We therefore improved the mapping result by using the statistical shape analysis technique.

(iii) Contour extraction

In existing techniques for SEM contour extraction, a secondary electron intensity profile is scanned along the normal direction of the image edge, and the SEM contour is extracted by analyzing the intensity profile. Due to the model calibration process, image edges are not smooth, and therefore the scan direction is unstable. To address this problem, we automatically set scan directions for each shape structure. For the LINE and EOL structures, we set scan directions by using the same CD-SEM method (i.e., along the normal direction of mask edge), while for the CORNER structure, we use the same method used with conventional techniques but only after thoroughly smoothing the image edge to improve the scan direction stability. Each technique comes with sub-nm extracting capability.

We evaluated the CD-gap with test patterns used for OPC model calibration. Experimental results show that the CD-gap was decreased to sub-nm, which clearly suggests the potential of our proposed technique to play a vital role in the lithography process.

7971-24, Session 6

Fast and accurate calibration for OPC process-window model using inverse weight algorithm

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Since the 130nm node, the key enabler for sub-wavelength lithography with cost-effective RET's has been model-based OPC. With the ever decreasing effective process-window for critical features, the same models have been called upon to verify marginal designs [1]. The process of calibrating these models is extremely tedious due to the empirical nature of the Resist and Etch (density) components of the model. Furthermore, accurate determination of process margin of complex design features poses an even bigger challenge. One widely used method to overcome these challenges has been to collect data from a large sample that include multiple measurements of the same features from different imaging tools, die and field placements and take a statistical sample of the same. Others have also created algorithms that

allow model calibration using patterned images. Nevertheless, there still remains a strong motivation not only in creating precise models, but also to minimize the data-collection and to speed the whole process.

The goal of this work was not only to improve the cycle-time for model calibration but to reduce the data volume required for fitting as well. A reduced data-set collected by inline metrology SEM using a single measuring threshold was used. In this methodology, the differential sensitivity to focus for different feature-types to a given Lithography systems is used. Input data for Process window models includes the traditional features at a range of pitch values as well as the entire Bossung curve for certain critical features. In all cases especially at far from best-focus conditions, data-error due to metrology and deteriorating resist profile increases. Curve fitting techniques have used weight assignment for the same feature at different focus conditions [2]. In this work, similar method was used to extract weights for full process data, and the weights for each feature depending on pitch were normalized to its focus sensitivity. Based on a pre-defined focus margin, a focus insensitive feature is assigned a weight of 1 while a highly focus sensitive feature assigned a proportional fraction of 1.

Based on the methodology described, regression on the same data-set was run with and without data weighting. The focus and image-depth parameters were extracted using the through focus data. Statistical fitting parameters such as Resist kernels or aerial image degradation were allowed to be extracted by regression runs over the entire data-set. Fig 1 shows the goodness of fit through focus for several features. Using the same data-set but now weight assignments as described, fitting error reduced by over 50% from +/- 6% to 0-4% (see Fig 2). With data weighting, not only drastic improvement in RMS values are seen but also accurate prediction for resist bridging. The quickness combined with precision of this technique has enabled implementation of this modeling methodology for various Digital and Analog layers.

7971-25, Session 6

Contact-edge roughness: characterization, modeling, and noise effects

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Roughness created by lithography is considered as one of the main sources of variability in device characteristics. For this reason, the issue of roughness has attracted a lot of interest during the last decade in the semiconductor industry. The main concern has been on the roughness in resist lines (the so called gate Line Edge Roughness (LER) problem) due to its effects on transistor gate performance. However, a semiconductor device contains not only gates but also interconnects, contacts and vias for the vertical and horizontal communication between the different parts of the device. These features also suffer from the presence of roughness on their surfaces. Compared to the huge amount of papers on LER, very few works have been devoted to roughness in contacts and vias [1-5].

In this work, the aim is to provide a characterization scheme, a modeling methodology and a control of the image-noise effects for the roughness in contact holes taking into account the peculiarities of their circular symmetry, which are usually overlooked in literature. To fulfill this aim, we divide our study into three parts.

In the first, we deal with the measurement and characterization of the roughness of contact holes from the analysis of top-down SEM images. In the SEM images, bright pixels denote the edges of contact holes and the deviation of these edges from a perfect circle is called Contact Edge Roughness (CER). We mainly focus on the characterization of the spatial aspects of CER. To this aim, the height-height correlation function (HHCF) and power spectrum (PS) are properly defined and calculated.. The three-parameter model (rms value, correlation length and roughness exponent) used in LER is applied to CER with emphasis on the calculation of , from the high frequency behavior in HHCF and PS. Furthermore, the role of the frequently appeared low frequency deformations of the hole shapes in HHCF and PS is discussed.

Secondly, we propose a methodology for generating computer synthesized SEM images with fractal contact edges characterized by predetermined roughness parameters. By using this model, we demonstrate that, in adjunction to what happens in lines with LER, CER can be considered as a source of CD non-uniformity among the contact holes on a wafer when the hole diameters get lower values.

Finally, the synthesized SEM images with CER are used to examine the effects of image noise and smoothing filters on CER parameters. Moreover, we explore the possibility of noise-free CER measurements by applying similar methods to those proposed for noise-free LER characterization.

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7971-27, Session 7

Hybrid CD metrology concept compatible with high-volume manufacturing

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The measurement uncertainty is becoming one of the major components that have to be controlled in order to guarantee sufficient production yield. Already at the R&D level, we have to cope up with the accurate measurements of sub-40nm dense trenches and contact holes coming from 193 immersion lithography or E-Beam lithography. Current production CD metrology techniques such as CD-SEM and OCD are limited in accuracy for various reasons (i.e electron proximity effect, outputs parameters correlation, stack influence, electron interaction with materials...). Therefore, time for R&D is increasing, process windows degrade and finally production yield can decrease. A new high volume manufacturing (HVM) CD metrology solution has to be found in order to improve the relative accuracy of production environment.

In this paper, we will present and discuss a new CD metrology concept so-called Hybrid CD metrology (HCDM) that smartly tuned 3D-AFM and CD-SEM technologies in order to add accuracy both in R&D and production. The final goal for devices manufacturers is to improve yield and save R&D and production costs through real-time feedback loop implement on CD metrology routines. We will discuss in details 3D-AFM and CD-SEM capabilities enhancements to answer future advanced roadmap requirements. We will discuss about measurement uncertainty, new 3D-AFM tip design compatible with HVM, CD-SEM threshold algorithm optimization through reference metrology feedback loop... Example of applications will be shown with typical sub-40nm trenches measurements dedicated to advanced lithography process development that will demonstrate that we have succeed to push ahead the limit of the 3D-AFM and CD-SEM technologies in measuring the tight dimensions that would allow to continue its use for current and upcoming technology nodes.

7971-28, Session 7

TSOM method for semiconductor metrology

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A relatively new "through-focus scanning optical microscopy" (TSOM- pronounced as "tee-som") method [1-5] potentially transforms conventional optical microscopes to truly 3D metrology tools for nanoscale to microscale dimensional analysis with nanometer scale resolution. The method can be used in both reflection and transmission modes of microscopes. It could be applicable to a variety of target materials ranging from transparent to opaque, and shapes ranging from simple nanoparticles to complex semiconductor memory structures, including buried structures under transparent films. Potential applications of TSOM include defect analysis, inspection and process control, critical dimension (CD) metrology, photomask metrology, overlay registration metrology, nanoparticle metrology, film thickness metrology, 3D interconnect metrology (large range depth analysis such as TSVs), line-edge roughness measurement, and nanoscale movement of parts, e.g., in MEMS/NEMS [3]. Numerous industries could benefit from the TSOM method -such as the semiconductor industry, MEMS, NEMS, biotechnology, nanomanufacturing, nanometrology, data storage, and photonics. The method is relatively simple and inexpensive, has a high throughput, provides nanoscale sensitivity for 3D measurements and could enable significant savings and yield improvements in nano/ microscale metrology and manufacturing. Potential applications are demonstrated using experiments and simulations.

TSOM is not a resolution enhancement method. However, it has a potential to provide lateral and vertical measurement resolutions of less than a nanometer using a conventional optical microscope [3-5], comparable to the dimensional measurement resolution of typical scanning electron microscopes (SEMs) and atomic force microscopes (AFMs) and is expected to extend the limits of optical metrology. The TSOM method has the ability to decouple vertical, lateral or any other dimensional changes at the nanoscale with little or no ambiguity and has the potential to analyze target dimensions ranging from a few tens of nanometers to relatively large dimensions (tens or even hundreds of micrometers in the lateral and the vertical directions, beyond the reach of typical SEM and AFM) with similar nanometer scale sensitivity. This presentation will describe the method of constructing a TSOM image along with experimental and simulated results showing nanoscale sensitivity. An experimental measurement with about a nanometer difference in the linewidth of a 45 nm wide Si line on Si substrate is shown on the left (using 546 nm illumination wavelength).

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7971-29, Session 7

Diffraction imaging of defects with the helium-ion microscope

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The Helium ion microscope (HIM) is now recognized as being the highest performance form of "scanning microscopy" that is available. The combination of sub-nanometer image resolution, and the high contrast and superior signal to noise ratio that the HIM provides make it the choice for future advanced metrology and defect review applications. One unique property of ion beam interactions with solids as compared to the corresponding electron interactions is the strong crystallographic 'channeling' contrast that is generated from the region within a few tens of nanometers of the surface of the sample. As a consequence crystallographic features such as dislocations, grain boundaries, stacking faults and point defects can be imaged at high resolution with excellent contrast from bulk solids - such as wafers - without any need to thin specimens as required for observation in a transmission electron microscope (TEM). Although electrons can also display crystallographic effects from bulk samples these are only visible when using a back-scattered detector, and they are of low visibility because the electron beam suffers inelastic scattering which de-channels the electrons and produces a high noise background.

Examples of the types of crystallographic information that are possible in the HIM image will be shown, together with details on how to maximize channeling contrast by the selection of optimum operating conditions, and on the procedures for analyzing the crystallographic data that is generated. In particular analysis of the ion channeling image could provide insights into near surface strain fields, stress induced misorientations, and in combination with other analytical imaging techniques such as ion beam induced conductivity could provide valuable insights into how the transport properties of a material are modified by surface defects.

7971-63, Poster Session

Real-time detection system of defects on a photomask by using the light scattering and interference method

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Recently, the ArF excimer laser light at the wavelength of 193 is widely used for many microelectronics facilities in the process of lithography. One of the critical problems in the lithography process is the formation of small defects on the surface. To inspect the defects it is necessary to develop the real time monitoring system. We developed the new detecting system of small defects based on the analysis of the interference fringes formed by the scattered light from defects and the reference light reflected from the surface area without defects.

The cross section of the defects is too small compared to the cross section of the reflecting area without defects. Therefore the light scattered from the small defect is very weak and the reference light reflected from the surface area without defects is relatively strong. For the good contrast of the interference fringe, the new detecting system is designed to obtain the same intensity between the scattered beam and reference beam. To make the equal intensities of reference light we reduced the beam intensity of the reference beam by optically adjusting the incidence angle near the Brewster's angle. At exact Brewster's angle no light should be reflected from the surface area without defects. By controlling the incidence angle near the Brewster's angle it is possible to reduce the intensity of the reference beam. The light source is the p-polarized 532 cw laser the second harmonic wave generated from diode pumped solid state Nd:YAG laser. Since the scattered light is weak it is desirable for the light source to have high power for the enough detectable signal on the CCD sensor. Considering that the monitoring device should be installed in the lithography equipment we used the compact 200 laser.

The laser beam with a p-polarized plane wave is incident on the photomask at near Brewster's angle. If there are any defects in the illuminated observed area, the defects will scatter the light and it is possible to obtain the interference fringe between the scattered light and the reference light. In our monitoring system a convex lens is located at the position separated focal length distance from the center of the observed area. This lens focuses the reference beam at the focal point and diverges after that. The scattered beam is collimated by the same lens. The collimated scattered beam and the diverged reference beam make interference fringes. The CCD sensor detects the interference fringes at the optimized distance. In front of the CCD sensor a polarizer is located to filter out the s- polarized light of scattered beam.

To evaluate the defect detection system, the test target is made by forming chromium dots on the quartz plate. The diameter of the chromium dots are 0.6 , 0.8 , 1.0 , 1.5 , 2.0 , 5.0 , 8.0 and 10 . For all of the dots in range 0.6 and 10 we succeeded to detect the Interference fringes between the scattered beam and the reference beam.

7971-64, Poster Session

Improved secondary electron extraction efficiency model of model-based library matching method for accurate measurement of narrow-space patterns

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The model-based library (MBL) matching method was improved to enable it to more accurately measure narrow space patterns. The MBL matching method estimates the dimensions and shape of a target pattern by comparing a measured scanning electron microscopy (SEM) image waveform with a library of simulated waveforms.

In a previous paper, we considered very small line patterns and modified the MBL matching algorithm for cases in which the left and right white bands have merged with each other. This modification introduced line-width variation into the libraries and it compensates for changes in waveforms induced by changes in line width. The effectiveness of the modified MBL method was verified by applying it to actual silicon patterns with line widths in the range 10 30 nm.

In the present paper, we consider narrow space patterns. To accurately measure narrow space patterns, we improved the secondary-electron extraction efficiency model. The extraction efficiency is a parameter that expresses the strength of the SEM extraction field, which deflects electrons away from the sample. In the conventional model, the same extraction efficiency was applied to all electrons, regardless of where they were emitted from. It is based on the assumption that the extraction field strength is uniform. However, this assumption is not valid for narrow space patterns (i.e., for widths less than 25 nm); the extraction field strength at the bottom of a narrow space pattern is generally much lower than that in open space patterns. This has prevented the conventional MBL method from accurately measuring narrow space patterns.

In our improved extraction efficiency model, the extraction efficiency is calculated as a function of the pattern shape and the emission positions of the electrons. The function is based on simulation results for the electric field strength of the SEM optics.

We applied a new model to the self-aligned double patterning (SADP) space variation sample that was fabricated by varying the exposure dose. We verified the MBL results by comparing with cross-sectional SEM images.

7971-65, Poster Session

Scatterometry simulator using GPU and evolutionary algorithm

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Scatterometry is capable of measuring the Critical dimension (CD) and profile measurements of grating structure down to approximately 16nm with high precision in semiconductor manufacturing process control. At present, the scatterometry analysis is developed for the shape measurement in two-dimensional period line division. In the papers on Microlithography in 2004-2008, we completed the 3D-FDTD (finite difference time domain) analysis of the arbitrary shapes for vertical and oblique incidence for isotropic and anisotropic mediums.

Scatterometry uses Maxwell's equations to simulate what the light signature might look like, based on input such as grating pitch, film properties, angle of incidence, CD and film thickness. The practical application is to simulate a large set of possible parameter combinations, generating a large set of spectral signatures, and when the measurements are actually taken on the wafer's grating structures, we find the simulated signature with the closest match to the measured signature. The quality of the results depends not only on the measurement setting parameters, but also on algorithms used by the analysis software. However, the scatterometry equipment is very expensive, and it cannot easily check the performance. In Microlithography 2010, we developed the scatterometry simulation software which has the spectroscopy calculation and optimization algorithm systems. Threading Building Blocks (TBB) techniques are used in the parallel computing. We calculate the spectroscopy using the rigorous coupled wave analysis (RCWA) which provides a method for calculating the diffraction of electromagnetic waves by periodic grating structures. The conjugate gradient (CG) method was used to automatically search the data which resembles the given spectrum. But, the obtained shapes sometimes did not converge on the purpose shapes. This phenomenon was caused by the optimum solution sometimes falling into another local field in the CG method.

In this paper, the analysis is continued in order to improve the performance of scatterometry simulation. In the optimization algorithm, we use the Evolutionary Algorithm (EA) referring to the evolution of the organism. The mechanism is the algorithm which obtains the idea in the evolution mechanism of reproduction, mutation, gene recombination, natural selection and survival of the fittest. Next, we speed up the parallelization using the GPU (Graphics Processor Unit). The calculation speed of GPU is 50-100 times faster than that of the CPU. We can carry out the parallel processing with many more threads up to tens of thousands than the number of streaming processor (SP) in the GPU. Here, we use the programming language CUDA (Compute Unified Device Architecture) for the NVIDIA GPU.

The Scatterometry characteristic is examined by choosing the n-th power cosine type period groove. We approximate the smoothly changing groove shape by three or four trapezoids. The optimization using EA is excellent in the global search, but it takes time for the detailed optimization to get the best value. The CG method's solution falls in the localized solution by the multi-crests. Then, we get the rough solution by EA and optimize the solution by the CG method. And finally, the results using this simulator are provided.

7971-66, Poster Session

Simulation of non-uniform thin films residual stress on overlay errors

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Thin film deposition is a critical process step in integrated circuit (IC) manufacturing. The deposition processes often result in thin films with non-uniform residual stress distributions that vary across the wafer. In the current study, the effect of non-uniform residual stress on lithography overlay error in lithography processes is investigated. Overlay errors are one of the key yield limiters at advanced technology nodes. Specifically, overlay error (misalignment) between a first level pattern on an ideal flat wafer and a second level pattern printed on the same wafer after the deposition of a residually stressed thin film process is simulated using a two step finite element model. In the first step, the deposition of a thin film with a non-uniform residual stress on a flat wafer with first level pattern is simulated and the resulting wafer shape and distortion is predicted. This process induces in-plane distortions (IPD) at the pattern surface due to both stretching and bending of the wafer. In the second step, the subsequent chucking and patterning of the wafer after thin film deposition is simulated. The chucking process results in IPD at the pattern surface due to bending of the wafer that offsets a portion of the IPD introduced during film deposition. The overlay between layers 1 and 2 can be derived from the IPDs from model 1 and model 2, and separated into correctable and non-correctable overlay error contributions. Six different cases with different residual stress distributions were analyzed: one uniform stress distribution and five non-uniform residual stress distribution cases. A sample non-uniform residual stress distribution case and the resulting overlay is shown in Figure 1. It was observed that uniform residual stress distribution in thin film results in negligible non-correctable overlay after wafer and field level corrections, whereas non-uniform residual stress distribution resulted in non-correctable overlay to the scales with the magnitude of higher order (non-uniform) residual shape change induced by thin film deposition (Fig. 2). The results provide fundamental insight into the impact of non-uniform residual stresses in thin films on lithography overlay and the need to control the thin film deposition processes in order to meet stringent overlay requirements. Furthermore, this study shows how wafer shape measurements in combination with information about the residual stress

variation in the thin film can be used to predict overlay, thus offering new opportunities for overlay management.

7971-67, Poster Session

Study of scanner stage vibration by using scatterometry

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The stage synchronization performance highly decides exposure quality, especially for ArF immersion tool due to high NA and high scan speed are used. But it is very difficult to judge scanner stage vibration effect by measuring CD impact since different factors like energy, focus, stage vibration of x and y direction all may cause CD variation. It is impossible to decouple stage vibration's impact on CD variation from other process parameters. The difficulty can be solved by a focus-energy regression model based on scatterometry CD measurement. Wafers are exposed by ArF immersion Scanner with different scan speed and measured by Scatterometry with 12X13 intra field measurement points. Measured data is regressed by using the focus-energy regression model to get the energy, focus, and fitting error. Based on the regression result, stripe pattern can be clearly seen in the fitting error map. This kind of fitting error stripe pattern becomes more obvious with increasing scan speed, and the map of fitting error in x-direction does not match with the map of fitting error in y-direction. So this kind of fitting error variation is scan dependent and highly correlated with stage vibration (MSD). Simulation study also shows the impact of stage vibration is feature type dependent. To reduce this kind of CD variation, stage vibration should be well controlled from hardware point of view. Before that can be achieved, reducing scan speed is the best containment solution.

7971-68, Poster Session

Analysis of overlay error by different aperture mixing at 2x-nm node

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As the cell size of memory device is decreasing, various resolution enhancement techniques have been developed to make smaller patterns on the wafer. One of preferred techniques to make fine patterns in microlithography is the application of customized source which is optimized to specific memory cell structure or orientation. Diverse shapes of source are used for different layers during integration of memory device. It is known that each source shape gives different effect on the lens distortion and also it causes overlay error between layers printed with different source shape. While the lithography technology node is approaching to 2Xnm regime, it is extremely tough task to control the overlay within device specification. Intra-field overlay error caused by mixing the illumination apertures can be high hurdle to surmount during the development of next generation memory devices. In this study, intra-field overlay error by combination of different apertures is analyzed and also its characteristics under specific process condition are investigated. The analytical understanding of misregistration between different layers by mixed illuminators will contribute to enhance overlay performance at 2Xnm node.

7971-69, Poster Session

New design-based metrology for fast detection of crucial lithographic defects

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Variation and uniformity of transistor length profoundly affect device performance, as the minimum transistor length becomes smaller. Several recent design based metrologies (DBMs) are commonly employed in wafer verification. Such DBMs are also utilized to obtain design for manufacturability (DFM) feedback generated through a process window qualification (PWQ) and process control. In general, the amount of output data from DBM is, however, too large to process the valuable feedback data for a given time constraint. We detected in excess of thousands of hotspots on a single chip at the edge of the process window in a PWQ case. In addition, we must consider the trade-off between DBM process time and its accuracy. Consequently, we noticed that there are frequently repeated designs related to fixing systematic defects. Thus, we realized we need to construct a fast DFM feedback flow. In this paper, we proposed a new design based metrology system to save runtime for the detection of crucial lithographic defects. To the best of our knowledge, we developed for the first time the weak point management system that is a database control environment with the repeated design related systematic defects after model-based verification. Then, the defects are again verified with DBM. Using the result of model-based verification and the weak point management system, we efficiently verify the most crucial hotspots with DBM, resulting in significant saving in processing time. The communication between DBM and the results of model based verification is improved by the proposed DBM, as much as tenfold process time reductions, compared to the conventional counterpart. There was negligible accuracy degradation for the application on sub 50 nm node DRAM. We believe that the proposed method can be used for the next DRAM generation that requires significant runtime.

7971-70, Poster Session

Advancements of diffraction-based overlay metrology for double patterning

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As the dimensions of integrated circuit continue to shrink, diffraction based overlay (DBO) technologies have been developed to address the tighter overlay control challenges. Previously data of high accuracy and high precision were reported for double patterning process using normal incidence spectroscopic reflectometry (NISR) and Mueller Matrix spectroscopic ellipsometry (MM-SE) on specially designed targets composed of 1D gratings in x and y directions[1-3]. Two analysis methods, empirical (eDBO) and modeling based (mDBO) algorithms were performed. Recent advances in modeling capability and computation power enabled mDBO, which allows measurement with reduced number of pads per target, reducing the total target size and MAM time for overlay measurements. Using MM-SE, it is feasible to extract overlay errors from only one pad per direction (x, or y) using mDBO[3].

Previously double patterning wafer made from litho-etch-litho-etch process was measured using different DBO techniques. In this work we compare DBO techniques and image based overlay (IBO) for a different process: litho-freeze-litho-etch process. In addition to the standard 1D targets, we will also explore the feasibility of measuring X and Y overlay using complex 2D targets. 2D targets comprise of patterns that are repeated in two dimensions to form gratings. One example is shown in fig. 1, which is similar to the one used in conventional imaging metrology, i.e., box in box. Pitch, CD and offset between two sets of boxes are designed to maximize diffraction efficiency and overlay sensitivity. Overlay errors in x and y directions are de-correlated by measuring diffraction signals in two orthogonal azimuth angles for MM-SE (Fig. 2) and two orthogonal polarization states for NISR (Fig. 3). One advantage of 2D target over 1D target is to further reduce silicon real state occupied by DBO targets. Secondly mDBO performance may be more superior for 2D over 1D targets due to reduced parameter space. For 2D targets the patterns in x and y directions are designed to be symmetric, so it is usually valid to couple some of the profile parameters, eg., CD, SWA, and height, in x and y directions. For 1D targets x and y gratings are printed on different pads. Typically CD, SWA are not identical for vertical and horizontal lines. Therefore it is not valid to couple these parameters,

which lead to more floating parameters than 2D target.

Each type of DBO targets is designed to optimize overlay sensitivity and de-correlate x and y directions for a specific spectroscopic technology. Data are analyzed using both eDBO and mDBO approaches. Data accuracy is checked with image-based overlay (IBO) measurements on bar-in-bar and blossom targets printed nearby. In addition, we report precision, TIS and TMU. We evaluate and optimize DBO performance from aspects of target design, hardware configuration and analysis algorithm for double patterning process.

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7971-71, Poster Session

CD-SEM image-distortion measured by view-shift method

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As device design rule shrinks, metrology by the critical dimension scanning electron microscope (CD-SEM), is not only measurement of dimension but also shape, such as 2D contour of hot spot pattern and OPC calibration pattern. The measurement accuracy of the shape metrology is dependent on image-distortion of CD-SEM. The magnification distortion in horizontal direction (x-direction) can be measured by pitch-calibration method, in which pitch of identical vertical line-and-space pattern is measured while view-shifting the identical pitch in x-direction. However, the number of measurement point cannot be sufficient because this method requires long measurement time. Not only the horizontal magnification but also vertical magnification (y-direction) and shear deformation (i.e. distortion of shape) are necessary to keep highly accurate measurement.

In this paper we introduce view-shift method for quick and accurate measurement of the image-distortion. Using this method, both local distortion of magnification and shape can be measured in horizontal and vertical directions at once. Firstly, two SEM-images of evaluation sample are taken. The sample should have a lot of unique features, for example, black silicon. View-shift about one ninth of the image size should be done between two images. They have a lot of unique features in overlap region between two images. Distribution of the unique features, dislocation between two images indicates the local image-distortion. Using this quick and accurate method, the image-distortion varying under unstable noisy-environment can be measured and corrected by automated procedures.

7971-72, Poster Session

Scatterometry for EUV lithography at the 22-nm node

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Moore's Law continues to drive improvements to lithographic resolution to increase integrated circuit transistor density, improve performance, and reduce cost. For the 22 nm node and beyond, extreme ultraviolet lithography (EUVL) is a promising technology with a larger k1 value and lower cost of ownership than other available technologies.

For small feature sizes, process control will be increasingly challenging, as small features will demand smaller measurement uncertainties. Optical scatterometry is a primary candidate metrology for EUV lithography process control. Using simulation and experiment, this work will explore scatterometry's application to a typical material set used in EUV development, which should be representative of those to be used in manufacturing EUVL. Issues considered in this study include thinner photoresists than were used in the past and different underlayer materials or film stacks which are used for EUVL pattern transfer and for EUVL lithography performance improvement.

[1] Bunday, B. et al., "Unified Advanced Critical Dimension Scanning Electron Microscope (CD-SEM) Specification for sub-65 nm Technology (2009 Version)." Publicly available at http://www.sematech.org .

7971-73, Poster Session

Study of the three-dimensional shape measurement for mask patterns using multiple detector CD-SEM

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As the designs of future node masks become smaller and more complex, the requirement of the three-dimensional (3D) shape measurement is getting tighter. Especially, the side wall angle control of mask patterns becomes important in Extreme ultra violet (EUV) lithography because of mask shadowing effect. The quality assurance of EUV mask patterns requires the pattern edge information including the side wall angle.

The Multiple Detector CD-SEM acquires the secondary electron from pattern surface at each detector. The 3D shape and height of mask patterns are generated by adding or subtracting signal profile of each detector. In signal profile of the differential image formed in difference between left and right detector signal, including concavo-convex information of mask patterns. Therefore, the 3D shape of mask patterns can be obtained by integrating differential signal profile. As the width of pattern edge is generally smaller than the primary electron beam diameter, the side wall angle cannot be measured by signal profile peak width without destructive inspection. However, in differential signal profile, the width of pattern edge appears at the signal profile peak width due to an influence of the primary electron beam diameter can be countered by opposite detector signal. Furthermore, we found that proportional relation between pattern height and shadow length on one side of pattern edge.

In this paper, we will report some evaluation results of the 3D shape, side wall angle and height measurement for various mask patterns.

7971-75, Poster Session

Electron-beam proximity effect model calibration for fabricating scatterometry calibration samples

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Scatterometry has been proven to be a tool for CD and sidewall angle (SWA) measurements with good precision and accuracy. In order to study the feasibility of scatterometry measurement of line edge roughness (LER), calibration samples with known LER have to be fabricated precisely. Electron-beam-direct-write lithography (EBDWL) can be used to fabricate the calibration samples with programmed LER structures. With the increasingly demanding requirements on lithography resolution, the corresponding programmed LER feature size becomes more and more challenging and difficult to make. EBDWL has been widely used in

nano-scale fabrication. It is well known that due to the electron scattering effects, distortion of fabricated patterns versus designed layouts can be significant. Proximity effect correction (PEC) is an enhancement methodology for EBDWL to precisely define fine resist features. The effectiveness of PEC depends on the availability of accurate electron-beam proximity effect models and effective simulation methods for electron beam lithography. In this work, two significant factors which influence the results are determined. One is the effect of beam size and the secondary electron diffusion to represent the blur of the patterning image. The other is the development threshold level to denote the undeveloped and the developed resist. An accurate proximity effect model at 50 keV accelerating voltage from Monde Carlo simulation is calibrated to actual EBDWL results.

7971-76, Poster Session

EB defect inspection of EUV-resist patterned wafer for hp 32 nm and beyond

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In EUV lithography, the potential of additional defects and particles during lithography process or mask handling is much higher because of pellicle-less mask. Also, there is the potential to print the absorber defects on wafers which are not detected by mask inspection system because EUV masks have the multi-layer substrate. Further, there is the potential of marginal defects which are caused by the mask degradation by lithography illumination to the mask.

From these backgrounds, it is important to establish the method to monitor mask defects, especially killer defects on wafers.

In this paper, the mask defectivity monitoring method that inspects the resist printed wafer is discussed. Because the defect detection sensitivity of conventional Bright Field Inspection is not enough at the hp 32 nm and beyond, the effectiveness of Electron Beam Inspection System has been studied. Despite the benefit of the higher resolution and sensitivity, Hitachi EB inspection system (I-6300E2) has the following challenges; 1) trade-off between S/N ratio of SEM image and inspection time, 2) charging effect at resist pattern, and 3) damage to the resist material. To solve these challenges, the resolution has been improved at low landing energy by optimizing column condition. Also, the new scan method has been developed to reduce the charging effect.

Using this tool, the following results have been obtained;

(1) The defect detection sensitivity is quantified using 32-nm line and space pattern with 6 nm roughness. Programmed defects of 15 nm narrowing and 10 nm widening have been successfully detected.

(2) Results from mask inspection system and EB wafer inspection system have been compared to clarify the characteristics of defects each system can detect. First, 32-nm L/S mask pattern was inspected with mask inspection system. Then the pattern was printed on to a wafer and inspected with EB wafer inspection system. Most of defects detected by mask inspection system were also detected by EB system.

(3) EUV resist damage due to EB irradiation has been evaluated. Resist shrinkage of 1.8 nm was observed with CD-SEM.

These results have demonstrated the potential of resist pattern inspection using EB system.

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7971-77, Poster Session

The study of high-sensitivity metrology method by using CD-SEM

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It is no exaggeration that modern society is dominated by the use of products containing semiconductor devices such as the computer, cell phone, automobile, and even the toaster. It is difficult to meet the demands of the semiconductor market with its ever-growing appetite for increased performance of its devices. The size of semiconductor device's critical dimensions continues to shrink following Moore's Law, fueled by the market demand for smaller, faster and more efficient devices. We are on the verge of realizing the 2Xnm (20/22/25nm) node device production in the very near future.

The earliest semiconductor device manufacturing employed optical microscopes for measurement and control of the manufacturing process. The introduction of the Critical Dimension Scanning Electron Microscope (CD-SEM) in 1984 provided a tremendous increase in capability for process monitoring and has been the standard for in-line metrology for over 25 years. The advantages of the CD-SEM are highly accurate and reproducible measurements at very specific locations throughout the device. The evolution of the CD-SEM in Metrology has included improved resolution, development of advanced measurement and pattern recognition algorithms, all required by performance improvement demands from the market.

The very stringent requirements placed on in-line Metrology for the last couple of technology nodes has produced an additional metrology methodology, beyond the CD-SEM, that involves large area measurements with very high precision for the most critical levels. We will refer to this methodology as "Macro Area Measurements".

Consequently we investigated the applicability of using a CD-SEM Macro Area Measurement methodology in this paper.

The areas investigated focused on the following five points:

1) Scanning the macro area using a large pixel number compared with the conventional method.

2) Optimization of the averaging of multiple features, Average CD (ACD)

3) Optimization of the measurement parameters.

4) Optimized sampling plans for the macro area.

5) Traditional uncertainty related to the conventional CD-SEM measurement.

In the results, we were able to validate a new methodology that we called "Macro Area Measurement" which was demonstrated to successfully detect small process variations with very high precision. This new methodology adds to the traditional advantages of the CD-SEM that include the ability to measure discrete hot spots and edge roughness.

7971-78, Poster Session

High-order dose and focus correction for improved CD uniformity

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CD uniformity (CDU) and feature profile control are key parameters in advanced photolithography for semiconductor integrated circuit (IC) manufacturing. We have developed a scheme of process control combining a CD metrology system optimized for lithography, unique modeling capability, and an exposure tool with advanced compensation capability. This paper is a continuation of work reported previously [SPIE 2010]. KLA-Tencor's Archer 300 LCM optical CD (OCD) metrology system, optimized for lithography with improved performance, is the input. KT Analyzer's CDU Package is the next step, where a model based on Neural Networks has been developed to calculate dose and focus errors simultaneous from CD parameters, such as mid-CD, SWA, and height information. The Nikon NSR-S620 and CDU Master derive control parameters for each high order dose and focus scanner compensation function. The result is the precise controllability of complex CD error distributions caused by heterogeneous processes. In this report we show experimental results of improved CDU in advanced ArF lithography.

7971-79, Poster Session

EUV defect-characterization study post litho and etch for 2x processes

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EUV mask metrology infrastructure and mask inspection strategy is yet one of the top industry gaps to be defined and resolved to enable moving EUV to pilot & production, as manifested by recent published reports & presentations(1). In accordance, there were many publications in recent years directed to defect printability studies of EUV masks. However, there were no publications yet on studies done EUV Litho & Etch wafer defect characterization using representative EUV stacks, process tools and wafer defect inspection tools.

In this work we will present a collaborative work between Applied Materials and Global Foundries which characterizes the defects from post EUV Litho and etch and the correlation between both using 80nm & 56 nm line/space pitches. The objective of the work was to study the Litho & Etch process window Vs pitch as well as learn and tune the best detection BKM'S [Best Known Methods] in Applied Materials DUV BF wafer inspection system to EUV stacks in order to detect EUV related DOI's.

In addition to the defect characterization work, we will present results of an optical detection modeling for EUV Litho stacks, which models the detection SNR [Signal to Noise Ratios] of the major defect of interest Vs various inspection system and process stack variables in order to understand Signal to Noise Ratio trends Vs these variables.

Short description of data collection:

A test mask with structure of 40nm & 28 nm L&S has been printed by an EUV stepper [ASML ADT stepper....?] on a wafer with underlying EUV litho stack [Figure 1]

This wafer was scanned by Applied Materials DUV BF wafer inspection tool, to create the defect pareto [Figure 2] post Litho. Then the wafer was etched and scanned again by the BF DUV wafer inspection tool.

The correlation between the defect at the Litho and the Etch step was studied in order to isolate those defects which formed at the Litho step Vs the added ones at etch [Figure 3]

The next step was to understand the root cause for the key defects formed at Litho Vs those formed post etch in order to improve those processes towards future production readiness. Our future plan is to re-evaluate the results after the defect reduction & elimination activities. Figure 4 shows an example of defect attributed to edge of slit issue in the scanner.

The work summary presentation will include the root cause of the various defects optimizations made to reduce them.

7971-80, Poster Session

High-order stitching overlay analysis for advanced process control

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For many years field stitching overlay methods, using interlocking metrology targets from overlapping adjacent fields, have complimented layer-to-layer overlay analysis between subsequent patterned layers for scanner qualification and on-product scenarios in integrated circuit (IC) manufacturing. Stitching overlay techniques to date typically involve only a small number of metrology targets, 1 or 2 per side, and of necessity the analysis of this data is limited to linear modeling. As IC industry advances to smaller design rules and higher density lithographic patterning smaller overlay error tolerances are required. As a result, in recent years, layer-to-layer overlay methods moved from the linear regime into non-linear high-order methods in order to meet the shrinking overlay requirements. In this study we investigate a large number of metrology structures in the overlapped scribe-line between adjacent scanner fields and the opportunity for improved overlay performance. Sampling and modeling considerations are discussed. In this investigation we consider the opportunities for high-order stitching analysis in reticle heating, run-to-run control, and scanner matching applications. The goal of this work is to establish a systematic methodology for high order stitching to characterize and reduce overlay errors for advanced IC manufacturing.

7971-81, Poster Session

Overlay process misregistration control through variance analysis and layout optimization

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To evaluate the quality of products, manufacturers and suppliers use measures. When measures are affected by error, it is relevant to assess if errors are due or not to pure random error. Especially on the most aggressive technology nodes it is important, in particular for the most demanding processes, to minimize measurement uncertainty in order to obtain optimal process control and best yeld.

This is a mandatory requirement when we consider monitoring techniques for Overlay measurement on wafers; current metrology statistical process control (SPC) focus on maintaining the performance collecting data on charts that compare fluctuation of process variable with control limits; these are calculated through well defined statistical techniques like, for example Maximum overlay error, MEP analysis and Mean plus Three Sigma evaluation.

This paper explores an alternative method in analyzing Overlay SPC monitor data through the analysis of variance based on a variance component model; its purpose is to minimize the variability due to the error of the instrument with respect to the one of the monitored process and also to improve parameters stability in presence of outliers and process issues.

In addition will be analyzed the importance of the improvement of monitoring strategy through better sampling and monitor selection.

7971-82, Poster Session

Influence of BARC filtration and materials on the reduction of spire defects

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The fabrication of semiconductor devices can be complicated by various defectivity issues with respect to fabrication process steps, their interactions, the used materials used and the tool settings. In this paper we will focus on a defect type, called spire or cone defect. This conducting defect type is very common in the shallow trench isolation (STI) process. The presence of a single defect can be responsible for a device breakdown or reliability problems, which will result in a serious impact on the competitive edge for a product qualification. Spire defects, which can only be detected after etch, are observed on all our technology nodes using 248nm or 193nm exposure techniques.

Bottom ARC (BARC) impurities are considered to be the main root cause for the formation of spire defects. Therefore we focused our efforts on chemical filtration of the BARC material and related solvents, the usage of different BARC materials and the influence of the subsequent etch steps in order to reduce or overcome the spire defect problem. In this paper we will discuss the effectiveness of different filter materials, pore sizes and different BARC materials (organic and dielectric BARC) with respect to defect analysis, lithographic performance and interaction between the dispense process and the filtration process.

7971-83, Poster Session

Novel CD-SEM magnification calibration reference of sub-50-nm pitch multi-layer grating with positional identification mark

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Because the minimum feature size of ultra-large-scale integrations is already smaller than 50 nm, a sub-50-nm pitch reference grating is required to calibrate critical dimension-scanning electron beam microscope (CD-SEM) as an advanced version of the established 100-nm pitch reference grating. We designed a reference chip with sub-50-nm pitch grating patterns oriented in the x- and y-directions and address marks for positional identification in a 15-mm square chip. First, the SiO2/Si multi-layer was deposited on the surface of the silicon substrate and the address mark was fabricated by EB lithography and dry etching processes. Next, the reference chip was fabricated by the substrate bonding, die cutting and polishing process. Finally the sub-50-nm pitch grating pattern was achieved using the material-selective chemical etching of the polished cross-sectional surface. We evaluated the sub-50-nm pitch grating reference chip using CD-SEM. The uniformity of the pitch size in the reference chip was smaller than 1 nm in 3-sigma. The positional identification marks were useful for obtaining accurate calibrations by specifying the location of the grating and the number of calibrations. Also, the pitch size was obtained absolutely by diffraction angle measurements with a high-accuracy grazing incidence small-angle x-ray scattering (GISAXS). The resultant average pitch of the grating by GISAXS was expected in very high-accuracy with standard uncertainty of less than 10 pm. This accuracy should be good enough for the calibration of the sub-50-nm pitch grating reference for CD-SEM.

7971-85, Poster Session

Expanding the applications of computational lithography and inspection (CLI) in mask inspection, metrology, review, and repair

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Mask manufacturers will be impacted by two significant technology requirements at 22nm and below: The first is more extensive use of resolution enhancement technologies (RET), such as Inverse Lithography Technology (ILT) and Source Mask Optimization (SMO); the second is EUV technology. Both will create difficulties for mask inspection, defect disposition, metrology, review, and repair. For example, aggressive OPC and Sub-Resolution Assist Features (SRAFs) on the mask are essential for accurate on-wafer imaging, and mask patterns generated by Inverse Lithography Technology (ILT) and Source Mask Optimization (SMO) may also be necessary for production. However, their use results in significantly increased mask complexity, making mask defect disposition more challenging than ever. EUV actinic inspection and AIMSTM will not be available for at least a few years, which makes EUV defect inspection and disposition more difficult. Computational Lithography and Inspection (CLI), which has broad applications in mask inspection, metrology, review, and repair by providing additional information to assist the operator in making accurate and efficient decisions on defect disposition, has become an essential technology to fill this technology gap. In one such application of CLI for mask inspection, Lithography Plane Review (LPR), the original mask patterns stored by mask inspection systems can be recovered using a patented algorithm based on the Level Set Method. More accurate lithography simulation models can be used to further evaluate the defect in simulated resist patterns. An automated defect classification based on lithographic significance and local CD changes has also been developed that enables disposition of tens of thousands of potential defects in minutes, minimizing impact on inspection throughput. Another CLI application that uses the recovered mask pattern is mask CD metrology, where the recovered mask pattern used in combination with the mask inspection image serves as the basis for a virtual CD SEM which generates a global mask CD map of thousands of locations on the real mask pattern without needing access to CD metrology tools. In the mask repair area, one application of CLI is Reference Pattern Generator (RPG), where the simulated SEM image obtained from mask design using mask process and SEM image models can be used as the reference pattern for E-beam repair tool. In AIMSTM review, CLI can be used to close the gap between aerial image intensity and wafer resist CD, automatically dispositioning defects, and can also be used to generate the reference AIMS image; in other words, the die to database capability for AIMS. This is needed for single die mask and high-MEEF patterns. In the EUV arena, CLI can be used to reconstruct EUV phase defects by using DUV inspection images captured under different conditions, followed by a fast defect printability simulation; thereby, filling the technology gap created by the lack of actinic EUV inspection and AIMS. In this paper, these CL applications are presented and discussed.

7971-86, Poster Session

Methodology for overlay mark selection

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Overlay mark design and selection are the first two steps of overlay control. Some target designs might be sensitive to lithography processes, and they could show differences in field overlay component. Certain target designs might be more sensitive to etch or CMP loading and manifest different responses to wafer linear or high order components. Some targets could be easily damaged by process and will result in higher statistical overlay noise than other design.

The same overlay mark used in 45nm process node might not be suitable for 30nm or 20nm process node due to changes in the processing of the wafer. Traditional overlay target selection mainly focuses on TMU performance which considers only precision, TIS variability, and tool-to-tool matching. In addition to TMU, metrology engineers may also consider linear residuals as an indication of target robustness. However, neither TMU nor linear residuals alone or in combination can adequately represent the full complexity involved in determining the optimal target design. Wrong selection of overlay mark for overlay control can cause issues, such as frequent faults alarms or even yield loss. As the overlay control spec becomes tighter, metrology engineers need a more sophisticated methodology that goes beyond the traditional TMU and residual metrics.

In this paper, the authors employ a source of variance methodology which decomposes and compares overlay raw data into various systematic components such as wafer, field, and un-modeled components. By comparing the SOV component differences between different overlay mark designs and by knowing process setup conditions, the metrology engineer can apply this methodology to determine the optimal overlay mark which would meet production overlay control requirements.

In summary, the authors demonstrate a new systematic methodology that will prove to be a powerful new tool for the metrology engineer to easily employ in the fab environment in order to fully characterize and determine optimal target performance and overlay control.

7971-87, Poster Session

Process solutions for reducing PR residue over nonplanar wafer

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Self-aligned source (SAS) process has been widely adopted on manufacturing NOR Flash devices. To form the SAS structure, the compromise between small CD patterning and photo resist residue has been a critical challenge as the device scaling down. In another word, the general problem of patterning SAS is the resist can not be clearly removed from underlying patterns while exposing a small space. The photo resist residue remains in between poly lines will induce etch depth variation and non-uniform resistance of source, as depicted in Figure 1. Though larger resist feature exposed on top of poly lines can reduce

the PR residue at trench bottom, it leads to poor word line profile after etching accordingly degrading the electrical properties of device.

In this study, photo simulation, resist processing, layout optimization, etch process and tri-layer materials were evaluated for SAS application of 75nm NOR flash devices. Photo simulation suggested more coherent light source enables the incident light reaching the trench bottom that facilitates the removal of photo resist, several illumination modes including Conventional, Annular and Dipole have been assessed to accompany with the optimization on layout dimension. In the resist processing trials, soft bake and post-exposure bake splits were carried out to tailor the solvent content for changing the diffusion rate during post-exposure bake as well as the resist development rate. The results demonstrated the process margin can be improved but at the cost of poor photo resist profile. The change on photo resist thickness is also helpful to improve the process latitude by energy swing but the improvement is not significant. Thermal flow was also explored for post-exposure pattern shrinkage however the material loading effect on shrinkage and profile at array edge is a roadblock for application. Tri-layer stack was finally proposed to associate with etch effort to solve the SAS non-uniformity problem. The tri-layer stack is typically comprised of a thick gap-filling organic bottom layer, silicon-containing middle layer and photo resist. The process steps for tri-layer application on SAS patterning were shown in Figure 2. The tri-layer stack approach has demonstrated excellent process latitude on SAS patterning and it is also promising to extend to even smaller technology nodes.

7971-88, Poster Session

Impact of pellicle on overlay in double-patterning lithography

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Reticle Pattern Placement Errors (PPE) has been identified as one of the key challenges of Double-Patterning Lithography (DPL) as the overlay in the circuit patterns between 2 masks is a critical parameter for successful implementation. According to the 2009 ITRS roadmap, double-patterning lithography is expected to extend 193nm immersion lithography to the 23nm node by 2016 and the corresponding PPE requirements is 1.9nm. PPE between 2 DPL mask pair affects the resulting critical dimensions of the circuit pattern and the final device performance.

In this paper, we study how the reticle PPE can be affected by the pellicle. The pellicle can induce a mechanical stress on the reticle such that after the lithography process, the actual placement of the circuit patterns on wafer will be distorted. We conducted experiments by using different combinations of pellicle frames, frame adhesives and pellicle mounting conditions on a DPL mask pair to study how reticle PPE can change with each combination. The LMS IPRO-4 mask registration metrology tool was used to measure the PPE before and after the mount/un-mount of each combination. The analysis is done using the KLA-Tencor DEVA® software to quantify how the pellicle can affect the individual reticle PPE and the relative errors between the DPL mask pair. The mechanical properties of the pellicle and glue are also used to model sag correction while reporting PPE.

7971-89, Poster Session

Contact hole measurements using YieldStar: an angle-resolved polarized scatterometer

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Metrology on 3D features like contact holes (CH) is more challenging than on lines and spaces (L/S) structures especially if one wants to have profile information. Scatterometry has been widely used on L/S structures and has enabled characterization of lithographic features providing with critical dimensions (CD) as well as feature height and side wall angle. In this paper, we will present the application of scatterometry to the measurement of 3D structures using an angle resolved polarized scatterometer: ASML YieldStar S-100. Contact hole measurements will be presented and correlation to standard metrology tools will be shown. Measurement capability will be discussed in terms of reproducibility, calculation time, sensitivity of the parameters of interest and correlation between them leading to a proper model choice. Finally initial results on on-product measurements will be presented.

7971-90, Poster Session

Microbubble size characterization for liquid chemical pressure dispense systems

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Minimization or elimination of the generation of micro-bubbles in a chemical dispense train is critical in controlling the on-wafer defects such as micro-bridging. Multiple bubble sources exist in a dispense train. In addition to bubbles entrapped in the system, gas dissolved in the liquid chemical may be released out as bubbles after the liquid experiences pressure drops in the dispense train, such as pump, filter, or orifice. Bubble traps and vented reservoirs are used in dispense trains to remove bubbles. However, these traps or reservoirs are incapable of removing gas dissolved in the chemical and ineffective in removing micro-bubbles, especially micro-bubbles that are smaller than e.g. 0.2 µm. In order to effectively control these micro-bubbles, it is critical to first characterize the size distribution of these bubbles.

This study simulates a typical dispense train in a lithography tool. As shown in the figure, Propylene Glycol Methyl Ether Acetate (PGMEA), a commonly used solvent in photoresists, is pressure dispensed from either a direct pressure or liner-based system to a vented reservoir. A pump draws the solvent from the bottom of the reservoir to flow through a filter, a macro-bubble trap, a pneumatic valve, and an orifice. A Rion KS-17A liquid particle counter that detects particles down to 0.065 µm is used to measure bubble size distribution. Prior to the test, the PGMEA used in the system is re-circulated through a 0.03 µm filter to minimize the background particle counts. The bubble size distribution is obtained by deducting the background particle counts from the readings of the liquid particle counter.

The effect of the volume of the reservoir and the relative locations of the pump and the filter on the micro-bubble size distribution is evaluated. The liquid particle counter is used at different locations in the dispense system, such as at the end of the dispense train or downstream of the reservoir, to characterize micro-bubble information at different sections of the system. The results provide insights on parameters that affect micro-bubble formation in the dispense train in a lithography tool.

7971-91, Poster Session

Small particles inspection on critical layers of 22-nm spacer self-aligned double patterning (SADP)

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SADP (Spacer Self Aligned Double Patterning) is one of the leading patterning approaches that enable a cost effective definition of line & spaces in 2X node and meeting the scaling timeline. This approach is initially targeted for memory devices, but now the focus has been shifted to logic device which moved from complex 2D structure to Gridded Design Rule, GDR [line/space @ constant pitch].

Since the SADP process is composed of the mandrel, spacer deposition, hard mask deposition and etch steps, it is essential to ensure there is no small particles contamination. Contamination control requires an extensive defect characterization work to understand the defect sources

and its impact on yield. Based on the results of this work, a yield focus inspection strategy [steps & recipe] can be developed for each module.

In this paper we will describe a systematic approach that was used to characterize small particles sources, root causes and impact on the 22nm SADP module yield. The results of this work helped to develop a yield focus defect inspection strategy.

A comprehensive study of the small particles impact on SADP defect types was performed. Wafers from SADP modules were inspected using advance DUV Dark-field inspection tool in order to find particles down to 30nm. The wafers process continued from several steps, and a BrightField inspection was performed using Applied Materials' UVision in order to find each particle possible impact on yield. Each particle that was detected at preliminary steps of the SADP process was traced and reviewed in the following process steps, in order to understand their evolution along with the SADP processing steps. The analyzed SADP module was developed by the Maydan Technology Center of Applied Materials. The inspection work was performed using a DUV laser based dark-field inspection system.

Exploring the particles induced defects propagation by tracing the defects along the SADP process, has been verified as a suitable methodology for defect source analysis. Tracing the defects evolution from the preliminary deposition step throughout the SADP module steps down to the formation of 22nm line/space can enable better capture of the critical defects at earlier process stages.

Implications of this work regarding the development of an optimized inspection strategy of the module will be discussed.

7971-92, Poster Session

The assessment of the impact of mask pattern-shape variation on the contour-based OPC-modeling by using wafer and mask CD-SEM

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As design rules shrink, Optical Proximity Correction (OPC) becomes complicated. As a result, measurement points have increased and improving the OPC model quality has become more difficult. From the viewpoint of decreasing OPC calibration runtime and improving OPC model quality concurrently, Contour-based OPC-modeling is superior to CD-based OPC-modeling, because Contour-based OPC-modeling uses shape based rich information. Hence, Contour-based OPC-modeling is imperative in the next generation lithography, as reported in SPIE2010*1.

Hitachi High-Technologies has continued to develop "Technology for improving OPC model quality by using SEM-contours". Advanced SEM contouring technology which is combined with Fine SEM Edge (FSE) technology, alignment and averaging method on 2D structures was developed. FSE makes an equal SEM edge quality for horizontal and vertical edges from a same SEM image. Alignment and averaging method eliminates rotation and XY shift error between SEM-contours and predicted contours which is induced by OPC calibration and roughness impact. In SPIE2010, Contour-based OPC-modeling by using Advanced SEM-contours on 2D structures was examined, and shown that OPC model quality was significantly improved to RMS 1.32nm.

In this study, Mask-SEM-contours were input into OPC model calibration in order to verify the impact of mask pattern shape on the quality of the OPC model. Advanced SEM contouring technology was applied to Wafer-CD-SEM and Mask-CD-SEM in examining the effectiveness of model calibration and verification with Wafer-SEM-Contours and Mask-SEM-Contours on arbitrary 2D structures. The evaluation results of the model quality will be reported. The advantage of Contour based OPC-modeling with Wafer-SEM-Contour and Mask-SEM-Contour in the next generation computational lithography will be discussed.

*1: D.Hibino et.al., "High accuracy OPC-modeling by using Advanced CD-SEM Based Contours in the next generation lithography", Proc. SPIE, vol.7638, pp. 76381X-1-11, 2010

7971-93, Poster Session

Calibration studies of pattern top resist loss detection by CD-SEM for advanced lithography process

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The decrease in the depth of focus margin by lithography tool is acknowledged to be one of the important concerns and is a key issue for a high-NA immersion lithography process. As reported by Osaki et al SPIE2008[1], it was confirmed that resist loss has a big impact to after etch line width. Accordingly, the resist loss detection technique is critical for line width control.

We have developed resist loss measuring function which is based on quantified pattern top roughness. The principle of the resist loss measurement method, detecting resist loss variation by analyzing the roughness of resist pattern top surface from CD-SEM images as Pattern Top Roughness(PTR) index, was validated by measuring resist loss and pattern top roughness from cross-sectional SEM. The PTR measurement improved Process Window determination for the evaluated different exposure condition samples. Based on the relationship between PTR index and resist loss measurement, it has good linearity to detect resist loss variation[2]. The PTR index can be applied to all resist types, and it can be easily adapted to new litho-process monitor as an index for resist loss detection. However, as for dependence of resist thickness and difference of resist, we need to investigate the sensitivity of PTR index.

In this study, we continued to evaluate those subjects. As for dependence of resist thickness and difference of resist, we investigated the sensitivity of PTR index in several resist conditions. Furthermore, the calibration methods of several resist conditions were explored by using such kind of reference metrology as cross-sectional SEM measurements of resist loss or AFM. As a result, the PTR index was aligned with Model-Based Library(MBL)[3] which is 3D measurement technique, giving pattern height index, which is one of the important information for MBL. In consequence, the advanced 3D modeling of pattern shape by top-down SEM images could be improved.

We finally discuss that the function to resist loss detection can be effectively used for practical litho-process monitoring.

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7971-94, Poster Session

Approaches to airborne molecular contamination assessment

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Airborne molecular contamination (AMC) assessment approaches can vary greatly between different fabs and even between different divisions within a given company. Some companies have very rigorous testing schedules (such as those needed to maintain tool warranties) while others only feel AMC testing is necessary when they are having a problem. While choosing to only test for AMC when a trouble arises may be cost effective in the short term it can have significant impacts

on tools, in particular tool optics, and product losses due to defects which can cost significantly more in the long term than the AMC testing would have. Another critical issue in assessing AMC is what species you should be testing for. Some volatile species may not cause an issue in your process while part-per-trillion volume (pptv) amounts of others can do serious damage to your tools and/or products. Knowledge of which volatile compounds can cause problems in your applications and at what levels is crucial in deciding what type of AMC assessment to perform and at what frequency. Typically four classes of AMC are routinely monitored in clean rooms and tool environments: acids, bases, hydrocarbons, and refractory compounds. Ideally measurement of all classes of AMC would be performed with an on-line analyzer (capable of providing almost instant results). Unfortunately the best analyzers currently available are only capable of providing 100 pptV detection for only some species while detrimental effects can be observed at concentrations below this level. Historically, sub ppbV acidic and basic AMC detection has been performed utilizing liquid impinger sampling. Impingers draw the sample gas through a solution, typically DI water, and analyze the resulting solution by Ion Chromatography (IC). An innovative solid-state trapping technology has been recently developed by SAES Pure Gas which traps acidic and basic onto a solid media which is then subsequently extracted into a small volume of solution and analyzed by IC. Solid-state trap technology has the advantage of being able to sample for much longer periods of time and at higher flow rates than the impingers. Hydrocarbon and refractory compound testing is routinely performed by collection of the compounds onto a solid-state trap with subsequent analysis by thermal desorption gas chromatography mass spectrometry (TD-GC-MS). Real world examples will be presented (an example is given below in Figure 1) using the solely solid-state trap collection methods utilized by SAES Pure Gas along with a discussion of the actions taken to reduce the AMC's present in the fab.

7971-95, Poster Session

Metrology of micro-step height structures using 3D scatterometry in 4x-nm advance DRAM

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As DRAM design rule scaling continues below 4Xnm. Step height measurement after etching process of patterning become more and more critical because it will affect post CMP process and furthermore affect yield. Scatterometry critical dimension (SCD) technology now is wildly used in metrology measurement for process control at CMOS and DRAM in the IC industry.

Nowadays, SCD 3D's technology applications in measuring at cell area or proximity structure in grating pad is getting mature. In the study, latest Multi-Azimuth angle method of SCD were used to measure step height difference after etching process of patterning and confirmed with AFM measurement successfully.

7971-96, Poster Session

A study and simulation of the impact of high-order aberrations to overlay error distribution

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With reduction of design rules, a number of corresponding new technologies, such as i-HOPC, HOWC and DBO have been proposed and applied to eliminate overlay error. When these technologies are in use, any high-order error distribution needs to be clearly distinguished in order to remove the underlying causes. Lens aberrations are normally thought to mainly impact the Matching Machine Overlay (MMO). However, when using Image-Based overlay (IBO) measurement tools, aberrations become the dominant influence on single machine overlay (SMO) and even on stage repeatability performance. In this paper, several measurements of the error distributions of the lens of SMEE SSA600/10A prototype exposure tool are presented. Models that characterize the primary influence from lens magnification, high order distortion, coma aberration and telecentricity are shown. The contribution to stage repeatability (as measured with IBO tools) from the above errors was predicted with simulator and compared to experiments. Finally, the drift of every lens distortion that impact to SMO over several days was monitored and matched with the result of measurements.

7971-97, Poster Session

Wafer-edge defect reduction for tri-layer materials in BEOL applications

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As the semiconductor feature size continues to shrink, the thickness of photo resist needs to be thinner and thinner to prevent resist features from collapse. Coupling with the need of high NA lithography for small feature patterning, both the reflectance control and the etch budget on resist thickness are becoming major challenges for lithographers. One way to simultaneously satisfy the needs of superior low reflectance, sufficient etch resistance and minimizing the resist feature collapse is to adopt tri-layer lithography scheme. The common tri-layer approach is the combination of a Si-rich anti-reflective hard-mask and a carbon-rich pattern transfer under-layer, the use of the above two layers provides a highly planar surface for thin photo resist. Furthermore, the substrate etch can be successfully fulfilled through alternating plasma etch selectivities among organic resist, inorganic Si-rich anti-reflective hard-mask and organic carbon-rich under-layer.

This work investigated the applications of tri-layer materials to back-end-of-line (BEOL) AlCu patterning. One critical problem met in this application is defect after AlCu patterning majorly from wafer edge, as can be seen in Figure 1. The defects were finally ascribed to the hump formation of Si-rich anti-reflective hard-mask by edge bead removal (EBR) process. The hump of Si-rich hard-mask yields etching masking behavior during AlCu etch accordingly leading to pattern bridging or peeling of inorganic hard-mask after AlCu patterning. To reduce the defect, several evaluations were made to suppress the hump formation including the EBR optimization for Si-rich hard-mask, baking condition of Si-rich hard-mask, different EBR layouts for PR/Si-rich hard-mask/carbon-rich under-layer and surfactant additive added Si-rich hard-mask. A synergy effect among process factors has been proposed to effectively fix the defect problem around wafer edge.

7971-98, Poster Session

Enhanced defect of interest [DOI] monitoring by utilizing sensitive inspection and ADRTrue review

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As design rule shrink, differentiation between Defect of Interest [DOI] and nuisance becomes increasingly difficult for inspection tools, hence process monitoring becomes a real challenge.(figure 1)

In this paper we describe a new approach to enhance process monitoring quality by utilizing Applied Materials SEMVision capability for automatic defect redetection (ADR).

Traditionally inspection tool recipes are optimized to keep data load in a manageable level and provide defect maps with ~10% of nuisance rate. As defect of interest get smaller with design rule, this requirement results in a painful compromise in detection sensitivity. As for SEM review, due to time and resources limitations, SEM utilized reviewing a small sample of the inspection defect map: Sample is usually 50~60 random selected defects, Review done manually in most of the times, and manual classification done for all the reviewed defects.

In the new approach (figure 2) we prefer sensitivity over nuisance rate and the inspection recipe is tuned for optimized sensitivity (i.e. detect all defect of interest with compromising on a higher nuisance rate).

The outcome of inspection with high nuisance rate is challenging requirements from SEM review methodology & tools:

A. Increase review sample- since many of the defects reported by inspection are nuisance or “false defects”, there is a need to review more defects to get meaningful data for process monitoring

B. Automatic review - As many defects are being reviewed, there is a need for automatically fast, robust and cost effective review flow, as manual review is no longer acceptable. (Will take too long and utilize both operator and SEM time)

C. false defects filtering - since defect classification done manually and many of the reviewed defects are false, the SEM tool need to be able to automatically disregard the false, leaving only real defects for manual classification.

We will present the results of a collaborative case study done by the Process Diagnostic & Control Business Unit of Applied Materials® and GLOBALFOUNDRIES® .

In order to show the added value of the new approach, we ran the new flow in parallel to the traditional flow, data was collected on 20 wafers and the 2 methods were compared in terms of sensitivity (figure 3) and the required review and classification effort (figure 4). We clearly demonstrated a significant improvement in the process monitor quality, and the ability to identify excursion of new types of defects of interest that couldn’t be identified using the traditional flow. By utilizing SEMVision automatic defect redetection algorithm as filter keeping true defects only (ADRTrueTM) the manual work required by the FAB to review and classify large sample of defects significantly reduced and make the new method production worthy.

7971-99, Poster Session

Multifeature focus exposure matrix for tool diagnosis

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Lithography tool’s performance is a major contributor to CDU. The tool’s designer or user require an accurate method to measure tool’s error factors at wafer side in order to improve CDU. Engineers typically use FEM method to find out DOF or EL, and then predict the CDU. Based on these exposure data, it is often difficult to separate the system-level physical errors, such as DOSE repeatability, focus repeatability and motion blur, because the combined impact of these errors on the CDU. In this paper, we introduce a systematic method based on exposure data to diagnose the lithographic tool information for CDU improvement. Multiple-Dimension Exposure Matrix is designed to record CD uniformity value, and in each dimension, one special physical factor can be varied based on the motion stage or illuminator’s structure and control method. In SMEE SSA600/10, the increments of DOSE repeatability focus repeatability and motion blur can be added to special dimensions during the exposure process. As a result, the CDU sensitivity can be studied in every different dimension for corresponding error factors and machine’s physical random errors can be calculated from the matrix analysis. As compared to the general FEM process, this method can capture more useful tool diagnosis information for CDU improvement. In SSA600/10, a forward control signal with different amplification and frequency can be added to motion stage and illuminator in order to prepare experimental data efficiently using only a few wafers. A set of experimental data collected on the prototype version of the exposure tool is presented, with estimations of tool’s errors based on the wafer data compared to in-situ diagnostic results.

7971-100, Poster Session

Scatterometry measurement for gate ADI and AEI critical dimension of 28-nm metal gate technology

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For reduce gate leakage and enhance device performance a lots of IC maker foundry decide entering novel metal gate technology. Mostly use node 28 nm is the good starting for the novel device. This paper discusses the scatterometry-based measurement of a gate ADI and AEI layer structure with metal gate. The WA and CD of grating are critical measurement parameters for such a structure. WA and CD of photo resist (PR) grating are gate ADI critical parameters. WA and CD of poly/metal gate films grating are the gate AEI critical parameters.

First, the paper discusses the dispersion analysis challenges and approaches for this 28 nm node structure with metal gate. Verify all of film stack is very important to build the simulation model. Metal gate film has using one film and one interfacial layer between silicon substrate is critical film stack. Metal film on the top of gate is challenge to see the CD bow on the gate AEI stage. It is very difficult to measure metal CD bow by traditional CDSEM hardware. Metal CD is key factor to electricity test for gate AEI stage and OCD model and hardware can provide the helpful information on this stage.

Second, the brand-new scatterometry KLA-Tencor SpectraShape8810 was used to measure the critical parameters. CDSEM and TEM are used as a reference metrology to assess the accuracy performance. The SpectraShape8810 extended wavelength range down into the deep UV (DUV) and enhanced ultra violet reflectivity (eUVR) can provide a noticeable improvement in measurement accuracy due to the significantly greater parameter sensitivity in this wavelength range.

The author have a lot of experience on the standard poly gate device on the node 90/65/45/40 device by using OCD tool to measure gate ADI and AEI layer. OCD tool have proven on the in-line APC control system to improve process variation compare to traditional CDSEM tool. This paper proving the SpectraShape8810 tool is working on the novel metal gate ADI and AEI layer measurement. In the future SpectraShape8810 tool will help on the research development and production ramp up process control.

In summary, SpectraShape8810 can achieve metal gate ADI PR CD and WA measurements. The ADI result will provide data to APC in-line system can reduce metal gate AEI CD variation. SpectraShape8810 can achieve metal gate AEI poly/metal gate CD and WA measurements. The AEI result will provide real time information to improve AEI CD variation and let late implantation process enhance device performance. SpectraShape8810 provides DUV wavelength and eUVR are helpful on the metal gate film stack structure.

7971-101, Poster Session

Closed-loop registration control (RegC) using PROVE as the data source for the RegC process

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At sub 4X nm nodes in memory and Sub 3X nodes in logic devices mask registration (Reg) is becoming a significant yield limiting factor. This is especially true for Double Patterning Technologies (DPT) where mask to mask overlay on the wafer is heavily influenced by mask registration error. Getting advanced mask Reg in to specification is a challenge for all mask shops as the tight Reg specs are driven by tight wafer overlay specs.

The first step in meeting the Reg spec challenge in the mask shop is to be able to measure Reg with the required specifications. With PROVETM Carl Zeiss SMS has recently introduced into the market a new registration and overlay metrology system which utilizes 193nm illumination for high resolution and a six axes controlled stage. The second step in meeting the Reg spec challenge is to actively correct for intrinsic Reg errors on the mask. For this Zeiss SMS has developed the RegC tool. The RegC tool is based on writing strain zones with the help of an ultrashort laser in the bulk of the mask. The strain zones induce deformations in the mask

which practically push the misplaced features back to their designed position.

By combining the RegC tool with data generated by PROVE it is possible to close the loop on the registration control process in the mask shop without wafer print or mask re-write. The closed loop solution works like this:

1. After completing the mask manufacturing process the mask is measured on the PROVE tool. A Pre RegC error map is prepared.

2. The Pre RegC map is loaded to a special software (SW) that calculates a Reg correction job

3. The Reg correction job is loaded to the RegC tool together with the mask and the RegC process is run

4. The mask is then measured again on PROVE which generates a Post RegC map.

5. The improvement in Reg in terms of residual Reg error in nm and % improvement is calculated and reported.

In this paper we report the results of a first demonstration of a closed loop process between PROVE and the RegC tools

Figure 1 shows the Registration Control closed loop process flow in the mask shop

7971-102, Poster Session

Surface scanning inspection system defect classification of chemical mechanical polishing induced scratches

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The methodology of Surface Scanning Inspection System (SSIS) for the Chemical Mechanical Polish (CMP) Process is to inspect the wafers on a SSIS and then subsequently perform a Defect Review SEM (DRS) review of the detected surface and subsurface anomalies. The subsequent defect review on a DRS allows for the classification of defects into discrete classification bins. The challenge of utilizing an automated DRSEM on micro and macro scratches resides in the accurate classification. When the DRSEM Field of View (FOV) is too large or too small, the defect(s) may be incorrectly classified into the incorrect defect classification bin.

The paper explores the feasibility of utilizing the Hitachi LS9100 SSIS to automatically classify CMP induced scratches as a means of bypassing subsequent Defect Review SEM Automatic Defect Classification steps as one of the key indices into the accelerated release of new slurry products from research and development into full manufacturing.

7971-103, Poster Session

RS-Mini: an enterprise class highly compact mask inspection defect management framework for the mask and wafer fab infrastructure

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We live in a world where information is ‘key’ to everything. Having access to the right information at the technicians finger tips in a fab environment, could amount to substantial insight not just into the quality of the Mask but also the nature of the process, and the steps that may be necessary to improve yield and throughout time. This article outlines details of a compact, low foot print, defect management framework for the Mask inspection tools. The system described here is ideal for Mask and Wafer fabs, to essentially bring the inspection tool terminal to the end user’s desktop, and allow the user to query and summarize year’s worth of inspection defect data with images, and establish trends and statistics in a matter of seconds.

Generally speaking, Mask inspection tools save the inspection records locally and then transfer the data to a vendor supplied server for archival. These servers are large in foot print, run customized software and hardware, and include basic software features for everyday production and engineering use. Due to the cost of such servers, typical Mask fabs may not house more than one or two such systems. In the case of a wafer fabs, the limited number of Mask inspection systems do not warrant the investment for even a single such backend server. Furthermore, these servers are generally slow, operate on a non-windows based platform, and require extensive support from the vendor for maintenance and upkeep.

The RS-Mini, described here, is capable of receiving inspection data from tens of inspection tools, and than archives the data into a high performance relational database. This data is then made available via a client software package installed on the desktop or a mobile computer of the end users. This installation is performed from a web server hosted on the RS-Mini. The client software mimics the inspection tools terminal, and it can be used, amongst other things, to review inspection results with images, overlay multiple inspection reports, archive defect repair history in the form of user entered comments, and to offline classify inspection reports. The client software can also assist the end user with defect dispositioning by rank ordering defects via smart filtering and automated image analysis. The client software allows the end user to review multiple inspections with images at the same time for side by side comparison. The system is designed to deliver robust performance even when several hundred clients are simultaneously connected to the RS-Mini. For scalability, in the case of multiple RS-Mini’s installed across an enterprise spanning a large geographic distance, as in a company with several wafer fabs, a single client can access information from all RS-Mini’s, ensuring capability to review data across organizations. In its most compact form all software and hardware needs of the RS-Mini, including redundancy to guard against failure have been packaged on a rack mountable 1U form factor server blade, measuring at less than 2 inches in thickness, thus taking up minimal space in the data center.

7971-104, Poster Session

Wavefront measurement for EUV lithography system through Hartmann sensor

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Extreme Ultraviolet lithography (EUVL) is considered as the next generation of patterning technology for the production of computer chips after the current 193 nm based optical lithography. EUVL uses photons of 13.5 nm wavelength and promises patterning of feature size of the order of 32 nm and even better.

However, when a EUV wavelength is used to carry out the imaging, the surfaces of the mirrors should exhibit unprecedented levels of perfection. In order to achieve diffraction-limited imaging, it has been proved that the root-mean square (rms) wavefront error on each mirror must be accurate to 0.25 nm. Moreover to achieve a very good image quality, it would be necessary to introduce an adaptive optics system in order to correct the aberration that a wavefront can acquire during its path through the system.

Therefore, a very important and challenging task is to develop a metrology technique that can measure the wavefront with a high accuracy.

To date, most of the wavefront characterization at this wavelength have been performed with interferometric techniques such as Phase Shift-Point Diffraction Interferometry or Lateral Shearing Interferometry, but in spite of a very high accuracy such techniques are very hard to setup, require excellent temporally and spatially coherence and have a very limited range of aberration magnitudes that can be measured with them.

On the contrary, Hartmann wavefront (HWF) sensors have important advantages over interferometry. With this technique, we can measure both phase and intensity at the same time. A HWF sensor can work with relaxed coherent requirement regarding the source. We can measure a widespread magnitude of aberration. Furthermore, this system is more compact, inexpensive and easy to setup.

In the HWF sensor, the beam under test passes through a grid that consist of an hole array and the shadow of the mask is projected onto a CCD. The wavefront is thus sampled by the hole array and the position of the individual spot centroids (xc,yc) are measured and compared with reference position (xr, yr).

The difference in distance in the both x and y direction is directly related to the partial derivatives of the wavefront across the grid.

The geometry of our first model developed with the software Matlab consists of a hole array with 44x44 holes. The holes are 80 micron size squares, spaced by 225 micron and rotated by 25 degree to minimize the overlap from the adjacent diffraction orders in the measurement plane. The distance between grid and image plane is set to 400 mm. With these parameters the field distribution on the image plane is to very good accuracy approximated by the Fraunhofer pattern.

The determination of the spot position is based on a centre of mass algorithm applied to the field in the detector plane and the aberration function is expressed in terms of Zernike Polynomials.

Our first simulation involving a mix of astigmatism and coma shows the accuracy of the algorithm in the reconstruction of the original wavefront with an average deviation of 0.7 nm

The purpose of the research is to investigate the advantages and possible constrains in the characterization of the wavefront using an Hartmann Wavefront Sensor working at 13.5 nm to be coupled in a EUV Lithography system. Further developments for improving the accuracy of the reconstruction algorithm and for searching an optimized set of parameters for a future experimental setup are currently under investigation.

7971-105, Poster Session

Bright-field optical-inspection recipe-setup supported by simulation

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The sensitivity to defects with bright-field inspection systems is dependent on their inspection parameters, including magnification, wavelength and wavelength bandwidth, illumination and collection aperture shapes, and polarization. The possible evaluation of these mode combinations is limited by the time limitations during the process development process. The optical simulation of defect images has been considered an effective way to select the best recipe for the optical inspection systems. In this paper, defect and reference structures of an interesting layer have been simulated by RCWA-based solution to Maxwell's equations and the simulation prediction has been compared with wafer inspection results. The bridging defects at the gate-etch process step for the sub-20nm node NAND flash devices have been studied by conventional defect inspection engineering and simulation-supported engineering. The RCWA optical simulation suggested the best mode for KLA Inspection system, KLA2830 and its result showed good correspondence with the signal-to-noise of the wafer-level inspection.

7971-106, Poster Session

Sensitivity analysis of line-edge roughness measured by scatterometry: simulation-based investigation toward ITRS' "manufacturable solution"

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As the semiconductor industry still follows the Moore's Law the Critical Dimensions of new generation Integrated Circuits (ICs) are getting smaller and smaller. One of the issues faced by the industry is the Line Edge Roughness/Line Width Roughness (LER/LWR) defined as variations of a given edge's/feature's position/width occurring quickly over its length. Various reports state that LER/LWR has significant impact on lithography-fabricated ICs, so it is desirable to be able to determine the LER in-line so that it never exceeds certain specified limits.

ITRS gives an indication what the LER values should be, with those indications being very tight and commented "Manufacturable solutions are NOT known". In our simulation work we deal with the challenge measuring LER on 50nm CD resist gratings using plane-mount scatterometry. We show that there is a difference between LER and no-LER scatter signatures which: first, depends on the polarization and second: is proportional to the amount of LER. Moreover - we show that the difference can be best-fit to the difference of scatter signatures from two no-LER CDs. This allows us to predict the sensitivity of "manufacturable solution" for LER measurement based on scatterometry using just two no-LER scatter signatures. As it can be shown the sensitivity is not uniform for all realizations of the same CD (e.g. for different resist heights), so not in all gratings the LER is equally easy to determine.

7971-107, Poster Session

Diffraction-based overlay analysis for spacer patterning and double patterning technology

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Overlay performance will be increasingly important for SPT (Spacer patterning technology) & DPT (Double patterning technology) as various RETs (Resolution Enhancement Technology) will be employed to extend the resolution limits of lithography. Continuous shrinkage of device dimensions makes overlay accuracy one of the most critical issues while overlay performance is completely dependent on the exposure tool.

IBO (Image-based overlay) has been used as the mainstream overlay metrology by the main memory IC companies, but IBO is not suitable for some critical layers due to large TIS (tool induced shift) values. Hence new overlay metrology is required to improve overlay measurement accuracy. DBO (Diffraction-based overlay) is regarded to be an alternative metrology to IBO for more accurate measurements and reduction of reading error. Good overlay performances of DBO have been reported in many articles however applying DBO for SPT & DPT layers poses extra challenges for target design.

In this paper, we optimize the design of DBO targets and the performance of DBO to meet the overlay specification of a sub-30nm device which is using SPT & DPT. We report the overlay performance for residuals and TIS for new DBO vernier target designs. The paper also demonstrates the effects of the vernier structure on overlay accuracy from SEM analysis.

7971-109, Poster Session

CD-SEM recipe automatic creation technology for mass production using CAD data

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In recent years, the introduction of automation technology for cost reduction has been important for large semiconductor manufacturing factories. For the cost reduction, Over Head Hoist Transportation System (OHT) focusing on processing equipments, Advanced Process Control (APC) and Yield Management System (YMS) have been introduced. On the other hand, as for measuring equipments, issues such as recipe automatic creation and recipe quality remain. These prevent trial cycle

time reduction important for the cost reduction, development cost reduction and facility retention time maximization.

As the measuring equipments, we studied issues regarding Scanning Electron Microscope (SEM). In conventional SEM recipe creation, sample preparation for image matching pattern registration and hand work on actual equipments using the sample are needed and the time needs to be included in the trial time. The increase of the number of CD-SEM recipes with complicated manufacturing process and complicated measurement pattern shape also causes the reduction of recipe quality and facility retention time. Automatic creation of quality recipes without sample preparation is needed for SEM recipe creation. For CD-SEM recipe automatic creation, we have introduced RecipeDirector that can create recipes using CAD data and measurement information. We have expanded the functions on RecipeDirector so that the measurement information of RecipeDirector is adapted to text file input for the adaption of automation system. At the same time, we have developed the system that automatically creates CAD data and text data necessary for RecipeDirector recipe creation. These have leaded to the creation of CD-SEM recipe creation system with 100 automation ratio that can reduce the time of sample preparation and hand work on actual equipments.

Accuracy improvement for image matching was an issue for introducing CD-SEM recipe creation system using RecipeDirector. There were the difference in vision between the design templates for matching created from CAD data and actual SEM images. Thus, robust pattern matching algorithm for allowing the difference needed to be developed. At the beginning of the RecipeDirector development, optical alignment and pattern matching measurement error occurred. However, addition of image processing of templates for matching and lower layer CAD pattern shape processing has leaded to the robust pattern matching.

Through the development, the perfect automatic CD-SEM recipe creation system without sample preparation and the reduction of equipment operating rate has been applied to production line. That leaded to the reduction of equipment down time for SEM recipe creation by 100 %

The trial flow time reduced by one (1) week for each device since recipes can be prepared before lot arrival. The time needed for recipe creation improved by more than 90 %. Stable and quality recipes were created since the personal difference of recipe completion rate and error occurrence were cut off through no hand work recipe creation. At the same time, the robust pattern matching improved matching success rate compared to that of conventional SEM recipes and reduced unscheduled equipment down time caused by recipe errors by more than fifty (50) %.

7971-30, Session 8

Experimental validation of 2D profile photoresist shrinkage model

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For many years, lithographic resolution has been the main obstacle in keeping the pace of transistor densification to meet Moore's Law. For the 32 nm node and beyond, new lithography techniques will be used, including immersion ArF (iArF) lithography and extreme ultraviolet lithography (EUVL). As in the past, these techniques will use new types of photoresists with the capability to print smaller feature widths and pitches. These smaller feature sizes will also require the use of thinner layers of photoresists, such as under 100 nm.

In previous papers [1,2], we focused on ArF and iArF photoresist shrinkage. We evaluated the magnitude of shrinkage for both R&D and mature resists as a function of chemical formulation, lithographic sensitivity, scanning electron microscope (SEM) beam condition, and feature size. Shrinkage results were determined by the well accepted methodology described in ISMI's CD-SEM Unified Specification [2]. In other associated works, we first developed a 1-D model for resist shrinkage for the bottom linewidth [3] and then a 2-D profile model that accounted for shrinkage of all aspects of a trapezoidal profile along a given linescan [4]. A fundamental understanding of the phenomenology of the shrinkage trends was achieved, including how the shrinkage behaves differently for different sized and shaped features. In the 1-D case, calibration of the parameters to describe the photoresist material and the electron beam was all that was required to fit the models to real shrinkage data, as long as the photoresist was thick enough that the beam could not penetrate the entire layer of resist. The later 2-D model included improvements for solving the CD shrinkage in thin photoresists, which is now of great interest for upcoming realistic lithographic processing to explore the change in resist profile with electron dose and to predict the influence of initial resist profile on shrinkage characteristics. The 2-D model also included both shrinkage due to the primary electron beam directly impacting the profile and shrinkage due to backscattered electrons from the electron beam impacting the surrounding substrate. This dose from backscattering was shown to be an important component in the resist shrinkage process, such that at lower beam energies, it dominates linewidth shrinkage. In this work, these results from the previous paper will be further explored with numerically simulated results and compared to experimental results to validate the model.

With these findings, we can demonstrate the state of readiness of these models for predicting the shrinkage characteristics for photoresist measurements and estimating the errors in calculating the original CD from the shrinkage trend.

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7971-31, Session 8

High-throughput critical dimensions uniformity (CDU) measurement of two-dimensional (2D) structures using a scanning electron microscope (SEM) system

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Background

CD-SEM and optical CD (OCD) or scatterometry CD measurement system are the two systems commonly used for CD measurement in semiconductor industry. CD-SEM has very high resolution and can measure CD on any isolated or nested printed feature. One of the main limitations of CD-SEM is low throughput. Another limitation is pattern degradation in resist films. OCD systems measure CD on a test structure, usually line-space patterns, on the scribe line of the wafer. OCD measurement is very fast with minimum damage of the wafer, especially the photoresist on the wafer. One limitation of OCD is the large measurement area required compared to a CD SEM. Another major limitation of scatterometry CD measurement is it cannot measure CD on 2D device structures. The optical proximity correction (OPC) is widely used for photolithography used to pattern structures with sub-wavelength CD. These 2D structures could have different CD variations from the line-space pattern when focus or exposure of scanner drifted. Therefore, the requirement of measuring CD on 2D structure increases as technology approaches smaller and smaller groundrules.

Abstract

In this paper, a novel methodology of CD uniformity (CDU) characterization using SEM-based measurement and inspection was tested. The system was used to take images of 2D array patterns and measure CDU values in a custom designated fashion. Because this methodology combined SEM imaging and OCD-like CD value averaging

over a large array pattern, the system can measure CDU on 2D structures with high repeatability and high accuracy.

Initial Results

Table 1 compares SEM-based 2D CDU metrology with OCD and CD-SEM. Figure 1 shows an example of 2D device structure, gate pattern of a static random access memory (SRAM) array and the parameters that need to be measured, such as gate CD, gap between gates, and tip space. Figure 2 shows the wafer maps measured by the system of interest. Figure 2a, 2b and 2c are the wafer maps of the average gap between two gates, average gate CD, and average tip space, respectively. The system measurements were obtained in significantly less time than traditional CD-SEM measurements. In addition, they were obtained intra chip and did not require special CD targets or a large OCD area. Further evaluations will quantify accuracy and repeatability of methodology and compare with traditional CD SEM metrology.

7971-32, Session 8

Verification and extension of the MBL technique for photoresist pattern shape measurement

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As pattern dimensions shrink below 32nm, the need to acquire detailed pattern profile information becomes a critical path both to process development and process control. This need necessitates metrology suppliers to explore and to extend measurement capabilities beyond simple top-down CD measurement capabilities to much more complex pattern profile metrology. While scatterometry metrology has been shown to have the capability to measure pattern profile, this capability requires measurements to be made on a periodic grating structure, thus limiting measurements to specially designed metrology targets. Important pattern shape information in the device area continues to require huge amounts of measurement correlation of a non-device structure to the patterns in the device area. The CD-SEM has the advantage of not requiring specially designed targets and therefore device structures can be measured directly, however it does not provide profile information, only top-down CD measurements.

The Model Based Library (MBL) technique has been pursued rigorously as one of the solutions for CD-SEM to achieve non-destructive profile measurements. MBL estimates the pattern shape such as sidewall angle by comparing the actual SEM signal with its various simulated-SEM-signals which are saved in the library, and calculates the CD at any height of the pattern. In previous work, the MBL was applied to various photoresist pattern shape measurement [1]. We confirmed that the results of the MBL show good correlation with the results obtained by litho-simulation, but its accuracy was not discussed.

In this work, we report on verification of the accuracy of the MBL technique and also show how the capabilities of the MBL technique can be extended. Finally, the MBL was applied to line end shape metrology to further demonstrate its capability.

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7971-33, Session 8

Surface modification of EUVL mask blanks by SEM exposure

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Mask review of pattern features and defects is normally carried out using a scanning electron microscopy (SEM) technique. Ideally, such mask reviews should be non-destructive; nonetheless, as reported in this presentation, high-dose exposures of EUVL mask surfaces have resulted in significant topographical changes, which were revealed by topographical mapping of reviewed masks using atomic force microscopy (AFM).

Exposures with 10-keV electron beams above the 100-250-kX magnification level resulted in the formation of topographical features in and around the scanned region on EUVL mask surfaces. Three different mask surfaces-a Ru-capped multilayer blank, a chromium-nitride backside, and a low thermal expansion material (LTEM) substrate--were compared after being exposed to the same exposure matrix. The current density of the electron beam, the primary experimental variable, was changed by varying the magnification. Two different exposure times and two different beam energies provided additional experimental variables.

A separate study of cleaning particle defects showed that the surface modification was not limited to changes in topography; but adhesion properties also changed. After cleaning, exposures with 10-keV electron beams above the 50-kX magnification level significantly degraded particle removal efficiency for 28 nm SiO2 particles.

This paper will define scanning electron microscopy (SEM) analysis conditions for which changes to the mask surface are negligible. Furthermore, it will characterize the topographical features on various surfaces. Finally, it will discuss the extent to which current understanding can explain the topography formation. This part of the discussion will focus on comparing the observed topographical features with modeled energy-deposition distributions resulting from the electron collision cascade within the near-surface region.

7971-34, Session 8

Optical properties of scanning electron microscope for inspection of nanodevices

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The scanning electron microscope (SEM), which enables high resolution observation at a beam acceleration below 1 kV, is used in the research and development as well as yield enhancement of integrated circuits. For example, there are the critical dimension SEM for a metrology tool, the defect review SEM for a defect classification tool, and the inspection SEM for a defect inspection tool. However, the resolution of SEM will need to be enhanced to 0.9 nm during the next five years, because the half-pitch technology node of flash memory will be reduced to 18 nm.

Figure 1 plots the optimum dependence of the depth of focus on resolution in a typical beam acceleration of 1 kV. The optimum resolution is at the most advantageous condition of the beam convergence half-angle. The depth of focus is defined by a focal depth of a 10% resolution degradation [1]. These are calculated by the density of the information-passing capacity. There is a trade-off between the improvement of the resolution and of the depth of focus, because the resolution is improved by decreasing the lens aberration, and by increasing the beam convergence half-angle. For example, at 0.9-nm resolution, the depth of focus is restricted to 8 nm. The density of the information-passing capacity depends on the condition of observation. For example, the minimum defect size in an inspection image is 18 nm, the defect is detected in 3.5 pixels, and the pixel size of the defect inspection image is 5 nm. Figure 2 plots the experimental result of measuring the dependence of the depth of focus on the beam convergence half-angle with the pixel size of 5 nm. The horizontal axis is the height of the focus from the sample surface. The vertical axis is the image resolution, which is a weighted basis mean value of the local brightness slopes of images of 280-nm holes on a Si substrate [2]. In the experimental setup the resolution in the focus condition was sufficiently smaller than the 5-nm pixel size when the beam convergence half-angle changed from 25 mrad to 10 mrad. The reduction of the beam convergence half-angle improves the depth of focus up to 1000 nm because the resolution variation does

not influence the image resolution. The depth of focus can be improved by varying the observational conditions through the influence of the density of information-passing capacity.

Furthermore, the chromatic aberration coefficient must be reduced to 0.1 mm when the resolution is 0.9 nm. With this aberration, the focal length must be below 0.2 mm, and the axial magnetic field peak must be above 1 T due to the theoretical limitations of the magnetic lens [3]. The immersion lens has an advantage of a narrow focal length of the object lens, although the narrow focal length increases the deflection aberrations. Deflection aberrations of the immersion lens are reduced by dynamically controlling two deflectors to make the electron beam pass through the center of the lens. Deflection aberrations are also thought to be reduced by the variable axis immersion lens [4].

We investigated the optical properties of an SEM with high-resolution observation at a beam acceleration below 1 kV and which was used for metrology and defect classification and inspection of integrated circuits. There was a trade-off between resolution and depth of focus, which was restricted to 15 nm with 0.9-nm resolution. We confirmed that the depth of focus could be improved up to 1000 nm by varying the observational conditions. The resolution required a focal length below 0.2 mm based on theoretical limitations. The immersion lens had an advantage of a narrow focal length. Deflection aberrations that were increased by the narrow focal length were reduced by dynamically controlling two deflectors and by using a variable-axis immersion lens. The enhanced resolution will be applied in the research and development and yield enhancement of integrated circuits.

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7971-35, Session 9

Metrology characterization of spacer double patterning by scatterometry

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Spacer defined double patterning offers an attractive solution that minimizes the dependency on dual mask overlay accuracy in the litho-etch litho-etch (LELE) double-patterning1. However, the spacer defined double patterning process sequence, for example, self-aligned double patterning (SADP) spacers (dielectric-defined core defined spacer double patterning) introduces additional challenge requiring tight CDU control, larger edge exclusion (~3nm), and higher uniformity of core film processing. As the processes consists of multiple depositions, post strips and etch steps, it is inherently susceptible to the cumulative effects of defects from each process step leading to higher rate of defect detection. The low temperature oxide deposition on resist spacer with fewer core films is used in this study thus minimizes to less number of layers for processing and metrology control steps. Although it is simpler in process, it also enhances shape variations leading to footing, top rounding and tilting during the intermediate formation steps, and thus it requires different measurement techniques to meet the metrology specifications.

While CDSEM is capable of characterizing top-down, the inability to resolve cross-sectional variability during post-litho steps as shown in Figure 2 (leading to footing and top rounding grating shapes) further emphasizes the need for alternative metrology technique. Although AFM is capable of resolving such shape variations, it is very slow and destructive technique. The scatterometry technique is rapid, precise, accurate and non contact and capable of resolving shape variations such as footing, rounding, and tilting in addition to controlling the CD and sidewall angle during the process.

Scatterometry techniques have been used to characterize the performance of scanner in terms of CD uniformity and stability and exhibited very good agreement with CD-SEM2. In our previous work, we characterized the self-aligned double patterning (SADP) structures (Figure 1a)1 using scatterometry measurements with rigorous coupled-wave analysis (RCWA) approach. In this paper, we extend our scope to direct low temperature oxide deposition on resist spacer (Figure 1b) to monitor CD uniformity (CDU), sidewall angle (slope) and resist and underlying layer thickness and shape variation during the intermediate steps across the wafer. We will also study the contribution of CD variations to overlay errors and compare the characteristics across various spacer defined double patterning processes.

The spectral response with combined Mueller spectroscopic ellipsometry (MM-SE) and reflectometry (NI-SR) showed a strong signal with increased sensitivity and improved measurement quality that help resolve the shape variations (top rounding, footing and tilting) and derive profile parameters of interest (CD, side wall angle and stack thickness) by (Figure 3). Measurements will be made on targets with three different L/S combination targets and up to 80 dies per wafer to compare the metrology (same wafer with different L/S across the wafer). The data collection and analysis will be performed on Atlas tool with NISR and MM-SE measurement techniques.

Finally, comparison of CDU variance across various spacer defined double patterning techniques by scatterometry, AFM and CD-SEM will be presented to distinguish the simplified process and metrology steps.

7971-36, Session 9

Optical far-field measurements applied to microroughness determination of periodic microelectronic structures

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In the device manufacturing industry, scatterometry type measurements are now widely used to monitor critical dimensions (CDs). Indeed, scatterometry is well recognized as the technique of choice for replacing or complementing CD-SEM monitoring in order to achieve better measurement repeatability or precision but also to provide a fast access to 2D information on the post photo-lithography or etch profiles. In addition, with the reduction in device sizing, the variability induced by local micro roughness is becoming less and less negligible in terms of statistical control of CDs. It is thus becoming mandatory to quantify this parameter to assess its impact on electrical parameters and be able react in terms of process control improvement in both photo lithography and etch areas.

Recently, a novel approach was proposed for the determination of micro roughness on periodic structures through optical far field characterization using an angle resolved scatterometry set up developed at Fresnel Institute [Ref 1 and references herein]. The light source used in our experiment is a He-Ne Laser using a wavelength of 632.8 nm. The incidence angle equals to 0° and the measurements are performed in the incident plane at a scattering angle ranging from 10° to 90°. A somehow similar approach but at a single 90° collection angle has been reported recently [Ref 2 and references herein].

The scattered intensity is the sum of the scattered intensities by a periodic structure and that of a rough surface. The exact numerical model allows treating the periodic part of the structure while the roughness is viewed as a perturbation and treated using a first order approximation. From an experimental point of view, the information on the periodic part of the structure lies in the diffraction orders, while the roughness signature is mainly found between diffraction orders. Scattering intensity is extracted and is calculated in each direction of space .Theoretical simulation performed using a computer code developed at Fresnel Institute based on differential method [Ref 3] and results derived from measurement performed with the aforementioned optical set-up demonstrated the validity of the approach. Good correlations with AFM on micro roughness values extracted from common part of power spectrums were obtained. For the sake of model and experimental validation, these preliminary experiments were performed on standards

aluminium triangular diffraction gratings with density of 600 to 1200 lines/mm and 85 nm maximum height.

Building on this promising results we have applied this methodology on actual semi conductor repetitive structures (active and gate level). These structures were designed to accommodate the relatively large spot of the optical beam. Reduction in beam spot size, which will allow measurement in conventional scribe line scatterometry monitoring structures, is underway. During this presentation we will review the theoretical approach and show roughness data derived from measurement on the aforementioned structures. Comparison with figures derived from in-line CD-SEM measurements will be shown as well.

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7971-37, Session 9

A holistic metrology approach: multi-channel scatterometry for complex applications

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Scatterometry has become the metrology of choice for fast, non-destructive measurement of linewidth and profile of printed geometries in semiconductor manufacturing. In a typical scatterometry measurement a controlled beam of light is sent to a precise target on the wafer and the reflected intensity is collected as an optical response function of wavelength. The collected optical response carries information about the target structure. To retrieve this information theoretical optical response is calculated as a function of different modifications of the target structure linewidth and profile shape and is compared to the measured optical response. The best match indicates the linewidth and profile shape of the target structure measured. The amount of profile details depends critically on the amount of optical information contained in the collected optical response. The more optical information - the more details can be modeled and measured.

There are a few traditional methods used to increase the amount of useful optical information collected from the scatterometry target:

a. Enlargement of the wavelength range. This is typically accomplished through specialized opto-mechanical components to allow UV extension of the collected light. More wavelength = more information.

b. Separate measurement of light polarized longitudinally and transversally to the line-space structures. Differently oriented polarized light couples differently to the measured structures giving rise to multiple spectral responses from the same structure. More spectral response = more information (Fig 1)

c. Different angle of incidence. The sensitivity of measuring the details of the scatterometry target profile is different for light incident at different angles. Selecting the more sensitive angular orientation = more useful information (Fig 1)

The most advanced approach to increase the amount of useful optical information is to combine in a single model all available sources of information: multiple polarizations, reference data from different toolsets, multiple angles of incidence, and even multiple targets with selected common profile parameters [1]. This is the Holistic Approach = combined modeling using all available channels of information for the optimal measurement of most profile details (Fig 2)

Here we demonstrate the benefits of the Holistic Approach for Scatterometry through combination of multiple optical channels. Results obtained through the traditional single channel, normal incidence, multi-polarization measurements are compared to results obtained through the Holistic Approach combination of multiple optical channels. The critical step of optimal selection of channels will be discussed. Technologically important complex measurement applications will be used as the demonstration vehicle (examples include 3D trench-via and HKMG applications).

7971-38, Session 9

Diffraction-based overlay reassessed

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In recent years, numerous authors 1,2 have reported the advantages of Diffraction Based Overlay (DBO) over Image Based Overlay (IBO), mainly by comparison of metrology figures of merit such as TIS and TMU. Some have even gone as far as to say that DBO is the only viable overlay metrology technique for advanced technology nodes; 22nm and beyond. Typically the only reported drawback of DBO is the size of the required targets. This severely limits its effective use, when all critical layers of a product, including double patterned layers need to be measured, and in-die overlay measurements are required 3.

In this paper we ask whether target size is the only limitation to the adoption of DBO for overlay characterization and control, or are there other metrics, which need to be considered. For example, overlay accuracy with respect to scanner baseline or on-product process overlay control? In this work, we critically re-assess the strengths and weaknesses of DBO for the applications of scanner baseline and on-product process layer overlay control. A comprehensive comparison is made to IBO. For on product process layer control we compare the performance on critical process layers; Gate, Contact and Metal. In particularly we focus on the response of the scanner to the corrections determined by each metrology technique for each process layer, as a measure of the accuracy. Our results show that to characterize an overlay metrology technique that is suitable for use in advanced technology nodes requires much more than just evaluating the conventional metrology metrics of TIS and TMU.

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7971-39, Session 9

Overlay measurement by Mueller polarimetry in the back focal plane

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Angle resolved Mueller polarimetry implemented by polarimetric imaging of the back focal plane of a high NA microscope objective has demonstrated a good potential for single layer metrology (Proc. SPIE 6518 65180X-1), possibly with targets a few µm wide. In this work we present a series of simulations which indicate that this technique may also be competitive for measurements of the overlay error delta between two gratings at different levels.

For delta = 0, the Mueller matrix elements exhibit two types of symmetries: their absolute value is invariant by matrix transposition and each element is also invariant by central symmetry about the surface normal. These symmetries break down when delta is not equal to 0. As a result, we can define the two following estimators of delta:

E1=max(abs(mij(theta,phi))-abs(mji(theta,phi)))

and

E2=max(mij(theta,phi)-mij(theta,phi+180°))

where mij are the Mueller matrix elements normalized by m11, theta and phi stand for the polar and azimuthal angles, and "max" means the maximum value of the respective quantities over the image.

The simulations were carried out for structures consisting of two superimposed gratings, respectively made of resist and c-Si and separated by a SiO2 flat layer. The resist grating was deposited on the top of the silica layer, while the c-Si grating was embedded at the bottom of the this same layer, above c-Si substrate. Both gratings featured 1 µm pitch, 500 nm CD and 200 nm thickness, and were vertically separated by 200 nm of SiO2. The overlay error was varied from 1 to 25 nm.

These simulations show that the matrix elements most sensitive to the overlay are m14 and m41. The estimators E1 and E2 were thus calculated only from these elements. Both estimators were found to vary essentially linearly with delta; with a slope of about 0.01 per nm, for delta values up to 25 nm. More precisely, E2 exhibits a true linear dependence on delta in this range, as expected for overlay values much smaller than the grating pitch, while E1 already exhibits a small curvature, probably because of the "non linearities" introduced by the absolute values.

As a result, with the considered structure the lower limit imposed by the current experimental accuracy of the instrument available at LPICM may be estimated around 1 nm. However, if we keep in mind that the considered structure is not optimized with respect to the sensitivity to the overlay, on the one hand, and that the polarimeter performance has still to be evaluated on selected elements and may be improved, on the other hand, this limit should be reduced by an order of magnitude in the near future.

A series of samples of superimposed gratings with well controlled overlay errors are currently being prepared at CEA-LETI and will be available shortly. The results of measurements on these samples will be presented.

7971-40, Session 10

Nested uncertainties and hybrid metrology to improve measurement accuracy

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There has been significant interest in new methods that combine measurement techniques to reduce uncertainties and improve measurement throughput. These methods attempt to combine measurements from different tool configurations or different platforms potentially improving throughput and measurement accuracy. Currently this approach has immediate utility when performing model-based optical critical dimension measurements. When modeling optical measurements, a library of curves is assembled through the simulation of a multi-dimensional parameter space. A least square fitting routine is then used to choose the optimum set of parameters that yields the closest experiment-to-theory agreement. This model-based approach assumes that the model is adequately describing the physical measurement conditions and that an acceptable goodness-of-fit is achieved with the best set of parameters.

Parametric correlation, measurement noise, and model inaccuracy all lead to error and measurement uncertainty in the fitting process. Although some elements of the physical model and measurement noise can in principal be addressed directly through improved hardware, better sample parameterization, and improved optical characterization and normalization procedures, fundamental limitations exist due to parametric correlations. The cross-correlations among parameters can lead to very large uncertainties even when a measurement technique demonstrates good sensitivity to a single parameter. This hybrid metrology method can directly improve measurement uncertainty introduced through parametric correlation and has further utility in selecting the correct minima among multiple nearby local minima in the fitting space.

In this presentation we will provide a strategy to decouple parametric correlation and reduce measurement uncertainties. We will develop a rigorous underlying statistical model to apply this methodology and present applications of the approach to scatterometry and scatterfield measurements. The basis for this new approach is the use of a priori information in the optical fitting process. We apply Bayesian statistical methods that rigorously use a priori information to reduce measure uncertainty. The approach can also reduce the calculation volume of the parametric simulation space as well as providing the basis for improved reference metrology.

This presentation will apply embedded metrology methods to different optical metrology tool combinations, taking account of each methods best attributes and measurement uncertainty. In this application we will explore the importance of an expanded uncertainty for each measurement or measurement method and develop the concept that a more accurate measurement can be achieved even though larger uncertainties may result. We will also directly apply the hybrid metrology approach to embedded AFM reference measurements to improve the resulting uncertainty from the library fitting process. We will present both simulation results and experimental data demonstrating this methodology.

7971-41, Session 10

Reconciling measurements in AFM reference metrology when using different probing techniques

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CD-AFM can report different CD measurements to several nanometers when different probing techniques including different probe types, scan methods or data analyses are employed on the same sample despite using self-consistent referencing techniques. This potentially weakens the assertion that this instrument is inherently accurate. It is even more important to resolve these discrepancies given the measurement challenges where multiple probing techniques need to be employed to get complete CD information. Probe type refers to different geometrical aspects of probe such as effective length, width, and edge height as well as material composition and coating. Scan code refers to CD or DT mode of tool operation. Analysis includes probe geometry deconvolution and measurement algorithms. These challenges in measurement accuracy are even more prominent for the foot or bottom CD metrology of 3D structures. This paper explores the impact of these different probing techniques on the measurement accuracy. In one series of experiments, measurements for different probing techniques are compared when the test and the referencing structures are composed of similar material and possess smooth vertical profiles. The investigation is then extended to explore the accuracy of bottom CD measurement of non vertical profiles encountered in actual process development. A hybrid method

using CD and DT modes has been tested to measure the bottom CD of challenging pitch structures. The limited space for the probe is particularly problematic for CD mode but the accuracy of DT mode for CD measurement is a concern. Other challenges will also be discussed along with possible solutions. CD-AFM has increased uncertainty when it comes to measuring within 15 nm of the bottom of a structure. In this regime details of the shape of the probe and the method by which this shape is extracted from the raw data become important. Measured CDs can vary by a few nanometers depending upon the algorithm employed for data analysis. These algorithms apply approximate methods for probe shape deconvolution from the raw data. Figure 1 highlights such difference in measured bottom CD. Given all these sources of variation in CD determination it important to understand their impact on the accuracy of measurement in order to properly estimate uncertainty and drive improvement.. Overall this paper provides a practical guideline in pursuit of accurate CD metrology and scope for improvements for upcoming technology nodes.

7971-42, Session 10

New 3-dimensional AFM for CD measurement and sidewall characterization

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As the feature size in the lithography process continuously shrinks, accurate critical dimension (CD) measurement becomes more important. Just as nano-roughness became significant with ultrathin films, the sidewall roughness becomes significant in determining the functionality of devices with extremely small features. Accordingly the sidewall increasingly influences the CD measurement and characterizing the CD of a structure becomes more critical on the nanoscale. Over the past few years, atomic force microscopy (AFM) has become a powerful tool for accurate nanometrology. However, because most operate in a top-down configuration, AFM has limited access to the sidewall; this is especially true when the sidewall angle is near or greater than 90 degrees. To overcome this obstacle, special “boot shaped” tips have been developed with sophisticated detection algorithms to image sidewalls laterally, but this method has limited resolution due to the large radius of curvature of the tip and blind spots at feature corners where the tip does not have sufficient physical access. This usually results in a rounded profile for the sharp corners at the bottom of features.

A new 3-dimensional (3D) metrology AFM has been designed on a decoupled XY and Z scanner platform for CD and sidewall characterization. In this decoupled scanner configuration, the sample XY scanner moves the sample and is independent from the Z scanner which only moves the tip. The independent Z scanner allows the tip to be intentionally tilted to easily access the sidewall (Figure 1). This technique has been used to measure both isolated and densely patterned lines. The tilted scanner design allows CD measurement at the top, middle, and bottom of lines as well as roughness measurement along the sidewall. The method builds upon the standard AFM tip design resulting in a technique that a) maintains the same resolution as traditional AFM, b) can be used with sharpened tips for increased image resolution, and c) does not suffer from corner inaccessibility from large radius of curvature tips.

A dense 165nm 1:1 line:space photoresist pattern was imaged with the 3D AFM (Figure 2). The measured feature depth was approximately 345nm. Line profiles were obtained and sidewall angles were measured at slightly over 90 degrees, showing good agreement with SEM images of the structure. The top, middle, and bottom CD’s of the lines and the sidewall roughness were measured from the high-resolution AFM data. In this paper, measurement repeatability for both isolated and dense pattern structures using the 3D AFM will be discussed

7971-43, Session 10

Rapid probe microscope for high-throughput review of semiconductor wafers

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The rapid shrinkage of the manufacturing nodes in the semiconductor industry is introducing additional and more demanding challenges to the current in-line monitoring tools. In this paper, we will present a new probe microscopy based technology, the Rapid Probe Microscope (RPM) which offers unique capabilities that addresses these challenges in alternative ways to existing review and inspection tools. The Rapid Probe Microscope produces nano-scale images with 3D information in the open-atmosphere and at the throughput required for the in-line monitoring tools in the industry. This paper will present applications of the RPM process which cater to the requirements of the semiconductor industry. Several standard semiconductor wafer layers have been used to demonstrate the capabilities of the RPM process, including nano-scale surface imaging at high throughput.

Similar to the RPM process are other conventional probe based technologies such as the AFM which has been extensively used in the semiconductor industry for nano-scale measurements. The key feature of an AFM which is similar to the RPM process is that it provides true 3D surface measurements and topographic information about the sample such as surface roughness and step heights. In addition to the advantages of a conventional AFM, the RPM process operates at a very high imaging speed. This paper will present results from the RPM process and it’s application in the semiconductor industry. Example images of the semiconductor samples which will be presented in this paper include Copper CMP Layer (Figure 1a) and layers with features at 32nm (Figure 1b) technology node and beyond. The 3D information provided by the RPM process has been used to image structures and assist in the identification of defects on these wafers.

Additionally the RPM process offers the advantage of operating in a non-vacuum environment. The use of a non-vacuum environment for the imaging of the semiconductor wafers provides several benefits such as increased throughput, reduced tool complexity, ease of integration with other platforms and the review of semiconductor materials which are incompatible with the vacuum environment. The data presented will also show that the RPM process meets the reliability requirements to be applied in the semiconductor manufacturing environment. Finally we would like to conclude that the Rapid Probe Microscope process is a new probe based technology which offers additional capabilities to address the increasingly demanding requirements of the in-line monitoring tools in the semiconductor industry.

7971-44, Session 10

Artifacts of the AFM image due to the probe controlling parameters

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Image of the atomic force microscopy is the convolution of probe shape and specimen geometry. However, probe shape for AFM imaging is not equivalent to the actual probe shape. Gap distance was controlled with the interaction between probe and specimen. Method to control the gap distance and other imaging parameters is one of the origin of image artifacts. Artifacts of the AFM image due to the controlling mechanism of the AFM were analyzed using well defined reference specimen. Two kinds of typical objects, such as single protrusion and narrow gap were used for the analysis artifacts related to the controlling mechanism in the AFM image.

The reference specimen was fabricated as an AFM probe characterizer for the analysis of effective shape of the AFM probe [1,2]. Effective probe shape, which is the probe shape for AFM imaging, is used for the analysis of image artifacts. Trajectories of the AFM probe on the sharp

ridge- and narrow trench structures were compared. Apparent width of the trench is usually observed narrower due to the infinite size of the probe, and additionally, apparent depth of the trench is also measured to be shallower than that expected from ridge structure. In the case of measuring trench depth, of which width is narrower than 100nm, it is not able to measure the trench depth due to the gap controlling mechanism of the AFM, if the probe is sharper than trench. Apparent probe shapes were compared under various vibration amplitude applied to the cantilever and set-points. Apparent aspect ratio of the probe apex changes significantly as a function of set-points.

Trajectories of the AFM probe were also compared between amplitude controlled AFM (AM-AFM) and frequency controlled AFM (FM-AFM). Dissipation is the major interaction for gap control in case of the AM-AFM, and conservative force is the major interaction in case of FM-AFM. In case that small amplitude is used for reducing degrading of the probe, effective probe shapes are strongly affected with the operating mode of the instruments. In case of the AM-AFM, apparent depth of the trench becomes deeper if the original oscillation amplitude applied to the cantilever is larger. However, apparent depth does not change significantly in case of FM-AFM, because the probe moves toward the base of the groove up to detecting upward force. Change of the apparent probe shape for trench measurement was analyzed using well-defined probe characterizer, and limitation of the trench depth measurement under specific probe and specific operating parameters was analyzed.

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7971-37, Session 11

Correcting image placement errors using registration control (RegC) technology

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The 2009 ITRS update specifies wafer overlay control as one of the major tasks for the sub 40 nm nodes. Wafer overlay is strongly dependent on mask image placement error (registration errors) in addition to CD control and defect control. The specs for registration or mask placement accuracy are twice as difficult in some of the double patterning techniques (DPT). This puts a heavy challenge on mask manufacturers (mask shops) to comply with advanced node registration specifications.

Carl Zeiss SMS has developed new a technology named RegC that enables the user (mask shop) to correct and improve image placement error of a manufactured mask. This enables the mask maker to bring an out of spec mask into the specification limits and to increase the mask manufacturing yield. In this work we will present some initial results to demonstrate the RegC technology.

Registration (Reg) test masks as well as production masks were measured on a standard registration tool and the Reg error field was calculated and plotted. A specially developed algorithm was used to compute a correction lateral strain field that would minimize the Reg error field. A laser based prototype RegC tool was used to generate a strain field which corrected for the pre measured Reg errors. Finally the post Reg error map was measured. The resulting residual Reg error field with and without scale and orthogonal was calculated.

Results: Reduction of the Reg error of 15% to 50% was achievable without significantly affecting CDU or any other mask property.

Conclusions: It was proven that a Reg correction strain field can be computed using a special algorithm and that a laser based correction method can be used to effectively reduce the Reg error in the mask by using this method without significantly affecting any other mask property.

7971-45, Session 11

In-line dose and focus monitoring and control for 32-28 nm processing

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In this paper we demonstrate that the combination of SCD metrology on the advanced Archer 300LCM tool and modeling methodology based on KT Analyzer's neural network modeling allows accurate focus and dose in-line monitoring and control of full production stacks such as gate stack or metal stack. In order to allow dense intrafield sampling for intrafield focus and dose monitoring and control, we designed a test reticle with suitable SCD targets. For every stack, optimized FEM wafers were exposed. Then isolated and dense targets were selected with CDs to optimize focus sensitivity for measurements on Archer 300LCM. A set of test wafers with nominal F/E conditions and induced F/E variations across a wafer and across a field was created and measured. In the next step we fitted two alternative FEM models: standard polynomial and neural networks. We demonstrated that NN based models perform more accurate rather than polynomial models. In the experiment we performed focus and dose correction on an additional set of wafers and demonstrated significant focus improvement on the corrected wafers. In a separate experiment we showed, that focus corrections obtained on test wafers also improved focus performance on product wafers.

7971-46, Session 11

High-sensitive and fast scanner focus monitoring method using forbidden pitch pattern

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Focus control is one of the critical parameter on lithographic tool performance controls, and the capability of focus control is directly related to lithographic process window. Therefore, many focus monitoring methods including traditional manual SEM image based method were developed to monitor the best focus position of the scanner system. However, other focus monitoring methods use special pattern which shows sensitive changes along focus changes. To print desired pattern, either complicated reticle design or sophisticated sensor systems are required. Also all the methods are discrete measurement within a field and wafer. Hence measuring focus change on the large area or high spatial resolution is required to measure very large number of point. In this paper, we suggest the newly developed focus monitoring method to overcome the above shortfalls. The forbidden pitch where the smallest DOF is obtained under dipole illumination is applied to monitoring a focus. This forbidden pitch pattern shows a rapid change on pattern shape and CD as the focus of scanner system is moving toward out of focus range. This pattern change creates color differences under the optical microscope, because the change of the patterning size results in reflectivity changes. Therefore, a focus change of a scanner system can be detected by the color change under the normal bright field defect inspection image, even though the resolution of microscope is low. Commercial macro inspection system was used to detect the focus behavior and showed good correlation with traditional machine focus monitoring methods. The benefits and sensitivity of current methodology will be discussed in details.

7971-47, Session 12

Overlay improvement roadmap: strategies for scanner control and product disposition for 5-nm overlay

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No abstract available

7971-48, Session 12

Improved overlay methodologies to meet 45 nm and beyond technology node challenges

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As the overlay tolerance continue to shrink to meet advanced technology node requirement, various overlay improvement techniques flourish over recent year to address for wafer grid and field grid distortion, in addition to the introduction of more sophisticated exposure tool from scanner vendors. In order to enlarge the overall overlay process window, it is time to adopt a more detailed methodology which consist of unmodeled residuals decomposition, in-die overlay characterization, higher order process correction and overlay sampling optimization. In this paper, we manage to demonstrate the importance of these overlay components using intentionally designed experiment under scanner mix and match condition. The final proposed overlay BKM is applied on 45nm production wafers at the most critical Gate and Contact level to prove the actual improvement under integration process influences.

7971-49, Session 12

Accuracy of scatterometry overlay and image-based overlay

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There is no overlay standard in the world. For critical dimension (CD), we may use the VLSI standard or programmed pitch offsets to determine the CD accuracy or CD sensitivity. Programmed overlay offsets can provide relatively accurate sub-nanometer level overlay splits but it is only on a single layer and does not contain layer-to-layer process variations. The splits of scanner expansion can check the trend of overlay sensitivity but it cannot provide the exact value of overlay offsets. Transmission electron microscopes (TEM) can be used as a final overly error verification tool. However, TEM sample preparation for after-development-image (ADI) will introduce even more sample distortion errors. Therefore, unlike CD metrology, there is no clean and systematic way to verify the accuracy of overlay metrology. These technical barriers necessitate matching scatterometric overlay and image-based overlay, especially for sub-nanometer point-to-point matching requirement.

In this paper, we compared the correlation of after-etch-image (AEI) to ADI by using scatterometric overlay measurement and image-based box-in-box overlay measurement on the same wafer. Data were taken in the x and y directions. The AEI-to-ADI overlay data consistency plays a key role for photo APC success and AEI overlay should be treated as the final standard for overlay accuracy. The AEI-to-ADI overlay correlation (R-squared) is adopted as the index of overlay accuracy.

Our experimental results show that R-squared of image-based box-in-box overlay is about 0.75 but that of scatterometry overlay is larger than 0.99 as shown in Figure 1. Furthermore, the slope of scatterometry overlay is much closer to unity than image-based box-in-box overlay. These results make us believe that scatterometry overlay is much more suitable for APC in advanced lithography control. Otherwise, image-based box-in-box imaging or target design must be optimized more.

7971-50, Session 12

Investigation on accuracy of process overlay measurement

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Recently, the introduction of double patterning expedited the shrinkage of design rule, and necessitated corresponding tighter overlay control. The overlay control is mainly composed of scanner overlay performance, overlay key design and metrology. All the contributors are doing their best to extend their technology to future generation, delivering new scanner, new metrology tool, and new mark. However, in advanced applications, these extensions may not be able to meet the control requirement, consequently, additional breakthroughs are required. Overlay metrology accuracy has been considered that it is dependent on stack complexity and key deformation. We have paid attention to key and process optimization, on the assumption that low residual number means more accurate measurement. However, cost and technology limit makes it impossible to meet well-optimized process every time. When well-optimized process is not used, both real misalignment and measurement inaccuracy would be considerable. In this study, we investigated a method to enhance the overlay control, approaches by extraction of real misalignment out of overlay measurement. So far, only the destructive inspections like vertical SEM have enabled us to measure real misalignment. However, we are not able to apply this destructive method to monitoring and overlay control for real products. Instead, a concept of non-destructive method is proposed in this paper, extracting vertical information from the results of multiple measurements with various measurement conditions, keys or recipes. The wafer with simple key structure, for example resist patterned wafer, it can be assumed that the measurements represent real misalignment and insensitive to recipes. However, as stack becomes more complex, the overlay results become sensitive to measurement condition, and we should select single best recipe and key combination. Instead of using single condition, we measured various conditions and extracted additional information from the results of unselected conditions. We compared the results of various recipes and various process stack wafers, and ADI and ACI results were investigated also. With this proposed method, the measurement accuracy can be improved and we can enable a new knob for overlay control.

7971-51, Session 12

Improved overlay control using robust flyer-removal for backend layers

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Overlay control is one of the most critical areas in advanced processing of semiconductor integrated circuit (IC) manufacturing. Maintaining optimal product disposition and control requires high quality data as an input. For this purpose state-of-the-art overlay metrology systems have been developed, as well as advanced overlay target designs and sophisticated analysis techniques. In extreme cases, such as aluminum backend layers with grainy background, fliers (or outliers) can contaminate lot statistics that can negatively impact lot disposition decisions and feedback control to scanners. Advanced flier removal methods have been developed to minimize the impact of fliers on overlay data processing, which are generally based on (1) target quality metrics provided by the sophisticated algorithms of the metrology tool, (2) raw data statistical methods removing data which fall far from the data mean or median, and/or (3) residual data statistics based on overlay modeling. Methods based on residual data statistics can be very useful, however, typical overlay modeling is based on least square regression whereby outliers have a quadratic impact on the model which is being used to detect and remove them. In this paper we discuss the pros and cons

of several statistical flyer removal methods, including the use of robust regression methods in order to more accurately eliminate flyers.

7971-52, Session 12

Wafer-quality analysis of various scribe line-mark designs

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Scribe Line Mark (SLM) printed on substrate is a standard method used by modern scanners for wafer alignment. A diffraction pattern will be formed from the light that is reflected from the SLM, and the scanner detects the desired diffraction order to determine the exact position of the wafer. The signal strength of the diffraction order needs to reach a certain threshold for the scanner to detect it. During wafer processing, marks go through various processes such as chemical mechanical polishing (CMP) and etching and are buried underneath complex film stacks. These processes and film stacks can severely reduce wafer quality (WQ). In order to avoid process damage, many different marks are recommended by equipment manufacturers, but most of these variations have reduced WQ. Theoretical analysis of how different designs affect WQ will be performed in this paper. The challenge of self-aligned double patterning (SADP) SLMs will also be addressed. The analysis is verified by experimental results using various structures.

7971-53, Session 13

Application of small angle x-ray scattering to characterize cross sections of nanoscale line gratings on silicon wafers: comparison of grazing incident measurements with transmission measurements

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The ever-decreasing dimensions of individual circuitry components will soon reach 22 nm where the acceptable tolerance in the variation of the linewidth or feature roughness will be less than 1 nm. This creates significant challenges for measurements based on electron microscopy and optical scatterometry. Device viability also requires the measurement be non-destructive. In addition, the continuing development of new materials for extreme ultraviolet photoresists, nanoporous low-k dielectrics, and metallic interconnects requires high precision dimensional measurements for process development and optimization.

Small angle X-ray scattering (SAXS) is a new metrology platform that is capable of measuring the average cross section of nanoscale surface patterns ranging from 10 to 500 nm in pitch with sub-nm precision [1]. These capabilities are obtained by measuring and modeling the scattering intensities of a collimated X-ray beam with a sub-nanometer wavelength from a periodic pattern, such as line/space gratings and arrays of vias and posts. In this work, we evaluate and compare the capability of both a laboratory-based and a synchrotron-based SAXS measurement for critical dimension characterization. To compensate for the relatively low X-ray intensity of the laboratory-based instrument, all lab-based measurements were conducted in grazing incident geometry [2] such that the sampling area is at least a few orders of magnitude greater than that of a transmission SAXS measurement using a synchrotron source. The test samples were line gratings with sub-50 nm linewidths made of poly, embedded SiO2 and other materials. Identical samples were used for both grazing incident and transmission measurements, and the experimental results were analyzed with a cross-section model consisting of linewidth, height, sidewall angle, top corner radius, and bottom corner radius. Results from line gratings made of multiple layer material stacks will also be discussed.

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7971-54, Session 13

Critical dimension measurement of line gratings using specular x-ray reflectivity: the coherence length effect

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Specular x-ray reflectivity (SXR) is a powerful technique to investigate surfaces and interfaces including their roughness, diffusion across buried layers and thickness of single and multilayer stack by depth profiling the electron density in the direction normal to the surface of a flat sample with a sub-nanometer resolution. We have further extended the application of SXR to quantify the cross section of nanoscale line and space patterns. The efficacy of the SXR is based on the use of an effective medium approximation (EMA); when the coherence length of the x-ray is larger than the lateral dimensions of the line gratings the density of the lines and spaces (for a grating structure) are averaged laterally as an “effective” density, thus the EMA. For periodic patterns such as the gratings studied here, this effective density contains quantitative information about the line-to-space ratio as a function of its depth. This notion of EMA has also been used successfully in determining the effective refractive index of porous material for optical ellipsometry or scatterometry where the wavelength is far greater than the length scale of the heterogeneities. This condition is far from being obvious for SXR since the wavelength is near 0.1 nm, a value far smaller than the lateral dimension of the line gratings.

In this work we experimentally determined the coherence length of the X-ray reflectometer, hence, to explore the limitations of the SXR technique by measuring line-gratings with periodicities ranging from 300 nm to 16 um at various azimuthal angles between the incident x-ray and the lines. A clear break down of EMA was noticed at certain x-ray incident angle depending on the sample azimuthal angle; this information provided a useful pathway for determining the coherent length of the x-ray reflectometer precisely. It also set the guideline for the proper use of SXR to measure critical dimension in nano-structured surface patterns.

7971-55, Session 13

EUV-resist metrology with the scanning helium ion microscope (HIM): benefits and limitations

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HIM

Recently, Zeiss has introduced its scanning Helium Ion Microscope (HIM), a sensitive surface inspection apparatus with sub-nanometer resolving power[1]. This paper presents the assessment of critical dimensions of patterns that are written with the latest generation ASML optical and EUV lithography apparatus using both the HIM [2] and the industry-standard CD-SEM.

Critical Dimension (CD) metrology methods

Shrinking the CD puts more stringent demands on the metrology tools that qualify the lithography results of the latest scanners. CD metrology can be performed using optical tools (OCD), deploying scatterometry on a CD marker. A more direct image of the CD is obtained through

using scanning microscopy tools like SEM, AFM and, recently Helium Ion Microscopy. These technologies scan an nm-sized probe over the sample to image the surface structure and shape. Ultimately, the interaction mechanism of the probe with the sample limits the achievable resolution and quality of the images. This contribution addresses the benefits and limitations of HIM as a new technology for CD-metrology, especially addressing the requirements of future CD nodes.

CD-SEM and CD-HIM

At present, Critical Dimension Scanning Electron Microscopy (CD-SEM) is an essential part of the current Critical Dimension (CD) metrology tooling: It is needed for flexible image making, to get a first image on a new scanner type and to troubleshoot wafers. Benefit of CD-SEM is that all kind of targets can be measured, at the expense of throughput when compared to OCD. The resolution of CD-SEM images is blurred by several nanometers due to the interaction of the electron beam with the resist. The interaction of the helium ions with the resist is intrinsically different, thus allowing the imaging of the sample surface with a higher accuracy and lower Total Measurement Uncertainty (TMU). Fig.1 shows a benchmarked between CD-SEM (left) and CD-HIM (right) imaging for the challenging application of qualifying ASML's NXE:3100 on EUV resist. The larger line width observed in the SEM image may be due to the longer mean-free path of the generated Secondary Electrons. The larger line width roughness is partly attributed to a higher EMC and acoustic noise level in the SEM.

SEM
HIM

Fig. 1 EUV resist with 27 nm dense lines (pitch 1:1) imaged with SEM (left) and HIM (right). The thinner white edge of the lines in the HIM image indicates a better resolution. The lines in the HIM image look smoother and thinner. The cause of these effects is still under investigation.

In conclusion, CD-HIM has several (potential) benefits over CD-SEM: a different interaction mechanism enables higher resolution imaging and a reduced interaction volume yields less systematic errors in CD measurements. The improved topology measurements will lead to lower TMU if the modification of the CD during HIM imaging (due to swelling or shrinking of the resist and/or wafer [3]) is kept sufficiently small.

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7971-56, Session 13

Through-silicon via etch depth metrology for 3D integration

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Through-silicon vias (TSVs) will dominate 3D integration and present particularly challenging metrology when their high aspect ratio (HAR) geometries exceed 10:1. As via diameters for high density TSVs shrink to as small as 0.8 micron, according to the 2009 International Technology Roadmap for Semiconductors (Table 1), optical metrology techniques using visible wavelengths will become complicated by a diminishing return of etch depth information from those HAR features. Traditionally, these features are measured by cross-section scanning electron microscope analysis, a destructive technique.

Using infrared optics and illuminating the wafer from the back-side will eliminate the high aspect ratio effect resulting from illuminating the wafer's top side to measure etched TSVs. Reflections off the bottom of TSVs are compared to the reflections from the wafer's surface, and TSV etch depth is calculated using an interferometric technique. Etch depth measurements can be completed on etched vias or on etched and copper-filled vias.

This paper reviews an in-line metrology tool featuring backside infrared illumination and interferometry for non-destructive TSV etch depth metrology enabled by backside infrared illumination. As a non-destructive technique, backside infrared illumination lends itself to being developed as a high volume, in-line TSV metrology tool to support 3D integration. Capabilities for a TSV etch process that yields both a 5 by 50 micron and 1 by 20 micron etch depth profile are demonstrated. Measured TSV etch depths are also correlated with cross-section scanning electron microscopy results.

7971-57, Session 14

Overlay and focus stability control for sub-3x-nm nodes on immersion scanners

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As semiconductor technology is migrating into sub 3x nm nodes aggressively, the process windows for both CD and overlay are becoming increasingly tight. In order to meet such challenges, the overlay stability or lithography tools must be at the level of 1-2 nm within the product cycle time, while focus needs to be stable within 5 nm. In addition, for a mass production environment, well-matched tools are crucial to improve the flexibility of tool usage. In addition to this, the pressure for higher productivity will continue, allowing less time for periodic maintenance. To keep costs under control, all of this needs to be implemented without complicated fab automation systems and without the need for special, highly trained operators.

The BaseLiner platform consists of a software interface on the scanner and an offline scanner performance control system. The latter contains a correction feedback loop employing angle resolving scatterometry The feedback control is based on scheduled updates using a reference wafer set mimicking the production process. The applied metrology scheme provides high order interfield/intrafield corrections per scan direction making it the most comprehensive scanner correction available.

Here, we report on methods for the control wafers creation and selection with in-house processes. A sub-selection method was introduced to reduce the overlay difference between wafer sets in order to minimize the overlay impact when wafer exchange is needed. Then focus (FD) models were created and overlay metrology was qualified for the chosen illumination settings and processes.

Most importantly the tool stability for TWINSCANTM XT:1900i scanners for focus is found to be controlled in a range of less than 5 nm for focus while the total focus uniformity is improved from 30nm to 25 nm (Fig.1). Overlay is stabilized in a range of 2 nm (99.7% overlay, Fig.2) during a period of 30 days. The point-2-point (p2p) difference to the reference obtained on "Day0" is less than 4 nm. The scanner control was extended to control on products where the stability is compared with the fab's in-line metrology.

Additional to the basic product functionalities scanner control with customized illumination conditions and processes, but also matching, and WIP impact management were studied.

The capability of WIP handling was demonstrated based on several different scenarios such as tool interventions. Fig.3 shows that the product is able to recover the tool overlay status to the original state after an intervention. The simulated and measured recovery performance is in good agreement. Results of overlay matching between machines and illumination settings show that a match of 99.7% 8 nm (raw data, point-to-point tool status difference) can be obtained between two XT:1900i scanners.

7971-58, Session 14

Toward 22 nm: fast and effective reticle CD monitoring and minimizing the impact of reticle on intrafield CDU and process window

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ITRS lithography stringent specifications for 22nm node are a major challenge for the semiconductor industry. With EUV approaching point insertion node, ArF lithography is expected to stretch within its fundamental limits. The current prevailed view of holistic lithography methods, together with double patterning techniques, will target to bring lithography performance towards the 22nm node (i.e. closer to the immersion scanner resolution limit) to an acceptable level.

At resolution limit, the mask is a top contributor of systematic errors within the wafer intrafield domain. Amid diminishing ITRS CDU specification, it would be crucial to monitor the mask static and dynamic critical dimension (CD) changes in the fab and use the data to control the intrafield CDU performance in a most efficient way. Furthermore optimization and monitoring of process windows becomes more critical due to the presence of mask 3D effects [1]

This paper will present double patterning inter and intra field data, for CDU and PW monitoring and optimization, measured by aerial imaging mask inspection and CD-SEM tools.

Special emphasis was given to speed and effectiveness of the inspection for production environment.

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7971-59, Session 14

Focus budget breakdown for advanced process control in 3x-nm node DRAM device

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The semiconductor industry is aggressively pushed to produce smaller features with the existing ArF immersion systems. As design rule of memory device shrinks down to 3X nm node, its process window becomes so small that it is very hard to insure high production yield with current process control capability. So, high-accuracy focus monitoring and focus control techniques will be necessary for production of 3X nm node DRAM. Focus budget breakdown was carried out to identify individual focus budget contributors which can be classified into machine focus budgets and product-specific focus budgets. Through various tests, the total focus budget of ArF immersion scanner has been quantified. According to the focus budget breakdown result, there is some possibility to enhance overall focus control performance by applying AGILE leveling system which uses air-gauge focus sensor and CD-FEC (Circuit dependent focus edge clearance) system.

In this paper, focus budget breakdown procedures and test results will be discussed in detail and the optimum focus control methods for 3X nm node DRAM device will be proposed.

7971-60, Session 14

Automatic optimization of metrology sampling scheme for advanced process control

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Full overlay wafer maps of selective production wafers were first collected to estimate the maximum correctables with a variety of overlay correction schemes. Linear and High Order Process Correction (HOPC) models including Correction Per Exposure (CPE) and Intra-field HOPC (i-HOPC) were investigated and resulting correctable was compared to each other for the best possible performance. Once the optimal correction scheme was decided from the above-mentioned calculation the semi-empirical algorithm of overlay markers selection automatically produces a set of preferred measurement sites with desired sampling size. In one example the current production correction scheme resulted in 17% and 36% residual correctable in X and Y direction respectively, whereas our optimal correction model with 38% reduced sampling projected a superior performance of 13% and 16% residual correctable. A long-term time dependent overlay stability study indicated that the optimal scheme with reduced sampling has surprisingly better residual overlay variation in the range of 6%~21%, comparing to the current production scheme of 29%~32%. The enhanced overlay performance, the notably improved stability and the relatively low CoO in manufacturing by the proposed overlay scheme effectively enable researchers to continue the legend of device miniature in the next couple years without blocking.

7971-61, Session 14

Computational defect statistics in process analysis and control

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Reliability of manufacturing processes is the key to a stable performance and thus to customer satisfaction. In photo-mask manufacturing the quality of a single mask can be assessed with extremely high confidence due to the performance of manufacturing engineers and tool suppliers in the areas of mask metrology and mask inspection.

This ability in mask quality assessment enables process improvements as to increase the reliability, resulting in yield improvements. At the current state of the art in mask manufacturing the systematic effects impacting each mask in are quickly analyzed and addressed. Stochastic effects, however - whose probabilistic mask impact is driven by deterministic laws - are much more difficult to address. Defects are a prime example for deterrents of mask quality which have often a deterministic root cause but whose stochastic reproducibility hampers corrective actions. This type of behaviour tends to be especially pronounced for critical defects. Thus the underlying probability distribution needs to be constructed to enable improvement actions which can be achieved by the means of applying the statistical tools of spatial point pattern analysis to large sets of production masks.

In this paper we present how the tools of spatial point pattern analysis can be used to elucidate the origins of defects in the manufacturing process and to drive mask process improvements. It is shown how the pooling of mask data allows to construct the probability distribution of critical defects and how the specific shape of the probability distribution relates to the underlying mechanisms which generate defects. Pattern density dependent defects for example show a defect pair correlations distinctly different from design independent defects. Also the comparison of the defect localization pattern with stochastic simulations helps to elucidate the root cause of defects. Thus we are able to use the spatial distribution of defects in a novel way as to identify, classify and control defects in our manufacturing process.

In figures 1) and 2) we depict the typical graphical presentation of a spatial defect analysis for two distinct defect scenarios. Besides analyzing the defect size and counts on a mask (upper left) the defect density (upper right) and the inter defect distance (lower left) are depicted. This is complemented with a computational test for defect clustering in the lower right. Here, the observed defects densities as a function of distance from an average defect are tested against the theoretically computed density of random defect placement. In figure 1) the observed density lies within the expected ranged of densities thus

the defects are randomly distributed. In figure 2) clustering of defects is documented as the observed defect density is outside the confidence band of a random distribution.

7971-62, Session 14

CD uniformity improvement of through-pitch contact hole patterning for advanced logic devices

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Down sizing with miniaturization of semiconductor devices have brought high performance of the devices. However, it is difficult to maintain high yield and reliability of the devices because the process margin becomes narrower with the shrinkage of pattern sizes. Therefore, process control, especially control of CD uniformity (CDU), is becoming more and more important. For better across-wafer CDU, it is necessary to optimize CDs in both a lithography process step and an etching process step. Improvement of across-wafer CDU after etching by optimizing the post exposure bake (PEB) temperature or the exposure dose in lithography processes has been reported in the previous works [1] [2]. In those reports, the CDU of a particular pattern was improved while the CDUs of other patterns were not thoroughly considered. However, for most advanced logic devices, it is necessary to improve the CDUs of entire patterns including through-pitch patterns, because the logic devices require higher CD accuracy in random layout patterns with OPC.

In this report, we propose an enhanced across-wafer CDU improvement method considering through-pitch contact hole patterns. We evaluated contact holes with diameters less than 45nm after etching in this work. We tried two CDU optimizing methods: zone control of PEB temperature, and shot-by-shot exposure dose control. In addition, we carried out simulations using a fully calibrated physical resist model to analyze the detailed effects of each optimization method. From the simulation and experimental results, the advantages of each method are discussed in detail. It is found that the overall CD optimization by exposure dose control gives better through-pitch CDU than that by PEB temperature control. Furthermore, to have better CDU for random layout patterns by dose optimization, the middle pitch patterns which have middle CD/ dose slopes were suitable for the reference patterns. When dense or isolated patterns with much higher or lower CD/ dose slopes as the dose control reference patterns, the overall CDU of through-pitch patterns becomes worse.

As a result, the across-wafer CDU of through-pitch contact hole patterns was optimized by exposure dose control using the middle pitch patterns as the reference patterns. By this optimization, the CDUs for isolated patterns, dense patterns, and SRAM patterns were improved from 7.9 to 3.9 nm, from 6.2 to 2.6 nm, and from 5.3 to 2.6 nm in 3 respectively. After the CD optimization, CDs from target were nearly equal to that before the optimization. Therefore, our method was proved to be effective for CDU improvement of through-pitch contact holes in advanced logic devices.

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7972-01, Session 1

Critical challenges for EUV resist materials

P. P. Naulleau, Lawrence Berkeley National Lab. (United States)

No abstract available

7972-02, Session 1

Materials for directed self-assembly: functional properties and future needs

W. D. Hinsberg, IBM Almaden Research Ctr. (United States)

No abstract available

7972-03, Session 1

Materials innovation for sub-20-nm lithography challenges

J. W. Thackeray, Dow Electronic Materials (United States)

No abstract available

7972-04, Session 2

Solvent develop processing of chemically amplified resists: chemically, physics, and polymer science considerations

C. K. Ober, Cornell Univ. (United States)

No abstract available

7972-05, Session 2

Fundamental investigation of negative-tone development for the 22-nm node (and beyond)

G. Landie, STMicroelectronics (United States)

Negative Tone Development (NTD) is a promising technique to further expand the resolution limits of 193nm immersion lithography for contact holes and trenches. The benefits of bright field imaging with negative tone development over dark field imaging with a conventional positive tone process have already been demonstrated, both from a theoretical perspective and experimentally.

In this work, we investigate the negative tone develop process from a fundamental materials/process interaction perspective. Several key differences exist between a negative tone develop process and a traditional positive tone develop system. The organic solvent dissolves the unexposed, hydrophobic material, while the deprotected hydrophilic material remains intact. Thus, the surface energy interaction between developer, remaining resist, and underlying substrate are quite different, and as a result Resist/substrate adhesion in the presence of organic developer is an important consideration. In addition, the capillary forces that are responsible for resist collapse are different in the case of NTD, and are not currently understood. Also, the propensity for a partially deprotected polymer (that happens to be surrounded by fully non deprotected polymers) to become a resist residue defect is also quite different with NTD, and is not fully understood in either a positive tone or negative tone process.

We have carried out fundamental studies to understand these new interactions with negative tone develop systems, including contact angle/surface energy characterization, critical aspect ratio for collapse studies, and defectivity measurements. In addition, we present first results on OPC modeling and source-mask optimization results of current NTD resist/developer systems.

7972-06, Session 2

Top-coat free immersion lithography using negative-tone development

Y. C. Bae, C. E. Andes, R. Bell, T. Cardolaccia, S. Kang, Y. Liu, J. Sun, G. G. Barclay, The Dow Chemical Co. (United States)

Negative tone development (NTD) of conventional 193nm photoresists using an organic solvent developer relies on the polarity switch through the formation of methacrylic acid units in the patterned areas. This chemical change in the polymer backbone of the patterned areas can cause loss in the resist thickness and etch resistance. This can further result in the pattern collapse due to the polarity mismatch in the interface between resist and substrate films. This pattern collapse in the NTD process appears to be more severe on inorganic substrates such as Si hard mask. For example, dense line and space patterning is limited to 130nm pitch on inorganic substrates and 110nm pitch on organic substrates. In order to overcome these shortcomings with the NTD process, we developed top-coat free NTD optimized resists that give minimum thickness loss, improved etch resistance and excellent pattern collapse margin. In this paper, we will present our recent progress on the development of NTD optimized resists in terms of thickness loss, etch resistance and pattern collapse margin. In addition, we will discuss the effect of NTD developers and develop recipes on the defectivity in the contact hole lithography.

7972-07, Session 3

Assessment of resist outgassing related EUV optics contamination for CAR and non-CAR material chemistries

I. K. A. Pollentier, I. Neira, R. Gronheid, IMEC (Belgium)

EUV lithography is expected to be the key lithography option for sub-22nm device manufacturing. In order to meet the required imaging capability, resist performance improvements are being investigated by exploring both chemically amplified resists (CAR) and non-CAR chemistries. Another critical item related to resist chemistry is the EUV irradiation induced outgassing and its risk for optics contamination, especially towards high source power (pre-) productions tools. In this area it is important to characterize for the different chemistries which resist components are critical for EUV induced outgassing and - more important - which can result in non-cleanable mirror contamination.

In this paper, we will explore the outgassing and contamination behavior of CAR and non-CAR resist by using Residual Gas Analysis (RGA) for identifying the resist outgassing characteristics, by Witness Sample (WS) testing to evaluate the tendency for contamination, and by analytical techniques such as XPS (X-ray Photo-electron Spectroscopy) to identify non-cleanable elements.

For CAR resists, it has been found previously that the PAG cation is a key resist component resulting in non-cleanable contamination [1-2]. In this report, its contribution is investigated in more detail, but also the impact

of other resist components, such as the polymer structure, blocking groups, quencher, PAG anion, ... Recent results with polymer bound PAG containing model resists suggest that non-PAG species contribute also to the contamination, which is currently under investigation (see Figure 1).

For non-CAR resists, much less investigation has been reported so far. Therefore evaluations are ongoing with experimental imaging materials, but also with designed model polymers. For some materials, it has been found that the WS contamination is very limited, despite that a huge EUV outgassing is generated. These materials are currently under investigation, since they can provide information on high and low contaminating species. For other materials, it has been found that the contamination is reduced compared to a background contamination test, which suggests that some resist outgassing is able to remove carbon contamination.

The combined work on CAR and non-CAR outgassing and contamination is expected to provide understanding on how to design good performing EUV resists with minimal risk for optics contamination in EUV device manufacturing.

[1] I. Pollentier et al., Proc. SPIE, 7636 (2009)

[2] I. Pollentier, J. Photopolymer Science and Technology, Vol. 23 (5), p. 605-612 (2010)

7972-08, Session 3

Performance of EUV molecular resists based on fullerene derivatives

H. Oizumi, K. Matsunaga, K. Kaneyama, J. J. Santillan, G. Shiraishi, T. Itani, Semiconductor Leading Edge Technologies, Inc. (Japan)

The development of high-quality EUV resists is still the top-three critical issue in EUV lithography. Especially, line width roughness (LWR) is the most challenging issue. It is presumed that the cause of LWR from the standpoint of the resist material is non-uniform dissolution, which gives rise to “aggregates” in the resist sidewall. A potential solution to this is the use of molecular resists, which have two strong points concerning reduction of the LWR: One is the intrinsically small size of the molecules, which results in small “aggregates” and a small LWR; and the other is monodispersion, which provides uniform dissolution and a small LWR.

Recently in fabricating 2x-nm-test-devices using a full-field EUV exposure tool, dry-etching durability of a resist as well as resolution, LWR and sensitivity (R-L-S) performance is noteworthy. Last year, we reported the chemically-amplified positive-tone molecular resist based on fullerene resin named M100 with a high dry-etching-durability. These results showed a distinct possibility of practical use of fullerene based resists for device fabrication.

This presentation summarizes the systematic evaluation of EUV resists based on fullerene derivatives for practical use in device fabrication: a large supply of the fullerene resist, the optimization of the resin structure, its protection ratio, the formulation of PAG and quencher, under-layer materials, defect reduction and so on. We will demonstrate the fullerene resist performance (R-L-S, dry-etching-durability and resist outgassing) and will scope their potential for 22nm-hp and below. In addition, the application of the fullerene resists to actual test-device fabrication (2x-nm TEG) will be presented.

A part of this work is supported by New Energy and Industrial Technology Development Organization (NEDO).

7972-09, Session 3

Characterizing polymer bounded PAG-type EUV resist

S. Tarutani, H. Tamaoki, H. Tsubaki, T. Takahashi, H. Takizawa, H. Takahashi, FUJIFILM Corp. (Japan)

Extreme ultra violet (EUV) lithography process is one of the most promising candidates for half-pitch 22nm generation device manufacturing and beyond. In EUV lithography, great evolution of resist materials is as important as that of light source, exposure tool, and mask quality. The important performances required for EUV resist material are high sensitivity, excellent resolution, small line width roughness (LWR), and low out-gassing level. It is well known that there is triangle-tradeoff relation among the performances of sensitivity, resolution, and LWR. A lot of efforts have been paid to make a breakthrough in the tradeoff relation, however, these three performances can not simultaneously satisfy the ITRS roadmap target of hp 22 nm node at this moment. There are some resists satisfying sensitivity (10 mJ/cm2) alone, or resolution (hp 22 nm) alone. On the other hand, no resist could achieve the target LWR level of hp 22 nm node (<1.2nm) even if resists are specialized for LWR performance.

It is well known that acid diffusion length relates strongly to resolution. Long acid diffusion length leads large chemical blur in the resist film, that results worse resolution performance. Therefore, it is good method to suppress acid diffusion length through the resist process for achieving better resolution performance. There are some method to suppress acid diffusion length, for example, application of low post exposure bake (PEB) temperature, high Tg resist film, large molecular size of generated acid, anion-bounded polymer to generate acid-bounded polymer with EUV exposure, and so on. In recent years, several papers reported that good resolution was obtained with anion-bounded polymer type resist. However, there are few papers making discussion on characterization of polymer bounded PAG type resist to design materials.

In this paper, some results of material characterization will be shown with experimental data of dissolution rate, contrast curve, sensitivity, and PEB sensitivity for several materials having different PAG anion loading to polymer, acidity of generated acid, protection ratio, activation energy of protecting group, monomer type, and molecular weight. From these data, the design strategy of polymer bounded PAG will be discussed. Lithographic data with EUV exposure of the latest resist platform will be introduced as well.

7972-10, Session 4

Novel approaches to implement the self-aligned spacer double-patterning process toward 11-nm node and beyond

H. Yaegashi, K. Oyama, A. Hara, K. Yabe, S. Natori, S. Yamauchi, Tokyo Electron AT Ltd. (Japan)

Double Pattering process is one of the most promising lithography techniques for sub-40nm half-pitch technology node. Especially, Self-aligned spacer Double Patterning (SADP) has been adopted in NAND Flash memory devise manufacturing for 3X nm technology node and beyond. The uniqueness of our proposed SADP scheme is the utilizing of ultra-low temperature SiO2 film deposition for spacer pattern with photo-resist core pattern. It would contribute to simplify the process steps and to minimize any process deviations.

In this study, we would mention further more optimization of Pitch-Quadrupling using SADP and 2D pattern fabrication for 2X nm technology node and beyond.

7972-11, Session 4

The resist-core spacer pattering process for the fabrication of 2x-nm node semiconductor devices

K. Sho, Toshiba Corp. (Japan); T. Oori, K. Iida, K. Kikutani, Toshiba Materials Co., Ltd. (Japan); K. Yamamoto, F. Aiso, K. Matsunaga, E. Shiobara, K. Hashimoto, Toshiba Corp. (Japan)

The spacer patterning process is one of the strongest candidate in double-pattering technologies (DPT) for fabricating 2xnm-node semiconductor devices using ultra-low-k1 lithography. The most severe

problem of the spacer patterning process is its too many patterning steps, i.e., resist patterning step, core film etching step, spacer film deposition step, spacer film etchback step, core film removal step, hard mask patterning step, and so on.

In this paper, we studied simplified spacer patterning process where a resist pattern was directly used as the core film pattern. For the spacer film, we adopted a low-temperature-deposited oxide film, which could be fabricated around the resist pattern without damaging the resist material. This new spacer pattering process, “resist-core” spacer pattering process, can dramatically reduce the patterning steps. We applied the resist-core process to 2xnm-node semiconductor devices fabrication using an ArF immersion scanner.

We found that there were two key issues in the resist-core spacer pattering process. One is the controllability of the resist pattern profile, which could directly affected the spacer film pattern profile. Therefore, we clarified the effect of the resist profile by varying the resist patterning conditions such as resist materials, illumination conditions, and bottom anti-reflecting materials. The other is resist slimming method. Since the resist slimming process by over exposure dose might degrade the process margin, an additional slimming process should be implemented before spacer film deposition step. We compared two slimming method, a wet slimming and a dry slimming. The evaluation results will be shown at the presentation.

7972-12, Session 4

A novel double-patterning approach for 30-nm dense holes

S. D. Hsu, W. Wang, W. Hsieh, C. Huang, W. Wu, C. Shih, S. Shih, Nanya Technology Corp. (Taiwan)

Double Patterning Technology (DPT) was commonly accepted as the major workhorse beyond water immersion lithography for sub-38nm half-pitch line patterning before the EUV production. For dense hole patterning, classical DPT employs self-aligned spacer deposition and uses the intersection of horizontal and vertical lines to define the desired hole patterns. However, the increase in manufacturing cost and process complexity is tremendous. Several innovative approaches have been proposed and experimented to address the manufacturing and technical challenges.

A novel process of double patterned pillars combined image reverse will be proposed for the realization of low cost dense holes in 30nm node DRAM. The nature of pillar formation lithography provides much better optical contrast compared to the counterpart hole patterning with similar CD requirements. By the utilization of a reliable freezing process, double patterned pillars can be readily implemented. A novel image reverse process at the last stage defines the hole patterns with high fidelity.

In this paper, several freezing processes for the construction of the double patterned pillars were tested and compared, and 30nm double patterning pillars was demonstrated successfully. A variety of different image reverse processes will be investigated and discussed for their pros and cons. An economic approach with the optimized lithography performance will be proposed for the application of 30nm DRAM node.

7972-13, Session 4

Resist freezing process challenges on cross-pattern application

Z. Zhang, S. L. Light, K. Jain, A. J. Devilliers, Micron Technology, Inc. (United States)

In recent years, resist freezing technique are widely studied by photolithography industry from resist vendors to R&D manufacture fabs. Whether these freezing technique can be really used in the production is a still a question. In this paper, we studied 3 differents freezing methods (fluoride plasma freezing, chemical and thermal freezing) in R&D production fab in Micron. We use a cross pattern as a test vehicle-printing 2nd layer pattern directly on top of freezed 1st layer resist. A waved equal line and space pattern is chosen as a first layer and straight equal line and space is 2nd pattern to see process reliability.

In this paper, we throughly study the process through photo, dry etch, wet etch and defect and run production part to yield. We also build up Response Surface Model to control both 1st layer and 2nd layer CD after substrate etch. Thermal freezing process is very well controlled by this model, but chemical freezing process is still not good enough, which needs more study.

From process complex (also cost saving) view, thermal freezing is the most simple process, but high temperature baking will change the wave degree when print resit line is smaller than 50nm. Chemical freezing process requires extra offline track and fluoride plasma freezing needs extra dry etch tool.

In this paper the challenges for different freezing process are well studied by cross pattern.

7972-14, Session 4

Double-patterning lithography with photobase generators: a progress report

X. Gu, Y. Cho, T. Kawakami, Y. Hagiwara, T. Ogata, B. Rawlings, The Univ. of Texas at Austin (United States); A. K. Sundaresan, N. J. Turro, Columbia Univ. (United States); R. Bristol, J. M. Blackwell, Intel Corp. (United States); R. Gronheid, IMEC (Belgium); C. G. Willson, The Univ. of Texas at Austin (United States)

Double Patterning Lithography (DPL) with photobase generators allows the printing of grating images with twice the pitch of the grating on a mask e.g., it enables projection printing with a k factor near 0.125. Printing of 45nm half pitch gratings using a 90nm half pitch mask was reported last year, but the developed images displayed worse line edge roughness than a typical 193nm resist printing at 1:1. Efforts have been made to understand and limit the line edge roughness in this process. New DPL resists with polymer bound photoacid generators (PAGs) and resists with polymer bound photobase generators (PBGs) were successfully synthesized, characterized and tested. A number of photobase generators with varying absorbance and quantum efficiencies were also tested. In each case, the effect of formulation and process variables on the E factor of the resist was measured. The first images generated with a 193nm projection tool were made at IMEC in a pristine environment free of airborne base contaminants. These experiments showed the sensitivity of the process to adventitious base and they demonstrated the effect of limiting the mass transport of base and acid on the process. The process continues to look very promising.

7972-15, Session 4

Optimization of pitch-split double-patterning photoresist for applications at 16-nm node

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Pitch-Split lithography techniques have been identified as a possible method of continuing scaling of semiconductor devices beyond 74 nm pitch applications. We have previously characterized some initial pitch-split resist materials utilizing both chemical freeze and thermal cure process options, and demonstrated their use at 64 nm effective pitch. Over the past year, we have further refined the thermal cure materials to enhance focus/expose process latitude, resist profile, resist height,

lithographic defectivity, and stability of both first and second layer resist materials. We have also extended the resolution capability of the materials to 56 nm effective pitch applications, for line/space and via chain structures. Exceptional defectivity results have been obtained, similar to that for conventional single-layer resist patterning methods.

This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

7972-16, Session 5

In-situ dissolution analysis of EUV resists

T. Itani, J. J. Santillan, Semiconductor Leading Edge Technologies, Inc. (Japan)

Resist materials and processing are considered as one of the most critical issues in realizing next generation lithography technologies. Extensive research on high-performance resist materials and lately, improved methods for resist processing have been reported [1]. One such process that has been gaining attention in the past few years is resist development or dissolution [2]. The characterization of the resist dissolution process after exposure has also been continuously investigated in search for possible clues in the optimization of resist materials and processes.

As we have recently reported, a visual observation of the actual pattern formation of resists during dissolution was realized with the application of high speed atomic force microscopy (HS-AFM) [3]. The HS-AFM system (Nano Live Vision by Research Institute of Biomolecule Metrology) is equipped with highly sensitive, ultra-fast cantilever and AFM scanning capabilities. Utilizing this system, an in situ resist dissolution analysis method was established. Here, measurements were performed by preparing EUV resist (wafer) samples exposed at the small field exposure tool (SFET). Focusing on 32 nm isolated line (I/L) pattern, the physical changes of the exposed EUV resist film during development are observed and analyzed in situ.

With the application of this analysis method, it was further reported that the PHS-based polymer resist gradually dissolves with slight “swelling” properties while the acryl-based polymer resist showed significantly large “swelling” characteristics. On the other hand, gradual dissolution at finer film grains was observed with for the fullerene-based low molecular resist. Moreover, using the tetrabutylammonium hydroxide (TBAH) developer on the acryl-based polymer resist, “swelling” was reduced. [4]

In this paper, recent developments on the HS-AFM with the application of ultra-narrow cantilevers for the analysis of very fine line and space patterns will be presented. Moreover, with the application of an optimized and detailed analysis method, the in situ dissolution analysis of various polymer and low molecular resists will be shown. Lastly, findings on the fundamental research regarding the dissolution characteristics of unexposed polymer resins (i.e. PHS, Novolac) of varied molecular weights and dispersion conditions will be discussed.

7972-17, Session 5

Two complementary methods to characterize long-range proximity effects due to develop loading

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Variations in critical dimension (CD) as a function of the proximity of an individual feature to other exposed areas are a continuing problem both in mask fabrication and in optical lithography. For example, the CD uniformity (CDU) may degrade significantly depending on the proximity to densely or sparsely exposed areas. These pattern density effects will continue to worsen as feature sizes decrease to and beyond the 22 nm technology node.

Pattern density effects in electron beam lithography using chemically amplified resists are believed to arise from several sources. One such source, fogging refers to the backscattering of secondary electrons onto the resist to cause deviations from the nominal pattern size. A second contributor is acid volatility, where photogenerated acid is presumed to redeposit on the wafer or mask during exposure or bake; here we refer to this effect as chemical flare. A third source of pattern density effects is develop loading, which results in local depletion of developer in highly exposed regions. All three of these may simultaneously contribute to a net observed CD variation.

In this report we describe the application of two different techniques for evaluating these proximity effects. The first is based on electron-beam lithography patterning, and compares CD values of test patterns which are exposed under bright-field and dark-field conditions. The second uses a series of different test patterns formed by DUV (248nm) exposure and a custom liquid flow cell to separately characterize resist related density effects

7972-18, Session 5

Measurement of modulation transfer function using a linear resist

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In the 1970’s Tokyo Ohka Kogyo developed and marketed a deep UV resist based on poly(methyl isopropenyl ketone) under the name ODUR [1]. We now find that it is possible to process this resist in a fashion that provides a linear increase in dissolution rate with dose. This is a very rare resist characteristic. We know of no other materials that display this sort of behavior. While such behavior is not useful for imaging, it does allow the production of essentially pure sinusoidal relief images from interference lithography and it allows direct measurement of the modulation transfer function of 248 and 193 nm steppers. Measurement of the depth of development in the deepest and shallowest parts of the relief image can be correlated to the intensity function derived from simulators such as Prolith to display the actual intensity function in the resist. Experiments with this interesting material provide access to direct measurements of any tool related variance from the ideal intensity functions predicted by simulations.

Reference:

[1] M. Tsuda, S. Oikawa, Y. Nakamura, H. Nagata, A. Yokota, H, Nakane, T. Tsumori, Y. Nakane, and T. Mifune, Photographic Science and Engineering, volume 23, p 290, 1979.

7972-19, Session 5

Revisit pattern collapse for 15-nm node and beyond

K. Yoshimoto, IBM Corp. (United States); T. I. Wallow, GLOBALFOUNDRIES Inc. (United States); K. E. Petrillo, M. E. Colburn, IBM Corp. (United States)

Pattern collapse is the deformation of photoresist structures in response to unbalanced capillary forces present during the drying step of the lithographic process. There are some conventional methods to prevent it, e.g., reducing an aspect ratio of resist features, changing a contact angle between the patterns and the rinse solution. However, as the

critical dimension of resist features becomes comparable to polymer's characteristic length scale, their physical properties change significantly from the bulk. For example, molecular simulations indicate that at sub-50 nm length scale, the resist patterns become softer than the bulk, due to their higher surface-to-volume ratio [1]. In the case of EUV, the resists may get damaged and softened due to extremely intensive beams.

In this study, we will analyze various new data sets of pattern collapse obtained from 193 immersion and EUV tools. Arrays of test structures consisting of various line widths and spaces are used to characterize pattern collapse. A key metric of our analysis is the critical aspect ratio of pattern collapse (CARC). Previous study shows that CARC has a strong correlation with the space of one-dimensional patterns [2]. We will revise this relation with new sets of data collected from 22 nm and 15 nm test masks. The mechanical properties of resist patterns will also be estimated by fitting the data to a beam-bending model. Based on the analysis and characterization, we will discuss on an intrinsic limit of pattern size, in terms of dimension-dependent properties and polymer degradation during fabrication.

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7972-20, Session 5

Characteristics of main chain decomposable STAR polymer for EUV resist

J. Iwashita, T. Hirayama, I. Takagi, K. Matsuzawa, K. Suzuki, S. Yoshizawa, K. Konno, M. Yahagi, K. Sato, Tokyo Ohka Kogyo Co., Ltd. (Japan); S. Tagawa, K. Enomoto, Osaka Univ. (Japan) and JST-CREST (Japan); A. Oshima, Osaka Univ. (Japan)

The concept of nonlinear acid diffusion coefficient would be emphasized to achieve better latent image quality. [1] Focusing on realizing the concept, we previously reported about a main chain decomposable star shaped polymer (STAR polymer). [2] [3] STAR polymer consists of a core unit and several arm units which connect to the core unit with easily acid cleavable bonding. The main chain decomposition system is ideal to achieve promoted acid diffusion at exposed area because it accompanies great molecular weight reduction at exposed area. The significance of the STAR system had been confirmed for partially protected poly(p-hydroxystyrene) (PHS) considering arm length and core structure.

Employing p-hydroxy- -methylstylene (PHOMS) for arm structure, novel STAR polymer with appropriate Tg could be realized. Poly PHOMS is known to undergo acid-catalyzed decomposition from the polymer end. [4] Lithographic performance comparison between the STAR polymer and the control linear polymer using a Micro Exposure Tool (MET) would be exhibited.

Thermal property change with exposure and outgas property will be also discussed. Moreover main chain decomposition mechanism was investigated with flood EB irradiation.

7972-21, Session 6

Negative-tone imaging (NTi) at the 22-nm node: process and material development

J. R. Cantone, S. Dunn, S. Kawakami, TEL Technology Ctr., America, LLC (United States); K. E. Petrillo, Y. Xu, M. E. Colburn, IBM Corp. (United States); G. Landie, STMicroelectronics (United States)

Since difficulties exist in the implementation of EUVL for the 22nm node, it is beneficial to find new and creative ways to drive existing immersion lithography to smaller feature sizes. There is an ongoing effort to examine the application of the negative tone imaging (NTi - also called negative tone development, NTD) process for current and future nodes. Although NTi was once dismissed as a niche science because of swelling, high chemical reactivity with oxygen, and the need for special equipment needed for the solvent-based development, NTi photoresists (PR) typically exhibit stronger adhesion to Si and lower LER/LWR than that of positive tone photoresists. In addition, it has been shown that bright field imaging with a negative tone process has improved aerial image benefits compared to a similar structure imaged with a dark field mask and a positive tone process. Improvements in exposure latitude, DOF, and MEEF have been previously demonstrated for various structures. This paper will focus on process window, CDU, and defectivity optimization for trench and via structures. We will compare several advanced NTi photoresists, as well as solvent based developers, and present a methodology for quickly evaluating and optimizing new NTi materials.

7972-22, Session 6

High-volume manufacturing capability of negative-tone development process

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Double patterning process with 193 nm immersion lithography process is one of the candidate for 3x nm half pitch device manufacturing, and the possibility of extension to 2x nm half pitch device is now hot topic in 193 nm immersion lithography evolution. At the beginning, several kinds of double patterning method were proposed. Today, spacer defined process is being applied to the flash memory devices manufacturing. Positive tone freezing process is one of the candidates as cost reduction process of litho-etch-litho-etch (LELE) double line process, and has been studied by material supplier and equipment supplier in the viewpoint of material and process respectively. It is well known that it is very difficult to open narrow trenches below 40 nm with positive tone 193 nm immersion lithography process. Of course it is possible to form a trench pattern with LELE double line or freezing process, however, the trench size depends on the first line size, the second line size, and even overlay error of exposure tool as well, therefore, it is difficult to control trench size not only among wafers, but also across a wafer. This fact indicates that trench pattern should be formed just as trench pattern in one exposure step. However, there was no solution in narrow trench patterning with single exposure process.

Negative tone development (NTD) process has been proposed as one of double patterning method with 193 nm immersion lithography process for 3x nm below half pitch devices manufacturing. NTD process has big advantages for narrow trench and contact hole pattern imaging, since negative tone imaging enables to apply bright mask for these pattern with significantly high optical image contrast compared to positive tone imaging. Furthermore, combination of double exposure with both vertical and horizontal line and NTD process was proposed as good candidates for dense contact hole imaging down to sub-40 nm half pitch, through-pitch contact hole imaging, and complex array contact hole imaging process. Therefore, many IC manufacturers have become serious about applying this process to their device HVM due to its large ability in extension of application in recent years.

However, not enough discussions have been held in the viewpoint of high volume manufacturing capability. In this paper, defectivity, CD uniformity, and process stability with immersion lithography will be shown, and its capability for HVM will be discussed. The latest resist material for each process will be updated in this paper as well as process capability of this process.

7972-23, Session 6

Patterning conventional photoresists in environmentally friendly silicone fluids

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In this paper, we demonstrate the novel development of conventional photoresists in environmentally friendly silicone fluids. Silicone fluids are linear methyl siloxanes that only contain carbon, hydrogen, oxygen and silicon. They are not ozone-depleting, they are low in toxicity, and they contribute little to global warming. They degrade into naturally occurring compounds instead of accumulating in the atmosphere and can be recycled. Their unique physical and chemical properties also make them promising developers for lithography. For example, their low surface tension can eliminate the pattern collapse problem associated with high aspect-ratio features. Silicone fluids are non-polar solvents and their solvent strength is less than that of saturated hydrocarbons but stronger than that of the commercially available saturated hydrofluorocarbons and may be enhanced by adding other solvents. Two conventional photoresists used in this study, PBOCST and ESCAP are both insoluble in silicone fluids before or after exposure. However, the solubility of PBOCST and ESCAP in silicone fluids can be increased by using a silicon-containing additive. Using this strategy these resists were successfully patterned and subsequently developed in silicone fluids. Both resists are shown to be positive-tone when developed in aqueous base, however, we are able to show positive-tone images with PBOCST and negative-tone images with ESCAP in silicone fluids, with features as small as 60 nm. It was also shown that PBOCST developed in silicone fluids has a better sensitivity compared to the same resist developed in standard 0.26 N TMAH solution.

7972-25, Session 6

Patterning process study for 30-nm hole

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In order to continue scaling down the feature sizes of the devices until extreme ultraviolet lithography (EUVL) reaches to production capability, the methods such as double patterning technology (DPT) and spacer patterning technology (SPT) are applied for half pitch (hp) 2x~3x nm line / space imaging.

In the storage node of DRAM, both stable hole patterning and high k dielectric material development are key factors to secure the capacitance. In terms of hole patterning, we anticipate that hp 4x nm hole will be possible with combination of vertical and horizontal lines. But, the patterning process for hp 3x nm hole has to find a solution in trade-off relationship between process stability, complexity and cost of ownership (CoO) until EUVL is accomplished.

In this paper, we will demonstrate 3x nm hole patterning process using double patterning technology combined with negative tone development (NTD). Contrary to general method (positive tone development with dark field mask) for hole patterning, intention to use NTD with bright field mask will first be discussed. Evaluation and analysis of the simulated and actual wafer result will be discussed for CD uniformity improvement. In addition to patterning, overlay performance will be tested through NXT 1950i to confirm DPT process feasibility.

7972-26, Session 6

Surface property matching for negative-tone developing of a conventional positive-tone photoresist

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New patterning techniques always present a new set of challenges that material developers must overcome to allow for adoption of the process. The recent work on negative-tone developing (NTD) of conventional positive-tone ArF photoresists by organic solvents is not an exception. This technique uses higher-contrast bright-field imaging to produce exceptional contact hole and line space patterns. Bottom anti-reflective coatings (BARCs) are still required in the NTD process to enhance the resolution and to improve the adhesion of the photoresist. Changing the developer used does not change the reflectivity control of a BARC, but it does pose challenges to the adhesion of the photoresist, especially when the BARC is a spin-on silicon hardmask. The solvents used in the NTD process interact differently with the BARC-photoresist interface than the typical waterborne developer. Chemical mismatching at the BARC-resist interface can permit the solvent to penetrate and topple features. We will show control of resist adhesion through both process means and chemical modifications to the silicon BARC. Previously, we have shown that a conventional BARC coating between the hardmask and photoresist provides the correct surface for resist adhesion in NTD. We will extend that work by looking at the minimum organic BARC thickness required to prevent line collapse. Additionally, because silicon hardmasks are typically coated on top of a carbon-rich layer, we will investigate how different spin-on carbon films impact hardmask/resist adhesion through the thin hardmask layer. Resist adhesion will be evaluated by printing dense line patterns, and surface properties will be characterized using contact angle measurements and AFM.

7972-27, Session 7

Directed self-assembly for lithography applications

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Directed self-assembly (DSA), which combines self-assembled polymers and substrates with lithographically-defined directing prepatterns, has been considered as a potential candidate to extend the resolution limit of conventional lithography. Frequency multiplication and pattern rectification have been successfully demonstrated using block copolymers on patterned substrates defined by electron-beam lithography, EUV lithography or 193nm lithography have been demonstrated. Critical parameters such as DSA materials, process conditions as well as methods to prepare the directing prepatterns play significant roles in DSA performance. In this paper, we systematically investigate materials, directing prepatterns, and their interactions using experiments and simulations. Track-compatible DSA process and materials provide a simple and straight forward DSA platform to generate sub-lithographic line-space patterns and vias with precise placement and better CD uniformity.

7972-28, Session 7

Polymer blends for patterning applications

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Self-aligned double patterning (SADP) is one prominent scheme to extend 193 nm immersion lithography; however, the numerous inorganic material deposition and etch transfer steps significantly increase the cost of SADP schemes. Therefore, an SADP process based capable of forming spacers using a spin-on material and typical wafer track processing would eliminate a significant amount of process complexity and cost.

Directed self-assembly (DSA) provides an alternative approach to create sub-lithographic features. While most DSA demonstrations use block copolymers to create phase separated domains with precise periodicity, dimension, and morphology, the use of self-assembled polymer blends provides a simple, lower-cost route to generate phase-separated polymer domains. Without the intrinsic domain dimensions and symmetry characteristic of self-assembled block copolymers, polymer blends

form conforming sub-lithographical polymer structures with a variety of geometries. In particular, a self-assembling spin-on polymer blend system has potential as an alternative on-track technique to create sidewall spacers for SADP. In this paper, we report DSA results based on the combination of binary polymer blends and 193 nm resist topography. The materials, processes and pattern transfer of guided polymer blend patterns will be discussed.

7972-29, Session 7

Using controlled polymerization RAFT technology

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No abstract available

7972-51, Poster Session

EUV negative-resist based on thiol-yne system

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Extreme ultraviolet (EUV) lithography is a leading candidate to meet the requirements of the microelectronic industry roadmap. Development of resist for EUV lithography is one of the most important matters. Chemically amplified (CA) resist systems have been used for the highly sensitive KrF and ArF resist processes and many types of EUV resists based on the CA process have been investigated. In CA resists, diffusion of acids from exposed regions to unexposed regions during PEB treatment is a major contributing factor for the line width roughness and resolution limits. To overcome the limitations, it is a good challenge to develop non-conventional CA resists with high sensitivity. In this study, we have designed negative-tone EUV resist based on thiol-yne stepwise radical reactions. OH groups of poly(4-hydroxystyeren) (PHS) were modified with functional units bearing C-C triple bond structure. Resist was formulated as a mixture of modified-PHS, multifunctional thiol compound, and photo-radical generator. The present resist was developable with standard 2.38 wt% TMAHaq solution. The resist was highly sensitive to EUV exposure. The amount of outgas from the resist film was lower than that from the Selete standard resist.

7972-52, Poster Session

Molecular layer deposition of organic thin films for EUV photoresist applications

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Current photoresists face many challenges to meet the requirements of EUV lithography, such as ultrathin (less than 50 nm thick) and highly homogeneous films. One method to achieve the needed level of control over resist film thickness and composition is molecular layer deposition (MLD), which is an analogue to atomic layer deposition (ALD). MLD utilizes a series of self-limiting reactions of organic molecules at the substrate to build up thin films and provides a novel method by which to deposit photoresists. In this study, nanoscale organic resist films are deposited on silica substrates via urea-coupling reactions between isocyanate and amine functionalities in a layer-by-layer fashion using MLD. The organic films are designed to serve as chemically amplified photoresists via highly controlled incorporation of photoacid generators, acid-labile groups and matrix elements. The deposited films have a linear thickness dependence on number of MLD cycles as measured by ellipsometry. Urea-linkages within the MLD resists were confirmed by infrared spectroscopy, and X-ray photoelectron spectroscopy measurements showed that the resist films were deposited with stoichiometric composition. In addition, the MLD films had good thickness uniformity as investigated by atomic force microscopy. We incorporated alkyl- and aryl-sulfonium triflates into the MLD resist film via methylation of corresponding sulfides embedded within the backbones of the diamine precursors to achieve uniform distribution of photoacid generators, thereby avoiding the non-uniform distribution that can result from conventional spin-coating methods. These MLD resists show reactivity to electron beam irradiation, and the results show that nanoscale features can be achieved upon electron beam exposure. Results of applying the MLD films for advanced photoresist applications will be presented.

7972-53, Poster Session

High-sensitivity EUV-resists based on flourinated polymers

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There is a growing interest in the fluorinization of resist materials in improving pattern formation efficiency for extreme ultraviolet (EUV) lithography. The increased polymer absorption coefficient obtained through this resist platform is expected to enhance acid production and in effect improve pattern formation efficiency. Our work over the past several years has shown that the main-chain fluorinated base resins realized by the co-polymerization of tetrafluoroethylene (TFE) and norbornene derivatives offer high dissolution rates. Based on this, a EUV resist which was prepared by the fluorinated polymers was investigated. Imaging evaluations, using the small field exposure tool (SFET by Canon / EUVA) with annular (outer 0.7 / inner 0.3) illumination conditions were performed. Relatively high sensitivity of 6.3mJ cm-2 for half-pitch (hp) 45nm and satisfactory resolution limit of hp 40nm was achieved. At present, line width roughness (LWR) was measured at comparatively large values of more than 8.4nm at hp 45nm. Further material and process optimizations may be necessary to improve its present lithographic capability. However, these initial results have shown the potential of fluorinated-polymer based platform as a possible solution for high sensitivity, high resolution and low LWR EUV resists. During the conference, results obtained utilizing a number of protecting groups and photo acid generators will be presented.

7972-54, Poster Session

Characterization of EUV irradiation effects on polystyrene derivatives studied by x-ray photo-electron spectroscopy (XPS) and ultraviolet photo-electron spectroscopy (UPS)

H. Yamamoto, T. Kozawa, S. Tagawa, Osaka Univ. (Japan) and JST-CREST (Japan)

The resolving power of lithography has been improved by the repeated replacement of exposure tools toward shorter wavelength. With this trend, the energy of exposure tools has gradually increased. Currently, extreme ultraviolet (EUV) is expected as next generation lithography in mass production lines. The energy of exposure source will firstly exceed the ionization potential of resist materials by the deployment of EUV. Therefore, the ionization process dominates acid generation processes in EUV lithography. Reaction in resist materials induced by EUV photon is more complicate. In particular, the trade-off relationship between sensitivity, resolution and line edge roughness (LER) is the most serious problem in EUV lithography. The resist requirements for the EUV lithography are so strict that fundamental understanding of pattern formation reactions is strongly needed for the development of resist materials acceptable to mass production lines. X-ray Photoelectron Spectroscopy (XPS) and Ultraviolet photoelectron spectroscopy (UPS) provides information about chemical bonding as well as about

structure of the molecules. Thus, XPS and UPS is a powerful probe in the investigation of the molecular structure change induced by the EUV irradiation-degradation. In this study, the Structure degradations in polystyrene (PS) derivatives thin films induced by EUV radiation were analyzed by XPS and UPS.

PS derivatives were used as polymers. Propylene glycol monomethyl ether acetate (PGMEA) was used as a casting solvent. PS derivative solutions were spin-coated on gold-coated Si wafers to form ultrathin films. The thickness of the polymer films was estimated to be less than 20 nm. The sample films are thin enough to prevent any sample-charging problem arising from its electric non-conductive nature. The samples were exposed to EUV. After EUV exposure, the samples were introduced into JPS 9010MC XPS/UPS system. The cleanliness and structure change of samples was confirmed by XPS. The UPS spectra were recorded using SPECS UVS-300 UPS Source, He I radiation (h =21.2 eV). The energy resolution of analyzer is less than 0.2 eV, estimated from the Fermi edge of the Au-coated wafer. Also, the sample was biased by a variety of minus vias in order to estimate the ionization potential of degraded polymers.

The XPS and UPS spectra of degraded PS derivative films upon exposure to EUV photon were obtained. Also, the ionization potential of them was estimated. Structure degradations in polystyrene (PS) derivatives thin films induced by EUV radiation were analyzed by XPS and UPS. The effect on polymer structure on difference in them was discussed.

7972-55, Poster Session

Ultra-thin-film EUV resists beyond 20-nm lithography

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Extreme ultraviolet (EUV) lithography is one of the most promising technologies for achieving 22nm HP lithography and beyond. EUV resist is required to improve resolution limit down to less than 20nm hp. To achieve such a performance, innovative materials' development is necessary under ultra-thin resist film condition for preventing line collapse. In addition, more refined etching processes compatible with ultra-thin resist film are needed.

In this study, we will report our several approaches for both materials and processes towards forming less than 20nm HP pattern under ultra-thin film condition. We will also introduce our tri-layer system formed with combination of spin on glass (SOG) stack and organic spin on carbon (SOC) stack for refined etching process.

7972-56, Poster Session

Fundamental study on reaction mechanisms in chemically amplified extreme-ultraviolet resists by using 61-nm free-electron laser

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Extreme ultraviolet (EUV, 13.4 nm) is considered as the most promising exposure tool for the mass production of next-generation semiconductor devices. For chemically amplified EUV resists, secondary electrons derived from ionization events play a critical role in the sensitization of acid generators. The ionization occurs in spaces where energy is deposited by incident photons and /or secondary electrons. The microscopic space is called "spur". A several number of spurs are overlapped in EUV irradiations (multiple spur effect). The overlaps are considered in two cases. One is the case that the spurs generated by the same incident photon are overlapped, and the other is the case that the spurs generated by different incident photons are overlapped. In the former case, we have reported the relationships between spur distribution and acid distribution (acid generation efficiency and resolution blur) 1. The acid generation efficiency and resolution blur decrease with the increase in the average number of overlapped ion pairs because of the strong electric fields generated by multiple cations and the cross recombination. In the latter case, it may become a serious problem when a high-power EUV source is applied. In this presentation, we show the dependence of acid generation efficiency on dose rate (fluence per pulse duration) by using 61 nm free-electron laser (FEL) light irradiation of the SCSS test accelerator2. The wavelength of 61 nm (20.3 eV) is applied because single incident photon induces only single ionization event and resulting single spur, in contrast to the 13.4 nm photon that induces 4 ionization events on average. The 61 nm FEL has a pulse intensity as high as 30 uJ within a 300 fs pulse, where multiple photons produce successive photoabsorption events temporally and spatially close enough to make multi-spur events. This indicates the possibility to control the spur overlap by changing the incident pulse intensity and focusing size owing to that high peak intensity of FEL as well as the high absorption coefficient of the resist.

Acid yields generated in thin films were determined by spectroscopy. Poly(4-hydroxystyrene) (PHS) (Aldrich) was used as polymer matrices. Triphenylsulfonium triflate (TPS-tf; Midori Kagaku) was used as an acid generator. Coumarin 6 (C6; Aldrich) was used as an indicator to evaluate the acid (proton) concentration. These solutes were dissolved in tetrahydrofuran (Aldrich). The weight ratio of the polymers, TPS-tf, and C6 was 100:10:5 in all samples. The sample solutions were spin-coated onto quartz substrates at 3000 rpm for 45 s. Film thicknesses were about 1000 nm, which is enough to absorb the all irradiated energy. The samples were baked at 110 °C for 60 s and exposed to 61 nm FEL pulses generated by the SCSS test accelerator2. The absorption spectra were recorded by using a spectrophotometer (JASCO; V-550). The analyzing light passed through an aperture of 2 mm in diameter, which was set near the center of the exposed pattern.

Upon exposure to FEL pulse, radical cations of PHS and the secondary electrons are produced through ionization processes. The secondary electrons react with acid generators. Acid generators are decomposed to form counter anions of acids. Protons derived from PHS radical cations are mainly scavenged by C6. Therefore the acid yield is equal to the yield of proton adducts of C6 (C6H+). Two characteristic absorption bands which have been attributed to a neutral form (460 nm) and a C6H+ (~533 nm)3 were observed. The dose rate was controlled by changing Ar gas pressure in a vacuum line. The acid yield efficiency has enhances with decreasing the dose rate. It is suggested that high density ionization enhances the multiple spur effect. The details of reaction mechanisms are discussed.

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7972-57, Poster Session

Calculated reactivity analysis of photo-acid generators for EUV resist

M. Endo, S. Tagawa, Osaka Univ. (Japan) and JST-CREST (Japan)

We evaluated reactivity of photoacid generators for EUV resist using the quantum chemical calculation. As the secondary electron from the polymer in resist causes the reaction of photoacid generator, the reactivity of photoacid generator is determined as its electron affinity.

We performed optimization of the molecular structure with and without electron addition to the photoacid generator and calculated each molecular energy. We defined the difference of molecular energy as the stabilization energy, which can be the electron affinity of photoacid generator.

The typical substituent group to photoacid generators of triphenylsulfonium trifluoromethanesulfonate was investigated. We found that incorporation of electron withdrawing substituent group such as nitrile, fluorine, amino qroup enhances the reactivity of photoacid generators. The theoretical analysis will be discussed and we will propose the effective photoacid generators for EUV resist.

7972-59, Poster Session

Defect printability analysis in negative-tone development lithography

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In general, contact hole patterning has various challenges such as narrow process window, large mask error enhancement factor (MEEF), poor circularity, and low image contrast compared to line & space patterning. For that reason, it is difficult to make sub-60nm size contact hole with 193nm ArF immersion single process. In order to achieve sub-40nm contact hole patterning, we have need of shrink bias over 20nm. However, conventional pattern shrink technology such as resist reflow process is difficult to get shrink bias over 20nm because the shrink volume gets smaller as the pitch gets narrower.

Recently several authors have specifically noted the advantages of using negative tone materials for patterning narrow trenches. A new negative tone imaging with application of new developer to conventional ArF immersion resist materials is proposed for small contact hole pattern formation. Significantly better LWR and resolution on small contact hole pattern were observed with this negative tone development compared to positive tone development.

In this paper, we will introduce the experimental results of sub-40nm contact hole patterning using negative tone systems for contact hole patterning. We will report results of comprehensive studies of defects originating in negative tone photolithography and reveal the defect generation mechanism of each negative tone imaging-specific defect types

7972-60, Poster Session

A study on post-exposure delay of negative-tone resist and its chemistry

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Airborne amines are well known to drastically affect the lithographic performance of chemically amplified (CA) resists. Resist contamination with airborne amines or other bases can rapidly quench the photo-acid, generated during CA resist exposure process. This can severely disrupt the polymer deblocking of positive tone resists. Mild amine contamination causes variations in the critical dimension (CD) of resist patterns and T topping or no imaging in severe cases. Similarly, the quenching of the photo acid, interrupts the crosslinking mechanism of the negative resist, leading to printing slimmer lines, patterns film loss or even total resist washout in severe contamination.

The delay between resist exposure and post exposure bake (PEB) is the most critical time in the total process. This delay is called post exposure delay (PED). At this point the acid generated during the resist exposure step is present in the exposed patterns, however, it cannot catalyze the deblocking or crosslinking of the polymer unless it is heated (PEB).

That is with the exception of some acetal type resists that deblock at room temperature. The longer the PED, the more chance for the amine contaminant to get adsorbed in the resist film and quench the acid more effectively.

This study is limited to negative phenolic resin based resist formulations, comparing and relating their PED to their varied compositions. Key information was revealed in this investigation allowing the development of super stable PED resist. This resist endures more than 48 hours of PED out side of amine controlled fab environments without any significant changes in its patterns CD.

7972-61, Poster Session

Predicting resist sensitivity to chemical flare effects though use of exposure density gradient method

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A POR resist was found to have severe CD and profile variation between dense and non dense areas. Investigation led to the conclusion that this resist had a high susceptibility to what is described as chemical flare. Using an exposure density gradient design with testing patterns known susceptible to chemical flare a method is described in this paper for evaluating resists for chemical flare. Further, a quantifiable value defining a level of the chemical flare effect value that can be used for material evaluations and feedback to vendors is described.

7972-62, Poster Session

Deprotonation mechanism of poly(styrene-acrylate)-based chemically amplified resist

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Lithography using ionizing radiation such as extreme-ultraviolet (EUV) radiation and/or electron beam (EB) is expected in next-generation lithography. Poly(styrene-acrylate)-based resist, which has been used in KrF excimer laser (248 nm) lithography as a backbone polymer, is also one of the promising materials for EUV or EB lithography. Although the dynamics of the radical cation of polymer is an important key for elucidating the proton dynamics in resist materials, little investigation in copolymer system has been carried out so far [1-3].

In this study, the dependences of degree of copolymerization of poly(styrene-ran-methyl methacrylate) and poly(styrene-b-methyl methacrylate) (P(S-MMA)) on the deprotonation mechanism for EUV chemically amplified resists were investigated by pulse radiolysis method and on quantity of the acid yield.

1. EXPERIMENTAL

Pulse radiolysis experiments were carried out at the ISIR, Osaka University. Sample solutions were irradiated with an 8 ns electron pulse to induce radiation-chemical reactions. Short-lived intermediates were analyzed by using light from a Xe flash lamp. Polystyrene (PS), poly(methyl methacrylate) (PMMA), and P(S-MMA) were used as solutes in 1,2-dichloroethane.

Acid yields were determined by spectroscopic methods. The details have been reported previously [3,4]. Solutes (base polymer, triphenylsulfonium triflate and Coumarin 6 (C6) (10:1:0.5 (weight ratio))) were dissolved in tetrahydrofuran. PS, PMMA, and P(S-MMA) were used as base polymers. The solutions were spin-coated onto quartz substrates at 3000 rpm for 45 s. After baking at 70.0 C for 60 s, the samples were exposed to a 100 keV electron beam (ELS-7700H, ELIONIX) at Open Facility Hokkaido University. Absorptions in visible were measured by a spectrophotometer (V-570, JASCO).

2. RESULTS AND DISCUSSION

The dependences of degree of copolymerization on the acid yield were studied. In the previous result of poly(styrene-co-4-hydroxystyrene) [P(S-HS)], it was suggested that a hole transfer from radical cations of

PS units to PHS units is an important reaction before deprotonation [1]. In the case of P(S-MMA), a hole transfer from the radical cation of PMMA unit to the PS unit was assumed, because the ionization potential of the PS unit (8.5 eV) is lower than that of the PMMA unit (> 9.7 eV). The lower deprotonation efficiency of the PS unit than the PMMA unit (< 1/10) expects the significant decrease in acid yields with increase in PS mole%. However, with increase in the PS mole% in P(S-MMA) from 0 to ~50%, the acid yield shows no decrease in P(S-HS). It is suggested that radical cations of PMMA are mainly decomposed and deprotonated before the hole transfer to the PS unit. Therefore, the hole transfer is not an important reaction for deprotonation of the radical cations in P(S-MMA).

The transient absorption spectra of P(S-MMA) in 1,2-dichloroethane solutions were also observed by using pulse radiolysis to study charge localization on the PS unit. Absorption maxima at 500 nm are attributed to the overlapping of the monomer and the multimer radical cation of the PS unit. And, absorption maxima in the near-IR (1000~1200 nm) are assigned to the multimer radical cation. The oscillator strength of the two absorptions increases with mole fraction of PS with different tendencies. That of the former band shows the charge localization on the PS unit, and that of the latter band shows the delocalization on the PS unit. Assuming the intramolecular hole delocalization in the PS unit, the hole is spread into 2~3 unit (0.36~0.72 nm) in PS.

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7972-63, Poster Session

Diffusion of amines from resist to BARC layer

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In chemically amplified resist process, photo-chemically generated acid can diffuse in resist matrix, inducing the de-blocking reaction. To control the chemical reaction, small amounts of amines must be added. The concentration of amines in resist matrix should be constant during the post-exposure-bake treatment. In the practical resist processes, organic bottom anti-reflective coating (BARC) is essentially important to provide reflectivity control for resist patterning. However, in some cases, amines added as a quencher in resist layer can diffuse into BARC layer, which causes the undercut of resist patterns. In this study, we have studied the diffusion characteristics of amines from resist layer to BARC layer during post-exposure-bake treatment. The amine concentration in resist layer was estimated using the rate of de-blocking reaction of resist. It was found that the diffusion rate of amines from resist layer to BARC layer was negligibly low compared to the diffusion of acid.

7972-64, Poster Session

Reduction of micro-bridging defects for 193-nm immersion resists

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In this study, potential causes for micro-bridging defect were investigated and approaches to address each driving factor were proposed. The result confirms that post-develop hydrophobicity, polymer aggregation and acid diffusion length are main factors that contribute to the formation of micro-bridging defect. It is found that micro-bridging can be significantly reduced by applying smaller filter pore size and improving the wettablity of TMAH dwell. Introducing of bulky PAG also improves the defectivity performance. However, major OPC changes are needed for the PAG modification.

7972-65, Poster Session

Study of major factors to affect to photoresist profile on developable bottom anti-reflective coating process

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As critical dimensions continue to shrink in lithography, new materials will be needed to meet the new demands imposed by this shrinkage. Recently, there are needs for novel materials with various substrates and immersing process, including double patterning process, a high resolution implant process, and so on. Among such materials, Developable Bottom Anti-reflective Coating material (D-BARC) is a good candidate for high resolution implant application as well as double patterning application. D-BARC should have reflectivity control function as an ordinary BARC, as well as appropriate solubility in TMAH-based conventional developer after exposure and bake process. Major advantage of D-BARC is to skip BARC etch process that is required in normal BARC process. In spite of this advantage, the photoresist profile on D-BARC could be influenced by components and process condition of D-BARC. Several researchers and companies have tried to solve this issue to implement D-BARC to new process.

We have studied material-related factors to affect to resist profile, such as polymer, photo-acid generators (PAGs), and additives. And we researched the effect of process condition for photoresist and D-BARC. In case of polymer, we studied the effect of dissolution rate in developer, polarity, cross-linking functionality, and thermal properties. For PAGs and additives, the effect of acid diffusivity and cross-linking degree according to their bulkiness and blending ratio were examined. We also evaluated coated film stability in a resist solvent after BARC bake process and compared lithographic performance of various D-BARC formulations. In addition, the effect of photoresist profile with bake condition of photoresist and D-BARC were investigated. In this paper, we will demonstrate the most influential factors of D-BARC to photoresist profile and suggest the optimum formulation and process condition for D-BARC application.

7972-66, Poster Session

Photo-initiated polymerization of new hybrid monomer containing vinyl ether and (methyl) acryloyl groups

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The photopolymerization kinetics of 4-(vinyloxy)butyl methacrylate containing cationic and radical polymerizable vinyl groups was studied by Fourier transform real-time infrared spectroscopy (FIRT) .The cationic polymerizable vinyl ether moieties(Vc) of the hybrid monomer in solution polymerized rapidly by exposure to UV light in presence of a cationic photoinitiator such as an iodonium salt or suflonium salt .High conversions, of 90%, were obtained for most of the systems investigated. The efficiency of the cationic photoinitiators in initiating the polymerization of the vinyl ether moieties (Vc) of the hybrid monomer was in the order: suflonium salt > iodonium salt . The radical polymerizable C=C groups (Vr) of the hybrid monomer in solution polymerized by exposure to UV light in presence of a radical photoinitiator such as 2,4,6-trimethyl benzoyl diphenylphoshine oxide (TPO), 2-isopropyl thioxanthone (ITX) , Phenylbis(2,4,6-trimethylbenzoyl)phosphine oxide (Irgacure 819), 2-Methyl-4'-(methylthio)-2-morpholinopropiophenone (907), or Double 2,6 - difluoro -3 - pyrrolo-phenyl-titanocene (FMT). Among the photoinitiators , the best effect in initiating the polymerization of C=C groups (Vr) of the hybrid monomer is initiator 907 and FMT as a photosensitizer.

7972-67, Poster Session

Analysis of the generating action of the acid from PAG using acid-sensitive dyes

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The Acid Sensitive Dyes (ASD) to which it colors with acid is used for a fixed quantity of the acid generated from PAG, and reaction analysis. Until now, the analysis method is examined [1-2]. This method should just add an ASD to resist. The generating action of acid can be known. It is a very simple method. The resist containing coloring material is applied to a quartz board by the conventional method. Next, it exposes and absorbance in 530nm is measured with a spectroscope after that. However, by this method, the coloring ingredient after exposure causes a variation per hour (breaching reaction). Then, we made the equipment which can measure 530nm absorbance by In-situ as an experiment, glaring 193nm light. Using this equipment, since measurement of the generating reaction constant of acid was tried, some PAG(s) are reported.

[1]Proc. SPIE 6923, 44 (2008).

[2]Proc. SPIE 6923, 97 (2008).

7972-68, Poster Session

Simulation of the formation of undercut for a Novolac-based negative photoresist

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Novolac based negative photoresist has the potential of high resolution, high thermal stability and can form useful undercut profile for lift-off process. The degree of the undercut is critical for the successful lift-off process. It's controlled by both the resist formulation and the process condition. In this paper, we use a couple of simple models, which describe the exposure kinetics, crosslink reaction kinetics and development process, to simulate the formation of undercut for this kind of resist.

The aerial image of mask caused the formation of exposure product distribution in the resist through exposure, with the addition of non-bleachable dye, this distribution not only through the horizontal, but also through the vertical of the resist. During PEB these compounds caused crosslink reaction of the resist and thus formed resist dissolution distribution, and through development this distribution of resist dissolution finally transferred to photoresist profile. Our simulation focused on how the information of the mask is transferred from one process to the other and how the process factors and resist formulation affected the information transfer.

The aerial image was calculated for both dense and isolation patterns with CD from 5μm to 0.5μm. The exposure kinetics was modeled based on the absorption of the resist with different PAGs and dyes. The critical part is the development simulation. We measured the dissolution rate of the resist with different exposure energy, and dissolution rate of the resist with certain crosslink degree, thus got the relationship between exposure energy, crosslink degree and dissolution rate. These experiment data was used as the model parameter crosslink reaction kinetics and development process simulation.

By changing the formulation and process condition, their impact on the above kinetics was calculated and compared with X SEM profile of the resist.

7972-69, Poster Session

Primary structure control of ArF resist polymer by regulating feed rate of monomers and initiator

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Optical lithography has been the workhorse of semiconductor manufacturing ever since its inception. half pitch is becoming narrower and narrower, at the same time, requirement to resist materials is also increasing. In particular, resist polymer has large effect to resist performances such as line edge roughness (LER), and defectivity. The defectivity is serious problem, because it decrease yields ratio and increase production cost.

For the purpose of decreasing the defect risk, we focused on a primary structure of a polymer such as molecular weight, composition of comonomer and its sequence. Our goal is to produce "homogeneous" polymer in term of primary structures. Concerning to a typical radical polymerization, molecular weight and composition are controllable by regulating feed rate of initiator and monomers, because molecular weight depends on a ratio between initiator and monomer, and composition of comonomer depends on the ratio among the comonomers. The important point to produce homogeneous polymer is to keep a constant ratio of initiator and monomers during the reaction.

For the search of optimum parameter toward the homogeneous polymerization, we constructed a simulation program to predict the polymerization reaction. The program is based on the theoretical equation for the radical polymerization.

The simulation result of a usual semi batch reaction indicates the production of off target polymers , so-called heterogeneous polymers in early and latter phases. We resolve these problems in a stepwise manner by the control of feed of initiator and monomers. In a first step, the heterogeneity in the early phase of polymerization was resolved , as the next step, the heterogeneity in the latter phase was cleared away.

As mentioned above, heterogeneous polymers are produced in early and latter phases. However in the middle phase, the composition showed good agreement with the target value. This result means the ratio of comonomers in a vessel was ideal state in the middle phase. Thus, based on this finding, we tried to maintain the ideal comonomer ratio in the vessel from the start to the end of the polymerization.

We also defined "heterogeneity" of the bulk resin as the content of heterogeneous polymer (accurate definition will be presented in front of the poster). The smaller heterogeneity means more precise control of the polymerization.

We examined actual homogenized polymerization in the procedure sophisticated by above simulations. As the results, molecular weight and composition of homogenized polymer were nicely controlled and showed excellent agreement with simulation results.

We also studied estimations concerning to resist performance of the homogenized polymer. For instance, solubility of the homogenized polymer to the resist solvents is greater than that of polymer obtained by usual semi-batch polymerization, even though two polymers have almost same composition and molecular weight as the average. In addition, the polymer with smaller heterogeneity has greater solubility. This result shows heterogeneity is usable as a ruler to measure resist performances of the bulk polymer. It is expected that a homogenized polymer exercise a good resist performance such as the defectivity.

7972-70, Poster Session

Double-patterning lithography using one-stage and two-stage carbamate photobase generators

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As recently described by Willson and co-workers, double patterning can be achieved through a single-exposure method by utilizing both photoacid generators (PAGs) and photobase generators (PBGs) in the same photoresist. The key to successful double patterning is controlling the relative rates and concentrations of the PAG and PBG to control the net concentration of acid as a function of dose. In low dose regimes, it is required that the concentration of photobase be minimal so as not to suppress polymer deprotection. On the other hand, at the highest doses, the amount of photobase needs to be sufficient to neutralize the photoacid and prevent polymer deprotection.

We are interested in developing new types of photobase generators where the amount of base created is minimized at low doses and maximized at high dose. In order to achieve this, we have designed several types of potential two-stage photobase generators which require two sequential photochemical steps to create a base strong enough to neutralize the polymer deprotection. This is represented by equation 1 where rather than utilizing a true PBG in the initial formulation, we use a latent PBG where the real PBG is created photochemically in the film during the exposure. Representative examples of latent PBG's are provided in Figure 1 and include both carbamate and arylamide systems, both of which are known to possess rich photochemistry.

In order to assess these types of molecules as two-stage PBG's capable of effecting dual tone imaging, we have combined lithographic imaging experiments with detailed mechanistic experiments aimed at identifying the photoproducts formed and assessing relative rates of two-stage photochemical processes. Both film exposures (193nm and 254nm) and solution exposures (254nm) have been utilized for these studies. Post-exposure analysis has utilized a number of common techniques including NMR, UV-vis, HPLC-MS and fluorescence spectroscopy to detect and quantify intermediates and photoproducts. Some details for these techniques are provided below:

General details of NMR study: 5-10 mM solutions of PBGs with 5 wt% methacrylate polymer were prepared in 2-heptanone and thin films were cast on silicon wafer. Typically, the wafers were exposed uniformly to193 nm UV light source for durations corresponding to 0, 10, 20, 40, 80,160 mJ/cm2 dose. The exposed resist films were extracted using dichloromethane as a solvent which was subsequently removed after extraction by roto-evaporation. The solids were redissolved in appropriate deuterated NMR solvent. For solution studies, 5 mM of PBGs in deuterated acetonitrile were prepared in quartz NMR tube. The tubes were periodically exposed to DUV source followed by NMR measurements.

General details of Fluorescence study: The amines generated from PBGs by UV exposure could be selectively detected by derivatizing them with dansyl chloride. Dansyl Chloride derivatives of amine fluoresce at 504 nm wavelength. The amines generated in resist films were extracted by methanol and dansylated derivatives were detected to 1 nM concentration. The growth of the amine concentration as function of UV dose allowed kinetic characterization of the decomposition reaction.

General details of HPLC study : The decomposition kinetics of PBGs generated from PBGs were investigated by HPLC. The HPLC method, using a C18 column and UV-visible detector combination, allowed detection of 1μM concentration of PBG. The sample preparation for this method was similar to NMR. Kinetic parameters for the loss of PBGs were found to be similar to that observed by NMR.

7972-71, Poster Session

Polymer-bound photobase generators and photo-acid generators for pitch-division lithography

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The semiconductor industry is pursuing several processes that provide pathways to print images smaller than the theoretical resolution limit of 193 nm projection scanners. These processes include double patterning, side wall deposition and pitch division. Pitch doubling lithography (PDL), the achievement of pitch division by addition of a photobase generator (PBG) to typical 193 nm resist formulations was recently presented. Controlling the net acid concentration as a function of dose by incorporating both a photoacid generator (PAG) and a PBG in the resist formulation imparts a resist dissolution rate response modulation at twice the frequency of the aerial image. Simulation and patterning of 45 nm half pitch L/S patterns produced using a 90 nm half pitch mask were reported. Pitch division was achieved, but the line edge roughness of the resulting image did not meet the current standard. To reduce line edge roughness, polymer bound PBGs and polymer bound PAGs were investigated in the PDL resist formulations. The synthesis, purification, analysis, and functional performance of various polymers containing PBG or PAG monomers are described herein. Both polymer bound PBG with monomeric PAG and polymer bound PAG with monomeric PBG showed a PDL response. The performance of the polymer bound formulations is compared to the same formulations with small molecule analogs of PAG and PBG.

7972-72, Poster Session

Single-component photo-acid and photobase generators for single-exposure pitch division

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The efficacy of replacement technologies for 193nm lithography is uncertain. Patterning at this wavelength is the current industry standard and represents a tremendous investment in equipment and research. At present, these factors have ensured the value of new and progressive solutions in 193nm technology. Since the availability of new optical improvements is difficult to guarantee, the pursuit of more sophisticated resist-driven solutions is not only prudent, but promises to be increasingly rewarding.

Double patterning has emerged as a proven extension of 193nm lithography. Its continued implementation stands to benefit from a higher degree of chemical complexity in the resist layer. Inspired by previous research from the Willson group,1 we are interested in using photoacid generators (PAGs) which are covalently coupled to photobase generators (PBGs) to effectively double the pattern density with a single exposure. Two classes of molecules shown below (carbamate PBG's and acetamide PBG's) have been synthesized and their photochemical properties have been studied in solution and in film using a variety of analytical techniques including UV-vis spectroscopy and 1H NMR spectroscopy. Preliminary lithographic performance of these new single component PAG/PBG molecules will be reported.

Other variations of these structures are being prepared and will be characterized in the same way. In both architectures, the PAG operates normally. The base would either originate from the decomposition of the nitrated carbamate (left) or from a photo-Fries rearrangement (right) of the acetamide. In each case, acid generation is more efficient than base generation, resulting in regions as shown in the illustration below. Where dose is low neither acid or base is generated and the polymer remains (grey). Where dose is moderate, acid is generated, base is not, and the polymer is destroyed and removed by solvent (blue). Where the dose is high, both acid and base are generated. The base quenches the generated acid and the polymer remains intact (yellow). Through this process the pitch is doubled via a single exposure. Preliminary data suggests that the PAG and PBG rates of photodecomposition occur as we suggest. Sharp contrast curves have already been observed.

These compounds offer some possible advantages over multiple component formulation (having both a PAG and a PBG components). First, the close proximity of the PAG and PBG may reduce line roughness by limiting diffusion. Additionally, stoichiometry is already built into each

of these systems. It would be possible to design other PAGPBGs having ratios besides unity.

By characterizing these advanced materials, we hope to draw mechanistic conclusions that will help us to design future generations of hybrid PAGPBGs.

1 Willson, C. G. et al, Proc. SPIE, Vol. 7639, p. 763906, 2010.

7972-73, Poster Session

Development of molecular resists based on Phenyl[4]calixarene derivatives for EUVL/EBL

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Extreme Ultra Violet (EUV) Lithography and direct Electron Beam (EB) Lithography are the candidates for 22nm half-pitch manufacturing. For both EUV and EB Lithographic technologies, several resist materials having high-resolution and low line-edge-roughness have been studied. However, with reducing to 32nm half-pitch, patterns of the resist materials are inclined to collapse.

In our latest works, we have confirmed that a molecule designed hydroxy-substituents openly restrained patterns from collapsing, however forced to reduce its sensitivity. Then, we proposed that the molecule additionally controlled the ratio of hydroxy-substituents in the molecule, obtained high-sensitivity and high-resolution, simultaneously.

In this study, we synthesized and evaluated negative-tone lithographic properties of the molecular, designed hydroxy-substituents openly and additionally controlled the ratio of hydroxy-substituents.

The hydroxylphenyl calix[4]resorcinarene derivative, CR-1 was synthesized by the condensation of alkoxyphenol and hydroxybenzaldehyde. The product has far higher solubility to a casting solvent such as propylene glycol monomethyl ether (PGME) or cyclohexanone (CHN), than C-4-cyclohexylphenylcalix[4]resorcinarene , CR-2.

We evaluated a negative-tone molecular resist containing CR-1 by EB Lithography, direct writing with an incident energy of 50keV. The resist was prepared from five components: CR-1, photoacid generator, quencher, cross-linker and solvent. The resist was spin-coated onto an organic layer primed silicon wafer, then baked at 110 for 90 s. After EB exposing, the wafer was baked at 110 for 90s, and was developed in 0.26N TMAH for 60s. As a result, half-pitch 25-50nm Line & Space (1:1) patterns were drawn at an EB exposure dose of approximately 50 μC/cm2. The patterns obtained by resist containing CR-1 were more smooth and well-defined than the patterns obtained by resist containing CR-2. The resist containing CR-1 also demonstrated the possibility of well-defined hp 20nm patterns.

Those conclusions suggested that the molecular designed hydroxy-substituents openly and additionally controlled the ratio of hydroxy-substituents in the molecule would be a remedy for pattern-collapsing and low-sensitivity.

7972-75, Poster Session

Si-based materials with good gap-fill and planarization properties in the pattern of high-aspect-ratio up to 36 for semiconductor application

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The importance of microelectronic devices has increased ever more in the information technology which demands ever smaller and faster devices. For increase of electron density, the shrinkage of feature size in microelectronic devices has been strongly needed, and the aspect ratio of deep hole pattern also has been dramatically increased with reduction of bottom length. For a secure construction of hole pattern with high aspect ratio, materials with good gap-fill and planarization properties are strongly needed. And electrical and physical damage onto substrate or accumulated structure should be forbidden through the process of gap-fill polymer coating, cross-linking, and elimination.

In this study, Si-based polymer with good gap-fill and planarization properties was synthesized and evaluated. This polymer could be filled without any void in the pattern of aspect ratio between 25 and 36 (i.e. 1800 nm height, 50 nm ~ 70 nm width). Also as this material is developable in basic aqueous solution, evenly partial filled pattern can be obtained.

The silicone polymer was synthesized by well-estabilished sol-gel method with alkyltrialkoxysilane. This polymer was cured at mild and low temperature (90 ~ 110), and the cured polymer can be easily removed by wet etch method with HF solution (breaking Si-O-Si bond) or clearly developed by weak basic solution such as tertramethylamonium hydroxide (TMAH) solution (dissolving polymer), without residual defects on the substrate surface.

Furthermore, we can control the dissolution speed in TMAH solution by changing the polarity of the polymer and the developing conditions. Using this technology we achieved the evenly partial filled pattern with the silicone polymer.

7972-76, Poster Session

Development of new Si-contained hardmask for trilayer process

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In the advanced semiconductor mass production, the tri-layer process have been used for the essential technique{photoresist/ silicon contained hard mask (Si-HM) / spin on carbon hard mask (SOC)}.Tri-layer process was introduced and applied to various L/S and C/H patterning in the ArF and ArF immersion lithography. Therefore, Si-HM should have the wider photoresist compatibility. To get wider resist compatibility, we investigate the interface behavior between photoresist and Si-HM in detail.

As the design rule shrinks, thickness of photoresist should be thinner due to the aspect ratio concerns. The requirement of Si-HM is classified into two direction. First is the n/k control that achieves low reflectivity in thin film thickness. From optical simulation result, high-n/high-k material is needed at the thinner stack. We found that the amount of Si-OH increase by using conventional chromophore to achieve the suitable n/k value. Surface Si-OH group significantly decrease the adhesion ability between photoresist and Si-HM interface during the alkaline developing process. In this study, we propose the novel chromophore to get high adhesion ability with photoresist. Second is the faster etching rate at pattern transfer etching (Si-HM open etch) with CFx plasma to get high etching selectivity for thin photoresist. To get faster etching rate with the CFx chemistry, we investigate the relationship between CFx plasma etching rate and material composition of Si-HM

In this study, we will discuss the detail of our approach and materials for tri-layer process.

7972-77, Poster Session

Etch durable spin-on hardmask

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As decreasing the device feature size, the film stack structure used in resist process is also changing. Especially multi-layer stack film structure is getting popular for pattern formation on critical layers. This is due to the thinning of resist film thickness and the introduction of planarization layers, which can improve the resist process latitude and endure the etching attack. Especially in a case of the very thick etched film like storage node formation in DRAM device, the selection of hard-mask

material is very critical.

Mainly harmask material can be divided into tow kinds, which are CVD type and spin-coating type. CVD hardmask like a CVD-Carbon film is very attractive for ensuring the high etching selection ratio, but has still big problems in particle reduction, alignment accuracy, non-planarized substrate and high cost process. On the other hands, Spin-coating type is very attractive for low cost process, highly planarized substrate and high alignment accuracy and no particle. Then, device maker is selecting these hardmask materials for individual application.

But only one weak point of spin-coating type hardmask is low etching endurability. This low etching endurability causes increase of LWR value and wiggling behavior. One example is shown in figure 1. The reason of the wiggled pattern generation is thought to be the knock-on of F ions into spin-on hardmask and/or the atom exchange reaction generation from H atom of organic polymer used in spin-on material to F atom of etching gas during etching process.

Material suppliers are struggling to develop spin-on coating hardmask material with low etching damage. One way of the solutions is to reduce the Carbon contents volume in polymer. But at this moment only this approach is not sufficient. Various kinds of approaches are expected greatly.

We are approaching to formation of spin-on hardmask film with high etching resistance by introduction of new baking function. The result showed that spin-on hardmask film operated by TEL underlayer coating system has drastically good etch resistance than that by conventional system. We will report the availability of new underlayer system using several kinds of underlayer materials.

7972-78, Poster Session

Implementation of KrF DBARCs for implant applications on advanced lithography nodes

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Almost a decade ago, the integrated circuit (IC) industry realized that traditional implant layers required new technology to achieve the requirements of the shrinking design rules and increased topography effects. In response, developer-soluble bottom anti-reflective coatings (DBARCs) were introduced. These DBARCs excelled over the traditional combination of single- layer resist and dyed resist/top anti-reflective coating (TARC). DBARCs offered the resolution and critical dimension (CD) control needed for the increasingly critical implant layers.

Traditionally, DBARCs have been wholly developer-soluble systems, exhibiting isotropic development. These systems are being used in more mature implant processes to attenuate light. As applications with more advanced designs expand, the traditional DBARCs may show issues with profiles, and clearing from small spaces, making through-pitch and topography performance unsatisfactory. In response, photosensitive (PS) DBARCs were developed that are anisotropic when developed. These PS DBARCs allow better CD control, improved resolution, through pitch behavior, enhanced clearing from small spaces and may increase resolution.

In this paper, the various merits of the PS DBARC technology will be addressed. Lithographic performance, focusing on CD control over topography and through-pitch behavior, demonstrated the inherent benefit of PS DBARC over the alternative solutions. Small-space residue testing showed the benefit of PS DBARCs for cleanout of sub 100nm trenches. A study of improved post-develop residue in various ion-implantation processes validated the use of new PS DBARC materials in implant layers.

7972-79, Poster Session

A study of conductive material for e-beam lithography

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As the critical pitch continues to shrink, E-beam and EUV are considered as the potential solutions instead of immersion lithography for 16-nm node and beyond. Unlike conventional optical system, electron-charging effect is one of the new concerns for E-beam lithography. During E-beam exposure, resist can trap charge and delay charge dissipation from the resist surface to the underlying substrate. Accumulated charge on the resist perturbs the electron route and result in pattern distortion or failure. Therefore, reducing the charge cumulation effect is vital and urgent for high-pattern-density manufacturing.

In this paper, a new bottom conductive material is evaluated. The result is positive. This bottom conductive layer is coated and formed under the imaging resist layer. The e-beams from the SEM are used to charge the resist image for evaluation. The conductive bottom layer shows better charge dissipation than the non-conductive BARC. The CD shrinkage by SEM charging is improved from 18% to 24% on the conductive material. Encouraged by this promising result, we will evaluate the feasibility of new conductive topcoats and bottom materials on the E-beam lithography tool. The influence to pattern quality, proximity, and resolution will be compared and discussed.

7972-80, Poster Session

Development of plant-based resist materials in electron-beam lithography

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Electron beam lithography has great potential for future production of photomasks, nano-imprint templates, light-emitting diodes, solar cell devices, actuators, biosensors, and micro electro mechanical systems (MEMS) where continued success ultimately requires improvements in current processing technologies. Electron beam lithography is promising for advancing multiple electronic applications due to several advantages such as high resolution, deep depth of focus, flexibility in material design, and assumable cost.

This study presents progress in the development of a new plant-based resist material (TPU-EBR) to achieve high sensitivity and the optimization of process conditions in electron beam lithography.

Highly efficient crosslinking properties and high-quality patterning line images were provided by specific process conditions of 30-100 keV electron beam lithography. The validity of our approach using the developed plant-based resist materials were confirmed experimentally. This new approach was demonstrated to apply dextrin derivative as an eco-friendlier compound to the resist materials in nano-patterning processes for environmentally-compatible electronic device fabrications.

7972-81, Poster Session

Environmentally friendly natural materials-based photo-acid generators for next-generation photolithography

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Photoacid generators (PAGs) are photosensitive materials capable of releasing protons (H+) upon exposure to UV irradiation. Because the

generation of strong acid is fast and well controlled, PAGs have been extensively used in the field of photolithography. Among the many types of PAGs, ionic materials based on the perfluorooctane sulfonate (PFOS) anion have been widely used because of their unique properties, including exceptional strength of the photo-released acid and good solubility in common processing solvents. However, recently the use of PFOS-based PAGs has come under regulation, as environmental investigations revealed toxic properties and bioaccumulation problems with PFOS. In addition to environmental concerns, PFOS-based PAGs may have the disadvantage of PAG segregation from the photoresist induced by their highly fluorinated nature. It is thus desirable to develop alternative PAGs which satisfy both environmental and materials performance issues. We have developed PFOS-free ionic PAGs with functionalized octafluoro-3-oxapentanesulfonate anions. Compared with conventional PFOS-based PAGs, the new PAGs with reduced CF2 content are environmentally friendly.

We describe the development of new triphenylsulfonium photoacid generators (TPS PAGs) with semifluorinated sulfonate anions containing glucose or other natural product groups, and their successful application to patterning sub-100 nm features using 193 nm and EUV lithography. The TPS PAGs with functionalized octafluoro-3-oxapentanesulfonate were synthesized efficiently in high purity and high yield by utilizing simple and unique chemistries on 5-iodooctafluoro-3-oxapentanesulfonyl fluoride. In particular, a glucose unit has been chosen expecting that the naturally occurring material would improve both PAG miscibility with resist polymers and help the biodegradation mechanism in the wastewater treatment process, rendering bioaccumulation no longer a serious problem. A monosaccharide-based “Sweet” PAG has been fully evaluated in terms of chemical properties, lithographic performance, environmental friendliness or toxicological impact. The Sweet PAG shows quite sensitive and demonstrates lower LER values for 90 nm (1:1) dense lines than TPS PFOS. The Sweet PAG is non-toxic and it is susceptible to chemical degradation and to microbial attack under aerobic/anaerobic conditions. The chemical and microbial degradation potential of other new PAGs is being evaluated. Glucose or other natural units in the PAG structure assist in bio-degradation processes, which result in decreased accumulation of waste PAG in the ecosystem. These new PAGs are very attractive materials for high resolution photoresist applications and they are particularly useful in addressing the environmental concerns caused by PFOS and other perfluoroalkyl surfactants and the challenges raised by 193 nm and EUV lithography.

7972-82, Poster Session

Synthesis and photo-initiated polymerization of silicon-containing hybrid monomers

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Vinyl-ether derivatives have been widely investigated in the literatures as the main components of UV-nanoimprint resist. The vinyl ether compounds, which are cationic polymerizable monomers, are oxygen insensitive, and have some benefits for imprinting maintaining a low viscosity and short photocuring time. However, water or other impurities may effect the cationic polymerization. Meanwhile the photoinitiated radical polymerization of allyl ethers has a very high reaction rate, but they are somewhat viscous and reactive oxygen air. In addition, silicon-containing resists has high etching resistance.

A series of silicon-containing hybrid monomers which contained both vinyl ether group and allyl ether group had been synthesized. The monomers’ photopolymerization kinetics was investigated with real time FTIR. Results showed that the hybrid monomers could photopolymerize effectively and both free radical and cationic polymerization processes were improved. When PAG201 (a kind of cationic photoinitiator) was introduced into the monomers, the conversion of vinyl ether double bond increased sharply. The final conversion was close to 100%, and at the 6 sec, the polymerization achieved maximum. At the same time, the allyl ether double bond left. When 2-methyl-4’-(methylthio)-2-morpholino-propiopheno (907, a kind of radical photoinitiator) was introduced into hybrid system containing PAG201, the final conversion of allyl ether double bond and polymerization rate (Rp) increased obviously. It was demonstrated that the hybrid silicon-containing monomers polymerized rapidly and completely with both of the free radical and cationic photoinitiators. The The property showed that the five monomers can be used for nanoimprint resist.

7972-83, Poster Session

Development of hard mask-resist materials in nanoimprint lithography

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Hard mask type resist material and the lithographic process are investigated to achieve low volumetric shrinkage in ultraviolet curing nanoimprint lithography. This procedure is proven to be suitable for resist material design in the process conditions of ultraviolet curing nanoimprint lithography. The developed inorganic resist material with UV crosslinking groups produces high-quality nanoimprint images. The distinctive bulky structure is considered to be effective for minimizing volumetric shrinkage of resist film during ultraviolet polymerization.

7972-84, Poster Session

Study on a few α-disulfone compounds as photo-acid generators

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It is well known that α-disulfone compounds can undergo rapid photolysis when exposed to light to give strong acids as photolytic reaction products. These compounds can be used as a new type of nonionic photoacid generators. In this work a few α-disulfone compounds with different substituents were prepared by a simple nitric acid oxidation of corresponding disufonylhydrazines which were prepared by the reaction of sulfonyl chloride and aqueous hydrazine.

Most of the compounds are soluble in common organic solvents for photoresists. The thermal decomposition temperatures of the compounds were detected to be above 180°C. The UV absorption spectra of the α-disulfone compounds were measured with the absorption peaks (max) around 250nm. Quantum yields of the photolysis of the disulphone compounds in solution were determined to be in the range of 0.2 - 0.6 with low pressure Hg lamp as exposure light source. The amounts of strong acids generated in the photolysis of the disulfone compounds were measured by using tetrabromophenol blue sodium salt as indicator.

The photoacids generated by the disulfone compounds can induce the quickly acidolysis of ester acetal polymers and become easily soluble in dilute aqueous base. So, two-component positive chemically amplified deep UV photoresists can be formed by ester acetal polymers and the disulfone PAGs.

7972-86, Poster Session

PAG-free chain scissioning resists for 193-nm immersion lithography that can be developed by aqueous base

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Interest in PAG-free chain scissioning resists has recently re-emerged in the past few years in a bid to tackle the issue of line edge roughness (LER). We have developed a series of polysulfone based chain scissioning resists designed for 193 nm immersion lithography, and do not require addition of PAG. A key design feature has been to include a controlled amount of absorbing units to dramatically increase the

propensity of the polymers to undergo chain scission which results in more sensitive resists. At the same time we have been able to maintain sufficient transparency to allow light to penetrate through the entire film.

Typically, chain scissioning resists have required organic solvents as developers. However, we have developed a series of resist polymers that are able to be developed by aqueous base developers following irradiation. This has been achieved by engineering the repeat units such that a polarity of the A number of the systems have been imaged via 193 nm interference lithography and also via e-beam lithography. Certain formulations exhibit sensitivities that are approaching chemically amplified resists. Interestingly, certain formulations have been shown to exhibit good imaging performance upon overdose, where significant CD shrinkage was observed and may be useful in double patterning strategies. Finally, the effects of various factors, such as polymer structure, PEB and developer on LER have also been investigated for the non-CAR systems.

7972-87, Poster Session

Comparison of new thick negative resist to SU-8

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This work reports on recent advances in microfabrication process technology for medium to high-aspect ratio structures realised by UV photolithography using different kinds of photoresists. The resulting structures were used as molds and will be translated into metallic structures by electroplating. We compared 2 types of photoresists: SU8 epoxy based (negative) and Intervia BPN acrylate based photoresist (negative). The motivation for this work was to find an alternative to SU-8 photoresist, which is difficult to process and remove after electroplating. The results presented in this paper will open up new possibilities for low-cost processes using electroplating for MEMS applications.

Up till now, the well known SU8 negative photoresist, has been extensively used in many applications because of its outstanding high aspect-ratio structures. However, its major disadvantages are: its mechanical stress which leads to adhesion problems and its stripping difficulties after processing without damaging the other present structures or materials like copper, silicon oxide...

Intervia BPN photoresist was developed to bump electroforming for interconnection applications. It was dedicated to these applications because the supplier announces an aspect ratio of 2:1, inappropriate for MEMS applications. So we have investigated its process steps in order to increase its capabilities. The most interesting one is the relaxation time after exposure, before development. After optimization, we gained in resolution to achieve an aspect ratio of 8:1 with vertical sidewalls. One of the advantages of Intervia BPN photoresist is that it can easily be stripped after electroplating using commercially available solvent based etchant. The stripping process, performed at low temperature (< 100°C), is a major advantage compared to the SU8. Another advantage of Intervia BPN is its low mechanical stress (< 3 MPa) which minimizes significantly the delaminating effects.

The Intervia BPN photoresist process was optimized for 3 thicknesses (27 µm, 90 µm and 160 µm) with various seed layers like gold and copper. The results are completely comparable to SU8 ones in the UV area. The processing steps, includes spin coating, pre bake, insulation and development, are similar to the SU8's. The main differences lie in the addition of a relaxation time for Intervia BPN photoresist and the need of 3 bakes (Soft and hard) for SU8 processing.

With Intervia BPN photoresist, we have realized copper coils of 160 µm thick and 20 µm width or laminate magnetic core of 90µm thick and 15µm width on lines of 3mm length. The mold and the seed layer were etched without damaging the metallic structures. The need to etch the seed layer makes the Intervia BPN a suitable photoresist compared to the SU8 which is difficult to strip.

With similar results and lower price (four times less expensive), the Intervia BPN can replace the SU8 in various applications.

7972-88, Poster Session

Advanced implant resist for profile control

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For the 32-nm node and beyond, different film schemes and structures are used for device yield improvement. However, the reflectivity may vary at different areas. This can produce resist profile changes. In the shallow trench isolation (STI) process, the isolation oxide is deposited in the silicon trenches. If the resist edge is located on the STI area, the strong interference of reflections from the walls of the trench causes severe undercut resist profile. Such undercut profile will impact the implant fidelity. An additional BARC may be used to reduce this effect but it involves additional cost as well as changes in the etching process and in the implant diffusion profile.

In this paper, we present a new design concept of introducing different phase separation materials to compensate for the optical interference effect. We have studied different material loadings at the resist top and bottom to see their influence to the profile. With the help of floatable PAG, we can lower the PAG loading at the resist bottom area to compensate for the undercut profile. Moreover, higher dye loading in the resist bottom area also reduces the undercut profile without degrading resolution. The image and profile from the new formulation will be provided and discussed on its effectiveness to control the profile undercut or footing.

7972-89, Poster Session

Tailorable BARC system to provide optimum solutions for various substrates in immersion lithography

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It is common knowledge that the semiconductor industry continues to shrink the features contained in integrated circuits to increase speed and density. Each time the critical dimension (CD) shrinks, new challenges arise to impede the progress to attain smaller feature sizes. Control over surface reflectivity becomes even more important. Single-layer bottom anti-reflective coatings (BARCs) have been used in photolithography processes for years to reduce substrate reflectance, thus reducing or eliminating CD swing, reflective notching, and standing waves. Continued use of this solution is highly advantageous because it is well-known and cost-effective. This paper will describe a cutting-edge BARC system that has tailorable optical constants designed specifically to greatly improve immersion lithography process latitude. This BARC system can be easily modified to make formulations that match the many different substrates that are being used in new devices, including highly absorbing substrates (nitrides), reflective substrates (oxide), metal layers, and hardmasks. The optimum optical parameters for this BARC system can be easily achieved through simulations. This paper will exhibit the correlation between optical simulations and lithography results.

7972-90, Poster Session

Using positive photomasks to pattern SU-8 masking layers for fabricating inverse MEMS structures

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Photolithography is an iterative process used to transfer patterns from a photomask design layer onto a photosensitive material or

photoresist. Once transferred into the photo resist, the pattern is then developed and "windows" to the underlying material are opened up. The underlying materials are then etched leaving behind a permanent pattern in the lower material. When fabricating surface micromachined microelectromechanical systems (MEMS) devices, thin film depositions are interlaced with photolithography, etching and lift-off processing steps. Typically positive photomasks and positive photoresists are used in MEMS fabrication to ensure fine resolution and precise minimum feature sizes. Sometimes, however, reverse field or complementary mechanical structures are needed which necessitates using a combination of bulk micromachining, aggressive etching chemistries and robust masking materials.

When these situations arise, the ability to use a positive photomask with a negative photoresist is helpful to avoid fabrication delays. In addition, certain negative photoresists (i.e. MicroChem's NanoTM SU-8) are desirable because when hard baked they become chemically and thermally resistant and stand up very well to aggressive etching profiles (i.e. SF6 when isotropically etching Si) needed for bulk micromachining. This paper discusses a novel processing technique for that uses a combination of negative and positive photoresists for use with positive masks resulting in masking layers suitable for bulk micromaching. Specifically, SU-8 and Clariant's image reversal photoreist, AZ 5214E are used, along with a barrier layer, to effectively convert a positive photomask into a negative photomask. The barrier layer is required to avoid exposing the lower negative photoresist during the flood exposure step which is required for image reversal of the AZ 5214E. This novel process was recently used to etch micromachined trenches into a ZnO film located between the interdigitated (IDT) fingers of a surface micromachined surface acoustic wave (SAW) sensor. The etched trenches were incorporated into the device to increase performance by increasing device sensitivity.

7972-91, Poster Session

Negative photo-imageable spin-on dielectrics: report on progress, challenges, and opportunities

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From the perspectives of IC fabrication simplification, cost reduction, and waste material cutback, it is highly desirable to combine the traditional pattern formation step (lithographical processes) and the pattern transfer step (etch processes) into a single step. Photoimageable spin-on dielectrics (PSOD) render it possible to achieve the aforementioned goal. However, the bestowed dual functionalities on PSOD put great challenges on the material design and development. PSOD needs not only to match all the performances of the advanced resists, but also to undertake all the duties of the dielectrics on the chips. We wish to report our modular approach employing Si-containing materials to address the challenge and to meet the requirements from the different material roles. This paper will also discuss the investigation and progress on lithographic performance, cure behaviors, thermal stability, and electrical and mechanical properties.

7972-92, Poster Session

Performance of trilayer process required for 22 nm and beyond

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Silicon-containing antireflection coating (SiARC) and spin-on carbon (SOC) under-layers have been widely implemented for advanced semiconductor manufacturing since the 45nm node. The combination of SiARC and SOC promises a superior solution for reflection control and a high etch selectivity. Both SiARC and SOC films work as bottom anti-reflection layers for the photo-resist during exposure. The exposure light passes the photo-resist and is absorbed by the SiARC and SOC films before reaching the substrate. This dual antireflection layer is believed to be particularly effective for hyper NA immersion exposures, where less than 1% reflectivity is desired at all incident angles from zero to near arcsin(nwater/nresist) for the purpose of profile and CD control. The pattern transfer occurs via plasma etch with different chemistries. Fluorine plasma is used to transfer the resist pattern into the SiARC, then, the patterns in SiARC is transferred to SOC by switching to oxygen plasma. Finally, the SOC pattern works as a hard mask for substrate etch. In this paper, we report comprehensive evaluation results of the Silicon-containing ARC (with high Silicon content) and carbon under-layer from manufacturing perspective. It focuses on the performances that are required to extend the tri-layer applications from the original 45nm nodes to 22nm and beyond, such as thickness selection, etch selectivity, resist compatibility, rework capability, and under-layer pattern wiggling issues.

7972-93, Poster Session

Regeneration of imprint molds using vacuum ultraviolet light

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Imprint-lithography is expected to become one of the next-generation nano-lithography techniques1-3. Repeatedly-used imprint-molds should be cleaned for the next series of imprint-lithography process. It is, however, that the cleaning method of the imprint-molds is left unsolved. Vacuum ultraviolet (VUV) light is here adopted from the points of cleaning effectiveness and ecological technique. Cleaning mechanism of the VUV light consists of two steps; the first is decomposition of organic materials (CxHyOz) with chemical bond dissociation energy of h , and the second is oxidation by a singlet-oxygen. Therefore, the cleaning by VUV is more than ten-times effective than that by ultraviolet (UV) light.

A cleaning machine equipped with Xe* excimer type lamp, which is made by ushio inc.,4 and which emits the light with wavelength of 172nm and power of 10 mw/cm2, has been originally developed. Four kinds of resins such as TR-21B for UV-imprint, PMMA for thermal-imprint, ZEP for electron-beam lithography, and AZ1500 for photolithography are used to measure the ashing characteristics. Two kinds of imprint-molds such as SiC for thermal-imprint and quartz for UV-imprint are used to examine the cleaning behaviors.

In order to investigate the effectivity of the developed VUV-exposure machine, ashing rates of four resins have been examined. They are 3.2, 9.2, 17.0, and 29.4 nm/min for AZ1500, ZEP, TR-21B, and PMMA, respectively, under the substrate temperature of 25 . The substance order of ashing rate is same as the well-known case of UV-ozone ashing, however, their ashig rates are 5-10 times higher. The higher substrate temperature is, the more effective ashing process becomes. Figure 1 shows the dependence of VUV-exposure distance, dRD on the amount of thickness loss(= ashing amount) for ZEP. VUV-exposure time is 4 min. The less dRD is, the more VUV reaches to the sample surface, and the more amount of thickness loss becomes, because the singlet-oxygen generated in the vicinity of sample surface decomposes resins efficiently. The amount of attainable VUV to the sample surface is influenced by the ambient oxygen concentration.

Figure 2 shows the cleaning result of quartz mold, which contains attached UV resin, TR-21B. The quartz consists of 150-300 nm L&S patterns with depth of ca. 250 nm 5. The UV-imprint resin is difficult to remove from the quartz-mold by using organic solvents, such as acetone and alcohol, which are generally used to wash out various resins. Figure 2(A), (B), and (C) show pictures of optical microscope taken before VUV exposure, and after 5 and 10 minutes exposure, respectively. Strongly attached UV-imprint resins are removed by 5 minutes VUV-exposure, and residual UV resins in the grooves are completely removed from the quartz-mold as shown in fig. 2(C).

The cleaning treatment of contaminated resins on the concavoconvex-substrates by exposure of vacuum ultraviolet (VUV) proves very effective

not only for the imprint resins but also for various resins. Effective ashing of resins is induced by long time-, high substrate temperature-, and short distance-vuv exposure. The cleaning procedures for imprint-molds is successfully established.

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7972-94, Poster Session

Plasma etching of high-resolution features in a fullerene molecular resist

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Aspect ratio related pattern collapse of dense resist patterns limits photoresist film thickness to less than 3 times minimum feature size. Given typical resist to silicon selectivity during plasma etching it is thus becoming difficult to transfer high-resolution patterns with useful aspect ratio by directly etching the resist. It has become increasingly common to use photoresist to pattern an intermediate hardmask, which is then used to mask the silicon during etching, adding process complexity. We have previously described a fullerene based resist capable of 20 nm halfpitch in e-beam lithography with a sensitivity of <10 µC/cm^2 at 20 keV. The etch durability of this resist is comparable to other high durability materials such as novolacs, using ECR etching with SF_6. [1] Here we present a detailed study of the ICP plasma etching capabilities of this new resist, in particular focusing of the successful transfer of high-resolution patterns.

Line-space patterns with a range of half-pitches from 25 nm to 100 nm were produced in 30 nm thick resist films using e-beam lithography. An Oxford Instruments PlasmaPro NGP80 inductively coupled plasma (ICP) etcher was used to perform plasma etching. The etching process employed a carbon/fluorine etch chemistry using mixtures of SF_6 and CF_4 as etchants and CHF_3 or C_4F_8 as passivating gases. Etch selectivity and anisotropy were studied as a range of etching parameters were varied. Figure 1 shows the selectivity achieved as ICP power was varied for two different etchant mixtures. It can be seen that the three gas SF_6/CHF_3/CF_4 process improves the selectivity in this case. Figure 2 shows (a) dense and (b) sparse features transferred from 30 nm resist films with selectivities of 2.2 and 5.1 respectively, using SF_6/C_4F_8 ((a) 20/30; (b) 30/30 sccm) etchant, with an RF power of 20 W, ICP power of 180 W and pressure 15 mT. A particular problem seen when etching dense high resolution features is aspect ratio dependant etching (ARDE), where the etch rate between dense features is reduced. Figure 3(a) shows a dense resist pattern. Etching with SF_6/C_4F_8 (25/30sccm) RF/ICP (W) 20/220 W, pressure 15 mT, leads to well defined features but with substantial footing, figure 3(b). A 2 second O_2 ash prior to etching removes the footing, but ARDE is still present, figure 3(c). Maintaining the O_2 ash, and increasing the SF_6/C_4F_8 plasma pressure to 30 mT decreases the ARDE.

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7972-95, Poster Session

Method of ellipsometric characterization of the resist and DBARC interface

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Anti-reflective layers benefit CD and profile control in high resolution lithography. Anti-reflective layers benefit CD and profile control in high resolution lithography. Traditionally, they have not been applied to implant levels because the required CD control was less stringent than for other layers. When present a traditional BARC film interferes with the doping process unless removed using a costly dry BARC open etch. Nevertheless, as implant features move to evermore challenging k1 values, reflection control becomes more unavoidable; firstly to control residual standing wave structures on the resist profile and secondly to maintain acceptable CD dimensions on substrates which exhibit large reflectivity variations at both the cross-wafer and the wafer-to-wafer level.

An important consideration for this application is to monitor and minimize intermixing between the resist and DBARC layers. Any method to do so must be sensitive to to layers less than 10 nm thickness. The use of ellipsometry is investigated in this work to show the degree to which intermixing, if any, is detectable. A method and its requirements are described that predicts intermixing down to Angstrom thickness. Cross-section SEM shows the effect from intermixing and from an optimized process (no intermixing).

7972-97, Poster Session

Process optimization of high-aspect ratio sub-32-nm HSQ/AR3 bilayer resist pillar

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New non-volatile memory, like RRAM, needs resist pillar pattern to act as etch mask for cell pillar definition [1]. The etched stacking film thickness of cell pillar is not easy to reduce below 50 nm for tolerating CMP process integration during CD scaling down. Sub-32 nm single layer resist (SLR) pillar pattern of aspect ratio (AR) < 1 is not thick enough for etching such thickness but will collapse for AR > 1.5 during wet development process. Bilayer resist (BLR) process is most suitable for forming high AR pattern. Dry develop process is the key step for generating sub-32 nm high AR BLR pillar pattern. O2, N2 and Ar gas flow rates, chamber pressure, top power and bottom power of dry etching chamber are the process parameters to be studied in detail. In this study upper thin imaging layer is hydrogen silsesquioxane (HSQ) for e-beam exposure while the thick underlayer for etching resistant is AR3-600. Optimization of dry develop process is investigated for obtaining pillar with highest AR.

Experimental results are summarized below. Highest AR of ~6 for HSQ/AR3 BLR semi-dense L/S=1/2 pillar with vertical profile is obtained under optimized dry develop condition of O2, N2, Ar flow rates, chamber pressure, top and bottom power of 8, 5, 0 sccm, 1 mTorr, 200 and 100 watts respectively. AR is lower for looser pattern density. Smaller pillar CD after dry develop corresponds to smaller designed CD in e-beam exposure. The most critical process parameters for obtaining high aspect ratio BLR pillar are O2 flow rate and top power. Sidewall profile angle of pillar is mainly dependent on chamber pressure and bottom power.

In summary, optimized dry develop process condition for high aspect ratio HSQ/AR3 BLR sub-32 nm pillar with vertical profile is obtained.

7972-98, Poster Session

The enhanced photoresist shrink process technique toward 22-nm node

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1, Introduction

In fine patterning process technology, not only the pitch shrink but also the pattern shrink process technique is indispensable. Up to now, TEL has been proving the application for the trench pattern shrink for dual trench LELE, the simple hole shrink for the contact layer, and the oval hole pattern shrink for cut mask of SADP. In this paper, it introduces the technology that can do the shrink of the photoresist as an application for a short trench pattern. The chemical shrink is assumed to be a reference as a relative comparison, and it reports on the effectiveness of the ALD SiO2 shrink of TEL's original process.

2, Experimental condition

We prepare the PR/ARC/hardmask/TEOS/Si structure. The controlled PR design consists of 100nm pitch of X direction and 192nm pitch of Y direction.

3, Summary

The 20nm order's short trench pattern is achieved by using ALD SiO2 shrink technique. The process of the shrink technique that TEL recommends shows an excellent performance for the fine patterning process. This is one of the promising shrink technologies now.

7972-99, Poster Session

Extend lithographic process limitation by shrink material

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Critical dimension and process margin are becoming big concerns in optical lithography beyond printing patterns of 45-nm half pitch, due to the limitation of NA and hyper NA of exposure tool. In this study, the shrink material that can effectively shrink the CD and extend process window with controllable isolate-dense bias was intensively studied with novel immersion lithography process. The shrinkage, shrinkage linearity, and shrinkage bias were considerably relied on mixing bake temperature. The shrink material, AZ® SH114A has demonstrated several attractive advantages, which are able to improve LWS, LER, sidewall roughness of contact holes, surface roughness, and side lobe. Moreover, we have successfully applied a novel shrink material for the patterning of sub-45nm contact hole and trench in the logic device.

7972-100, Poster Session

LWR reduction and flow of chemically amplified resist patterns during sub-millisecond heating

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Chemically amplified resists (CARs) are critical for sub-30 nm photolithography. As feature sizes decrease, challenges continue to arise in controlling the aerial image during exposure, acid diffusion during post exposure bakes (PEB), and swelling during development. Ultimately these processes limit the line width roughness (LWR), which the ITRS suggests must be reduced to <2 nm (3) by 2015. While there exists substantial research to modify resists and exposure protocols, post-development treatment of resist patterns to improve the LWR has received only modest attention.

In this work, we use a scanned laser spike annealing system (LSA) to anneal fully developed resist patterns at temperatures of 200-400 ^{o}C for sub-millisecond time-frames. We hypothesize that a patterned resist, heated above its glass transition for a controlled time, will flow to minimize the surface energy resulting in reduced line edge roughness. LSA, initially developed for shallow junction annealing following ion implantation, utilizes a scanned line-focused laser to heat the surface to a controlled temperature (up to ~1400 ^{o}C) followed by a rapid thermal quench into the bulk substrate as the laser source passes. The profile of the anneal can be controlled by the beam shape and scan speeds with heating durations between 100 µs and ~2 ms. In this ultra-short time regime, thermal damage or decomposition of the resist can be avoided while enabling the short range flow and reorganization of the polymer chains required for LWR reduction.

Changes in LWR profiles from several CARs have been investigated using conventional EUV lithography (EUVL) followed by laser heating. Figure 1 shows SEM images of 30 nm half-pitch lines before and after laser annealing at 22W (~200 ^{o}C) for 500 µs. Dramatic smoothing (reduced LWR) of the lines is immediately evident and likely a direct consequence of resist flow at temperatures above T_g. In Fig. 2, the CD and LWR are shown as a function of the incident laser power. A 1-2 nm shrinkage in CD is observed with increasing laser power (Fig. 2a) above an initial threshold (~13W or 130 ^{o}C), persisting until the resist begins to flow extensively at high laser powers (>28W or ~320 ^{o}C). Over the same laser power range, the LWR is reduced by almost 2 nm (Fig. 2b) from ~6 nm immediately after development to <4 nm after processing with LSA. Characterization of LWR reduction for different CARs and quantitative models to explain the behavior will be presented.

7972-101, Poster Session

Critical challenges for "non-critical" layers

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Historically, the block layers were considered "non critical layers". However, continuous scaling has brought these layers to a point, where resolution, tolerance and aspect ratio issues of the block masks now present significant challenges. Some of these challenges will be discussed in our talk.

In recent bulk technology nodes technology, the deep well implants require an aspect ratio of up to 5:1 in conventional resist leading to small process margin for line collapse and/or residue. New integration schemes need to be devised to alleviate this high aspect ratio, i.e. like scaling down the energy of the implant and the STI deep trench to reduce resist thickness, or new hard mask solutions with high stopping power to be dry etched.

Underlying topography creates severe substrate reflectivity issues that affect CD, tolerance, profiles and defectivity. In addition of the CD offset due to the substrate, the implant process induces CD shrinkage and resists profile degradation that affects the devices. Similarly, large challenges are posed by the wet etch levels with reduced ground rules - there adhesion of the small resist structures is compromised by aggressive wet etch treatments post litho. Minimizing these effects is paramount for controlling implant level processes and meeting overall technology requirements.

In summary, the "non-critical" layers will require the development of more complex processes and integration schemes to be able to support the coming technologies. We will characterize these process constraints, and offer some process / integration solutions for scaling from the 28nm to 20 nm node.

7972-102, Poster Session

SUEX process optimization for ultra-thick high-aspect ratio LIGA imaging

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The focus of this presentation is on the use of SUEX Thick Dry Film Sheet (TDFS) laminates which DJ DevCorp is developing as a thick resist material in optical and X-ray lithography. Preliminary thick dry film sheets up to 1mm thickness were successfully prepared and patterned at the CAMD X-ray beamlines and presented at HARMST 2007. Recently, new results have been published using SUEX resist sheets in UV lithography showing great market potential including plating molds for metal microparts, polymer MEMS, multilayer microfluidics structures, BioMEMS, medical devices, wafer level packaging processes, and displays. The SUEX TDFS are available in a range of thicknesses from 100µm to 1mm or more and are pre-cut into a number of standard wafer sizes.

This new material is a modified epoxy formulation containing an antimony-free photo acid generator (PAG) prepared under a highly controlled solvent-less process which provides uniform coatings between two throw-away layers of protective polyester film. As part of our initial studies resist layers of 250, 500 and 1000µm were laminated onto regular silicon wafers using a hot roll laminator at a speed of 1ft/min at 75°C. The entire substrate preparation takes about 1 hour and with practice users can prepare up to 10 substrates in this time which are typically ready to use within 2 hours.

In our efforts to develop a commercially viable product we have conducted experiments using standard equipment available at CAMD (Quintel UV aligner and CAMD XRLM 4 beamline). Initial X-ray exposure tests were done with a bottom dose ranging between 100 and 400 J/cm3 and a top/bottom dose ratio of less than 2 for sheets up to 2mm in thickness. Exposure time for typical conditions of the CAMD storage ring (ring current ranging between 100 and 160mA) is about 10-15min for a 4' wafer. After exposure the samples were immediately post exposure baked to 110°C using a convection oven, taken out and cooled to RT then relaxed up to 3 days before development to reduce stress. Development was done in PGMEA for up to 2 hours for the 1000µm thick samples followed by a short IPA rinse and drying in air.

Very high aspect ratios of 100 or more have been routinely patterned with nearly perfectly straight sidewalls (~1µm deviation for a 1mm tall structure) and excellent image fidelity.

7972-103, Poster Session

E-beam patterning and stability study of sub-22-nm HSQ pillars

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E-beam exposed HSQ resist pillar (island) is used as the mask for transferring pattern during dry etching. However, HSQ pillar is prone to collapse without any pre-treatment of substrate. CD resolution of HSQ pattern also depends on shelf life (aging effect) [1]. In this work, (1) designed CD (DCD) effect (2) dose vs L/S ratio (3) beam current dependence (4) underlayer effect (5) post-coat-delay (PCD) time before e-beam writing are studied for forming stable and reproducible sub-22 nm HSQ pillar. Three kinds of underlayer are evaluated, i.e. AR3-600, ZEP520A and TDUR-N700.

Experimental results are summarized below. A wider dose window of forming sub-22 nm HSQ pillar with looser L/S ratios is obtained. The dose window of sub-22nm pillar resolution with smaller designed CD is broader with higher center dose. CD variation for various L/S ratios and designed CDs exposed with different e-beam currents is due to the proximity effect from beam blur. AR3-600 is shown to be the most suitable underlayer for HSQ pillar. CD of HSQ pillar increases with thicker AR3-600 layer. PCD time range for obtaining stable CDs of HSQ pillar with designed CD of 20 nm is larger than that with 15 nm.

In summary e-beam patterning of sub-22 nm HSQ pillar is demonstrated. Underlayer below HSQ is most critical in forming stable HSQ pillar without position drift, aggregation or collapse. PCD time range with lowest CD fluctuation is a limiting factor for repeatable HSQ pillar patterning.

7972-104, Poster Session

A study of an acid-induced defect on chemically amplified photoresist applied to sub-30-nm NAND flash memory

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Recently, we found a peculiar acid induced defect on chemically amplified photo resist applied to sub-30nm NAND Flash Memory. This defect is like a hole pattern with about 1um diameter, and induced by diffusion of acid which makes photoresist soluble in developer, even though photoresist is not exposed with KrF. With some experiment results, we found out that HCl gas, by-product of high temperature oxide which is contained inside voids between two gate lines diffuses into photoresist through high temperature oxide from voids, makes photoresist soluble in developer, and eventually creates the hole-type defect on photoresist. To prevent this defect, we can suggest some methods which are substitution of KrF photoresist into I-line photoresist, modification of oxide deposition recipe to suppress by-product, and applying of Non-CAR (Chemically Amplification Resist) type KrF photoresist not sensitive to acid.

7972-105, Poster Session

Investigation of processing performance and requirements for next-generation lithography cluster tools

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As a continuation of TEL and ASML's commitment to lithographic process development on consistently reducing patterning feature sizes, this work is the summary of investigations into processing capability and requirements as evaluated on the LITHIUS ProTM -i / TWINSCANTM NXT 1950. Process performance with regards to critical dimension uniformity (CDU) and defectivity are investigated to confirm adherence to ITRS roadmaps specifications. Additionally, a study of backside particle contamination is performed to understand implications toward processing. As chuck cleaning on the scanner will require considerable down time, this study is critical to understanding requirements for manufacturability.

Previous work from this collaboration succeeded in a processing improvement of over 80% reduction in CDU by implementation of the newest PEB plate design and optimized developer process. With regards to defectivity, the use of the advanced defect reduction process with an optimized bevel cut of the resist allowed for the high contact angle process required for optimal immersion hood performance. In this work, further optimization of the process with consideration of the design concept of the NXT and hardware modifications on the LITHIUS ProTM -i will be performed. From this investigation, it is expected to understand the process capability of 38nm CDU using novel developer hardware. Additionally, the defectivity challenges for processing with higher scanspeeds in combination with the hydrophobicity of the coating materials and edge cut strategy will be clarified. Initial evaluation results are analyzed to understand the correlation of various types and densities of contaminates on the backside of the wafer to the formation of chuck hot spots.

7972-106, Poster Session

Characterization of filter performance on contact-hole defectivity

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The effect of filtration on defectivity has been studied extensively with line-space patterns. However, the ability to have defect free contacts is equally as important. Resist materials are specifically designed for contact holes, and therefore it is important to also study their varied sources of defectivity.

In this study, bare and patterned wafer defectivities have been studied as a function of point of use filter. The filter retention rating was held constant at 10nm while the filter membrane material was varied, including ultra-high molecular weight polyethylene (UPE), polyamide, and composite filters. A recommendation will be made as to which point-of-use filter performed best with the contact hole specific resists tested.

7972-108, Poster Session

Filter priming effects on bottom anti-reflective coating defects

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As semiconductor devices continue their never-ending march to become smaller, cheaper, and faster, more materials are needed to ensure success. In the photolithography sector, device level-specific organic Bottom Anti-Reflective Coatings (BARC) or photoresists are being tuned for certain imaging requirements, such as numerical aperture, immersion conditions, and optical properties to suppress light reflections off the substrate. In order to test the new materials to determine their properties, there is a need to install the materials on a coater-track quickly and efficently. Installation of new materials typically requires a new filter be installed, the dispense lines cleaned, and a minimum of 8-10 L of material purged through the filter to clear out bubbles and other nuisance defects. Because materials vendors are increasing the number of experimental formulations, the timelines to test new materials become shortened and the need to faster startup is increased. Utilizing the Entegris IntelliGen® Mini dispense system, various filter priming processes were tested with the goal of minimizing the volume purged through the filter to reach baseline defectivity. In addition to studying filter priming technique, different filters were used to determine the effect of different membranes on filter priming. Results during this testing indicated that certain priming process could cause the defects to increase during the process, requiring the user to perform additional purging to achieve baseline, thus negating time and chemical savings. Optimized priming recipes, however, reduced the purging time and purging volume by 50-70%.

7972-110, Poster Session

Resist dispense system for further defect reduction

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As pattern size becomes smaller in lithography process, requirement of defect reduction is getting higher and higher. It is known that defects occur in various steps of lithography process. In this study, we focus on defects related to the resist supply system. Of those defects, the most typical is bridge defect. Bridge defect is caused by foreign substances contained in resist film. The source of those foreign substances is considered to be insoluble substances, such as resist gels, in resist solution. The conventional countermeasure has been the development of resist line filters (optimization of materials, shrinking of pore size, and so on). Not only filter type but also filtration condition has certain influence on bridge defect generation. In addition to bridge defect, micro-bubbles also require attention. Circular defects approximately 1 m in size are occasionally observed on resist film. Most of those defects are caused by micro-bubbles formed in resist solution. Pressure fluctuation in resist supply system may easily form bubbles. So that, a resist line filter with smaller pore size is concerned to increase the risk of micro-bubble generation, although such a filter is effective for reducing bridge defect. Those led us to start developing the new resist supply system to get the bridge defect consistent with the bubble defect.

In this study, we examine the influences of resist supply system structure and its parameters, focusing on bridge defect and micro-bubble defect. This paper provides the data obtained from the series of experiments and introduces our approaches to the optimization of resist supply system and its effects.

7972-30, Session 8

Analysis of resist patterns for material and process design: parameter extraction from dose pitch matrices of line-width and edge roughness and cross-sectional SEM images

T. Kozawa, Osaka Univ. (Japan); H. Oizumi, T. Itani, Semiconductor Leading Edge Technologies, Inc. (Japan); S. Tagawa, Osaka Univ. (Japan)

As the development status of extreme ultraviolet (EUV) lithography approaches the requirements for the high volume production of semiconductor devices with the minimum line width of 22 nm, the extraction technique of resist parameters becomes increasingly important from the viewpoint of the accurate evaluation of resist materials for resist screening and the accurate process simulation for process and mask design. In this study, we investigated the line-and-space resist patterns delineated using the third, fourth, and fifth Selete Standard Resists (SSR3, SSR4, and SSR5). The line-and-space patterns were fabricated using the small-field exposure tool (SFET) installed to Semiconductor Leading Edge Technologies, Inc. (Selete). SFET is an indispensable tool for the development of resist materials and processes for EUV lithography. By analyzing the dose-pitch matrices of line width and edge roughness (LER) and the cross-sectional SEM images of line-and-space patterns, the resist parameters (quencher concentration, acid diffusion constant, proportionality constant of line edge roughness, and dissolution point) were successfully extracted without the knowledge on the details of resist contents. The average error of reproducibility of line width and LER was 10% within the dose range of 8.0-12.0 mJ/cm2 and the half-pitch range of 22-60 nm.

7972-31, Session 8

Stochastic post-exposure bake kinetics of chemically amplified photoresists: a simulation study

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The kinetics of post-exposure bake (PEB) reaction and diffusion in chemically amplified resists plays an important role in determining the line-edge roughness (LER) of the final lithographic features. The diffusion of acid smoothes out high-frequency roughness with a correlation length related to the diffusion length. Diffusion, however, reduces the deprotection gradient, causing an increase in LER. As a result, an optimum acid diffusion length will give a minimum LER. Additionally, the role of quencher is known to be critical to the magnitude of LER. Higher amounts of quencher cause an increase in the uncertainty in the amount of deprotection taking place, but an even greater increase in the gradient of deprotection, resulting in an improvement in LER. Unfortunately, the complex interactions of acid diffusion, quencher loading, and quencher diffusion on LER has yet to be fully quantified.

In this paper, the stochastic resist model (SRM) in PROLITH X3.1 will be used to study the impact of acid and quencher amounts and diffusion on the relative uncertainty in deprotection due to stochastic effects. By varying the exposure dose for an open-frame exposure, the relative uncertainty in the level of protection remaining after PEB as a function of the mean level of protection will be simulated for varying amounts of quencher, and for differing diffusivities of both acid and quencher. These results will then be described by simple, approximate equations that provide analytical prediction of deblocking uncertainty. The result will be useful for optimizing resist formulations and processing for minimum LER.

7972-32, Session 8

Stochastic resist simulation of a negative tone development process

S. A. Robertson, KLA-Tencor Texas (United States); M. Reilly, Y. C. Bae, Dow Advanced Materials (United States)

Negative tone development (in solvent) of a nominally positive tone (in TMAH) photoresist has been shown to significantly improve process latitudes for several feature types (small single pass contact hole, semidense trenches etc.) and can allow double exposure techniques to form very small, low MEF contact holes.

SEM images often show a distinct difference in Line-edge-roughness (LER) for the same printed feature when the development tone is switched.

In this work we develop stochastic physical resist models for one immersion ArF chemically amplified photoresist developed in both positive and negative tone developers under otherwise identical process conditions (thickness, Softbake, PEB etc.). The stochastic model has previously been shown to a good predictor of LWR and CDU for positive tone ArF resist [1]. In this study, we will use the calibrated models to identify key sources in the differering LER behaviors.

Model calibration is a mixture of parameter fitting to experimental CD data and direct measurement of key physical parameters (Negative tone development rate is measured by optical DRM and threshold deprotection levels are measured via FTIR techniques).

Independent data under different optical conditions will be used to verify the predictive accuracy of the models obtained to the calibration data.

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7972-33, Session 8

Meso-scale simulation of the line-edge structure based on resist polymer molecules by negative-tone process

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Recently, we proposed the simulation method for the positive tone lithography process based on the meso-scale simulation of dissipative particle dynamics (DPD) method to study the problem of the line edge roughness in the unit of a resist polymer chain. In the positive tone process, the line edge can be described as the interface between soluble and insoluble polymer phases and the line edge was formed as aggregated structures of polymer chains near the line edge. On the other hand, in the negative tone process, the cross linking reaction occurs in the photo irradiated regions, and its region becomes insoluble. In this study, we proposed the simulation method for the negative tone lithography process based on our simulation technique in the positive tone process.

First we prepared the initial structure of resist film on the model of dissipative particle dynamics method. We treat the cross-linking reaction as a bond creation between polymer particles in the limited region. After the reaction, the cross linked polymer was obtained in the central region of the film. After the cross linking reaction, we performed the dissolution process simulation using the same interaction parameter between solvent and free or cross-linked polymers. As time goes on, free polymers dissolved into the solvent phase and the cross-linked polymer was swelling. The line edge after the dissolution of free polymer shown in yellow surface was roughened, though that was almost flat in the initial structure. Our simulation will inform you about the formation mechanism of the line edge in the negative tone process using polymer chains.

7972-34, Session 8

Resist line-edge roughness modeling for continuous space simulations

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Resist line edge roughness (LER) is generally regarded as noise inherent from multiple sources: the film coating, the exposure step, post-exposure bake, and aqueous development. Current state of art LER simulations attack the numerically challenging LER simulations at each step individually, by considering a wide range of variations that are relevant to the step, and by using a collection of stochastic, multi-scale numerical algorithms. With a high level of complexity involved, convergence and efficiency is often unacceptable for practical usage. Yet the largest road-block to industrial adoption is their incompatibility for plug-and-play with most standard commercial simulation packages.

This work proposes a straightforward but conceptually innovative modeling method that works around all current difficulties in LER simulations. By adding an appropriate amount of noise into the intermediate solutions or initial values, we are able to inject the desired process noise into a temporally sequential, transient system without modifying any existing models or solution methods. LER is therefore a natural consequence from solving the current step with randomness carried on from the previous step. The novelties of the work include:

1. Only two randomness parameters that need to be calibrated to the measured wafer LER data. This leads to higher modeling confidence.

2. High computational efficiency. This LER model can be seamlessly integrated into the current computational framework without jeopardizing any existing speed enhancement conditions or numerical algorithm improvements for current transient continuous systems.

3. Ready to be integrated into any current commercial photo process simulation programs.

7972-35, Session 8

Physical modeling of developable BARC at KrF

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Resist CDU and profile control in high-resolution lithography are improved with the use of spin-on bottom anti-reflective coatings (BARCs). Typically, BARCs have not been applied on implant levels because they interfere with the doping process and also because of the cost of performing a reactive-ion etching step to open the BARC in bright areas. As implant CDs shrink to challenging k1 values, reflection control is increasingly required. One solution is to use a reactive-soluble antireflection layer to control CD and profile, thus eliminating the need for an additional etch step. Developable bottom antireflective coatings (DBARCs) provide improved control while minimizing increased cost.

Computer simulation methods are a valuable tool for research and design. Complex reaction phenomena, often difficult to measure

experimentally, may be studied within the limits of the models used, and their effect upon the resulting lithography evaluated. In this work, we describe DBARC functionality and application. The physics of a computer model for the study of DBARC is discussed. The effect of the model parameters upon the simulated lithography is discussed. The model is calibrated to experimental data and model predictions are compared to data of resist profiles on DBARC for key features at KrF.

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7972-36, Session 9

Extendibility of EUV resists in the exposure wavelength from 13.5 down to 3.1 nm for next-generation lithography

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The increasing density of semiconductor devices has required the development of high resolution exposure techniques. Extreme Ultraviolet (EUV) Lithography at 13.5 nm exposure wavelength is expected to begin 2014-2015. The miniaturization of feature sizes has been achieved mainly by shortening the exposure wavelength. EUV lithography at 6.8 nm exposure wavelength based on experiments such as reflective multilayer optics at 6.7 nm[1] was proposed by ASML has been proposed for the extendibility of EUV down to sub 5 nm resolution[2].

Here the pattern formation reaction mechanisms of EUV resists have been investigated in the wavelength from 13.5 to down to 3.1 nm. Especially the sensitivities of EUV resists were investigated by EUV exposure to several resist materials in the exposure wavelength down to 3.1 nm.

The shortening of exposure wavelength means the increase in energy of exposure light. The energy of exposure lights exceeds the ionization potential of EUV resist materials. The knowledge base of resist reactions shifts from photochemistry to radiation chemistry. The first systematic research on details of reaction mechanisms of EB and X-ray resist materials was carried out by pulse radiolysis [3]. Radiation mechanism of chemically amplified resists was first proposed based on pulse radiolysis experiment of a model solution of chemically amplified resists [4]. The detailed mechanism of radiation chemistry of chemically amplified resists based on both product analysis and pulse radiolysis was done in 2000 [5]. The systematic research on the details of reaction mechanisms on EUV chemically amplified resists at 13.5 nm exposure wavelength has been done. A number of papers on radiation chemistry of EUV resists at 13.5 nm have been published and recently reviewed [6]. Here the dependence of the exposure wavelength on reaction mechanisms of chemically amplified EUV resists in the wavelength from 13.5 down to 3.1 nm has been investigated. Especially the sensitivities of several kinds of typical resists were investigated experimentally in EUV wavelength down to 3.1 nm. The experimental results and theoretical prediction agree quite well with each other. The sensitivities of resist materials were roughly proportional to absorbed dose calculated by line absorption coefficients of resists. The details of the dependence of the exposure wavelength on EUV resist performance in the exposure wavelength from 13.5 nm to 3.1 nm will be explained in the conference.

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7972-37, Session 9

Underlayer physical properties and their effects on the lithographic performance of extreme-ultraviolet photoresists

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In EUV lithography, the initial conclusion was that antireflective coatings (ARCs) were not required because the reflectivity of silicon surfaces at 13.5 nm was minimal. However, combining DUV ARCs with EUV resists has been shown to improve lithographic imaging. Although some explanations have been advanced to explain this improved lithographic performance, the fundamental principles behind understanding the experimental results have not yet been proposed.

We will present the effect of water contact angle (WCA) and coefficient of thermal expansion (CTE) of the underlayer. We lithographically evaluate multiple sets of CNSE organic underlayers and commercial hardmasks specifically designed with variations WCA and CTE. Resist adhesion and line-edge roughness performance was correlated to underlayer physical properties to better understand the interactions between thin resist and underlayer films. Explicit details of both organic underlayer and resist formulations are disclosed. Additionally, we further explored the development of low CTE organic underlayer systems through variations in underlayer formulation and evaluated their ability to support high resolution imaging with good adhesion performance.

A correlation between resist adhesion and underlayer coefficient of thermal expansion was observed (Figure 1A). Significant improvement in resist line-edge roughness was also achieved through the use of underlayers when compared to a primed silicon substrate (Figure 1B).

7972-38, Session 9

EUV underlayer materials for 22-nm HP and beyond

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EUV lithography is expected to be an important technology for manufacturing 22 nm node and beyond in semiconductor industry. To achieve the desired resist RLS performances for such fine feature patterns, multilayer materials are almost certainly needed to define the overall lithography process. In this paper, we report the studies of new EUV underlayers (EBL) based on new crosslinkable organic underlayer materials. The lithography results have demonstrated advantages over conventional organic underlayer in terms of resist sensitivity, resolution, process window, pattern profile, collapse margin, and possibly line width roughness

7972-39, Session 10

Impact of post-litho LWR smoothing processes on the post-etch patterning result

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In the last years, interest in reducing line width roughness (LWR) in EUV

lithography through a dedicated process step has significantly increased. Various post-litho processing techniques to improve LWR without compromising resolution or sensitivity have been proposed [1]. While these techniques are giving smoothing levels up to 30% before etch, the important question is of course how efficient they are in the full patterning process.

To evaluate the effectiveness of the smoothing techniques on the post-etch pattern, a few of the most promising techniques have been selected for an evaluation on a fully optimized EUV patterning process. Analysis of LWR in the frequency domain [2] at the different stages of the patterning process gives a better insight into the impact of the different steps. It becomes clear that LWR reduction by the post-litho processes and the etch transfer process are not simply additive, yet display a distinct, partly overlapping fingerprint in the LWR frequency domain.

This analysis will give a better insight in the effectiveness of the different smoothing techniques and could potentially indicate new pathways to effectively reduce the roughness of the final pattern.

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7972-40, Session 10

Developable BARC (DBARC) technology as a solution to today's implant lithographic challenges

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Lithographic patterning on implant layers is now proving to be among some of the most challenging imaging steps in advanced IC manufacture. For example, many implant layers are characterized as having significant topography e.g., post gate level and also variable substrate types (silicon, oxide and nitride) leading to reflectivity and in some cases potential poisoning issues thereby making lithography particularly challenging.

Up until recently, device makers were able to pattern such layers using a dyed KrF photoresist on silicon or more commonly a dyed KrF photoresist with TARC. These approaches offer limited reflectivity control and as result there is a concern that these approaches may no longer satisfy industry requirements as ground rules shrink.

In this paper, we describe our results in evaluating an alternative approach to implant lithography based on developable antireflective coatings (DBARC's). In this study, we evaluate both KrF and ArF DBARC technology with emphasis on post gate levels where topography poses a significant challenge. Our DBARC approach is benchmarked against the incumbent TARC solution using the following criteria: profile integrity, CD Bias, CDU and defectivity. Furthermore, we evaluate the applicability of our DBARC solution to device integration by checking electrical performance on several implant levels.

7972-41, Session 10

193-nm resist chemical modification induced by HBr cure plasma treatment: a TD-GC/MS outgassing study

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HBr plasma treatment offers promising capabilities to improve 193nm photoresist (PR) chemical and physical properties. It was originally introduced to increase 193nm PR etch resistance during plasma processes following the lithography step and also to decrease the resist pattern linewidth roughness [1]. Moreover, it shows remarkable potential for double patterning strategies, either for the litho-litho etch (LLE) or for the sidewall image transfer (SIT) approaches. Indeed, HBr plasma treatment can be used as a freezing process in LLE approach or as an hardening process in SIT approach to allow CVD spacer deposition directly on the 193nm PR patterns. It is now acquired that plasma VUV light plays a key role in the PR chemical modifications but a fundamental understanding of the impact of HBr plasma treatment on 193nm PR is still lacking.

In this paper, we propose to bring new insights of the resist chemical modifications induced by such plasma treatment by using thermal desorption-gas chromatography/mass spectrometry (TD-GC/MS) measurements [2] and thermal analysis.

In order to isolate effect of plasma ions and radicals of resist chemical modification induced by VUV plasma light, samples coated with a model 193nm resist (polymer only and full formulation) and exposed to a HBr plasma (directly or via a LiF window) are analysed. Our approach, based on TD-GC/MS technique, is an indirect method to monitor the by-products outgassed during different process steps [3]. Samples are heated in a quartz chamber under an inert gas flow driving the outgassed species through a cooled Tenax adsorbent tube where they are trapped. Then, the compounds are analysed by GCMS with an injection by thermo desorption of the collection tube. Some results are reported in figure 1. Thus the outgassing rate associated with sample exposed directly to HBr cure plasma is significantly lower that outgassing rate of the samples exposed under LiF window, suggesting plasma induced surface hardening. Moreover a short O2 plasma treatment seems enough to remove the surface layer. Quantitative and qualitative TD-GCMS analysis correlated with Thermo-Gravimetric Analysis (TGA) allow us to show that plasma H+ ions induce resist deprotection (see for examples fig.2).

In conclusion, using such methodology we propose a fine analysis of fundamental mechanisms involved in 193nm resist modification under HBr cure plasma treatment.

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7972-42, Session 10

Systematic studies on reactive ion etch-induced deformations of organic underlayers

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Underlayers (UL), also known as organic planarizing layers (OPL) or spin-on carbon (SOC) layers, play a very important role in various integration schemes of chip manufacturing. One function of OPLs is to fill in any kind of pre-existing patterns on the substrate, such as previously patterned vias, to enable lithographic patterning of the next level. More importantly, their resistance to reactive ion etch (RIE) processes used to etch silicon-containing materials is essential for the successful pattern transfer from the photoresist into the substrate. Typically, the pattern is first transferred into the OPL layer through a two-step RIE sequence, followed by the transfer into the substrate by a fluorine-containing RIE step that leaves the OPL pattern mainly intact. However, when the line/space patterns are scaled down to line widths below 35 nm, it was found that this last

RIE step induces severe pattern deformation ("wiggling") of the OPL material, which ultimately prevents the successful pattern transfer into the substrate.

We developed an efficient process to evaluate OPL materials with respect to their pattern transfer performance. This allowed us to systematically study material, substrate and etch process parameters and draw conclusions how changes in these parameters may improve the overall pattern transfer margin.

7972-43, Session 10

Hexafluoroalcohol (HFA) containing molecular resist materials for high-resolution lithographic applications

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Molecular glass resists have gained attention for the past decade as a potential platform for high resolution lithography. Several molecular resist materials based on the calix[4]resorcinarene system have been developed. Though this molecular system is very versatile, there are several challenges with the synthesis and processing of these materials. The difficulty to synthesize a monodipserse unit, the poor solubility in casting solvents and incompatibility with conventional developer are some noted challenges. We have addressed these issues by designing a new calix[4]resorcinarene resist material with hexafluro alcohol (HFA) units. The resist platform has been evaluated with e-beam and EUV lithography.

7972-44, Session 10

Bound PAG resists: EUV and electron-beam lithography performance comparison

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One of the most promising resist design strategies for the development of high resolution materials for EUV lithography is the anion-bound polymer approach[1]. We have published several reports in the past few years on the structure/property relations of anion bound PAG resist polymers [2]. This paper will focus on relative performance of novel bound PAG polymers in EUV and electron beam lithographies. We will analyze the performance characteristics of a series of well characterized bound PAG resist polymers using several PAG monomers. Due to the limited access to EUV exposure tools, we analyze the initial lithographic performance with electron beam lithography for improved cycles of learning. We have found several examples of poor correlation between EUV and e-beam (EB) results. We will offer rational for the difference in performance, with the goal of improved insight into both EB and EUV resist design.

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7972-45, Session 11

Addressing challenges in lithography using sub-millisecond post exposure bake of chemically amplified resists

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Chemically amplified resists (CARs) typically require a post exposure bake (PEB). This bake, performed on a hot plate at 90-150 ºC for 30-120 seconds, enables pattern formation by deprotection of the resist and diffusion of photogenerated acids. Sufficient time must be provided to achieve the deprotection level required for solubility switch in a developer, yet excessive time results in acid diffusion with loss of line edge definition, blurring of latent images, and increase in line width roughness (LWR). The lithography roadmap requires LWR (3) to be reduced to <2 nm by 2015, demanding an unprecedented level of control of acid diffusion while maintaining high resist sensitivity. Although strategies have been proposed and investigated to control acid diffusion by either binding PAG moieties to polymer chains or by increasing the size of the PAG anion, existing PEB studies and the characterization of acid diffusion on these modified resist materials has shown limited improvement.

In this work, we have shifted the time/temperature regime of PEB into the millisecond regime using a scanned laser source. Under scanned CW laser irradiation, the PEB temperature is changed from the range of 100-150 ºC for seconds duration to a temperature range of 200-500 ºC for sub-millisecond times. In this ultra-fast laser PEB (/-PEB) regime, the relative impact of acid diffusion on the resist deprotection can be reduced. Several polymer and photoacid generator (PAG) resist systems have been studied under 500 µs heating at temperatures estimated between 200 and 400 ºC. All of the resist systems exhibit remarkable stability at these temperatures - a direct consequence of the short duration of the heat cycle. Despite five orders of magnitude difference in PEB duration, resist sensitivity is enhanced under deep UV by at least 50% for conditions exhibiting comparable acid diffusion. Similar behavior in deprotection and acid diffusion is observed under extreme UV lithography (EUVL). Preliminary imaging using EUVL shows ~20% reduction in LWR - a result from optimizing resist sensitivity and diffusion under sub-millisecond PEB (Fig. 1).

The kinetics of the both deprotection and diffusion have been quantified across the seconds to milliseconds time frame and indicate significant changes in mechanisms between the two regimes. Comparable E_0 is observed under the same PEB temperatures despite a 10^5 factor difference in PEB duration, suggesting a fundamental change in deprotection mechanism between seconds and millisecond time frames. At constant temperature and exposure dose, the deprotection reaction rate under /-PEB is enhanced by 4 orders of magnitude (Fig. 2). These results suggest that the reaction kinetics are heavily dependent on temperature ramp rate (hot plate ~100 K/s and /-PEB: >10^5 K/s). While diffusivity for hot plate follows the expected WLF model near the resist's glass transition temperature, diffusivity under /-PEB jumps by 3 orders of magnitude at overlapping temperatures. However, the activation enthalpies in both regimes are similar (160 kJ/mol for hot plate and 120 kJ/mol for /-PEB). A model explaining the significant difference in reaction kinetics between two time frames is currently under investigation.

7972-46, Session 11

Extension of photo-patternable low-k concept to 193-nm lithography and e-beam lithography

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Increasing complexity and manufacturing costs, along with the fundamental limits of planar CMOS devices, threaten to slow down the historical pace of progress in the semiconductor industry. We have proposed and demonstrated proof-of-concept of a simple and low-cost way to fabricate dual-damascene copper (Cu) on-chip interconnect or Back-End-Of-the-Line (BEOL) structures using a novel multifunctional on-chip electrical insulator, called a photo-patternable low dielectric constant (low-) dielectric (PPLK) material [Q. Lin, et al, Proc. SPIE, 2010]. This demonstration was accomplished with a silsesquioxane-based (SiCOH), =2.7 PPLK material which is compatible with 248 nm optical lithography. A PPLK material combines the functions of a traditional photoresist and a dielectric material into one single material. It eliminates the need for sacrificial layers (including a separate photoresist) and their related deposition, pattern transfer (etch), and removal processes for dual-damascene BEOL patterning. Therefore, this novel PPLK concept offers the benefits of dramatically reduced process complexity and manufacturing costs.

In this paper, we wish to report on the extension of the photo-patternable low-K concept to the ultra-low- (<2.5) regime and resolution down well below 100 nm with 193 nm lithography as well as e-beam lithography. We have accomplished this demonstration using the same SiCOH material platform as that of the 248 nm PPLK materials. The 193 nm PPLK materials possess dielectric constants below 2.5 and are able to resolve 100 nm half-pith line/space features with dry 193 nm single exposure lithography. The resolution of PPLK materials can be pushed down to 40 nm half-pith line/space features with line-edge-roughness less than 3.0 nm with e-beam lithography. Therefore, the photo-patternable low- material concept is a promising material platform technology for highly efficient, low-cost and “greener” semiconductor manufacturing.

7972-47, Session 11

Process capability of implementing ArF negative resist into production

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Resist supplier has successfully demonstrated applying negative tone resist into ArF lithography. It is capable to achieve 50nm dense line and <30nm isolated space pattern by over dose operation under topcoat-free immersion lithography. Additionally 65nm grid contact hole patterns could also be generated by using ArF dry system with double exposure. For specific application, negative PR ArF lithography has better benefit of cost and process control capability than other various approaches. In this paper, we have determined process capability of 65nm grid contact hole by ArF dry double patterning and compared with LELE process including DOF, EL, CDU and cost. By continuously optimizing process parameter, >0.21um DOF and 4.6nm global CDU are achieved on DRAM capacitor process. It revealed strong relation to development parameter setting. Furthermore, specific pattern formation considering optical items, ex: OPE, NRF (non-resolution feature) and inter reaction between double exposure, have also been analyzed and figured out difficulties of generating a specific pattern with negative tone resist double exposure.

7972-48, Session 11

Development of an inorganic nanoparticle photoresist for EUV, e-beam, and 193-nm lithography

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As feature sizes continue to decrease, film thickness must be reduced in order to prevent pattern collapse. Thinner films prevent sufficient pattern transfer during the etch process, creating the need for a hardmask, thus increasing production cost. We have developed a transparent, high refractive index inorganic photoresist with significantly higher etch resistance than even the most robust polymeric resist. Compared to PHOST, we have shown over 10 times better etch resistance. Organic photo-crosslinkable ligands have been attached to a hafnium oxide nanoparticle core to create an imageable photoresist. This resist has shown superior resolution with both E-beam and 193 nm lithography, producing sub-50 nm patterns. In addition to improved etch resistance, the inorganic photoresist exhibits a high refractive index of around 2.0, increasing the depth of focus (DOF). The small particle size of around 1-2 nm has the potential to reduce line edge roughness (LER).

7972-49, Session 11

Fast dry cleaning of resins by high-power vacuum ultraviolet light

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Cleaning of resins is continuous subject at the lithography process of semiconductor manufac-turing. Many alternate processes are industry-widely investigating to reduce process compli-cation and liquid waste disposal instead of current wet cleaning methods. Dry cleaning meth-ods by ultraviolet (uv)-ozone and o2-plasma are frequently used in the semiconductor process, because they are clean and easy. However, they are not effective against heavily contaminated samples. Therefore, the use of high power irradiation of a vacuum ultraviolet (VUV) has been introduced as an effective decomposition of resins. For example, mold-cleaning is one of re-maining problems in the imprint-lithography process1, which has attracted many attentions as next-generation lithography. Repeatedly-used molds should be cleaned for the next series of imprint-process.

Cleaning mechanism of VUV light is briefly introduced. It consists of two steps; the first is decomposition of organic materials (CxHyOz) by VUV light with chemical bond dissociation energy of h , and the second is oxidation by a singlet-oxygen, O(1D). Both reac-tions are shown by Equations (1) and (2), respectively.

CxHyOz + h Cx’Hy’Oz’ (1)

Cx’Hy’Oz’ + O(1D) CO, CO2, H2O (2)

Cx’Hy’Oz’ represents chemical product of CxHyOz after breakage of chemical bonds, and the equations here are qualitatively shown. Then they are stoichiometrically incorrect. The singlet-oxygen is generated by following Equations of (3) and (4). Conventional UV light by mercury lamp also generates the singlet-oxygen by Eq. (3). On the other hand, VUV light generates the singlet-oxygen directly from oxygen by Eq. (4). Therefore, the cleaning by VUV is more than ten-times effective than that by UV.

O2 + h O3, O3 + h O(1D) (3)

O2 + h O(1D) (4)

Three kinds of resins are used, i.e, acrylic resin for UV-imprint, novolac resins for i-line , and acetal resin for KrF. They are coated on silicon wafer using a spinner. The VUV light, which is manufactured by Ushio Inc. 2, is

irradiated on the resins on silicon. Figure 1 shows relationship between ashing rates and power of VUV light for three UV-resins. VUV-exposure condition is as follows; substrate temperature is 25 , radiation distance is 2 mm. Acrylic-base resins are etched much faster than other resins. The ashing rates of resins for i-line and KrF increase gradually with VUV-irradiation intensity. The values of the ashing rates reach almost 100 nm/min or more. These are much higher than that by well-known UV-ozone using a mercury lamp, whose ashing rate is at most several nm/min.

This is the first report to show results of effective dry cleaning by VUV light for resins, especially for the acrylic-base resin. The ashing rates reach almost 100 nm/min or more, those are much faster than that of conventional cleaning methods such as uv-ozone cleaning. The cleaning by VUV light is found to be very hopeful method from the viewpoints of cleaning effectiveness and solving environmental problem. We are now focusing on cleaning of im-printed molds, which are contaminated by organic substances such as UV-resins through many imprinting processes.

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7973-01, Session 1

Lithography beyond the IC

B. W. Smith, Rochester Institute of Technology (United States)

No abstract available

7973-02, Session 1

Design architecture, metrology, and integration: OPC at the age of discovery

C. E. Tabery, GLOBALFOUNDRIES Inc. (United States)

No abstract available

7973-03, Session 1

Present and future of NAND flash scaling at the lithography crossroad

T. D. Pham, SanDisk, Inc. (United States)

No abstract available

7973-04, Session 2

Freeform and SMO

R. J. Socha, ASML US, Inc. (United States)

No abstract available

7973-05, Session 2

Qualification, monitoring, and integration into a production environment of the world's first fully programmable FlexRay illuminator

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This presentation will describe the development, qualification, monitoring, and integration into a production environment of the world's first fully programmable illuminator for 193 nm optical lithography. FlexrayTM, the programmable illuminator based on a mulit-mirror MEMs array developed for 1900i series ASML immersion scanners [1], was first installed in January 2010 at Albany Nanotech. After a brief overview of the principle and benefits of Flexray, this paper will provide a comprehensive assessment of the imaging performance of Flexray. This will include comparisons between Flexray and standard diffraction optical elements (DOEs) on a given tool, tool-to-tool matching on multiple tools with Flexray and DOEs, and long term monitoring and stability performance.

A procedure for evaluating the imaging performance of Flexray will be described. Programmable illuminators enable a nearly infinite number of possible illumination pupil shapes determined by advanced RET techniques such as source mask optimization (SMO). It is often not useful to describe these complicated pupils with standard analytic pupil models. Thus, a CD-based simulation approach has been developed to quickly analyze a large number of measured pupils, allowing a quick assessment of pupil quality and a prediction of imaging performance. For example, this procedure enabled roughly 3000 pupils to be evaluated during the factory acceptance and on-site acceptance of the first Flexray unit in less than three and five days, respectively. CD-based analysis data will be provided for all tools that have been installed, showing a match-to-target performance of typically less than about 1%.

In addition, a series of experimental data sets from various 22nm levels will provide in-resist assurance that Flexray is providing excellent imaging performance. To date, any variations that may be due to Flexray have not been observable in photo-resist. Also, the integration of Flexray in to a fully functional production environment will be discussed, to include the qualification procedure, IT infrastructure, and production line monitoring. Lastly, some of the unique advantages of a fully function programmable illuminator will be explored, such as fine-tuning RET performance and tool specific pupil tuning.

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7973-06, Session 2

Agile and accurate control of lithographic imaging using a freeform illuminator

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As shrinkage of semiconductor device pattern progresses, more precise control of critical dimension (CD) of resist pattern is needed. There is increasing demand for improvement of accuracy of optical proximity correction (OPC) and enlargement of exposure latitude (EL) and depth-of-focus (DOF). Consequently, requirements for mask OPC performance, accuracy of mask CD control, and imaging performance of exposure tool are becoming more exacting.

In recent years, exposure techniques using freeform shape illumination have attracted attention as a means of improving accuracy of fine resist CD. In particular, freeform illumination formed by a micro mirror array (e.g. ASML FlexRay) has remarkable features, such as freedom of illumination shape and short lead time for creating new illumination, prompting expectations of more precise control of imaging performance and the possibility of satisfying more exacting requirements. A freeform illuminator of that type is often considered to be (1) a means of source mask optimization (SMO) and (2) a tool for fast correction of mask error, exposure tool fingerprint and process variation. (2) is effective not only in the process-development phase but also in the mass-production phase.

In this paper, we focus on (2). We evaluate the technical potential of tuning image performance using modification of illumination shape in the freeform manner. The evaluation contains two steps: (a) development of illumination design software to calculate the illumination modification for compensating the difference between "as is" and "to be" with respect to the resist image and (b) measurement of the performance of image tuning thorough exposure and resist CD measurement. We describe the calculations of freeform illumination and present the exposure results, and discuss the effectiveness of image tuning by freeform illumination in detail.

7973-07, Session 2

Design-specific joint optimization of masks and sources on a very large scale

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Source Mask Optimization (SMO) has been proposed and demonstrated as a RET for extending optical lithography without further increases in the scanner NA. For some levels at the 22nm node and beyond, SMO is able to recover forbidden pitches and non-printable 2D features by co-optimizing all such difficult design patterns jointly with the source. As has been reported by our group and others, source optimization is improved when the simultaneous interactions of all mask variables with the source variables is directly taken into account during a joint optimization step [1,2] .

Previous SMO publications have focused on small-scale joint optimization, in which only few generic or critical clips are co-optimized with the source. However, for a fab to provide finely tuned support for different customers whose layouts may exhibit significant variation, an automatic selection of a broad and encompassing clip population from an actual design is preferred. When SMO uses a process window objective, only a very small proportion of features in a layout is likely to be binding on the common process window, and it is only these features which are determinative of the optimum source for the layout. Other features will not contribute binding constraints when included in the optimization, and so will not affect the source solution. However, without knowing these binding features in advance it is preferable to extract as many unique clips as possible to represent the design. Unfortunately, every mask variable is coupled to every other mask variable via the source variables during joint optimization (since each source variable illuminates all parts of the mask), presenting SMO systems with a very challenging optimization problem as mask area is increased to include a large number of clips.

In this paper we show that a two-stage SMO technology has been developed to meet the challenging problem of layout-specific source design. First we demonstrate with examples that jointly optimized extremely large mask areas together with the source variables can be carried out on high performance computing platforms that are available today. Second, we show that it is not necessary to exhaustively optimize the entire mask together with the source in order to identify these binding clips.

This paper shows how having such an approach can be used to address variability among different users' designs, with the aim of delivering a better RET process for specific layouts. These sources can be realized using pixelated illumination from a programmable illuminator, or alternatively from a custom diffractive optical element (DOE). In addition, we will discuss the operational flows used in assessing this approach along with associated experimental results.

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7973-08, Session 3

Illuminator predictor for effective SMO solutions

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Source Mask Optimization (SMO) is one of the most important techniques available for extending ArF immersion lithography. However, imaging with a small k1 factor (~0.3 or smaller) is very sensitive to errors in the illumination pattern. As a result, care must be taken to insure that the source solution from SMO can be produced by the real illuminator, which is subject to its own imaging constraints. One approach is to include an illuminator simulator in the SMO loop so that only realizable illumination pupils are considered during optimization. Furthermore, any illuminator predictor used in SMO should operate quickly compared to the imaging simulation if it is to avoid increasing the computational load.

In this paper we present and describe an illuminator predictor that accounts for the constraints of an ArF immersion illuminator in a very physical way, including the effects produced by all of its various components, illuminator-setting specific mapping, and shift-variant imaging properties. The illuminator predictor is also shown to operate with a speed that is comparable to standard lithographic imaging simulations. We demonstrate the accuracy of the illuminator predictor by validation against raytraced and experimental illumination pupilgrams and their OPE curves.

7973-09, Session 3

Full-chip source and mask optimization

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Below the 32 nm node, manufacturable designs can only be achieved by using an increasing number of advanced computational lithography (CL) techniques during the OPC tape-out flow. These CL techniques typically involve increased computational load and complexity, and as a result, tape-out time and costs increase. This paper examines an approach called full-chip source mask optimization that is designed to enable the targeted and efficient use of these advanced techniques that might otherwise be limited due to high computational cost.

Full-chip source mask optimization is an approach that strives to achieve an optimum solution among the competing requirements of manufacturing process window, mask complexity and cost, and tape-out throughput time. Its two components are source mask optimization (SMO) and full-chip mask optimization (FMO). SMO is used to optimize the source given a representative set of clips, and FMO achieves the user-required process window (PW) and MEEF with acceptable runtime during the full-chip tape-out.

SMO has been widely accepted and, combined with the FlexRay programmable illuminator from ASML, has enabled user-tunable off-axis illumination for optimum resolution based on actual designs. Prior publications [1-6] have demonstrated how this is achieved using a representative set of design clips. This paper proposes a new method using a diffraction order technique to optimize this clip selection, for greater efficiency and better representation of full-chip designs.

FMO is a framework employed during the OPC tape-out flow where advanced computational methods for mask correction are applied only where they are most needed, thereby balancing performance and cost. Computationally inexpensive methods are used for design areas where a satisfactory process window can be achieved, and more expensive techniques are used for the remaining critical areas where such techniques are the only viable means of achieving the desired process window. These techniques - like model-based freeform SRAFs and full co-optimization of SRAFs and main features -- will be discussed

in this paper. Essential to this FMO approach is to resolve any boundary conflicts between the different methods, so that no new defects are created on the boundaries.

Figure 1 showed an example of using this technique. A source was optimized through SMO, and then applied to a full-chip MB-SRAF OPC. A high MEEF critical area was detected and corrected by co-optimization. Details of this full-chip source and mask optimization approach using realistic design data will be presented in the full paper. The combination of an SMO-optimized source with the new FMO flow permits the efficient identification of solutions that maximize process window and CD uniformity, while minimizing MEEF, mask complexity, and computational cost and time.

7973-10, Session 3

Joint optimization of layout and litho for SRAM and logic toward the 20-nm node using 193i

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This paper reports on a study in which we are comparing different possibilities to find a litho solution for SRAM and Logic for technology nodes between 28 nm and 20 nm. At these nodes, it becomes essential to include the layout itself into the optimization process. The so-called gridded design style is an attractive candidate to facilitate the printability of several layers, but the benefit of this design style, as compared to less restricted design styles, is not well quantified for the various technology nodes of interest. In addition, changes in cell-layout can often eliminate, relax or move the lithography constraint to another layer which can therefore be interesting to consider, even if they have a (small) area penalty. Layout design changes can also help 'postpone' double (or multiple) patterning or other cost-increasing options to slightly more aggressive nodes. For all solutions, the layout optimization impact on the cell area needs to be evaluated, in order to also quantify possible area trade-offs when adopting certain layout- or lithography options. This paper will be looking into these issues and will try to quantify some of the relevant options and trade-offs.

For this study we are using a small test chip containing SRAM and a mini Logic library, which we think has enough variety to be representative for a real Logic chip. We investigated all critical layers from Active to Metal2. For each choice of the Layout- and lithography-options the litho performance is optimized using the Tachyon SMO software from Brion. Litho performance options studied include the use of negative-tone development, the use of double patterning, the choice of litho target etc. Also the type of double patterning, split layers with LELE, or SDDP with cut-mask, is taken as a variable in our study. We are using simulated DOF, EL and MEF values as the main metrics, and compare them to the adopted target values to evaluate whether the predicted performance is good enough, and to compare the different layout-litho options. The comparison of the options included should therefore help understand what their advantages and drawbacks are at each technology node and provide useful information for anybody who needs to decide how to solve litho constraints and adopt a combined Litho-Layout_Design optimum solution for the next technology node.

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7973-11, Session 3

Applicability of global source mask optimization to 22/20-nm node and beyond

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Source-Mask Optimization (SMO) in optical lithography has been the subject of increased exploration to enable 22/20nm and beyond technology nodes in recent years [1-6]. It has been shown that intensive optimization of the fundmental degrees of freedom in the optical system allows for the creation of non-intuitive solutions in both the soruce and mask, which yields improved lithographic performance.

This paper will present the value of SMO software in Resolution Enhancement Techniques (RETs). The main benefits observed are the improved through-pitch performance, the possibility of avoiding double exposure, the capability of printing denser layouts without further increase in the scanner NA, etc. The benefits from optimized source, optimized mask as well as optimized source and mask together will be demonstrated. Furthermore, we leverage the benefits from intensive optimized mask, for solving larger array cases, in Memory Use Model (MUM), and developed mask synthesis & data prep flows to incorporate this methodology.

We have incorporated usage of SMO, including both RETs and MUM, in several critical layers during 22/20nm technology node development. Experimental assessment will be presented to demonstrate the benefits that we can achieve by using SMO during 22/20nm.node development.

7973-12, Session 3

Supreme lithographic performance by simple mask layout based on lithography and layout co-optimization

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The area ratio of SRAM to logic in ICs is becoming larger while the cell size is expected to continue to shrink. The contact layer is, among several critical layers in SRAM, the toughest. In this paper, our innovative SMO technology is applied to this contact layer. In our SMO the mask layout is parametrized and the parameters are optimized simultaneously with lithography parameters such as illumination source. Balancing correction of CD error by mask layout and correction of CD error by OPE due to illumination source in the combined optimization space, higher CD accuracy than conventional OPC and better lithographic margin than SRAF can be achieved with simple mask layout.

We investigate the effectiveness of our approach for cases of 45nm node (170nm hole pitch) that is manufactured as the most up-to-date device and 28nm node (100nm hole pitch) that might be the limit by single exposure method with ArF and NA=1.35, which is the standard condition in our evaluation.

At 45nm node better performance than conventional OPC and SRAF is achieved with very simple mask layouts of rectangles for the general holes. Even for the shared contact whose design does not consist of single rectangle but instead a polygon, the optimized mask layout has the same shape as the original. Our SMO is evaluated at other NA values

below than 1.35 to determine how the performance of this technology varies under lower k1. It turns out that NA of 1.1 works well for the resolution of the cell. This lower NA is preferable for the peripheral circuit pattern that consists of random patterns with less severe dimension and pitch. Though the fidelity of shared contact becomes worse under the lower NA, a slightly more complicated parametrized layout improves the fidelity.

At 28nm node using conventional OPC technology the performance is not sufficient due to large MEEF close to 10. However our SMO can get good performance with some increase of mask complexity in comparison to the one at 45nm node, as well as some algorithm refinement.

The simple mask layout reduces MEEF by around 30% compared to the OPC layout. Combining the smaller MEEF and the ease of manufacturing mask with simple layout can attain high CD accuracy in the actual printing. The simple mask layout also reduces mask cost due to reduced mask data.

Our innovative SMO technology shows supreme lithographic performance with lower cost than conventional technology for the SRAM device from the present mass production stage to the future one that might be the limit by single exposure method.

7973-13, Session 4

Simultaneous OPC and decomposition for double-exposure lithography

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Double exposure techniques are an economically viable method for extending the life of the current 193nm wavelength immersion lithography techniques into future generations of semiconductor scaling. One popular example of double exposure is the use of double dipole illumination, where the X and Y dipoles are separately optimized for vertical and horizontal features respectively. The primary challenge in such double exposure techniques lies in the process of target layout decomposition into patterns that can be optimally printed using their respective source. Current approaches for decomposition are rule-based. They suffer from the drawbacks of scalability, rule count explosion and inability to guarantee sufficient yield in the presence of process variation. Further, rules are characterized specific to sources and are relatively easy to develop for dipoles, but far more difficult to develop for more complex sources such as used in source mask optimization (SMO). Decomposed target layouts have to further undergo optical proximity correction (OPC) in order to be converted to a mask for use in manufacturing. In this paper, we propose a novel approach which integrates the processes of decomposition and optical proximity correction. We preclude the intermediate target decomposition stage. Instead, we directly optimize the masks for both exposures simultaneously in order to obtain a wafer image that both closely matches the target layout and is also robust to process variation. For this purpose, we define a lithographic cost function that is weighted sum of intensity error and intensity slope. We develop methods to analytically predict the change in this cost function due to movement of fragments on each mask. We then utilize a gradient-descent algorithm for fragment movement to minimize the cost function. Since our methodology is based on the knowledge of the SOCS decomposition kernels, it is not restricted to dipoles alone, but can be utilized for any complex sources for which such kernels are known. Our experiments on 1x metal (M1) show significant improvement in layout process window compared to traditional rule-based decomposition methods.

7973-14, Session 4

Toward manufacturing of advanced logic devices by double patterning

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The IBM Alliance has established a DETO (Double-Expose-Track-Optimized) baseline, in collaboration with ASML, TEL, and CNSE, to evaluate commercially available DETO photoresist system for the manufacturing of advanced logic devices. The DETO technique produces pitch-split patterns capable of supporting 16 nm and 11 nm node semiconductor devices. We present the long-term monitoring performances of CD uniformity (CDU), overlay, and defectivity of our DETO process. CDU and overlay performances for controlled experiments are also presented. Two alignment schemes in DETO are compared experimentally for their effects on inter-level & intra-level overlays, and space CDU. We also experimented with methods for improving CDU, in which the CD Optimizer and DoseMapper were evaluated separately and in tandem. Overlay improvements using the High-Order Wafer Alignment (HOWA) and the intra-field High-Order Process Correction (i-HOPC) were compared against the usual linear correction method. The effects of the exposure field size are also compared between a small field and the full field. Included in all the above, we also compare the performances derived from stacked wafers and bare-Si wafers.

7973-15, Session 4

Innovative self-aligned triple patterning for 1x half-pitch using single “spacer deposition-spacer etch” step

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We successfully demonstrate a new approach to achieve 15nm half pitch with a spacer based self-aligned triple patterning (SATP). This new concept has a single spacer deposition and etch step to achieve 15nm half pitch using immersion lithography. Current spacer based triple or quadruple patterning approaches use two iterations of “spacer deposition / spacer etch” for pitch splitting, thus generating multi-modal trench CD, line CD and, trench depth population leading to challenging process control. The new concept overcomes CD population issues and reduces additional steps over implemented double patterning, thus could relax process window. The key innovative aspect is an undercut dry trim achieved by layer-by-layer trim process, followed by flowable CVD (Eterna FCVD) based gap-fill that can fill undercut structures. The process flow is described in the following chronological order: 45nm half pitch structures are printed on 193nm immersion lithography (Fig. 1a and 1b). Printed pattern is transferred thru APF and Poly preserving CD integrity (Fig. 2a and 2b). Poly is selectively trimmed down to around 15nm using a layer-by-layer dry etch process with high selectivity to core APF (Fig. 3a and 3b). The selective dry layer-by-layer etch process has the advantage to protect line integrity without collapse unlike common wet removal processes. Trimmed Poly will eventually act as imbedded hard mask. Features are then filled with a flowable oxide FCVD (Fig. 4a and 4b). Flowable oxide enables void-free gap fill underneath a sacrificial APF hard mask, as well as planarization (XSEM tilted view in Fig.4b). Dry etch-back is then used to recess the flowable oxide down to clear APF (Fig.5a and 5b). Spacer material is chosen to be the same material as the imbedded Poly hard mask (Fig.6a and 6b). Spacer is then etched-back to expose a 45nm line sacrificial APF core (Fig.7a and 7b). At this step, Poly spacer line size is close to 15nm. Imbedded hard mask and spacer materials need to have close etch- selectivity with respect to gap fill material. Both Poly Spacer and imbedded Poly hard mask are used for pattern transfer. Final result is 15nm half pitch structures.

Further transfer of this new 15nm ½ pitch pattern to the substrate (e.g., Oxide, APF, Poly, Si...). Different substrates will require an adequate choice of imbedded hard mask and spacer materials.

7973-16, Session 4

DPT-restricted design rules for advanced logic applications

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With the advance of the semiconductor roadmap, optical lithography has reached its resolution limits using single patterning because of limited wavelength and numerical aperture (NA) scaling. Double patterning was proposed as the extension to immersion lithography before next generation lithography technologies mature. There have been discussions [1-2] on wafer process and layout decomposition for two typical double patterning approaches: Litho-Etch-Litho-Etch (LELE) and Self-Aligned Double Patterning with spacer lithography (SADP). Beyond the regular line/space gratings, the decomposed layers derived from original target layer can be complicated which present significant lithography challenges especially for metal layers in logic applications. For example, on the block mask in the SADP process, there are small holes or posts, thin lines and spaces, and complex 2D shapes generated by the decomposition algorithm. Restricted design rules have to be applied to constrain design layouts for both printability and compatibility with double patterning.

This paper will start from coloring rules for double patterning, and analyze the required design rule constraints so that the decomposed layers can be manufacturable and combined to create the original target layer faithfully. The manufacturability constraints utterly limit the layout complexity and designability in logic designs. Source mask optimization (SMO) is used to maximize the printability of all derived patterns at the same time for respective decomposed layers. This helps to evaluate choices in layout decomposition, such as the use of stitching in LELE and the use of block mask in SADP to resolve odd-cycle color conflicts. This joint optimization in design rules between design, decomposition and process constraints is necessary to achieve the best scaled designs for manufacturing.

[1] Patrick Wong, Vincent Wiaux, Staf Verhaegen, and Nadia Vandenbroeck, “Litho-process-litho for 2D 32nm hp Logic and DRAM double patterning,” Proc. SPIE, Vol. 7640, 76400I (2010)

[2] Yuansheng Ma, Jason Sweis, Chris Bencher, Huixiong Dai, Yongmei Chen, Jason Cain, Yunfei Deng, Jongwook Kye, and Harry J. Levinson, “Decomposition Strategies for Self-Aligned Double Patterning,” Proc. SPIE, Vol. 7641, 76410T (2010)

7973-17, Session 4

Scanner alignment performance for double patterning

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Double patterning (DP) is now widely accepted as a viable technology for the further extension of 193nm lithography towards the 22nm /18nm technology nodes. Several DP processes are being examined. Two of the most promising are Double Patterning with Spacer (DPS) and Litho Etch Litho Etch (LELE). Both of these techniques may introduce new challenges for the scanner alignment system.

LELE Double patterning on thin film hard mask allows two types of alignment strategies. The second DP layer can aligned either on the first DP Layer or directly on the same layer as the first DP layer. For a k1=0.14 Double Patterning process, these alignment strategies will be statistically evaluated. (Ref. #2; #3).

DPS may result in alignment marks with reduced image contrast after completion of spacer patterning Consequently there is an elevated risk that alignment performance of the Cut lithography layer on the spacer (Ref. #1) may be negatively impacted. Initial studies indicate that it may be necessary to consider new mark designs. In this paper we discuss the basic design of these alignment marks and make a statistical assessment of their relative performance.

Spacer patterning is an asymmetrical process and is defining two types of surface (inside and outside of the spacer). The impact of this asymmetry will also be assessed. Mark geometries will be charactered with 3DAFM measurement and alignment performance analyse.

7973-18, Session 4

Effective decomposition algorithm for self-aligned double patterning

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As the 193nm optical source and double patterning lithography will be the only option for the mass production of integrated circuit (IC) of sub-32nm technology in the near future, the self-aligned double patterning (SADP) is now taking the most promising position with its intrinsic property on less overlay requirement compared to other double patterning lithography techniques.

Instead of simple decomposition method for SADP application in 1D memory design, a much more complex decomposition strategy is needed in order to fulfill the flexibility requirement on logic design patterns. Most recently, a newly developed SADP process - the positive tone process, has been introduced in [1], in which the spacer pattern and block mask can work together to generate complex 2-D features. However, [1] did not report any algorithm/tool to automatically decompose the layout and generate optimal spacer and block mask efficiently. In this paper, based on the positive tone process and complex 2D layout, we will first provide an effective decomposition algorithm on generating the spacer and block masks automatically.

First, we will characterize the three types of decomposition methods in the positive tone SADP process which will bring three different overlay scenarios. Indeed, the final metal patterns will be generated following the Geometric Boolean Equation:

Pattern=~(Sidewall OR Resist)=~Sidewall AND Block_Mask.

As sidewall width is uniformly defined by the CVD process all over the chip, in order to generate different wire width without worrying about overlay error, the patterns need to be covered by the block mask and surrounded by sidewalls, as the two options shown in Fig. 1.

Based on the two options in Fig. 1, we need to place sidewalls on the edge of the CD. As shown in Fig. 2, in order to generate the rectangle (green), sidewalls (orange) should be placed on the boundary, whose extension lines will define five regions labeled as “+” and “-” sign. For an overlay-free decomposition result, either “+” or “-” region should be defined as spacer and the rest will be assigned as blank space. Since any spacer will form a sidewall ring, therefore a successful decomposition solution should have no conflict on the area sign assignment, match the non-regular design rule of spacer layer, and minimize the edge length on CD which is not covered by sidewalls. We can formulate this problem into a Boolean Satisfiability Problem (SAT) problem and apply an effective SAT algorithm to solve the problem. We have justified the validation problem in some small layout, and expect to achieve a whole chip one time solution in the near future.

7973-19, Session 5

Mandrel-based patterning: density multiplication techniques for 15-nm nodes

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In many ways, sidewall spacer double patterning has created a new paradigm for lithographic roadmaps. Instead of using lithography

as the principal process for generating device features, the role of lithography becomes to generate a mandrel (a pre-pattern) off-of-which one will subsequently replicate patterns with various degrees of density multiplication. Under this new paradigm, the innovativeness of various density multiplication techniques is as critical to the scaling roadmap as the exposure tools themselves.

Sidewall spacer double patterning was the first incarnation of mandrel based patterning; adopted quickly in NAND flash where layouts were simple and design space was focused. But today, the use of advanced automated decomposition tools are showing spacer based patterning solutions for very complex logic designs. Future incarnations can involve the use of laminated spacers to create quadruple patterning or by retaining the original mandrel as a method to obtain triple patterning. Directed self-assembly is yet another emerging embodiment of mandrel based patterning, where self-separating polymers are registered and guided by the physical constraint of a mandrel or by chemical pre-pattern trails formed onto the substrate.

In this summary of several bodies of work, we will review multiple forms of mandrel based patterning including sidewall spacer based double, triple and quadruple patterning techniques capable of 15nm half-pitch. We will discuss the theoretical CDU performance capabilities combined with the wafer level data. To address concerns surrounding spacer double patterning design restrictions, we worked with an EDA partner to study decomposition solutions for a typical 45nm node micro-processor routing layer, scaled to 60nm pitch (15nm node) dimensions. Additionally, leading researchers in directed self-assembly have begun testing materials in the context of our 300mm pilot fab, and these experiences and results will be shared as perhaps the ultimate embodiment of mandrel based patterning which can address feature sizes well beyond 15nm half-pitch.

7973-20, Session 5

Characterization of a thermal freeze LLE double-patterning process for predictive physical simulation

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Frequency double patterning is the most immediate lithography candidate for IC technologies requiring pitches below the single exposure capabilities of todays water immersion ArF scanners. Materials based LLE processes potentially offer substantial cost and throughput benefits over the more proven LELE approaches. However, there are many potential process and material interactions between the lithographic layers (BARC, Resist 1, Resist 2).

In this work, a thermal cure resist freeze process is studied. Basic models are derived for the BARC and resist materials and the impact of all processing steps on each of the materials is studied in detail experimentally.

The effects are binned into two main catagories: optical (n&k changes on exposure and bake, non-conformal topography coverage) and kinetic (unintended exposure/deprotection/diffusion and chemical cross-talk between materials).

For the case studied here, the complex index of refraction for Resist 1 only changes slightly during processing, however large index changes were observed in the BARC layer before it is re-used for Resist 2. Resist 2 was found to largely planarize the topography created by the first material, however some detectable residual deformation of the upper resist 2 surface was detected.

The kinetic effects are ranked based upon magnitude change on CD and new physical models which described the observed phenomena are developed. The models predictions are then tested against independent double patterning results using the full experimental LLE process.

7973-21, Session 5

Improving double-patterning flow by analyzing diffractive orders interactions

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To print sub 22nm node features in the near future, current lithography technology has been facing some tool limitations. One possible solution to overcome these problems is to use double patterning (DP). The pattern split is the core of DP; two adjacent features must be assigned opposite colors corresponding to different exposures if their pitch is less than a predefined minimum coloring pitch. However, there exist pattern configurations for which features can not be assigned opposite colors. These configurations are flagged in a design as conflicts and must be resolved. In this work we focus on contact layer and contact conflicts. We propose an optical method based on diffraction orders analysis in the pupil plane to identify such conflicts. We show that our method permits us to detect forbidden orientations in a design and provide guidance to designers to resolve conflicts.

7973-22, Session 5

Spacer-defined double patterning for 20/15-nm logic BEOL technology

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In order to maintain the scaling trend in semiconductor devices beyond of the resolution limit of state-of-the-art water-immersion scanner (= 193 nm), we explore patterning of back-end-of-line (BEOL) of 20-nm and 15-nm node logic technology using spacer-defined double patterning. Key lithographic achievements such as printing minimum pitch of 64 nm and 56 nm, controlling CD uniformity, effective overlay, and line edge roughness (LER), and challenges in printing complex design, alignment/overlay marks and others will be discussed. In addition, full field and across-wafer process performance up to integration levels that encapsulate lithographic patterning, etch, metallization and CMP will be accessed together. Finally, the feasibility of spacer-defined double patterning into high-volume manufacturability is discussed.

7973-23, Session 6

Accuracy and performance of 3D mask models in optical projection lithography

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Different approaches were used to model the light diffraction from typical mask structures such as periodic contact hole arrays and line endings. In the Kirchhoff approach the mask is considered to be infinitesimally thin and the diffracted light is computed by means of scalar diffraction theory. In contrast, rigorous electromagnetic field (EMF) modeling takes the complete information of the topography of the mask and its material properties into account to solve Maxwell's equations for the three-dimensional space. Decomposition techniques allow for a reduction of a 3-D problem to several 1-D and 2-D problems.

An important aspect of mask modeling is the consideration of spatial coherence. Modern lithographic methods use off-axis illumination (OAI) techniques. The mask is illuminated by a spectrum of mutually incoherent plane waves. Using the Hopkins assumption, the diffraction spectrum is evaluated only for the vertical incidence. Diffraction orders of obliquely incidence angles are approximated by shifting that spectrum accordingly. Without the Hopkins assumption, the diffraction spectrum of each

incident wave is computed through rigorous EMF models.

All simulations in this work were done for water immersion lithography at a wavelength of 193 nm. Both the illumination conditions and the mask feature sizes were optimized to achieve the best lithographic performance for given target sizes and numerical apertures. The resulting aerial images were evaluated in terms of lithographic process windows. The Fraunhofer IISB lithographic software Dr.LiTHO was employed for all simulations in this paper.

In order to identify the most appropriate mask model for a given accuracy requirement, the mask models discussed here are compared in terms of their process windows. The most accurate model -rigorous EMF simulation without Hopkins' assumption- is used as a reference. The performance of the different mask models is evaluated by means of a relative error function that represents the difference between the considered model and the reference model.

Pupil filtering techniques are applied to improve the accuracy of less rigorous but more efficient mask models. The aim of this work is to minimize the difference between mask models by introducing Jones pupils. The Jones pupil covers amplitude, phase and polarization effects which are introduced by the mask. The validity of this technique for different feature sizes, shapes and illumination conditions is investigated.

7973-24, Session 6

Accounting for mask topography effects in source-mask optimization for advanced nodes

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It had been shown that source-mask optimization with pixilated free-form illumination can improve the process window, contain the mask error sensitivity impacts and consequently improve the process robustness. It is also known that mask topography effects need to be accounted for advanced node RET/OPC solutions, in particular to ensure improved CD accuracy and side lobe printing predictability. In general, accounting mask topography in source-mask optimization is fundamentally challenging due to the time consuming nature of rigorous 3D simulations. Empirical fast 3D mask models, on the other hand, requires calibration against experimental data or rigorous simulations from a predefined illumination source. In this paper, we will present a comprehensive study of applicability of a fast 3D mask model in the context of source-mask optimization. We will compare the Kirchhoff and 3D mask models against rigorous 3D simulation and wafer data in the context of customized source and mask optimization. This comparison will include process metrics such as depth of focus (DOF), exposure latitude (EL), mask error sensitivity, and source changes. In addition, polarized illumination is widely used to enhance the process window for advanced nodes. However, a strong mask topography effect is introduced by polarized illumination sources. It is important to take this effect into account when investigating the process window of polarized illumination maps. We quantify the effect of considering polarization information in source and mask optimization with both 3D and Kirchhoff mask models.

7973-25, Session 7

Improved fab CDU with FlexRay and LithoTuner

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As the technology node continues to shrink, the need to match a population of scanners in a fab increases. By matching a population of scanners, the total CDU of the fab improves which leads to better device yield. In this paper, FlexRay illumination and LithoTuner applications are used to reduce the CD error. Two use cases are studied. The first use case is matching a XT:1950i with FlexRay illumination to a XT:1700i with a Diffractive Optical Element (DOE) illumination. The second use case is eliminating hotspots on XT:1950i with FlexRay illumination, and thereby reducing the CD error on wafer relative to target. In both use cases, the reduction of CD error is verified through wafer exposures at the Albany Nanotech facility.

In the first use case of XT:1950i FlexRay to XT:1700i DOE matching, the matching was peformed with LithoTuner Pattern Matcher FullChip (PMFC) for two illumination sources, annular and cquad. A reference model for each illumination is created and the model sensitivity to changes in optical parameters are determined. These parameters include the NA, dose, and illumination. From the parameter sensitivity, the XT:1950i scanner is tuned to match to the XT:1700i. For FlexRay illumination there are two types of parameters in the source that are tuned. In one set of parameters, sigma-in and sigma-out are tuned to mimic the type of changes possible for DOE illumination. In the other set of parameters, the source is treated as a freeform source and more aggressive illumination changes are allowed. The CDU results for both types of illumination changes are reported through simulation and verified with wafer exposure.

In the second use case hotspots were reduced by using LithoTuner Design Hotspot Fix (DHF). The FlexRay illumination is tuned to fix hotspots from OPC errors or from reticle manufacture errors. On the XT:1950i, a reference model is created and possible design hotspots are detected by running a lithography manufacture check through Tachyon LMC. The FlexRay illumination is tuned to eliminate these hotspots. The elimination of hotspots are reported through simulation and verified with wafer exposure.

7973-26, Session 7

Optical proximity stability control of ArF immersion clusters

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Once a process is set-up in an IC manufacturers' fabrication environment, any drift in the proximity fingerprint of the cluster will negatively impact the yield. In complement to the dose, focus and overlay control of the cluster, it is therefore also of ever growing importance to monitor and maintain the proximity stability (or CD through pitch behavior) of each cluster.

In this paper, we report on an experimental proximity stability study of imec's XT:1900i cluster for a 32 nm poly process from four different angles. First, we demonstrate the proximity stability over time by weekly wafer exposure and CD through pitch measurements. Second, we verify that proximity is maintained through the lot when applying Lens Heating Correction. In a third approach, the stability over the exposure field (intra-field through-pitch CD uniformity) is investigated. Finally, we also perform proximity matching to maintain a stable proximity behavior from tool to tool.

Monitoring and maintaining the scanner's optical proximity through time, through the lot, over the field, and from tool-to-tool, involves extensive CD metrology through pitch. In this work, we demonstrate that fast and precise CD through pitch data acquisition can be obtained by scatterometry (YieldStar S-100), which significantly reduces the metrology load.

The results of this study demonstrate how scatterometry enables thorough optical proximity control in a fabrication environment.

7973-27, Session 7

Scanner matching using pupil intensity control between scanners in 30-nm DRAM device

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It is impossible to make the perfectly identical pupil shape between scanners. The problem is how much of an effect the pupil shape difference between scanners will have upon the pattern CD difference on real wafers. According to the recent dramatic acceleration in dimensional shrink of memory devices, the pattern CD difference between scanners caused by pupil mismatch has negatively influenced the electrical performances of memory devices and process margin. It will be a burden to the memory chip makers who are forced to shrink the device technology node for the cost reduction of mass production.

In order to reduce scanner mismatch, the scanner manipulators such as inner sigma, outer sigma, and NA (Numerical Aperture) have been frequently used so far through modeling and exposure condition split. At some point, it was not enough to reduce the scanner mismatch with only NA, sigma conditions and there is also a limit to use a variety of sigma range.

In this work, the matching performance using pupil intensity control based on modeling has been evaluated for the layer of sub-3x nm technology memory device. The reference scanner was ASML XT 1900i, and the TBM (to be matched) scanner was ASML NXT 1950i. It had been confirmed before the matching process there are pupil shape mismatch and the pattern CD difference derived from it between two scanners. It was possible by comparing the extracted pupil parameters from the measured source maps using PFM (Pupil Fit Model). The matching process was based on the model which is calibrated by the measured CD data from the wafer exposed in different pupil shapes. In previous work, it was published that some pupil parameters are critical to CDs of some special kind of patterns, but it couldn't still give us how to manipulate the parameters. This study now introduces the way to minimize the electrical performance difference between memory devices which are produced from different scanners by controlling not only scanner knobs but also pupil intensity.

7973-29, Session 8

Solutions for 22-nm node patterning using ArFi technology

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ArF immersion lithography will be the main candidate for lithography patterning at the 22nm node. For both logic and memory type applications, double patterning techniques have to be applied to reach design pitches well below 70nm. In the lithography this combines aggressive imaging at low k1 (0.28... 0.31) and aggressive absolute CDU requirements (approximately 6-10% of nominal CD) of 1.5..2nm 3 . We will look into the lithography requirements to achieve such aggressive CDU numbers and will discuss solutions for achieving the required level of intrafield, interfield, wafer-to-wafer and scanner-to-scanner CD variations. An example is shown in Figure 1 for the intrafield contribution. The intrafield CDU, as investigated after litho mainly comprises contribution of scanner and reticle CD variations. While DoseMapper is capable of and established for correcting low-order variations across the exposure field, sometimes steep CD gradients are observed, which would require a high-frequent spatial dose profile. In the example of Figure 1, the CD fingerprint without any corrections (left fingerprint) shows a rather smooth CD variation in the center of the exposure field and a CD drop at the edge. After applying DoseMapper, the CD variations in the center of the exposure field have been reduced. However, at the edge the CD has been overcompensated, therefore not leading to a net CDU gain. Applying a high-frequent spatial dose profile can both compensate the smooth CD variations in the middle and the steep CD drops at the edge and gives a CDU improvement of 21%.

Figure 1: observed CD fingerprint across the exposure field after litho.

Left: measured without any dose corrections, 3sigma=1.8nm

Middle: measured after applying DoseMapper, 3sigma=2.0nm

Right: measured after applying higher order dose correction, 3sigma=1.4nm.

For the across wafer and wafer-to-wafer performance we will demonstrate improved individual scanner stability with respect to focus and overlay and its link to CDU. Finally, the enhancements in scanner-to-scanner matching will be demonstrated in terms of CDU improvement

7973-30, Session 8

Characterization and control of dynamic lens heating effects under high-volume manufacturing conditions

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Scanner manufacturers continuously increase the throughput of exposure tools, while ever-decreasing dimensions of chip features keeps requiring tighter process controls. Under high volume manufacturing conditions, absorption of exposure light in the projection optics of the scanner will cause slight temperature rise in the lens materials, and induce aberrations due to changes in refractive index and expansion of lens materials. These lens heating (LH) effects can be compensated by adjustable lens elements and dedicated manipulators.

This paper addresses calibration, prediction, and correction of LH effects on 1.35NA ASML scanners, and aims to:

- provide thorough experimental proof of LH correction by comparing 'hot - cold' wafer CD data.

- demonstrate the applicability of a dynamic (i.e. through batch) LH model for computational characterization and control of design-specific lens heating response.

- assess the effects induced by non-standard source shapes, such as generated by FlexRayTM freeform illumination, and their correction potential.

Precise control of LH effects requires the application specific calibration of the exposure system for each critical process layer. As a basis in this work, the correction of the hot-state aberration levels and their impact on CD is experimentally demonstrated for two different user relevant and LH sensitive illumination conditions. For different mask features, it is shown how the CDs over the full exposure slit are controlled throughout the heating of the lens.

A lens heating modeling suite has been integrated on ASML-BRION's Tachyon computational litho platform, which enables simulation of LH effects over time during regular lot exposure and characterization of the correction potential of different tool configurations.

Integration on Tachyon also directly facilitates simulation and analysis of impact on full chip CDs due to any LH residuals. Furthermore, the modeling enables off-line calibration; i.e. the simulated lens heating response for any specific reticle layout and exposure setting can be loaded to the scanner for precise application-specific LH compensation without requiring calibration of the actual reticle on the exposure tool.

The paper evaluates the lens heating model by comparison against the above and other experimental data (wave front and wafer CD).

Further LH experiments and simulations include an assessment of hot-state aberrations for a variety of freeform illumination cases, which can conveniently be obtained on ASML scanners equipped with a FlexRayTM

illuminator. Such variety of non-standard illumination shapes consists of sources with non-YX poles (e.g. rotated dipole), XY asymmetric poles, or pixelated sources originating from source-mask optimization (SMO) with varying pupil fill factors. Multiple cases are examined in terms of impact on aberration type and level, and their correction capabilities.

In summary, this work demonstrates that control of lens heating effects at the leading edge of immersion lithography can be obtained by modeling techniques next to technical solutions in the exposure tools.

7973-31, Session 8

An aberration control of projection optics for multiple-patterning lithography

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“High throughput with high resolution imaging” has been key word for multiple patterning lithography. In order to achieve high throughput and high resolution simultaneously, the management of thermal aberration due to projection lens heating becomes very important. The aberration causes the CD drift and overlay error. In case of off-axis illumination for resolution enhancement technique (RET), the aberration management is the most critical issue.

We have developed new aberration control system. It consists of high response adaptive optics and a measurement system. Regarding adaptive optics, 2-theta wavefront compensator (2TC) is constructed with the deformable mirror and high accuracy piezo-driven hardware in the projection lens. This unit can work to control the 2 theta wavefront with the specific orientation angle (ex. Z5 and Z6 of Zernike terms) shot-by-shot. Previously, we developed an adaptive optics using the thermal energy with infra-red irradiation, which was called IAC. It has worked to control the thermal aberration, so far. However, the lithography for multiple patterning requires high power exposure and switching of illumination condition. Under this situation, the adaptive optics using the thermal energy has drawback, which is slow response due to thermal transmission. Our new quick adjustment system with piezo-driven deformable mirror has the benefit for the aberration optimization at the timing of illumination switching, which requires the perfectly different aberration control, as the x-dipole exposure after the y-dipole exposure. Additionally, the side effect of aberration adjustment with 2-theta wavefront compensator has been improved comparing with IAC. This will help to obtain the imaging performance for multiple patterning layers. The measurement system to monitor thermal aberration during exposure has been realized on scanner. The measurement will be done several times in the lot. Therefore, we can control the thermal aberration with closed-loop system to improve the adjustment accuracy, compared to our current open-loop aberration control.

In this paper, we will show practical performance of the lens heating with dipole illumination for finer patterning and confirm that our new control system can reduce the astigmatism drift (V-H Focus difference) due to the 2-theta of wavefront drift. We will also show that we can keep the imaging performance even just after the illumination switching.

7973-32, Session 9

Fine calibration of physical resist models: the importance of Jones matrix, laser bandwidth, mask error, and CD metrology for accurate modeling at advanced lithographic nodes

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The availability of accurate and predictive physical resist models is seen as one enabler for fast and efficient exploration of new technology layers, especially if fully qualified OPC models are not yet available due to the early pre-production stage of the technology development. The continued shrinking of the minimal feature size down to limit of optical/resist resolution requires that physical resist models cover the prediction for a wide spectrum in the design space ranging from minimal features at the smallest pitch to various large features at relaxed pitch. Therefore, many effects of optics and metrology, which are negligible for large feature sizes, should be covered in physical resist models to describe real lithographic process accurately. Usually, resist model calibration - based on measured wafer CDs from test patterns - must be performed to capture the relevant effects and thus it is indispensible to understand the contribution of components of optics, mask and CD metrology to the resist model calibration.

In this paper, we discuss the accuracy of resist model calibration under various aspects. The study is done based on an extensive OPC dataset including hundreds of CD values obtained with immersion lithography for the below 30 nm node. We address imaging aspects such as the role of Jones matrices, laser bandwidth and mask bias. Besides we focus on the investigation on metrology effects arising from SEM charging and uncertainty between SEM image and feature topography. For theses individual contributions (Jones matrix, laser bandwidth, mask error and CD metrology) we perform a series of resist model calibrations to determine their importance in terms of relative RMS (root mean square value of the deviation between simulated and measured CD data) as summarized for our particular technology layer in Figure 1. With respect to Jones matrix for example, we also discuss the separation of aberration and apodization effects into the lithographic lens and pellicle specific effects, both found to be similarly important. Furthermore, we discuss the methodology how to compare and correlate a simulated CDs with a measured CD obtained from a top down SEM CD measurement. In this case, there are two things to be considered: one is how to include the difference between simulated CDs and SEM CDs obtained by SEM scan line signal and the other is how to add CD shrinkage (resist slimming) effects into lithography simulations. Currently, the former problem is solved by adopting a CD bias during resist model calibration and the latter one is taken into account by correcting the measured SEM CDs based on a correlation table obtained from an independent experiment. As seen in Figure 1, for our model the dominant contributor is CD metrology arising from CD shrinkage by SEM charging. The impact of Jones matrices, laser band width and mask bias is 14%, 22% and 14%, respectively and for the below 30 nm node they all are not negligible for accurate resist model calibration.

7973-33, Session 9

Criteria of photomask line-edge roughness for computational lithography and EUV lithography

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As semiconductor features shrink in size and pitch, there are strong needs for an advanced lithography which has better resolution. To overcome the difficulties of low k1 process, there are extensive developments for advanced lithography technologies such as computational lithography and EUV lithography. These advanced lithography technologies require more complex mask layout and the tight control of mask patterning.

Here, we have investigated the effect of mask line end roughness (LER) on wafer patterning in computational lithography and EUV lithography based on diffractive optics simulation. In computation lithography, the round pattern of mask layout results in the amplified LER due to the shot segmentation for VSB e-beam writer. Furthermore, the EUV lithography has the enhanced LER transfer ratio from mask to wafer because of its small wavelength. Based on these circumstances, we present the criteria of photomask line edge roughness for advanced lithography by the simulation and error budget analysis.

7973-34, Session 10

Stability and calibration of overlay and focus control for a double-patterning immersion scanner

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Spacer technology is already being used in actual production and looking ahead to the future of lithography, quadrupling spacer and pitch splitting double patterning (DP) will be the most likely litho solutions beyond the 22 nm node. However, to enable these advanced technologies, the overlay and CD control requirements for lithography tools are becoming more stringent.

To achieve the 2 nm overlay accuracy required for double patterning, we have introduced the NSR-S620D immersion scanner that employs an encoder metrology system. By incorporating sophisticated encoders, scanner overlay performance has been dramatically improved to less than 2 nm, and within wafer focus uniformity below 20 nm has been demonstrated via the PSFM test method. The NSR-S620D has been implemented in the production of NAND flash and MPU. In this paper we will provide an update on the latest performance of the tool, with an emphasis on overlay and focus control.

The key challenges for an encoder metrology system include both its stability as well as the methods of calibration. In the case of the advanced NSR-S620D hybrid metrology design, the absolute coordinate system of the encoder metrology can actually be calibrated by being compared to the coordinate system of the interferometer. This is essential as an absolute grid is needed for effective overlay matching between litho tools. In addition, with the S620D design, a drift in the encoder metrology system can also be calibrated wafer to wafer, as well as lot to lot. Such calibration is vital in achieving the necessary level of overlay stability for DP manufacturing.

This work will show the calibration results of the absolute grid and provide an analysis of overlay stability. Overlay matching results between the tools will also be shown, validating that the NSR-S620D delivers the sufficient level of accuracy and stability for the production phase of double patterning.

7973-35, Session 10

Advanced CDU improvement for 22 nm and below

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ArF water immersion lithography is expected to be used down to the 22nm hp node or below. However, such advancements in technology nodes have lead to extremely small process margins. This necessitates more accurate means of process control. CD uniformity in resist image is affected by many sources. In the case of the exposure tool, CD error on the reticle, exposure dose and focus errors are the key factors. For the resist process, heterogeneity of the stacked resist film thickness, post exposure bake (PEB) plate temperature, as well as development all have an impact. Further, the process wafer also has error sources that include under-layer uniformity or wafer flatness. Fortunately the majorities of these uniformities are quite stable in a volume production process and can be compensated using simultaneous exposure dose and focus control of the scanner.

A technique to calculate exposure dose and focus correction values simultaneously from the measured resist image feature was reported previously [1]. Further, a demonstration of correction loop using a neural network calculation model was reported in SPIE 2010 [2], and the corrected CD uniformity was less than 1.5 nm (3 sigma) within a wafer. In this paper, we will report the latest CD uniformity correction results using the the NSR-S620C ArF immersion scanner (fig.1), with correction values estimated by scatterometry, CD SEM and an optical macroscopic inspection tool.

The method of correction using CD SEM is newly suggested. A Maximum of nine parameters extracted from the resist profile are used in this correction. In general, the CD variation of an isolated line pattern caused by focus error is more sensitive than that of dense pattern. Thus, we estimate the focus error from the isolated pattern, with the dose error estimated from both isolated and dense patterns. Further, using the Nikon AMI-3500 (Automatic Macro Inspection) system, we found it is possible to successfully extract the dose and focus errors using the optical image contrast deviation of resist pattern. Since the AMI single wafer measurement time is only a few minutes, this method's fast turnaround time is a compelling factor for an efficient correction loop.

The Nikon CDU Master then derives the optimal control parameters for each compensation function in the scanner using the exposure dose and focus correction data with the NSR-S620 having the capabilities to also control higher order dose and focus distribution. This high degree of controllability ultimately enables precise correction of the complicated CD error distribution that is caused by heterogeneities in the process.

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7973-36, Session 10

Combined overlay, focus and CD metrology for leading edge lithography

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As the leading edge lithography is moving to 22-nm design rules, control and setup replace resolution as the driver and enabler to meet remarkably tight process requirements. In addition, the way of thinking and executing setup and control is changing in four ways.

First, unusually tight process tolerances call for extremely dense spatial sampling of the wafer, which in effect means measurements at high throughput combined with high order modeling and corrections to compensate for wafer spatial fingerprint.

Second, complex interactions between scanner and process doesn't allow anymore separation of the error sources through traditional metrology approach which is based on using one set of metrology tools and methods for setup and another one for control scanner performance. Moreover setup and control of overlay is done independently from CDU which in effect leads to independent and conflicting adjustments to the scanner.

Third, traditional CD setup and control is based on focus and dose calculated from their CD-response and not from direct measurement of their direct effect on pattern profile which allows a clean and orthogonal deconvolution of focus and dose variations across wafer.

Fourth, scanner setup and control has to take into consideration the final goal of lithography, which is accurate printing of a complex pattern describing a real device layout. This points toward introduction of a new setup and control metrology step: measuring-to-match scanner 1D and 2D proximity.

In this paper we will describe the principle of the YieldStar metrology tool and present results on overlay, CD and proximity scanner setup and control, demonstrating performance improvements based on the new way of thinking. YieldStar-200 is a new, high throughput metrology tool based on a high aperture scatterometer concept. The tool can be used as stand-alone as well as integrated in a processing track and is suitable for combined XYZ measurements of overlay, focus, dose, CD and proximity.

By using a technique[1, 2, 4] to de-convolve dose and focus based on the profile measurement of a well characterized process monitor target, we show that the dose and focus signature of a high NA 193nm immersion scanner can be effectively measured and corrected. A similar approach was also taken to address overlay errors using the diffraction based overlay capability [3] of the same metrology tool. We demonstrate the advantage of having a single metrology tool solution, which enables us to reduce dose, focus and overlay variability to a minimum non-correctable signatures.

This technique, makes use of the high accuracy and repeatability of the YieldStar tool, provides a common reference of scanner setup and user process control, and most important, the setup wafers are exposed in the same way as in production resulting in more accurate feedback to optimize the tool performance. Using ASML's YieldStar in combination with ASML scanners, allows for a direct link from the metrology tool to the system settings, ensuring that the appropriate system settings can be easily and directly updated.

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7973-56, Poster Session

Hotspot repair using ILT

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For low k1 lithography the resolution of critical patterns on large designs can require advanced resolution enhancement techniques for masks including scattering bars, complicated mask edge segmentation and placement, etc. Often only a portion of a large layout will need this sophisticated mask design (the hotspot), with the remainder of layout being relatively simple for OPC methods to correct. In this paper we show how inverse lithography technology (ILT) can be used to correct selected regions of a large design after standard OPC has been used to correct the simple portions of the layout.

The hotspot approach allows a computationally intensive ILT to be used in a limited way to correct the most difficult portions of a design. We will discuss the most important issues such as: model matching between ILT and OPC corrections; transition region corrections near the ILT and OPC boundary region; mask complexity; total combined runtime. We will show both simulated and actual wafer lithographic improvements in the hotspot regions.

7973-57, Poster Session

Fast algorithm for quadratic aberration model based on triple cross-correlation operator

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With recent progress in resolution enhancement techniques, understanding the effects of wavefront aberration represented by Zernike coefficients on imaging is crucial in optical lithography. The approximate linear response of Zernike coefficients to image intensity and critical dimension (CD) has been widely used, by supposing that the aberration coefficients are small and the higher order terms are ignored. Flagello et al proposed a quadratic aberration model which is a natural extension of the linear model by taking into account interactions among individual Zernike orders. The quadratic aberration model has been tested and verified in many applications, such as aberration sensitivity analysis, phase wheel target aberration monitoring, CD or depth of focus (DoF) uniformity and illumination optimization. However, the effects of Zernike coefficients on partially coherent imaging are usually obtained by extensive experiments or lithographic simulators, due to the complexity of the model expression. The calculation of the quadratic aberration model directly by analytical expression is time consuming and thus impractical for in-situ measurement or characterization. Therefore, a real-time analysis and fast algorithm for the quadratic aberration model is necessary.

In this paper, we propose a novel concept named triple cross-correlation operator (TCO), which is defined as the integral product of the three functions where two are shifted in different direction at the same time. It is a bilinear extension of cross-correlation for two arbitrary shifted signals. In fact, according to the concept of transmission cross coefficient (TCC), TCC which involves the shifted pupil function and its conjugation then multiplying the source function, can be considered as an exceptional case of TCO. We also develop a fast algorithm to simulate the quadratic aberration model simplified by TCO, by convert the expression of the complicated quadratic aberration model into an algebraic sum of TCOs. The TCO based algorithm is similar to the conventional TCC algorithm, but it overcomes the restriction that the two shifted signals must be the same pupil function in TCC. Therefore, the fast algorithm is expected to achieve real-time simulation in optical lithography and will be more prominent in the quadratic aberration model calculation. Simulations were performed by the proposed TCO based algorithm with different input Zernike aberrations for binary and phase shift masks of multiple pitches and orientations.

As an instance, Figure 1 and Figure 2 show the aerial images each of which was decomposed into an unaberrated term, linear terms and quadratic terms, with inputting odd type aberrations (Z7 and Z10) and even type aberrations (Z12 and Z17) respectively. From a lot of simulation results for binary and phase shift masks with multiple pitches and orientations, the proposed TCO based algorithm are demonstrated to successfully provide an efficient and accurate approach for revealing interactions among different Zernike orders under partially coherent illumination. Because the TCO based algorithm is able to deal with such interactions, the proposed approach will have further applications in cubic model or higher order model in the future. It is fully expected that this TCO based quadratic aberration model and algorithm will provide a practical method for the in-line image detection and characterization in lithographic tools.

7973-58, Poster Session

Choosing objective functions for inverse lithography patterning

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As Moore's law marches on and semiconductor manufacturers make the push towards the 22nm technology node and beyond, the challenges faced by microlithography are ever increasing. The need to print such small features using 193nm illumination -- which is way beyond the Rayleigh diffraction limit -- has made resolution enhancement techniques (RETs) mandatory.

Optical Proximity Correction (OPC) is a resolution enhancement technique that modifies mask layout designs in order to minimize their distortion when transferred to silicon. A good OPC implementation may prove sufficient for a given process technology, precluding the need for a more expensive alternative, like Double Patterning, Alternating Phase Shift Mask (AltPSM), Immersion Lithography and so on. Evidently, OPC has clear advantages in efficiency and manufacturing cost. Segment-based OPC, in particular, is the most-widely-used RET and has been a standard industry practice since the 90nm node. Because segment-based OPC only modifies edges already present in the design layout, it is relatively easy to implement, particularly in iterative algorithms. However, as the need for stronger OPC increases, this simplification has become a major limitation. As the reachable solution space lies strictly in the vicinity of the original layout, segment-based OPC is often not expressive enough and does not exploit the full range of possible mask configurations to get the best possible pattern fidelity and image contrast.

To overcome this limitation in advanced CMOS processes, inverse lithography are proposed to promise better patterning fidelity than conventional mask correction techniques due to the nature of reverse mask optimization. As a general rule, the success of any particular IL algorithm depends strongly on the nature and form of its cost function which is constituted by various objective functions. A properly designed cost function and algorithm can help avoid issues such as getting trapped in local minima, slow convergence, mask discontinuities, etc.

In the literature, the most-commonly used objective functions have traditionally been the aerial and resist images. The former compares the optical intensity distribution on the photoresist (after exposure but before developing) to a desired target intensity, while the latter compares the developed photoresist profile to the desired outcome for a given mask. Other cost functions, such as edge contours, aerial image contrast, and mask error enhancement factor (MEEF), have also been proposed and can be customized to satisfy strict technological specifications.

In this paper, we investigate the impacts of various objective functions and their superposition for the cost function of inverse lithography patterning using a generic image-gradient decent approach. We investigate the most commonly used objective functions, such as the 1) resist image, 2) aerial image, and we have also derived a formulation for 3) aerial image contrast.

7973-59, Poster Session

Physical conversion of a general Mueller matrix into the respective Jones matrix applicable to the calculation of lithographic images

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The whole polarimetry for immersion lithography equipment that comprises Stokes polarimetry of illumination and Mueller matrix polarimetry of projecting optics had been established[1-5]. It was found that illumination and projecting optics were slightly different from our expectation. These differences might affect optical proximity correction (OPC) and source mask optimization (SMO). However, no lithographer can desterilize parameter sets from the whole polarimetry for the use of lithography calculation because of their formats, Mueller matrix and Stokes parameters. Conventional lithography simulators require the Jones matrix only.

When the illumination was partial polarization or the projecting optics was partially polarizing or partially depolarizing, Jones calculus cannot deal with such optical systems. Mueller calculus is needed for the case that involves polarization-depolarization and depolarization-polarization translations. However, previous works showed that an actual depolarized illumination was somewhat polarized in the y direction and an actual catadioptric projecting optics was partially polarizing in the x direction.

On the other hand, if you took the aberration effects into the lithography calculation, you had to use Jones calculus. Therefore, for the lithography calculation with actual polarization as well as data actual aberration data, a special technique is required to handle these data.

This paper describes how to physically convert from a general Mueller matrix into Jones matrices and how to apply the physical conversion to the calculation of lithographic images. According to the Lu-Chipman decomposition[6], a general Mueller matrix can be decomposed into three matrices of a depolarizer, a retarder, and a diattenuator. The retarder doesn't influence on the un-polarization component, but on the polarization component. Therefore, a light is divided into the two components of un-polarization and polarization in the virtual projecting optics, and the two components are individually used for the image calculation. This method permits to use the actual polarization data to the lithography calculation.

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7973-60, Poster Session

Self-aligned triple patterning for continuous IC scaling to half-pitch 15 nm

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Sub-20nm (half-pitch) patterning poses tremendous challenges in lithography, materials, and process technologies for the semiconductor industry. Double patterning based on 193nm immersion lithography can drive the half pitch down to about 19nm. EUV, nano-imprint, and e-beam maskless lithography, all with various manufacturability challenges, will not be ready for high-volume manufacturing (e.g., NAND flash) in the near future. To meet the scaling timeline, a self-aligned triple patterning (SATP) technology is proposed.

The SATP process to enable line/space density tripling is shown in Fig. 1, wherein small APF lines/mandrels are patterned first. After that, sacrificial spacers (e.g., nitride spacers as shown in Fig. 1) are formed prior to structural spacers (e.g., oxide). Nitride spacers can be wet etched later by phosphoric acid (which does not attack APF and oxide), leaving mandrel lines and structural spacers, which results in a spatial frequency tripling.

The feasibility of SATP process has been demonstrated by carrying out experiment in both dry and immersion scanners. In Fig. 2, we show SEM images that were taken during different stages of a SATP process. In Fig. 3, SEM images of half-pitch 21nm and 16nm lines/spaces fabricated by a SATP process are shown. 16nm lines/spaces result is from our first immersion test wafer and further process optimization is needed. We can see that the lithography defined lines/mandrels have worse LER. Apparently, optical patterning of small lines in steps (2) and (3) of a SATP process is a non-trivial challenge and a major focus of our early-stage research is to develop an etching/trimming process that can pattern small lines of good quality. Novel ideas such as using low-energy ion implantation to shrink line CD and harden resist/BARC (to improve etching selectivity) have been investigated and the results will be reported.

The triple patterning technique (SATP) can drive (half-pitch) CD down to about 13nm. Moreover, the SATP bright-field features are separately defined by optical lithography (step (2)) and spacers (step (7)), thus SATP process can include arbitrary bright-field 2-D patterns (e.g., peripheral circuits) and lines/spaces within one mask. In general, SATP process can save significant costs, e.g., 1-2 masks & litho plus the following etch step for each critical layer containing both lines/spaces (possibly with multiple CDs) and 2-D features. For example, in NAND flash wherein SADP has been widely used, normally the dense arrays and peripheral circuits (including pads) are decomposed into two separate masks and totally 3 masks are needed for one critical layer. By a SATP process, we can combine dense arrays and peripheral circuits into one mask and totally only 2 masks are needed (see Fig. 4). As the peripheral circuits (containing iso and 2-D features) will be printed together with core/mandrel lines using C-Quad illumination, we shall study if SATP process works well under such illumination conditions for both 1-D array and 2-D patterns. Moreover, it is possible to apply SATP methodology into double (not triple) patterning to reduce mask number from 3 to 1 for one critical layer containing dense L/S array with pads and 2-D features (e.g., DRAM & NAND applications), as demonstrated in Fig. 5. All above possibilities are currently under investigation and the results in both test mask design and process integration will be reported.

7973-61, Poster Session

Sidewall spacer quadruple patterning for 15-nm half-pitch

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Despite the challenges in scaling below 20nm half-pitch, several NAND-Flash manufacturers are pursuing 15nm planar NAND technology nodes

within the near future. 25nm NAND-Flash parts have already begun production in 2010, and given the traditional 2-year cycle, 15nm should see pilot or mass production as early as 2014 by the manufacturing leaders. Using a brute-force patterning technique, such as sidewall spacer quadruple patterning (upon 120m pitch dry-ArF lithography) or sidewall spacer triple-patterning (upon 90nm pitch immersion-ArF lithography), we can extend optical lithography to 15nm half-pitch and demonstrate capabilities that can nearly meet the ITRS roadmap requirements for that technology and node.

In this paper, we conduct an in-depth review and demonstration of sidewall spacer quadruple patterning; including 300mm wafer level data along with a mathematical assessment of the various data pools for lines and spaces. By understanding which processes (lithography, deposition, and etch) define the critical dimension of each data pool, we can make predictions of CDU capability for the sidewall spacer quad patterning. Our wafer level demonstration shows capability to meet the NAND-Flash requirements for lines with CDU of 1.1nm (3 sigma) on 15nm half-pitch arrays, while space CDU is slightly trailing requirements with 2nm CDU (figure 1). The mean LWR is 2.2nm, however, 30% of the data is showing LWR less than 1.2nm (figure 1); we therefore believe that capability is present to meet the LWR requirement, and that a yield-up process is required to get all wafer sites matching the fundamental capability.

As the spacer quad-patterning pushes the pitch to extreme dimensions, the CD-SEM must also rise to the challenge and demonstrate edge fitting of these 15nm half-pitch features. Ultimately, the Verity 4i CD-SEM, demonstrated high measurement yield, during fully automated measurements, enabling accurate CDU measurements and automated sorting for the various data pools (figure 2).

7973-62, Poster Session

Spacer-defined double patterning for sub-20-nm half-pitch single damascene structures

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Double patterning techniques are of interest to overcome the lithographic patterning size limits and obtain sub 0.25 k1 feature densities. Self-Aligned Double Patterning or Spacer Defined Double Patterning (SDDP) is an attractive patterning scheme allowing for the definition of narrow lines at a reduced pitch, by forming spacers adjacent to a patterned template. After removal of the template material the line density is effectively doubled.

In this paper we discuss the spacer defined patterning approach for 20nm half pitch (HP) single damascene Cu interconnect structures using immersion lithography and show the capability of SDDP to further scale the feature sizes to 15nm half pitch using either EUV lithography or a double patterning (DP) approach based on immersion lithography.

Three masks are required to generate electrical test structures using SDDP. These are CORE, TRIM and PATCH. CORE defines one-dimensional dense lines at 40nm HP for spacer formation; TRIM makes large openings to cut the spacer loops away by etch; and PATCH defines bond pads and electrical connections with critical patches at 40nm HP.

To achieve 20nm HP structures we start from 40nm line/space structures patterned in resist using 1.35NA immersion lithography. This is followed by a combined trim and etch process to form 20nm lines with 60nm spaces in an amorphous carbon template layer, and then a conformal CVD nitride spacer deposition, a spacer etch and amorphous carbon removal, resulting in 20nm HP spacer structures.

Final results on wafers will be discussed, focusing on critical double patterning topics such as CD & overlay budget and line edge roughness (LER); and their impact on the electrical functioning of the back-end-of-line test structures.

The feasibility of extending the SDDP technique down to 15nm HP structures is also discussed. The 30nm line/space structures patterned in resist, required as a starting point for this exercise, will be patterned using EUV lithography or by a double patterning approach using immersion lithography.

7973-63, Poster Session

Recessive self-aligned double patterning with gap-fill technology

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In this paper, we present a recessive self-aligned double patterning (R-SADP) process enabled by the gap-fill technology that can double the density of both trench and via arrays.

A process flow to demonstrate how the via array density can be doubled by a R-SADP process is shown in Fig. 1. First, a stack of multiple layers (nitride/APF/oxide/nitride) is deposited on substrate as shown in step (1). Dense vias with 2.8F pitch (along the dashed line tilting at an angle of 45°, see Fig. 2) are printed first on resist using a lithographic process with 2F as the minimum resolvable pitch (in the horizontal direction). The resist pattern is transferred to the nitride/APF (hard mask) layer and then to the oxide/ nitride stack underneath with a dry etching. After this, the sacrificial oxide underneath the nitride layer is partially etched by an isotropic process (e.g., diluted HF or dry etch process), leaving the oxide width about 0.7F as shown in step (3). APF is then stripped in step (4) with a dry ashing process, and a gap-fill film is spun on in step (5) to fill the etched vias. A following trimming step (6) will expose the top of oxide such that HF solution can flow in to etch oxide. (It should be reminded that this oxide should be replaced by other material if we want to use flowable CVD oxide as gap-fill material.) Once oxide is completely removed, an array of cavities surrounded by the remaining gap-fill material is formed as shown in step (7). Finally, a dry etching will transfer the newly formed cavities to the nitride layer underneath, resulting in via density doubling as shown in step (8). Further transfer of this new via pattern from nitride to the substrate (e.g., APF hard mask) is possible.

Fig. 2 is a top-view cartoon that describes the sacrificial wet etching process (APF layer is ignored), showing how the shape of the added vias (and oxide as well) evolves and why they are self-aligned to the original vias. Moreover, a 1-mask process flow is proposed to simultaneously pattern dense lines/spaces with pads and 2-D features as shown in Fig. 3. The critical step is to create a gap-fill film thickness difference between the dense array and peripheral/blank areas in (5) such that only the top oxide lines in the array area are exposed after gap-fill trimming as shown in (6). Although BEOL trenches is used here for demonstration purpose, FEOL application is immediately possible by a trench-fill followed by CMP. This can significantly reduce the manufacturing cost of self-aligned double patterning if the concept is proved to work. Fig. 4 shows the SEM images of four selected steps in via process. It starts from a 52nm via pattern on resist (half pitch: 70nm) as shown in step (2), and achieves a final via pattern (on nitride) with 50nm half pitch as shown in step (8). Excellent control of recessive oxide CD with diluted HF is demonstrated by the image of step (4). In Fig. 5, we show the images of three selected steps in a R-SADP trench process (the last etching step (8) not completed yet). It starts from a trench array with 60nm half pitch, with some shrink techniques applied to pattern 30nm trenches (pitch: 120nm). The final half pitch is reduced to 30nm as shown in Fig. 5.

As a summary, using a R-SADP process, we have achieved 50nm (half pitch) vias using a dry 193 nm scanner (NA=0.93) which is capable of direct printing 70nm (half-pitch) vias (shrunk by a factor of 1.4). The feasibility of 30nm half-pitch trench patterning using a R-SADP process is also demonstrated and a 1-mask process flow to simultaneously pattern FEOL lines/spaces with pads plus 2-D features is proposed.

7973-64, Poster Session

Simplified self-aligned quadruple patterning toward half-pitch 10-nm patterning

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A novel self-aligned quadruple patterning (SAQP) technology is proposed and developed to overcome the challenges of continuous IC scaling down to 10nm. In a standard SAQP sequence, normally the spacer

forming process will be repeated separately such that the final spatial frequency is four times of what is defined by optical lithography. Forming spacers in two separate steps involves a lengthy process including CVD, etch, wet cleaning, etc.

The key innovation of this SAQP process is the lateral etching of sacrificial material, wherein diluted HF solution (or dry isotropic etch) is used to partially etch the sacrificial oxide at an uniform and controllable rate. After that, four self-aligned spacers can be simultaneously formed in every pitch, thus eliminating the need of two separate steps to create them. In Fig. 1, a cartoon of the simplified SAQP process example is shown. A stack of multiple layers (nitride/APF/oxide/Si/APF, APF: advanced patterning film) is first deposited on Si substrate in step (1). Trench patterns are printed first on resist using a lithographic process. The resist pattern is then etched into the top nitride/APF stack which is used as a hard mask to further transfer patterns to the oxide and Si layers underneath. After this, the sacrificial oxide underneath the top APF is partially etched by diluted HF (or by dry isotropic process), leaving the oxide width about ¼ of the original half pitch as shown in step (3). APF is then stripped in step (4) with a dry ashing process. The partial etching of sacrificial oxide allows us to form small oxide core lines self-aligned to the center of patterned amorphous Si. After depositing and etching back nitride as shown in steps 5 and 6, we can simultaneously create four nitride spacers in every (optically defined) pitch. The oxide core lines are then etched away by HF solution which etches nitride at a very low rate. After releasing the sacrificial oxide, a Si etching process with high selectivity to nitride is applied in step (8) to achieve self-aligned density quadrupling. Finally, the pattern can be transferred to APF layer which acts as a hard mask for general film stacks to be etched. Other process schemes with different materials are possible, e.g., using nitride as sacrificial material while oxide as spacers.

Fig. 2 is a top-view SEM image at step (4) showing small oxide lines are placed on the top & at the center of Si structures. Fig. 3 shows that using above self-aligned density quadrupling process, we can simultaneously create four nitride spacers in one (optically defined) pitch. In Fig. 4, we have demonstrated the feasibility of using above SAQP process to pattern 20 nm lines/spaces with a starting half pitch of 80nm (printed by 193nm dry scanner). It might be possible to extend this technology to 10nm (half-pitch) patterning with a 1.35NA immersion scanner. We also identified a critical CD bias issue that needs more research effort. The (dry) etch resistance of the spacers at different levels varies significantly in our process, which leads to our observation that post-etch CD of upper spacers is larger than that of bottom spacers. Apparently, further process optimization to overcome this issue is needed.

7973-65, Poster Session

Influence of the illumination source on model-based SRAF placement

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Sub-Resolution Assist Features (SRAFs) have been extensively used to improve the process margin for isolated and semi-isolated features. It has been shown that compared to rule-based SRAFs, model-based placement of SRAFs can result in better overall process window. Various model-based approaches have been reported to affect SRAF placements. Even with model-based solutions, the complexity of two-dimensional layouts results in SRAF placement conflicts, producing numerous challenges to optimal SRAF placement for each pattern configuration. Furthermore, tuning of SRAF placement algorithms becomes challenging with varying patterns and sources [1-3].

Recently, pixilated source in optical lithography has become the subject of increased exploration to enable 22/20 nm technology nodes and beyond. Optimization of the illumination shape, including free-form pixilated sources, has shown performance gains, compared to standard source shapes [4-6]. This paper will demonstrate the influence of such different free-form sources as well as conventional sources on model-based SRAF placement. Typically in source optimization, the selection of the optimization patterns is exigent since it drives the source solution. Small differences in the selected patterns produce subtle changes in the optimized source shapes. It has also been previously reported that SRAF placements are significantly dependent on the illumination [1]. In this paper, the impact of changes in the design and/or source optimization patterns on the optimized source and hence on the SRAF placement is reported. Variations in SRAF placements will be quantified as a function of change in the free-form sources. Lithographic performance of the different SRAF placement schema will be verified using simulation.

7973-66, Poster Session

Comparison of clear-field and dark-field images with optimized masks and illuminators

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Comparison of Clear-Field and Dark-Field Images with Optimized Masks and Illuminators

Robert Sinn, Paul Rissman, and Bob Gleason

Clear-field photo-masks offer significant advantages over dark-field photo-masks for some important classes of target patterns, including small isolated features and dense arrays of contacts. Prior work has established that images of clear-field patterns have higher contrast and lower MEEF1, even though the poorer contrast of negative tone development diminishes the inherent optical benefits. This work compares lithographic performance of clear-field and dark-field images when mask patterns and illuminators are optimized for respective mask tones. Because our purpose is to study optical behavior, we compare computed images without resist models. In order to explore performance limits, we do not constrain optimized masks or illuminators to limit their complexity.

The numerical optimization algorithm used in this work minimizes an objective function with weighted terms corresponding to dose, defocus, and mask bias. It therefore yields greater differences between mask and illuminator solutions for different mask tones, as compared to methods based on diffraction spectra when applied to complementary targets. Some of the differences are easily understood in context of the physics of image formation. Influence of partial coherence, and the distance over which SRAFs are effective vary with tone. Perhaps less obvious, the optimization process drives other differences, particularly when the optimum illuminator is a compromise over a set of patterns with different characteristics. The set of patterns chosen for optimization usually contains some for which dark-field contrast is very low, so the algorithm seeks a solution that minimizes variations due to dose and mask bias for these patterns. Because the solution for the illuminator applies to all patterns, even those not subject to the inherent lower contrast of dark-field imaging are affected. On the other hand, using the same target patterns and weighted image conditions, higher contrast implies that defocus terms will exert more influence on clear-field optimization. In such a case, the SMO process has coupled defocus performance into the comparison of clear-field and dark-field imaging. Even when there is no inherent benefit in clear-field defocus, it can be better because the solution did not have to compromise it to improve contrast for a subset of the target patterns.

Because the optimum masks and illuminators are different for clear-field and dark-field imaging, it is necessary to include optimization in the comparison so that conclusions are not biased. In this work, we examine classes of test patterns that cover typical layouts with poor process margins. These include finite arrays of contacts with different pitches and orientations, and ends of narrow lines close to other features. We compare contrast, MEEF, and depth of focus for optimized clear-field and dark-field masks, matched to their optimized illuminators.

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Printing the Metal and Contact Layers for the 32 and 22 nm Node: Comparing positive and negative Tone Development Process, Optical Microlithography XXIII, Proc. of SPIE Vol. 7640, 764011

7973-67, Poster Session

Custom source and mask optimization for 20-nm SRAM and logic

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Custom Source and Mask Optimization for 20nm SRAM and Logic

The 20nm generation for logic will be challenging for optical lithography, with a contacted gate pitch of ~82nm and a minimum metal pitch of ~64nm. A gridded design approach with lines and cuts has previously been shown to allow optimizing illuminator conditions for critical layers in logic designs.[1] The approach has shown good pattern fidelity and is expected to be scalable to the 7nm logic node. [2,3,4]

A regular pattern for logic makes the optimization problem straightforward if only standard cells are used in a chip. However, modern SOC's include large amounts of SRAM memory as well. The proposed approach truly optimizes both, instead of the conventional approach of sacrificing the SRAM because of logic layouts with bends and multiple pitches.

We consider a design with the logic and SRAMs unified from the beginning. In this case, critical layer orientations as well as pitches are matched and each of the layers optimized for both functional sets of patterns.

The layout for a typical standard cell using Gridded Design rules is shown in Figure 1a. The Gate electrodes are oriented in the vertical direction, with Active regions running horizontally. Figure 1b shows a group of SRAM bit cells designed to be compatible with the logic cell. The Gate orientation and pitch are the same.

Illuminator optimization results will be presented for the co-optimization of critical layers for both the logic and SRAM cells. Source-Mask Optimization (SMO) method used can optimize the illumination source [5] and mask for multiple patterns to improve the 2-D image fidelity and process window while controlling the mask sensitivity. It can incorporate the design intensions that are implied by Gridded Design rules. SMO will be done to balance complexity of the source and the complexity of the mask (OPC & MBSRAFs). A flexible approach to the optimization will be introduced.

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7973-68, Poster Session

Enabling 22-nm logic node with advanced RET solutions

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The 22-nm technology node presents a real breakthrough compared to previous nodes in the way that state of the art scanner will be limited to a numerical aperture of 1.35. Thus we cannot "simply" apply a shrink factor from the previous node, and tradeoffs have to be found between Design Rules, Process integration and RET solutions in order to maintain the 50% density gain imposed by the Moore's law. One of the most challenging parts to enable the node is the ability to pattern Back-End Holes and Metal layers with sufficient process window. It is clearly established that early process for these layers will be performed by double patterning technique coupled with advanced OPC solutions.

In this paper we propose a cross comparison between possible double patterning solutions: Double Dipole Lithography (DDL), Pitch Splitting (PS) and Sidewall Image Transfer (SIT) and their implication on design rules and CD Uniformity. Advanced OPC solutions such as Model Based SRAF and Source Mask Optimization will also be investigated in order to ensure good process control.

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7973-69, Poster Session

Lithographic process improvement by FlexRay illuminator for memory application

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Source Mask Optimization (SMO) has been long recognized as one of the most promising techniques for extension of the lifetime of a certain photolithography generation without extremely pricey upgrade to the next generation optical system. Not until the debut of the pixel-like programmable illuminator in 2009 for producing near freeform illumination, the full potential of the source optimization was first time brought to reality from a textbook theory. By the programmed illumination, researchers have previously shown almost identical optical performance to what generated by the traditional Diffractive Optical Element (DOE) without the prolonged manufacturing time and the relative high cost of stocking up a variety of DOEs.

In our study, a commercially available pixel-like programmable illuminator from ASML, namely the FlexRay, was employed to investigate the limitation of FlexRay in the enhancement of lithography common window and the image contrast. Before the wafer exposure, a simulation of source-only optimization was done by Tachyon SMO software for the selection of the best illumination source. Exposure was carried out by ASML XT-1950i equipped with FlexRay on one of the most critical layer of 50nm DRAM with known hotspots of resist peeling. Pupil information was collected by scanner's built-in sensor for the confirmation of the produced source shape against the programmed source and the optically simulated CD.

We achieved impressive complete elimination of lithography hotspots along with a remarkable depth-of-focus improvement as much as 50% by the use of FlexRay system. Regular focus-exposure matrix and the subsequent critical defects scanning indicated that the common process window of the tight-pitched array and the periphery can be simultaneously enhanced with no additional hotspots identified. The benefits by the use of a programmed source in the additional manufacturing flexibility and lower CoO for effective yield improvement in high volume production are therefore unarguable.

7973-70, Poster Session

Quantification of the difference between sources by Zernike polynomial decomposition

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Source Mask Optimization (SMO) technique is an advanced resolution enhancement technique with the goal of extending optical lithography lifetime by enabling low k1 imaging [1,2].

Sources generated with SMO, can have very complicated shapes but can be realized with the state of the art scanners such as the FlexRay [3] technology from ASML, with a good accuracy. However, it had been shown that the free form or complex sources show higher sensibility to source variations than parametric or DOE sources [4]. This may be observed as higher MEEF or larger PVBand on the imaging process. Therefore, the pupil has to be analyzed, in order to measure the impact of any source deformation [5].

In this study we introduce a new way to quantify the difference between sources, based on a Zernike polynomial decomposition [6]. Such method can be used for several usages: from quantifying the scanner to scanner pupil difference or matching, to analyzing the impact on OPC models resulting from slightly modified sources. We present the use of this method in the 22nm technology RET development.

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7973-71, Poster Session

A simple method of source optimization for advanced NAND FLASH process

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We have developed a very simple source optimization (SO) method for advanced NAND flash. Source-mask optimization is a proven technique for ArF exposure tools to improve the process window of 32 nm generation logic devices, and has become one of the candidates to bridge the gap between ArF lithography and next generation lithography. For advanced memory devices such as 40 nm node NAND FLASH, typical off-axis illumination shapes are insufficient because CD difference is growing greater between dense/sparse/rough patterns, and source optimization is hence essential as well.

In this paper, we study the influence of SO on L/S and C/H critical layers patterning of advanced NAND FLASH device. Starting from the strong off-axis illumination shape which is optimized for the finest structure of the mask pattern, a systematic procedure is performed to extract the optimum parameters of additional assist sources to balance the imaging performance (DOF, contrast and optical proximity effect, etc.) of dense/sparse/rough patterns. Performance equations (linear optimization) with performance map (sensitivity) are utilized to search the best combination of intensity for each assist source. For C/H pattern, the optimization procedure is modified to solve the non-linearity and non-continuity problems on the relationship between assist source intensity and each imaging performance. Finally, optimized source shapes have been successfully demonstrated and experimentally verified on 40 nm node NAND FLASH L/S and C/H critical patterns despite the simplicity of the optimization method, without utilizing SO dedicated software.

7973-72, Poster Session

Gradient-based fast source mask optimization (SMO)

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Semiconductor fabrication is the cornerstone of the current IC (Integrated Circuit) industry. With advances in microlithography now pushing towards nano-scale features, the problem of how to print circuit layouts on wafers has become more intricate and convoluted. Optical Proximity Correction (OPC) is a resolution enhancement technique (RET) that modifies mask layout designs in order to minimize their distortion when transferred to silicon. A good OPC implementation may prove sufficient for a given process technology, precluding the need for a more expensive alternative, like Double Patterning, Alternating Phase Shift Mask (AltPSM), Immersion Lithography and so on. Evidently, OPC has clear advantages in efficiency and manufacturing cost.

Segment-based OPC has been the general industry approach and has proven successful through many CMOS generations. Because it only modifies existing edges in the layout, segment-based OPC has the advantage of being easy to implement, particularly in iterative algorithms. However, as the Critical Dimension (CD) becomes ever smaller, this type edge-only compensation is not expressive enough to exploit the full range of possible mask corrections. Therefore, the inverse mask design, or named Inverse Lithography Technology (ILT) that optimizes the cost function, has been proposed as an alternative due to its more relaxed constraints and full-mask approach. Indeed ILT provides lots of promising solutions for inverse mask correction due to the full mask space calculation. For different optimal requirements, fro example : Depth of Focus (DoF), Normalize Image Log Slop (NILS), Mask Error Enhancement Factor (MEEF) and etc, engineers can design adequate cost functions for relative issues. However, as the CD still shrinking, the highly dense configures of drawn mask, ex : Dynamically Random Access Memory (DRAM), limit the correction space of ILT. Therefore the ILT incorporating source optimization (SO) or generally called Source Mask Optimization (SMO) is recently widely studied. To perform the source optimization an Abbe method is usually employed to computation partially image formation. Nevertheless such approach are extreme time consuming because the four fold integrate are demanded. Moreover the local minimum, slow convergence and other issues in ILT still exist. Actually the SMO can be seen as another inverse technique for resolution enhancement like ILT where all algorithms used in ILT can be applied to SO and have similar thorny issues. So far SMO still need more developments and studies to become a conventional RET.

In this paper, we propose a gradient based source and mask optimization. Two current widely used cost functions, aerial image and resist image, are employed to investigate the inverse optimization. The former compares the optical intensity distribution on the photoresist (after exposure but before developing) to a desired target intensity, while the latter compares the developed photoresist profile to the desired outcome for a given mask. Fig. 1 systematically shows the calculation flow. Finally a test template which is composed by dense vias will be exploited in our simulation. The width and length of every visa in the template are 0.63 and 0.88 respectively.

7973-73, Poster Session

Beam shaping: top hat and customized intensity distributions for semiconductor manufacturing and inspection

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Enabling the next technology nodes with optical technologies means further reduced error budgets for optical systems and new optical approaches for higher precision and increased throughput. This contribution discusses important aspects and features of laser beam shaping in optical systems for semiconductor manufacturing and inspection. Beam shaping principles for different types of lasers and illumination requirements are explained.

LIMO’s unique production technology based on computer-aided design enables the manufacture of high precision asphere arrays for a wide range of wavelengths in any optical material like CaF2 or fused silica. These free form micro-optical lens arrays can provide very steep intensity profiles with high uniformity significantly better than 1% P-V at numerical apertures above 0.35. They enable lossless polarization control, do not

suffer from zero order losses like diffractive elements, and are extremely efficient with fill factors close to 100%. These homogenizing elements in the illumination optics can provide a custom designed intensity distribution, and provide the possibility to compensate effects of other optical elements. Each lens can be designed individually and can also be shaped asymmetrically. Thus unusual lens sizes and shapes can be produced, and various far fields can be achieved.

Due to the special free form such as asymmetric profile these lens arrays can provide extremely uniform far fields at the target under also for a non orthogonal illumination path. This enables new inspection geometries because the wafer or mask can be uniformly illuminated even if normal incidence is obstructed by detectors.

Another strength of lenslet arrays is multi channel beam shaping for massively parallel processing with high power lasers. Anamorphotic telecentric microoptic objectives can split beams into several uniform segments and image the spots onto the working plane. This results into accurate dimensions and uniform intensity distributions for every single illuminated area. Field dimensions are only restricted by the diffraction limit. Applications can be direct material processing as well selective mask illumination approaches.

These manufacturing capabilities are also used for phase shifting elements. These elements are required for beam shaping of single mode lasers. Because of coherence effects, lenslet arrays are not suitable for single mode lasers and phase shifting approaches are needed.

7973-74, Poster Session

Practical aspects of source and mask optimization for logic and embedded flash volume manufacturing

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Among available lithography resolution enhancement techniques the Selective Inverse Lithography (SILT) approach recently introduced by authors [1] has been shown to provide the largest process window on lower-NA exposure tools for 65nm contact layer patterning. In present paper we attempt to harness the benefits of source mask optimization (SMO) approach as part of a hybrid RET. The application of source mask optimization techniques further extends the life-span of lower-NA 193nm exposure-tools in high volume manufacturing. By including SMO step in inverse OPC flow, we show that model-based SRAF solution can be improved to approach SILT process variation (PV) band performance. Additionally to OPC, the complexity of embedded flash designs requires a high degree of exposure tool matching and a lithography process optimized for topographically different logic and flash areas. We present a method how SMO can be applied to scanner matching and topography-related optimization.

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7973-75, Poster Session

Hierarchical kernel generation for SMO application

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The recent progress of advanced Microlithography demonstrates that source mask optimization (SMO) can provide significant improvement on the print quality. However, with the rapid growing complexity of source mask configuration, the runtime of kernel generation is also increasing tremendously.

In this paper, we propose to use hierarchical kernel generation method to reduce the kernel generation runtime. The key idea is that we first partition the source into several zones and generate compact set of kernels for each zone then combine the reduced kernel together and perform compaction again. The experimental results show significant runtime improvement over flat compaction while accuracy is within 1%.

In addition, with the help of Arnoldi/Lanczos algorithms, we can further reduce the runtime and memory consumptions by 2X.

7973-76, Poster Session

Aberration-aware source and mask optimization to enhance the optical lithography performance

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In order to fulfill the demand to print continuous shrinking pattern on the wafer, various techniques have been researched and developed. Among them, source and mask optimization (SMO) is considered to be a key enabler to push the technology node to 32nm or 22nm. Traditional SMO methods do not take aberration into account, which makes the optimization result less usable in reality, especially in high NA regime. In this paper, we propose a method to improve the optimization result by considering the aberration condition in lithographic projection optics. The aberrations in lithographic projection optics are represented by combination of Zernike polynomials with consideration of typical Zernike coefficient distribution and variation in lithographic projection optics. An algorithm that mutually optimizes source and mask under this representation is developed. With certain compromise in computation efficiency and the quality of optimization result in the ideal condition, more robust optimization performance against the aberration in real lithography conditions is realized, which is more meaningful in applying in the real lithography tools.

7973-77, Poster Session

Multiphoton micro/nanolithography technique with femtosecond laser direct-writing processing

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Recently, the researches and developments of unconventional micro/nanolithography have been become an attractive interest. Among various techniques, the micro/nanolithography technique based on multiphoton polymerization (MPP) has emerged as a powerful tool, which might hold the key to complex 3D structures fabrication with nanometer scale precision. MPP micro/nanolithography technique basically belongs to laser direct writing processing without masks. The spatial resolution of MPP micro/nanolithography is one of key issues for its application in micro/nanolithography. With normal laser direct writing technique, the spatial resolution is difficult to be achieved at nanometer scale due to the diffraction limit. The micro/nanolithography based on multiphoton process provides the potential to break the diffraction limit and realizes the spatial resolution within nanometer scale. In the last decade, the spatial resolution of MPP micro/nanolithography has been improved to several tens nanometers. Here, we will review the progress on multiphoton micro/nanolithography and report the latest progresses on the improvement of the spatial resolution as well as its applications in the fields of semiconductor micro/nanodevices, photonic devices, BioMEMS.

In the practical multiphoton micro/nanolithography, we use a mode-lock Ti:Sapphire femtosecond pulse laser system with a center wavelength of 800 nm, a pulse width of 100 fs and a repetition frequency of 82 MHz. The laser beam is tightly focused by an oil immersion objective lens with the numerical aperture NA of 1.45. The laser focus spot is scanned in the horizontal directions by a pair of galvano mirrors (SCANLAB, HurrySCAN 14). A piezostage (PI, P-622.ZCL) is used to move the laser

focus spots in the axial direction. The commercial negative resists for UV lithography, SCR500 (JSR) and SU-8, have been widely used in the experiments of multiphoton micro/nanolithography. Since the two-photon absorption cross-section of the photoinitiators in the photoresists strongly influences the threshold of two-photon photopolymerization, the controls of laser power induced to photoresists and the exposure time become critically important for achieving the spatial resolution at nanometer scale. To obviate the difficulty of varying measurements of LSR of MPP nanofabrication, we set the center of the focus point onto the surface of the substrate, which leads to the cured portion of the resin fixed on the substrate surface to avoid shrinkage in the lateral direction. We investigated the changing tendency of the linewidth of the cured polymer lines with using the different laser power and the exposure times. Figure 1a shows an example of scanning electron microscope (SEM) image of polymer lines cured by 3.3 mW laser power after various exposure times. The linewidth of the cured polymer is improved to 65 nm when the exposure time is reduced to 0.40 ms as shown in Figure 1b. We successfully obtained a linewidth of 50 nm by using a laser power of 2.5 mW with an exposure time of 1.07 ms as shown in Figure 1c. The results of the polymer linewidth are summarized in Figure 1d as a function of exposure time under different laser powers.

7973-78, Poster Session

High-range laser light-bandwidth measurement and tuning

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High performance lithography is increasingly demanding light sources to deliver laser light over a much larger range of stabilized bandwidths. The applications range from improved optical proximity correction (OPC) to the high-speed printing of vias and contact holes, through a process called focus drilling. Several advances in light source technology must integrate to provide the improved bandwidth performance required by the industry.

This paper will outline three of the core technologies developed by Cymer and integrated into its most advanced XLA and XLR series light sources to meet this need. Novel improvements in line narrowing offer the actuation necessary to tune the bandwidth over the large range. Advanced bandwidth metrology yields accurate measurements of the bandwidth over the wide range. And new controls and feedback algorithms provide the integration to stabilize the bandwidth to the desired target. The result provides laser light bandwidths that can be tuned to and accurately stabilized at any target from 0.3 pm to 1.6 pm, while maintaining all other laser performance parameters. The feature is called focus drilling. Focus drilling extends the utility of Cymer XLA and XLR lasers by adding more flexibility to the light source, allowing the end-user chipmaker to select the exact properties of the laser light necessary for a wider range of process steps.

The article will discuss the above technologies and emphasize their important aspects. It will also highlight some of the key performance aspects using data from Cymer's testing. Some of the design features and trade-offs will be provided, and a few of the relevant metrics will be presented and justified. Finally, potential future improvements to the technology will be presented.

7973-79, Poster Session

DUV-light source availability improvement via further enhancement of gas management technologies

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The continuous evolution of the semiconductor market necessitates ever-increasing improvements in DUV light source uptime as defined in the SEMI E10 standard. Cymer is developing technologies to exceed current and projected light source availability requirements via significant reduction in light source downtime. As an example, consider discharge chamber gas management functions which comprise a sizable portion of DUV light source downtime. The recent introduction of GLXTM (Gas Lifetime Extension) gas management system as a productivity improvement technology for its DUV lithography light sources has demonstrated noteworthy reduction in downtime. This has been achieved by reducing the frequency of full gas replenishment events from once per 100 million pulses to as low as once per 2 billion pulses.

Cymer has continued to develop relevant technologies that target further reduction in downtime associated with light source gas management functions. Our current subject is the development of a technology to reduce downtime associated with gas state optimization (e.g. total chamber gas pressure). Current gas state optimization is performed at regular intervals throughout the lifetime of light source core components and contributes to downtime. We aim to introduce a product enhancement that allows the light source to perform continuous adjustments to optimize the gas state as needed with no operational interruption.

Further, we aim to motivate the relevance of eliminating the manual procedure via analysis of light source downtime using data from production systems. Concrete projections of uptime on DUV light sources which incorporate this new technology will also be detailed.

7973-80, Poster Session

Focus drilling for increased process latitude in high-NA immersion lithography

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Double-patterning ArF immersion lithography continues to advance the patterning resolution and overlay requirements, and has enabled continued semiconductor bit-scaling. In order to resolve a range of 2D structures at the minimum pitch, high-NA lithography often results in process performance that is limited by the available depth of focus, particularly for patterning of contacts, vias or trenches. Achieving sufficient overlapping depth of focus over a range of geometries can be particularly challenging for these applications. Therefore, lithographers today employ a range of design, process and resolution enhancement techniques to overcome the depth of focus and other process constraints required for manufacturability of sub-45 nm half-pitch technologies.

In this paper, we discuss a focus drilling technique applied to increase the depth of focus, and therefore reduce process variability, for contact hole patterning. Several focus drilling approaches have been discussed previously; in this case it is enabled by operating the lithography light-source at an increased spectral bandwidth and has been made possible by new actuators and metrology in dual-chamber light-sources. We report wafer experimental and simulation results, which demonstrate significant process window enhancement for targeted device patterns. The depth of focus can be increased by 50%, or more in certain cases, with only a modest reduction in exposure latitude, or contrast, at best focus. Given this tradeoff, the optimum laser focus drilling setting is carefully selected to achieve the desired depth of focus gain at an acceptable contrast, mask error factor and optical proximity behavior over the range of critical patterning geometries. In this work, we also define the metrology and control requirements for the light-source spectrum in focus drilling mode required for stable imaging and report initial trend monitoring results over several weeks on a production exposure tool. We additionally simulate the effects of higher-order chromatic aberration and show that cross-field and pattern-dependent image placement and critical dimension variation are minimally impacted for a range of focus drilling laser spectra. In conclusion, this paper discusses practical benefits of tradeoff design and co-optimization of the target focus drilling set-point and appropriately selected resolution enhancement approach to maximize the depth of focus and process-window overlap, and increase effectiveness of the source-mask solution for contact patterning.

7973-81, Poster Session

Compensation of mask-induced aberrations by projector wavefront control

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Rigorous simulation of light diffraction from optical and EUV masks predicts phase effects with an aberration like impact on the imaging performance of lithographic projection systems [1, 2]. Some of these mask induced aberration effects can be compensated by a wavefront control of the projection lens. Recently, experiments by Finders [3] presented significant focus offsets of lines with different pitches and orientations and the reduction of the best focus difference among these features by proper control of the wavefront.

This paper demonstrates the application of advanced modeling and optimization methods for the compensation of mask induced aberration effects. All simulations are performed with the Fraunhofer IISB research and development lithography simulator Dr.LiTHO. The Waveguide method is applied for the rigorous computation of the mask diffraction spectra. Bulk images are simulated with a vector imaging model based on an extended Abbe approach. A typical ArF full physical resist model was used for the modeling of the photoresist processing. The wavefront modifications are described in terms of Zernike coefficients. Selected simulations demonstrate the complex impact of the Zernike coefficients on the resulting focus budget.

A genetic algorithm is applied for the optimization of the wavefront in terms of Zernike coefficients. For an optimization run with settings close to that of Finders [3] the adjustment of the wavefront reduces the maximum best focus difference from 41.9 nm to 21.9 nm. This improvement is achieved by setting the Zernike coefficient Z4 to -270 millilambda, Z9 to -180 millilambda, Z16 to 6 millilambda and Z25 to 14 millilambda.

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7973-82, Poster Session

Advanced scanner matching using freeform source and lens manipulators

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Proximity matching is a common activity in the wafer fabs, for purposes such as process transfer, capacity expansion, improved scanner yield and fab productivity. The requirements on matching accuracy also become more and more stringent as CD error budget shrinks with the feature size as technology advances. Various studies have been carried out, using scanner manipulators including NA, inner sigma, outer sigma, stage tilt, ellipticity, and dose. In this paper, we present matching results for critical features of a logic device, between an ASML XT:1900i scanner and an XT:1700i (reference), demonstrating the advantage of freeform illuminator pupil as part of the adjustable manipulators to provide additional flexibility. We also present the investigation of a novel method using lens manipulators for proximity matching, effectively injecting scalar wavefront to an XT:1950i to mimic the behavior of the XT:1700i lens.

7973-83, Poster Session

Measurement of wavefront distortions in DUV optics due to lens heating

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Lens heating due to absorbed UV laser radiation can diminish the achievable spatial resolution of the lithographic process in semiconductor wafer steppers. At the Laser Lab Göttingen a measurement system for quantitative registration of this thermal lens effect was developed. It is based upon a strongly improved Hartmann-Shack wavefront sensor with extreme sensitivity, accomplishing precise on-line monitoring of wavefront deformations of a collimated test laser beam transmitted through the laser-irradiated site of a sample. Caused by the temperature-dependent refractive index as well as thermal expansion, the formerly plane wavefront of the test laser is distorted to form a rotationally symmetric valley, being equivalent to a convex lens.

The new sensor, which is capable to record relative changes in the range of /10000 (corresponding to deformations of < 100pm), allows registration and precise characterization of induced wavefront distortions by real-time Zernike analysis. On the other hand, the photo-thermal technique can be employed for a rapid assessment of the material quality, since the extent of transient wavefront deformation is directly proportional to the absorption losses. When used in orthogonal test geometry on cuboid samples, quantitative determination of both surface and bulk contributions to the overall absorption can be obtained by comparison with thermal theory (cf. Fig. 1).

Along with a description of the new technique we present photo-thermal measurements on various fused silica samples under 193nm irradiation. The data are compared with theoretical results obtained from a semi-analytical solution of the heat diffusion equation. Excellent agreement is achieved regarding both shape and extent of the lens heating effect.

7973-84, Poster Session

Improved immersion scanning speed using superhydrophobic surfaces

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Failure of the receding meniscus during immersion lithography is one of the well known problems [1,2]. A thin liquid film left behind on the wafer during the high speed scanning may affect the advancing meniscus during subsequent scans and thereby generate imaging defects. In this work we report a method to use slightly rough hydrophobic (sticky) and superhydrophobic (slippery) surfaces to avoid liquid loss at high speed scanning. The study revealed that the sticky and slippery surface showed identical meniscus behavior under immersion conditions with improved critical velocity >2.5m/s.

The receding meniscus behavior of water drop on the nano-textured polymethylmethacrylate (PMMA) surfaces has been studied for water immersion lithography purposes. PMMA was nanotextured (randomly nanoroughened) in Oxygen Plasma followed by 40nm Teflon deposition to make it superhydrophobic [3]. The study of the receding meniscus has been performed at ASML research laboratories by means of a turn table set-up [4]. A two-concentric-needles system provides simultaneous water supply and extraction. In this way a continuously refreshing cylinder-like droplet is created on the wafer substrate below the needle. A turn table is used to accelerate the surface, while the meniscus shape of the droplet is captured with a high-speed camera.

To our knowledge it is for the first time that the dynamic contact angle behavior of a superhydrophobic surface and at such high velocities is studied. On the smooth hydrophobic surface, the instability of the receding contact line occurs at the critical velocity ~0.8m/s. Surprisingly on a sticky surface there were no instabilities on the receding meniscus even at setup’s maximum velocity 2.5m/s. The drop on superhydrophobic surface was also showing a stable meniscus up to 2.5m/s. We note that a comprehensive study of the liquid loss properties on superhydrophoic

surfaces for immersion system has not yet been done due to the processing constraint of smooth and wettable photoresist surfaces needed for lithography. Since we nanotexture the surfaces, the method proposed in this work is specifically focused on improving the scanning speed in the chuck area surrounding the wafer. However, we have shown that the water drop on both the sticky hydrophobic and the slippery surface exhibited no instabilities up to ~2.5m/s. We thus concluded that the scanning speed on the immersion system could largely be increased with this type of surfaces. It is also significant to note that even a small roughness would improve the maximum stable scanning velocity over a smooth hydrophobic surface. With a roughness of 7nm rms we have reached velocities higher than 2.5m/s. We thus expect that the scanning speed on a photoresist can be significantly improved, provided the roughness is permissible.

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7973-85, Poster Session

ArF scanning exposure tool using high-NA projection lens

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As a new company of the lithography world, SMEE has developed and produced a prototype wafer exposure tool, with an ArF laser light source. This tool, SMEE SSA600/10, adopted step and scan technology to obtain a large exposure filed and to average optical aberrations for a scanned image to improve CD uniformity and reduce distortion. The maximum numerical aperture is 0.75 and the maximum coherence factor of illumination system is 0.88. The illuminator provides continuously variable conventional and off-axis illumination mode to improve the resolution. In this paper, the configuration of the exposure tool is presented and the design concepts of the scanner are introduced. We show actual test data such as synchronization accuracy, focus and leveling repeatability, dynamic imaging performance (resolution, depth of focus) and overlay.

7973-111, Poster Session

Evaluation of different application cases for simulation-based scanner tuning

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Differences in imaging behaviour between lithographic systems of the same wavelength result in variations of optical proximity effects (OPE). A way to compensate these irregularities is through scanner tuning. In scanner tuning, scanner specific adjustments are obtained through the determination of scanner knob sensitivities of relevant structures followed by an optimization to adjust the structure CD values to be close to the desired values.

Traditionally, scanner tuning methods have relied heavily on wafer-based CD metrology to characterize both the initial mismatch as well as the sensitivities of CDs to the scanner tuning knobs. These methods have proven very successful in reducing the mismatch, but their deployment in manufacturing has been hampered by the metrology effort. In this paper, we explore the possibility of using ASML's LithoTuner PatternMatcher FullChip (PMFC) computational lithography tool to reduce the dependence on wafer CD metrology.

One tuning application using scanner knobs for a manufacturing environment is presented in this work; in this application individual critical features in wafer printing are improved without affecting other sites. Potential uses of this technology are for process transfers from one fab to another where the OPC signature in the receiving fab is similar but not identical to the signature of the originating fab.

The tuning application is investigated with respect to their applicability in a production environment, including further metrology effort reduction by using scatterometry tools.

7973-87, Poster Session

Challenge for compensating the mask topography effect by staged modeling method under the hyper-NA condition

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Generally speaking, OPC (Optical Proximity Effect Correction) model can be divided into three parts, mask part, optic part, and resist part. For the excellent quality of the OPC model, each part has to be described by the first principles. However, OPC model can not take the all of the principles since it should cover the full chip level calculation during the correction. Moreover, the calculation has to be conducted iteratively while the correction until the cost we want to minimize converges. Normally the optic part in OPC model is described with SOCS (Sum of Coherent System) method. This method makes us calculate the aerial image so fast without the significant loss of accuracy. As for the resist part, the first principle is too complex to implement in detail, so it is normally expressed in a simple way, such as the approximation of the first principles, and the linear combinations of factors which is highly correlated with the chemistries in the resist. The quality of this kind of the resist model depends on how well we train the model through fitting to the empirical data. The most popular way of making the mask function is based on the Kirchhoff's thin mask approximation. This method works well under the condition that the features on the mask is sufficiently large, but as the line width of the semiconductor circuit become smaller, this method causes significant error due to the mask topography effect. To avoid the error from the mask topography effect, we have to use rigorous methods of calculating the mask function, such as FDTD (Finite Difference Time Domain) and RCWA (Rigorous Coupled-Wave Analysis). But these methods are too time-consuming to be used as a part of OPC model. In this paper, we suggested a solution to catch up with the mask topography effect. The solution includes how we manipulate the mask function to mimic the rigorously computed mask function. Even though this method works quite well, the operations for the mask manipulation do not increase the total calculation time significantly. We were able to have some results that the total model accuracy was improved with just small amount of time increase. In addition, we suggested the staged modeling sequence in finding out the proper parameters for the mask manipulation.

7973-88, Poster Session

Large-scale model of wafer topography effects

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Wafer topography proximity effects (TPE) are playing an increasing role in 193 nm lithography patterning. In particular, implant layers, lines are patterned without any underlying BARC in proximity to underlying features such as shallow trench insulation (STI) regions. Reflections from this geometrical and optical wafer topography affects the line contour, in some cases leading to line collapse and in some cases managing to fully disrupt it.

The goal of this paper is to extend techniques used for optical proximity correction to include TPE. Central to this is an imaging model that efficiently includes the TPE with high performance and sufficient accuracy, capable of addressing very large areas. This large scale model can then be used in standard correction approaches, compensating for both the optical proximity effects and wafer topography proximity effects.

Development of the approximate models was strongly based on rigorous lithography simulation with wafer topography, and on qualitative experimental data. In particular rigorous lithography simulation enables us to build an extensive set of test patterns to enable, quantify and verify accuracy over a wide range.

We examine a number of approaches to models and to model fitting, focusing in particular to TPE originating from STI and gate layers. Particular care is given to the compatibility with traditional OPC models, in structure, speed as well as the fitting and verification process. Capturing ability and performance of the model is numerically evaluated on a number of test patterns. The performance of the model is close to that of OPC models.

Traditional test pattern sets for planar OPC models are extended with non-planar test patterns, both for model fitting and verification. The model building and verification flow allows to mix experimental data with simulated data.

We analyze the relevance of the model to various specifics of wafer topography and lithography, including complex topography, 3D resist profiles, stack layers and materials. We illustrate model accuracy and the ability of capturing problematic patterns, and compare the performance on large areas.

7973-89, Poster Session

Study of model-assisted rule base SRAF for random contact

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As the end nears for Immersion lithography, greater amount of pressure is placed on RET(Resolution Enhancement Technology) to extend the life time of Immersion lithography tool prior to EUVL(Extreme Ultra Violet Lithography) Era. One form of RET that's attracting much attention for extension of immersion lithography for contact layer is models based SRAF(Sub Resolution Assist Feature). Model based SRAF utilizes IL(Inverse Lithography) to optimize the placement and size of the SRAF required for photo lithography process margin enhancement. Many research centers are reporting great improvement in process margin using IL but this improvement comes with some side effects. One of the side effect using model based SRAF is difficulty in making the mask. Since the SRAFs are generated using the IL technology, generated SRAFs are often place uneven and size of the SRAF are unstable for mask fabrication. This kind of unstableness in the mask may result in local defect and unwanted process margin degradation on wafer level.

In this paper, we will evaluate model assisted rule base SRAF. Model assisted rule base SRAF combines the advantage of both model based SRAF and rule base SRAF to ensure high process margin without the mask making difficulty with stable wafer output. Model will assist in generating a common rule for rule based SRAF. Method to extract the rule from the models will first be discussed. Model assisted rule based SRAF will be applied to 3Xnm DRAM contact. Evaluation and analysis of the simulated and actual wafer result will be discussed. Our wafer result showed that by applying Model assisted rule based SRAF showed nearly equal performance to models based SRAF with clearly better stability and mask fabrication feasibility.

7973-90, Poster Session

Development and evaluation of rigorous OPC using physical lithography simulation

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The accuracy of OPC models is one of the top process control challenges for below 30 nm node. Despite excellent OPC model calibration procedures there can be lacks in correct simulation of critical pattern traded for the OPC models computational speed. Therefore rigorous lithography simulation is used to compliment the OPC flow with predictive simulation for verification and manual fine tuning of OPC results. In this paper we go one step further and apply rigorous simulation already in automatic OPC.

Computational speed and OPC turnaround time (TAT) is the major challenge for application of rigorous simulation in an OPC workflow. It takes about 100 times longer than the conventional OPC model to calculate the unit work template so that it has been practically impossible to employ the rigorous OPC to real device OPC.

We apply several ways to reduce TAT significantly. We introduce a rigorous OPC flow combining the computationally fast OPC model and the predictive rigorous model both serving the signal to the OPC engine. Adaption of the hierarchy structure to the marked hotspots leads to a higher partitioning efficiency. Improvement of correction solver algorithm leads to decrease the number of necessary rigorous simulations in one correction. We also investigate numerical settings of the rigorous simulator for acceleration while keeping simulation accuracy. Those speed improvements allow a final assessment of hot spots on full chip level.

Finally we discuss practical applications of rigorous OPC and rigorous OPC verification. We show the enhancement of OPC accuracy through rigorous OPC at critical points for array edges, array corners and periphery hot spots. After TAT optimization of the rigorous OPC, we continue developing and evaluation the practical applications.

7973-91, Poster Session

Mask data correction methodology in the context of model-based mask data preparation and advanced mask models

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The extension of 193nm lithography for single and double patterning is driving the industry towards more complex resolution enhancement techniques such as inverse lithography and source mask optimization. These techniques require extremely complicated mask shapes at the same time that the specifications are tightened by moving to more advanced nodes, by accounting for higher MEEFs, or by accounting for tighter CD and placement requirements for double patterning. The creation of more accurate mask models and the use of these models in model-based mask data preparation are needed to meet these requirements. Many different physical phenomena capable of distorting the mask shapes need to be modeled. Such models include for example fogging effects, Coulomb effects, forward and back-scattering effects, resist diffusion effects, etch effects, loading effects, etc. The range of these effects varies from a few nanometers to a few millimeters thereby creating a challenge when corrections need to be applied to the mask shapes or to the exposure dose. At the same time model-based mask

data preparation opens up more degrees of freedom when the shots can be overlapped and the dose can be assigned for each shot individually. The impact of model-based mask data preparation on proximity effect correction was already assessed but limited to back-scattering effect corrections [1].

In this paper we will review a methodology to handle these various models in the context of model-based mask data preparation. In particular we will report on how models with very different ranges can be implemented to apply mask data corrections.

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7973-92, Poster Session

Optimizing OPC data sampling based on "orthogonal vector space" for model calibration

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In OPC model building process, appropriate wafer data sampling plan plays a key role. On the one hand, the empirical OPC model is calibrated with selected wafer data sets, which are supposed to represent the real product design. If the selected wafer data have insufficient coverage, the built model will be inclined to be unstable due to failure in interpolation or extrapolation. On the other hand, excessive data collection will not guarantee an OPC model with better accuracy and stability. The redundant gauges contribute little to estimate model parameters more accurately. In the meanwhile, the model building cycle time will be limited by the metrology loading. On the contrary, if there is only a compact set of effective gauges are used in calibration; we can reduce modeling turn-around time significantly. Moreover, fewer gauges for calibration mean higher measurement quality for the same SEM budget. Accordingly, it is necessary to come up with a method for data selection with optimum coverage. In this paper, we will investigate the feasibility of using Tachyon Pattern-selection-tool for data selection.

In Tachyon pattern-selection-tool, a high dimension "pattern vector space" is constructed with a set of orthogonal basis functions. The optical signals of each gauge are projected into this space as a vector. The distribution of all vectors in this space represents the process properties "seen" by calibration flow. By down sampling the vectors in this pattern coverage space while keeping the coverage distribution volume and shape, smaller number of gauge patterns can take equivalent effects in calibration flow as original full gauge set. Pattern selection tool realizes a platform to optimize gauge files for better model quality and more efficient calibration flow.

Our study focuses on using the "pattern vector space" to answer three following three questions,

1. Whether current full data sampling is enough to represent the product design? A reference domain is needed to verify the coverage of testpattern.

2. What's the relationship between selection points and model accuracy and how to get an optimum coverage without sacrificing the model quality?

3. Whether the model built with selected set of data have comparable quality compared with the model built with full gauge data?

Before doing the pattern selection on current full gauge set, we need build a reference domain which represents the real device design. According to ref. 1, generalized pattern shapes for 1D and 2D respectively are employed to approximate the product layouts. The representing patterns are put into four categories, 1D-line, 1D-space, 2D-line, 2D-space. The 1D line patterns have three geometrical sizes w0, w1 and s0, while the 2D patterns have five geometrical sizes w0, h0, s0, w1, h1. By varying the parameter sizes, a big set of testpattern groups are generated. With a constant threshold model and pattern-selection-tool, the testpattern are projected into the high dimension vectors space, which are regarded as our representing domain. The advantage of this representing domain is it is general not restricted to certain layouts as chip designs are usually various. Subsequently, by overlapping the project vectors spaces of original full sampling plan (before pattern selection) and reference domain, we could confirm whether the current data sampling is sufficient or not to represent. Furthermore, ORC weak points and SRAM designs are mapped into a vector space as well, which should be covered by the projection space of current data.

In our test cases, the original full-set calibration wafer data totally has 907 points. Through the pattern-selection-tool, we selected 300, 400, 500, 600 sub-set points groups respectively the full-set, and OPC model are calibrated with these selected wafer data subsequently. The model accuracy in terms of RMS of all five models could are compared. Through the comparison, we found that 400 points of data already have comparable model quality while the sampling points are reduced by 56%. Furthermore, we did full-chip contour matching using 400pts and full gauge model, which will confirm the model quality is close to full-gauge model.

Another application of pattern-selection-tool is to further improve the testpattern coverage. By overlapping the whole OPC testpatterns with our proposed reference space and weak-points & SRAM chip designs, we could found out which shapes and sizes of pattern will improve the coverage of testpatterns.

7973-93, Poster Session

Effect of pattern-image log slope on OPC model

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Some large errors come from rather large target size when we analyze the results of across-chip linewidth-variation (ACLV) for the OPCed layers. It means that the OPC model error cannot be explained only by the target size. This paper focuses on the basic meaning of OPC modeling and concludes that pattern ILS strongly affects on CD error variation.

OPC modeling is one of the fitting processes. Users select the model type, parameter set, and sample patterns to fit the simulation thresholds to the measurement thresholds. The model made by sample patterns is applied to the OPC process for the real patterns which has lots of pattern types. The meanings of each word are as follows. "Model type" is divided into two types: optical model and resist model. And the examples of resist model are sparse model and dense model. Each model has many fitting model types. The available fitting "parameter set" is normally given by model type. "Sample patterns" are a number of patterns of various pattern types that can represent the real patterns. "Simulation (or Model) threshold" means the fitted intensity threshold by OPC model. "Measurement threshold" is the intensity at which the measured CD can be calculated. And "fitting" is the process that minimizes the cost function, such as CD error RMS, between model threshold and measured threshold.

OPC model can not exactly predict the whole measured data. The root cause is the fact that only a few model parameters can not fully explain the complicated PR patterning mechanism. To overcome the weakness of the OPC modeling, modeling tools provide additional meaningless fitting parameters and a weight method by which user can weight on critical patterns. However, both methods can not perfectly fit the whole samples.

It was concluded that the OPC modeling is just one of the fitting processes and some errors are inevitable. Due to the fact that the intensity is non-linear, the fitting error strongly depends on intensity shape. In this paper, pattern image log slope (ILS) was regarded as a representative factor of the intensity shape. From the relation between the threshold error and the CD error for different ILS, it can be concluded that the large CD errors result from the patterns with small ILS for the same threshold error.

We analized the modeling results differently from the previous method, the CD error as a function of ILS for ACLV patterns and model sample patterns. CD error was normalized by the largest CD error. The ILS range of selected sample patterns is 20 ~ 55 um^-1. The CD error range at the small ILS is over 1.6, while that of the large ILS is around 0.4. However, it should be noted that the pattern ILS affects on the CD error variation not the CD error itself. To sum up, the smaller the pattern ILS is, the larger the CD error variation is. This trend is easily understandable when we think about Fig. 1. ACLV patterns also show the same CD error variation trend as is in the model sample patterns.

7973-94, Poster Session

Tolerance-based OPC and solution to MRC-constrained OPC

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Model based OPC (MB-OPC) has been widely used in advanced lithography process today. However controlling the edge placement error (EPE) and critical dimension (CD) has become harder as the k1 process factor decreases and design complexity increases. Especially, for high-NA lithography using strong off-axis illumination (OAI), ringing effects on 2D layout makes CD control difficult. In addition, mask rule check (MRC) limits also prevent good OPC convergence where two segment edges are corrected towards each other to form a correction-conflicting scenario because traditional OPC only consider the impact of the current edge when calculating the edge movement. To ensure MRC compliant OPC results, MRC enforcement is normally employed during OPC and (or) in later step after correction job is finished. However, edge movement during MRC enforcement step ignores the change in EPE and thus can degrade OPC convergence dramatically near edges with high mask error enhancement factor (MEEF). While more strict design rules are applied to smaller node, such correction-conflicting dilemma cannot always be avoided at 30nm node and beyond. The MRC-constrained OPC has been a universal problem for traditional MB-OPC. A more sophisticated OPC algorithm that considers the interaction between segments is necessary to find a solution that is both MRC and convergence compliant.

Our solution to tolerance-based OPC and MRC-constrained OPC is by solving multiple segments together which take into account both the geometry interaction and lithographic interaction between segments. We perform normal MB-OPC first, which neglects the interaction between the neighboring segments while estimating the edge movement for each segment. For hot spots where contour width or contour space are out of bridging, pinching, EPE or CD variation specification, segment groups are created around the hot spots and are being re-corrected together. For segments that are MRC constrained, the limit for the edge movement is being considered during the re-correction step, and the residual errors on the hot spots are minimized while the neighboring segments still stay in-spec. Better convergence and tighter EPE control can be achieved with the matrix solver. Prioritization rules and weighting schemes can be used to prioritize critical locations or features. The re-correction step can be applied iteratively until no hot spots are indentified. Overall the tolerance-based OPC and MRC-constrained OPC approach provides a method to control the convergence better while still being able to provide a MRC-compliant solution. This correction approach can be applied to different layers (contact, poly, metal, etc) and is easy for user customization. The performance penalty by utilizing the matrix solver is minimized by applying the matrix solver in limited and critical areas only.

7973-95, Poster Session

Study of various RET for process margin improvement in 3x-nm dram contact

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As the DRAM node shrinks down to its natural limit, photo lithography is encountering many difficulties. 3Xnm DRAM node seem to be the limit for ArF Immersion. Until the arrival of EUV, double patterning (DPT) or spacer double patterning (SPT) seems like the next solution. But the problem with DPT or SPT is that both increases process step their by increasing the final costs of the device. So limiting the use of DPT or SPT is very important for device fabrication. For 3Xnm DRAM, storage node is one of the candidates to eliminate DPT or SPT process. But this method may cost lower process margin and degradation of pattern image. So, solution to these problems is very crucial.

In this study, we will realize storage node(SN) pattern for 3Xnm DRAM node with improved process margin. First we will discuss selection of illumination for optimal condition, second, correction of the mask will be introduced. We will also talk about the usage of various RET such as model based assist feature. Value such as DOF, EL and CDU (critical dimension uniformity) will be evaluated and analyzed.

7973-96, Poster Session

A cost-driven fracture heuristics to minimize external sliver length

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Mask writing is a significant step in optical lithography affecting the fidelity of the printed image on the wafer, and critical dimension (CD) control. During mask data preparation process, the mask pattern is initially fractured into numerous trapezoids. Subsequently, these trapezoids are exposed by the variable shaped beam mask writing machine. There are two independent metrics to be optimized during the fracturing process: trapezoid count and total external sliver length. Each trapezoid corresponds to at least one shot in the VSB machine. Thus, lower trapezoid count is desired, to reduce the writing time. A trapezoid with lateral dimension w smaller than a prescribed threshold is referred to as a sliver. There are two different kinds of sliver: external and embedded. The external sliver is located on the boundary of the layout, while the embedded sliver is not. Only external slivers introduce inaccuracies in the mask writing process and affect CD uniformity. Therefore, total external sliver length should preferably be minimized.

The main challenge in the current fracturing tools include increasing transistor density, smaller feature sizes, and aggressive use of resolution enhancement techniques (RET). Pixel-based OPC (PBOPC) is a RET that modifies the mask by adding sub-resolution assist features (SRAF) to the mask pattern. These SRAFs introduce numerous additional vertices and corresponding edges, thus dramatically increasing the trapezoid count and total external sliver length in the resulting fractured pattern. Recently, Kahng, et al. developed a fracturing method relying on integer linear programming (ILP) and a set of heuristics to speed it up [1]. Kahng's ILP algorithm is computationally complex, and cannot tackle the huge volume of vertices on PBOPC makes. In addition, the growth of tiny SRAFs on the PBOPC necessitates algorithms aimed at suppressing the external sliver length.

In this paper, we propose a cost-driven fracturing algorithm aimed at suppressing the total external sliver length, while keeping the trapezoid count low. First, a bipartite graph matching algorithm is developed to choose maximum non-intersecting chords on the mask with minimum induced external sliver length. Chosen chords are used to divide the parent-polygon into child-polygons. Subsequently, each child-polygon is decomposed into elemental rectangles by the rays emitted from each concave corner. Then, a rectangle combination technique (RCT) is applied to search and eliminate the external slivers from the child-polygon's boundaries by merging them with the neighboring rectangles. RCT is tailored to effectively reduce the external sliver length, while ignoring the harmless internal slivers. Then, we post-process all internal nodes and concave corners in the child-polygon to guarantee they satisfy the "convexity constraints". The post-processing step ensures the resulting trapezoid count approaches the theoretical lower bound described by Kahng et al. Finally, the fracture patterns of all child-polygons are stitched together to obtain the fracture pattern of the parent-polygon. Our proposed algorithm is shown to reduce the external sliver length of a commercially available fracturing tool by 8% to 13% on

the PBOPC of a Poly layer of a random logic layout with CD=90nm.

Reference:

[1] A. B. Kahng, X. Xu, and A. Zelikovsky, “Yield- and cost- driven fracturing for variable shaped-beam mask writing,” in Proc. 24th BACUS Symposium on Photomask Technology and Management, XI, pp. 360-371, Sep. 2004.

7973-97, Poster Session

A recursive cost-based approach to fracturing

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A Recursive Cost-Based Approach to Fracturing

In the microelectronic industry, a mask pattern is first fractured into trapezoids then fabricated by a variable shaped beam mask writing machine. The resulting fracturing affects the mask writing process. The growing transistor density, shrinking feature sizes, and increasing use of resolution enhancement techniques have created new challenges in fracturing: long mask write time and increased CD uniformity requirements. The challenges are influenced by many factors: number of trapezoids, type of trapezoids, and position of trapezoids.

There are multiple metrics to assess the quality of a fracturing. C. Spence et al.1 showed that the resulting number of trapezoids is closely related to the mask write time while M. Bloecker et al.2 showed external sliver length to be a suitable metric for quality assessment. Slivers are small trapezoids with width smaller than , a parameter of the mask writing tool. External slivers are slivers that are located on the boundary. In this paper, we solve an optimization problem for a cost function that captures the fracturing criteria by taking into account the weighted sum of the number of trapezoids and the external sliver length.

Specifically, we propose a recursive algorithm for rectilinear polygons that guarantees optimality under certain conditions. First, the input polygon is completely enclosed by a rectangle. Second, rays are generated from all the polygon corners in the Cartesian directions. The resulting intersections between the original polygon boundary, the enclosing rectangle boundary, and the additional rays are marked. This forms a grid that is bounded by the enclosing rectangle. The grid is then transformed into a binary array of points with values determined by whether the point exists within the input polygon. With this array, any sub-rectangle of the original rectangle may be represented with two coordinates namely the location of the upper-left and the lower-right points.

From here we develop and assign a cost to the sub-rectangles based on whether the sub-rectangle is entirely exterior to the polygon, an interior trapezoid, or an external sliver. The costs of the remaining sub-rectangles, with points both interior and exterior to the polygon, are calculated via a recursive algorithm. After solving for the costs of the enclosing rectangle the polygon fracturing is generated. We have developed two recurrences to solve for the remaining costs. The first one is a natural recurrence that splits the input rectangle in half, along the Cartesian direction with minimal cost resulting in an O(n5) runtime. The second recurrence divides the input rectangle into five smaller rectangles resulting in a longer runtime, O(n8); we have shown that under convexity restrictions for the Cartesian directions, this second recurrence provides optimal solutions. We solve both of these recurrences using dynamic programming resulting in polynomial runtime.

Our proposed algorithm successfully reduced external sliver length by 40-60% as compared to a commercially available fracturing tool for a pixel-based post edge-based OPC layout of Poly and Metal 1 layer with CD=90nm.

1. Chris Spence, Scott Goad, Peter Buck, Richard Gladhill, Russell Cinque, Jrgen Preuninger, Uwe Griesinger, Martin Bloecker, “Mask data volume: historical perspective and future requirements”, Proc. SPIE Int. Soc. Opt. Eng. 6281, 62810H (2006).

2. M. Bloecker, R. Gladhill, P. D. Buck, M. Kempf, D. Aguilar, R. B. Cinque, “Metrics to Assess Fracture Quality for Variable Shaped Beam Lithography” Proc. of SPIE Vol. 6349, 63490Z (2006)

7973-98, Poster Session

A novel mask error modeling approach for OPC

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As critical feature size shrinks at sub 30nm technology nodes with low k1 imaging, which is often characterized with a high Mask Error Enhancement Factor (MEEF), small mask errors can be actually magnified on the wafer to an extent that can no longer be ignored. It makes it indispensible to take mask errors into account for OPC modeling. Generally, there are two types of mask errors: random and systematic. Random errors are preferred to be treated as data noise, while systematic errors are preferred to be modeled as one part with the physical processes. A two stage modeling methodology is straightforward. In it, a mask process is first modeled, providing an output mask layout, to be followed by the OPC modeling. This usually involves two stages of data collection and model calibration, and the actual OPC algorithm would call the corresponding two models to correct the original layout from database. The disadvantages of above approach are obvious. In this work, a novel one stage method is proposed. In order to incorporated mask error effects as part of the OPC modeling, the mask error effects are firstly characterized across all areas. The characterization depends on optical settings and mask layout geometries. Uniform bias error, density dependent bias error and layout cornering rounding effects can be well characterized by this method. Using this characterization, the model contribution from the different mask error types is calibrated based on metrology data from printed wafers. The method is tested with a set of empirical wafer data. Results show this to be an efficient approach for including mask error effects in OPC modeling. Further testing with layout correction illustrates that the model form is compatible with our existing OPC algorithms.

7973-99, Poster Session

Full-chip OPC and verification with a fast mask 3D model

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As the pattern dimension on the mask becomes close to or smaller than the exposure optical wavelength, mask topography (3D) scattering has to be taken into account for a more accurate OPC solution. We report full-chip OPC and verification with a fast mask 3D model. This fast 3D model depicts the polarized waveguide effects of the mask topography. The model requires calibration against experimental wafer data or against rigorous electromagnetic field simulations. The aqua/aerial images formed by the fast 3D model are validated by rigorous 3D simulations. For a thorough investigation of its impact on OPC and verification, the fast 3D model is compared to the conventional mask model with Kirchhoff approximation. We performed lithography model calibration, OPC correction, and verification on a 40nm half-pitch metal layer using both approaches. OPC accuracies of both models will be evaluated by measuring the CD data on the printed wafer. OPC time with the fast 3D model is increased by 5% for the studied lithography configurations in this paper. Post-OPC verification of SRAF printability estimated by both models will also be compared to the CD-SEM measured contours at various dose and focus values.

The calibrations for the fast 3D and Kirchhoff models are carried out by fitting each model to measured wafer data. For XY-polarized c-quad illumination, the RMS fitting error is 1.5nm using the fast 3D model and 2.1nm using the Kirchhoff model as illustrated in Figure 1. Even though the fitting error of the Kirchhoff model is only 0.6nm larger than the fast 3D model, the fast 3D model is superior to the Kirchhoff model in predicting both the CD values and SRAF printability. Detailed data will be presented in the paper. For Y-polarized dipole illumination, the mask topography effect is expected to be more significant. The RMS fitting error is 2.1nm for 3D model and 5.9nm for Kirchhoff model.

7973-100, Poster Session

Overcome the process limitation by using inverse lithography technology with assist feature

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Patterning of contact hole using KrF lithography system for the sub 90nm technology node is one of the most challenging tasks. Contact hole pattern can be printed using Off-Axis Illumination(OAI) such as dipole or Quasar or Quadrupole at KrF lithography system. However this condition usually offer poor image contrast and poor Depth Of Focus(DOF), especially isolated contact hole. Sub-resolution assist features (SRAF) have been shown to provide significant process window enhancement and across chip CD variation reduction. The insertion of SRAF in a contact design is mostly done using rule based scripting. However the rule based SRAF strategy that has been followed historically is not always able to increase the process window of these 'forbidden pitches' sufficiently to allow sustainable manufacturing. Especially in case of random contact hole, rule-based SRAF placement is almost impossible task. We have used an inverse lithography technique to treat random contact hole.

In this paper we proved the impact of SRAF configuration. Inverse lithography technique was successfully used to treat random contact holes. It is also shown that the experimental data are easily predicted by calibrating aerial image simulation results. Finally, a methodology for optimizing SRAF rules using inverse lithography technology is described. As a conclusion, we suggest methodology to set up optimum SRAF configuration with rule and inverse lithography technology.

7973-101, Poster Session

Improvement on post-OPC verification efficiency for contact/via coverage check by final CD biasing of metal lines and considering their location on the metal layout

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As IC design complexity keeps increasing, it is more and more difficult to ensure the pattern transfer after optical proximity correction (OPC) due to the continuous reduction of layout dimensions and lithographic limitation by k1 factor. To guarantee the imaging fidelity, resolution enhancement technologies (RET) such as off-axis illumination (OAI), different types of phase shift masks and OPC technique have been developed. In case of model-based OPC, to cross-confirm the contour image versus target layout, post-OPC verification solutions continuously keep developed - contour generation method and matching it to target structure, method for filtering and sorting the patterns to eliminate false errors and duplicate patterns. The way to detect only real errors by excluding false errors is the most important thing for accurate and fast verification process - to save not only reviewing time and engineer resource, but also whole wafer process time and so on. In general case of post-OPC verification for metal-contact/via coverage (CC) check, verification solution outputs huge of errors due to borderless design, so it is too difficult to review and correct all points of them. It should make OPC engineer to miss the real defect, and may it cause the delay time to market, at least.

In this paper, we studied method for increasing efficiency of post-OPC verification, especially for the case of CC check. For metal layers, final CD after etch process shows various CD bias, which depends on distance with neighbor patterns, so it is more reasonable that consider final metal shape to confirm the contact/via coverage. Through the optimization of biasing rule for different pitches and shapes of metal lines, we could get more accurate and efficient verification results and decrease the time for review to find real errors. In this paper, the suggestion in order to increase efficiency of OPC verification process by using simple biasing rule to metal layout instead of etch model application is presented.

7973-102, Poster Session

Measurement of local pellicle thinning and line-width variation with different pellicle thicknesses

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Step-and-scan modes of wafer patterning require masks with no killer defects in order to achieve good yields. While masks are made without any defects that result in nonfunctional die, preventing particles from depositing on masks during extended mask usage is a challenge, even in the state-of-the-art clean rooms. Pellicles are attached to photo masks to avoid new printable defects. Currently, thickness of ArF dry pellicle is 833 nm. However, the thickness of pellicle is getting thinner and the extinction on pellicle is larger with immersion and off-axis illumination. In addition to that local thinning takes place with increased dose of 193 nm laser source. This thinning will cause loss of transmission and will make non-uniform transmission across the pellicle. As a result line width will be varied across the field. The pellicle thinning and transmission loss are measured with our new tool on the accuracy of less than 0.5 %. We will also report the line width and process window dependency on global pellicle thickness and local non-uniform pellicle thickness.

7973-103, Poster Session

Performance of a bilinear photoresist model

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A bilinear photoresist model expands the approach of a convolution kernel-style process models to include second-order effects. Using an effective acid concentration after post-exposure bake as the latent image, we approximate the reaction-diffusion operator as a second order Volterra series. The series expansion is calculated for several photoresists. Both the linear kernel and the Bilinear Resist Transfer Function (BRTF) are estimated at the same time, using a set of training images and varying exposure dose levels. The linear kernels of the Volterra series are found to have a Gaussian behavior, while the shape of BRTFs appear to vary greatly depending on exact details of photoresist composition. In several cases, the BRTF exhibits behavior that is clearly inconsistent with semi-definiteness assumptions which normally guide the estimation of optical bilinear transfer functions (TCCs). The accuracy of the estimated photoresist operator is studied using typical OPC validation through-pitch curves. The estimated operator is applied to a set of validation aerial images, and the resultant CD values are compared against full photoresist simulation. The accuracy of such calculations was found to be a significant improvement as compared to a best-fit linear model. Eigenfunctions of BTRFs are then identified and presented for several photoresist systems. In addition to expected Gaussian functions, some eigenfunctions are found to be represented by a Gaskill odd-impulse pair, , in the position space. The action of these functions and their similarities to a squared gradient operator is addressed.

7973-104, Poster Session

Applications of an inverse Mack model for negative-tone development simulation

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Dark field (DF) masks typically have lower image intensity and contrast which leads to poor process window for metal and contact layers as compared to poly lines which are exposed with light field (LF) masks. A negative tone development (NTD) process makes use of the superior imaging quality obtained with LF masks to print the metal and contact layers resulting in improved process window. Therefore, NTD process

is seen as one of the promising techniques to further extend the applications of ArF immersion lithography. In this paper, we introduce an inverse Mack development model to simulate the NTD process and demonstrate its prediction capability. Based on this inverse Mack development model, a NTD resist model calibration has been carried out and the model results are presented. With this model, various NTD application cases have been studied and simulations are compared with experiments: 1) in double patterning of both contacts and trenches, simulations reveal that an LF+NTD process helps to achieve a broader pitch range and smaller feature size compared to the traditional DF+PTD process. The benefits in exposure latitude and MEEF for both 1D and 2D patterns can be quantitatively determined through simulation. 2) The NTD process has been explored in double exposure with extreme off-axis illumination using line and space patterns with horizontal and vertical orientation, respectively, which create contact holes arrays down to 80nm pitch. This technique can be modeled by simulation. 3) Simulation can also be used to validate new process concepts such as printing semi-random contact holes by NTD and the dual-tone development process. In conclusion, this study demonstrates the predictive power of the inverse Mack model for NTD and its usefulness in NTD technique exploration and process development.

7973-105, Poster Session

A study of quantum lithography for diffraction limit

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Collective behavior of N-photon entangled states can reduce the effective wavelength by a factor of N, and consequentially beat the conventional diffraction limit of light. Its phenomenon can achieve arbitrary focal and image plane patterning with classical laser light at submultiples of the Rayleigh limit. In this research, nano-phenomena to beat the optical limitation are described and simulated. A theoretical proposal to emulate the NOON-state-based super-resolution using classical laser light and lambda-type atoms is also presented.

7973-106, Poster Session

Analytical equation for resolution of optical lithography with considering depth of focus

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We had already derived the analytical equation which reveals the resolution considering depth of focus. We have reviwed and found out more precise equation.

In this paper, we will derive the new equation. We apply this equation to invetigate many aspects of optical lithography. For example, we utilize this equation not only for the NA versus Resolution analysis but also for Resolution versus DOF analysis. This equation will be useful for prospecting the capabilities of optical lithography methods and for comparing them.

7973-108, Poster Session

Lithography process control using focus and dose optimisation technique

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In production, dose and focus parameters are fixed when the process is set up, nevertheless, natural variation are ever present. To correct these variations, a lithography process model has been built. A Bossung curve is first set up with high dimensional sensitivity to dose and focus pattern. The system takes advantage of accurate and precise top and bottom CD data produced by scatterometry measurement. Top and bottom CD are used to calculate best CD and, dose and focus sentivity coefficients. These coefficients will be used to extrapolate the focus and dose from the data measured on production wafers. The Ausschnitt1 deconvolution method analytically inverts the model, so that every measured (CDbot, CDtop) pair results in a dose/focus deviation (D, F).

The logical process flow would be that the wafers are exposed and processed in the lithography cluster. These same production wafers are measured on the scatterometry tool. Immediately after the measurements have been completed, the raw measurement data are passed (along with any needed coefficients) to the Ausschnitt deconvolution analyzer. At this moment, each point measured on the wafers can be associated to couple of dose and focus offsets. Then, on the photolithography tool, a new recipe is created with a dose and focus offset matrix. Finally, this new recipe can be applied on the next lot. With this method, dose and focus can be corrected, enabling seamless transition to technology nodes with reduced depth-of-focus (DOF).

Bare silicon monitor wafers have been the primary vehicle used for this study. The paper provides experimental evidence confirming that this method reduces CD variation by 50% and improves the slope of the photoresist.

[1] C. P. Ausschnitt, T. A. Brunner, "Distinguishing dose, focus and blur for lithography characterization and control", Proc. SPIE 6520 (2007)

7973-109, Poster Session

Process window improvement in the 2x-nm node DRAM contact hole using full-chip level model-based assist feature technology

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As the design rule shrinks down and k1 value is pushed down under 0.3, it is very hard to obtain enough process window and acceptable MEEF (Mask Error Enhancement Factor) for sub 2Xnm contact layers. Resolution Enhancement Techniques (RET) such as off-axis illumination and sub resolution assist features (SRAFs) is essential. Rule based assist features have generally been placed and adjusted according to the empirical rules. The complexity of these rules increases rapidly with shrinking features size requiring more wafer data for calibration and optimization. Recently, Model-based assist features (MBAFs) generation method is widely adopted over rule based assist features (RBAFs) placement. MBAF method can be used to obtain better coverage in complex 2D situation, reduce rule generation time when process condition such as design rule, illumination and stack conditions change. Also, have better process window than RBAF method.

In this paper, we have compared performance of MBAFs vs. RBAFs for 2Xnm-node DRAM contact holes. First, we co-optimize a source and mask for critical clips. Second, the selected source-mask combination is applied to model based assist feature placement for full-chip level database. And then, the results are compared with the conventional RBAFs with regard to process window, pattern fidelity and AF printability. As a result, it is shown that MBAFs methods have advantage for full-chip level DRAM contact hole patterning compared to RBAF.

7973-110, Poster Session

Feasibility study on the mask compensation of gate CD non-uniformity caused by etching process

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Tighter control of gate CD within a few nanometer range is quite common in most of semiconductor manufacturing places due to concern on the yield, which in turn tells us that there're hidden or uncounted factors

causing CD non-uniformity and the subsequent yield loss. Intra-field CD variation caused by etching process which was not so much emphasized at the beginning of gate process development could be one of them and thus lots of efforts has been taking to define its characteristics and fix it systematically as a part of OPC (optical proximity correction) in recent years. It's well known that geometrical features of the chip layout influences the etch performance in macroscopic and microscopic ways but how well those impact could be measured and compensated are still of concern. In this paper, the former factor is trying to be translated in terms of local pattern density measured in a critical radius and the latter one is in terms of distance to the nearest feature. The magnitude of each contribution has been measured for gate process by locating designed test patterns in the reticle of 0.18 um technology node. Increase in local pattern density accompanying the slow etch rate within a certain critical radius results in more than 5 nm CD drop. An attempt to acquire more comprehensive data related to this local pattern density has been made and the chip-scale compensation rule for the real application has been prepared accordingly. Meanwhile, the rising trend of post-etch CD with the increase in distance to nearest feature is well observed as expected but it never stops until the distance reaches 12um, which is much larger than the optical distance considered in the photolithography-based OPC setup. The final post-etch CD difference caused by this short-ranged geometrical influence is huge reaching 30 nm so that another challenge should be taken into consideration as the full compensation of the difference will ask you to sacrifice the lithographic process margin.

7973-38, Session 11

Ground rule considerations for the 20-nm logic node

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No abstract available

7973-39, Session 11

Optical lithography applied to 20-nm CMOS logic and SRAM

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Achieving 20nm designs with 193nm lithography is difficult even with immersion technology. At 20nm, the metal-1 pitch will be ~64nm, which is well below the 80nm limit for single exposure. In this work we extend on our earlier results [1-4] to show simulation-based patterning of both SRAMs and logic cells. This is consistent with the emerging industry consensus that regular designs and multiple exposure techniques will extend 193nm immersion as far down as 7nm [5].

The approach relies on 1D Gridded Design Rules with Lines/Cuts (1D GDR LC) selective double patterning. Due to the highly regular patterns of 1D GDR LC we are able to determine a sharp lithographic optimum as a result of numerical co-optimization of key layout parameters and lithography settings such as scanner illumination, etc. including realistic scanner capability.

Critical layers (holes/cuts in 1D GDR LC) consist of a number of identical hole/cut patterns with varying density. We use both SRAM and logic cells to show that after co-optimization CD error can be brought below 1nm at best focus conditions. We further consider manufacturability and show Depth of Focus (DOF), Normalized Illumination Log Slope (NILS) and Mask Error Enhancement Factor (MEEF) metrics before and after co-optimization. Finally, thanks to close ties to a leading scanner manufacturer we were able to consider realistic lens distortions using experimentally obtained Jones-Zernike expansions as well as realistic entrance pupil illumination.

Imaging properties of idealized scanner lens and illumination are compared to a realistic scanner lens model at 20nm. Direct process optimization in scanner variables as well as scanner-specific optimization of lithography settings and OPC are shown.

Co-Optimization of Layout and Lithography

Simultaneous optimization of layout patterns and lithography settings is made possible by the uniformity and repeatability of the lines/cuts patterns (Fig. 1, Fig. 2). We use direct optimization and experimentally validated lithography simulation for the critical cuts layers. Optimization variables are:

cuts geometry (width, height, hammer heads)

illumination of the scanner lens entrance pupil (Fig. 4)

groups of cuts in similar optical environments are biased to account for proximity effects (Fig. 3)

The optimization cost function was the RMS CD error across all cuts. Minimizing this cost function also reduces variation among cuts by getting all CDs close to the same target value.

Link to Scanner Data

A data base capturing the measured lens entrance pupil illumination was built in collaboration with an industry leading scanner manufacturer. As a result, we were able to carry out optimization directly in equipment variables such as lens zoom settings, apertures, etc. This ensures practical relevance of results and provides an interesting comparison between idealized and realistic illumination patterns. In addition, measured lens polarization effects and distortions are included using Jones-Zernike expansions, providing scanner-specific manufacturability predictions.

Results and Conclusions

Exposure and RET optimization for 1D GDR SRAM and standard cells was used to reduce CD variation and improve manufacturability of critical hole/cut layers. This reduction of variation substantially simplifies the layout and OPC and produces manufacturable designs including both SRAM and logic.

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7973-40, Session 11

3D litho modeling for ground rule development

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The ability to simulate lithographic processes in 3-dimensional space with actual topographic substrate could shorten the process development significantly. The 3rd dimension contains important information about resist profile shapes which, among other parameters, influence the post etch patterns. The capability to incorporate the effect of patterned underlayers in a 3-dimensional physical model that truly mimics the process on real wafers could be used to formulate robust ground rules for design.

We have shown as an example a block level simulation, where the resist critical dimension is determined by the presence of STI (shallow trench isolation) and/or patterned gate level underneath (Fig.1). The substantial change in litho critical dimensions with bare silicon stack to patterned underlayer stack is confirmed on wafer. A systematic study was undertaken to show how the critical dimensions variation is dependent on the underlying gate level and STI spacing. We will demonstrate how the results of such study could be used for creating ground rules which are truly dependent on the interaction between the current layer resist

and presence of patterned layer underneath.

We have also developed a new way to visualize lithographic process variations in 3-D space that is useful for simulation analysis that can prove very helpful in ground rule development and process optimization. Such visualization helps in easy determination of effects of certain ground rules in the entire process space. These so called process bands in 3-dimensions allow numbers of process parameters to be varied and lead to visualization of 3D contours in one image. In this paper we demonstrate the methodology for generating such litho process variation (PV) bands in 3-dimensions (Fig.2), based on a model calibrated in-house. The traditional PV bands are generated at one resist height and therefore could potentially fail to catch information such as bridging at the bottom. Such 3D depiction of process variation ahead of mask tapeout also could shorten the technology development cycle substantially. The plan is to plug in such model capability in the dataprep flow to flag issues or dispose critical structures in a more robust way.

7973-41, Session 11

Mask enhancer technology with source mask optimization (SMO) for 2x-nm node logic layout gate fabrication

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Resolution enhancement technologies (RETs) have been developed to reduce the minimum feature size in optical lithography. For 2Xnm-node, a strong RET combined with the hyper NA ArF immersion lithography with source and mask optimization (SMO) become necessary to realize sufficient resolution and depth of focus (DOF) , simultaneously. However, even if applying the single exposure with immersion lithography, the mask error enhancement factor (MEEF) issue is still remained. Furthermore, the patterning at line end gap of SRAM gate should be a big challenge for manufacturing logic devices. In order to overcome these challenges, we have developed a new RET using attenuated mask with phase shifting aperture, named “Mask Enhancer”. In this study, we applied Mask Enhancer on gate patterning with optimized illumination source shape, and ensured that Mask Enhancer can improve MEEF and pattern shape at line-end of SRAM gate.

Mask Enhancer for line fabrication consists of two features, those are the main feature consist of binary or gray tone attenuated layer on open field, and the phase shifter aperture inside of main feature as shown in Fig 1. The phase of shifter aperture has the opposite phase to open field and main feature. We can enhance the image contrast of the line pattern with this mask configuration as shown in Fig 2. In this study, we adopt a optimal illumination source shape combined with Mask Enhancer to balance lithographic performance for the resolution limit at line end gap to ensure a sufficient process margin for SRAM gate layout pattern.

In this study, we demonstrated the SRAM gate layout printing by using Mask Enhancer. Fig 3 shows a simulation result of a gate patterning at line end gap. We obtained the acceptable value of DOF, EL and MEEF less than 4 at 38nm gate gap. Thus, Mask Enhancer can achieve 2Xnm-node SRAM gate printing without double patterning. We strongly propose that Mask Enhancer is one of the most effective solutions for logic gate fabrication for 2Xnm node.

7973-42, Session 11

Evaluation of a new mask topography model

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Departure from the simple Kirchhoff thin mask approximation was revealed in the early 1990s with the use of alternating aperture phase-shifting masks as the depth of the mask patterns was larger than the exposure wavelength. These effects were simulated using slow but accurate methods such as FDTD and RCWA. Correction methodologies including quartz undercut and sizing were also implemented. Fifteen years later, the mask main feature sizes were now smaller than the exposure wavelength resulting in mask polarization effects even for binary and attenuated phase-shifting masks. With the advent of model-based OPC, a fast simulation of these effects was now necessary in order to apply corrections. Various approaches were proposed to account for these effects including for example the placement of additional polygons with adjustable phase and transmission along the edge of the patterns. More recently we have implemented a fast and accurate mask topography model [1]. This model is created using the mask topography information and can be directly applied to the mask data with no prior calibration.

In this paper we will investigate the accuracy of the mask topography model for a wide variety of test structures in 1D and 2D environments. Such test structures will also include complex mask shapes such as the one created by inverse lithography and source mask optimization tools. One particular aspect of this study is to evaluate the impact of mask corner rounding on the model accuracy.

[1] Pierrat, C., Proceedings of SPIE Vol. 7823, 782330 (2010).

7973-43, Session 11

High-performance intensity slope correction method for global process variability band improvement and printability enhancement in RET applications

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Further reduction of critical dimension (CD) imposes new challenges on resolution enhancement technique (RET), especially in case of dense layouts composed, in part, of broken pitches (BP). BP can be defined as irregular node pitch structures that do not form well-pronounced pitch array. For such layouts, printability becomes a function of local placement configuration due to the interference of scattered field. This effect becomes significant in contemporary optical immersion lithography due to high sensitivity of sub-resolution printability to the intensity perturbations near the threshold. Even at nominal process conditions, the BP pattern fidelity transfer to wafer is done at the edge of technological abilities. Variation of process window in such structures can lead with high probability to (soft) pinching/bridging which makes production of error-free resist contour questionable without involvement of process window (PW) aware optical proximity correction (OPC). It is doubtful, however, that traditional PWOPC can be efficiently applied for the structures under consideration because it suffers from a) requirement of prohibitively expensive additional simulations with modified process window variables and b) predominantly local treatment of detected hot spots without account for violation free surrounding environment.

Arguably, formation of robust BP image may strongly depend on mutual impact of neighboring areas. This global dependency may be strong enough to prevent PWOPC from the achievement of an optimal local solution. It can also lead to divergence of the solution by generating new problems as a result of the attempt to fix the hot spots under consideration.

In this presentation, the preliminary results obtained from application of qualitatively new Intensity Slope Correction (ISC) method for the improvement of dense layout printability during OPC are revealed. Unlike traditional PWOPC, this method does not require additional process window simulations to make decision about local mask treatments. Instead, ISC facilitates global process variability band (PVband) improvement on-the-fly using the information about intensity distribution available during OPC simulation of nominal image. The PW hypercube is involved at verification stage only. The results were obtained in the framework of development of Mentor Model-Based Double Dipole Lithography tool. They suggest that ISC is capable of resolving printability problems by making intelligent tradeoffs between edge placement error (EPE) and PVband. As a result, layouts with irremovable by traditional PWOPC soft pinches/bridges become error free. This is achieved through the iterative process of global cost minimization using a unique feedback mechanism derived from the intensity distribution information. The overhead CPU time needed for ISC-driven OPC is

unprecedentedly small - just a fraction of pure OPC runtime per iteration. Because of the global nature of ISC operation, the narrower integral PVband as well as enhanced printability is achieved through the entire layout. The quality of the final result is characterized in terms of mismatch factor defined as cumulative areas of target XOR nominal image, (soft) pinch/bride markers, and PVband.

7973-12, Session 12

Comparing double-patterning methods for logic design routing

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Double Patterning (DP) is the only solution to enable the scaling for advanced technology nodes before EUV or any other advanced patterning techniques become available. In general, there are two major double patterning techniques: Litho-Etch-Litho-Etch (LELE) and sidewall spacer technology, a Self-Aligned Double Patterning technique (SADP). While numerous papers have previously compared these techniques on wafer process capabilities and processing costs, no rigorous paper has been presented studying the design rule capabilities and dies cost. Ultimately, the preferred double patterning method should encompass the best solution space based on four factors: manufacturability, design ability, extendibility and cost. In the past, we compared SADP with LELE in terms of overlay, critical design rules, extendibility to smaller pitch and CD control etc.1 In this paper, we will present the impact of each double patterning technique on logic design, and compare the resulting die-size capabilities of SADP and LELE.

SADP and LELE double patterning have different critical design rules, such as line end-to-end, end-to-side, and the enclosure of via in metal etc. These differences arise from their different decomposition natures and their different sensitivities to process variations like overlay. Additionally, the MRC and DRC rules impact SADP and LELE very differently. It is therefore important to supplement the previous wafer level comparisons with these design based comparisons to complete the overall technology assessments.

In this paper we address the following key questions:

1. How would the design be impacted, more/less restrictive, with different DP techniques when all the decomposition strategies are understood for SADP and LELE?

2. Which set of design rules will ultimately enable the smallest die?

3. How much does the design need to scale in order to meet the cost expectation when the process is taken into consideration

Thus, this paper ultimately presents the comparison results of a SADP compliant design with a LELE compliant design, when routed thru metal 5.

7973-13, Session 12

Single-exposure contacts are dead: long live single-exposure contacts

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Even if not breaking through the ultimate single exposure resolution limit, using double patterning lithography processes can offer significant yield enhancement for challenging circuit designs. This was believed to be true for contact levels in particular due to its two-dimensional nature. While logic standard cell design could potentially live with a relaxed minimum pitch to stay single exposure compatible - requirements for a competitive SRAM design of advanced technology nodes could not. Hence, double patterning for the contact levels seemed to be the answer...

The sentiment changed as 193nm resist development still progressed significantly over the last years. Printing 100nm dense contact arrays robustly became very well possible. Consequently, the question needed to be raised again, whether single exposure for the contact levels of advanced technology nodes such as the 28nm logic node would be a valid option. This thought was also supported by the fact that typical SRAM designs do not really benefit much from two layer decomposition (i.e. the process of dividing the layout design into first and second exposures). The available RET choices were still limited, because the remaining minimum pitch resolution still drove a fairly aggressive illumination typically accompanied by intermediate pitch printing issues - pitches some of the decomposed SRAM contacts would exactly land on.

The paper describes a true process/design co-optimization effort based on an SRAM design to enable a single exposure contact process for the 28nm technology half node.

For a start, a conceptual change to the wiring concept was implemented to the standard SRAM design. The resulting individual contact layer elements may seem even more resolution critical to the casual observer. But in reality, the flexibility for source-mask optimization had been significantly improved. In a second step, wafer targets and mask dimension options (using various kinds of OPC methods such as inverse lithography, rules-based SRAFs, conventional OPC) were run through several optimization iterations. This included also interlevel considerations due to stringent overlap requirements. Several promising SRAM design as well as mask options were identified and experimentally verified to finally converge to an optimum mask and wafer target layout. Said optimum solution still supports an automated OPC approach using standard EDA tools and off the shelf OPC solutions.

In a last step, a 1M electrically testable SRAM was designed and manufactured together with alternative SRAM designs and process options.

After explaining the changes to the wiring of the SRAM design, the paper discusses in great detail various mask optimization solutions (inverse lithography as well as various sophisticated OPC solutions) and their consequences on wafer target and printability. Simulation and experimental results are compared and the concluding optimized solution is explained. Furthermore, some key litho and etch process elements that became the single exposure process enabler are explained in more detail. Finally, the authors will take a look at electrical results of the 1M electrically testable SRAM as the ultimate proof of concept.

7973-45, Session 13

Polarization holograms for source-mask optimization

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The semiconductor industry has used computer-generated holograms (CGHs) as an efficient way to form mask illumination patterns for several years. By implementing a CGH, custom mask illumination patterns, like ring, dipole, quadrapole, etc., can be efficiently used. This report discusses arbitrary control of irradiance and polarization for mask illumination. The technique employs polarization synthesis, where light diffracted from two or more CGH patterns combine to produce the desired irradiance and polarization distributions in the image plane. A tangentially polarized annulus was chosen as the target image for all designs, where irradiance is a uniform around the annulus. Ideally, the diffraction efficiency should be at least 70% and the ratio of polarization

(RoP) should be at least 0.90. Using the synthesis technique, pairs of CGHs are illuminated, where one CGH produces a vertically polarized pattern and the other produces a horizontally polarized pattern. Coherent addition of the two pattern channels, which overlap in the target field, produces tangential polarization. Although the primary application is for optical lithography, designs and experiments in this project primarily use a laser wavelength of 632.8nm. In order to realize a PCGH that produces the desired synthesized image patterns, mathematical developments were necessary. The primary realization is that synthesized arbitrary image irradiance and polarization can only be accomplished with the combination of two separate planar elements. One element is used to establish a spatially varying polarization state, and the second element is used to produce a spatially varying phase distribution that adds with the first element transmission to produce the PCGH effect. A key component to the success of this project is the development of a software design technique using a modified Gertzberg-Saxton algorithm that uses a common diffuser between the two polarization channels. Three structures were chosen for detailed design and experiments. Two structures are interlaced, where CGHs are overlapped to produce synthesis. A column-based interlacing was used, where alternate columns of each component CGH are combined in a single plane. The first structure consisted of two Ronchi gratings that produced alternating orthogonal polarization states on an interlaced CGH. The second structure is similar, except an etched uniaxial crystal grating is used as the illuminator instead of the Ronchi gratings. The third structure was a binary uniaxial crystal plate combined with an isotropic phase plate. This structure is not interlaced, so all of the energy ideally goes into the primary diffraction order. Ratio of polarization (RoP) was close to the target of 0.90 for all three structures. Diffraction efficiency (DE) was only measured for the third structure, because interlacing exhibited 1st diffracted orders that reduced overall efficiency. DE for the third structure was close to the 70% target, and losses are most probably due to scattering in the uniaxial crystal material. Improvement of fabrication and alignment techniques could increase RoP and DE to nearly ideal values.

7973-46, Session 13

Extending SMO into the lens pupil domain

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As nanolithography is pushed to smaller dimensions, the yield of the process tends to suffer due to sub-wavelength imaging effects. Several resolution enhancement technologies have been employed in order to improve the image quality, such as source mask optimization (SMO), which finely tunes the process by simultaneously optimizing the source shape and mask features. However, SMO has a limitation in that it fails to compensate for undesired phase induced effects because the source and mask have little control over the phase. The planar resist interface induces spherical aberration which results in a pitch-dependent focal point. For features on the order of /4, the topography of the mask induces aberrations which brings asymmetry to the focus-exposure matrix (FEM) and ultimately decreases the process window. This paper examines the dependency of the FEM asymmetry on factors such as the number of diffraction orders that contribute to imaging, the illumination shape, and standing waves. It is shown that lens induced spherical aberration strongly impacts the symmetry of the FEM.

In this work, phase correction is achieved by including the pupil plane in the optimization. It is shown that a phase pupil function can correct for effects including the shift of best focus and the tilt in the FEM. A pupil function with an optimized coefficient of negative spherical aberration compensates for the spherical aberration induced by the mask and photoresist. In Figure 1, the FEM with the optimized pupil function shows a 50% improvement in depth of focus (DOF) over the FEM with no induced spherical aberration. This example is for a pitch of 90 nm on an alternating phase shift mask with 1:1 features. The illumination source is =193 nm =0.3 and the NA is 1.35. The simulation is performed in KLA-Tencor Prolith. In order to drive to an improved solution, simultaneous optimization of source, mask, and pupil parameters is performed. Given the large parameter space, smart algorithms, such as gradient descent and evolutionary algorithms, are employed to converge to a solution. Each algorithm is evaluated for its success in the lithographic optimization problem.

7973-47, Session 13

Production-ready full-chip mask synthesis using inverse lithography technology

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It is well known in the industry that the technology nodes from 32nm HP (logic 28nm node) and below will require model based SRAF / OPC for critical layers to meet production required process windows. Since the seminal paper by Saleh and Sayegh thirty years ago, the idea of using inverse methods to solve mask layout problems has been receiving increasing attention as design sizes have been steadily shrinking. ILT in its present form represents an attempt to construct the inverse solution to a constrained problem where the constraints are all possible phenomena which can be simulated, including: DOF, sidelobes, MRC, MEEF, EL, shot-count, and other effects. Given current manufacturing constraints and process window requirements, inverse solutions must use all possible degrees of freedom to synthesize a mask.

Various forms of inverse solutions differ greatly with respect to lithographic performance and mask complexity. Factors responsible for their differences include composition of the cost function that is minimized, constraints applied during optimization to ensure MRC compliance and limit complexity, and the data structure used to represent mask patterns. In this paper we describe the level set method to represent mask patterns, which allows the necessary degrees of freedom for required lithographic performance, and show how to derive Manhattan mask patterns from it, which can be manufactured with controllable complexity and limited shot-counts. We will demonstrate how full chip ILT masks can control e-beam write-time to the level comparable to traditional OPC masks, providing a solution with maximized lithographic performance and manageable cost of ownership that is vital to sub-30nm node IC manufacturing.

7973-48, Session 13

A numerical continuation approach to inverse lithography

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Pixel-based inverse lithography has been extensively studied as a mask optimization method for low-k1 optical lithography. When partially coherent kernels are used, the problem is inherently a constrained non-linear optimization problem, of which the prohibitive runtime poses a challenge. Another issue is that the resulting masks can be highly fragmented, which pose a mask manufacturability problem.

In this paper we proposed a novel approach to the inverse lithography problem. To address the runtime issue, we use the barrier method to convert the constrained optimization problem into an unconstrained one. The constraint from photo-resist thresholding is modeled by a sigmoid function. The constraint of the binary mask is modeled by another parametrized sigmoid function. Because the mask transformation is tunable, it significantly helps in addressing issues of both the choice of the initial mask and convergence rate. When a steep sigmoid function is used, numerically the problem is identical to the original binary mask. However, since the sigmoid function is a C1 function, we can rely on the Jacobian to apply an unconstrained optimization algorithm. Our method is inspired by an earlier proposal of barrier method approach. However, we further cast the overall optimization flow as a homotopy continuation problem to address the two pertinent issues, as will be described next.

A more significant benefit of the parametrized sigmoid function is that when the controlling parameter is small, the Jacobian of the image

differences tends to ``leak" into the neighboring locations. Hence the cost function of the image difference tends to introduce a clustered change on the mask, which alleviates the fragmentation tendency of the earlier pixel-based optimization methods. As a result the generated masks are much less likely to have very fine features as in the other inverse lithography methods. By gradually ``harden" the controlling sigmoid parameter, a coarsely grained mask can be achieved without using the ``regularization" term as in the earlier approach.

The computational task now becomes how to dynamically adjust the controlling sigmoid parameter in the optimization process. This problem can be cast as a homotopy continuation problem, in which the controlling parameter can be treated as an independent variable governed by an ordinary differential equation. The topic has been widely studied and there exist many efficient numerical routines. In our approach, we use a numerical continuation method to achieve high computational efficiency. The flow starts with a ``soft" controlling sigmoid parameter. The sigmoid parameter is dynamically adjusted while in the mean time, the mask pixels are tuned using a unconstrained optimization method. The optimization loop terminates when the sigmoid parameter is sufficiently large and the wafer image difference is sufficiently small.

The effectiveness of the method is demonstrated in a state-of-the-art 193nm lithography environment. In average the method converges in 120 iterations for all features in a 1600 x 1600 optical window. The final mask does not present the fragmented small features and has excellent manufacturability after a post-processing step. Good image fidelity is achieved compared to masks generated by traditional RET methods.

7973-49, Session 13

A study of source mask optimization for logic device through experiment and simulations

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Source and Mask co-Optimization (SMO) plays an increasingly important role in the advanced RETs required to continue shrinking designs in the low-k1 lithography regime. Instead of costly double pattering patterning techniques, SMO has been explored as an enabling technology for low-k1 design node. It is clear that intensive optimization of the fundamental degrees of freedom in the optical system allows for the creation of non-intuitive solutions in both the mask and the source, which leads to improved lithographic performance.

In this work, combination of freeform source and mask shape for logic device was searched in order to enable the printing of critical SRAMs along with a range of horizontal and vertical gratings. In terms of simulation, critical factors such as Mask Error Enhancement Factor (MEEF), size of image blur and cost functions were studied. Mask effects including thickness of photomask and minimum size of mask feature were also considered because mask effects get critical for SMO mask. Based on simulation results, the corresponding experimental results were investigated as the evidence of the performance advantage by SMO. As a result, it is shown that SMO represents a significant advancement over state-of-the-art as well as reduces the number of exposure time.

7973-50, Session 14

Practical performance and its enabling technologies in immersion scanners for the double-patterning generation

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We demonstrated excellent performance of our cutting edge immersion lithography tool S620D (Fig1) based on the new platform "Streamlign", focusing mainly on machine evaluation data at SPIE2010 last year. Now, many S620Ds are working at our customers' fabs and are contributing to device manufacturing. In this paper/presentation, introducing the latest factory data, our techniques which enable superior yield and further productivity in actual wafer processing will be introduced.

EUV is still expected to be the most favorable technique for device shrink to the 22nm hp node or beyond because of its resolution capability. However, it is also true that we still face technical and economic difficulties regarding EUV and it is not clear whether or not EUV will be able to dominate future lithography. This is the reason why we have to extend ArF immersion lithography with a variety of techniques such as Double Patterning or Source Mask Optimization.

As is well known, we must overcome several practical issues if we are to realize device shrinking without traditional techniques like NA expansion or wave length enhancement. Extremely tight overlay performance will be required for pitch splitting double patterning, for example, and we need to control the image plane and the aberration of the optics much more severely. Of course these improvements must also be achieved with enough productivity (throughput). In order to meet all of the requirements for mass production at actual customer factories, we must deal with many variable factors.

For instance, one of the variable factors is the characteristics of processed wafers such as non-flatness, grid distortion, steep topology around the edge, or topography of the previous layers' patterns. These factors generally influence overlay or auto focus accuracy. Another variable is the difference of exposure conditions between layers which include illumination conditions, dose, reticle transmittance, and the alignment marks. Especially exposure induced heating is the key issue with today's enhanced throughput capability in terms of achieving both accuracy and productivity. At some mass production factories, typically at foundries, many kinds of products are manufactured in parallel. But to obtain better accuracy, we sometimes need to optimize machine parameters for each product, and in that case, it is also important to achieve quick tuning for them and to minimize the overhead for each product.

As stated above, we have to prepare various techniques in order to minimize the gap between machine inspection data and practical performance at customer sites. This paper/presentation discusses the techniques and the data mainly from this point of view.

7973-51, Session 14

Advanced wavefront engineering for improved imaging and overlay applications on a 1.35 NA immersion scanner

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Leading edge lithography is moving to the 22 nm node and beyond. Although EUV lithography is developing at high pace, it is believed that 193 nm immersion will be extended further as well. With water as practical immersion fluid, increase of lens NA is not possible anymore and thus other type of optical system improvements are needed to assure patterning at the 22 nm node. In previous papers we introduced advanced illumination pupil engineering using the FlexRay illumination concept [Proc. SPIE 76401P (Mar. 3, 2010), Proc. SPIE 75200Y (2009)]. With FlexRay, illumination sources can be optimized towards the application without any major constraint on the pupil shape. In this paper we will present the FlexWave concept allowing further imaging enhancement.

FlexWave is a new high resolution lens manipulator, performing both static and dynamic wavefront correction and control. Wavefront control with FlexWave minimizes lens aberrations under high productivity usage of the scanner, hence maintaining overlay and focus performance. This optical phase tuning can be used to compensate for process induced effects. Low k1 imaging artifacts - like reticle and resist 3D effects - grow with smaller mask dimensions and more aggressive illumination sources. This results in more dominant feature dependent focus shifts and pattern

shifts. With FlexWave the phase can be tuned with a high degree of flexibility to enlarge the common process window and improve CDU. Wavefront optimization towards different performance metrics for full chip designs can be realized with LithoTuner's computational lithography techniques.

In this paper we will describe the basic principle of FlexWave and discuss experimental data on imaging, focus and overlay. For this purpose we integrated the FlexWave module in a 1.35 NA immersion scanner.

7973-52, Session 14

Pupilgram adjusting scheme using intelligent illuminator for ArF immersion exposure tool

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Source Mask Optimization (SMO) is one of the most important techniques available for extending ArF immersion lithography. However, imaging with a small k1 factor (~0.3 or smaller) is very sensitive to errors in the imaging system, such as pupilgram shape, lens apodization, etc. As a result, the real source shape must be re-adjusted to realize expected imaging performance as may be seen, for example, in an OPE curve. The intelligent illuminator can modify the pupilgram with high spatial and intensity resolution. The question is how to adjust the pupilgram parameters properly to match target OPE without sacrificing the imaging performance expected from the SMO solution.

In this paper we present and describe a pupilgram adjusting method that can effectively control the various illuminator parameters. The method uses pupilgram modulation functions, which are similar to Zernike polynomials used in wavefront analysis, to describe the optimal pupilgram adjustment, and the resulting modulation can then be realized by the intelligent illuminator.

We demonstrate the effect of this method and the capability of the intelligent illuminator in this paper. Using this method, SMO solutions will be more realistic and practical for extending the ArF immersion lithography.

7973-53, Session 14

Scanner matching for standard and freeform illumination shapes using FlexRay

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IC manufacturers have a strong demand for transferring a working process from one scanner to another. Recently, a programmable illuminator (FlexRayTM) became available for ArF scanners that, besides all the parameterized source shapes of the earlier AerialTM illuminator can also produce any desired freeform source shape. As a consequence, a fabrication environment may have scanners with each of the illuminator types so both FlexRay-to-Aerial and FlexRay-to-FlexRay matching is of interest. Moreover, the FlexRay illuminator itself is interesting from a matching point-of-view, as numerous degrees of freedom are added to the matching tuning space.

In this paper, we experimentally study the impact of the illuminator (FlexRay or Aerial) on the proximity behavior. We focus both on parameterized (Annular, Quasar, CQuad) as on freeform source shapes that are suited for advanced contact and metal layer printing at 1.35 NA. We investigate the various FlexRay approaches that can be used for matching different 1.35 NA ArF scanners. Indeed, the standard set of tuning knobs (NA, Sigma, Focus Drilling) is now expanded with new parameters, including source intensity manipulators. The CD sensitivities to each of these parameters, which we obtain both from simulation and experiment, are used for determining the optimal matching conditions. In addition, a different matching approach will be discussed in which one moves away from this 'sensitivity based' type of matching and uses advanced computational source optimization techniques to perform e.g. a pixel-based matching.

This work illustrates how advanced source manipulation using the FlexRay illuminator enhances the matching capabilities for a broad application range.

7973-54, Session 14

Light source technology advances to enable high-volume manufacturing for ArF immersion double patterning

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Double patterning (DP) lithography places significant demands not only on the optical performance of the light source (higher power, improved parametric stability), but also on high uptime in order to meet the higher throughput requirements of the litho cell. In this paper, we will describe the product improvements that Cymer has developed which deliver improved performance while achieving better reliability and resultant uptime as embodied in the XLR 600ix light source from Cymer.

One challenge for double patterning lithography is to develop a cost-effective solution using a process that effectively doubles the lithography steps required for critical layers. As a result, the light source requirements for DP fall into 3 main categories: (a) higher power to enable higher throughput on the scanner, (b) lower operating costs to offset the increased number of process steps, and (c) high stability of optical parameters to support more stringent process requirements. Previously, we reported on the XLR 600i (6kHz, 90W @15mJ) introduced in 2009 to enable DP through improved optical performance stability and higher power. Here, we will report on the introduction of additional capabilities that further enhance ArF immersion lithography.

As features shrink, certain layers are further challenged with depth-of-focus (DOF) limitations, particularly for contact or via layers. We have recently introduced a method to improve DOF through the use of light source bandwidth broadening. This method provides all the advantages of DOF improvements without any negative repercussions, and required the development of advanced bandwidth metrology to accurately monitor and control this process.

With the introduction of more complex illumination schemes, especially pixellated illumination, there is a higher reliance on the light source beam stability (pointing and divergence). To this end, we have developed additional on-board metrology that provides real-time near- and far-field data, as well as pointing and polarization. This enables a higher level of light source to scanner optimization and ultimately the ability to implement closed-loop control where needed.

Finally, to further enhance litho cell productivity, we have continued to minimize the need for service events related to gas management for the light source discharge chamber. With the introduction of GLX several years ago, we dramatically reduced the frequency of gas management functions that were necessary to maintain consistent operation by a factor of 20, resulting in significant improvements in availability. More recently, we have developed a solution that optimizes the gas functions near-real-time with the goal of ultimately making gas function events invisible to the litho cell.

7973-55, Session 14

Ecology and high-durability injection locked laser with flexible power for double-patterning ArF immersion lithography

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ArF immersion technology has been used widely in volume production for 45nm node. For 32nm node and beyond, double patterning technology with ArF immersion lithography is considered to be the main stream solution until EUV becomes ready. To achieve this, market demands for ArF light source are getting more severe, for example, higher power and narrower spectral bandwidth are required for higher throughput and higher NA lithography respectively.

We have already released an injection lock ArF excimer laser with high output power and high repetition rate for higher throughput and higher NA first immersion tool: GT60A (60W/6000Hz/0.5pm (E95)) to the ArF immersion market in Q1 2006. In the technology for 45nm and beyond, a light source is required to offer a narrower spectrum and high average laser power. We succeeded in releasing the next generation model, GT61A (6kHz/60W/0.30pm (E95)) with narrower spectral bandwidth used for high-NA lithography at the 45nm node in 2007. Both a newly developed high-precision E95 measuring module and a stabilization control system are provided as standard features, allowing a highly stable spectrum performance throughout the entire product lifetime. The higher throughput model, GT62A (6kHz/90W/0.30pm (E95)) with the higher power was developed for double patterning lithography at the 32nm node. For the GT62A, a variety of technologies to reduce the running cost of laser is introduced, which is applicable backward for the previous GigaTwin series lasers. In addition, the latest generation model with flexible output power (60W - 90W) laser GT62A-1SxE is the laser matching the enhancement technology of advanced illumination systems. For example, in order to provide illumination power optimum for resist sensitivity, it has extendable power from 60W to 90W. All laser systems are built on the GigaTwin platform, a common and reliability-proven platform.

This laser meets the specification of the advanced illumination system as a matter of course, it not only reduces CoC(Cost of Consumable) and CoD(Cost of Downtime); it achieved ecological performances to reduce CoE(Cost of Energy) like electric power or gas consumption.

We have confirmed ecology and reliability of duration test under the regulated operation condition with flexible power 60-90W.

We show the ecology and high durability data of GT62A-1SxE in addition to the results the field reliability and availability of our Giga Twin series (GT6XA). We also show technologies which made these performances and its actual data. A number of innovative and unique technologies are implemented on GT62A.

- Reduce total cost (Cost of Consumables, Cost of Downtime and Cost of Energy & Environment)
- High durability : even if the output power changed
- Support the latest illumination optical system
- Support E95 stability and adjustability

Conference 7974: Design for Manufacturability through Design-Process Integration V

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Design for Manufacturability through Design-Process Integration V

7974-01, Session 1

Moore's Law in the innovation era

M. T. Bohr, Intel Corp. (United States)

No abstract available

7974-02, Session 1

Achieving Moore

J. Kibarian, PDF Solutions Inc. (United States)

No abstract available

7974-03, Session 1

DFM: past, present, and future

M. E. Mason, Texas Instruments Inc. (United States)

No abstract available

7974-22, Poster Session

Extending analog design scaling to sub-wavelength lithography: co-optimization of RET and photomasks

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Historically, scaling in Analog Technologies was characterized by adapting design rules and processes of mature CMOS technologies and adding analog components to them. This approach had worked very well in the past with Texas Instruments (TI) deploying High-Density Analog (130nm) and High-Power BiCMOS (180nm) even in the lithographically sub-wavelength regime. The digital technologies manufactured under the low-k regime were enabled by intensive manipulation of design data with liberal use of OPC and other RET methodologies. To transfer these intricate designs, now fractured with serifs and jogs, on the photomask with reasonable fidelity required a quantum jump in reticle manufacturing by requiring the use of high-performance 50keV Vector tools. The down-side of this method has been an increase in complexity of the design to reticle to Si flow with the accompanying increases in cost and cycle-time of the reticle set. With designers integrating increasingly larger number of components on a chip on one hand with the higher reticle cost being a barrier to entry on the other hand, the cumulative number of designs taped-out from 180nm node to 65nm node at TI has declined by over 90% going with only a handful migrating to 45nm. This business proposition needs to be fundamentally altered since the Analog technology platforms deploy very high number of devices that require the design and reticle costs to be amortized over a smaller volume of wafers.

In this paper we focus on the mask requirements for 110nm half-node BiCMOS process. Among other things, this process requires a high density CMOS process along with high-power Bipolar, LDMOS and DECMOS components. The high voltage components are characterized by Active and Gate geometries that are curved (non-manhattan). The Contacts are allowed to be merged to form Rectangular or Stretched Contacts to allow conductance of high currents and in other cases serve as local interconnect layer. To meet customer needs but still manage the Computational Lithography overhead as well as the patterning process performance, we evaluate this process in terms of RET and Photomask co-optimization. We compare CD and device performance on wafer from standard CMOS-derived mask processes with the optimized choice for analog. We analyze the changes in OPC calibration necessary to switch to the new mask process. The overall goal of the project was to get improved performance at lower cost and shorter cycle times. The presence of curved features in the data is particularly detrimental to the write time on a 50KeV mask writer due to the increased shot count (see Figure 1 below). This is just one example of how this collaborative approach improved cost, cycle-time and capacity within the design, mask data prep and mask manufacturing portion of the process flow with little to no capital cost for Toppan and no impact to TI on yields and/or product performance. Not only does the Analog lithography and process have unique challenges, but the Analog product space is broad and not as concentrated as traditional digital CMOS. NRE and prototyping are still critical to product development and product variants, even though the actual design rule is now more mature. Through collaboration these unique Analog challenges are being addressed.

7974-23, Poster Session

Self-aligned double-patterning (SADP) friendly detailed routing

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Amongst the possible double patterning strategies for sub 32nm processes, self-aligned double patterning (SADP) has moved from Flash specific processes to more general purpose devices. The reason is that while Litho-etch-Litho-etc (LELE) process were originally preferred due to its simplicity and relative low cost, its sensitivity to overlay errors has prompted the search of other method that are not as sensitive to overlay.

Layout decomposition is a major challenge for all double patterning methods. The main problem is due to the fact that not all native layout configurations are colorable, and therefore the selective insertion of feature breaks (cuts) becomes one of the major sources of layout sensitivity to process variations. DPL-oblivious layouts are even more challenging for SADP, where cuts are prohibited because they cause irresolvable pinching problems.

In general, there are two main approaches to achieve double patterning compliant layouts. The first one considers the DPL-specific manufacturability requirements, i.e. minimum number of cuts and maximum overlay robustness, during the decomposition process of a given layout. The second one translates the DPL compliance into a set of cost metrics, which are considered by detailed router to find the optimal routing solution in terms of DPL constraints and traditional design objectives such as wire-length.

In this paper, a SADP-ware detailed routing is proposed. This method performs detailed routing and layout decomposition concurrently to prevent the creation of litho-limited layout configurations. The approach was derived from a series of experiments that highlighted a common set of layout configurations which cause litho failures in spite of applying the most aggressive OPC conditions. We have observed that the trim patterns should be protected by a Mandrel pattern or be moved away to sparsely populated areas of the layout where the addition of assist features can make them more robust. In addition, we maximize the uniformity of the pattern density to be defined on the trim mask as this mask. To our best knowledge, this is the first attempt to provide a SADP-aware detailed router.

As the first step of detailed routing, we use a graph coloring algorithm to color routing blockages such as pins. We also assume that both pins of a net must be assigned to the same mask (Mandrel or Trim) without

causing a pitch violation. Otherwise, the conflicting nets are discarded and reported to the place engine as un-routable nets. After pin coloring, some nets are pre-assigned to either the Mandrel or the Trim mask while the preferred mask for others will be determined during net routing.. During this process, the optimal path in either Mandrel or Trim mask is found with respect to its wire-length and its overall benefit for SADP compliance. Next, the neighborhood of the selected path is updated. The neighborhood state attaches information to the detailed routing grids about their preference for being occupied by paths passing through Mandrel and Trim masks. In this way, the neighborhood state shows the proximity effects that certain features can have with respect to other layout patterns, which are imaged in the same or different mask level. We propose a cost function to determine the penalty of inserting a trim element at a critical distance from a Mandrel feature which in turn has shown to cause the worst litho performance.

While this approach does not fully guarantee that the layout will be manufacturable due to complex interplay between other pattern transfer effects like etch, dielectric deposition, etc. The litho analysis shows that there is a considerable improvement in the reduction of litho-induced errors.

7974-24, Poster Session

Partial least squares-preconditioned importance sampling for SRAM yield estimation

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Quick estimation of parametric IC yield is necessary to correctly assess the impact of process variability without inducing overdesign. The classic Monte Carlo method is inefficient in estimating very low failure probability (high yield), as commonly found in SRAM design. To circumvent this difficulty, several researchers adopted the importance sampling method [1, 2], of which the success hinges on the choice of the biased distribution. A popular method [2] based on the idea of "norm-minimization" picks a shift point through a random search, and moves the center of the original distribution to that point. However, the norm-minimization procedure cannot guarantee the quality of the point (and therefore the efficiency of the simulation) due to the random nature of the search algorithm.

In an attempt to reduce the problem into a simple line search, we propose an alternative method based on partial least squares (PLS) regression. The method starts with PLS regression of the performance metric against the parameters representing process variability. The resulting weighting coefficients determine a single "optimal" direction in the process parameter space, effectively reducing a high dimensional search into a simple line search. Through this line search a boundary point is located, and the biased importance sampling distribution is placed around that point. The rationale behind the method is that the direction picked by PLS gives the best explanation of the covariance between the relevant performance metric and the underlying process variability.

We compare the proposed method with the norm-minimization method via the example of SRAM failure probability estimation. The threshold voltage variation across the SRAM cell is described by a hierarchical model [3]. To have a fair comparison, we repeat the entire procedure of both methods 50 times. Each time we use a randomly generated set of 500 process samples in order to perform PLS in our method and 3,000 process samples in order to drive the norm minimization procedure. Both methods are required to reach the same convergence criterion of a standard error of less than 10% at the importance sampling stage. The failure probability being simulated is around 1e-5. Our simulation results show that the sample size required to reach convergence for the proposed method is consistently around 1e3, whereas that in norm-minimization method varies significantly, and is often orders of magnitude larger. This indicates that the preconditioning step assisted by PLS regression generates a better biased distribution than that given by norm-minimization, and the quality of the simulation is highly repeatable. We conclude that the proposed method provides a robust approach towards simulating rare events. The failure point as picked through PLS regression can be further used as a customized design corner and performance density function estimation as described in [4].

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7974-25, Poster Session

Applications of DBV (design-based verification) for steep ramp-up manufacture

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Semiconductor industry has been experiencing rapid and continuous shrinkage of feature size along with Moore's law

As the VLSI technology scales down to sub 40nm process node

The first controllability of critical dimension (CD) becoming more challenging and difficult

Especially development and mass-production of memory devices, controllability of gate transistor CD is the one of the greatest concern for both designer and manufacturer since characteristics of device chip, speed and power, are largely depend on the gate CD.

The second is device design rule scaling down

As the design rules become more and more complicated than before. These complicated design rules have to guarantee process margin for the most layout environments.

However, some layouts have narrow process windows that were still within the design rules.

Complicated layout continues to push lithographic pattern to higher numerical aperture (NA) and smaller k1 factor, extensive use of resolution enhancement techniques becomes a general practice. Use of these techniques not only adds considerable complexity to the design rules themselves, but also can lead to undesired and unanticipated weak point pattern effects known as "hotspots."

Hotspots could be quickly fed back to layout designer, OPC, mask making, by full-chip lithography simulation before tape-out and making photo masks.

However, it is difficult to exactly estimate hotspots on final patterned features on wafers by full-chip lithography simulation. Therefore, experimental full-chip inspection methodologies for hotspots extraction are necessary in order to reduce TAT for steep ramp up Manufacture

In this paper, we introduce the concepts of an innovative reduction Turn-around-time (TAT) in manufacture production with applications of DBV

The first one is reduction of extraction hotspots time

The exact hotspots could be detected four times faster than in the case of using the conventional NGR-2150 system inspection in the full chip window

The conventional NGR-2150 system already have reasonable operation time; however, tend to detect not only real defects but also virtual defects and NGR-2150 bug defects.

NGR-2150 output raw data are also getting larger on the scale of ten of thousands, even millions. it takes much time and labor to review and analyze all raw data and pattern images.

How to efficient analyze output raw data is also directly impacting the productivity

Therefore, the noble hotspot extraction methodology employed by our own technology with application of DBV is highly advantageous for shortening development TAT.

The full-chip inspection capability NGR-2150 output data is normally so

large that it is difficult to handle the data for real hotspots. So we already extract hotspots from result of the full-chip Layout GDS, with model-based post-OPC verification and Simulation Tools.

All of extracted points can group and classify huge amount of data from simulation weak point into HPA (Hotspot Pattern Analyzer)

Extracted point list from HPA goes back to NGR for inspection or review, and the results can be used for estimated hotspots

It would be possible to save a lot of time for the analysis.

The second, it is possible to exactly determine for process judgment go or no-go about process equipment variation or stack thickness change?" by estimate gate layer CD distribution just inspecting in the some window not in the full chip window with applications of DBV.

The third, it is possible to setup hotspots prescreen procedure for wafer processing in mass-production of memory devices

Hotspots prescreen will be promising way for reduction of mask revisions cost effective manufacturing until the layout is printed on the silicon.

7974-26, Poster Session

Rerouting and guided-repair strategies to resolve lithography hotspots

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With the upcoming technology generations, it will become increasingly challenging to provide a good yield and/or yield ramp. This holds in particular for a multi-sourcing environment where the demands on the layout style may be incompatible. In contrast to defect limited yield loss, systematic yield detractors such as lithography hotspots may cause a huge yield loss per event. Such events are increasingly treated like DRC violations. Therefore, lithography compliance became a sign-off criterion for the 40 nm and subsequent technology nodes, and any lithography hotspots have to be removed before tapeout. Under the time pressure of a tapeout, manual repair even of a few hotspots bears the risk of failure.

We report a comparison of cleanup strategies, re-routing and guided-repair for the backend layers - metal and via layers - from a use-model point-of-view. Re-routing is implemented in the routing engine and controlled just by a blockage defined at the location of the lithography hotspot, i.e., an error marker created by the verification step of the lithography simulation. It can be treated without any knowledge of the physical background of the hotspot. It becomes obvious that re-routing applies changes of the original layout in a radius >10 µm, and usually modifies several metal layers at a time. Such changes definitely invalidate the timing closure, timing sign-off is required again after re-route. If many hotspots are removed by re-routing, a whole block may require re-routing.

Guided repair, in contrast, delivers local optimizations of a layout similar to layout polishing. Many hotspots can be treated independently, and there is usually no impact on the timing closure due to the small changes in wire geometry. This is the justification for an application outside the routing flow, i.e. after the layout has been streamed out. The litho engine can provide more information than just the location of the hotspot like sensitivities of the adjacent polygon edges. Accordingly, the guided repair is based on an excellent knowledge of the critical layout situation leading to the lithography hotspot. In addition, there is no need to use the routing grid for repair which is usually much coarser than the design grid. However, guided repair may fail for several reasons. Any shapes in the lowest metal layer belonging to standard cells must not be modified. The guided repair requires the creation of cell variants or even flattened layout portions at the hotspot location(s), especially if a part of a polygon from this cell has to be removed to resolve the hotspot. This approach implying cell variant generation is likely impossible within the routing engine. Changes ranging over several metal and via layers which form a real challenge for any DRC-like engine, and finally, extremely nested layout situations may be intractable at all, if no edge can be moved without creating a new hotspot.

The layout aspects of both cleanup strategies are based on concrete layout examples. Various flow variants are assessed in comparison, and an optimal flow is derived from the results.

7974-27, Poster Session

Accurately predicting copper interconnect topographies in foundry design for manufacturability flows

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We present a new CMP process prediction method for foundry's DFM (Design for Manufacturability) in this paper. As process technologies move to 65nm, 45nm, and smaller feature sizes, qualities of CMP (Chemical Mechanical Polishing) planarization become crucial to preventing copper pooling and optimizing DOF (Depth Of Focus) for photolithography. Both erosion and dishing effects vary DOF levels at different proximities across a wafer. DOF tolerance has been demanded to be significantly below 100nm for both 65nm and 45nm technologies. Discovery of either copper pooling or DOF failures during the manufacturing cycles is often too late for any recovery, or takes costly and lengthy split wafer experimentation to repair. Therefore, to resolve those manufacturing failures, a foundry must be able to accurately predict post-CMP copper interconnect topographies and use them to feed back hot spots to designers in an efficient DFM flow, before the manufacturing starts.

In this paper, we present a model-based CMP-DFM method to detect the copper pooling and DOF failures. The proposed model-based check can be applied to screen highly environment sensitive layouts which are prone to early process window limitation and hence failure. Moreover, CMP modeling technology enables multi-level simulation, which can capture hotspots caused by interactions among several metal levels; this kind of hotspots cannot be easily detected by rule-based approach.

We show the method to generate CMP process models for simulating both post-ECP (Electroplating) and post-CMP copper topographies for a 65nm process technology and also for other ones. The work cycle, as shown in Figure 1, uses rich calibration test structures. They go through dimensional silicon measurements. As shown in Figure 2 with partial data, the model calibrated with the silicon measurement data is then generated in our method. During the calibration process, fitting accuracy was achieved greater than 95%. Accuracy of the model is then further validated through additional silicon measurement on a different set of test structures, as also shown in Figure 1. This is a necessary procedure to ensure the quality of the model. The accuracy achieved by the validation method has goodness of fitting higher than 90% and satisfies our criteria of process simulation, as shown in Figure 3. The high level of accuracy achieved by our method is key to successful copper pooling prevention and DOF variability mitigation in a DFM flow.

Using the method, we have been able to build our DFM flow for hot spot detection in terms of erosion, dishing, and copper thickness variations. Copper pooling prevention and DOF variability mitigation are achieved once the hot spots are fixed through design modifications. In this paper, we show the hot spot detection renders accurate process prediction and fix at as early as block design levels. It is also able to link the copper thickness profiles to RC extraction and timing analysis flows to evaluate performance yield and timing impacts at both block and full-chip levels. The method is also useful in verification of our model based dummy metal fills introduced earlier. We will also show silicon proof of these efforts on 65nm designs.

7974-28, Poster Session

Lithography aware standard cell characterization

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As the regularity of the IC design becomes necessary in sub-45nm technology, the on-grid 1-D standard cell design has shown the trend for a better printing capability. Targeting on the property of dense

line printing techniques, an optimal algorithm on dummy insertion and wire-end extension has been introduced to greatly increase the printability [1][2]. However, as those lithography-aware modifications have inevitable impact on the circuit performance, power consumption and system variations as shown in Fig. 1, it is necessary to build up a characterization tool to characterize the standard cell under lithography-aware modification and use it to guide the trade-off between lithography and design.

In this paper, for each standard cell in a 1-D standard cell library, instead of allowing unlimited modification, we will set extension limit on each cell and apply different extension strategies for better printability. With those lithography-aware modifications on each cell, we can apply our characterization tool to obtain the "extension bound vs performance" curve giving the relationship between printability and impact on performance. Then we can use the curve to guide our trade-off to setup the modification strategy for different design margin.

As the modification is always changing due to the change of surrounding environment of a certain cell, 1-D on-grid standard cell can be therefore further characterized with the impact of surrounding patterns, which can be approximately localized based on several types of environmental pattern. The final cell characterization will be classified by the type of cells and their environmental patterns, which can be a very important role in design-manufacturing co-optimization flow.

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7974-29, Poster Session

Efficient approach to early detection of lithographic hotspots using machine learning systems and pattern matching

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Semiconductor manufacturing is heavily dependent on lithography systems. Feature size scaling brings advantages such as improved circuit performance and reduced cost per unit, but the challenge in achieving satisfactory production yield is becoming greater and greater. Since the wavelength of practical illumination sources remains 193nm, diffraction effects cause severe shape distortion to the on-silicon printed images. Presently, pattern fidelity is primarily sustained through aggresive application of resolution enhancement techniques (RET) such as optical proximity correction (OPC) and off-axis illumination (OAI). Since RET cannot completely eliminate the printability problem, physical verification tools capable of identifying potential lithographic hotspots are required. Design rule checking (DRC) has been the conventional interface between designers and manufacturers. However, as the layout objects' sensitivity to proximity shapes becomes greater and design rules cannot efficiently describe two-dimensional layout patterns, a design-rule-clean layout may still have manufacturing problems. Lithography simulations based on well-calibrated process models have become the golden physical verification for lithography-related issues, but they are extremely computationally expensive and time-consuming.

Approximate lithorgraphic hotspot detection solutions have emerged due to their high runtime efficiency. Pattern matching-based algirithms are widely adopted in the industry. They scan through design layouts using a pattern database containing previously known undesirable patterns. However, even with fuzzy matching algorithms, pattern matching-based solutions are weak in detecting bad patterns not present in the database. Machine learning-based hotspot detection algorithms are proposed to address this issue. Since machine learning techniques construct a classifier based on the training pattern samples, it can make "educated" predictions on unseen pattern samples. Therefore, it is believed that machine learning methods are capable of classifying test pattern samples unknown to the training process.

We proposed a characterization methodology for machine learning-based techniques that provides measurable quantification of (1) capability to predict test samples unseen in the trianing set, (2) inevitable false alarms caused by feature encoding, and (3) other misclassifications due to the learning system itself. We provide justification for the belief in the predictive capability of machine learning systems. Using the proposed experimental methodology, one can effectively compare and improve detection capabilities of machine learning-based hotspot detection tools. As Figure 1 shows, the machine learning method captures more hotspots than pattern matching method does. Meanwhile, they both results in some false alarms, with machine learning methods reporting more false alarms.

Finally, based on the experimental observations, we apply both pattern matching and machine learning algorithms to create a hybrid lithograhic hotspot detection tool. Experimental results show that the hybrid solution combines the strengths of both algorithms and delivers improved detection accuracy without sacrificing runtime efficiency.

7974-30, Poster Session

Fast process-hotspot detection using compressed patterns

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Lithographic hotspot detection using pattern matching techniques with hotspot libraries defined by existing simulation-based verification has been recently adopted due to its high hit rates over runtime ratio.

However, most of existing exact pattern matching techniques lack the ability to predict the behavior of structures outside the calibration set. One common approach is to generate a priori as many exact variants of the base pattern to be detected. This requires the addition of an increasing number of patterns to the litho hotspot library in order to reach an acceptable coverage. However as the number of hotspots increases traditional the runtime increases making a pure pattern matching method less appealing.

In this paper we present a method that compresses litho hotspot patterns in compliance with an exact pattern matching technique. The resulting compressed patterns are then used instead of the complete library of exact matches.

The method parses the hotspot library, determines similar litho hotspots patterns using a geometric comparison that weeds out unnecessary information in the patterns and then determines the common geometrical structures between patterns and inserts adaptive edge tolerance constraints for each individual pattern in an automatic fashion.

While the performance of a non-exact pattern matching process is in principle more expensive than an exact match process, the analysis presented in this work shows the compression rates needed to achieve a better performance than the exact matching process while maintain the original quality of results. In addition, we explore the ability of this method to correctly interpolate between patterns and provide correct hotspot predictions of patterns that do not exist in the calibration set, but rather can be found in subsequently verified layout that otherwise would have been missed during verification.

7974-31, Poster Session

32-nm CMP model development and application to design optimization

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In this paper, we present a model-based CMP-DFM methodology which is used to avoid CMP related manufacturing failures. This methodology is used to detect and fix CMP hotspots during design and also to analyze the CMP impact on interconnect parasitics.

We demonstrate how to characterize physical model for ECP and CMP process steps. The model is then used to predict surface topographies for 32nm designs. An accurately calibrated CMP model is very capable of predicting physical hotspots caused by dishing, erosion and depth of focus. Once hotspots are detected, the model is then used to evaluate different corrective approaches for copper pooling and DOF variability mitigation in a DFM flow. At Samsung, 32nm CMP model has been calibrated using a rich set of calibration test structures. The model has been further validated with additional silicon data from different designs. The validation accuracy achieved was greater than 90% of goodness of fit. The model has been further utilized in CMP-aware RC extraction flow for assessment of performance impact of thickness variation.

7974-32, Poster Session

Hotspot detection using image pattern recognition based on higher-order local auto-correlation

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Below 40nm design node, systematic variation due to lithography must be taken into consideration during early stage of design.

So far, litho-aware design using lithography simulation model is widely applied to assure that design prints on silicon without any fail.

However, lithography simulation approach is very time consuming, and under time-to-market pressure, repetitive re-design by this approach may cause loss of market window opportunity.

This paper proposes the fast hotspots detection support method by flexible and intelligent vision system image pattern recognition based on Higher-order Local Auto-Correlation (HLAC).

Our method learns the geometrical properties of the given design data without any defects as normal patterns, and automatically detects the design patterns with hotspots from the test data as abnormal patterns. The HLAC method can extract features from the graphic image of design pattern, and computational cost of the extraction is constant regardless of the number of design pattern polygons.

This approach can reduce Turn around Time (TAT) dramatically only on 1CPU, compare with the conventional simulation based approach, and by distributed processing, this has proven to deliver linear scalability with each additional CPUs.

7974-33, Poster Session

The effective etch process proximity correction methodology for improving on chip CD variation in 20-nm node DRAM gate

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This paper presents an effective methodology for etch process proximity correction (PPC) of 20 nm node dynamic random access memory (DRAM) gate transistor. As device shrinks, on chip critical dimension variation (OCV) control becomes more important to meet the performance goal for high speed in DRAM. The main factors which influence OCV are mask, photo, etch process proximity effect (PPE) in DRAM gate. Model based etch PPC is required to properly correct etch PPE as device density increases. To improve OCV in DRAM gate, we applied new type of etch loading kernel. It is called Vkernel which accounts for directional weight from the point of interest. And we optimized the etch PPC convergence by optimizing the etch PPC iteration. Because of density difference between spider mask and real gate mask, the skew difference occurs between them. We tested the effect of long range density using the same real gate pattern clip by varying mask open image size from 0.5 ~ 10 mm. The after development inspection CD difference was on average in the order of 2 nm for varying the mask open image size. But the ACI CD difference with varying open image size was very noticeable (about 15 nm). The etch skew was affected by long range density by mm size. Due to the asymmetrical pattern in real gate mask, spider mask which has symmetrical sample patterns designed for etch skew is necessarily used to make PPC model. The etch skew of real pattern clip in spider mask was not also same as real gate spider mask. To reduce this skew difference between spider and real mask by the difference of long range density around real gate clip, we applied open field mask correction term and long range density effects correlation equation to PPC modeling. There was noticeable improvement in the accuracy of PPC model. By applying these improvement items, OCV of 20 nm node DRAM gate was improved by 31%.

7974-35, Poster Session

Defect-aware reticle floorplanning for EUV masks

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Producing defect free mask blanks has become a major “show-stopper” for EUV lithography. EUV mask blanks suffer from defects that are buried under multiple layers of Si/Mo making them difficult to repair. A 3.5 nm high buried defect can cause a 20nm CD change on the wafer [2]. One possible solution to minimize the impact of these buried defects is to floorplan dies on the mask such that the impact of these defects is minimized. We develop such a novel floorplanning method using design criticality information of various regions on the layout.

In this work, we restrict ourselves to single-project reticles. Design criticality map of the design is generated using the method proposed in [3]. Only gridded placement of die is considered so that no die is lost due to side-to-side wafer dicing. Buried defects are assumed to have a gaussian shape with CD impact proportional to height of defect [1]. With these assumptions, we develop a simulated annealing based gridded floorplanner. In order to minimize the impact of defect on critical areas of design we propose a cost function which is the exponent of the difference between the CD impact of a defect in the region and the CD tolerance of the region.

An initial solution of the floorplan is constructed by placing multiple copies of the design in a compact grid till no more dies can be fitted in. This solution is then perturbed by changing the orientation of the die (rotation or flipping) or by accepting valid grid line moves in order to minimize the cost function.

In our experiments, we consider a reticle of dimensions 26cmX33cm, and a poly layer of MIPS processor with different regions marked as critical or non-critical as the die to be floorplanned. Since the design is very small, multiple copies of MIPS are placed together in a grid to constitute a single die. Gaussian buried defects have half width of 70nm, maximum CD impact of 5nm and are placed randomly on the reticle. The results show that die yield (Average percentage of dies per mask for which CD impact of defect is less than CD tolerance) can be improved by up to 44% and 30% for a 10-defect and 20-defect mask blank, respectively. The corresponding mask yield (Average percentage of masks with all die functioning) can be improved by 78% and 24%, respectively.

Our ongoing work is to account for criticality of multiple layers instead of just the poly layer during floorplanning. Better defect models that account for location of absorber patterns are also being studied. We are also exploring floorplanning methods that can generate non-gridded solutions after accounting for dicing yield.

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7974-36, Poster Session

Standard cell electrical and physical variability analysis based on automatic physical measurement for design-for-manufacturing purposes

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A fully automated system for process variability analysis of high density standard cell was developed. The system consists of layout analysis with device mapping: device type, location, configuration and more. The mapping step was made by a simple DRC run-set. This database is then used as an input for taking SEM images and specific layout parameter extraction, for SPICE simulation.

We used our method to analyze a large arrays of standard cell blocks, manufactured using Tower TS013SL (0.13um Standard Logic for General Purposes) and TS013LV (Low Voltage) Platforms. Variability of different physical parameters (Lg, LWR and others) as well as of electrical parameters (drive current (Idsat), Off current (Ioff)) were statistically analyzed, in order to understand the variability root-cause. Comparison between transistors having the same W/L but with different layout configuration and different layout environment (around the transistor) was made in terms of performances as well as process variability. We successfully identified “robust” and “less-robust” transistors configurations, to be used as guidelines for Design-for-Manufacturing (DfM).

7974-37, Poster Session

Aerial image retargeting (AIR): achieving litho-friendly designs

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Rule-Based Catastrophic OPC was introduced many years ago to do simple rule-based retargeting of the design to prevent on-wafer catastrophic failures. This is usually done by biasing certain width-space combinations to prevent on-wafer failures that are due to process window limitation of certain design pitches. However, as the design density increases, we have reached a state where the designs are dense enough so that the nearby (but geometrically shielded) designs can affect the process window immunity of the design. This is because the exposure wavelength is still the same while the designs are getting smaller and smaller. As well as the fact that the general biasing rules for 1D features are not necessarily the best rules for complex 2D designs. Moreover, the tighter specifications that are enforced on the fabrication in terms of Across Chip Line variation (ACLV) whether it is for gates or wires in order to maintain the electrical characteristics to their best across the full chip. All this makes it necessary to explore new techniques to do the retargeting of the designs seeking more PW-friendly (Litho-Friendly) OPC targets. In this work, we are proposing to use the Aerial Image (AI) signature of the litho target to pre-process the design and do some retargeting it to a more Litho-Friendly target. The paper is organized as follows, in section (II), we are introducing the concept and doing our analysis to show that the AI signature is sufficient in identifying the hotspots and how it can be used to modify the design in a pre-OPC step. In section (III), we are presenting the results and the proof of concept after applying Aerial-Image-Retargeting (AIR) on a 28nm metal design.

An efficient model-Based OPC target correction is needed to achieve better litho-Friendly targets is needed. This technique needs to be accurate, fast and computational efficient so that it can be efficiently used in OPC production environment as well as a part of the designer’s environment to back annotate this retargeting and its effects on the parameter and parasitic extraction. Also, if this approach can catch most of the retargeting needed to have a PW-friendly OPC target, then this would enable two important applications. The first is on the fab’s side which is to reduce the number of iterations of their OPC recipes (better Turn-Around-Time (TAT)) as the target is more Litho Friendly and simpler OPC recipes are needed. The second is for the designers as it is always very hard to back-annotate the retargeting information (especially those due to PWOPC) to the designer in the parameter and parasitic extraction phase.

Aerial Image Retargeting (AIR) is based on the assumption (that is verified in this paper) that we can identify weak PW areas and classify them as pinching-weak (width sensitive or lines tending to pinch) or bridging-weak (space-sensitive or lines tending to bridge) using the design’s aerial image simulation signature. After this, each fragment of the target is moved according to its Aerial Image (AI) signature to widen the spaces or widths of the design and result in a more litho-friendly OPC targets. (This shouldn’t be confused with the OPC where the target fragments move to minimize their Edge Placement Error (EPE) between the printing image and the design intent). The decision of how much to move the fragments and its sign (inward or outward) is based on a lookup table that is developed by the fab’s OPC engineers after training the recipe on a large dataset of the PW sensitive patterns and interpolating for missing AI signatures.

Figure 1 shows the AI cutline through three different metal designs and how AI parameters can be used in uniquely identifying different designs not only based on their geometrical description but on their optical performance which implicitly contains all the proximity around them. Figure 1(a) shows the design and example of where the AI parameters are computed, Figure 1(b), is showing the AI distribution and Figure 1(c) is showing the weakness of this spot in process window. Training the AIR recipe on such PW-sensitive design space, we can identify and correct PW-sensitive designs.

7974-38, Poster Session

Timing variability mitigation for layout-dependent-effects in 28-nm custom and standard cell-based designs

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This paper identifies most recent sources of transistor layout dependent effects (LDE) such as stress, lithography, and well proximity effects (WPE), and outlines modeling and mitigation methods for 28 nm. These methods apply to custom layout, standard cell designs, variability-aware placement and context-aware post-route analysis. We show how IC design teams can use a model-based approach to mitigate variability induced by LDE and reduce the need for guardbands that negate the performance advantages that stress brings to advanced process technologies.

Intentional stress is used to enhance performance in CMOS ICs since 65 nm technology, but stress also causes layout dependent variations [1]. This means that designers can’t just look at transistors in isolation, the location and dimensions of neighboring layout features change the surrounding stress, and therefore the performance of custom analog layout, standard cells and System-On-Chip (SOC) designs.

In analog custom design, the designer’s intent and requirements

are conveyed in the schematic and hence the layout should behave similar to the drawn schematic. But the impact of layout proximity on transistor performance is considerable. Consequently, it is easy to end up with post-layout simulation mismatches between the layout and the schematic, resulting in long iteration loops. Instead, the analog designer can perform an LDE analysis to find that the layout is diverging from the schematic during the layout creation before extraction of the stress parameters and full transistor-level simulation.

Developers of standard cell libraries need to also evaluate the LDE effects by using design rule decks to extract stress and WPE parameters from layout and SPICE models to run transistor-level simulations. However, if one takes a standard cell and places it in a different layout context, the simulation results may be quite different [2]. Using the LDE analysis, designers can perform a library variability analysis which consists of running many circuit simulations in many different contexts to find out the possible extent of delay and leakage variability due to LDE, and to architect the layout to minimize unwanted variability. LDE analysis can also extract critical context variability information that can be used to mitigate variability during placement, timing analysis, and pessimism using cell-by-cell derating factors.

In addition to library variability analysis, the LDE model can be used prior to tapeout to run a post-route lithography [3, 4] and stress variability analysis. Chip designers can run static timing analysis with cell-based derating factors generated during the library variability analysis. They can also analyze critical paths that might be especially sensitive to proximity effects, and optimize those paths to reduce sensitivity to variations.

While more focus has been on post-placement gate-level timing analysis [5] and optimization [6], there is room for conducting earlier analysis in the flow without compromising significant gate-level timing accuracy. While [7] has contributed to this domain for stress in 45 nm technology, a faster methodology which can target 28 nm, and also include lithographic effects is needed. In this paper, we target this particular gap.

7974-39, Poster Session

Statistical approach to specify DPT process in terms of patterning and electrical performance of sub-30-nm DRAM device

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Double-patterning technology (DPT) has been a primary lithography candidate of the sub-30nm technology node. The major concern of DPT is the critical dimension (CD) skew and overlay error between 1st and 2nd patterning, which cause the degradation of the electrical performance in terms of timing delay. In this paper, we newly develop a systematic method to determine the DPT scheme and the proper process specification using a statistical approach in perspective of the pattering and electrical performance. Applying the method to the bit-line layer of the sub-30nm DRAM device, we determine the DPT scheme (i.e. either litho-etch-litho-etch (LELE) or self-aligned double pattering (SADP) to avoid the patterning hotspots. In addition, analyzing the statistical simulation result, we provide the process specification and exposing sequence of two masks to avoid the electrical degradation.

7974-04, Session 2

Using templates and connectors for layout pattern minimization in 20 nm and below technology nodes

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Layout pattern minimization has become a necessity at the 20nm technology node. Not only is it the only way to guarantee convergence for source mask optimization (SMO), having a well defined design space by limiting the total number of layout patterns, is the only way to ensure complete verification of design space during technology bring-up. In this paper we would reveal the details of PDFs template and connector based layout design methodology that enables designers to achieve compact layout density by limiting layout patterns. The use of this methodology enables a 25X pattern count reduction compared to the gridded logic layouts and is the only solution available that ensure pattern count saturation within a 100um x 100um random block of logic. Results on SMO compatibility has been highlighted by the collaborative work between ASML and PDF Solutions. In this paper we will discuss the development of the optimal fabric for SMO and DPT compatibility, the definition of the base template and corresponding connector templates to provide the fabric constraints to designers and results highlighting the lithographic benefits of this approach. We propose a design solution that can provide a low-risk 20nm technology node solution.

7974-05, Session 2

Lithographic variation aware design centering for SRAM yield enhancement

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SRAM cells use the smallest manufacturable device sizes in a given technology and hence see a highly pronounced random dopant effect. Moreover, SRAM cells are traditionally designed to satisfy conflicting read and write requirements. It makes SRAMs extremely vulnerable to failures in the presence of lithographic variations. An SRAM cell can fail in multiple ways (data retention fails, access fails, read disturb fail, write fails, Vmin fails, etc.) and each failure mode exhibits different sensitivities to lithographic variations in different devices. Therefore, the joint electrical yield exhibits a highly non-linear or piecewise linear behavior with yield degrading asymmetrically with positive and negative CD variation. Furthermore, the nature and magnitude of asymmetry in the joint yield response curve is different for variation in access, pull-up, and pull-down devices due to differences in their electrical sensitivities.

We propose a design centering approach for maximizing SRAM electrical yield under lithographic variation. The centering is obtained by applying small biases to the gate lengths in the circuit. We refer to this process of changing the original target layout as electrically driven layout retargeting. The idea behind layout retargeting is that the default distribution of process variability band (PV-band) around nominal design edge is sub-optimal for through process window electrical yield maximization. The overall worst-case electrical yield can be improved by intentional shifting of the lithographic PV-band in the preferred direction. The PV-band can be shifted through retargeting the layout such that nominal target CD is biased up or down to obtain a desired shift. The optimal direction and magnitude of the PV-band shift is different each device and this optimal shift can be obtained by a linear programming formulation that optimizes the worst-case yield across process window.

To setup the yield optimization framework, we consider that different fail modes in a circuit can be modeled by N electrical yield constraints. We can pre-characterize the sensitivity of each yield term to CD variation in each device in the circuit. Here we assume that each individual yield term varies linearly (and thus strictly monotonically) with respect to CD variation. Under this assumption, the joint yield varies piecewise linearly with CD variation and the worst case yield always occurs at either the inner or the outer CD contour. Therefore, we can calculate the bounds on each yield term by evaluating the corresponding electrical metric at inner and outer CD contours. These yield bounds can be improved by retargeting CD of various devices in the circuit. We setup a linear program (LP) to obtain the optimal retargeting values for each device. The LP constraints are setup such that the bounds on the individual yield terms (or failure modes) do not exceed the overall worst-case yield criterion, which is maximized through optimal selection of the retargeting values.

The proposed retargeting flow was tested on an SRAM design. The results show that the scheme improves the worst-case through process SRAM yield from 0.89 (read access yield at outer contour) to 0.95 (read disturb yield at inner contour), which corresponds to about 6.7% improvement in failure sigma.

7974-06, Session 2

Multi-selection method for physical design verification applications

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Model based verification and rule based verification are routinely used in the design of products to be manufactured with advanced technology nodes. While each methodology has found its own niche: model based simulation in standard cell development, and rule-based verification anywhere else; there is a concern that even more complex design rules are reaching a productivity and predictability limit in which more complex rules are hard to develop and even more difficult to guarantee for completeness. However, those limitations have been overlooked since model based verification is limited to the models that it contains (mostly litho, etch and CMP) and the large computing requirements that those model imposed to design team in order to meet traditional productivity goals.

In order to enhance traditional DRC, there have been methods proposed to extend DRC verification with pattern matching techniques. While this approach incrementally improves the total verification coverage (meaning that fewer difficult layout configurations will make it to the production line), there are no formal techniques that guarantee or can predict the level of verification coverage that is available. On the other hand these pattern matching techniques have been increasingly adopted because their runtime performance are at par of traditional design rule checks, and therefore they do not impose additional productivity cost to the design teams.

In this paper we present a modular approach which combines model based verification, pattern matching and machine learning methods in order to achieve a high accuracy over computing time ratio.

Pattern matching techniques in many instances are limited by the fact that they can only describe the known environment that causes a given failure and they fail to predict any new failure. This limitation has been tried to be corrected by the introduction of a fuzziness criterion which allows other similar structures to be considered also failing. The problem with that approach is that fuzziness is pattern matching method specific. If the pattern matching method utilizes a layout Boolean operation, the fuzziness can be described as the area of the XOR operation between the search pattern and the current pattern. A spectral-based pattern matcher can modify the magnitude of the signal or have a “smearing” function that allows two patterns to be considered the same. While indeed such approaches will capture more possible verification failures, they do so in a manner that homogeneously increases the number of false defects which causes a design productivity loss.

In our proposal, we utilize pattern recognition technique using a supervised machine learning system (as opposed to pattern matching) to classify the patterns either as failures (hotspots) or non-failures. In this case failure and non-failure locations are used to teach the support vector machine (SVM) decision system. The SVM system will draw based on the learning patterns a boundary (hyper-plane) between failing and non-failing patterns in the pattern space. Inherent to any pattern recognition system is the loss function; that represents the inability to correctly classify some of the patterns. These wrongly classified patterns can either be categorized in the pattern space as patterns that are “outliers”, (i.e. they are either far inside the known failing configurations or far inside the known non-failing configurations) or they are at the boundary between the failing and non-failing configurations. (figure 1) For the former we use pattern matching and the latter we use model based simulation to complement the machine learning system.

We use pattern matching to detect all the outlier misses and false detections in each of the regions (based on the calibration set), which will be added or removed from the set of hotspots later on. Doing so allows us to do two things: Reduce the number of patterns that need to be pattern matched since only the outliers of the machine learning system need to be considered and more importantly it allows us to add trained predictability to new configurations that were not in the training set but that can be interpolated from the system.

In addition, once the machine learning model has defined the failure, interface and non-failure regions, and the pattern matching has added or removed structures, the system has the ability to feed the boundary candidates to traditional model-based simulation (in the case models exist), to determine unequivocally if they are failure or non-failure locations, thus reducing the total number of structures that need to be processed by the expensive model based verification step.

Finally such process of developing the machine learning and pattern matching databases can be fully automated and included in a closed loop system in which as more failing and non-failing information become available, the system converges towards complete failure identification.

The main contributions of this paper are:

Formalize pattern matching fuzziness by defining it as the boundary region of a pattern recognition classification method.

Combining machine learning, pattern matching and model based verification to obtain an optimal accuracy/runtime ratio for layout verification applications.

7974-07, Session 2

Applying litho-aware timing analysis to hold time fixing reduces design cycle time and power dissipation

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ABSTRACT

In this paper, we present an innovative approach to reduce over-design, reduce power and accelerate timing closure by using litho-aware static timing analysis. Initial application of this technique to hold time fixing, reduced power impact of the hold buffer insertion by almost 30% and the TAT of the hold buffer insertion by 45.6%.

During timing closure, one of the most time-consuming steps is hold-time fixing. The “traditional” approach uses STA sign-off tools to identify the signal path that are too fast and can create a hold violation with the clock signal and then insert buffers on these signal paths to slow them down. Buffer insertion to fix hold-time can take up to 7 days and has a significant impact on power dissipation. So it is important to focus on the real errors to reduce the design cycle time and minimize power impact. Since traditional static timing analysis are using margins to compensate for systematic effects instead of accurate modeling, designers typically waste time fixing some false violations and add too many buffers to fix hold-time violations.

In order to have a more silicon accurate timing analysis, we have developed a litho-aware timing analysis based on Cadence Litho Electrical Analyzer (LEA) and Cadence Encounter Timing System (ETS). As described in [1], we used simulated silicon-calibrated contours to predict the litho effects on transistor gates, and extracted delay variations due to litho using LEA, and then performed litho-aware critical paths analysis in Static Timing Analysis tool. This method allows accounting for variations in Lgate that affect circuit timing properties, which can lead to timing errors and performance loss. We used that approach to filter the false hold-time violations and focus designers’ actions on most important violations.

In this paper, we describe the chip timing methodology, its validation and its application to hold-time fixing. The litho-aware timing analysis developed by Renesas Electronics is shown in Figure 1. First we establish the accuracy of the litho-aware timing flow against silicon data, validating that the timing variations due to litho are consistent with silicon variations as shown in Figure 2. We then show the results of this flow on a production microprocessor design, and how after litho aware STA, the average of slack shift by “+54.2ps”, and how 276 paths of the 1000 hold paths are reported as false hold time violation as shown in Figure 3. Our initial results show that instead of using 1383 buffers to fix all hold-time violations reported by the traditional approach, we were able to focus our fixing effort where it matters most and only used 982 buffers, reducing by 29% of number of inserted buffers. By applying this technique, we also reduced the time spent on this task from almost 7 days down to less than

4 days, where the actual litho-aware timing analysis flow runs overnight. This represents a 45.6% runtime reduction.

This study not only demonstrated the feasibility of the litho-aware timing analysis flow but also show its value to reduce hold-time fixing effort and reduce power dissipation caused by buffer insertion.

7974-08, Session 2

Lithography aware design optimization

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For increasingly small and dense designs requiring adequate DOF, MEEF, and EL numerous technologies have been employed to increase yield. Some techniques such as process optimization (i.e. SMO) are effective, and are not easily modifiable once an initial choice is made. Design optimization can be done separately from knowledge of the fab's OPC correction, but for sub 32nm nodes the complexity and interaction of the design target shapes is becoming too complicated for predefined design rules to produce an acceptable result.

In this paper we introduce a method called Lithographically Enhanced Edge Design (LEED) suited for IDMs. This joint target and mask optimization method takes into account the full OPC correction and process, and modifies the user's design in a controlled way so as to produce a new design with improved lithographic performance which can be used in place of the initial design. Control is given to the user so that inter-layer dependencies are not broken. Also, integrated target, mask, and source optimization is available in cases where target and mask optimization in not sufficient to produce adequate results. The use of ILT allows efficient target, mask, and source correction without extensive user OPC scripting and target modification sweeping. We show LEED results which enable production at 20x node.

7974-09, Session 2

Is manufacturability with double patterning a burden on designer? analyses of device and circuit aspects

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Stringent printability requirements of sub-22 nm features have made double-patterning lithography (DPL) a necessity for certain layers with tight-pitch features. There are three commonly known types of DPL [1]:

1) Double Exposure (DE): Two lithography steps are followed by a single etch. In another flavor of this process, a 'freezing' step can be used, i.e. the litho-freeze litho-etch (LFLE) process [2] [3].

2) Double Patterning (DP): Two lithography and etch steps are used.

3) Spacer Double Patterning (SDP): One lithography and one etch step are followed by spacer formation, oxide deposition, chemical-mechanical polishing, and a second etch.

As there are more than one mask per layer for which double patterning is applied, overlay becomes a problem.

Overlay may cause reliability problems such as copper intrusion into dielectric due to non-overlapping trench and contacts and thereby reduce yield. When such issues are not present, there still are variability issues as gates may land close to device contacts on one side and farther away on the other side due to overlay.

In this paper, we provide device and circuit variational analysis techniques for a double patterning process. In our FEOL device-level analysis, we assume that gates, contacts, and lowest interconnect layer are to be manufactured in a DPL technology. We simulate combinations of translational overlay on each layer.

For circuit-level analysis, we use full RC extraction on a 101 stage ring oscillator. We assign gate layer features to two different masks. We then shift each mask in opposite direction with respect to the other.

We repeat this experiment towards either longitudinal direction for translational overlay. The translational component, longitudinal direction, and 3sigma values ensure that the corner cases are covered. We measure timing in the transient domain and compare the frequencies of oscillators that are affected by overlay with respect to the nominal case.

The methods we provide are very useful to designers for designing circuits with the impact of overlay on variation properly accounted for. Our results also provide technology developers an idea of overlay budgets based on electrical performance.

[1] International Technology Roadmap for Semiconductors

[2] K. Chen, W. Huang, W. Li and P. Varanasi, "Resist Freezing Process for Double-Exposure Lithography", Proc. of SPIE

Advances in Resist Materials and Processing Technology XXV, Vol. 6923, 2008, pp. 69230G-1-69230G-10.

[3] M. Hori et al., "Sub-40-nm Half-Pitch Double Patterning with Resist Freezing Process", Proc. of SPIE Advances in Resist Materials and Processing Technology XXV, Vol. 6923, 2008, pp. 69230H-1-69230H-8.

7974-10, Session 3

Evaluation of a new fast resist model: the Gaussian LPM

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Many computational lithography problems require fast, accurate resist models (often called compact models) to enable lithography simulation of an entire chip in a reasonable time. While rigorous resist simulators solve physically-based models in three dimensions, compact models simplify their descriptions of the phenomena and reduce the problem to two dimensions. The result is a dramatic increase in speed, but also some loss in accuracy. Further, the resulting compact models are often more empirically than physically based, so that model parameters are hard to relate to readily observed properties of the lithography process.

The most commonly used compact model of resist behavior is (with many variants) the variable threshold resist model (VTR). For example, one might define a variable threshold that is a simple polynomial function of the maximum local intensity and maximum local slope near to and perpendicular to the feature edge, or a polynomial function of the maximum local intensity, minimum local intensity, image slope at the mask edge, and the mask CD. Usually polynomials out to second order are sufficient, and some cross terms may be included. The coefficients of these polynomials are determined by comparison with experimental through-pitch CD data.

There are two main disadvantages of these empirical models. First, the accuracy of the predictions made by the VTR models are only expected to be sufficient when interpolating within the range of features used to calibrate the model. Thus, considerable effort is spent in determining the appropriate range of features used to calibrate the models and whether they are representative of any given mask design. Second, any change in the resist process (or even the mask making process) will likely change the model coefficients in some unknown way. Thus, a change in process must be accompanied by an expensive recalibration exercise. Thus, there is a desire to use simple, high-speed compact resist models that have a more straightforward physical interpretation so that these two disadvantages can be mitigated.

One promising approach is the Lumped Parameter Model (LPM). This model performs a very simplified calculation of resist development in three dimensions that produces an accuracy intermediate between rigorous resist models and compact two-dimensional models such as a VTR. The LPM makes two basic assumptions: the resist contrast, , is independent of dose, and the path of dissolution can be segmented into vertical followed by horizontal development steps. The result is a prediction of edge position as a function of dose for a given image in resist

The numerical integration required of the LPM is too time consuming for many modeling applications. This integration can be carried out

analytically by noting that in the clear region of an image, near the edge of a line, the aerial image (and the image-in-resist) can be well approximated as a Gaussian function. Using this approximation, a simple model predicting CD as a function of dose is derived, capable of computing resist behavior at least as fast as a VTR, but with the advantage of using fewer (and possibly the minimum amount of) physically relevant parameters. It is believed that this model will prove more robust and predictively accurate than a VTR with the same number of parameters. A detailed examination of these claims will be given in this paper.

7974-11, Session 3

Methodology for balancing design and process trade-offs for deep-sub-wavelength technologies

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For process development of deep-subwavelength technologies, it's become accepted practice to use model-based simulation to predict catastrophic and parametric failures. Increasingly, these techniques are been used on the "design side" to ensure layout manufacturability, as an alternative to, or complement to, restrictive design rules. The benefit of this is that manufacturability problems can be addressed in a design-aware way, making useful trade-offs, e.g., between overall chip density and process cost and yield. On the other hand, using model-based simulation in design has several disadvantages: computation cost, incompatibility with automated layout generation tools (e.g., routers), and inaccuracy due to mismatch between process models in early development vs. product manufacturing. A bigger problem is that such analyses will indiscriminately flag hot spots caused by early process limiters and the lack of fully optimized RET capabilities as seen in Figure 1.

This paper describes a methodology that has been developed to balance these benefits and disadvantages, consisting of several elements. The first is selective layout analysis using fast rule-based and pattern-matching techniques to identify potentially problematic areas of designs, and subjecting those to full model-based simulation, as a way of reducing overall computation cost while maintaining accuracy. The second element of the methodology is the use of wafer data to anchor failure points and develop a set of threshold values used for checking simulation results. The third element of the methodology are the design analysis flows to best answer the needs of different design units, from IP library development to routing and post routing optimization flows. The third element differentiates signals actionable in the design from process related signals as shown in Figure 2.

The paper shows how IP Libraries and the full ASIC design flow benefit from eliminating hot spots and improving design robustness early in the design cycle. It demonstrates a path to yield optimization and first time right in the implementation of new technologies.

7974-12, Session 3

Comparing double-patterning methods for logic design routing

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Double Patterning (DP) is the only solution to enable the scaling for advanced technology nodes before EUV or any other advanced patterning techniques become available. In general, there are two major double patterning techniques: Litho-Etch-Litho-Etch (LELE) and sidewall spacer technology, a Self-Aligned Double Patterning technique (SADP).

While numerous papers have previously compared these techniques on wafer process capabilities and processing costs, no rigorous paper has been presented studying the design rule capabilities and dies cost. Ultimately, the preferred double patterning method should encompass the best solution space based on four factors: manufacturability, design ability, extendibility and cost. In the past, we compared SADP with LELE in terms of overlay, critical design rules, extendibility to smaller pitch and CD control etc.1 In this paper, we will present the impact of each double patterning technique on logic design, and compare the resulting die-size capabilities of SADP and LELE.

SADP and LELE double patterning have different critical design rules, such as line end-to-end, end-to-side, and the enclosure of via in metal etc. These differences arise from their different decomposition natures and their different sensitivities to process variations like overlay. Additionally, the MRC and DRC rules impact SADP and LELE very differently. It is therefore important to supplement the previous wafer level comparisons with these design based comparisons to complete the overall technology assessments.

In this paper we address the following key questions:

1. How would the design be impacted, more/less restrictive, with different DP techniques when all the decomposition strategies are understood for SADP and LELE?

2. Which set of design rules will ultimately enable the smallest die?

3. How much does the design need to scale in order to meet the cost expectation when the process is taken into consideration

Thus, this paper ultimately presents the comparison results of a SADP compliant design with a LELE compliant design, when routed thru metal 5.

7974-14, Session 4

Integrated model-based retargeting and optical proximity correction

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Conventional resolution enhancement techniques (RET) are becoming increasingly inadequate at addressing the challenges of subwavelength lithography. In particular, features show high sensitivity to process variation in low-k1 lithography. Process variation aware RETs such as process-window OPC are becoming increasingly important to guarantee high lithographic yield, but such techniques suffer from high runtime impact. An alternative to PWOPC is to perform retargeting, which is a rule-assisted modification of target layout shapes to improve their process window. However, rule-based retargeting is not a scalable technique since rules cannot cover the entire search space of two-dimensional shape configurations, especially with technology scaling. In this paper, we propose to integrate the processes of retargeting and optical proximity correction (OPC). We utilize the normalized image log slope (NILS) metric, which is available at no extra computational cost during OPC. We use NILS to guide dynamic target modification between iterations of OPC. We utilize the NILS tagging capabilities of Calibre TCL scripting to identify fragments with low NILS. We then perform NILS binning to assign different magnitude of retargeting to different NILS bins. NILS is determined both for width, to identify regions of pinching, and space, to locate regions of potential bridging. We develop an integrated flow for 1x metal lines (M1) which exhibits lesser lithographic hotspots compared to a flow with just OPC and no retargeting. We also observe cases where hotspots that existed in the rule-based retargeting flow are fixed using our methodology. We finally also demonstrate that such a retargeting methodology does not significantly alter design properties by electrically simulating a latch layout before and after retargeting. We observe less than 1% impact on latch Clk-Q and D-Q delays post-retargeting, which makes this methodology an attractive one for use in improving shape process windows without perturbing designed values.

7974-15, Session 4

Validation of process cost-effective layout refinement utilizing design intent

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1. INTRODUCTION

Continuous shrinkage of design rule (DR) in ultra-large-scale integrated circuit (ULSI) devices brings about greater difficulty in the manufacturing process. The keys to meeting small process margin are adequate extraction of critical dimension (CD) tolerance for each object and budgeting the tolerance for each process step.

Furthermore, to extract adequate tolerance, design intent in terms of electrical behavior should be carefully considered. Electrical behavior is carefully verified in both cell and chip design stages with respect to timing, IR drop, signal integrity, crosstalk, etc., using various electronic design automation (EDA) tools. However, once the design data is converted to layout data and signed off, most of the design intent is abandoned and unrecognized in the process stage. Thus, instead of essential tolerance according to layout-related design intent, uniform and redundant tolerance is used, and so excess tolerance is assigned for some layouts.

To solve the problem described above, a tolerance-based manufacturing system utilizing flexible layout-dependent speculation derived from design intent has been discussed 1-4). In this paper, design intent database utilization and cost merit is examined applying to 40nm node several testing chips.

2. UTILIZATION OF TOLERANCE-BASED MANUFACTURING SYSTEM

A test flow of a tolerance-based manufacturing system utilizing design intent has been examined. In the design stages, various electrical verifications are performed such as clock tree synthesis, timing, signal integrity, IR drop, electromigration, crosstalk, and lithography compliance checking (LCC). For each item, critical path and net is extracted and process sensitivity in terms of electrical behavior is examined. Then, process sensitivity information is assigned to each object, including net, instance, path and other figures, and described in the form of design intent database. At the time of layout data sign-off, designed data is converted to layout data, and the layout data is sent to manufacture stage with the design intent database including information of process sensitivity corresponding to each object is assigned to specific net, instance, path and other figures in the layout. These tolerances derived from several design intent are totally assigned for each figures and budgeted among process steps of mask data processing (MDP), optical proximity correction (OPC), lithography simulation checking, mask making and wafer process, and test/failure analysis step, considering proficiency of each process. Design intent of various category, direction, levels are mapped onto layout, and utilized for appropriate tolerance level setting, pattern retargeting, to enhancing margin, and also to reduce manufacturing cost.

3. RESULT AND DISCUSSION

Using test flow, tolerance mapping and estimation of process cost effectiveness is examined. Using several 40nm-node logic test chip, several sign-off verification items are verified, and design intent database for each items are generated. In the test flow, utilizing essential tolerance flexibly assigned to each object, process cost reduction with maintained yield is expected. In our previous work4), we have shown that, with proper tolerance management, OPC turnaround time was reduced according to the distribution critical and non-critical path number. In this paper, a practical method for accurate tolerance extraction and tolerance assignment to design objects is examined and the effect on the yield and TAT is verified.

7974-16, Session 4

New double-patterning technology for direct contact of sub-30-nm device considering patterning margin and electrical performance

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In this paper, we newly develop the DPT methodology to decompose the direct contact of the pair transistors to the same mask using the optimized marking polygons, decomposition algorithm and design guides. Our main contributions are as follows. (1) The optimal marking polygons, which group the direct contacts of the pair transistors, are designed to consider the layout configurations of pair transistors. The space between each contact located on the same marking polygon is designed to be larger than the resolution limit of the single exposure, so that the contacts grouped by the same marking polygon can be decomposed as the same color. (2) The whole contacts grouped by the same marking polygon are transferred to the representative single contact, and then the colors of the grouped contacts are assigned by the representative single contact and its surrounded contacts. (3) If the grouped contacts have two colors because of the layout situations, then the design guides such as the odd-cycle removing are applied to assign the single color to the grouped contacts. Consequently, we can achieve the pattering margin and electrical performance of the sub-30nm device by applying the new DPT methodology to the direct contact.

7974-17, Session 4

Performance and manufacturability trade-offs of pattern minimization for sub-22-nm technology nodes

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The traditional design rule paradigm of defining the illegal areas of the design space has been deteriorating at the advanced technology nodes. Radical design space restrictions, advocated by the regular design fabrics methodology, provide an opportunity to reshape the design/manufacturing interface by constraining the layout to a set of allowable patterns. As such, this would allow for guaranteed convergence of the source mask optimization techniques (SMO) and complete validation of the legal design space during technology development and ramp. However, the number of the unique patterns generated by the layout adhering to even the simplistic gridded design rules prohibits this approach. Nevertheless, we have found that just 10% of the unique geometric patterns are sufficient to represent 90% of all layout pattern instances. Furthermore, the overall number of layout patterns on Active, Contact, and Metal-1 design layers can be reduced through modification of existing layout shapes in the final layout database and insertion of non-essential layout features. Unlike the ‘dummy fill’ used for chemical mechanical polishing (CMP), the newly added shapes must resemble the patterning of the functional design features and be inserted in close proximity to them. In this paper, we evaluate the digital circuit performance impact of the additional layout parasitics introduced by these ‘dummy’ features. In particular, we have found that a significant pattern count reduction can be achieved with minimal performance penalty. Furthermore, we will show how the pattern minimization can lead to reduction in variability of the layout parasitics, and thus require less design margining to achieve equivalent design specifications. These results have been used at PDF Solutions to enable a correct by construction layout style, such as the templates and connectors-based layout methodology presented in the companion paper.

7974-18, Session 5

Design strategies for cost-effective, automatically DPT/MPT-compliant layout for advanced logic nodes

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As device scaling progresses beyond the 28nm logic node, the economic challenges associated with lithography become almost as formidable as the technical challenges. In particular, in light of the uncertainty in cost and availability of EUV technology, many device manufacturers are now investigating double-patterning (DPT) and multi-patterning (MPT) strategies to achieve the required die area scaling with existing optical technology. The mask count for such approaches can be quite high, and the cost of multiple patterning must therefore be carefully justified by the amount of area shrink achievable, with cost-per-good-die becoming a critical metric for assessing design rule and patterning choices.

To that end, we have developed a sophisticated infrastructure for (i.) streamlining design rule definition for 20nm and 14nm logic nodes assuming a number of single-exposure, double- and multiple-pattern techniques; (ii.) relating those rules to area scaling using a 'perturbative' place-and-route technique with appropriately scaled standard cells; and, (iii.) combining the results with rigorous cost modeling to assess cost-per-good-die. In this paper, we apply this infrastructure to assess patterning and rule choices for 20nm and 14nm logic nodes for a wide range of design rule and patterning choices, including single-exposure with source/mask optimization, litho-etch-litho-etch double-patterning (LELE DPT), litho-freeze-litho-etch DPT and spacer-assisted double-patterning. We demonstrate that aggressive double patterning with appropriately chosen design rules is by far the most cost effective solution for the 20nm node, independent of mask cost assumptions. Furthermore, for the 14nm logic node, we demonstrate that a multi-patterning solution also can be cost-effective if design rules are judiciously chosen.

One important side benefit of this work is that we have been able to develop several strategies for ensuring automatic DPT decomposition compliance, in both standard cell layout and in auto-routing, based on a handful of rule restrictions. We discuss benefits and tradeoffs of these design strategies, from the perspective of complexity and cost-per-die added. We also show results from detailed place-and-route studies to demonstrate the implementation of the above restrictions and strategies in software. For LELE DPT, we find minimal impact on actual routed area and run time, even in the most restrictive rule case.

7974-19, Session 5

Decomposition-aware DRC to enable double-patterning compliant standard cell libraries

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See attached file for full text with figures

Abstract

Maintaining the microelectronics industry's aggressive pace of density scaling beyond the resolution limits of optical lithography is forcing the introduction of double-patterning techniques. One specific implementation of double-patterning, commonly referred to as: 'pitch-splitting', extends the useable resolution of optical lithography by employing sequential, interdigitated, and optically-decoupled patterning operations at twice the ultimately desired feature pitch to achieve the desired pattern density. While the process-complexity and cost impact of double-pattering continues to be a concern, this work focuses on mitigating the inevitable impact to design rules, tools, and methodologies.

After briefly reviewing the design constraints imposed by pitch-split double-patterning and comparing several approaches to ensuring decomposition compliant layouts, this paper presents a design flow that has been implemented in the 20nm technology node to support design for double-patterning of a local interconnect level. Based on cell-level design rule checking that incorporates feature decomposition under observation of appropriate boundary conditions, the developed design flow is shown to minimize the impact of double-patterning on established design methodologies while guaranteeing that a decomposition solution can be found during chip tape-out or during mask data preparation. Data are presented demonstrating the design efficiency, density, and manufacturability benefits of the developed solution.

Further Details for Program Committee Review

As described in the author's 2010 SPIE publication (1), double-patterning layout compliance can be achieved by either: restrictive design rules, split-level design rules, or double-patterning embedded design rule checking. While restrictive design rules offer a very efficient correct-by-construction solution for many design levels, the necessary pitch and orientation restrictions do not lend themselves well to all design levels in conventional layout styles. Some design levels, like the local interconnect level under investigation here, need to be significantly two-dimensional and generally unrestricted to achieve their intended function. Split-level design rules, in which the two components making up the desired design level are simply specified as two unique design levels with inter and intra level design rules, are attractive in that they require no enhancements to existing design tools and they do not constrain designer creativity. However, exercising split-level design rules in the 20nm node, raised two specific concerns:

Manually solving the two color mapping problem imposed by the split-level rules for complex two-dimensional layouts proved extremely challenging and negatively impacted design efficiency.

Explicitly decomposing layouts at the cell-level impacted cell placement density. As shown in figure 1, three standard logic cells that are each legally decomposed into the two pitch-split mask levels, can not be placed adjacent to each other due to intra-cell decomposition conflicts. The space between the 2nd and 3rd cell would have to be increased to account for the sub-resolution space formed by layout features decomposed onto the same mask level. And, as illustrated by the space between the 1st and 2nd cell, even an innovative placement tool that could reverse the assigned decomposition based on same-level spacing errors, would not be able to resolve conflicts arising from decomposition 'stitches' propagating across cell boundaries.

Figure 1, Three logic cells decomposed for pitch-split double-pattering using explicit split-level design rules can not be placed next to each other without density loss due to cell-to-cell decomposition errors.

The goal of the developed double-patterning design flow was to overcome these shortcomings by providing an automated decomposition solution in which the design is not permanently decomposed at the cell-level. Rather, once the decomposability of the design has been verified at the cell-level, only the combined design level is taken forward to allow optimal post-placement decomposition. Key to this solution are a set of boundary conditions which guarantee that cells, once deemed pitch-split compliant at the cell level, can always be legally decomposed after placement. These boundary conditions are illustrated in figure 2 in form of a net-coloring diagram. The different color nodes in the nets indicate transitions from mask 1 to mask 2 (red) and mask 2 to mask 1 (green). While the colored nets inside the cell can have as many branches and loops as are necessary to decompose complex two-dimensional layouts, this set of boundary conditions prohibits decomposition information from bridging across the horizontal cell boundaries and allows only a single node on each vertical boundary. By ensuring linear coloring runs across all rows of placed cells, these boundary conditions guarantee that post-placement decomposition will always be successful.

Figure 2, Boundary conditions imposed on automatic layout decomposition at the cell-level (left) ensures that a legal decomposition solution can be obtained after placement without sacrificing cell-to-cell spacing.

Figure 3 shows the same three logic cells decomposed with these boundary conditions and Figure 4 shows one possible placement of these cells with post-placement decomposition.

Figure 3, Three logic cells decomposed with boundary conditions preventing decomposition information crossing the horizontal cell boundaries and preventing feature 'stitching' near the vertical cell boundaries.

Figure 4, Three logic cells placed and decomposed in context of

each other, demonstrating the effectiveness of the imposed boundary conditions in ensuring legal decomposition.

This paper will present more details on this innovative design solution and will shown the design efficiency and manufacturability benefits it provides.

(1) Taming the final frontier of optical lithography: design for sub-resolution patterning, Lars W. Liebmann, Jongwook Kye, Byung-Sung Kim, Lei Yuan, and Jean-Pierre Geronimi, Proc. SPIE 7641, 764105 (2010)

7974-20, Session 5

Layout decomposition of self-aligned double patterning for 2D random-logic patterning

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Self-aligned double pattering (SADP) is a pitch-splitting sidewall image method that is a major option for sub-30nm device node manufacturing due to its lower overlay sensitivity and better process window compared to other double patterning processes, i.e., litho-etch-litho-etch (LELE) DPT. SADP is in production use for 1D patterns in NAND Flash memory applications but applying SADP to 2D random logic patterns is challenging.

The favored type of SADP for complex logic interconnects (called SID “Spacer Is Dielectric”) is a two mask approach using a Core (Mandrel) mask and a Trim mask. The Core mask is the 1st lithographic mask, meanwhile sidewall spacer patterns are formed around it in a subsequent process. The Core mask layout consists of two kinds of features: a Base Core layout which is a chosen subset of the design intent, and an Additional Core layout whose features need to be newly generated. There are many challenges involved with choosing manufacturable Base Core layouts and creating additional Core features for complex 2D layouts. The Trim mask provides additional flexibility for patterning 2D patterns on wafer but it requires an intelligently designed Core layout as a good starting point. Therefore the design of a Core mask as well as a Trim mask is of utmost important step in an SADP mask synthesis process.

In this paper, we report the application of SADP technique to sub-30nm logic metal layouts by utilizing SID-type SADP design automation program. This paper describes methods for automatically choosing and optimizing the manufacturability of Base Core patterns, generating Additional Core patterns, and optimizing Trim mask patterns in SID SADP process. Moreover, we review the unique layout decomposition requirements for SID-type SADP. Results of SADP for metal layouts are compared with other double patterning technologies, e.g., LELE DPT.

7974-21, Session 5

A state-of-the-art hotspot recognition system for full-chip verification with lithographic simulation

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In today’s semiconductor industry, prior to wafer fabrication, it has become a desirable practice to scan layout designs for lithography-induced defects using advanced process window simulations in conjunction with corresponding manufacturing checks. This methodology has been proven to provide the highest level of accuracy when correlating systematic defects found on the wafer with those identified through simulation. To date, when directly applying this methodology at the full chip level, there has been unfavorable expenses incurred that are associated with simulation which are currently overshadowing its primary benefit of accuracy - namely, long runtimes and the requirement for an abundance of cpus. Considering the aforementioned, the industry has begun to lean towards a more practical application for hotspot identification that revolves around topological pattern recognition in an attempt to sidestep the simulation runtime. This solution can be much less costly when weighing against the negative runtime overhead of simulation. The apparent benefits of pattern matching are, however, counterbalanced with a fundamental concern regarding detection accuracy; topological pattern identification can only detect polygonal configurations, or some derivative of a configuration, which have been previously identified. It is evident that both systems have their strengths and their weaknesses, and that one system’s strength is the other’s weakness, and vice-versa.

A novel hotspot detection methodology that utilizes pattern matching combined with lithographic simulation will be introduced. This system has a high potential to decrease the amount of processing time spent during simulation, to relax the high, cpu count requirement, and to maximize pattern matching accuracy by incorporating a multi-staged pattern matching flow prior to performing simulation on a cropped data set. Also brought forth will be an original methodology for constructing the core pattern set, or candidate hotspot library, in conjunction with establishing the hotspot and coldspot pattern libraries. Lastly, it will be conveyed how this system can automatically improve its overall potential as more designs are passed through it.