Technical Abstract Summaries

SPIE Advanced Lithography

Conferences and Courses: 21-25 February 2010
Exhibition: 23-24 February 2010
San Jose Marriott and San Jose Convention Center, San Jose, California, USA

Technical Abstract Summaries:

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Conf. 7636: Extreme Ultraviolet (EUV) Lithography

Monday-Thursday 22-25 February 2010

Part of Proceedings of SPIE Vol. 7636 Extreme Ultraviolet (EUV) Lithography

7636-01, Session 1

Actinic phase-defect detection and printability analysis for patterned EUVL mask

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Understanding the impact of phase defects on the printed pattern size variation is important for the development of practical defect-free EUVL mask fabrication processes. We have developed an actinic EUV mask blank inspection tool which has the potential to detecting all critical phase defects on EUVL mask blanks (Fig. 1). In this tool, a 0.5 mm square area dark-field image of the mask blank was captured by a backside-illuminated CCD camera. Full field mask blank inspection was performed using TDI (Time Delay and Integration) operation mode. Despite the comparatively large pixel size of 500 nm at mask blank, inspection sensitivity of detecting small defects of 60 nm in width and 1.5 nm in height was confirmed using programmed phase defecs. Moreover, natural phase defect detection using this tool has also been started.

In this tool, the use of the dark-field observation method has been extended to the inspection of EUV patterned mask with periodic absorber patterns. To evaluate the effect of overlap error between phase defects and absorber patterns on both the phase defect detection sensitivity and its printability, a test mask including programmed bump phase defects and absorber lines with several sizes was fabricated (Fig. 2). Programmed phase defects with a height of 2 nm were arrayed in such a way that the pitch differs from that of the absorber line pitch (256 nm, 288 nm, 360 nm) because it is almost impossible to locate the absorber patterns with pre-defined specific distance from the phase defect due to a lack of an alignment capability in the absorber patterning.

When the periodic absorber line patterns are illuminated, they generate diffracted light. The higher orders of these diffracted lights are captured by the dark-field imaging optics and then contribute to the pixel intensity even when there is no phase defect involved. Simulation and experimental results show that the periodic absorber lines increase the backgrounds of inspection signal depending on the absorber pitch while a phase defect signal component is maintained when the phase defects were located between the absorber patterns (Fig. 3).

Based on these, projected pattern images obtained from the mask with both the absorber patterns and the phase defects were evaluated. Multilayer defect printability as a function of distance between multilayer phase defect and neighboring absorber lines were clarified by image simulation and exposure experiments. The relationship between phase defect detection sensitivity and its printability from the viewpoint of projected pattern CD error will be discussed.

This work was supported by New Energy and Industrial Technology Development Organization (NEDO).

7636-02, Session 1

Optics for EUVL production

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We review the current status of EUV optics development at Carl Zeiss SMT AG for ASML's NXE 3100 tools and give an outlook on the EUV optics roadmap.

In 2005, Carl Zeiss SMT AG has shipped two sets of illumination and projection Optics for ASML's Alpha Demo Tools. Meanwhile, the Alpha Demo Tool has been successfully tested and imaging down to 25 nm was demonstrated.

In parallel, new mirror sets with improved specifications for the next generation tools have been fabricated. These sets of optics are characterized by significantly lower flare and wave-front levels. In addition a new illumination system has been developed. We will focus on mirror fabrication and at wavelength qualification results of the optical systems produced so far. In detail we will discuss the obtained wave-front and stray-light performance.

We will give an outline of the next generation, a 0.32NA exposure tool including EUVL off-axis illumination for resolutions down to 16nm. We take the expected imaging requirements as a starting point and compare it with the current status of our technology development. A brief overview for further tool extensions by higher NA will be given as well.

We gratefully acknowledge support for our EUV program by the Bundesministerium für Bildung und Forschung, MEDEA Project EXTATIC" and European Commission Project More Moore".

7636-03, Session 1

Characterization of promising resist platforms for sub-30-nm HP manufacturability and EUV-CAR extendibility study

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EUV lithography (EUVL) is the most effective way to print sub-30 nm half-pitch (HP) features. Using the 0.3 NA SEMATECH Berkeley microfield exposure tool (MET) and Albany EUV MET, we have evaluated resists for potential use on full-field tools. We characterized the performance status of three major kinds of EUV resist platforms for developing advanced EUV resist: a blended PHS type, a polymer-bound PAG, and a molecular type. We will analyze both the strong and weak points of these resist platforms, considering EUV resist manufacturability including process feasibility data such as resolution, depth of focus, photosensitivity, line edge roughness/line width roughness (LWR), resist collapse, and LWR improvement dependency with a post-rinse process.

We will characterize EUVL resist readiness for sub-30 nm HP manufacturability with advanced resists using a full-field alpha demo tool (ADT) scanner. Detailed process data for ~27 nm HP patterning will be reported, and the feasibility of a ~0.50k1 resist process using an ASML ADT will be characterized. We will demonstrate sub-20 nm HP resolution and 16nm HP image modulation for a chemically amplified EUV resist extendibility study.

7636-04, Session 2

Characterization of line-edge roughness (LER) propagation from resist: underlayer interfaces in ultra-thin resist films

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It has been understood for some time that physical properties of thin polymeric films coated on substrates are dominated by their surface interactions with the substrate. For glassy polymers such as those employed in photoresists, perturbation of bulk properties at the substrate interface may propagate more than 50 nm into the polymer film.1

As semiconductor lithography moves toward pitches below 80 nm,

resist films with thicknesses of 100 nm and below will be required. Behavior of these films will become increasingly dominated by their substrate interactions. Numerous previous studies have demonstrated that properties of photoresist materials such as glass transition temperature, acid diffusivity, and imaging behavior change systematically as film thickness is decreased.2 Recent work in EUV photoresist development has highlighted that substrate materials play a critical role in affecting imaging performance and can improve LER, resolution, and process window.3

In this presentation, we describe another aspect of ultrathin resist behavior, specifically LER evolution along the resist sidewall of EUV resists. We amplify on Foucher's observation4 that LER both increases and becomes less isotropic as the resist sidewall approaches the substrate interface. We observe that the sidewall topography of multiple EUV photoresists is dominated by striated features that originate at the substrate and propagate toward the top of the resist film. These findings are in contrast to observations of isotropic, pebbled roughness of larger resist sidewalls described in previous studies5 and predicted by recently developed stochastic models.6 We detail systematic efforts to reduce these striated structures based on resist and substrate characterization (chemical, AFM, etc.) and engineering of the surface interaction between EUV resists and high-silicon content spin-on hardmask materials.7 We use the results of these studies to assess several hypotheses regarding the origins of the striated structures.

7636-05, Session 2

Mechanistic studies of arylsulfonate photoacid generators (PAGs) for EUV lithography

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One of the requirements of photoacid generators (PAG) in extreme ultraviolet (EUV) lithography is an increase in quantum yield and higher acid generation. Arylsulfonates are a new class of neutral photoacid generators being developed for EUV lithography. These neutral photoacid generators have shown sufficient thermal stability, potential for high loadings in resists, and functionalization to triflates, nonaflates, tosylates or other potential acid producing molecules.

This research focuses on elucidating the mechanism of activation and acid production in arylsulfonate PAGs to improve the overall acid production and photospeed in future PAGs. At this time arylsulfonates are much less potent acid generators than the ubiquitous triarylsulfonium salts. The study focuses on diarylsulfidotriflates such as 1 which have shown great potential with fast photospeeds (relative to other neutral aryltriflates) and straightforward structural tuning. Based on product analysis following pulse radiolysis, DUV photolysis, electrochemical reduction and e-beam exposure, we propose that aryltriflate PAGs can undergo one of two major cleavage pathways (Scheme 1). In the case of PAG 1, one pathway involves C-O cleavage producing triflic acid, CF_3SO_3H, and phenyl compound 2. The other path leads to S-O bond cleavage which produces the weaker triflinic acid, CF_3SO_3H, and phenol 3. The reactivity of PAG 1 is compared to related compounds where varying ratios of C-O vs O-S cleavage products is observed depending on molecular structure. The proposed reaction pathways are used to understand and predict performance of arylsulfonate PAGs in EUV resists.

7636-06, Session 2

Thin EUV resist and underlayer stacks: correlating Tg, surface polarity, density, and image quality

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Traditionally, one of the best ways to improve the resolution of a resist has been to reduce its thickness. Unfortunately, however, the lithographic properties of today's many advanced resists degrade dramatically when coated to thicknesses of < 50 nm. Figure 1 shows how the LER of resists prepared by us (OS1 and OS2) and by commercial resist suppliers degrade in thinner films. This is an important problem, independent of wavelength, which needs to be understood and resolved by the electronics industry so that resists capable of meeting the goals of the 22 nm node and beyond can be produced. More mechanistic investigations into the physical properties of these films are necessary to further understand the imaging degradation in thin photoresist films. We assert that inserting organic underlayers between the resist and substrate with specifically designed physical properties can help improve the overall performance of the resist.

In this work, we physically characterized the glass transition temperature (Tg) of multiple EUV resist systems using thermally programmed ellipsometry and x-ray reflectometry as a function of thickness. The density profiles of these resist systems as a function of thickness was also measured using x-ray reflectometry. The measured Tg's and density's were directly compared to the imaging quality of the resist materials as a function film thickness. A series of organic underlayers were specifically designed to cover a range of glass transition temperatures and surface polarities. The image quality of resist/underlayer stacks as a function of Tg and surface polarity of the individual resist and underlayer materials will be presented.

7636-08, Session 2

Study on approaches for improvement of EUV-resist sensitivity

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Extreme ultra violet (EUV) lithography process is one of the most promising candidates for half-pitch 22nm generation device manufacturing and beyond. In EUV lithography, great evolution of resist materials is as important as that of light source, exposure tool, and mask quality. The important performances required for EUV resist material are high sensitivity, excellent resolution, low line width roughness (LWR), and low out-gassing level. It is well known that there is triangle-tradeoff relation among the performances of sensitivity, resolution, and LWR. A lot of efforts have been paid to make a breakthrough in the tradeoff relation, however, these three performances can not simultaneously satisfy the ITRS roadmap target of hp 22 nm node at this moment. There are some resists satisfying sensitivity (10 mJ/cm2), however, such resists usually showed poor resolution or / and LWR performances. Therefore, the technology for improvement on sensitivity with keeping good resolution and LWR performances is keenly desired.

In this paper, study on approaches for improvement of EUV resist sensitivity will be discussed. It is well known that high chemical amplification efficiency is one of the effective methods to improve sensitivity. Enlargement of generated acid diffusion length at post exposure bake (PEB) step can increase chemical amplification efficiency, however, resolution performance should become worse due to the large chemical blur caused by long diffusion length. This fact indicates that it is important to enhance the chemical amplification efficiency without increase of chemical blur.

Larger acid loading amount can improve sensitivity without chemical blur increase, since larger density of photo acid generator (PAG) results effective secondary electron trapping by PAG cation unit. However, we have found that there's limitation in sensitivity improvement with this method, because the PAG density increase leads decrease on density of EUV light sensitizer that generates secondary electron.

To enhance the efficiency of sensitization to EUV light, and to enhance the efficiency of secondary electron generation are also effective to improve sensitivity. We have found that several low ionizing potential polymer showed high acid generation efficiency with e-beam radiation, however, the sensitivity to EUV of the resist is not as high as expected.

Another viewpoint is de-blocking reaction step. If the reaction efficiency can be enhanced without any acid diffusion length increase, the sensitivity should be increased. We have found that a generated acid with large molecular size showed less acid diffusion length dependence on temperature compared to the conventional smaller molecular size acid. Higher sensitivity with keeping resolution and LWR can be expected with such large molecular size acid by higher temperature at de-blocking reaction, if the de-blocking reaction efficiency depends on temperature strongly. We have newly designed the large molecular size acid for PAG and appropriate blocking group, and sensitivity improvement with keeping resolution and LWR performance was confirmed by e-beam direct writing patterning. Evaluation results with EUV lithography will be also discussed.

7636-09, Session 2

Polymer photochemistry at the EUV wavelength

T. H. Fedynyshyn, R. B. Goodman, A. Cabral, Lincoln Lab. (United States); C. Tarrio, T. B. Lucatorto, National Institute of Standards and Technology (United States); A. Spanos, Lincoln Lab. (United States)

Polymer photochemistry depends on photon absorption, which leads to the production of an excited electronic state of the polymer. If the excitation level is greater than the bond dissociation energy, the excited polymer dissociates into free radical fragments that can then further react to produce chain scission or polymer crosslinking. The energy associated with wavelengths of light commonly employed in lithography gradually increases as the wavelength is decreased, going from 115 to 147 to 182 kcal per mole at 248-nm, 193-nm, and 157-nm respectively. This level of energy can be compared with typical carbon-carbon bond dissociation energies of 90 to 120 kcal per mole implying that significant bond breaking photochemistry occurs.

The insertion of EUV, with a 13.4-nm wavelength, into the lithographic roadmap greatly increases the energy available for deposition into the resist polymer to 2133 kcal per mole. The higher energy associated with EUV coupled with the high molecular absorptivity for most organic polymers at EUV should lead to increased excited state population and higher quantum yields of photoproducts. The pathway in which different polymers respond to this light energy, be it chain scission or crosslinking, will determine in large part the ability of resists designed at 193 or 248-nm to operate as EUV resists.

Polymers representative of those commonly employed in resists as well as some model polymers were selected for this study. Polymer photochemistry at EUV was catalogued as to the effect of absorbed 13.4-nm radiation on a polymer's propensity toward chain scission (s) versus crosslinking (x). In selected cases, the chain scission and crosslinking quantum yields were also compared to those previously determined at 157-, 193- and 248-nm. Quantum yields were determined by following the change in molecular weight, both Mn and Mw, as a function of different absorbed doses, D, by a GPC (gel permeation chromatography) method. Solving Equations [1] and [2] simultaneously allows both s and x to be determined.

Equation 1 1 / Mn,D = 1 / Mn,0 + [s - x] * D / NA

Equation 2 1 / Mw,D = 1 / Mw,0 + [s / 2 - 2 x] * D / NA

In the case where molecular weight decreases, it is important to determine if material outgassing is occurring and whether the outgassing occurs from small molecular weight fragments caused by chain scission or by side change fragmentation. The nature of the material loss was determined for selected polymers where chain scission and material loss are significant. This knowledge can be used to design polymers that minimize undesired photochemical transformations and reduce material outgassing.

*The Lincoln Laboratory portion of this work was sponsored by a Cooperative Research and Development Agreement between Lincoln Laboratory and Intel Corporation. Opinion, interpretations, conclusions, and recommendations are those of the authors and are not necessarily endorsed by the United States Government.

7636-10, Session 2

Analysis of trade-off relationships in resist patterns delineated using SFET of Selete

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The small-field exposure tool (SFET) installed to Semiconductor Leading Edge Technologies, Inc. (Selete) is an indispensable tool for the development of resist materials for extreme ultraviolet (EUV) lithography. In the development of next-generation resist materials, the trade-off relationships between resolution, sensitivity, and line edge roughness (LER) are the most serious problem. Among three requirements, LER is known to be inversely proportional to the chemical gradient. In this study, we investigated line-and-space resist patterns delineated using SFET in terms of the trade-off relationships. By changing the exposure dose and half-pitch of line-and-space patterns, the width of line patterns and LER were measured. The range of half-pitch was 22-60 nm. The exposure dose was changed from 9.5 to 13.5 mJ cm-2 with a step of 0.5 mJ cm-2. The experimental results were analyzed using a simulation on the basis of EUV sensitization mechanisms. The relationships between resolution, sensitivity, and LER were successfully reproduced. On the basis of experimental and simulation results, the reaction mechanisms of chemically amplified EUV resists are discussed.

7636-07, Session 3

Laser-produced plasma source development for EUV lithography

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We report the latest status of our laser produced plasma light source for high volume manufacturing (HVM) EUV lithography [1]. The light source is based on a high power, high repetition rate CO2 laser system, a tin droplet target and magnetic plasma guiding for collector mirror protection. This approach enables cost-effective high-conversion efficiency and EUV power scaling. The light source is scalable to more than 200 W EUV in-band power based on a 20-kW CO2 laser.

The drift of the droplet target was reduced to maintain stable EUV pulse energy with high power CO2 laser and the Sn droplet target. Collector mirror lifetime can be extended by using the droplet target with magnetic plasma guiding. Effectiveness of the magnetic plasma guiding is examined by monitoring the motion of fast Sn ions in a large vacuum chamber. The ion flux from a Sn droplet plasma was confined along the magnetic axis.

We have achieved a maximum average laser output power of more than 10 kW at 100 kHz for a single laser beam with good beam quality. High duty long term CO2 laser system operation is currently being tested. EUV in-band power and image are measuring at intermediate focus point with high power CO2 laser and Sn droplet target configuration.

The development status of the source system and its performance including EUV characteristics will be described in detail. Relevant topics of HVM sources including the future light source development will be outlined. A part of this work was supported by the New Energy and Industrial Technology Development Organization (NEDO), Japan.

[1] A. Endo, et al., 'Laser-produced plasma source development for EUV lithography': Proc. SPIE 7271 (2009).

7636-08, Session 3

EUV source development for AIMS and blank inspection

M. J. Partlow, S. F. Horne, M. M. Besen, D. K. Smith, D. Gustafson, P. A. Blackborow, Energetiq Technology, Inc. (United States)

With EUV Lithography readying for production, the need for commercially available actinic mask inspection tools has become more critical. In June 2009, Bryan Rice of Sematech stated: “The lack of mask inspection gear for EUV lithography threatens the future viability of EUV in the market”. A key to developing a successful mask inspection tool is a reliable high brightness EUV light source that is readily available to support production pilot lines. Requirements have been identified by the major tool inspection and metrology manufacturers outlining brightness needs to ensure a high throughput, high sensitivity tool required by the fabs [1].

The Energetiq EQ-10 is a commercially available, medium-power (10 W /2 pi, 13.5nm +/- 1%, Xenon) electrodeless Z-pinch light source, with the demonstrated reliability of over 15 sources in the field [2]. The EQ-10 EUV source is being used today for laboratory based actinic mask blank inspection at Selete [3].

Results will be presented from a development program, currently under way, to optimize the EQ-10 source for higher brightness specifically for use in mask inspection tools. The platform used for this work is a new version of the EQ-10, designed for longer lifetime of components. The redesigned source demonstrates increased EUV power and brightness when compared with the standard EQ-10. The development program aims to optimize source operating conditions and pinch geometries of the new source to reduce plasma size without loss in power and thus maximize brightness. We will also report on an EUV transmission module that, when combined with the EQ-10, offers a system that meets inspection tool requirements including spatial stability, pulse to pulse stability, clean photons as well as high reliability in 24/7 operation.

Finally, a novel technique will be introduced that is intended to increase the brightness of the EQ-10 by a further order of magnitude, to improve mask inspection tool throughput to high volume levels.

[1] SEMATECH EUV Source Workshop. 29-30 May 2009; Baltimore, Maryland

[2] P. A. Blackborow, M. J. Partlow, S. F. Horne, M. M. Besen, D. K. Smith, and D. S. Gustafson, “EUV Source Development at Energetiq,” Emerging Lithographic Technologies XII. Proc. SPIE 6921, pp. 692121-692121-11 (2008).

[3] T. Terasawa, T. Yamane, T. Tanaka, T. Iwasaki, O. Suga and T. Tomie, “Development of actinic full-field EUV mask blank inspection tool at MIRAI-Selete,” Alternative Lithographic Technologies. Proc. SPIE 7271, pp. 727122-727122-8 (2009).

7636-09, Session 3

Analysis, simulation, and experimental studies of YAG and CO_2 laser produced plasma for EUV lithography sources

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Efficient laser systems are critical for the realization of high volume manufacture in EUV lithography development. Current solid-state Nd:YAG lasers are usually have lower efficiency and source suppliers are alternatively investigating the use of high power CO2 systems. However, CO2 laser plasmas have specific characteristics that should be taken into account when designing Laser Produced Plasma (LPP) devices. The analysis of recent experimental and theoretical work showed significant differences in properties of plasma plumes produced by the CO2 and the Nd:YAG lasers including EUV source formation, debris generation, and the conversion efficiency. The much higher reflectivity of CO2 laser from liquid, vapor, and plasma of a tin target results in the production of optically thinner plume with higher velocity and in a shifting of plasma properties (temperature and density values) for more efficient EUV source. The irregular temporal pulse shape of current CO2 devices will additionally affect the properties of the produced plasma.

We have developed unique combination of experimental facilities (CMUXE Laboratory) and advanced computer simulation (HEIGHTS package) for studying various lasers and target parameters and optical collection system concerning EUV lithography. Detail plasma characteristics of both CO2 and Nd:YAG lasers were analyzed and compared both experimentally and theoretically for optimization of LPP and higher conversion efficiencies. This study explains the less overheating of plasma by CO2 laser with time and explains how to utilize the high reflectivity of such lasers in different target geometries to significantly enhance the conversion efficiency.

7636-10, Session 3

Sn debris cleaning by plasma in DPP EUV source systems for HVM

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The tin (Sn) debris contamination is one of the technical challenges for the development of high power EUV light source with Sn fuel with a long lifetime of EUV collectors. The debris mitigation techniques (DMTs) can considerably minimize the Sn debris coming out of the source thereby reducing the need or effort for cleaning. However, for HVM, which requires higher EUV power output than today, it is questionable if the DMTs alone will completely eliminate the Sn contamination. Besides, at abnormal instances, we also need to clean thick Sn debris from the mirror surface.

For this purpose, the Center for Plasma Material Interactions (CPMI) at University of Illinois, Urbana-Champaign has developed a plasma-based Sn cleaning method using chlorine plasma with densities and temperature around ~9x10^9 /cm3 and ~ 4 eV respectively. From our previous studies, it was shown that chlorine plasma etching can remove Sn debris from Ru mirror surface in a fast (> 400 nm/min) and in situ manner. In this study, we applied the same method to clean Sn contamination on the mock-up collector in our XTS13-35 DPP EUV source system. The mock-up is made of two shells with different gap widths (1 cm, 7.5 cm and 10 cm) in similar size with the actual collector optic. The cleaning rate at different locations on the mock-up was experimentally investigated, and it was found that the cleaning rates vary largely with the distance from the chlorine plasma in the range of 20 - 100 nm/min. In addition, a simple analytical model to predict the cleaning rate was developed based on the plasma-surface reactions and the plasma transport. The model describes how plasma transport, chlorine radical distribution and pumping flow affect the Sn cleaning rate with chlorine plasma. Finally, the model is then compared to the experimental results and validated.

Based on the knowledge of chlorine plasma and Sn interactions obtained in this study, a remote plasma cleaning technique was also investigated and the results obtained therein are presented. The experimental results along with our model predictions will help design an integrated cleaning system for collector optic in the high power EUV source system for HVM.

7636-11, Session 3

Development and performance of grazing and normal incidence collectors for the HVM DPP and LPP sources

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Media Lario Technologies has designed the HVM collector for the Sn-fueled DPP source developed by Philips Extreme UV and XTREME technologies, and has developed the corresponding manufacturing technology and processes based on replication by electroforming. The performance of the HVM collector demonstrator described in this work supports a point-source collection efficiency of 25% and is enabled by an integrated thermal control system ensuring optical stability for an absorbed thermal load of 6 kW. The ruthenium reflective layer has been custom tailored to match the debris mitigation strategy developed and characterized by Philips Extreme EUV, supporting a 1-year lifetime proposition of the source-collector module. This optical collector system, integrated in the Sn-DPP source developed by Philips EUV and XT, supports the source power scaling roadmap meeting the HVM scanner requirements of 200+ W at intermediate focus.

This work will also report a progress update on the application of MLT’s proprietary manufacturing processes, based on replication by

electroforming, to normal incidence collector optics for LPP sources. Particularly, we will report on metallic normal incidence mirrors with figure accuracy better than 150 nm and Angstrom level surface roughness, showing compatibility with EUV reflective layers.

7636-12, Session 3

Experimental and numerical investigations on the density profile of CO_2 laser-produced Sn plasma for an EUVL source

Y. Tao, Univ. of California, San Diego (United States)

A powerful, efficient, long-lifetime, and cost-effective extreme ultraviolet (EUV) source is the most critical issue in the development of EUV lithography. CO2 laser-produced Sn plasma has been considered as the most promising EUVL source for high volume manufacturing. Even though, industries are trying to deliver CO2 laser driven EUVL source for the starting application of EUVL, fundamental researches are still necessary to make further understanding of the plasma physics, to enable more meaningful numerical simulation with a radiation hydrodynamic code to optimize and design the EUVL source with higher power and a lower cost for the improved EUVL.

The density profile of the CO2 laser-produced Sn plasma was experimentally observed with a time-resolved IR interferometer under the favorite conditions for efficient 13.5 nm EUV emission generation. At the same time, the density profile was numerically evaluated with a 1-dimensional radiation hydrodynamic code (HYADES), which predicts a good agreement with the experimentally observed density profile of the Sn plasma irradiated with Nd:YAG laser. It was found that the experiments show much steeper plasma density profiles as compared with those from numerical simulation. Typical results for 25 ns pulse duration are shown in Fig.1. Much larger differences in plasma expansion from experiment and numerical simulation are noted for longer pulse durations, like 85 ns. It is suggested that the physics involved in the Sn plasmas irradiated with Nd:YAG and CO2 lasers are much different. The plasma physics models and parameters for ionizations, thermal electron transport, and radiation transport etc. used in the numerical code should be very carefully chosen according to the experimental data. We will present the comparisons between the experimentally observed density profiles with laser various pulse durations with those from the numerical code using various physics models and parameters. This research could provide a more solid foundation for the application of numerical method to the development of the EUVL source.

7636-13, Session 4

Complex species and pressure dependence of intensity scaling laws for contamination rates of EUV optics determined by XPS and ellipsometry

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The experience with pre-production extreme-ultraviolet (EUV) lithography systems has demonstrated that carbon contamination of the illumination and projection optics is one of the primary sources of throughput loss. Although successful cleaning strategies have been demonstrated, it is important to know what contamination rates to expect under different conditions in order to predict the down time for cleaning in high volume manufacturing. The ongoing EUV optics contamination program at the synchrotron facility of the National Institute of Standards and Technology (NIST) addresses this issue by measuring the contamination rates and scaling behavior of various organic species that are likely to be found in the tool vacuum environment of an EUV lithography tool.

Previous NIST studies of TiO2-capped multilayer samples exposed to synchrotron radiation demonstrated a highly sub-linear (approximately logarithmic) dependence of the carbon-deposition rate on the partial pressure of the ambient organic species over 3 to 4 decades.[1] Strong correlation with independent studies of non-irradiated surface coverage at Rutgers University suggested this behavior is the result of adsorption/desorption processes with coverage-dependent adsorption energies.[2] The previous NIST work used micro x-ray photoelectron spectroscopy (XPS) to determine the peak thickness of the small [(1.0 by 0.8) mm] contamination spots created by the tightly focused EUV beam. This is a relatively slow technique, and direct observation of deposited C on Ru-capped samples is complicated by overlapping XPS peaks. Most importantly, the tradeoff between sensitivity and high spatial-resolution prevented reliable imaging of the spatial distribution of sub-nanometer C deposits. To overcome these limitations we have explored the use of small-spot spectroscopic ellipsometry and have obtained a sensitivity of a few Angstroms and found good correlation with XPS results.

By combining the complementary compositional information of XPS with the high-sensitivity of ellipsometry, we report new measurements showing that contamination rates for some species have a highly non-linear intensity dependence and can be strongly influenced by admixtures of water vapor, while the rates for other species are linear over the same intensity range and are less affected by ambient water. This is demonstrated in Figure 1 which shows spatial distributions of EUV-induced contamination (measured by small-spot ellipsometry) of TiO2-capped samples for isobutene and toluene with and without admixtures of water vapor. In all cases the EUV intensity distributions have a roughly two-dimensional Gaussian profile. The Gaussian contamination distribution for toluene [Fig. 1(a)] reflects this dose distribution and is not significantly perturbed by added water [Fig. 1(b)]. The less-contaminating isobutene exposure, however, shows saturation behavior at the highest intensities [Fig. 1(c)], and the addition of water results in a lower net contamination rate at the center of the beam than in the lower-intensity wings producing the halo pattern in Fig. 1(d). Results of similar exposures of other species over a range of partial pressures and intensities will be presented along with possible models to explain the observed trends. We will also discuss progress towards implementing an in situ null-field ellipsometric imaging system to monitor the contamination growth in real time.

This work is supported in part by Intel Corporation.

[1] Hill, et al, Alternative Lithographic Technologies, Proc. SPIE 727113 (2009)

[2] Yakshinskiy, et al, Alternative Lithographic Technologies, Proc. SPIE 727110 (2009)

7636-14, Session 4

Carbon film growth on model MLM cap layer: interaction of selected hydrocarbon vapor with Ru(10-10) surface

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In the present work, we report studies of the interaction of benzene, isobutene and toluene vapor with the Ru(10-10) surface, a model cap layer for multilayer mirrors (MLMs), using temperature programmed desorption (TPD), X-ray photoelectron spectroscopy (XPS), low energy ion scattering (LEIS), and electron stimulated desorption (ESD). A tunable broad-beam low energy electron source (0-200 eV) is used to simulate EUV-radiation-induced surface reactions. We have bombarded the entire sample with a defocused electron beam while exposing it to a hydrocarbon vapor from a capillary array doser. The experimental TPD results indicate that bonding of any of adsorbed hydrocarbons is dissociative on Ru(10-10). On clean Ru we find for each of these molecules that a fraction of a monolayer (ML) dissociates almost completely. Performing repeated adsorption/desorption cycles of these gases without cleaning the sample surface between cycles leads to a stepwise increase in the surface carbon coverage until saturation of about 1 ML is approached after several cycles. Desorption of molecular hydrogen due to decomposition of hydrocarbon molecule, with a multiple-peak TPD spectrum, is the only reaction product observed from the sample surface. The pyrolysis of hydrocarbon molecules with formation of 1 ML of carbon on Ru surface at temperature of 650-750 K is clearly seen. Electron bombardment

of Ru in the presence of these gas phase hydrocarbons leads to C-buildup whose thickness depends on pressure and temperature. Carbon layer thickness was evaluated from the attenuation of the Ru 3d5/2 XPS peak. On clean Ru, the C-buildup is relatively intense due to dissociative hydrocarbon adsorption and followed by the slower carbon-on-carbon growth rate. This latter rate is ~10 times higher in the presence of toluene vapor than in the presence of benzene or isobutene vapor. This behavior correlates with a higher binding energy of toluene molecules on a carbon-covered Ru surface observed in TPD spectra. Electron bombardment of fractional ML of hydrocarbon molecules yields H+ as the only ionic desorption product. A quadrupole mass spectrometer (QMS) with its ion source turned off was used for mass analysis of positive ions produced by electron impact on the adsorbed hydrocarbon layer. The total cross section for electron-induced dissociation of hydrocarbons on clean and C-covered Ru can be determined from the decay of H+ ion current as a function of time.

The work is supported by Intel.

7636-15, Session 4

Carbon contamination topography analysis of EUV masks

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Carbon contamination in extreme ultraviolet (EUV) exposure tools is one of the critical issues for the introduction of EUV lithography into high volume manufacturing (HVM), and occurs when multilayer surfaces are exposed to EUV radiation with low, partial-pressure residual hydrocarbons present. The impact of carbon contamination on EUV masks is significant due to the CD change, reflectivity loss, and contrast loss. In this work, we simulated the film stack of an Ru-capped EUV mask, but built on a 4" silicon wafer to simplify cross section analysis. Selected fields on this wafer mask were then contaminated with a series of exposures and then printed using the SEMATECH Berkeley Microfield-Exposure (MET) tool. In addition, the SEMATECH Berkeley Actinic-inspection tool (AIT) and an Atomic Force Microscope (AFM) were used to analyze the mask to determine the effect of the contamination layer on the absorbing features and printing performance.

To understand the effect of contamination topography on the printed images, the mask was cleaved and prepared for transmission electron microscopy (TEM) cross-sectional analysis in order to directly measure the carbon layer. Simulations were also used to compare the effect of actual topography on measured printed-image changes. With a full understanding of simulation accuracy, results were then used to predict printing effects that have not yet been measured including other duty cycles, carbon thicknesses, and feature designs.

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7636-16, Session 4

Monitoring EUV reticle molecular contamination on ASML's alpha demo tool

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Recent empirical results suggest that molecular contamination of EUV reticles, even at the very low partial pressures expected in the exposure chamber of EUV exposure tools, poses challenges in the implementation of EUV lithography in large scale volume manufacturing of devices. To assess the molecular contamination risk to the use and lifetime of a given EUV reticle, we have monitored the contamination build-up on a specially designed reticle during one year as it was exposed on the ASML's Alpha Demo Tool (ADT) located in Albany, New York. The reticle was exposed to an accumulated dose of well over 1600 J/cm2 of EUV photons, analyzed using a suite of complementary surface analytical techniques (such as Auger electron spectroscopy) and chemical analytical techniques (such as FTIR) as well as imaging techniques (such as scanning electron microscopy and optical microscopy), then cleaned. The influence of molecular contamination on the reflectivity of this reticle was monitored with the SEMATECH/Berkeley actinic inspection tool.

Our presentation will detail the identity and quantity of the molecular contaminants and the impact of the contaminants on EUV reflectivity and feature printing. Further, we will quantify the impact of contamination on the lifetime of the mask and the efficiency of the cleaning protocols in removing the contaminants.

7636-17, Session 4

Lifetime of EUV optics with different capping layers under pulsed source

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Optics lifetime and contamination is one of the major challenges for extreme ultraviolet (EUV) lithography. In this paper we present several potential solutions towards an improvement of optics lifetime such as the selection and optimization of capping layers for oxidation protection, the mitigation of carbon growth and the development of efficient cleaning techniques that are soft to the multilayer surface.

Comparative lifetime studies of high-reflective Mo/Si multilayer mirrors (R > 67.0 %) with different capping layers (Ru, TiO2, Nb2O5) have been performed in various vacuum conditions (water/ethanol/other gases) at the new Exposure Test Stand (ETS) using a pulsed Xe-discharge EUV source at XTREME Technologies GmbH (Göttingen, Germany). The homogenous exposure of up to four samples with a large exposed area (> 35 mm2 on each sample) was suitable for a detailed study of degradation processes of multilayer mirrors by conventional characterization techniques. It was found that carbon growth and silicon oxidation are responsible for reflectivity losses of multilayer mirrors after low-dose EUV exposures (up to 15 J/mm2) in different vacuum conditions. The effect of the capping layer material, vacuum conditions and EUV-dose on optics lifetime will be discussed.

Radiation-induced carbon contamination and removal experiments on Ru-, TiO2- and Nb2O5- capped Mo/Si multilayer mirrors have been conducted at the ETS. Carbon contamination layers with thickness of > 5 nm were created by low-dose exposure (~ 5J/mm2) of the multilayer mirrors in different hydrocarbon atmospheres (tert-butyl-benzene with M = 134 or isobutene with M = 56). EUV exposure in different cleaning-gas atmospheres was used for the in-situ cleaning of contaminated multilayer mirrors. Additionally the stability of clean multilayer samples under cleaning conditions (EUV + cleaning-gas) was studied by exposure of uncontaminated multilayer mirrors to test the compatibility of the capping-layer materials with different cleaning procedures. The effect of the EUV-dose, the cleaning-gas, and the capping-layer material on the degradation and cleaning mechanism will be discussed.

7636-18, Session 5

Assessing EUV mask defectivity

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Mask defectivity is one of the main remaining challenges yet to be satisfactorily resolved before the implementation of EUV lithography in high volume manufacturing. Of the many types of mask defects, the critical ones are those that are printable on the wafer. To this end, this paper investigates wafer printability of well characterized reticle defects, with particular emphasis on those reticle defects that cause electrical errors on wafer test chips. The test reticles are equipped with test marks that are inspected in a die-to-die mode (using DUV inspection tool) and reviewed (using a SEM tool), and which also comprise electrically testable patterns. The test reticles have features with pitches smaller than 80 nm. In order to determine whether specific defects originate from the substrate, the multilayer film, the absorber stack, or from the patterning process, the reticles are inspected after each fabrication step. Following fabrication, the reticles are used to print wafers on a 0.25 NA full-field EUV exposure tool. The printed wafers are inspected with bright-field inspection tool; some of them are subsequently processed in a standard damascene process flow, before being tested electrically for short- or open-circuit conditions. Each electrically-testable cell is approximately 0.06 cm2. In our presentation, we will detail our defectivity assessment of the readiness of EUV masks for pilot line operation.

7636-19, Session 5

A study of defects on EUV mask using blank inspection, patterned mask inspection, and wafer inspection

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The availability of defect free masks remains one of the key challenges for inserting extreme ultraviolet lithography (EUVL) into high volume manufacturing. The successful production of defect free masks will depend on the timely development of defect inspection tools, including both mask-blank inspection tools, and also absorber pattern inspection tools to meet the 22-nm half-pitch node.

We have fabricated one full field EUV patterned mask in collaboration with a blank company and mask shop. The defectivity is characterized using a DUV blank inspection tool and a patterned mask defect inspection tool during mask fabrication. Exposures are done using the EUV ADT (Alpha Demo Tool) at CNSE in Albany. After exposure, the wafers are inspected with a wafer inspection tool at CNSE. The repeater defects found with the wafer inspection tool are related the defects on the mask. This information on repeater defects includes defects on the blank, absorber, and particles added during mask handling. This paper will present how to define the defects induced from the mask blank. The phase defect, which is not detected the patterned mask inspection tool, can be detected using this verification method.

Printability of real defects on the mask blank can be studied using the SEMATECH Berkely AIT(Actinic Inspection Tool) and AFM at SEMATECH. Our results show that there are various kinds of native defects on the mask blank. Not surprisingly, the surface height and measured EUV intensity profile of real blank defects can differ significantly from a Gaussian shaped defect. This makes printability predicted by defect printability simulation difficult. All defects found by the M7360 were observable in the AIT, yet many do not perturb the intensity enough to be printable in isolation. This paper will show various defect sizes and types, and clarifies what must be done to learn more about real defect printability to achieve the defect free mask blanks.

Our survey of defect printability simulations showed that most simulations have been based on a monochromatic assumption. However, stand alone sources for EUVL scanners will have a broad EUV spectrum. Owing to the wavelength-dependent appearance and printability of phase defects, this means that accurate simulations must include a wavelength range. This paper will summarize the simulation of defect printability considering broadband in EUV source, the three-dimensional effects, and resist parameters to find reasonable defect specifications. We will also report EUV imaging spanning a 3% wavelength bandwidth range using the AIT to emulate broadband effects in a stand alone source. This will show the reasonable defect specification and requirement on EUV mask blanks.

7636-20, Session 5

Impact of EUV mask absorber defect with pattern-roughness on lithographic images

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Extreme Ultraviolet Lithography (EUVL) is one of the most promising technologies in lithography for the fabrication of ULSI devices with 32nm half-pitch (HP) and beyond. Mask plays a key role and should be regarded as an integral part of a lithographic system. One of the requirements for EUV mask is high lithographic performance, such as higher image contrast, smaller shadowing effect caused by oblique illumination, low thermal expansion of substrate material, high flatness control, etc. We have been developing the high-lithographic-performance EUV mask. And in our previous papers we had demonstrated that by the thinning down of LR-TaBN absorbers with EUV light shield area, the shadowing effect could be reduced without any loss of printability.

On the other hand, one of the key issues with EUVL is to make defect-free masks. There are mainly three categories of mask defects: phase defects that are embedded within the multilayer blanks, absorber defects that are formed during the patterning of absorber, and particles that can result from mask handling. While it is important to identify the root cause of defects in order to realize defect-free masks, it is also necessary to set suitable specifications of mask defects for the production of ULSI devices. However, with conventional experimental procedure to investigate defect printability, it is difficult to measure critical defect size precisely because printed resist pattern's line-width-roughness (LWR) is still larger than the CD tolerance of 32nm HP and beyond.

In this paper, we investigate the defect printability of the thin absorber, high-lithographic-performance mask. In order to extract systematic component from printed resist pattern's LWR, we newly apply two kinds of procedures. One is usage of refined line-edge-roughness (LER) resist material and the other is CD averaging method of multiple exposure shots. And we estimate the systematic component originated from mask in the systematic LWR component by measuring mask pattern image. Finally, we will clarify the specification of the mask absorber defect from the measured systematic component of printed pattern and the measured image of programmed mask defect by comparing with lithography simulation results.

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7636-21, Session 5

Printability of EUV mask pattern defects for 22-40 nm half-pitch features

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Assessment of the printability of EUV mask pattern defects is critical for determining EUV mask patterning, defect metrology, and rework technology requirements. Printability of mask defects at the wafer level depends on defect size, defect shape, defect location, and the line width and pitch of the structure being printed. Earlier reports showed the relationship between the defect size on the mask and the printed critical dimension for 40-70 nm dense lines [1]. Improved optics and photoresists now enable assessment of mask pattern defect printability for 22-40 nm half-pitch features.

We report here the smallest mask pattern defects that printed at different locations in 22-40 nm structures using the Intel Micro-

Exposure Tool (MET). Various types of defects such as intrusions and extrusions were purposely incorporated into features on an EUV mask. The sizes of the patterned defects on the mask were drawn between 10-250 nm (= 2-50 nm on the wafer). The minimum printable defect size varied by as much as 100 nm, depending on the defect shape and location.

[1] T. Liang, G. Zhang, P. Naulleau, A. Myers, S. Park, A. Stivers and G. Vandentop, “EUV Mask Pattern Defect Printability” Proc. SPIE Vol. 6283, 62830K-1 (2006).

7636-22, Session 5

Particle removal challenges of EUV patterned masks for the sub-22-nm HP node

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EUVL is one of the main contenders for the sub-22 nm half-pitch node high volume manufacturing. In contrast to conventional optical masks, EUV patterned masks work in reflective mode. These masks have introduced new materials and surfaces that pose challenges to particle adhesion and cleaning. The process of fabricating an EUV mask includes deposition of 40 to 50 pairs of MoSi bilayers on top of an extra smooth low thermal expansion material (LTEM) substrate. Typically, the MoSi multilayer (ML) is capped by a 2.5 nm Ru layer. An absorber layer composed of Ta, N, B, and O, 50 to 70 nm thick, is coated on top of the capping layer. EUV masks are built by patterning this absorber layer. After patterning, surfaces exposed to chemicals during cleaning include TaN, TaNOB, CrN, LTEM, and Ru.

Cleaning challenges for these EUV masks include removal of 20 nm particles from 60 nm to 80 nm trenches without oxidizing the capping layer surface or damaging patterns.

The surface potential of absorber lines and the capping layer are modified by the presence of the MoSi underlayer. These modified surface potentials will lead to a modified double layer on the pattern surface. Compared to binary masks, which have Cr and quartz surfaces, the adhesion of typical particles to the surface and sidewalls of the absorber and capping layers is stronger. Therefore, particle removal from these surfaces requires overcoming stronger adhesion forces. The greater particle adhesion forces require larger fluid velocities for removal. However, due to the small feature sizes, slower fluid velocities are required to prevent damage, which makes particle removal a challenging problem.

This paper will present the results of our studies of removing 20 nm to 50 nm particles using different conventional chemistries in the presence or absence of megasonic agitation. SEM inspection will be used to show local particle removal, as illustrated in the figure above. The paper will also include adhesion force measurements of deposited particles and surfaces of interest for patterned EUV masks. Finally, our experimental work is accompanied by computational fluid dynamic (CFD) modeling of simple trenches and lines.

7636-23, Session 5

Removal of carbon and nanoparticles from lithographic materials by plasma-assisted cleaning by metastable atom neutralization (PACMAN)

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System cleanliness is a major issue facing the lithographic community as the prospects of integrating EUV lithography into integrated circuit manufacturing progress. Mask cleanliness, especially of particles in the sub-micron range, remains an issue for the implementation of EUV lithography since traditional mask cleaning processes are limited in their ability to remove nanometer scale contaminants. The result is lower wafer throughput due to errors in pattern transfer to the wafer from the particulate defects on the mask. Additionally, carbon contamination and growth on the collector optics due to energetic photon interactions degrade the mirror and shortens its functional life. Plasma cleaning of surfaces has been used for a variety of applications in the past, and now is being extended to cleaning surfaces for EUV, specifically the mask and collector optics, through a process developed in the Center for Plasma Material Interactions (CPMI) called Plasma Assisted Cleaning by Metastable Atom Neutralization (PACMAN). This process uses energetic neutral atoms (metastables) in addition to a high-density plasma (Te ~ 3 eV and ne ~ 10^(17) m^(-3)) to remove particles. The PACMAN process is a completely dry process and is carried out in a vacuum which makes it compatible with other EUV related processing steps. Experiments carried out on cleaning polystyrene latex (PSL) nanoparticles (30 nm to 500 nm) on silicon wafers, chrome coated mask blanks, and EUV mask blanks result in 100 % particle removal with a helium plasma and helium metastables. Removal rates greater than 20 nm/min have been achieved for PSL material. Similar removal rates have been achieved for the PACMAN cleaning of carbon from silicon wafers (simulating collector optic material) with 100% removal with helium plasma and helium metastables. The PACMAN cleaning technique has not caused any damage to the substrate type being cleaned either through roughening or surface sputtering. Current results of cleaning various particle types from surfaces through the PACMAN process will be presented in addition to an updated damage analysis.

7636-24, Session 6

Assessment of resist readiness for 22-hp EUV lithography

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The readiness of EUV materials is currently a high risk area according to assessments made at the 2008 EUVL Symposium. The main development issue regarding EUV resist performance has been how to simultaneously achieve high resolution, low line width roughness (LWR), and high sensitivity. In 2008, we demonstrated a 30nm HP L/S process with an Esize of 7.5mJ/cm2 and an LWR <4.0nm by developing an integrated materials solution package that combined the use of an acrylic polymer-bound PAG resist along with a tailored BARC and the use of a post-develop rinse agent.

In 2009, Intel has continued to use a parallel materials development approach incorporating both evolutionary and revolutionary materials to ensure that technically capable and commercially viable material solutions will be ready for EUV HVM insertion. This paper describes our strategy and the current status of EUV resist development at Intel Corporation. Data is presented utilizing Intel’s Micro-Exposure Tool (MET) and is focused on examining the feasibility of establishing a resist process that simultaneously exhibits ≤ 22 nm half-pitch (HP) L/S resolution at ≤ 12.5 mJ/cm2 with ≤ 4nm LWR. 22 nm hp pattern transfer on silicon through a hardmask (HM) will be presented.

7636-25, Session 6

Patterning with EUVL: the road to 22-nm node

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Extreme ultraviolet lithography (EUVL) is being developed to replace double patterning technology thus allowing patterning of fine features for high density memory device fabrication. Despite tremendous advances in EUVL, several issues related to the EUV source, mask, and resist must be overcome before this next generation lithography can be considered for high volume manufacturing (HVM). Resist development for EUVL is characterized using the Z factor that accounts for the RLS (Resolution, line-width roughness and sensitivity) tradeoffs. Most importantly, recent advances in resist development are mainly centered on the evolutionary approach wherein resist platforms of previous generation lithography are intuitively modified to suit the wavelength switch. In this approach, chemically amplified resist (CAR) wherein the catalytic generation of acid followed by multiple deprotection reaction cum acid generation during post-exposure bake is employed for meting

solubility switch to the resist. While this approach has been successful in KrF and ArF lithography, the very mechanism has been sounded as the death knell for EUVL patterning especially at dimensions below 20 nm. However, several key developments in the evolutionary approach point to the contrary. In this paper, we will present our recent data on EUV resist pattering using the resists developed by the evolutionary approach. Several key parameters involved in improving resolution viz., the resist platforms, polymer molecular weight, photo acid generator (PAG) size, PAG acidity and film thickness will be discussed. With the help of above studies we explore the potential of CARs for pattering features beyond 20 nm by intuitive modifications to account for the wavelength switch coupled with other changes involving EUVL.

7636-26, Session 6

Resist pattern prediction at EUV

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Accurate and flexible simulation methods may be used to further a researcher's understanding of how complex resist effects may influence the patterning of critical structures. In data of EUV resists, we have observed that, while base lithographic responses such as the exposure latitude of trench CD are about equal among samples of interest, corner rounding and the end-of-trench show much variability. The reason is unclear but may be related to the exposure mechanism of resist in EUV. At lambda = 13.5 nm, the acid generation mechanism is similar to that found in electron beam resists: acid generators are hypothesized to be activated by low energy electrons yielded by ionization of the resist matrix by high-energy EUV photons, suggesting that electrons may activate acid generators some distance from the absorption site. It is hypothesized that, depending upon the properties of a given EUV resist system, the initial condition of the exposed image-in-resist may differ from sample to sample, modifying some downstream behavior.

In this work, we attempt to gain insight into the causes of the observed differences between several EUV resists through the use of stochastic resist modeling and inductive reasoning. The model's parameterized fit to experimental data from several resists irradiated EUV will be shown and discussed. Resist pattern prediction using a well-characterized EUV mask will be discussed.

7636-27, Session 6

Development of resist material and process for hp 2x-nm devices using EUV lithography

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Extreme Ultra-Violet (EUV) lithography is the leading candidate for semiconductor manufacturing of the hp 22-nm technology node and beyond. Selete program covers the evaluation of manufacturability for EUV lithography process. Therefore we start to study the yield analysis of the hp 2x-nm test chip by full field exposure tool "EUV1". However, resist performance is still not achieved the stringent requirements for resolution limit, sensitivity and line edge roughness. To achieve the targets, Selete have evaluated more than 300 EUV resists from resist suppliers using the small field exposure tool (SFET) which is linked with a coater & developer track system under chemically controlled environments.

In the case of the resist process, the yield analysis of the hp32-nm test chip using the 3rd generation Selete Standard Resist (SSR3) was reported in SPIE Advanced Lithography 2009. (1) From this evaluation, we found that defect and pattern collapse might be critical issue for EUV lithography. (2) Defects by resist material and process are one of the causes of the lower yield. And the requirement of resist thickness is 80 nm for pattern transfer process of hp 32 nm test chip, however resist thickness have to be less than 50 nm because of pattern collapse in hp 2x nm test chip. It is necessary to prevent the pattern collapse with required thickness of resist film.

In this presentation, we will report the progress of development of resist materials and integration of resist process for the hp 2x nm devices. We will present the resist performance of next generation SSR. And we will discuss the resist process to prevent the pattern collapse and defect in addition to resolution limit, sensitivity and line edge roughness.

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(1) D. Kawamura et al., Proc. of SPIE Vol. 7273 (2009)72131O.

(2) H. Aoyama et al., Proc. of SPIE Vol. 7271 (2009) 727120-2.

7636-28, Session 6

Development of EUV resist for 22-nm half-pitch and beyond

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Extreme ultraviolet (EUV) lithography is one of the most promising candidates for next generation lithography (NGL), which can cover 22nmhp lithography and beyond. In order to implement EUV technology, resist is one of the critical items that will require significant improvements in overall performance. In order to achieve these improvements, many research groups are developing new materials such as molecular glass (MG), polymer bound photo-acid generator (PAG), high quantum yield PAG, sensitizer and high absorption resin. In this study, we focused on MG since its low grain size, monodispersity and high dissolution contrast have potential to break the resolution, line width roughness, sensitivity (RLS) trade-off. We have developed NORIA as our unique MG. We characterized its properties and advantages, which is mainly resolution, with EUV exposure. This achievement will contribute to the eventual utilization of EUV technology in mass production.

7636-29, Session 7

Improvement of total quality on EUV mask blanks toward volume production

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Extreme ultraviolet (EUV) lithography is a leading candidate for manufacturing semiconductor device at 22-nm half-pitch (hp) and beyond, and several devices have been developing and evaluating using EUV lithography toward future volume production. Defect-free EUV mask is one of critical challenges in implementing EUV lithography. An EUV blank with nearly zero defects over 25 nm is currently required for manufacturing defect free EUV mask. We have developed an EUV blank consisting of a Mo/Si multi-layer (ML) and a TaBN absorber. Beta type EUV blanks on glass substrates with low thermal expansion (LTE) have been supplying for alpha type exposure process since 2006. We have moved to next gamma program for upcoming preproduction development. We integrated newly pilot line for gamma type EUV blanks with present best infrastructures used in production of advanced photomask blanks. Our target in the program is to improve qualities such as defects and flatness on the EUV blanks, and to make practical specifications toward future production. Defect quality on the ML blanks is evaluated by M1350, M7360 and actinic inspection tool. M1350 and M7360 have 60 nm and 45 nm sensitivity, respectively. And actinic inspection tool made by Selete has high potential of 25 nm sensitivity. Defects on the ML blanks have been steadily reduced over 80 nm by improving substrate finishing and ML coating processes. Present ML blank defect is counted over 60 nm. Furthermore, we are focusing on reduction in smaller defects inspected by M7360 and actinic inspection. An LTE substrate with a flatness of less than 50 nm on both sides is required in EUV mask process without any flatness correction. In order to meet the demand, local polishing process has been developing. A flatness of around 50 nm would be available by local polishing process as routine. We are also challenging to attain lower blank bow and lower defects on the TaBN absorbers.

In this work, newly integrated pilot line for the EUV blanks will be introduced and recent quality on EUV blanks produced by the pilot line will be presented.

7636-30, Session 7

Mask inspection technologies for 22-nm HP and beyond

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Reticle quality and the capability to qualify a reticle are key issues for EUV Lithography. Current and planned optical tools will continue to provide inspection capability adequate for production of 2X HP masks, which we illustrate through application of 193nm-based inspection to advanced EUV patterned masks, including programmed defect masks. The influence of EUV absorber design for 193nm optical contrast and defect sensitivity will be identified for absorbers of current interest. For inspection of EUV masks at sub-22nm half-pitch, additional technologies must be considered, including actinic and electron-beam. We will summarize the latest results of our ongoing investigations into the leading technology options for EUV patterned mask inspection, as well as their development challenges.

7636-31, Session 7

E-beam correction methodology for compensation of mask nonflatness in EUVL pilot line

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There are many issues affecting the ability of Extreme Ultraviolet Lithography (EUVL) to meet the overlay performance specified by the International Technology Roadmap for Semiconductors (ITRS). One of the key components to the overlay budget is the contribution from the mask, and in EUVL that contribution is largely due to the impact of mask flatness variations in non-telecentric EUVL scanners. The mask non-flatness is impacted by blank polishing, uniform film stress (bow) and non-uniform film stress, and how the mask is held during the e-beam pattern writing step and during the actual lithographic scanning. For 22nm half-pitch manufacturing the overlay requirements indicate that mask non-flatness will need to decrease to 400nm bow and 23nm residual non-flatness, significantly impacting yield and cost-of-ownership.

SEMATECH is leading the industry in validating the nonflatness compensation strategy and to develop the methodology including building commercial EUVL masks and test overlay with wafer exposures. The main purpose is to develop the methodology for flatness compensation for EUVL pilot-line production. In addition, SEMATECH and NIST are working to improve the absolute flatness metrology capability. The substrate / blank flatness measurement technique for pilot-line will be discussed in this paper. We also present the results of using e-beam image placement corrections during mask writing to compensate for the bow and non-flatness of the masks. Models by finite element method and analytical calculation techniques were used to generate the predicted e-beam image placement corrections based on the mask non-flatness including modeled echuck contributions. A total of four masks will be analyzed using both non-corrected and corrected structures, with wafers exposed using the ASML alpha demo tool. A recommended e-beam correction methodology to compensate for mask non-flatness for EUVL pilot-line is presented based on the wafer printing results.

7636-32, Session 7

Lithographic performances of EUVL masks with various absorber thicknesses in alpha demo tool

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Extreme ultraviolet lithography (EUVL) is the most leading lithography technology for high volume production of sub-32-nm node devices. During the past two years, ASML alpha demo tools (ADT) have been in running and considerable exposure works including device applications and printability tests were performed. Moreover, EUV pre-production tools (PPT) with higher throughputs will come into operation in 2010. Hence, the age of EUVL in semiconductor industries is near at hand. Among the issues in EUVL, shadowing effect results in H-V bias on the printed images and it becomes worse with decreasing feature size. Therefore, new mask structure with thinner absorber stacks needs to be applied to 22 nm node and beyond. In the previous works with micro-field exposure tool (MET) and simulations [1,2], we demonstrated that EUVL masks with thinner absorber are advantageous in lithographic performances, especially in H-V bias reduction.

In this paper, we will present the results of an investigation of the dependence of mask absorber thickness on the wafer printability by using EUV ADT. For this purpose, we designed absorber stack structures and fabricated several full-field masks with various absorber thicknesses using commercial EUVL blanks. Variations on the absorber thickness have little effects on the minimum resolutions while H-V bias reduces by more than 60 % with thinner absorber structure. Thinner absorber structure also shows improved lithographic performances in mask error enhancement factor (MEEF), process window (PW), and line width roughness (LWR). A noticeable disadvantage in thin absorber mask is low optical density (OD) which results in CD reductions around shot border areas. To prevent this, we applied extra light shielding treatments on the mask process and obtained stable CD variations on the wafer images.

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7636-33, Session 7

Techniques for the removal of organic and inorganic contamination from both patterned- and back-side of the EUVL photomask

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Mask Defectivity is an acknowledged road block for the accelerated introduction of EUV lithography for manufacturing. Not only does the EUVL scanner environment (vacuum) dictate a new set of stringent requirements to surface cleanliness and purity for EUVL reticle front- and backsides, but the character of the EUVL photomask (material and structure) requires a different approach of surface preparation prior to cleaning, contamination removal and surface protection after cleaning (creating a hydrophobic mask surface, free of critical residuals). HamaTech APE, IMEC and Intel are evaluating a set of techniques for the removal of organic and inorganic contamination from both the patterned side as well as the backside of the EUVL photomask, ensuring maximum integrity of its capping and absorber layer. There are significant challenges to extend the conventional methods of cleaning - developed for standard 193nm optical photomask - to meet the specific requirements for EUV mask structure and materials.

The principal functionality of several cleaning steps is described, including a discussion of surface dehydration used in wet cleaning. Integrity of capping and absorber layer is verified through surface metrology. In addition to cleaning processes, the handling and

interfacing modules for EUV mask transfer among different tools (exposure, cleaning, inspection, storage) have not been developed to meet the anticipated cleanliness requirements for defect-free printing. With the first mask cleaning tool to be installed by a full-field EUV exposure tool, these issues can be evaluated. We will discuss the procedures and possible solutions.

7636-34, Session 7

Inspecting EUV mask blanks with a 193-nm inspection system

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Defect-free, multi-layer EUV mask blanks are a major challenge for EUV lithography. Although mask manufacturers have made significant progress in reducing defect density, there is still a gap between the current state-of-the-art and the lithography requirements. Key to making rapid progress is the availability of an inspection tool of high sensitvity and high speed. Using a 193-nm mask inspection system, we have detected small (<2 nm x 50 nm FWHM) phase defects on EUV mask blanks,. Detection sensitivity is good enough for mask blanks that will be used in producing 2X HP masks. The system with some modification has potential for greater sensitivity. We will report inspection results from masks with programmed defects and with natural defects, including defect densities and sizes. Using a currently available tool for inspecting EUV mask blanks enables rapid learning in EUV mask blank development.

7636-35, Session 8

Tin DPP source collector module (SoCoMo): status of Beta products and HVM developments

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For industrial EUV (extreme ultra-violet) lithography applications high power EUV light sources are needed at a central wavelength of 13.5 nm. Philips Extreme UV GmbH, EUVA and XTREME technologies GmbH have jointly developed tin DPP (Discharge Produced Plasma) source systems.

This paper focuses in the first part on the results from the Beta SoCoMo that can be used in the first pre-production scanner tools of the lithography equipment makers. The performance will be shown in terms of power at Intermediate Focus, dose stability and product reliability but also its reachable collector lifetime, the dominant factor for Cost of Operation.

In the second part of the paper the developments for the HVM phase are described. The basic engineering challenges in thermal scaling of the source and in debris mitigation can be proven to be solvable in practice based on the Beta implementation and related modeling calibrated with these designs. Further efficiency improvements required for the HVM phase will also be shown based on experiments. The further HVM roadmap can thus be realized as evolutionary steps from the Beta products.

7636-36, Session 8

Debris measurement at the intermediate focus of a laser-assisted discharge-produced plasma light source

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The goal of making extreme ultraviolet light lithography (EUVL) viable within the next few years relies on the ability to produce clean photons at the intermediate focus (IF). Creating enough EUV power does not deliver an appreciable cost of ownership (COO) if all devices down field of the source must be replaced due to degradation by an energetic flux. To investigate debris emanating from intermediate focus locations, the Center for Plasma-Material Interactions (CPMI) at the University of Illinois at Urbana-Champaign (UIUC) has developed a Sn intermediate focus flux emission detector (SNIFFED). This device consists of the following five detectors: dual quartz crystal microbalance (QCM), Faraday cup (FC), Si witness plates, microchannel plates (MCPs) with charged species mitigation capabilities, as well as a residual gas analyzer (RGA). With these five detectors, one is able to measure the presence of charged and neutral flux coming from the IF. The dual QCM allows deposition or erosion to be detected and affords a second look at what is observed on the Si witness plates. Lastly, an RGA allows the species that are transferred from the source chamber to the chambers beyond the IF to be diagnosed. In conjunction with the SNIFFED apparatus, CPMI has added a mock-up collector optic to the laser-assisted discharge-produced plasma (LADPP) unit located on site. Although it is simply a stainless steel two shell, one bounce setup, this mock-up collector optic simulates how debris is transported in true collector optics. Using the mock-up collector optic, the SNIFFED apparatus, as well as the LADPP, CPMI has investigated IF debris of a simulated LADPP setup. While operating the pinch source at 20 Hz and the laser source at 100 Hz, it was observed that debris travels slowly to the IF compared to line of sight measurements. This debris has been determined to mainly consist of debris mitigation gas (Ar) as well as pinch gas (N) that is present during the production of EUV; although Sn is used as the EUV source, it is not seen as a residual gas in the SNIFFED chamber due to the condensation of the electrode materials on the walls of the mock-up collector optic. Three mitigation schemes were analyzed: buffer gas flow rate, increases in chamber pressure, and secondary plasma created with 100 W of RF power. Increasing the flow rate of the buffer gas from 200 sccm to 1000 sccm increased the observed residual gas inside of the SNIFFED apparatus from a partial pressure of Ar of approximately 5x10-7 Torr to approximately 2x10-5 Torr. The only other predominant species besides background water vapor was N, which was maintained at a constant partial pressure of approximately 1x10-5 Torr. The addition of secondary plasma was found to increase the flux of energetic neutrals by an order of 70 times from 109 hits to as much as 7038 hits over a one-minute sampling. Increasing the buffer gas flow rate from 200 sccm to 1000 sccm increased the amount of debris observed by nearly a factor of 8 from 168 to 1378 hits per minute, although unlike the low buffer gas scenarios, nearly all of the arriving energetic species consisted of energetic charged particles. Increasing the pressure in the chamber from 2 mTorr to 20 mTorr (at 1000 sccm buffer gas flow rate) reduced the measured hits from 1378 to 192 hits per minute, or an 86 percent decrease. With the flow rate at 1000 sccm and at any observed pressure, charged species accounted for the majority of the species observed. This was in stark contrast with the entirely neutral composition of the sub-1000 sccm measurements. With the use of charge particle electrostatic debris mitigation (a 3kV potential drop across a 1cm gap between parallel plates), it was found that the arrival flux of energetic species could be reduced by nearly 97 percent from 817 to 19 hits per minute in the ideal case of 10 mTorr operating conditions with 1000 sccm Ar buffer gas and 100 sccm N pinch gas. Although no immediate method exists for determining the energy of these species with the current setup, it is known that the energy of these ions/neutrals must be above 500 eV, as that energy approaches the limit of the detector. The detailed results of these measurements will be presented in this paper.

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7636-37, Session 8

Angular distribution of debris from CO2 and YAG laser-produced tin plasmas

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Extreme Ultraviolet Lithography (EUVL) is one of the leading candidates in the development of smaller features for computer chips in near future. However, for EUVL to be applied to a high-volume manufacturing setting several issues must be addressed. One of these issues is the development of an efficient, reliable, and clean light source that emits strongly at 13.5 nm, the preferred wavelength for EUVL. Laser-produced tin plasmas have been shown to have a high Conversion Efficiency from laser energy to EUV radiation at 13.5 nm; however, effective debris management with laser produced plasma is a big concern. Typical debris in laser produced plasma are ions with varying charges and kinetic energies as well as neutrals, both of which pose a serious threat to the lifetime of an EUVL collector mirror. To protect the EUV collector optics, it is first necessary to have a good understanding of atomic and ionic particle flux and its angular distribution.

In this study, the properties of debris emission from CO2 (25 ns, 10.6 µm) and Nd:YAG (8ns, 1.06µm) laser-produced tin plasmas were investigated through several diagnostic techniques. The purpose of this experiment is to investigate the differences in the angular distributions of debris from plasmas generated by CO2 and Nd:YAG lasers. In order to compare the angular distributions of ionic debris from the plasmas, a faraday cup was placed at various angular positions throughout a stainless steel vacuum chamber. To investigate the characteristics of particulate debris emission, silicon witness plates were placed throughout the chamber and allowed to collect debris from the expanding plasma plumes. X-ray photoelectron spectroscopy and Atomic force microscopy were used for analyzing the witness plates. It was found that the debris emission from Nd:YAG laser-produced plasmas fell sharply from the target normal. In contrast, the debris emission from the carbon dioxide laser-produced plasmas was almost constant until 50 degrees away from the target normal. Furthermore, the debris coming from the carbon dioxide laser-produced plasma was considerably lower in quantity than the debris from the Nd:YAG laser-produced plasma for the conditions studied in these experiments.

7636-38, Session 8

Novel debris mitigation for collector life for LPP sources

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The manufacturing technology for the next generation semi-conductor devices will be based on extreme ultraviolet lithography (EUVL) using a laser produced plasma (LPP) as a candidate 13.5nm light source. EUV sources must be stable, energy efficient and meet the power requirements at intermediate focus. Additionally the plasma debris load must be minimized without compromising the radiation intensity. One challenge of EUVL is the development of a debris-free source that fulfills the required number of operating hours.

In the first part of the present work, the central challenge of debris mitigation for EUV sources is addressed in experiments conducted in the plasma science facility at ETH Zurich. The LPP is formed from the interaction of a Nd:YAG laser and tin target inside a spherical vacuum chamber of inside diameter 800 mm. The EUV intensity and average radiation fluxes can be simultaneously acquired in the facility. The time dependent EUV intensity is collected with a EUV power-meter and the integrated flux of the full spectrum with a pinhole spectrometer. A quadrupole mass spectrometer together with ion detectors are used to monitor target ions (Sn species) and to measure kinetic energy distributions. Within the vacuum chamber, due to the modular design of the facility a collector or a number of supports for witness plates can be installed; thus it is possible to characterize, in an angular-resolved manner, phenomena including LPP-surface interaction, debris deposition and heat loads.

The debris mitigation is based on a design that has been developed using ETH suite of multi-scale computational tools. Typical results using Direct Simulation Monte Carlo (DSMC) are shown in Fig. 1. The synergistic use of computations and experiments facilitates this work. First, in the computations a series of parametric studies are conducted; then in experiment, the most promising configurations are studied; then based on the results from experiments, the computational model are validated and applied for further designs.

In the second part of the present work, the thermal deformation of the collector is examined. This issue is of importance as with high loads, thermal deformation can result in imprecise focusing under operating condition. Thus, the spatial distribution of temperature for our cooled collector optic is measured. The impact of the debris mitigation on the integrated thermal load and the spatial distribution of temperature are also assessed.

7636-39, Session 9

Feasibility of EUVL thin absorber mask for minimization of mask shadowing effect

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Feasibility of EUVL thin absorber mask for minimization of mask shadowing effect

Conventional EVUL mask has 80nm absorber height which brings considerable shadowing effect. H-V CD bias of 40nm line and space by shadowing effect is more than 4nm, and that is expected to increase much more for narrower patterns by simulation.

However various reports have been presented on mask shadowing bias correction, experimental results are not reliable to derive required mask bias correctly. Even more difficulty will arise when complex 2D structures are taken into account. Therefore minimization of shadowing effect by reducing absorber thickness is desirable.

To transfer EUV lithography from experimental stage to HVM era, we need to find optimum absorber height of EUVL mask which allows us less shadowing effect with minimum loss of process window.

In this paper, we present optimal absorber height of EUV mask which has been found in terms of shadowing effect and process window by simulation and exposure. To find minimized absorber height experimentally, we will compare the printing result of conventional and thin mask stack using simple 1:1 line and space and island patterns. Simulated H-V CD bias and process window will be presented.

All the wafers are exposed at ASML Alpha Demo Tool, and EM-SUITE is used for simulation.

7636-40, Session 9

Full-chip correction of EUV design

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Extreme Ultraviolet Lithography (EUVL) is currently the most promising technology for advanced manufacturing nodes: it recently demonstrated the feasibility of 32nm and 22nm node devices, and pre-production tools are expected to be delivered by 2010. Generally speaking, EUVL is less in need of Optical Proximity Correction (OPC) as compared to 193nm lithography, and the feasibility studies for 32 and 22nm devices were indeed carried out with limited or no correction. However, a rigorous optical correction strategy and an appropriate Electronic Design Automation (EDA) infrastructure is critical to face the challenges of the 22nm node and beyond, and EUV-specific effects such as flare and shadowing have to be fully integrated in the correction flow and properly tested.

This study aims to assess in details the quality of a full chip optical correction for a EUV design, as well to discuss the available approaches to compensate for EUV-specific effects. Extensive data sets have been collected on the ASML EUV Alpha-Demo Tool (ADT) using the latest IMEC baseline resist Shinetsu SEVR59. In total about 1300 CD measurements at wafer level and 700 at mask level were used as input for model calibration and validation. The smallest feature size in the data set was 32nm. Both one-dimensional and two-dimensional structures through CD and pitch were measured. The mask used in this exercise permits to modulate flare by varying tiling densities within the range expected in the final design.

The OPC model was fit and validated against the CD data collected on the EUV ADT. The shadowing was modelled by means of a single

bias correction throughout the design. Horizontal and vertical features of different type through pitch and CD were used to calibrate the shadowing correction, and the extent of the validity of the single bias approach is discussed. In addition, the quality of the generated full-chip flare maps has been tested against experimental results, and the model has been validated in the full flare range available within the mask. The model calibration yielded an RMS of about 1nm, and a EUV mask fully corrected for OPC, flare and shadowing was finally fabricated and qualified.

7636-41, Session 9

Study of practical TAT reduction approaches for EUV flare correction

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Extreme Ultraviolet Lithography (EUVL) is the strongest candidate of lithography technique for 3X-nm-device and beyond manufacturing with single exposure. Because the amount of the flare is relatively large in EUVL, the flare compensation must be done through exact estimation of flare amount. It will take long time for the flare correction process by modifying mask pattern because of the large effective length of the flare and the large size of the mask pattern.

A point spread function of the flare (flare-PSF) is used for calculating flare map by convolving with the mask pattern. The calculation time of the convolution is the most dominant in whole calculation process because the effective length of the flare-PSF reaches to several millimeters. Effective methods of reduction of calculation time of the flare map are dividing a range of flare point spread function (PSF) into several regions and selecting proper size of the meshes in each region. In other words, a precise calculation with small meshes are implemented for the flare-PSF region near the position of calculating flare, and the flare is accounted a constant over a relatively large size of a mesh for the far region.

By adopting the above consideration, because the mask pattern consist of the several same chips, the precise flare correction is done for only one chip and the result for one chip can be used for whole mask with modifying by referring the chip position in the mask. The correction of one-chip mask pattern corresponding to the flare map can be performed in OPC and MDP process with model-based calculation. The whole mask-level correction can be rule-based modifying pattern in MDP or OPC process and the time of flare correction can be reduced for whole mask-level. Other mask-level and wafer-level correction can be performed in EUV mask pattern fabrication process and wafer exposing process, respectively. In these processes, the flare map with relatively large size of the mesh can be used around 100 micrometers, while the size of the mesh in the one-chip-level flare map may be 1 micrometer or below. In the compensation in the EUV mask fabrication process, a mask-writer controls exposure dose in the position in the mask according to the flare map. In the compensation in the wafer exposure process, EUV exposure tool controls exposure dose in the position in the wafer according to the flare map, and the exposure tool may be expected that the dose can be modulated according to the position in the shot. These techniques can reduce the time of flare correction by modifying mask pattern. Especially, in the wafer exposure compensation, the accuracy of the flare compensation is expected to be higher with the flexibility for the layout of shot in the wafer.

It is effective for TAT reduction and higher accuracy of the flare compensation that those approaches are used in proper combination.

7636-42, Session 9

MOSAIC: revisited, reformulated, and NA independent

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As extreme ultraviolet (EUV) lithographic systems are scaled to numerical apertures (NAs) of 0.5 and beyond, it is critical to develop reliable and accurate metrologies that work in this regime. Lateral shearing interferometry (LSI) is currently the trusted method for characterizing 0.25 NA and 0.3 NA EUV lithographic systems [1]; however, LSI alignment tolerances scale with the NA, making its implementation increasingly more difficult as NA increases [2]. While print-based methods [3-4] are attractive alternatives to coherent metrologies, the majority of these tests are currently inhibited at EUV because of their reliance on diffraction-limited resist performance.

Recently a new print-based aberration monitor was proposed that enables complete aberration characterization at 0.5 NA without diffraction-limited patterning [5]. Called MOSAIC, the method images features that probe local regions of the optic and measures how focus varies with the probe point. In other words, it maps out the local focal length of an imaging system throughout its pupil. In this paper MOSAIC is reformulated to enable the aberrations to be recovered on a sphere instead of the plane. This new approach mitigates all NA dependence and greatly simplifies the mathematical formulas involved. Following a sensitivity analysis that identifies the optimal object and illumination settings, a model-based proof of principle recovers the aberrations of the SEMATECH Berkeley 0.3 NA Microfield Exposure Tool with 4.2% RMS error: an error 4X smaller than the reported errors of the original LSI measurement [1]. This work was supported by the Director, Office of Science, of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231.

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7636-43, Session 9

EUV flare correction for the hp-22-nm node

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Extreme ultraviolet lithography (EUVL) is one of the most promising candidates for the next-generation lithography. For the adoption of EUVL, however, there are some technological problems to be solved. One of the critical issues is flare which is an undesirable scattered light that reduces the aerial image contrast leading to a reduction in the process window such as exposure latitude. Therefore, methods to compensate for anticipated flare effect are required.

At Selete, correction for flare based on a flare point-spread function (PSF) is investigated. We divide a layout into a grid and calculate pattern density for each grid square, obtaining a density array as an approximation to the layout aerial image. Then, the density array is convolved with the PSF to create an array of flare values. Using this flare-value array, we resize the layout.

In the above correction flow, size of a grid square of density array and a selection of an approximate function of the PSF have a great influence on the accuracy of flare value computation. In our previous work, we ensured high accuracy in flare correction for half-pitch (hp) 32-nm node masks using 0.75-um grid size and a multifractal approximation of the PSF. We succeeded in achieving a CD control of within a few nm over various pattern densities.

However, our estimation shows that the previous flare correction scheme cannot meet accuracy criteria of flare computation for the hp 22-nm node. Therefore, we have modified the flare correction flow to implement variable gridding both for pattern-density calculation and a convolution of the density with the PSF. The variable gridding based on a shape of the PSF enables highly accurate flare calculation in practical runtime.

Furthermore, even high k1 EUVL requires model-based OPC for the hp 22-nm node because of tighter CD control requirements. So we have incorporated flare correction into model-based OPC. In this work, we report on experimental and theoretical results on the availability of model-based OPC including flare correction.

7636-44, Session 9

Physical resist models and their calibration: their readiness for accurate EUV lithography simulation

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Extreme Ultraviolet Lithography (EUVL) is seen as one of the main contender for the patterning of the 22 nm technology node. Historically, rigorous physical models have been proven very powerful in the fields of EUV modeling. Although the build-up of EUVL infrastructure is progressing steadily, the tool time available to lithographers to perform experiments is still limited. Therefore, an accurate and predictive physical resist model is very important to enable reliable studies in an early pre-production stage. Typically, predictability has to cover a wide range of mask features, including both 1D and 2D structures, such as contact holes or end of lines (EOL). EUV-specific effects such flare, 3D mask shadowing and H-V bias need to be included as well. Moreover, the quest for a well performing EUV resist is accompanied by a large number of possible EUV resist candidates, each of them requiring a well calibrated model. Therefore, from a practical point of view it is important that the resist calibration process must be sufficiently fast and straightforward, yielding accurate predictive models. Ideally, the predictability does not only apply for CD values, but it should also include resist profile information such as resist loss and side wall angle.

In this paper, we discuss the performance of EUV resist models in terms of predictive accuracy and we assess the readiness of the corresponding model calibration methodology. The study is done on an extensive OPC data set collected at IMEC for the ShinEtsu resist SEVR-59 on the ASML EUV Alpha Demo Tool (ADT) including more than thousand CDs. We address practical aspects such as the speed of calibration and selection of calibration patterns. The model is calibrated on 12 process windows varying in pattern width (32, 36, 40 nm), orientation (H, V) and pitch (dense, isolated). The minimum measured feature size at nominal process condition is a 32 nm CD at a dense pitch of 64 nm. Mask metrology is applied to verify and eventually correct nominal width of drawn CD. Cross-sectional SEM information is included in the calibration to tune the simulated resist loss and sidewall angle. The achieved calibration RMS is well below 1.5 nm. We show what elements are important to obtain a well calibrated model. We discuss the 3D mask effects for the Bossung tilt. We demonstrate that a correct description of the flare level during the calibration is important to achieve a high predictability at various flare conditions. Although the model calibration is performed on a limited subset of the measurement data (one dimensional structures only), its accuracy is validated based on a large number of OPC patterns (at nominal dose and focus conditions) not included in the calibration; validation RMS results as small as 2 nm can be reached. Furthermore, we study its extendibility to two-dimensional EOL structures.

7636-45, Session 10

Actinic imaging of native and programmed defects on a full-field mask

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Mask defectivity is one of the main issues for advanced lithography in any future technology node. This is especially true for extreme ultraviolet (EUV) lithography where the mask, the absorber pattern, and the various types of defects can have wavelength-specific optical properties. Developing a reliable and accurate method for defect inspection and imaging is an essential step towards the deployment of EUV lithography.

While deep ultraviolet (DUV) microscopy and scanning electron microscopy (SEM) provide valuable information at high resolutions, their sensitivity to defects can be remarkably different from EUV-wavelength imaging-they cannot guarantee measurements that predict EUV printing performance. Our research shows that some defects that are strongly evident in an SEM will not actually print, while others, which are faintly detected with SEM or DUV inspection, can clearly appear on the wafer. Aside from printing in photoresist, EUV aerial imaging is the only technique that provides quantitative information on the interaction between the EUV light and the blank or patterned mask surface.

In this paper we describe the imaging of native and programmed defects on a full field EUV mask, carried out using actinic light (13.4-nm wavelength).

Following exposure in the ASML Alpha Demo Tool (ADT) at CNSE in Albany NY, an EUV reticle and its printed wafers were inspected using KLA tools. Defects were also investigated using SEM, and a classification system was developed that separated the defects into the following categories: cleaning residue, particle, pattern defect, blank defects, and nuisance defects1.

EUV imaging, performed with the SEMATECH Berkeley Actinic Inspection Tool (AIT), adds new information about the optical properties of these reticle defects. We observed that defects that appear opaque in the SEM can be highly transparent to EUV light, and inversely, defects that are mostly transparent to the SEM can be completely opaque (Fig. 1 A). The nature and composition of these defects, whether they appear on the top surface, within the multilayer coating, or on the substrate as buried bumps or pits, influences both their significance when printed, and their detectability with the available techniques (Fig. 1 B).

Moreover, by the study of the through focus evolution of a defect's aerial image, and from a comparison with simulated data, it is possible to investigate physical characteristics, such as the apparent height and the three-dimensional profile, and to discriminate between absorber and phase defects. While absorber defects are somewhat easier to identify, some of the defects that we have investigated show a behavior that is characteristic of buried phase defects (Fig. 2).

We will present a characterization of several defects with multiple inspection techniques, including the through-focus EUV imaging; we discuss their nature, printability and detectability.

[1] EUVL reticle defectivity evaluation A. Tchikoulaeva, U. Okoroanyanwu, O. Wood, B. LaFontaine, C. Holfeld, S. Kini, M. Peikert, C. Boye, C.-S. Koay, K. Petrillo, and H. Mizuno, Proc. SPIE 7271, 727117 (2009), DOI:10.1117/12.815525

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7636-46, Session 10

Printability and inspectability study with substrate programmed pit defects at EUV lithography

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One of the big concerns for the launch of EUVL is the minimum size of blank defect which can be printed on the wafer, known as phase defect printability. Among the defect types in EUV mask blanks, pits are the most dominant ones. Thus, it is very important to decide the boundaries between printable and non-printable, as well as inspectable and non-inspectable, criteria of the pit defects.

In this paper, we will show the results of an investigation of the effects of Mo/Si multilayer depositions on the EUV printability and DUV inspectability of substrate pits. For this purpose, programmed pit defects with various sizes are fabricated on the Qz 6025 substrates and Mo/Si multilayers are grown on them. Then, AFM, LBNL actinic inspection tool (AIT), Lasertec M7360, and ASML alpha demo tool (ADT) are used to analyze their dimension, inspectability, and printability. During multilayer deposition, depth and size of pits become smaller by smoothing effects and the degree of smoothing

depends on both original pit size and incident angles of deposition flux. Consequently, we systematically compare the behaviors of phase defects on the mask blank, on the patterned mask, and on the wafer by using M7360, AIT, and ADT, respectively. These results are essential since they can suggest the criteria of defects which we have to focus on.

7636-47, Session 10

Actinic review of EUV masks

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Management of mask defects is a major challenge for the introduction of EUV for HVM production. Once a defect has been detected, its printing impact needs to be predicted. Potentially the defect requires some repair, the success of which needs to be proven.

This defect review has to be done with an actinic inspection system that matches the imaging conditions of an EUV scanner.

During recent years, several concepts for such an aerial image metrology system (AIMS) have been proposed. However, until now no commercial solution exists.

Today, advances in EUV optics technology allow envisioning a solution that has been discarded before as unrealistic.

We present this concept and its technical cornerstones.

While the power requirement for the EUV source is less demanding than for HVM lithography tools, radiance, floor space, and stability are the main criteria for source selection.

The requirement to emulate several generations of EUV scanners demands a large flexibility for the ilumination and imaging systems.

New critical specifications to the EUV mirrors in the projection microscope can be satisfied using our expertise from lithographic mirrors.

In summary, an EUV AIMS meeting production requirements seems to be feasible.

7636-48, Session 10

An inspection and defect review strategy for EUV pilot line and high-volume manufacturing

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One key dependency for EUV pilot line and high volume manufacturing (HVM) implementation in 2011 and 2013, respectively, is the availability of “defect-free” masks. This cannot be achieved without the ability to find and disposition defects for mask process development and qualification. SEMATECH has been leading an industry effort among key EUV stakeholders representing semiconductor manufacturers, consortia, equipment suppliers, and mask makers to assess how far current blank/mask inspection and review technology can be extended and to reach an industry consensus on a mask infrastructure technology and tooling strategy that will support EUV HVM implementation by 2013. This paper will present the summary, conclusions, and an inspection technology roadmap for blank/mask inspection and defect disposition to ensure the introduction of EUV pilot line in 2011 and HVM in 2013.

7636-49, Session 10

The analysis of EUV mask defectivity using a wafer defect inspection system

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EUVL is the strongest candidate for sub-20nm lithography solution after immersion DPT. There are still critical challenges on EUVL to become mature technology like today litho workhorse as ArF immersion. Source power and stability, resist resolution and LWR, mask defect control and mask infra structure building are listed as top issues to be focused. Source power showed reasonably good progress during last 2 years. Resist resolution was proved to resolve HP 32nm with good process windows even though there is still concerns on LWR. However defect control level of blank mask is still 3 orders higher than requirement as of today.

In this paper, mask defect control using wafer inspection system is studied as alternative solution for reducing gap of mask phase defect detection. In previous study, the requirement of better sensitivity with EUVL patterning is required because of smaller defect size printing. To improve the defect detection capability, not only inspection system but also wafer side preparation is crucial. Few parameters on wafer like LWR, wafer stack, wafer noise are investigated to enhance the capture rate on after development and after cleaning inspection. In addition to defect sensitivity overall defect control methodology will be suggested among mask, mask inspection, wafer print and wafer inspection.

7636-50, Session 10

Evaluation results of a new EUV reticle pod based on SEMI E152

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In 2004, Canon and Nikon jointly proposed a new pod concept for EUV reticles, “Dual Pod Cencept”; a mask is doubly protected by an inner pod and an outer pod and the mask is carried into an exposure tool with the inner pod. Canon, Nikon and Entegris have started collaboration in 2005 and developed three types of EUV pod prototypes, alpha, beta and gamma. The gamma pods were evaluated by MIRAI-Selete and the superiority of the dual pod concept has been verified with many experimental data on shipping, storage and vacuum handling. The dual pod concept was standardized as SEMI E152-0709 “Mechanical Specification of EUV Pods for 150mm EUVL Reticles” in 2009. Canon, Nikon and Entegris have developed a new pod design compatible with SEMI E152; it has a type A inner baseplate for uses with EUV exposure tools. The baseplate has two alignment windows, a window for the data matrix symbol and five exclusion volumes for front edge grip. In addition to the new features, there are some differences between the new pod design and the former design “CNE-gamma”, e.g. the material of the inner cover was changed to metal to reduce outgassing and the gap between the reticle and the side supports were widened to satisfy a requirement of the standard. The new pod design can be used for both the next full-field EUV exposure tools by Canon and Nikon.

MIRAI-Selete has started shipping, storage and handling tests on the new CNE pods in the same way as the CNE-gamma pods. The initial data shows the new pods have good particle protecting capability comparable to gamma pods and a very lower outgassing rate than gamma pods. We will report the latest data at this conference.

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7636-61, Poster Session

Mitigation of carbon deposition on multilayer mirrors

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It is important to mitigate oxidation of multilayer mirrors (MLMs) and carbon deposition onto MLMs to extend the lifetime of EUVL exposure tool. In the EUVA (Extreme Ultraviolet Lithography System Development Association) program, capping materials are screened for their resistance to oxidation in order to mitigate oxidation of MLMs. On the other hand, dependence of carbon deposition on EUV intensity,

hydrocarbon partial pressure and other parameters were also obtained. For mitigating carbon deposition, materials with the least outgas must be used. Cleaning methods for etching deposited carbon, irradiating ultraviolet light with oxidation gas or injecting atomic hydrogen, is developed. Additionally, it is necessary to mitigate carbon deposition for longer time between cleaning. For example, when injecting decane gas of partial pressure of 2x10-7 Pa as outgas sample, the carbon deposition rate was 0.07nm/hr for EUV intensity of approximately 0.4 W/cm2. If maximum acceptable value of deposited carbon thickness is 1.5nm, uptime of EUV exposure tool would be is approximately 21 hrs using above carbon deposition rate. So mitigation of carbon deposition is very important for reducing downtime of EUVL exposure tool.

It is known that irradiating EUV light with injection of oxidation gas can clean up carbon contamination. There is a possibility that carbon deposition may be reduced when mixing oxidation gas to the hydrocarbon gas, which causes carbon deposition. In this paper, we report on the experimental results on mitigation method of carbon deposition.

A long undulator beamline in NewSUBARU synchrotron radiation facility at University of Hyogo was used for EUV light source. The maximum EUV intensity of the beamline is approximately 200 mW/mm2. Decane(C10H22) was used for injecting hydrocarbon gas. We measured carbon deposition on Si/Mo multilayer mirror after the EUV irradiation injecting decane and oxidation gas. Comparing the carbon depositions of only decane and decane with oxidation gas, we show the effect of carbon deposition mitigation. Furthermore, we will report on whether the carbon deposition rate of the mixture of decane and oxidation gas can be determined by linear combination of the deposition rate of decane and etching rate of oxidation gas.

7636-62, Poster Session

Multi-technique study of carbon contamination and cleaning of Mo/Si multilayer optics exposed to pulsed EUV radiation

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One of the unresolved issues on the road to a commercial application of extreme-ultraviolet lithography (EUVL) is the short lifetime of Mo/Si multilayer-coated projection optics. Numerous studies show that carbon growth and oxidation, induced by residual water and hydrocarbons in the projection chamber, are the main reasons for the reduced lifetime of projection optics that are exposed to EUV light. However, the majority of these studies were conducted with synchrotron radiation at very high intensities but with a rather small and inhomogeneous exposed sample-area. This makes the characterization of exposed samples with conventional surface science techniques very difficult and gives rise to ambiguous results. It is not yet clear if the results of these studies are applicable to the degradation mechanisms which occur at the projection optics of real exposure tools.

In this work comparative lifetime studies of Mo/Si multilayer mirrors with different capping layers (Ru, TiO2, Nb2O5) have been conducted at the new Exposure Test Stand (ETS) using a pulsed Xe-discharge EUV source at XTREME Technologies GmbH (Göttingen, Germany). This set-up allows for the homogeneous exposure of up to four samples. The base pressure in the exposure chamber is $\leq$ 10-8 mbar during exposure and a controlled inlet of hydrocarbons or cleaning-gases is possible for contamination and cleaning experiments. The large exposed area on each sample ($\geq$ 35 mm2) is suitable for a detailed multi-technique study of the degradation effects with standard surface science techniques: After each exposure EUV-reflectometry was applied to detect degradation or cleaning effects. XPS was used to measure the sample composition at exposed and unexposed parts of the multilayer mirrors and get a better understanding of degradation mechanisms. SAXR was applied as a relatively fast method to measure thickness and density of carbon contamination layers and control the stability of the samples. OOB-reflectometry (200 - 1000 nm) is very sensitive to carbon growth and was applied as a cheap and fast method to estimate the thickness of carbon contaminations. Finally, the roughness development on exposed multilayer mirror surfaces was controlled by AFM.

The exposure set-up and the multi-technique approach to sample characterization were applied to conduct a comparative lifetime study of Mo/Si multilayer mirrors with different capping-layers. The influence of the EUV-dose, the cleaning-gas pressure and composition, and the capping-layer material of the Mo/Si multilayer samples on the degradation and cleaning mechanism were investigated.

7636-63, Poster Session

Removal and prevention of surface contamination from EUV mirrors using low-power downstream plasma cleaning

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Carbon contamination on extreme ultraviolet (EUV) optics is a problem which must be solved in order for EUV lithography to become a productive tool for the semiconductor industry. This contamination lowers the reflectivity of EUV mirrors to below that needed for efficient photomask exposure. Breaking vacuum, removing and then cleaning mirrors by hand is a time-consuming and expensive method for dealing with the problem. A safe yet effective in situ method for cleaning EUV optics and maintaining vacuum chamber cleanliness is important for progress in EUV lithography.

The issue of carbon contamination is also important for imaging in scanning electron microscopes (SEMs). Electron beam induced contamination can lead to poor image quality and non-repeatable measurement in SEMs. However, as presented at a NIST Workshop on EUV contamination in June 2009, the problem of contamination in SEMs has been solved by using low-power downstream plasma cleaning. A small radio frequency (RF) plasma device can be attached to an open port of an SEM chamber. The cleaning process works by passing a small stream of oxygen containing gas through low power RF plasma. The plasma dissociates oxygen molecules into neutral oxygen radicals. These radicals flow throughout the SEM vacuum chamber and chemically remove the carbon contamination. The products of the removal process are CO2, CO and H2O, which are pumped out of the SEM vacuum chamber. Since the process works by chemical etch and not by sputter etch, oxide layers such as those found on sensitive detector windows in SEM chambers and those found as caps on EUV mirrors will not be damaged by the cleaning process.

The efficacy of the downstream plasma cleaner can be demonstrated by using quartz crystal microbalances (QCMs). A silver coated QCM is placed in a vacuum chamber with the downstream plasma cleaner. Oxygen radicals create a layer of silver oxide on the QCM, which increases the thickness of the QCM. The rate of thickness growth is related to the concentration of oxygen radicals at the QCM surface. Oxygen radical fluxes up to1.3x1015 radicals cm-2 s-1 have been measured 20 cm from the device at 10 W RF power. Alternatively, a gold coated QCM can be contaminated with hydrocarbons or graphite and placed in a vacuum chamber with the downstream plasma cleaner. When the process is started, the contamination is removed and a thickness loss rate is measured by the QCM. At 17 W RF power thickness loss rates of ~1 nm minute-1 have been recorded.

This process will be repeatedly tested with mirrors contaminated during the operation of the EUV Lithography Tool at Lawrence Berkeley Laboratory. Contaminated EUV mirrors will be removed from the tool and cleaned in a separate test chamber. The EUV reflectivity of the mirrors will be measured before and after the downstream plasma cleaning to determine the effectiveness of the method.

7636-64, Poster Session

Characterization of contamination on the illumination optics of the SEMATECH extreme-ultraviolet micro-field exposure tool

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The SEMATECH micro-field exposure tool at Albany, NY, plays a critical role in the development of resist materials for extreme ultraviolet lithography. The illumination optics on the tool is composed of two grazing-incidence and two normal-incidence mirrors. The reflectivity of these mirrors degrades over time due to the formation of a carbonaceous layer on top of their surfaces. Angle-resolved, at-wavelength reflectivity and spectroscopic ellipsometry measurements of the mirrors was performed to determine the thickness and density of the carbonaceous layer. The elemental composition of the contamination layer was examined by X-ray photoelectron spectroscopy. To understand whether the contaminated mirrors could be reclaimed different types of cleaning approaches were employed, followed by post-cleaning characterization of the optics.

7636-65, Poster Session

Determining the binding energy of contaminating molecules on capping layer materials of extreme-ultraviolet optics by density functional theory

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Under extreme ultraviolet (EUV) radiation exposure, carbonization and oxidation are the two main mechanisms that degrade the reflectivity of EUV multilayer optics in the vacuum environment of exposure tools. The accumulation of carbon on the mirror surface is a consequence of residual hydrocarbons, while oxidation results from water vapor. One of the reasons that theoretical and numerical models of EUV optics contamination lack predictive quality is that the values of model parameters such as binding energies of contaminating molecules on the surface, reaction cross-sections, etc., are not accurately known. The work presented here focuses on determining the binding energy of various contaminating molecules by density functional theory calculations. Clean Ru (0001) and TiO_2 (110) surfaces were considered in the study due to their widespread use of Ru and TiO_2 as capping layer materials. The sites where carbon atoms typically attach on these surfaces were determined by generating potential energy surfaces. Further accumulation of carbon over time will change the nature of the interaction between the surface and the contaminants. The change in the binding energy of the contaminating molecules is thus determined due to the addition of graphitic-type carbon monolayers as opposed to a clean capping layer material.

7636-66, Poster Session

Modeling carbonization of extreme-ultraviolet optics

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The carbonization of extreme ultraviolet optic surfaces leads to a decrease in the reflectivity of mirrors. Understanding of the involved processes that lead to carbonization is far from complete, posing a challenge in modeling such interactions. We report on the progress made by SEMATECH in this field. A model developed by SEMATECH is able to predict the linear and non-linear dependence of contamination rates on the residual hydrocarbon partial pressure. The modeled results are compared with and found to be in close agreement with experiments performed by NIST for benzene and methyl methacrylate as contamination molecules on TiO_2 surfaces[1]. In addition, the model was extended to take into account the presence of more than one contaminant.

1 Hill et al., Proc. of SPIE, Vol. 7271, 727113, 2009

7636-67, Poster Session

Contamination study on EUV exposure tools using SAGA light source (SLS)

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Contamination control of optics is one of the critical issues for EUV lithography. EUV irradiation with residual hydrocarbon gas causes carbon-contamination growth on the surface of mirrors. EUV irradiation in the oxidizing environment including water vapor or oxygen causes oxidation of the surface of mirrors. These contamination issues degrade transmittance of optics and then reduce the throughput of exposure tools. Non uniform contamination growth on the surface of mirrors may affect the imaging performance of the optics.

We have been conducted R&D on such contamination issues using SBL2 at Super ALIS synchrotron facility at NTT Atsugi and BL9 at New Subaru synchrotron facility at University of Hyogo. Typical irradiances on test samples are 2.4W/cm2 and 25W/cm2, respectively. BL9 at New Subaru is an undulator beam line, which gives high photon flux. These beam lines are common facilities, so that we could not have enough machine time for our research. Therefore, we have constructed a new dedicated beam line (BL18) for R&D on contamination issues at Saga Light Source (SLS) synchrotron facility. Typical irradiance on test samples is 9W/cm2. We can take advantage of long-time exposure of BL18 at SLS. As an example, Figure 1 shows the change of reflectivity of Ru-capped Mo/Si multilayer mirrors irradiated with EUV radiation in the water vapor environment. Data obtained at New Subaru with high-irradiance and short-time exposure are also shown in the figure for comparison. Measurement error of the data at SLS was much smaller than the data at New Subaru. More accurate experiments are available by using BL18 at SLS.

Carbon-contamination growth under low irradiance condition was examined using BL18 at SLS. Mo/Si multilayer mirror samples were irradiated with EUV radiation while 5x10-5Pa of hydrocarbon gas was introduced. Irradiance on test samples was changed from 1W/cm2 to 0.01W/cm2 by using neutral density filters. We found that the degradation rate of reflectivity hardly depends on the irradiance. Degradation was almost proportional to the exposure time. Degradation rate was almost the same for different irradiance. In these conditions, the supply of photons is enough and degradation ratio is subject to the supply of contaminants. Based on these data, we can improve our theoretical modeling for contamination growth.

We have also been conducting the investigation on carbon contamination caused by outgas from resist. Mo/Si multilayer mirror samples were exposed with EUV radiation. A resist-coated Si tip was placed in front of the multilayer mirror, which reflects the EUV radiation on to the resist. Degradation of reflectivity during exposure was observed. Pressure rise during exposure was little. We have confirmed that very small amount of outgas from resist can cause carbon contamination growth.

A part of this work was supported by NEDO.

7636-68, Poster Session

The analysis of carbon contamination of EUV mask using CSM

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Extreme ultra violet lithography (EUVL) using 13.5nm wavelength is expected to be the mainstream of production process for 22nm half pitch and below. Carbon contamination on the mask is one of the critical issues to be solved for the commercialization of EUVL. The reflectivity of the Mo/Si multilayer masks decreases with carbon film deposition. This results in a reduction of throughput and deterioration of critical dimension (CD) uniformity.

In this paper, we analyze the impact of carbon contamination on the imaging performance using the accelerated contamination system combined with coherent scattering microscopy (CSM) which has been installed at Pohang Accelerator Laboratory. CSM has been proposed as an actinic inspection technique, which records the coherent diffraction pattern from the EUV mask and reconstructs its aerial image using a phase retrieval algorithm. The influence of carbon contamination on the imaging properties including image contrast, pupil density ratio, and CD change were obtained using CSM. These imaging properties were compared with calculated results using EM-SUITE simulation tool. The effect of phase shift and reflectivity depending on carbon film density and thickness were also calculated. In addition, strategies for carbon contamination mitigation will be discussed.

7636-69, Poster Session

Characterization of EUV-optics contamination due to photoresist-related outgassing

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Outgassing of photoresist material and the related risk for optics contamination in extreme ultraviolet (EUV) exposure tools are concerns in the development of EUV lithography, especially towards the high volume manufacturing tools. The characterization however of which resist species are important for the contamination, and their quantification, is still very challenging. Currently various techniques are explored worldwide, but there is still no full consensus on which technique is most adequate. On one hand, investigation is done by measuring only the resist outgassing by residual gas analysis (RGA), pressure rise or other related analysis techniques. Challenges in this field are the accurate determination of the quantity amongst all experimental set-ups, the identification of the outgassing in terms of chemical species, and - last but not least - its relationship to mirror contamination. Another investigation approach is focusing on the measurement of EUV optics contamination by analyzing the contamination generated on a witness sample which is exposed in the vicinity of resist outgassing. Although this approach requires a more complex experimental set-up (both resist and witness sample need to be exposed), and a more complex metrology for contamination analysis, this technique has the main advantage that the test result, i.e. the contamination on the witness sample, is directly related to the concern in the EUV lithography tools.

In this paper, we have focused mainly on the witness sample approach as a possible candidate for photoresist qualification. Contamination results obtained at ASML's and IMEC's test equipment are compared, which enables better understanding of the parameters that can affect the resist related contamination growth, and which helps to differentiate this from the contamination generated from the test tool background outgassing. Moreover, the contamination generated on the witness samples is characterized in detail towards thickness as well as composition, by using various material analysis techniques. Finally the contamination behavior is compared to the RGA resist outgassing information for better understanding of the over-all issue. In this way it should be possible to quantify what risk is involved with using a photoresist material in high volume manufacturing exposure tools, and how to qualify this with a simple but adequate test method.

7636-70, Poster Session

Wavelength dependence of carbon contamination on mirrors with different capping layers

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Optics contamination still remains one of the challenges of Extreme ultraviolet (EUV) lithography. In addition to the desired wavelength near 13.5 nm (EUV), sources used in EUV exposure tools emit a wide range of out of band (OOB) wavelengths extending out to the visible region. In the past, preliminary studies have shown that the contamination rate due to OOB is up to 20 times more than that of EUV. To that effect, we built a flat field spectrometer to study in detail the wavelength dependence of carbon contamination. We present experimental results of contamination rates for EUV and OOB using the custom-built spectrometer and a Xe plasma source. Heated carbon tape is used as a source of hydrocarbons in the vacuum chamber. We have measured the wavelength dependence of carbon contamination on a single layer mirror of Mo(2.9 nm)/Si(4 nm) deposited on a Si substrate with a Ru (2 nm) capping layer. We will compare these results for TiO_2 and ZrO_2 capping layers.

The mirrors were exposed with a known wavelength of light while the carbon tape is heated. The intensity of the light is measured, on the sample plane, with a calibrated photodiode before and after each exposure. The carbon thickness on the exposed mirrors was measured using XPS.

Moreover, using a deuterium arc lamp, we present contamination results for 190 nm and higher wavelengths.

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7636-71, Poster Session

Analysis and characterization of contamination in EUV reticles

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A host of complementary imaging techniques (optical photography, scanning electron microscopy), surface analytical technique (Auger electron spectroscopy), chemical analytical and speciation techniques (grazing incidence reflection Fourier transform infra-red spectroscopy and Raman spectroscopy) have been used to analyze and characterize the contamination on three EUV reticles that were contaminated to varying degrees. Two of the reticles were contaminated as a result of their exposure experience on the SEMATECH EUV Micro Exposure Tool at Lawrence Berkeley National Laboratories, while the third reticle was intentionally contaminated with hydrocarbons in the Microscope for Mask Imaging and Contamination Studies (MIMICS) tool at the State University of New York at Albany. Following the contamination experiments, which in some cases spanned more than one year, the reticles were cleaned at Advanced Mask Technology Center (AMTC) in Dresden and their EUV reflectivities were measured on the Actinic Inspection Tool at Lawrence Berkeley National Laboratories. In this presentation we will discuss our assessment of the relative strengths and weaknesses of the indicated techniques in analyzing and characterizing EUV reticle contamination, the impact of reticle contamination on EUV printing, on EUV reflectivity, as well as on EUV reticle lifetime.

7636-131, Poster Session

A simple Null-field Ellipsometric Imaging System (NEIS) for in situ monitoring of EUV-induced deposition on EUV optics

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In pre-production extreme-ultraviolet (EUV) lithography systems, carbon contamination of the illumination and projection optics is one

of the primary sources of throughput loss. To address the problem of such EUV-induced contamination, a program was established at the Synchrotron Ultraviolet Radiation Facility (SURF III) of the National Institute of Standards and Technology (NIST) to measure the contamination rates and scaling behavior of various organic species that are likely to be found in the tool vacuum environment of an EUV lithography tool. Previously, samples were exposed to a defined dose of EUV in fixed partial pressures of various admitted gases and then removed from the vacuum for characterization with ex-situ XPS and spectroscopic ellipsometry. This approach has worked well for studies of pressure and intensity scaling. However, the speed and breadth of experiments would be greatly improved with in-situ analysis, allowing real-time study of optic contamination and avoiding the possible influences of exposure to air before ex-situ analysis. Furthermore, since the intensity distribution of the EUV radiation on the sample is known, an in-situ measurement system with sufficient spatial resolution would permit simultaneous studies of the pressure, dose and intensity scaling of optic contamination.

To this end, we have recently constructed an in-situ imaging system to monitor carbon growth in real time based on single-wavelength null-field ellipsometry [1]. The current system uses a 635 nm diode laser coupled through a single mode fiber to an aspheric lens collimator as the source. The well collimated laser beam irradiates the sample at an incidence angle of 68 degrees and the reflected light is imaged with a CCD camera. The optical system is simple with only a thin film polarizer and a quarter-wave plate on an input arm constructed of modular components and, similarly, a polarizer/analyzer and CCD camera on the other. (See Figure 1.) The system is highly sensitive and capable of detecting sub nanometer deposits; a false color image of a deposition of ≈ 0.7 nm of carbon on a TiO_2-capped multilayer structure is shown in Figure 2. The system has a lateral spatial resolution better than 50 m which is more than sufficient to detect the variations in contamination with the spatial intensity distribution of the EUV exposure beam.

Thickness measurements of carbon on various samples that simulated capped multilayer mirrors were made by both Spectral Ellipsometry (SE) and with the NEIS. Since the optical properties of the substrate and the carbon deposition are known from earlier SE and XPS, the phase change between the P and S polarizations of the reflected beam (normally labeled delta) induced by the bare substrate and by carbon deposit of a given thickness on the substrate are known, and a measure of the difference between the delta of the substrate and the delta of the carbon deposit gives a value for the carbon thickness. The NEIS thickness values determined this way have thus far agreed to within 10% to those measured with the more sophisticated SE system.

7636-72, Poster Session

Deposition strategy to achieve near defect-free EUVL mask blanks

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Reducing mask blank defects remains a critical issue for the commercialization of EUV lithography. Ion beam sputter deposition (IBD) of Mo/Si multilayers (MLs) has been under continuous improvement since it first demonstrated ultralow defect density [1]. Despite much progress [2], the best reported mask blank defect density levels still greatly exceed the EUV roadmap requirements. Significant improvements are needed in both substrate quality and multilayer deposition. This paper will outline the strategy to achieve near defect-free deposition based on lessons derived from over 5 years of process and hardware optimization of the Veeco low defect deposition (LDD) system at the SEMATECH Mask Blank Development Center (MBDC) The key issues today include minimizing “decoration” effects resulting from defect nucleation during deposition [3], reducing particle contributions from the sputter targets and shields, and eliminating contamination in the transport of masks from the reticle pod to the process chamber. While some evolutionary improvements can still be made in the current LDD IBD system to achieve the near defect-free mask blanks needed for EUVL insertion, they will require several major equipment features that cannot be adequately realized by the current design. This includes the capability to uniformly coat masks at normal or near-normal incidence of the deposition flux to minimize particle decoration, full area ion beam erosion of the targets to reduce target generated defects without engendering harmful effects of beam overspill, and lastly the integration of an ultralow defect dual pod mask handling technology [4]. The conceptual design of such a system is already in progress.

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7636-73, Poster Session

Confirmation of EUV mask defect printability

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EUV lithography is one of the most suitable technique for halfpitch 22nm generation device manufacturing and beyond. But, there is not enough information about the printability of EUV-mask defect. EUV-mask defect has various characteristics (size, shape, material). EUV-mask defect include absorber defect, multi-layer defect and soft defect. The presence of such defects may prove harmful to EUVL, thus it is very important to confirm its printability.

In this paper, we will discuss about printability of EUV-mask defect. The main purpose is to compare the defect that was printed on the wafer due to EUV-mask defect.We will confirm about printability of EUV-mask defect using the following methods.

First, we will prepare test mask with L/S-pattern. This L/S-pattern has enough big areas.

After patterning process, it will be inspected with several kinds of inspection tools.

Inspection tools include die-die inspection tool for EUV-mask and blank inspection tool with EUV-wavelength. Highly sensitive inspection tools will detect various types

of real defect. Small size defect that was not detected with the conventional inspection tool will be detected. The defect that is detected by the inspection tools will be observed by CD-SEM or other tools. Above observation allow the specification of the defect size, defect shape and other defect information.

After identification of the EUV-mask defect information, we will carry out patterning of the wafer by EUV exposure tool. After patterning process the wafer will be inspected using a wafer inspection tool, and the defect will be specified. After that we will compare the EUV-mask defect information and wafer defect information, and estimate influence on transcription of the EUV-mask defect. This work is supported by New Energy and Industrial Technology Development Organization (NEDO).

7636-74, Poster Session

Holographic method for detecting amplitude and phase-shift errors (or features) in EUV ML reticle blanks

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Qualification of reticle blanks fabricated with absorbing and/or phase shift defects and/or features in the Multi-Layer (ML) on the thick mirror

substrate remains a key challenge for the implementation of extreme ultraviolet lithography (EUVL). A novel actinic method is proposed that enables the holographic recording of amplitude and phase variations in the out-going EUV beam after reflection due to the constructive interference in the ML stack of the reticle blank. It is anticipated that reticle blank phase and amplitude errors that cause printable defects in the EUV resist on a wafer will cause significant and detectable features in the EUV resist on the reticle as proposed in the present method. The holograph can then be inspected using existing reticle inspection methods, thus drastically reducing cost and risk.

The proposed novel inspection method "EDICT" comprises at least three of the following processing steps

E Exposure of the resist on the Multilayer on the optical element, e.g. a reticle or mirror designed for the actinic light, for example EUV having a wavelength between 9-15 nm

D Development of the exposed resist

I Inspection of the developed pattern using either existing (DUV and/or EUV) reticle inspection or wafer inspection infrastructure or a dedicated inspection tool

C Cleaning of the reticle to remove all traces of the resist and/or Curing of the phase errors with local modification methods such as e.g. e-beam exposure

T Test whether the reticle is indeed sufficiently cleaned and/or cured in step C.

The figure below illustrates the principle of recording the holographic image in the resist layer that is applied to the ML surface.

This paper presents the principle of the method and will quantify the sensitivity of the method for several types of defects / features.

7636-75, Poster Session

Compensation methods for buried defects in extreme-ultraviolet lithography masks

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Two methods will be presented to compensate for buried defects in extreme ultraviolet (EUV) masks with buried defects. The first method uses pre-calculated design graphs to determine the required absorber modification for a given defect. The second method attempts to engineer the spectrum transmitted by the absorber pattern to print the desired circuit pattern and to cancel out the spectrum reflected by the buried defect. Both methods require a fundamental understanding of the complex and non-spatially localized nature of buried EUV defects.

Buried defects are a major problem in EUV lithography because defects as small as 1nm tall on the multilayer surface near absorber lines can cause greater than 10% CD change for 32nm dense lines [1]. For smaller lines the allowable defect height will be even shorter. It may not be possible to reliably manufacturer EUV mask blanks without any defects larger than this limit so compensation could be necessary. Compensation for buried defects has been proposed before and experimental results show compensation should be possible [2]. The goal of the methods in this work is to prescribe modifications to the absorber pattern on the mask so that the final image printed on the wafer matches the intended pattern through focus.

The design graph method employs a simple two step algorithm: Determine the size of the critical dimension (CD) change due to the defect from an experimental aerial image of the mask or resist image, and then use previous simulation data represented in a design graph to choose the size of the modification to be made to the absorber near the defect. This analysis is done for negative focus because buried defects print worst for negative focus. For example, if a defect causes a -25% space CD change out of focus, a modification to the absorber should be made to reduce this change by 15% to -10%. The target CD change for the out of focus case is -10% because the space CD will be increased through focus.

Unfortunately, the simple design graph method does not work for all defects. Therefore a more complicated spectrum engineering method is being developed as well. This method attempts to create an absorber pattern which will cancel out the spectrum from the defect while still printing the desired pattern. This is difficult because the ideal compensated absorber pattern is often complex and has a transmission greater than one, while the actual pattern on the mask can only absorb light where there is absorber and reflect light where there is not. The key that makes this method possible is that not all of the light reflected from the mask enters the pupil. The effect on the orders outside of the pupil a modification to the absorber pattern will have is a degree of freedom that can be used to engineer the spectrum in the pupil to correctly compensate for the defect.

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7636-76, Poster Session

Stochastic simulation of photon scattering for EUV mask-defect inspection

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The photon propagation process in a multiple scattering medium has been modeled by Perelman et al. [1][2]. Energy transport in a multiple scattering medium is well treated by Feynman path integral [3]. A new insight of light propagation in a multiple scattering medium is explained by the most probable path taken by photons. The probabilistic process of the photon scattering is characterized by two parameters, the photon weight and the no-absorption photon path. Each interaction in a medium causes a photon to be scattered with a probability a and absorbed with a probability 1-a. The photon weight is reduced by a factor a, and the photon travels freely in a direction determined by the Gaussian phase function until its next interaction with the medium.

In this work, we utilize this modeling technique to calculate the number of reflective extreme-ultraviolet (EUV) photons scattered from mask surfaces. The reflective photons reveals information for both the mask structure and the mask defects. When EUV light is used to inspect mask defects, the number of reflective photons has to be enough for generating sufficient detector signals. Energy distribution in space can be obtained from the number of reflective EUV photons in different directions. We further investigate the minimum number of incident EUV photons needed for detecting mask defects with various sizes per unit mask area.

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7636-77, Poster Session

Particle protection capability of SEMI compliant EUV dual pod

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With the projected rollout of pre-production extreme ultraviolet lithography (EUVL) scanners in 2010, EUVL pilot line production will become a reality in wafer fabrication companies. Among EUVL infrastructure items that must be ready, EUV mask carriers remain critical. To keep non-pellicle EUV masks free from particle contamination, an EUV pod concept has been proposed. Early prototypes have been demonstrated with nearly particle-free results at 53 nm PSL equivalent inspection sensitivity during EUVL mask cycling, shipment, vacuum pump-purge, and storage. With the passage of SEMI E152, which specifies the EUV pod mechanical interfaces, standard-compliant EUV pods were built and tested. Their particle

protection capability results will be reported in this paper. Test results during vacuum operation will be included in this work as well as the results of several customized versions of standards-compliant EUV pods undergoing cycling, shipment, storage, and vacuum operation. A state-of-the-art blank defect inspection tool was used to quantify the defect protection capability at each step of the integrated test. To ensure the availability of an EUV pod for 2010 pilot production, progress and test results of commercialized EUV pods will be reported as well.

7636-78, Poster Session

Assessing out-of-band flare effects at the wafer level for EUV lithography

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Pulsed plasma based EUV sources generated from high-Z metallic elements radiate into a broad range of wavelengths; well beyond the 13.5 nm wavelength at the 2% bandwidth required for EUV lithography (EUVL). Calculations and measurements have shown that the Mo-Si multilayer based reflective optics necessary for band selection at EUV are also equally or more efficient reflectors for a range of wavelengths longer than 150 nm. Adding to this, the EUV resist development methods utilize existing molecular structures already developed for UV/DUV wavelength lithography, leading to the resists being sensitive to a group of wavelengths between 150nm and 300nm. The combined effect of all of these factors is the unwanted background exposure of the resist (flare) and reduced image contrast in patterning. A recent measurement from the alpha demo tool, estimates the flare contribution from out_of _band (OOB) light at the wafer level to be between 3-4% of the EUV light [1].

To accurately estimate the flare contribution from the OOB, we proposed the integration of a DUV source into the SEMATECH Berkeley 0.3-NA Micro-field Exposure Tool. This makes it possible for the controlled OOB exposure along with the EUV patterning of the resist. The details of the integration methods and available exposure measurements will be presented. The second part of the paper will provide a more detailed analysis of the potential impact of OOB radiation based on known resist, mask, and multilayer conditions. We expect that OOB can be treated as a pure reflectivity problem until the mask, beyond that mask absorber reflectivity and scattering will need to be accounted for. The simulation-based imaging results for predicting the effective flare as a function of mask feature types and sizes will be presented.

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7636-79, Poster Session

EUV modeling accuracy and integration requirements for the 16-nm node

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EUV lithography is widely viewed as a main contending technology for 16nm node device patterning. However, EUV has several complex patterning issues which will need accurate compensation in mask synthesis development and production steps. The main issues are: high flare levels from optical element roughness, long range flare scattering distances, large mask topography, non-centered illumination axis leading to shadowing effects, new resist chemistries to model very accurately, and the need for full reticle optical proximity correction (OPC). Compensation strategies for these effects must integrate together to create final user flows which are easy to build and deploy with reasonable time and cost. Therefore, accuracy, usability, speed and cost are important with methods that have considerably more complexity than current optical lithography mask synthesis flows.

In this paper we first analyze the state of the art in accurate prediction and compensation of each of these complex EUV patterning issues, and compare that to 16nm node expected production needs. Next we provide a description of integration issues and solutions which are being implemented for 16nm EUV process development. This includes descriptions of OPC model calibration with flare, shadowing, and topography effects. We also propose and critique a realistic (in terms of accuracy and mask area) flare parameter calibration flow to improve short and longer range flare correction accuracy above what can be achieved with only a measured EUV flare PSF.

7636-80, Poster Session

Identification, modeling, and observation of disturbing effects in EUV interferometer lithography

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The challenge of the Integrated Circuit size reducing leads to develop the next ways of processes for future years. In the lithography domain, since several years, the EUV Lithography appears as a possible technique to reach the ITRS roadmap requirements. Studies at different levels are so carried out. The EUV interferometry Lithography is still nowadays an efficient way to study and improve the EUV resist behaviors. The principle of an EUV interferometer is very close to the conventional one respecting some constraints induced by the incident wavelength. Two similar transmission gratings are placed in the same plan and are separated by an absorber pattern. These two gratings are lighted by a EUV coherent beam and diffract the light in different orders. The recombination of the +/- 1 order creates interference fringes with a pitch two times smaller than the grating pitch. Even if the principle seems to be obvious, the best use is only obtained regarding some huge constraints.

In this paper a large view of the behaviours that this kind of system must reach is presented. The disturbing effects, mainly on interference fringes, are also assessed.

The EUV source is also responsible for the contrast quality of the fringes. Then a photometry computation, taking into account the minimum light intensity and spatial coherence that the source must reach, is then detailed.

The interferometer design leads to disturbance impairing the interference fringes on the printing surface or on the contrast. The main reasons shown in the paper are:

- A Fresnel diffraction effect, due to boundaries of the grating windows.

- A shadowing effect on the +/- 1 order of diffraction, due to the thickness of the absorber pattern

- The resist wafer position, which can reduce the interference area is different to the focal distance.

Some simulations are made on the grating design to increase the diffraction efficiency on the first order. The gratings and the corresponding membranes are made in the cleaning room of the CEA-LETI. A Fresnel diffraction modelling is also built to quantify the impact of this phenomenon on the resist printing. All these simulation results are compared to experimental measurement made with the coherent EUV beam of the Synchrotron Radiation Center in Wisconsin. These results are also shown in this paper and improvement are proposed to decrease the disturbing effects.

7636-81, Poster Session

Flare modeling and calculation on EUV optics

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Flare impact is a critical issue in EUV lithography because it increases in proportion to reciprocal squares of the wavelength. The technique to estimate and control flare amount precisely is highly important for optical proximity correction (OPC) in EUVL.

Flare can be calculated by convolution a reticle pattern with a flare point spread function (PSF). For a single point on field it can be simplified as integration of the flare PSF within the bright field. Flare PSF is defined as (1-TIS)delta(r)+PSFsc(r); where TIS, total integrated scatter, is traditionally defined as integration of PSFsc to infinity; delta(r) is Dirac's delta function; and r is distance on wafer. PSFsc is a surrounding component of flare PSF around origin and is traditionally derived from the power spectral density (PSD) of surface roughness of each mirror. The amount of scatter light depends on mirror PSDs, while a portion of the scatter light with a higher scatter angle cannot reach wafer due to mechanical shadowing in optics. This means there is energy loss in optics. Due to this energy loss the total integration of PSFsc as a component reaching wafer is less than TIS which is the total integration of a different PSF as an "as-scattered" component. In other words, PSFsc is defined as light amount reaching wafer for use in calculation of image intensity, while TIS should be defined as total amount of as-scattered light.

We then introduced two PSFs: PSFsc and PSFsc0. PSFsc0 is directly derived from mirror PSDs. This is an "as-scattered" component. It is used only for calculation of TIS. PSFsc is calculated as light amount reaching wafer taking obscuration in optics into account including limitation of multilayer coating area. This is a component reaching wafer. Hence TIS should be provided seperately with PSFsc, instead of calculating by integration of PSFsc.

We also applied other consideration: release of linear approximation in domain conversion among f (spatial frequency) in PSD, scatter angle and r (distance on wafer) in PSF; and scatter extinct effect by multilayer.

Domain conversion from PSD to PSF is traditionally linear using a small angle approximation. However, for a distance of ca. 1mm or longer on wafer the linear approximation does not work well. Non-linear domain conversion is required for estimation of long range flare. In order to apply non-linear domain conversion we do not use an equivalent system PSD which is obtained by projecting mirror PSDs with scaling onto pupil.

Scatter extinct effect by multilayer is a factor reducing scatter light and flare. On a normal surface without interferential coatings scatter amount depends directly on PSD of surface roughness, while on a multilayer-coated surface scatter amount depends not only on PSD but also on interference by multilayer.

Using these consideration we can calculate flare behaviors which agree well with the results of experimental Kirk flare tests.

7636-82, Poster Session

Flare mapping and correction results for EUV alpha demo tool

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One of the major concerns developing EUVL technology is high flare effect introduced by short wavelength of the source and difference in optics used for the tool. Compared to conventional lithography, source wavelength is 14 times smaller and this coupled with change in the optics from lens to mirror may show significant rise in flare level. In our previous study, ADT tool at IMEC showed 16% flare level compared to 2~3% of conventional ArF scanner. Measurement from the wafer showed that high flare level of EUV tool limited the minimum resolution of printable feature size as well as degraded the output image on the wafer. Therefore flare correction is very crucial and prior to correction, prediction of flare effect is inevitable in order to acquire high resolution wafer result in EUVL technology.

In this study, in order acquire high resolution wafer result in EUVL technology, we mapped and corrected the EUV flare effect on real layer of DRAM. We investigated many aspect of flare correction such as flare mapping, data handling of flare corrected data, mask creation of flare corrected data and wafer result of corrected and uncorrected data. First, flare distribution of the EUV Alpha Demo tool was measured and was used in simulation tool to simulate several test case wafer result. Next, using the measured flare distribution result, flare mapping was performed on contact layer of DRAM. With acquired flare map, correction of the flare effect on layout was performed. In house EUV mask was then created using flare corrected and uncorrected data and wafer measurement was performed to verify the flare correction scheme. Currently, measurement of the corrected and uncorrected data is under way and comparison result will be presented at the conference.

7636-83, Poster Session

Practical flare compensation strategy for DRAM devices

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1st introduction of EUV lithography will be occurred in DRAM because logic is slightly behind in schedule and spacer based pitch split technology is already ready for flash memory. In order to realize the introduction of EUV successfully, optical correction of EUV mask shadowing and flare effect is also prerequisite in addition to overcoming well cited issues of EUV lithography such as source, mask, and resist performances. In this study, we studied about practical methodology of EUV flare correction limited to DRAM, because its layout has simple floor plan compared to others.

In order to split the flare level, test layouts with various sizes of surrounding open frame patterns are prepared. Corresponding flare levels are estimated to be 3~8% by simulation with approximate model of point spread function (PSF). Then implications of EUV flare in CD and process window of various DRAM patterns are investigated experimentally.

As well known, flare is hard to be controlled hardware-wisely in EUV lithography. Therefore flare compensation through layout correction is required. So is the modeling of PSF beforehand. PSF is measured along various slit positions by using Kirk pad with various sizes. The measured PSF is found to be well matched to that derived from the PSD modeling by mathematically calculated from surface roughness of the projection optics.

Flare is calculated as convolution of PSF and pattern density. This requires astronomical amount of computational time, because PSF in EUV has a very long tail that even reached around several tens of thousands micron range. Instead we calculated the pattern density of real devices with increasing radius of annulus. If the levels of pattern density are saturated over some radius range, convolution integral with longer tail part of PSF can be approximated with fixed DC flare level. Then we will talk about rightful flow of shadow and flare corrections.

7636-84, Poster Session

Effects of extreme-ultraviolet bandwidth on patterning of 22-nm node

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In EUVL (Extreme Ultra Violet Lithography), a 13.5 nm radiation wavelength generated by EUV source is used to print circuits. Most EUV is strongly reflected at this wavelength from the multilayer mask. However, the bandwidth of EUV source is very broad compared with currently available 248 and 193 nm source, which is in the order of 0.1 pm. Thus the broad bandwidth of EUV might give strong influence on the patterning even though EUVL uses mirrors for the imaging instead of lenses. For analyzing the effect of EUV wavelength and bandwidth to the image quality and process window margin, we used commercial S-litho of Synopsys as a simulation tool and we could get the simulation result such as reflectivity, image contrast, NILS (Normalized Image Log Slope), process window and Iso-Dense bias with respect to the change of central wavelength and bandwidth. This paper presents the patterning dependency of 22 nm node dense patterns and 25 nm contact holes on the change of central wavelength and bandwidth in EUV source. By changing the central wavelengths (13.4, 13.5, and 13.6 nm), there were noticeable differency. The contrast and NILS of 13.4 nm wavelength was better than those of 13.5 nm in 22 nm line and space pattern and 25 nm contact hole pattern. Changing the bandwidth (FWHM, Full Width at Half Maximum, 300 ~ 1550 pm), also

showed different simulation result. According to our simulation, the effect of EUV wavelength and bandwith should not be neglected for better EUV patterning. In this paper, the optimized wavelength and bandwidth will be suggested for improving patterning process margin at 22 nm line and space, and 25 nm contact hole patterns.

7636-86, Poster Session

Fabrication of 35-nm via-hole patterns for interconnect test chips with EUV lithography

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EUV lithography (EUVL) is a promising candidates for the fabrication of ULSI devices with a half pitch of 3x nm and beyond. Another candidate for fabricating 3x-nm-node devices is double pattering technology (DPT) using ArF immersion lithography. For hole patterns, however, minimum half pitch for the DPT is only around 38 nm. To fabricate 35-nm half-pitch interconnect test chips, we used EUVL for the three critical layers, which are metal 1, via 1 and metal 2. In this study, we used the EUV1 full-field scanner to evaluate the printing characteristics for 35-nm via-hole patterns.

The EUV1 full-field scanner was installed at Selete in 2007. The maximum field size is 26 mm x 33 mm. The EUV light source is Xe-fueled discharge-produced plasma (DPP). Since the wavefront error of the EUV1 is 0.6 nm RMS and the flare is about 10%, aerial images under conventional illumination (sigma = 0.8) are good enough for the fabrication of 35-nm via-hole patterns. We used EUVL masks with a 51-nm-thick LR-TaBN absorber layer and a 10-nm-thick CrN buffer layer. The absorber thickness was optimized to control the phase shift effect. The resist was an 80-nm-thick SSR3, which has a resist blur of about 10 nm. To reduce iso-dense bias and anisotropy of hole shapes, simple optical proximity correction (OPC) and shadowing effect correction (SEC) were applied to the mask patterns. There were no assist features in the mask patterns. Flare variation compensation (FVC) was not applied to the mask for via 1 layer because of the low pattern density. The EUV mask was successfully fabricated with good critical dimension (CD) control. The mean to target of the CD was about 2 nm, and CD uniformity was better than 5 nm (3sigma) on the 4x mask.

Figure 1 shows the SEM images of 35-nm via-hole patterns printed with the EUV1. The holes are nearly circle. For the aligned via pattern, the minimum pitch is 70 nm in the X-direction; and for the staggered via pattern, it is 99 nm in the diagonal direction. All three types of patterns were successfully fabricated with almost the same CD. A simulation analysis revealed that the mask error enhancement factor (MEEF) to be about 2.5, the exposure latitude to be about 20%, and the depth of focus (DOF) to be about 100 nm when the via-hole size was 35 nm. The experimental results agreed fairly well with the simulation results. We also evaluated the CD uniformity of printed 35-nm via-hole patterns.

Using a multi-stacked resist process, 35-nm via holes were successfully fabricated in a low-k dielectric layer. We fabricated interconnect test chips and measured electrical properties, such as the via resistance. The results demonstrated that EUVL is useful for the fabrication of ULSI devices with a half pitch of 35 nm and beyond.
A part of this work was supported by New Energy and Industrial Technology Development Organization (NEDO).

7636-87, Poster Session

Characterization of the clamp pressure of electrostatic chucks

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Berliner Glas KGaA is specialized on the manufacturing of high quality chuck systems.

Electrostatic chucks (ESC) are especially used for wafer handling, chucking during lithographic processing, coating and etching instruments. The main task of the chuck is to provide a well defined positioning and thermal stabilization of the wafer. The wafer material consists most often of silicon. In particular wafer material may be magnesia, alumina or glass.

For a functional qualification of the ESC clamp performance Berliner Glas has developed a process, which includes the measurement of the clamp pressure with an interferometer.

As representative wafers, silicate glass wafers are used among silicon for the qualification process. The bending of the chucked wafer due to the clamp pressure is measured in the range of 20..500 mbar. This new method allows for a lateral resolution and calibrated clamp pressure results. The theoretical bending and vacuum chucking with the same chuck gives evidence for the quantitative results. Transient clamp pressure variation can be measured with highest accuracy of 2 mbar. The results can be used for a local correction of the clamp force by adjustment of the effective dielectric thickness.

7636-89, Poster Session

Investigation of a ‘rule-of-thumb’ mask roughness induced LER model

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As next generation lithography techniques such as extreme-ultraviolet lithography (EUVL) push to ever smaller critical dimensions, achieving the stringent requirements for line-edge and -width roughness (LER/LWR) is increasingly challenging. Mask multilayer roughness has recently been demonstrated to be an important source of image plane LER. Studies in this area have thus far been dominated by rigorous modeling, but it would be beneficial to come up with a useful “rule-of-thumb” simplified model allowing mask multilayer roughness specs to be easily estimated for various feature sizes. To this end we are proposing a model based on open field speckle and image log slope (ILS) for the features on an ideal multilayer. In this study we examine the validity of this approach under a range of conditions including sigma, NA, CD, roughness correlation length, aberrations, ... Preliminary results show that the simplified approach works well at relatively low coherence (sigma > 0.5) but tends to break down at higher coherence with the simplified model under-predicting the LER. Reasons for this discrepancy are discussed.

7636-90, Poster Session

Mask roughness and its implications for LER at the 22- and 16-nm nodes

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Line-edge roughness is one of the leading challenges next generation lithographies. This is especially true for EUV where source power is of concern. Anything that further limits the resist LER budget is thus of significant concern. Another potential source of LER is phase roughness on the mask. Being a reflective architecture with a 13.5 nm wavelength, it takes very little roughness on an EUV mask to generate appreciable amounts of phase shift and thus LER. Here we describe EUV mask roughness requirements for the 22 and 16 nm nodes determined based aerial image modeling. We consider both multilayer roughness as well as capping layer roughness. We also consider the effects of roughness spectral content, imaging aberrations, and illumination conditions.

7636-91, Poster Session

The effect of line roughness on the reconstruction of line profiles for EUV masks from EUV scatterometry

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The development of EUV lithography is critically based on the availability of suitable metrology equipment. To meet the industries requirements, the Physikalisch-Technische Bundesanstalt (PTB) operates an EUV reflectometry facility at the electron storage ring BESSY II. It has been shown that EUV scatterometry is a versatile metrology for characterizing periodic structures, regarding critical dimension (CD) and other profile properties. The short wavelength of EUV is particularly advantageous since it increases the sensitivity to structure roughness. On the other hand, structure roughness also modifies the diffraction intensities used for structure reconstruction using rigorous calculations of EUV diffraction. We present here first investigations of the influence of roughness induced modifications of diffraction intensities on the subsequent reconstruction of line profiles. A method is developed to numerically estimate changes in measured diffraction intensities induced by line edge and line width roughness. Finally, the reconstructed profiles for undisturbed and disturbed diffraction intensities are compared.

7636-92, Poster Session

Electrostatic chucking of EUVL masks: co-efficient of friction

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In extreme ultraviolet lithography (EUVL), mask clamping is done with an electrostatic chuck in vacuum. For proper control of the chucking process and meaningful theoretical modelling, friction of the mask on the chuck is a critical parameter.

To determine static and dynamic friction values, measurements were performed in vacuum on a mask blank with a test chuck, that was smaller than a real EUVL mask chuck, but otherwise nearly identical in pin surface, materials and electrostatic forces. Experimental results were obtained at various voltages for a materials combination of Ultra Low Expansion Glass for the pin chuck surface and a chromium film for the mask backside metallisation, respectively.

For the experiment, a mono-polar pin-chuck of diameter 70mm was slid within the quality area of a metallised mask blank with dimensions $(152mm)^2$. Care was taken, to minimize Abbe-type errors in the measurement of the friction forces, using a tensile force sensor in a kinematic mount.

Both, the pin-chuck and the mask blank were highly flat and smooth on its particular surfaces. For the pin-structure, our previous design for an EUV-chuck was applied /1/ and a flatness value of about 110nm PV across the pin area was obtained.

From our measurements at different polarities and voltages up to 2kV, values in the range from 0.25 to 0.35 were derived for the resulting static friction coefficients. This justifies previous assumptions in FEM modelling of a static friction coefficient >0.2 and is in very reasonable agreement with recent experimental results of another group /2/.

7636-93, Poster Session

Influence of mask surface roughness on 22-nm node extreme ultraviolet lithography

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Extreme Ultraviolet Lithography (EUVL) is one of the patterning technologies for the 22 nm node and below. Generally, EUVL used a reflectivity type mask consist of absorber layer on a mask blank substrate coated with Mo/Si multilayer. Especially, reflectivity from EUV mask multilayer could be one of the important factors to make EUV process to be ready for 22 nm node. In spite of the developed technologies, the reported experimental reflectivity (60-66 %) is much less than the theoretical reflectivity (73 %) from the perfect EUV mask multilayer because of the Mo/Si rough boundaries and multilayer top surface roughness. The surface roughness that occurs in deposition of multilayer makes the reflectivity loss. It seems that it might be difficult to reach the ideal reflectivity and 22 nm node process has to live up with the imperfect reflectivity.

In this study, we focused on the influence of the surface roughness on the Mo/Si multilayer for 22 nm node. First we studied the reflectivity loss for the multilayer surface roughness. The magnitudes of short, medium, and long range roughness are compared in terms of the amplitude and phase non-uniformity because even 1 nm roughness can make huge difference in EUV. The aerial image and process latitude with surface roughness are studied and the possibility of 22 nm node patterning with surface roughness will be reported.

7636-94, Poster Session

A comprehensive study of IP error contributions in EUV lithography

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Image placement (IP) and overlay error specifications are serious concerns for lithography at each successive technology node. Some of the primary contributors to image placement error (IPE) in EUV lithography are reticle and chuck surface non-flatness and chucking flatness non-uniformity. In this paper, we describe the results of three sets of experiments designed to identify the different contributions to IPE and to determine the limits of each of the contributing terms.

The first set of experiments involved the imaging a non-flat reticle with an ASML EUV Alpha Demo Tool (ADT) in Rohm & Haas XP4502J resist. EUV resist images of XPA image placement fiducials were read out using ASML's Wafer Stage Accuracy test in the EUV ADT in Albany, New York. The non-flat reticle had an interferometrically measured flatness of 546 nm P-V (thickness variation) over its quality area and was grossly out-of-spec with respect to the flatness requirements of a production-quality EUV mask. Simulations were used to predict the IPE when printing with this non-flat reticle. The predicted IPE has two separate components: (1) IPEs due to reticle flattening and (2) IPEs due to reticle thickness variation and to non-telecentric illumination of the mask in the EUV exposure tool. The measured IP errors show good correlation to the predicted IP errors.

A second set of experiments was carried out using a flat reticle with 120 nm P-V thickness variation over its quality area. This reticle was designed to be rotatable, i.e., imageable in four different orientations - 0, 90, 180, and 270 degrees, so that chuck and reticle contributions to IPE could be determined. A third set of experiments was performed on both the flat and the non-flat reticles after varying the clamping pressure on the electrostatic reticle chuck. Changes in clamping pressure result in different IP errors due to reticle flattening and final as-chucked surface flatness. In this paper, we will discuss in detail the experimental results from the printing of both reticles.

7636-95, Poster Session

Photon flux requirements for EUV-reticle imaging microscopy in the 22- and 16-nm nodes

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Mask imaging microscopy is essential for the development of patterned reticles for each generation of lithography. This is especially true for extreme ultraviolet (EUV) lithography where the illumination wavelength is significantly smaller than in previous generations, and the optical properties of mask materials are highly wavelength specific. Coupled with the shrinking design rules of future generations, imaging EUV masks with EUV light gives direct, predictive measurements that other inspection wavelengths are not be able to provide.

Using EUV-wavelength microscopy to study the field reflected from EUV masks yields detailed information about mask defects and the

performance of defect repair strategies, without the complications of photoresist imaging. Furthermore, the measured aerial image intensity distributions can be used as feedback to improve mask and lithography system modeling methods. In addition to basic mask research and development, interest in commercial standalone EUV mask inspection tools, and intermediate EUV mask imaging "bridge tools" motivates an investigation of the fundamental measurement limits, based on shot-noise and various inspection parameters.

In order to understand the photon-flux-depenent pattern measurement limits of EUV-wavelength mask-imaging microscopy, we have investigated the effects of shot noise on aerial image line-width measurements for lines in the 22 and 16-nm EUV generations. In many ways, the measurement of defects in dense line patterns is limited by the line-edge or line-width roughness that appears in the recorded images. To be observable with high confidence, defects must stand out above the background noise level. The measured roughness arises both from the mask's inherent pattern and phase roughness (which is spatially filtered by the microscope's optical system and is affected by the illumination partial coherence) and from a combination of static and random noise sources, such as shot noise, CCD readout noise, background light, and optical system flare.

Using a simple model of image formation near the resolution limit, we probe the influence of photon shot noise on the measured, apparent line roughness. With this methodology, we can arrive at general conclusions that are independent of the specific microscopes under consideration.

The observed roughness level is most highly dependent on photon flux per image pixel. For constant mask-illumination photon flux densities, and at each linewidth value, there will be tradeoffs between the pixels' effective dimensions, and the exposure time. The effective dimension is controlled by the microscope's magnification ratio. A expected dependence on image contrast (image slope) is also considered.

As an example, with relevant imaging parameters, we find that in order to achieve a LWR 3-sigma value of 5% for dense 88 nm mask features with 90% contrast, and 13.5 nm effective pixel width, we require a photon flux of approximately 700 photons per pixel per exposure.

These results of these calculations are applied to the SEMATECH Berkeley Actinic Inspection Tool (AIT), a synchrotron-based EUV microscope that we operate at Lawrence Berkeley National Laboratory, and to potential zoneplate-based bridge-tool designs. The AIT uses high-magnification Fresnel zoneplate lenses, with various numerical aperture values, to directly image both blank and patterned EUV masks.

7636-96, Poster Session

Development of a super-precise ultrasonic measurement system of zero-CTE temperature for EUVL-grade TiO2-SiO2 ultra-low-expansion glasses

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Ultra-low-expansion (ULE) glasses having a coefficient-of-thermal-expansion (CTE) within ±5 ppb/K around desired room temperatures, for example 22±3°C, are required for basic substrate materials of photomask blanks and reflective optics in extreme ultraviolet lithography (EUVL) systems. TiO2-SiO2 glass is one candidate. CTE specifications, viz., temperatures at which CTE becomes zero, T(zero-CTE), should differ for mask substrates and mirrors at different positions because of high light-source power. The T(zero-CTE) can be controlled to room temperatures by adjusting the TiO2 concentrations C(TiO2) to around 7 wt%. It is very important to evaluate the surface properties for EUVL use.

We have completed to develop a practical-use system of super-precisely measuring the CTE characteristics of TiO2-SiO2 glasses as an indirect ultrasonic measurement method, based on our experience of the line-focus-beam ultrasonic material characterization (LFB-UMC) system. Evaluation is made by measuring the velocity of leaky surface acoustic waves (LSAWs), VLSAW, excited and propagated on a water-loaded specimen surface. This system operates at 225 MHz and/or 75 MHz under stabilized measurement environment of temperatures, for example, 22.00°C, with a measurement accuracy of ±0.17 m/s (±0.005%) at 225 MHz and ±0.07 m/s (±0.002%) at 75 MHz.

We demonstrated the performance of the system for a homogenized TiO2-SiO2 glass specimen at 225 MHz. We obtained two kind of specimens: two specimens (A and B) with dimensions of 70 x 70 x 5 mm^3 prepared from both ends of a commercial ULE glass ingot with 350 mm long; and one specimen (C) with dimensions of 67 mm x 10 mmt from an ingot homogenizing the commercial ingot by heat-treating above softening temperature. We measured two-dimensional distributions of VLSAW for both surfaces of the specimens: for specimens A and B averaged VLSAW of 3308.51 m/s with a maximum variation ∆VLSAW of 7.11 m/s associated with striae in the ingot; and for specimen C averaged VLSAW of 3307.16 m/s with ∆VLSAW of 1.08 m/s. Using the relationships among the VLSAW, C(TiO2), and CTE characteristics of CTE(22°C) and T(zero-CTE) obtained previously, we could estimate C(TiO2), CTE(22°C), and T(zero-CTE) as follows: for specimens A and B 7.07±0.21 wt%, 27.94±15.31 ppb/K, and 4.31±3.01°C; and for specimen C 7.15±0.03 wt%, 22.14±2.33 ppb/K, and 5.45±0.45°C. We obtained a homogeneous glass ingot satisfying the CTE specifications within ±5 ppb/K (corresponding to ±1.16 m/s), but having the small T(zero-CTE) because of the considerably small C(TiO2).

CTE characteristics for specimen C were measured by an optical heterodyne interferometric dilatometer in a temperature range of 5-35°C at the National Metrology Institute of Japan: CTE(22°C)=31.5±4.0 ppb/K, and T(zero-CTE)=6.0±2.3°C. C(TiO2) was measured as 7.03±0.02 wt% by X-ray fluorescence analysis.

The resolution in VLSAW of ±0.17 m/s at 225 MHz corresponds to resolutions of ±0.72 ppb/K for CTE(22°C) and ±0.41°C for T(zero-CTE). It can be expected that the system will be put into a practical use with more precise calibration lines for CTE characteristics.

Both glass manufacturers and users can conduct speedy inspection of all EUVL-grade TiO2-SiO2 ULE glass substrates with reliable data of T(zero-CTE) by this ultrasonic system.

7636-97, Poster Session

Improved performance of a table-top actinic full-field microscope with EUV laser illumination

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We present the most recent results on a table-top actinic aerial microscope capable of imaging absorption defects on EUVL masks with a half-pitch spatial resolution of ~55 nm.

In this zone plate-based microscope, the images are generated by guiding the output of a compact EUV laser emitting at 13.2 nm by a Mo/Si multilayer coated flat mirror onto a condenser zone plate which focuses the light onto the sample at an angle of incidence of 6 degrees. The reflected light is collected by an off-axis zone plate objective, forming an image on a back illuminated CCD detector located parallel to the sample.

Our previous setup (Fig. 1.a) was based on a 1 µW average power Ni-like cadmium EUV laser with highly monochromatic pulses (∆ / < 1E-4) and an average spectral brightness of brightness of ~4E12 photons mm-2mrad-2s-1(0.01%BW)-1. The condenser had an outer zone width of 100 nm and a diameter of 5 mm, with a working distance of ~40 mm at 13.2 nm wavelength. The off-axis objective zone plate had a diameter of 120 µm and a focal distance of ~1 mm at this wavelength. Its numerical aperture (NA=0.0625) was chosen to emulate the imaging characteristics of a typical 4x stepper (NA = 0.25) used for EUV lithography. With this setup, images of a test pattern were obtained with exposure times of 20 seconds at a magnification of ~610x with each pixel on the CCD corresponding to 22 nm in the sample plane (Fig. 1.b). The images had a measured spatial resolution

of 55 nm and a field-of-view of ~5x5 μm2.

We will now present results following extensive upgrades to the microscope in order to improve the quality of the images in terms of illumination uniformity and reduce image exposure time. These upgrades include a ten-fold increase in the output of the table-top EUV laser and the design of new condenser zone plates for higher control of the uniformity of the illumination.

The characteristics of this actinic imaging tool will be discussed in relation to the requirements established for EUVL mask inspection.

7636-98, Poster Session

Testing of EUV optics and sensors using focused radiation from a table-top LPP source

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As a consequence of the steadily increasing EUV powers and radiation doses, damage and degradation testing of EUV optical elements and sensor devices has become an important issue. In this contribution we report on first damage tests on optics and detectors for the wavelength of 13.5nm using a high fluence micro-focus from a laboratory-scale EUV source. The setup consists of a laser-generated plasma from a pulsed gaseous Xenon jet or a solid Au target, respectively. In order to obtain a small focal spot resulting in a high EUV fluence, a modified Schwarzschild objective consisting of two spherical mirrors with Mo/Si multilayer coatings is adapted to the source, simultaneously blocking unwanted out-of-band radiation. By demagnified (10x) imaging of the Au plasma an EUV spot of 5 μm diameter with a maximum energy density of ~1.3 J/cm² is generated at a wavelength of 13.5 nm and a pulse width of 8.8 ns.

We demonstrate the potential of this integrated source and optics system for damage testing on EUV optical elements and sensoric devices. As an example, single pulse (“1-on-1”) and multiple pulse (“S-on-1”) damage thresholds were determined for Mo/Si multilayer mirrors, using both on-line optical microscopy, inteferometry and atomic force microscopy for damage detection. The data are compared with in-situ measurements of the reflectivity change at 13.5nm. Moreover, thin metal coatings (Gold) used as grazing incidence mirrors were irradiated. Threshold energy densities for damage and film removal were determined, showing a linear dependence on the film thickness.

Furthermore, we have tested several EUV detectors with respect to linearity and radiation hardness. AlGaN photodiodes were compared to standard silicon diodes, showing much higher stability when exposed to intense EUV radiation. Sensors based on EUV-to-VIS quantum convertors (Ce:YAG crystals, phosphor coatings) employed for beam characterization of an FEL (FLASH / DESY) were investigated in terms of linearity, saturation behavior and conversion efficiency. As an example for high-resolution modification and structuring of solid surfaces, EUV ablation of PMMA, PC and PTFE was investigated as a function of fluence, offering the possibility of generating smooth structures with very small feature sizes.

7636-99, Poster Session

Absolute calibration of charge coupled-device using calculable synchrotron radiation

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Charge coupled devices (CCD) are commonly used for detection of X-ray and extreme ultraviolet (EUV) radiation. In anticipation of the need for precise imaging at EUV wavelengths in various applications such as the at-wavelength inspection of EUVL mask, the analysis of spectrally dispersed vacuum ultraviolet (VUV) or EUV source, and EUV microscopy, we have measured the responsivity and uniformity of a commercially available back illuminated VUV to soft x-ray charge coupled device (CCD). The calibration was performed at the EUV Detector Radiometry Beamline (BL-9) at the Synchrotron Ultraviolet Radiation Facility (SURF-III) at the National Institute of Standards and Technology (NIST). These measurements were performed at different wavelengths varying from 10 nm to 50 nm. Responsivity of the CCD was spatially averaged with a spot size of roughly 6 mm2. This calibration is traceable to a cryogenic radiometer as a primary standard.

7636-101, Poster Session

Enhanced optical performance of 5.5 sr LPP collector mirror

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The source output power and lifetime, including the collector optics lifetime, remain the key issues for EUV lithography systems today. In order to meet the challenging EUV pilot source requirements, both the reflectivity and the wavelength matching of the multilayer coated LPP collector mirrors have been enhanced considerably during recent development efforts. A number of 5.5 sr ellipsoidal mirrors with more than 660 mm outer diameter were coated with laterally graded high-reflective multilayers. The multilayer mirror coatings were optimized in terms of high peak reflectivity at 13.5 nm. The measured s-polarized reflectance of the LPP collector mirrors are well above 60 % within the clear aperture resulting in the specified non-polarized reflectance of R > 50 %. Further deposition technology optimization focused on precise wavelength matching. The design wavelength of 13.5 nm is routinely achieved within a wavelength deviation of ± 0.03 nm or less. The multilayer coated collectors collect EUV light with 5.5 sr solid angle thus representing by far the largest EUV multilayer collector mirrors coated to date. The current optical properties of the EUV collector mirrors and ways for future improvements will be discussed in detail.

7636-102, Poster Session

Characterization of the polarization properties of PTB’s EUV reflectometry system

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The development of EUV lithography is critically based on the availability of suitable metrology equipment. To meet the industries requirements, the Physikalisch-Technische Bundesanstalt (PTB) operates an EUV reflectometry facility at the electron storage ring BESSY II. It is designed for at-wavelength metrology of full-sized EUVL optics, a total uncertainty of 0.10 % for peak reflectance is achieved with a reproducibility of 0.05 % and a reproducibility of 1 pm for the centre wavelength. Measurements at PTB use almost linearly polarized radiation, whereas EUV lithography machines are operated with unpolarized sources and the status of polarization changes throughout the optical system. Therefore, to transfer these high-accuracy measurements to the EUV optical components under working conditions, it is essential to study the polarization dependence. We present a detailed characterization of the state of polarization for our EUV reflectometry system. We will discuss the uncertainties of PTB’s reflectometry for large oblique angles with respect to the influence of polarization. An example of such measurements is the characterization of large 5 srad collector mirrors for LPP EUV-sources; the largest EUV optical components presently available.

7636-103, Poster Session

EUV-multilayer coating of IR-eliminating reflection gratings

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For the spectral separation of EUV and parasitic IR, both critically present in the overall spectrum of some perspective EUV light sources, special multilayer-coated reflection gratings show great potential. Based on rigorous calculations is has been demonstrated that full spectral separation without additional losses in EUV throughput can be obtained from Mo/Si multilayers deposited on a blazed grating, provided the grating topography can be replicated by the multilayer stack. In this study, multilayer topographies near the key anomalies in such grating-like structures, namely sharp step edges and steep walls, are examined, employing different deposition schemes. Based on cross section TEM analysis an explanatory model describing the morphology of the successive layers is developed. Further insight into the periodicity and the general performance of the multilayer is obtained by EUV reflectometry. The main distortions in multilayer structure and hence EUV performance are found to be restricted to a region within micrometers from the anomalies, which is small compared to the proposed grating period (50-100 μm). These multilayer coated blazed gratings can thus be considered a viable option for spectral purity enhancement of EUV light sources.

7636-104, Poster Session

High-reflectance multilayer coating technology for 3100-EUVL projection optics

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Multilayer reflective optics for the first pre-production EUV scanners, the ASML NXE 3100 series, are currently being produced. Though these activities are based on know-how and development results from the Alpha Demo Tools, now in operation at CNSE and IMEC, the multilayer coating technology has been greatly improved by applying new compositions and processes. This includes a new multilayer stack with improved interlayer quality, resulting in a reflectance of the capped multilayers of close to 70% on the real optical elements of the scanners. This technology enables a dramatic improvement of the throughput of the optical system. This new multilayer stack, which results from the progress in the multilayer research, has successfully been deposited on the projection optics while meeting other specifications such as wavelength matching, lateral uniformity, multilayer induced stress and non correctable added figure error. The results of the multilayer coatings of projection optics elements will be presented in this paper.

7636-105, Poster Session

Corner rounding in EUV photoresists: tuning through development time, PEB temperature, and platform constituents

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At the 2008 EUV Symposium it was shown that corners patterned in EUV photoresist often exhibit a rounding bias between inner and outer corners [1]. SEM metrology of the experimental EUV photo mask showed no corner rounding bias in the mask; modeled aerial images assuming a thick mask (multilayer + absorber) revealed no aerial image bias; and various EUV resist blur models including PROLITH, single blur [2] and dual blur [3] models could not reproduce the experimentally observed bias. Today, the source of the corner rounding bias remains unknown.

Table 1 shows the average radii of inner and outer corners in Resist A as development time is varied from <<1 second to 3 seconds in 1-second intervals. Within the first three seconds of development the average inner and outer radii of Resist A increase by 19% and 13%, respectively, with a corresponding 25% increase in 50 nm 1:1 LER. These data warrant a more complete investigation of the EUV development process and how it affects the fidelity of corners and patterning in general. In this paper the corner rounding bias, deprotection blur, and LER of three of today's leading chemically amplified EUV photoresists is monitored as development time and post-exposure bake (PEB) temperature are varied. In addition, the same performance metrics of an experimental EUV resist platform are monitored as base and photo acid generator (PAG) size and weight percent are varied. All experimental results are compared to predictions from PROLITH PEB and development models and similarities/ differences between the two are elucidated. This work was supported by the Director, Office of Science, of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231.

7636-106, Poster Session

Absorption and outgassing of photoresists and underlayer materials upon irradiation at 13.5 nm

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We measured the ionic and neutral outgassing of polymethylmetacrylate, round robin resist, and underlayer materials following a photoabsorption event with irradiation at 13.5 nm. Radiation was delivered from a 08A1BM-LSGM beamline at the National Synchrotron Radiation Research Center in Taiwan. The absorption coefficient and film-thickness evolution of the sample upon irradiation were monitored in situ and actinic with an EUV reflectometer. The thickness evolution was derived and ascribed to an EUV ablation effect, which was proved by examining the film-thickness changes of overly exposed samples with a profilometer. For ionic outgassing, we determined the absolute ionic outgassing yield (AIOY) with a double-ion chamber method. We also characterized the outgassed ion species, and derived the relative extent of outgassing F^+, CH_3^+ and $C_2H_5^+$ ions with a quadrupole mass spectrometer (QMS). The exposure rate constants (Dill's C parameter) and diffusion for F^+, CH_3^+, and total ions were examined with the double-ion chamber method and QMS. For neutral outgassing, we monitored the relative pressure rise with an ion gauge, and characterized the outgassed neutral species by QMS. Results indicate that PMMA generates the greatest ablation and ionic and neutral outgassing. F^+ outgassing from fluorine-containing compounds and hydrocarbon ionic outgassing are equally important. Furthermore, this study shows that the neutral and CH_3^+ outgassing is polymeric type dependent, and the extent of both outgassing can be correlated with a photoabsorption and structural metric as [abs/double-bond equivalent per carbon atom]. Rate constant measurements show that the Dill's C parameters leading to CH_3^+ outgassing for the same polymer type are similar, and those leading to F^+ outgassing for the same fluorine-containing compositions are similar. Kinetic analysis also shows that ionic outgassing contributed from diffusion can be appreciable when the outgassing measurement is conducted under a low photon flux for a long exposure time.

7636-107, Poster Session

Challenges of EUVL resist process toward practical application

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Conf. 7636: Extreme Ultraviolet (EUV) Lithography

EUV lithography is one of the most promising technologies for the fabrication of 22nm generation devices. It has various advantages including shorter manufacturing TAT, higher k1 process factor and process extendibility to the subsequent generation devices in comparison with double patterning technologies. However, it is well-known that EUV lithography still has some big issues. The greatest concern is increasing the light source power followed by mask defectivity and resist process issues. Although there have been many papers and discussions regarding EUV resist process in previous technical conferences, the issue is still unclear for practical EUV lithography. We expect to uncover additional resist process issues, especially on a mass production level.

Risk extraction is generally important to find process issues. This paper reports the extracted risk issues for practical EUV resist processes and discusses verification for them. Firstly, this risk extraction was carried out with emphasis on critical dimension control, defectivity and productivity for mass production EUV resist process. As a result, some risk factors including the resist development process have been clarified.

Next, the authors have empirically verified these risk factors. The authors verified these uncovered risk factors by utilizing the knowledge that has been accumulated on current resist process development based on the similarities between EUV and conventional resist materials. Furthermore, the authors report on countermeasures for the issues that were identified as being risk factors in EUV resist processing.

7636-108, Poster Session

Evaluations of EUV resist outgassing by gas chromatography mass spectrometry (GC-MS)

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The development of high-performance EUV resists is still one of top three critical issues in EUV lithography. In addition resist outgassing is a specific issue for EUV resist. Many researchers have investigated EUV resist outgassing by use of pressure-rise method and quadropole mass analyzer (Q-MASS). These method, however, have some weak points evaluating the relation-ship between real contamination of mirror and masks and a specific outgassing molecule because pressure-rise method only measures total pressure from resist outgassing and Q-MASS method shows fragmentation of outgassing molecules. Therefore we introduce gas chromatography mass spectrometry (GC-MS) to measure exactly EUV resist outgassing species [1].

This presentation summarizes the systematic evaluations of EUV resist outgassing by GC-MS: the evaluation results of more than 20 numbers of new EUV resists based on various materials. It is found that relatively large molecular-weight components more than mass-number of 150 exist in resist outgassing and main components from resist outgassing originate from protection group and photo-acid generator (PAG).

This work is supported by New Energy and Industrial Technology Development Organization (NEDO).

[1] Shinji Kobayashi, Julius Joseph Santillan, Hiroaki Oizumi and Toshiro Itani, Proc. SPIE 7273 (2009) 727320.

7636-109, Poster Session

Measuring resist-induced contrast loss using EUV interference lithography

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The performance of lithographic exposure tools in terms of image contrast can be characterized by photoresist patterning. However, in the analysis of resist patterns, e.g. via exposure latitude measurements, the contrast loss induced by the resist has to be taken into account as well. This resist induced contrast loss is a measure of blur introduced by the resist itself. It can be described as the deviation of the resist performance from an ideal, binary behavior with a constant dose threshold. However, resist contrast measurements are only possible if the exposure tool image is known and its impact on the overall contrast loss can be determined.

In this paper we will present a different approach for determining the resist contrast loss which is based on extreme ultraviolet interference lithography (EUV-IL). The EUV-IL tool installed at the Swiss Light Source (SLS) is based on diffraction gratings and operates at a wavelength of 13.4 nm (92.5 eV). The grating-based interferometer makes use of the spatial coherence of the beam. Light diffracted by transmission diffraction gratings patterned on a semi-transparent membrane produces an interference image at a certain distance behind the gratings. The exposure of a photoresist with an interference pattern, which can be analyzed more easily than a projection image, enables an independent method for isolating and measuring the contrast loss due to the resist itself. The practically unlimited depth of focus in IL makes the experiments and analysis particularly simple in comparison to a projection system.

Several photoresists were exposed using our EUV-IL tool with a number of different pitches in the range of 40 to 200 nm over a range of exposure doses. SEM images of the patterns were taken for linewidth measurements. An edge detection software was used to determine the change in linewidth as a function of dose. In this way the exposure latitude is determined and can be compared to the theoretically expected performance of the EUV-IL tool. The normalized image log-slope (NILS) of the image in an interference lithography setup is a constant and equal to pi. Deviation of the measured contrast in photoresist images from that predicted by the constant NILS is either due to the resist contrast loss or imperfections in the aerial image due to factors such as mechanical stability or scattering due to roughness on diffraction grating lines. In this paper we present analysis of resist images and possible contributions due to factors that limit the contrast in the interference setup. The photoresist results are compared to images obtained on an EUV projection scanner.

7636-110, Poster Session

Measurement of EUV resists performances RLS by DUV light source

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Recently published experimental results indicate that current resists seem to be very hard to meet the International Roadmap for Semiconductors (ITRS) goals for Resolution, Line Edge Roughness (LER) and Sensitivity (RLS) simultaneously. This RLS tradeoff has also been demonstrated through modeling work. RLS goals may not be possible to achieve all three simultaneously by applying current standard chemically amplified resists and processes. In this paper, we have synthesized the various polymers for different protecting group, inert group and other molecular weight (Mw). We use DUV light to explore the impact of DUV contrast on the RLS relationships in EUV performances. We have measured Eth, tan and LER in DUV patterning process and correlated them with those obtained in EUV process. By using DUV light source we have setup EUV resist pre-screening and improving method.

7636-111, Poster Session

Study of post-develop defect on typical EUV resist

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This study reports on post-develop defect on typical EUV resist system. Now EUV resist is in the development stage for the resolution, sensitivity, LER and so on. During past transition, i-Line, KrF, ArF and Immersion ArF, it was confirmed there were a large number of defects

on the wafer. However, kinds of defect are 2 or 3 types and these defects were solved with improving the resist.

In this work, we confirm and show the defect types on typical EUV resist. We evaluated the defect appearing conditions, for example pattern type, layout of exposed area on the wafer and develop process.

Lastly we discuss the solution approach by past defect types which we gained experience in the past resist under development from i-Line to Immersion-ArF.

7636-112, Poster Session

Investigation of wafer track-related EUV process sensitivities

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As Extreme ultraviolet (EUV) lithography technology shows promising results below 40nm feature sizes, TOKYO ELECTRON LTD.(TEL) is committed to understanding the fundamentals needed to improve our technology, thereby enabling customers to meet roadmap expectations. TEL continues collaboration with IMEC for evaluation of Coater/Developer processing sensitivities using the ASML Alpha Demo Tool for EUV exposures. The results from the collaboration help develop the necessary hardware for EUV Coater/Developer processing. In previous work, process sensitivities for several resists such as critical dimension (CD) uniformity, defectivity versus resist material hydrophobic was investigated [1]. In this work, new promising resist materials have been studied. Specifically, post exposure bake impact to CD is studied in addition to dissolution characteristics and resist material hydrophobicity. TEL uses a background of simulation and modeling on EUV resist systems in conjunction with fundamental processing knowledge in order to further our understanding of processing sensitivities and any corresponding deviations against known sensitivities.

[1] Bradon, N. et. al., “Investigation of EUV process sensitivities for wafer track processing” SPIE Vol. 7271-154, (2009)

7636-113, Poster Session

Cobalt-containing polymers as patterning assist layers in EUV lithography

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As part of the ongoing research projects in our group, in this presentation we communicate the use of cobalt-containing polymers as materials in EUV lithography. Although the application of these metal-containing polymers as photoresists is not excluded, the presented work describes their utility as underlayers or patterning assist layers (PALs) in conjunction with an ESCAP polymer for EUV lithography.

Introducing cobalt in organic structure through the coordination to an alkyne group is a well-known reaction in organometallic chemistry and recently extended to macromolecular structures. The cobalt-containing polyester was synthesized in a two step process via polycondensation followed by the treatment of resulting polymer with dicobalt octacarbonyl (Scheme 1). This synthetic pathway permits the preparation of fully or partially coordinated polymers with a cobalt loading controlled by the molar ratio of dicobalt octacarbonyl to monomeric units.

Thermal properties of these cobalt-coordinated polymers are characterized by a transition around 100 C assigned to a crosslinking process which prompted us to consider them as versatile candidates for new EUV underlayers. Preventing intermixing with the photoresist upon sequential coating is one of the requirements for the materials designated to such applications. Since the investigation of reticulated polymer is hindered by its limited solubility, the crosslinking process was studied by reaction of model compounds of the polymer repeating unit (Scheme 2). Thermal analysis coupled with mass spectrometry in addition to FTIR, ToF-SIMS and XPS were used to characterize the formation and final state of the cross-linked films.

The benefits of using cobalt-containing polymers as PAL’s were explored using the EUV sources at LBNL and PSI using a common ESCAP photoresist. Positive and negative impacts of these underlayers on the resolution, LER, and photospeed of the photoresist is presented. Specifically, photospeed enhancements are observed as the amount of Co increases in the underlayer suggesting a direct role of these underlayers on the lithographic process. The potential utility of these materials as wet developable underlayers is also described.

7636-114, Poster Session

Development of novel positive-tone resists for EUVL

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The critical issues of EUV resist are low Line Edge Roughness (LER). Required LER value is less than molecule size of base resin, thus molecule size control is required in the pattern width control.

In the previous paper [1], it was demonstrated that Cyclic Low Molecular Resists (CLM-Resist) had good performance under Electron beam and EUV lithography. But the substituted site and number of protecting group obtained by this reaction is ‘random’.

Recent research indicates that controlling the distribution of the protecting groups in a molecular resist material has a great impact on improving LER.

To bring out the lithographic performance of CLM-resist, we designed and synthesized new CLM-resist, ‘CLMC-resist’, for which there is no variation in the position and number of protecting group. The protected site and the number of protecting group in CLMC-resist are completely regulated. This result means that CLMC-resist is uniform both molecular size and composition.

We have evaluated their EB and Extreme Ultraviolet (EUV) patterning performance. The EUV lithographic evaluation of the novel low molecular resists was carried out at SFET (small field exposure tool) in Semiconductor Leading Edge Technologies Inc. (Selete). Newly synthesized resists have shown high performance of sensitivity and resolution under EB or EUV exposures.

In this conference, we outline the design of new low molecular resists. The material properties, photochemistry and the patterning capability of these newly synthesizes low molecular resists are reported.

(1) T.Owada, et al. Proceedings of SPIE Vol.6923, 692346, (2008)

7636-115, Poster Session

Alternative resist processes for LWR reduction in EUVL

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EUV lithography (EUVL) is the leading candidate for the manufacture of devices with 22nm node and beyond. However, many challenges remain for the industry to understand clearly and to overcome before EUVL will be ready for application in volume production.

Efforts have been made to improve the various critical components of EUVL, such as light source, exposure tool, mask, resist material, and so on.[1] Among these, resist materials are considered as one of the most critical issues in realizing EUVL. In EUV resist material development, three factors; sensitivity, resolution limit and line-width roughness (LWR), have been known to have trade-off relationships and consequently, should be concurrently achieved. Among these factors, LWR is viewed as a possible major issue as pattern sizes reach the molecular level of the common resist materials presently used. Thus, the investigation of LWR-reduction from the point of view of resist processing becomes necessary.

Many research in resist material improvement are continuously being investigated for LWR-reduction.[2] Meanwhile, some groups have started working on resist process enhancements as possible solutions

for LWR-reduction.[3]

In Selete, initial work on resist process enhancements such as post application bake (PAB) and post exposure bake (PEB) in-vacuum, alternative rinse and developer solutions have been started.

At present, the following results have been obtained. PAB and PEB in vacuum were observed to have no significant effect on sensitivity, resolution while achieving a 20% improvement in LWR (7.8nm improved to 6.1nm). However, a difference in resist lithographic performance depending on the type of resist material used was observed between resist processes performed in-atmosphere and in-vacuum. With the application of alternative aqueous rinse solutions as a replacement to the commonly used de-ionized water (DIW) in the after-development rinse process, an 46% improvement in the LWR of a molecular resist at hp 45nm (10.3nm improved to 5.6nm) was achieved. It was also found that the importance of resist and rinse solution compatibility should be considered. Moreover, work on the evaluation of new developer solutions such as the tetrabutylammonium hydroxide (TBAH) as an alternative to the standard tetramethylammonium hydroxide (TMAH) solution was performed. Minimal or no effect on sensitivity and resolution limit was observed with the application of each developer type. Resist swelling was also non-existent. LWR at 32nm 1:1 L/S was improved by 20% (9.0nm 7.2nm) using the TBAH developer solution.

During the conference, further updates regarding the optimization of resist processing techniques for EUVL will be presented.

7636-116, Poster Session

Scissionable polymer resists for extreme-ultraviolet lithography

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A new type of scissionable polymer based on main-chain acid labile acetal linkages is reported as a resist for e-beam and EUV lithography. Copolymers were synthesized via ring-opening metathesis polymerization (ROMP) using various ratios of cyclic acetal and norbornene-type monomers. A critical issue for these lithographic processes was the high level of ruthenium content (0.2 %) found in the isolated copolymers. The problem was successfully overcome and Ru amount reduced to ppm level. The dependence of the Tg on the norbornene-derivative/acetal ratio was established by differential scanning calorimetry (DSC). As expected, copolymers with high Tg could be prepared by incorporation of bulky structure. According to thermogravimetric analysis (TGA), the copolymer with the highest Tg, had an on-set temperature for thermal decomposition around 100 C. This transition was asigned to a depolymerization process due to the presence of the acetal units, restricting both PAB and PEB temperatures to values below 100 C. Investigations by means of GPC, NMR and FT-IR, showed that the main-chain in the copolymer was cleaved on the acid-labile acetal in presence of photo-generated strong acids in both solution and thin-films. These properties are utilized to explore the synthesized polymers as candidates for positive-tone lithography systems. Results of patterning using both e-beam and EUV will be presented.

7636-130, Poster Session

Sensitive polycarbonate non-chemically amplified photoresists for extreme ultraviolet lithography

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A structurally diverse range of aliphatic tertiary polycarbonates with high glass transition temperatures have been prepared. Our previous studies, where we screened a variety of functional groups, have demonstrated that the tertiary carbonate groups have a high propensity to degrade when exposed with EUV photons. These materials have been assessed for their potential to be used as non-chemically amplified resists, where the molecular weight of the polymer decreases during exposure to EUV as a result of polymer chain scission, i.e. there is a molecular weight rather than a polarity-based solubility switch. The materials have passed outgassing limits with the primary species being carbon dioxide. The E0 values for these polymers were found to be significantly lower than PMMA and the most promising materials have been imaged at the Advanced Light Source, where features as small as 29 nm were written at 50 nm half pitch.

7636-117, Poster Session

Comparison of EUV spectral and ion emission features from laser-produced Sn and Li plasmas

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Extreme ultraviolet (EUV) lithography operating at 13.5 nm will take over optical lithography in the coming years. The selection of a 13.5 nm wavelength source is based on the advent of Mo/Si multi-layered mirrors (MLMs) that reflect 13.5 nm light with 4% bandwidth. The leading light sources of 13.5 nm radiation are laser-produced plasmas (LPP) and discharge-produced plasmas (DPP) and the target elements of interest are Sn, Xe, and Li. Among these targets, Sn and Li provide highest conversion of laser to in-band (13.5 nm with 2% bandwidth) energy. In this paper, we report a comparison of spectral and ion emission features from Li and Sn laser-produced plasmas.

Planar slabs of pure Sn and Li were irradiated with 1064 nm, 9 ns Nd:YAG laser pulses. The resulting plasmas were evaluated with an absolutely calibrated EUV power tool, a transmission grating spectrograph, a pinhole camera, and a Faraday cup. These diagnostic tools have allowed us to determine EUV conversion efficiency (CE), EUV spectral emission features, plasma EUV emitting size, kinetic energies, and ions flux. We evaluated the above features at various laser intensities for both Sn and Li plasmas. The Li2+ Lyman- line and Sn8-13+ lines generate the in-band emissions of Li and Sn. The intensity of Li2+ lines was found to increase with laser intensity. However, the Sn UTA showed remarkable changes with laser intensity, including appearance of satellite peaks, and a spectral dip at higher intensities. EUV images of the plasma showed that Sn plasmas take on a conical shape, as opposed to the hemispherical shape of Li plasmas. Ion debris analysis showed the kinetic energies for Li ions are lower than that of Sn ions under similar experimental conditions. Kinetic spread of Li ions has been found to be narrower compared to the kinetic energy distribution of the Sn ions. We also compared the ion flux emitted by Sn and Li plasmas.

7636-118, Poster Session

Time-resolved studies of laser-produced plasmas of tin

T. D. McCormack, Univ. College Dublin (Ireland)

Currently one of the most promising sources for 13.5 nm lithography is a laser produced plasma of Sn. Understanding the processes involved is one of the major roadblocks towards developing a commercial source at this wavelength. We report on time resolved studies of the light emitted in the 50 to 150 Å range when the output from a high power Nd:YAG laser is focussed on solid targets of tin. A fast gateable MCP coupled to an EUV spectrometer and a digital camera have been used to determine the dominant ion stage as a function of time during the evolution of the plasma. Gate widths of 5, 10 and 50 ns were used to capture the plasma at a range of times between 0 and 100 ns. The main properties of the set up are reported.

7636-119, Poster Session

Status of ETH Zurich high-power LPP EUV source

R. S. Abhari, ETH Zürich (Switzerland)

ETH Zurich has been actively developing a high power LPP source with application for actinic EUV metrology and lithography tools. The source focuses a high-powered pulsed laser on droplets of Tin at frequencies of up to 10 kHz. The fully integrated system operates with a drive laser, a tin dispenser, a multi-layer coated normal incidence collector with integrated thermal management and debris mitigation system, a droplet targeting system, and a debris-free system interconnect at the intermediate focus point. All these components are operating within a fully integrated system. This presentation will introduce the system and its salient features.

The 10 kHz-rate source dispenses Tin droplet targets into the high vacuum environment. Small droplets minimize the amount of debris, and are generated in synchrony with the pulsed laser. Droplet generation must be reproducible in size, with stable frequency and controllable speed. The conversion efficiency and debris profile of an EUV source depends strongly on droplet quality. At ETH Zurich, a novel patent pending system generates highly reproducible pure tin droplets, with advanced thermal management for stable long-term operation. The short- and long-term droplet train deflections, as well as the timing jitter at the target irradiation site are compensated by the tracking and targeting system. A specially designed opto-electronics module synchronizes the firing of the laser with the arrival of the target droplet.

The 1.2 π sr. normal incidence collector optics is designed with a Si/Mo multi-layer coating. The collector has an integral thermal management system tailored to match the incoming heat flux, minimizing the slope error of the mirror. By measuring and computing the debris load on the collector, a novel-design debris mitigation technique has been designed and deployed. This system combines an electromagnetic field together with a patent-pending gas curtain integrated with the collector optics.

The development of this integrated source collector module is facilitated by in-house multi-scale computational tools, used to simulate the dynamic LPP operation from the target-length scale (µm) up to the optics-length scale (m). This multi-scale suite of computational tools examines issues of collector lifetime, debris load and radiation conversion efficiency. In synergy with companion experiments for full-scale verification, these computational tools have accelerated the development of the EUV light source.

Integration of all the modules has been a primary consideration, to operate as a fully automated system with flexible operation, low cost of ownership and ease of maintenance. An array of various sensors is deployed to monitor the operation of the module. Finally, results from in-band measurements as well as the initial assessment of the collector optics lifetime will be presented.

7636-120, Poster Session

Laser-produced plasma lightsource for EUVL

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This paper describes the development of a laser-produced-plasma (LPP) extreme-ultraviolet (EUV) source architecture for advanced lithography applications in high volume manufacturing. EUV lithography is expected to succeed 193nm immersion technology for sub-22nm critical layer patterning. In this paper we discuss the most recent results from high EUV power testing and debris mitigation testing on witness samples and normal incidence collectors, and describe the requirements and technical challenges related to successful implementation of the technology. Subsystem performance will be shown including the CO2 drive laser, debris mitigation, normal incidence collector and coatings, droplet generation, laser-to-droplet targeting control, intermediate-focus (IF) metrology and system use and experience. In addition, a multitude of smaller lab-scale experimental systems have also been constructed and tested. This presentation reviews the experimental results obtained on systems with a focus on the topics most critical for an HVM source.

7636-121, Poster Session

High-brightness EUV light source modeling

S. V. Zakharov, EPPRA SAS (France); P. Choi, NANO-UV SAS (France); V. S. Zakharov, EPPRA SAS (France)

The selective EUV source for the actinic mask defect review and metrology to support pilot line EUVL operation is very different compared with the HVM Litho source with substantially higher EUV brightness to produce higher irradiance (power density) at IF and much smaller etendue to match the projection magnification and illumination field size. The self-absorption limits the in-band EUV radiance of the source plasma and etendue constraints limit the usable power of a conventional single unit EUV source. The in-band EUV radiance limits depend on atomic characteristics of emitting plasma and amount of transitions inside the necessary narrow spectral bandwidth. Unresolved transition array (UTA) 4f-4d of a bunch of ions from SnVIII to SnXIII emits into 2% bandwidth around 13.5nm for EUVL from the tin plasma, but only one transition 5p-4d in the ion XeXI emits into that band from xenon plasma of a conventional selective EUV source. The self-absorption limits the selective EUV brightness from xenon plasma at much lower radiance level than from the tin plasma. Previous papers have identified that the xenon source EUV brightness can be increased if to use the set of satellites and resonant transitions in highly charged Xe XVII - Xe XXXI ions under certain conditions. A theoretical model and robust numerical modeling tools are developed under international collaboration in the frames of FP7 IAPP project FIRE to model atomic properties and dynamics of the non-equilibrium multicharged ion plasma with nonmaxwelian electron distribution. Extensive numerical modeling is carried out to address fundamental issues in EUV plasma sources and to optimize the performance of the source. The plasma parameters providing high in-band emission for minimum energy input are in a very narrow range of values. In particular, it has been found that highly ionized xenon plasma of a micro-pulsed plasma under presence of fast electrons demonstrates a unique feature: the cumulative emission near 13.5 nm from Xe XXI to Xe XXIV ions produced in the plasma by fast electrons significantly exceeds that one from Xe XI ions of conventional xenon based EUV source. Due to larger amount of in-band transitions and higher plasma temperature the plasma self-absorption limits the selective radiance at a higher level than conventional xenon or even tin EUV sources.

Nano-UV is delivering a new generation of EUV light source based on a nanosecond, ultra fast micro-plasma capillary discharge with an in-built plasma structure for photon collection and projection. The micro-plasma pulsed discharge and photon collection structure are induced by an intense electron beam generated due to the transient hollow cathode effect. Parametric scan modeling has provided basic numbers to select the optimal regime for xenon based source performance. It was proposed that such a source could form the basic building block for EUV metrology source. Due to the very low etendue and the compact form factor of each unit the required selective source EUV brightness and resulting EUV power can be achieved by spatial multiplexing, using multiple source units. The spatial coherence of the source allows the EUV interferometer for metrology and for resist patterning to be made.

7636-122, Poster Session

High-brightness EUV light source unit for EUV interferometer and metrology

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The top challenges to EUVL deployment are the availability of a

powerful and reliable light source in 2% bandwidth around 13.5nm spectral wavelength along with the associated optics to collect the EUV photons, the so called SoCoMo (source collector module). To support pilot line operation and EUVL transition into manufacturing, a commercial EUV aerial imaging microscope (AIM) and actinic inspection tool will be required for mask defect review. The EUV source for the AIM tool is very different compared with the HVM Litho source with substantially higher brightness, higher irradiance (power density) and much smaller etendue to match the projection magnification and illumination field size. The self-absorption and etendue constraints limit the usable power of a conventional single unit EUV source. Previous papers have identified that the required irradiance can be achieved by spatial multiplexing, using multiple sources.

NANO-UV is delivering a new generation of EUV light source with an intrinsic photon collector, the i-SoCoMo concept, where an impulse micro discharge plasma source is integrated to a photon collector, based on an in-built active plasma structure (PlasmaLens). By performing extensive numerical modeling of the plasma dynamics and radiation the performance of the source was optimized. We present here experimental results from CYCLOPS, a commercial unit incorporating the i-SoCoMo technology. The micro-plasma pulsed discharge and PlasmaLens structure are induced by an intense electron beam generated due to the transient hollow cathode effect. At the same time the fast electrons shift the ionization equilibrium to necessary ionization degrees providing high in-band emission intensity. The CYCLOPS source, working in a multiple-kHz regime with a mixture of He:Ar:Xe, possesses exceptional irradiance without the use of external physical optics, and delivers more than 0.15 W/cm2 to a mm2 spot over 60 cm away from the source at the EUV band, with an etendue below 10-4 mm2.sr providing the radiance at the IF of more than 110 W/mm2.sr. It is proposed that such a source could form the basic building block for an ideal EUV metrology source. The spatial coherence of the source allows an EUV interferometer for metrology and for resist patterning to be made. Due to the very low etendue and the compact form factor of the i-SoCoMo source, the higher irradiance for aerial imaging requirements can be obtained by spatial multiplexing of multiple units, the HYDRA design.

7636-123, Poster Session

Present status of laser-produced plasma EUV light source

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The development status of the key technologies for a HVM laser produced plasma EUV light source will be presented. This includes the high-power RF-excited CO2 laser, the Sn droplet target and the collector mirror lifetime enhancement (debris, ion mitigation) technology. The laser system is a master oscillator power amplifier (MOPA) configuration. We have achieved a maximum average laser output power of more than 10 kW at 100 kHz and 20 ns pulse by a single laser beam with good beam quality. A superconductivity magnet have installed for the plasma guiding for a real scale mirror lifetime enhancement test.

Experiments that support the development, e.g. >30% duty long term CO2 laser system operation, are currently being performed. The drift of the droplet target was reduced to maintain stable EUV pulse energy, the ion flux from the Sn droplet plasma was confined along the magnetic axis.

Detail of the key technologies and the general outline of the system development towards >115/180 W will be given. A part of this work was supported by the New Energy and Industrial Technology Development Organization (NEDO), Japan.

7636-124, Poster Session

Modeling of atomic and plasmas processes in the LPP and LA-DPP EUV source

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The numerical simulation of the EUV source is useful for the analysis of the experimental results, to identify the pumping conditions to obtain more than 180W of output EUV power with high efficiency. We investigate the conversion efficiency and emission spectrum from tin LPP source using the radiation hydrodynamics simulation. We show results of studies of the detailed atomic processes both applicable to the LPP and LA-DPP EUV sources.

We perform calculations of level population of tin by solving collisional radiative equations, including a large number of atomic states of near 10 times ionized tin, and then the emissivity and opacity of the plasma are calculated over a density and temperature range of the plasma used for the EUV source. We verify the results in terms of both the atomic data and atomic model, because the results of the simulation critically depend on the accuracy of the emissivity and opacity data. The calculated spectrum assuming LTE plasma, now agree well with experiments including the structure of side peaks corresponding to 4d-4f and 4d-5f transitions from lower charge states (Sn7+) [1,2]. Reasonable agreement has also been obtained in terms of the absorption spectrum, after taking the effect of configuration interaction (CI) to the transition probabilities into account [3].

We calculate atomic data such as energy levels and radiative transition probabilities using the Hullac code. Although, the code usually provides atomic data with reasonably accuracy, calculated transition energy differs 3-5eV from experiment in the case of the 4d-4f resonance lines of near 10 times ionized tin. We corrected the transition energies of the resonance lines according to the measurements using the charge exchange spectroscopy [4]. Furthermore, we carry out iterative calculations of population kinetics as well as the emissivity and opacity of the plasma, by changing the set of atomic energy levels. Tin ions have a large number of multiply excited states, which have emission in the EUV wavelength region through 4d-4f | 5p | 5f and 4p-4d transitions. After comparison of the calculated emission spectrum with those from various EUV sources, it is found that not only the resonance lines such as 4di-1(4d-4f) and spectator satellite lines as 4di-2(4d-4f) nl, but inner shell satellite lines such as 4p54di(4d-4f) have significant contribution to the EUV emission. It is also found that transition energies of inner shell satellite lines subject to the significant effect of CI. We show that most of these lines should appear in the longer wavelength side of the 13.5nm band, to reproduce the experimental spectra.

We also report modeling studies of initial state of discharge for the LA-DPP EUV sources. Preformed plasmas produced by the laser irradiation are expected to be useful to have a stable discharge. We propose a new approach based on the percolation to model initial stochastic properties of discharge.

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7636-125, Poster Session

In-situ EUV plasma debris mitigation

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A challenge in the implementation of extreme ultraviolet (EUV) light photolithography in production tools is the accumulation of fuel debris on the collector optics near the plasma pinch region. This debris presents a challenge to the lifetime collector optics. Most debris mitigation processes investigated thus far have had trouble with selectivity; they require highly reactive gases that will degrade the

optics and chamber infrastructure in the removal process. In addition, the current cleaning gases have low transmission for the EUV light, eliminating in-situ operation as an option. An investigation into a new approach is researched by the Center for Plasma Material's Interactions (CPMI) at University of Illinois in Urbana. This unique concurrent plasma process mitigates EUV produced debris from accumulating on the collector optics surface at room temperature without damage to the underlying collector optics composition. The advantage to this plasma process is that it operates in situ and does not require offline time of the tool. A computer model of the plasma debris mitigation system has been developed and correlated to experimental results. This expansive model takes into account the coalitional cross sections of the input gas particles along with energy, density, flux and temperature dependence. The cross sections are developed from past research data on particle-particle interactions and are numerically integrated into the computer model. Interactions are initially set to related material specifications as this process is relatively new and unexplored. Comparison to experimental data allows for changes to the surface interaction inputs in the model. The developed procedure show great selectivity for specific debris mitigation. Variances are explored as to optimize the cleaning process. These results validate this as process as a viable pathway towards an in-situ cleaning process or a quick cleaning cycle in the EUV lithography process.

7636-126, Poster Session

Multiscale simulations of LPP-EUV sources

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The 13.5nm light source, required for extreme ultraviolet lithography (EUVL) is typically based on a laser produced plasma (LPP). In order to be applied in high volume manufacturing or in metrology, an EUV source must be stable and meet the power requirements at intermediate focus. Component life-time is today limited by the laser plasma debris load. As current sources do not fulfill the required number of operating hours, efficient debris mitigation strategies, which do not decrease EUV emission, must be developed.

In the plasma science facility at ETH Zurich novel debris mitigation techniques are being studied. Tin droplets are irradiated by a Nd:YAG laser. This facility is equipped with a 3D mapping system, which measures the spatial & temporal distributions of radiation and particle fluxes over 4π sr, the in-band & full-band emissions, as well as the heat load on the collection optics.

At SPIE 2009, we computationally examined the life-time of the collection optics, without debris mitigation, Fig. 1. In the present work, we extend this work further by examining critical operational issues of an LPP source with debris mitigation. These issues include, amongst others, the effect of target focusing/defocusing on conversion efficiency. The simulations are accomplished using our multi-scale computational tool set that consists of a hydrodynamic and a particle code, and which can model the expansion of the LPP over the very different length scales, ranging from the target size (10-6m) up to the mirror diameter (10-1m). The hydrodynamic code models the initial laser-target interaction as well as emissions at all relevant wavelengths. The particle code combines a particle-in-cell (PIC) and Direct Simulation Monte Carlo (DSMC) code. The boundary conditions for the particle code are provided through an unsteady interface on which sampled particles with Maxwellian distributions are determined from the hydrodynamic code.

The validated computational tools are used to predict an optimum laser/target configuration. The figures-of-merit include conversion efficiency, hence EUV power and collector heat load, as well as debris load. The computed highly resolved temporal and spatial distributions of both, ion and neutral debris, as well as EUV emission and out-of-band radiation, relevant for calculations of the heat load on the EUV collector, are obtained for the optimum laser/target configuration used in the dedicated test facility. The computational results improve our fundamental understanding, and in turn facilitate the accelerated development of EUV sources for both, HVM and metrology applications.

7636-127, Poster Session

Stability improvement of EUV source by advanced alignment system for collector module

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For commercial EUV (extreme ultraviolet) exposure tools, a SoCoMo (source collector module) with stable EUV light through the IF (intermediate focus) is absolutely necessary. EUV light characteristics through the IF such as power distribution or angular distribution are fluctuated by thermal deformation of the collector, degradation of collector mirror reflectivity, and displacement of plasma position.

The angular distribution stability at the IF is considered to be especially important. Therefore, an automatic alignment algorithm to compensate the change in angular distribution has been developed. Also, an angular distribution monitoring system has been fabricated. In the alignment algorithm, fuzzy logic is applied and a learning function is also implemented to reduce the time for alignment. Our angular distribution monitoring system can be installed in the SoCoMo, since a special designed filter is used to select the significant EUV rays. Any monitor is not needed inside the exposure tool.

It has been demonstrated that a deteriorated angular distribution returned to an initial distribution within one minute by adjusting the collector position with the alignment algorithm and with the monitoring system.

The concept of our automatic alignment system and its configurations will be shown, and the experimental results will be presented in detail.

This work was supported by NEDO, Japan.

7636-128, Poster Session

High-brightness NGL multiplexed EUV light source for EUV metrology and defect inspection

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Implementing EUV lithography, while scaling down to sub 22nm node, is considered as leading technology. Mask inspection tools are becoming a yield limiting optical element within the litho-imaging path, leading to a paradigm shift for the EUV. While several approaches have been attempted to satisfy technical criteria, a major issue remains in satisfying industrial solutions.

The unique approach developed at NANO-UV of spatial multiplexing the brightest existing source as a core device, is an enabling technology for manufacturing zero-defect masks solution as actinic, in-die metrology. This leads to the HYDRA product series.

The HYDRA system configuration relies on 12 GEN II CYCLOPS TM cells operating in sequential or simultaneous mode, using a gas mixture of He/Ar/Xe. Each unit operates at 5 kHz leading to a 60 kHz operation. Small cross talk, plug and play handling, low maintenance time and low downtime were the main objectives and key-parameters when designing, assembling and testing the system. The time averaged emission properties of each source unit show the radiance at IF to be more than 110 W/mm2/sr with an emission angle of 9.5 10-5 steradian and with an etendue of less than 10-4mm2/sr. Using spatial multiplexing of 8 - 12 units, an active optic will allow the time averaged brightness at IF, as well as the irradiance to be increased by 8 - 12 times with a high efficiency of ~ 90%.

A configurable pupil fill is uniquely incorporated on HYDRA, with expected performances such as, a low etendue of < 10-2 mm2.sr, an illumination field size of 0.01 to 1 mm2 and an irradiance of 1018 ph/cm2/s. Details of the source properties will be presented.

Particular care has been taken in thermal management, by running the

equipment during hours of non-stop operation, thereby showing it to be a very stable system. No degradation of illumination signal has been observed, thanks to the in built photon collection & projection plasma structure, the intrinsic-SoCoMo. Gigashot lifetime is expected at 5kHz operation, as well as print sampling to assess the HYDRA performance.

HYDRATM, is dedicated to satisfy throughput criteria, stability, reliability, reproducibility and lifetime.

7636-129, Poster Session

Aerial image improvements on the Intel MET

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Since its installment in 2004, Intel's Extreme Ultraviolet (EUV) Micro Exposure Tool (MET) has demonstrated significant improvements in its ultimate resolution capability. Initially capable of printing 45nm half-pitch (HP) lines with a 160nm depth of focus (DOF), it is now printing 22nm HP lines with a 300nm DOF and demonstrating modulation down to 18nm HP. While initial improvements in resolution have been chiefly attributable to the maturation of EUV photoresists, the most recent improvements that have enabled the 22nm HP imaging with a sizeable process window are largely due to new illumination options that have become available as a result of source-collector (SoCo) upgrades. In particular, the installation of a new nested Wolter-collector with an additional outer shell has extended the maximum outer sigma from 0.55 to 0.68 and thus enabled new cross-quadrapole and on-axis dipole illumination settings with 0.36 inner sigma and 0.68 outer sigma. Here we present simulated contrast curves alongside the latest experimental imaging results for the Intel MET using the newly available quadrapole and on-axis illumination settings and discuss our future plans for continued improvements to the Intel MET aerial image.

7636-51, Session 11

Nikon EUVL development progress update

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Extreme Ultra Violet Lithography (EUVL) is regarded as the ultimate lithography technology for semiconductor device manufacturing after ArF immersion lithography and the most promising technology from 22nm hp node. With such significant decrease in wavelength from 193nm to 13.5nm, the imaging system needs all reflective mirror optics and vacuum exposure environment. There are important technology areas to be developed such as reflective mask, resist, and exposure tool including light source in order to realized EUVL as high volume manufacturing lithography technology. The reflective mask should feature such characteristics as pellicleless, ultra-smooth blank flatness and defect free. The resist should be of high sensitivity and small line edge roughness (LER) as well as fine resolution. Contamination control of optics is one of the critical issues of EUV exposure tools. Because EUV photons have much higher energy than photons of conventional optical lithography, they easily induce chemical reactions, which lead to carbon deposition and oxidation, called contamination of optics. These contamination causes decrease of transmittance and degradation of optical performance.

Regarding projection optics development, Nikon has developed state-of-the-art polishing technologies, multi-layer coating technologies and new ultra high-precision interferometers for aspheric surface metrology. The latest projection optics has achieved the remarkable performance with the wavefront error of 0.4nmRMS and flare of 8%. The Mo/Si multi-layer coating technology has been also improved for not only projection optics but also illumination optics.

As to EUVL elementary and infrastructure developments, Nikon has been collaborating with Selete (Semiconductor Leading Edge Technologies, Inc.), EUVA (Extreme Ultraviolet Lithography System Development Association) and other organizations for mask related development, light source development, optical metrology development, and contamination prevention technology development. Since contamination control technology to prevent carbon deposition and oxidation on mirror surfaces is critical, Nikon established a new EUV irradiation test facility at "Saga Light Source" in Kyushu to facilitate experimental works.

Nikon has been developing the full field exposure tool called EUV1 for early process development for 32nm hp node. EUV1 was installed in Selete and used for EUV lithography process development. Nikon also has conducted continuous collaborative work with customers. Since the last SPIE Symposium in 2009, many exposure results taken on EUV1 tools were achieved. They showed excellent resolution capability down to 25nm L/S and overlay capability of 10nm (Mean + 3 sigma). Exposures of test chip patterns for process development are ongoing.

Nikon has considered the development scenario of high volume manufacturing tool for 22nm hp device node and beyond with high NA >0.3 optics. EUV light source development and mask infrastructure development are currently considered as most critical issues for EUVL development.

7636-52, Session 11

EUV into production: update on ASML's NXE platform

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The presentation will give an update on the integration status of ASML's NXE platform and the challenges of bringing EUVL tools into production manufacture.

The NXE is a multi-generation production EUVL system platform that builds on TWINSCAN technology and the designs and experience gained from the Alpha Demo Tools (ADTs) currently in use at two research centers for EUVL process development.

Shipping in 2010, ASML NXE:3100 will be the 1st generation of the EUVL production exposure platform. With an NA of 0.25 and a resolution of 27nm this tool is targeted for EVL implementation into production fabs and early volume production at the 27nm node. Following the development and manufacturing approach used on other systems, modules are tested separately for performance and functionality, then integrated, followed by system level functionality and performance testing. In this talk we will highlight the key features of the system including the manufacturing status and performance data of optics and source, and the results of wafer flow and reticle flow testing. The latest status of the system integration will be shared along with the challenges encountered.

The presentation will also give an outline of the 2nd generation, a 0.32NA exposure tool including EUVL off axis illumination for resolutions down to 16nm. Further extension by higher NA will briefly be discussed as well.

7636-53, Session 11

LPP source system development for HVM

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Laser produced plasma (LPP) systems have been developed as the primary approach for the EUV scanner light source for optical imaging of circuit features at sub-22nm and beyond nodes on the ITRS roadmap. This paper provides a review of development progress and productization status for a LPP extreme-ultra-violet (EUV) source with performance goals targeted to meet specific requirements from leading scanner manufacturers. We present the latest results on power generation, stable collection, and clean transmission of EUV through the intermediate focus. Semiconductor industry standards for reliability and economic targets for cost of ownership will be provided. We report on measurements taken using a 5sr collector optic on a production system. Power transmitted to intermediate focus (IF) and out-of-band

(OOB) measurements will be shown. The lifetime of the collector mirror is a critical parameter in the development of extreme ultra-violet LPP lithography sources. Deposition of target material as well as sputtering or implantation of incident particles can reduce the reflectivity of the mirror coating during exposure. Debris mitigation techniques are used to inhibit damage from occuring, the results of these techniques will be shown.

7636-54, Session 12

Development status of Canon's EUVL exposure tool

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Canon's latest EUVL tool roadmap and the development status of EUVL exposure tool will be presented.

To achieve required printing quality for 22 nm generation and beyond, wavefront error and flare of projection optics must be extremely suppressed. Mirror surface figuring and multilayer deposition are key technologies for such high precision optics.

We have improved mirror surface figuring techniques corresponding to each spatial frequency ranges. The results of our figuring technologies will be presented.

To suppress wavefront error of projection optics, not only thickness of multilayer but also the phase difference of reflected EUV light must be well controlled. We developed novel measuring method of phase difference of reflected EUV light on a multilayer mirror. Using the measuring method to the mirrors of projection optics, wavefront error of projection optics can be evaluated.

Optics contamination is a critical issue for optics lifetime of EUV projection optics. The issues are oxidation of multilayer mirror by water and carbon deposition of ML mirror by hydrocarbons.

Anti-oxidation capping materials were screened for mitigating oxidation of MLMs under the EUVA (Extreme Ultraviolet Lithography System Development Association) program. Cleaning methods for etching deposited carbon, irradiating ultraviolet light with oxidation gas or injecting atomic hydrogen, is developed. Additionally, we have to suppress carbon deposition for reducing downtime of EUVL exposure tool. There is a possibility that carbon deposition is mitigated by injecting oxidation gas during EUV irradiation. The experimental results for mitigating carbon deposition by injecting oxidation gas will be presented.

7636-55, Session 12

The SEMATECH Berkeley MET pushing EUV development beyond 22-nm half pitch

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Microfield exposure tools (METs) have and continue to play a dominant role in the development of extreme ultraviolet (EUV) resists and masks. One of these tools is the SEMATECH Berkeley 0.3 numerical aperture (NA) MET. Using conventional illumination, however, this tool is limited to approximately 22-nm half pitch resolution. Here we describe and demonstrate resolution enhacement techniques capable of pushing the SEMATECH Berkeley MET beyond this limit. We consider illumination-, system-, and mask-based techniques. In all cases, however, increased levels of coherence are used, which introduces the additional problem of increased sensitivity to mask multilayer roughness. Modeling and experimental results demonstrating this limitation are presented.

We use the methods described above to demonstrate patterning at the sub-22-nm level and summarize the latest resist performance results, including resolution, line edge roughness (LER), and sensitivity. Noting that the coherence limitations described above introduce significant LER, we also provide an update on mask contributions to LER under the various illumination conditions for resolution enhancement and discuss specifications for future MET masks that would allow the effects to be mitigated.

Ultimately, development at the sub-22-nm half pitch level will require a higher NA MET. We will conclude the presentation with a discussion of the design and capabilities of a 0.5-NA Schwarschild-like optic that would serve as the heart of a new MET installed at the Advannced Light Source synchrotron facility. As with the current SEMATECH Berkeley MET, utilizing synchrotron radiation will enable the system to benefit from a fully programmable lossless illumination control system.

This work was supported by SEMATECH and performed in part at Lawrence Berkeley National Laboratory, which is operated under the auspices of the Director, Office of Science, Office of Basic Energy Science, of the US Department of Energy.

7636-56, Session 12

Image-based method for in-situ EUV optical testing with an incoherent source

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As EUV optical systems move to higher numerical apertures to resolve smaller features, it becomes increasingly difficult to characterize their aberrations. Many EUV lithography tools and microscopes use incoherent sources, which makes interferometry difficult to perform; tiny spatial filters are nearly impossible to manufacture, and the strict tolerances on the position and tilt of the optical elements combined with low photon flux present significant experimental challenges.

Our in-situ, image-based method is an attractive alternative for characterizing EUV optical systems because it is independent of numerical aperture and coherence, and can be made to work with existing experimental setups. In our method, a computer model of the optical system is generated using a known test pattern and source parameters. An aerial image through-focus series is generated via the a-SOCS algorithm outlined below, using a trial set of aberrations. In the imaging setup, a merit function is generated by comparing the resulting image series to the experimental aerial images. In the lithography setup, the image series is convolved with the resist point-spread function, thresholded and compared with the printed line-edges. The aberrations and host function parameters are modified using a genetic algorithm and the calculation is performed iteratively until the merit function reaches a desired tolerance.

Our algorithm relies on the fast computation of aerial images. This step is greatly expedited by a-SOCS, an adapted form of the Sum Of Coherent Systems decomposition[1]. In a-SOCS, the coherence properties of the optical system and the mask are combined to form a Hermitian operator called the System Cross-Coefficeint (SCC) matrix, that maps pupil aberrations to aerial images. This operator is well approximated by a truncated sum of its spectral components.

Simulations and preliminary experimental results show our reconstruction to be robust to statistical variations due to photon noise and small uncertainties in the knowledge of the coherence properties of the system. In the imaging setup, a 0.3 NA system with coherence factor 0.5 was modeled and the aberrations were reconstructed to within a total rms wavefront error of .03 waves over 15 Zernike polynomials. The reconstruction took 57 minutes on a dual-core 2 GHz machine.

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7636-57, Session 12

Performance of the ASML EUV alpha demo tool

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The 22nm technology node is the target for insertion of EUV lithography into pre-production. To prepare this insertion, the issues that arise with the use of an EUV lithographic scanner in a pre-production environment need to be addressed. To gain better understanding of the issues that come with an EUV lithographic scanner, the Alpha Demo Tool (ADT) from ASML was installed at IMEC and is now in use since mid of 2008. Since then, the source has been upgraded to higher power from a 16W/2π Discharge Produced Plasma (DPP) source to a 120W/2π and recently to a 170W/2π DPP source. Over these upgrades, the ADT has been monitored closely with respect to the imaging performance. In this paper, we report on both the CD fingerprint analysis and the exposure tool stability.

For the CD fingerprint analysis, a new monitor reticle was produced with features down to 25nm, repeated across the entire image field. The reticle was characterized in detail at the mask shop. In addition, we have introduced ShinEtsu resist SEVR59 in the monitor procedure to resolve LS structures down to 30nm. The monitor reticle was then exposed on the ADT to characterize the fingerprint of the 32nm dense lines-spaces across the exposure field. The main contributions to the CD uniformity are the slit uniformity and focus plane deviation, but also the impact of EUV specific imaging effects are addressed like shadowing and flare. The contribution of the mask CD error to the total wafer CD budget was also estimated from the experimentally determined MEEF and the measured mask CD data. Simulations using a calibrated full resist model in a rigorous simulator are used to correlate the observed CD fingerprint to different factors that influence the CD.

To monitor the long-term stability of the EUV ADT exposure tool, we run a monitoring program that consists of a daily wafer exposed on the ADT. The monitor reticle prints both overlay markers and LS patterns over the entire field in a single exposure. The daily EUV exposure is aligned to an etched reference layer exposed on a state-of-the-art 193nm dry tool (the ASML TWINSCAN XT:1450). This way, both CD and machine-to-machine overlay stability data are obtained over the full field size of the ADT. We will also discuss the stability of the CD fingerprint over time.

7636-58, Session 12

EUV lithography at the 22-nm technology node

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We are evaluating the readiness of extreme ultraviolet (EUV) lithography for insertion into production at the 15 nm technology node by integrating it into standard semiconductor process flows for 22 nm node devices because we believe that device integration exercises provide the truest test of technology readiness and, at the same time, highlight the remaining critical issues. In this paper, we describe the use of EUV lithography with the 0.25 NA Alpha Demo Tool (ADT) to pattern the contact and first interconnect levels of small (~5.5 mm x ~10.5 mm) 22 nm node test chips and to print the contact level of a large (~24 mm x 32 mm) 22 nm node test chip using an EUV mask with state-of-the-art defectivity (~0.3 defects/cm2).

We have found that:

the quality of EUVL printing at the 22 nm node is considerably higher than the printing produced with double-exposure double-etch 193 nm immersion lithography;

the percentage of EUV mask defects that print is smaller than expected given current blank defectivity levels; and,

the performance of state-of-the-art EUV resists is now sufficient for 22 nm node pilot production.

The talk will compare the current CD uniformity and overlay performance of the EUV ADT to the requirements for 22 nm node devices.

Part of this work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

7636-59, Session 12

Applicability of device fabrication for hp-35-nm interconnect with extreme ultraviolet lithography

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Selete program covers manufacturability for devices beyond half pitch (hp) 45-nm with a scheme of lithography integration, which consists of exposure tool implementation, resist benchmark and mask technology development. At the last SPIE advanced lithography conference, we described the critical point of extreme ultra violet lithography (EUVL) on an assumption for device manufacturing up to hp 32-nm through wafer process. Since it was found that a resist and a mask with flare correction were usable on the process liability test site using EUV1 exposure, we have planed to fabricate a test chip of back-end-of-line (BEOL) evaluation.

In this study, we describe the lithographic performance on the test chip fabrication with hp-35-nm, which corresponds to beyond 22-nm logic node, for evaluations of Cu/low-k interconnect. Key points of test chip fabrication successful are durable multi-stacked resist process, accurate critical dimension (CD) accuracy, and usable alignment accuracy for 2-level dual damascene on lithography process. A multi-stacked resist process with 70-nm thick resist and 25-nm thick SOG was used on layers of metal 1 and metal 2. The resist thickness on via 1 layer was 80 nm. The resist of SSR3 with a resolution limit of 26-nm line-and-space patterns and a high sensitivity of 8-mJ/cm2 had been tested on the resist benchmarking. For obtaining accurate CD, we dealt with corrections of mask CD bias for compensating a flare variation, mask shadowing effect and optical proximity effect based on rule-base. An accuracy of CD variation with OPC on through the pitch of 35-nm was obtained about plus or minus 1 nm. From a result of test chip evaluation, we found that EUVL has a useful applicability for interconnect fabrication with hp-35-nm and will be able to accelerate device development.

7636-60, Session 12

Process liability evaluation for beyond 22-nm node using EUV

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Extreme Ultra Violet Lithography (EUVL) has been widely realized as a promising candidate for 32 nm half-pitch device manufacturing and beyond. Selete program covers manufacturability for these devices with a scheme of lithography integration, which consists of

exposure tool implementation, resist benchmark and mask technology development. We have planned to evaluate a process liability of EUVL due to recognize our current status of lithography technology development.

In previous study (1), we made the proof of 32nm node device manufacturing through wafer process using a full-field step-and-scan exposure tool called EUV1. To step forward for beyond 22nm node, off-axis illumination (OAI) is one of the efficient technique for resolution enhancement. In this study, we discribe the result of yield improvement work using 32nm node test chip, also the critical point of EUVL on an assumption for beyond 22nm device manufacturing through wafer processes.

A mask with 51-nm thick of LR-TaBN absorber was considered for optimum thinner mask structure to reduce a mask shadowing effect under keeping a contrast of aerial images. Since an accuracy of critical dimension (CD) control was essential in manufacturability evaluation, we dealt with corrections of mask CD bias for compensating a flare variation, mask shadowing effect and optical proximity effect under the OAI condition.

A test pattern was drawn for yield evaluation and exposed to a stacked multi resist layer. After the resist development, the pattern was replicated to SiO2 film with etching and metal wiring formed by damascine process. We will show a result of CD accuracy and availability through wafer processes.

A part of this work was supported by NEDO.

[1] H. Aoyama, et al.: Proc. of SPIE Vol.7271, (2009), 727120

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7637-01, Session 1

A different roadmap: lithographic patterning of discrete track and bit patterning magnetic media

T. R. Albrecht, Hitachi Global Storage Technologies, Inc. (United States)

No abstract available

7637-02, Session 1

Maskless lithography and nanopatterning with electron and ion multi-beam projection

E. Platzgummer, IMS Nanofabrication AG (Austria)

No abstract available

7637-03, Session 1

Directed self-oriented self-assembly of block copolymers: bottom-up meeting top-down

T. P. Russell, Univ. of Massachusetts Amherst (United States)

No abstract available

7637-04, Session 2

Step and flash imprint lithography: a ten-year progress report

C. G. Willson, The Univ. of Texas at Austin (United States)

No abstract available

7637-05, Session 2

Nanoimprint at SEMATECH: program update and an assessment of the technology for semiconductor device applications

M. Malloy, L. C. Litt, SEMATECH North (United States)

SEMATECH became actively engaged in nanoimprint in late 2008 with the purchase of the first Imprio300 from Molecular Imprints. The primary purpose of the SEMATECH program is to evaluate imprint lithography to determine whether it is a viable candidate for semiconductor manufacturing starting at the 22nm node. In addition, we are investigating several of the key technology issues, including an overlay improvement joint development project with Molecular Imprints.

Nanoimprint has shown promising results, especially when it comes to resolution and pattern fidelity. If a good template can be produced, then sub-30nm HP features with low LWR can be printed with ease. Initial capital costs are projected to be several times lower than EUV and 193i systems, not to mention orders of magnitude less complex. Plus, it is already being used by hard disk drive and other non-semiconductor device markets. It is clearly gaining ground. However, several hurdles must be cleared before the semiconductor industry will take it seriously. Defectivity and overlay require significant development to reach the levels required for production. The initial capital cost for an imprint tool may be low, but template costs are currently too high. The final template form factor has yet to be determined and proposed methods for cost-effective template replication have not yet been demonstrated. Particle contamination issues are also a huge concern due to the contact nature of the technology. SEMATECH's purchase of Molecular Imprints' Imprio300 puts it in the perfect position to explore these issues and provide a unique assessment for the industry.

The latest overlay results from a joint development overlay project between SEMATECH and Molecular Imprints will also be presented. The main goal of this project is to improve mix-&-match overlay on the Imprio300 platform towards the ITRS requirements. The final goal of the project is to consistently align and imprint on active, gate, and contact film stacks with <17nm mean+3sigma overlay. The zero layer alignment marks on these wafers were patterned by an ASML 1950i and processed using a shallow trench isolation process. As of this writing, the specification has not been achieved on the specified five-wafer sample, but individual wafers have demonstrated "hero" performance to this level. Updates on other ongoing nanoimprint projects at SEMATECH will also be presented.

Finally, a status report of the Imprio300 tool performance will be provided including tool stability, capability, and SPC data to give the reader a better feel for the tool's overall performance.

7637-06, Session 2

Status of the UV nanoimprint stepper technology for silicon IC fabrication

S. V. Sreenivasan, P. Schumaker, B. J. Choi, Molecular Imprints, Inc. (United States)

Imprint lithography has been shown to possess sub-5nm replication resolution and a potential for low cost of ownership based on the results from references. Historically, there have been concerns about its viability in manufacturing. However, in recent years it has become evident that UV imprint lithography is becoming viable for volume manufacturing with significant development in mask infrastructure, CD control through etch, low defectivity, overlay and throughput. It is opening up emerging nanomanufacturing applications such as patterned media for hard disk drives; and demonstrating the potential to become a complement to photolithography at sub-25nm half-pitch lithography for silicon ICs.

This presentation will discuss current status of UV imprint steppers relative to four lithography metrics that are affected by these steppers: (i) Residual layer uniformity (which indirectly affects CD uniformity through etch); (ii) High-resolution overlay; (iii) Throughput; and (iv) Imprint-specific defectivity. The stepper system evolution requires continued progress in all these four metrics simultaneously. This paper will present current status of UV imprint steppers demonstrating progress towards a full solution at sub-25nm half-pitch patterning. The presentation will conclude with a gap analysis on each of the four lithography metrics affected by the stepper.

7637-07, Session 2

Simulated and experimental characterization of planarizing materials for reverse-tone step and flash imprint lithography

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Reverse-tone step and flash imprint lithography requires materials that are highly-planarizing to be spin-coated onto patterned wafers with significant topography. Ideally, these planarizing materials must contain silicon for etch selectivity, they must be UV- or thermally-curable, and

they must have a low viscosity and low volatility. One novel material in particular, branched and functionalized siloxane (Si-12), is able to adequately satisfy these requirements.

This paper focuses on the correlation between the simulated and experimental results of Si-12 planarity on patterned wafers. Two different materials, methacryl- and epoxy-functionalized Si-12, were synthesized. Each of the samples was spin-coated onto patterned substrates. After crosslinking, the epoxy-functionalized Si-12 showed relatively low bias between patterned and un-patterned areas, indicating that it is a promising material for this application. The correlation of this data with simulated results is presented herein.

7637-08, Session 2

Incomplete cross-linking of UV-nanoimprint resists confined in nanoscale spaces

S. Kim, H. Lee, C. L. Soles, National Institute of Standards and Technology (United States)

Nanoimprint Lithography (NIL) is a next generation lithographic patterning technique with the potential to reduce tool costs and increase pattern resolution. NIL operates by a simple squeeze-flow mechanism where liquid resist is squeezed into the nanoscale cavities of a mold and is then “set” into a rigid resist pattern through a cross-linking process induced by UV radiation. This is a direct write process where the shape and dimensions of the cavity directly define the resolution of the pattern. This is unlike optical lithography where regions of the resist are selectively exposed through a photo mask, defining a latent image in the film, and the final pattern resolution depends on a reaction-diffusion mechanism that changes the solubility of the resist and the subsequent dissolution process where a developer dissolves the reacted regions of the film. With optical lithography, pattern resolution is always complicated by this diffusion bias and the way that the developer interacts with exposed/unexposed regions of the resist. In this respect NIL is very attractive as the pattern resolution is physically defined by the walls of the cavity. As the minimum feature size of interest continues to decrease, there is less room for uncertainty and the notion of simplifying the patterning process becomes very attractive.

This notion of NIL as a direct write technology is predicated on the ability of the resist material to faithfully replicate the features in the mold. To evaluate this process we have been developing non-destructive, high-resolution measurements that quantify the shape of the patterns in both the imprint mold and the pattern, and thereby quantify the fidelity of the pattern transfer process. Here we turn our attention to the chemistry and the cross-linking reaction which transforms the liquid resist into a rigid pattern. Incomplete cross-linking can lead the poor quality and mechanically unstable patterns. It will also be important for throughput and optimization to know the minimum UV dose required to achieve full cross-linking. Quantifying pattern shape is not sufficient; methods to quantify the degree of chemical conversion as a function of pattern size are also needed. We introduce a suite of measurements to determine the degree of cross-linking in model mixtures of acrylate liquids that are typical of UV NIL resists. Fourier transform infrared (FT-IR) spectroscopy is used to monitor the consumption of the alkene groups as a function of both the UV dose as well as the feature size of the NIL patterns. From this we calculate the degree of cross-linking. It is also well known that glass transition temperature Tg, or softening transition, of an polymer network systematically increase with the cross-link density. In bulk systems it is straightforward to correlate the Tg with degree of cross-linking. For these nanoscale structures we introduce a method to probe their individual softening transitions with an AFM that is locally heated at the tip. As the tip is heated, the material under the tip expands and the cantilever is deflected upwards. When the Tg of the material is reached, the tip plunges into the sample, identifying softening transition. In this presentation we report that both the FT-IR and locally heated AFM measurements yield consistent results for the cross-linking density. For length scales larger than 35 nm, the cross link density of the NIL patterns is consistent with the bulk material. However, reductions in the cross link density and thermal stability of the patterns are encountered when the features sizes become smaller than 35 nm, indicating that confinement is affecting the cross-linking reaction. The impact of these measurements on the patterning of sub-35 nm features with NIL is discussed in detail.

7637-09, Session 3

E-beam maskless lithography

K. G. Ronse, IMEC (Belgium)

No abstract available

7637-10, Session 3

50 keV electron-beam projection maskless lithography (PML2): results obtained with 2,500 programmable 12.5-nm sized beams

C. Klein, J. Klikovits, L. Szikszai, E. Platzgummer, H. Loeschner, IMS Nanofabrication AG (Austria)

Projection Mask-Less Lithography (PML2) is a potentially cost-effective electron multi-beam solution for the 22nm ITRS technology node and beyond [1]. First results obtained with the PML2 Alpha Testbench are presented, realized within the framework of the European MAGIC project [2].

The PML2 Alpha Testbench is equipped with a programmable Aperture Plate System (APS) providing about two thousand 2.5 micrometer-sized beams which are projected onto wafer level with 200x demagnification (Figure 1). The APS contains CMOS electronics which allows for addressable deflection of selected beams; only non-deflected beams make it to the wafer surface to achieve 12.5 nm spot size. Beam energy (50keV) and current density (~2 A/cm2) are the same as in future PML2 production tools. Thus, the results obtained with the PML2 Alpha Testbench unambiguously prove the patterning capabilities of the PML2 technology.

[1] C. Klein et al., Proc. SPIE Vol. 7271

[2] L. Pain et al., Proc. SPIE Vol. 7271

7637-11, Session 3

Evaluation of throughput improvement by MCC and CP in multicolumn e-beam exposure system

A. Yamada, Y. Oae, T. Okawa, M. Takizawa, M. Yamabe, Association of Super-Advanced Electronics Technologies (Japan)

In the Mask Writing Equipment Technology Research Laboratory of ASET MASK-D2I project, we have developed an e-beam multi-column-cell (MCC) exposure system made up of four column cells for the proof-of-concept (POC) of MCC with character projection (CP) technology.

We have evaluated resolution capability and stitching accuracy of the MCC system. In the resolution evaluation, we have shown that isolated lines of the width 35nm and 60nm 1:1 LS patterns were successfully exposed with each column cell of the multi column system. As for stitching accuracies, we have evaluated the stitching between patterns exposed in the fields with opposite deflection directions, and the stitching accuracies between patterns exposed with different column cells. We could show that the present stitching errors for both cases were better than 15nm.

We are exposing various patterns to evaluate exposure throughput of the POC system. Character patterns were extracted from mask pattern data in the Mask Design Data Technology Research Laboratory of this ASET project. We made a CP mask having the character patterns in a deflection area on the mask. Exposure data were prepared in the same Mask Design Data Technology Research laboratory.

In the conference, we will show some evaluation results of the throughput improvement using the character patterns and the multi-column-cell technology.

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7637-12, Session 3

Evaluation of maskless electron-beam direct writing with double character projection apertures

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As the feature size of LSI shrinks, the cost of mask manufacturing and turn-around-time continue to increase. Low-volume production of systems-on-chips is especially becoming infeasible economically. Maskless lithography using electron beam direct writing (EBDW) technology attracts attention in recent workshops and conferences on semiconductor lithography. However, the throughput of EBDW system based on the variable shaped beam principle (VSB) is low because many electron beam (EB) shots are required for exposure of whole patterns on a wafer.

Over years, EBDW techniques have evolved for the reduction of the number of EB shots or throughput enhancement. The character projection (CP) method is effective for decreasing the number of EB shots because the character patterns in several um square can be exposed in one shot. Since the number of characters available on one CP aperture is limited, character patterns must be suitably selected in order to minimize the number of EB shots. A cell library development methodology for throughput enhancement has been reported, where frequently-appeared patterns on a CAD layout are selected as characters of the CP method. As recent advanced techniques, CP friendly design flow and new direct write techniques like the multi-column cell system (MCC) have been developed. As far as we know, however, cost evaluation has not been reported.

In this paper, we evaluate maskless EBDW with double CP apertures. In the conventional CP-capable EBDW, the first aperture generates a square beam and the second aperture finalizes the complex character shape. In our proposed method, each aperture has complex character patterns. This double CP apertures system (DCP) projects patterns onto wafers by the combined use of two apertures. It is expected that the DCP improves productivity since it can produce a wider variety of the combinational patterns. Furthermore, it can provide better cost performance since it is constructed by adding just one deflector above the first CP aperture.

We extracted character patterns for double CP apertures from standard cell layouts synthesized with 0.35um cell library. Then we estimated effect on cost reduction and throughput enhancement against the conventional system with one CP aperture and the MCC with 16 column units. Experimental results showed that although the MCC achieved the highest throughput, the DCP yielded the lowest cost per wafer. Now we are developing an optimization algorithm for character patterns on double CP apertures. We will apply the proposed method to microprocessor layout synthesized with Nangate 45nm Open Cell Library. In the conference, we will report evaluation results on cost performance compared to the other CP approaches.

7637-13, Session 3

Multiple pass exposure in e-beam lithography application to the sub-32-nm layouts

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Electron Beam Direct Write (EBDW) lithography is used in the IC manufacturing industry to sustain optical lithography for prototyping applications and low volume manufacturing. This solution is also employed in R&D to study the future technological nodes ahead of their mass production. As microelectronics is now moving towards the 32nm node and beyond, the specifications in terms of dimension control and roughness becomes more stringent. Besides, the shrink of the feature size and pitch impacts significantly the process window, leading to difficulties to stabilize the full process flow.

To get a fine control of the dimensions and bias in a layout, sufficient energy latitude is required. In EBDW the standard proximity effects corrections based on dose modulation show difficulties to provide enough energy latitude to pattern the structures designed below the 45nm node. A new approach is thus needed to improve the process window of EBDW lithography and, as a consequence, push its resolution capabilities. In previous papers a new writing strategy based on multiple pass exposure has been introduced and optimized to pattern critical dense lines. This new technique consists in adding small electron Resolution Improvement Features (eRIF) on top of the nominal structures. Then this new design is exposed in two successive passes with optimized doses. Previous studies were led to evaluate this new writing technique and showed that the energy latitude and the writing time can be optimized by tuning the design of the eRIF.

This paper will generalize the application of the multiple pass exposure method to the patterning of sub-32nm layouts. The gains that can be achieved with this new writing technique will be presented. With an optimized design for the eRIF, this work will highlight that the energy latitude of 32nm lines can be multiplied by a factor up to four.

Design rules have already been established to improve the process window of critical dense lines. In this paper those rules will be adapted and optimized to specifically correct 32nm layouts. This work will show that a compromise on the design of the eRIF has to be found to optimize exposure latitude, line edge roughness and writing time. Finally, the results from wafer exposures will demonstrate that the multiple pass method provides an improved process window to pattern critical layouts, with a limited impact on the writing time. Thanks to this gain, the resolution of the lithographic tool will also be increased.

7637-14, Session 3

MAPPER: high-throughput maskless lithography

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MAPPER Lithography is developing a maskless lithography technology based on massively-parallel electron-beam writing with high speed optical data transport for switching the electron beams. In this way optical columns can be made with a throughput of 10-20 wafers per hour. By clustering several of these systems together high throughputs can be realized in a small footprint. This enables a highly cost-competitive alternative to double patterning and EUV alternatives [1, 2].

In 2009 MAPPER shipped two systems one to TSMC and one to CEA-Leti. Both systems will be used to verify the applicability of MAPPER's technology for CMOS manufacturing.

In this presentation an update will be provided about the development of the MAPPER system over the past year. Currently this is a system with 300 mm wafer capability containing 110 electron beams which can be individually switched on and off by means of an optical blanker array. Additional printing results will be shown and the status of stitching experiments will be presented.

[1] E. Slot et al., Proc. of SPIE Vol. 6921, 69211P, (2008)

[2] M.J. Wieland et al., Proc. of SPIE Vol. 7271, 72710O1, (2009)

7637-15, Session 4

Self-assembled systems for extensible patterning

W. D. Hinsberg, IBM Almaden Research Ctr. (United States)

No abstract available

7637-16, Session 4

Templated self-assembly of Si-containing block copolymers for nanoscale device fabrication

C. A. Ross, Massachusetts Institute of Technology (United States)

Thin films of microphase separated block copolymers, which can form patterns consisting of dense arrays of lines, dots, rings and other geometries, are attractive materials for self-assembled nanoscale lithography. In this work, we discuss nanolithography applications of Si-containing block copolymers, including polystyrene-b-polyferrocenyldimethylsilane (PS-PFS) and polystyrene-b-polydimethylsiloxane (PS-PDMS) diblock copolymers and PS-b-PFS-b-poly(2-vinylpyridine) (PS-PFS-P2VP) and polyisoprene-b-PS-b-PFS (PI-PS-PFS) triblock terpolymers. These materials are advantageous for nanolithography compared to all-organic block copolymers because first, they are characterized by a high etch selectivity and high etch resistance of the Si-containing block, simplifying pattern transfer; and second, they typically have a high interaction parameter, which allows small period features with low edge roughness to be achieved.

We first discuss strategies for templating the self-assembly of these block copolymers to make patterns relevant to electronic devices. For example, the locations of 40 nm period spherical PDMS microdomains were controlled by a sparse array of posts, allowing templating of up to 20 microdomains per post to form large area dot arrays with excellent order. Linear patterns were formed from 20 - 32 nm period cylindrical morphology PS-PDMS templated using topographical posts or steps, to form arrays of straight parallel cylinders with controllable period and orientation, arrays with angles or junctions, or sharply curved, concentric toroidal structures. The overall morphology and period of the block copolymer microdomain arrays can be varied by solvent annealing in mixed solvent vapors. We then discuss the formation of self-assembled patterns with sub-20 nm periods and sub-10 nm feature sizes. Linear features of 8 nm linewidth and 17 nm period with excellent order were obtained from films of PS-PDMS of molecular weight 16 kg/mol which were solvent-annealed at room temperature. Unlike the larger molecular weight block copolymers, which order well under toluene vapor annealing, the smaller period structures must be annealed in a low vapor pressure of a poorer solvent. Finally, we describe pattern formation in PI-PS-PFS and PS-PFS-P2VP triblock terpolymers, to form respectively square arrays of dots and close-packed arrays of rings. In the former case, the square symmetry arrays were oriented within topographical steps and the direction of the axes of the lattice with respect to the step edges was controlled by substrate functionalization.

Patterns were transferred into a range of metals by overcoating the block copolymer patterns with a metal film, then etching back using a combined chemical and physical reactive ion etch to leave a reverse-contrast image. Transfer into silica and into other polymer layers was accomplished using reactive ion etching. Device applications, including the fabrication of interconnect lines, silicon nanowires, patterned media, and conductive polymer sensors, will be described.

References: Bita et al., Science 321 939 (2008); Jung et al, Nano Letts. 7 2046 (2007); 8 2975 (2008); Chuang et al., Adv. Mater. 21 (2009)

7637-17, Session 4

CMOS process compatible directed block copolymer self-assembly for 20-nm contact holes and beyond

L. Chang, X. Bao, H. S. P. Wong, Stanford Univ. (United States)

Conventional lithography technologies have been experiencing costly development to meet the demands for fine feature patterning for device fabrication in the semiconductor industry. So far, there is still no apparent solution for patterning feature sizes beyond the 22nm node. Directed block copolymer self-assembly is an emerging lithographic technique that has been receiving extensive attention due to its simplicity and cost effectiveness for realizing sub-20 nm features, and even down to 5 nm [1]. Furthermore, layout design rules have now evolved to the use of highly regular patterns and double-pattern/double-etch to achieve fine features. Block copolymer self-assembly is compatible with this recent trend since it yields highly regular patterns and can be combined with conventional lithography for pattern alignment. Block copolymer has been previously used for back-gated FinFET [2] and 300 mm wafer manufacturing for airgap formation in BEOL [3] where the self-assembled features were not aligned to any existing features on the wafer. We have demonstrated top-gated field-effect transistors featuring 20 nm contact holes defined by diblock copolymer self-assembly at full wafer level [4]. The self-assembly process is fully integrated with an existing CMOS process flow using conventional tools where the 20 nm contact holes are aligned (registered) by guiding templates defined by coarse conventional lithography to patterns on a previous level. Printing contact holes is one of the key challenges in advanced technologies. Our results highlight the potential of block copolymer lithography for CMOS technologies beyond the 22 nm node. As a further step, we need to extend this technique to pattern multiple-size contact holes for integrated COMS devices at the circuit level. A double patterning strategy can be used to pattern different guiding templates at different levels for self-assembling contact holes with different sizes. We illustrate the use of such a strategy by showing possible guiding templates for the patterning of multiple-size contact holes for a 22 nm node SRAM cell.

[1] C. T. Black, et al. Trans. IEEE NANO, 3, 412 (2004).

[2] C. T. Black, et al. Appl. Phys. Lett., 87, 163116 (2005).

[3] P. Rodgers, Nature Nanotechnology, 2, 342 (2007).

[4] L.-W Chang et al. IEDM, paper 36.3 (2009).

[5] Haran, B. S., et al. Proc. IEDM, 625-628 (2008).

[6] Chang, L.-W., et al. Proc. SPIE, 6921, 69212M (2008).

[7] Tang, C., et al. Science, 322, 429-432 (2008).

7637-18, Session 4

Directed self-assembly for via patterning

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Limited critical dimension (CD) control is one of the major issues in printing tight-pitch interconnects using optical lithography. Directed self-assembly (DSA), which combines lithographically defined substrates and self-assembled polymers, provides a simple and effective method to improve CD uniformity. The intrinsic size of a self-assembled domain is determined by the block copolymer composition and molecular weight. Therefore, directed self-assembly of block copolymers can be used to produce patterns with both smaller CD and increased CD uniformity relative to the original lithographic pattern. Specifically, we show that self-assembly of cylindrical block copolymer domains within via arrays produces patterns with smaller CD and reduced %CD variation. We investigate the self-correcting behavior of block copolymer self-assembly as a function of the prepattern geometry and block copolymer composition. Quantitative characterization of CD variation reduction and pattern rectification will be presented. In practical terms, the DSA process can increase the effective process latitude and reduce the effective mask error enhancement factor (MEEF) when patterning tight-pitch vias and contact holes.

7637-19, Session 4

Low-molecular weight block copolymer surfactant/additive blends with hydrogen bonding induced phase segregation for use as sub-10-nm lithographic etch masks

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Block copolymer films with a thickness of a single domain layer have been shown to be effective etch masks for patterning features on the order of 10-20 nm. This work focuses on blends of low molecular weight, non-ionic triblock copolymer surfactant (Pluronics, PEO-b-PPO-b-PEO) with polymeric or molecular glass additives that provide access to domain sizes on the order of 10 nm and below. Specifically, hydroxyl or carboxylic acid-containing additives act as an important component of the resist blends by increasing the effective segregation strength between the PPO and PEO segments of the Pluronic surfactant. This increased segregation is a result of the hydrogen bonds occurring selectively between the PEO and additive components. Significant enhancements in the long-range order of the domains can also be attained. SAXS was used to observe the bulk phase behavior of blends of Pluronic surfactants and a phenolic-containing molecular glass, whereas films of these systems were characterized by AFM. Scattering data shows that the overall order and segregation strength clearly depend on temperature and additive concentration, while AFM of monodomain layer films exhibit a clear order-order transition (OOT) with increased additive loading. In addition to altering the phase behavior of the templates, these additives can have the additional benefit of increasing the fluorine-based reactive ion etch (RIE) resistance of the PEO domain, which helps to improve etch contrast between the two block copolymer domains. This contrast is a crucial property of an etch resist at the feature sizes of interest.

7637-28, Session 4

Integration of directed self-assembly into 193-nm lithography

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Directed self-assembly (DSA), which combines self-assembled polymers and lithographically defined substrates, has been considered as a potential candidate to extend optical lithography. Successful demonstrations of frequency multiplication and/or pattern rectification using patterned substrates transferred from features written by electron-beam lithography and EUV lithography have been reported. In order to move DSA from the research stage to a viable manufacturing technology, we seek to integrate DSA with state-of-the-art 193 nm optical lithography in a straightforward and process-friendly manner. In this paper, we discuss our recent progress with various integration strategies using 193 nm photolithography to produce topographical or chemical guiding patterns for DSA. This new ability to use 193 nm lithography to fabricate effective guiding patterns in a straightforward manner now enables DSA to be applied to large areas with conventional tools, opening the door to meaningful wafer-scale characterization of the impact of materials and process parameters on DSA performance.

7637-20, Session 5

Directed assembly of block copolymers on lithograpically defined surfaces

P. F. Nealey, Univ. of Wisconsin-Madison (United States)

No abstract available

7637-21, Session 5

EBL-directed assembly of DNA nanostructures and origami on silicon

M. Lieberman, B. Gao, K. N. Kim, Univ. of Notre Dame (United States); L. Mark, St. Joseph's High School (United States); G. H. Bernstein, K. Sarveswaran, Univ. of Notre Dame (United States)

This paper describes efforts to understand the binding of DNA origami and other nanostructures on chemically modified silicon surfaces, and to use EBL "anchor pads" to direct the binding of DNA nanostructures on silicon. DNA origami and DNA nanostructures are usually imaged on mica surfaces. They do not adhere to anionic silicon dioxide unless high concentrations of divalent cations such as Mg2+ are present, as in two recent reports from the groups of Kershner and Cha. However, cationic self-assembled monolayers (SAMs) can easily be formed on silicon dioxide via siloxane chemistry, and these SAMs provide robustly attached surface charges that anchor DNA nanostructures and origami. Because the anchor pads contain permanently attached positive charges as "glue", the bound DNA nanostructures and DNA origami are stable in buffer, water, and air.

In order to locate individual DNA nanostructures at desired sites, 35-40 nm aminopropyltriethoxysilane (APTES) dots or 100 nm APTES squares were fabricated by a combination of EBL and molecular liftoff. The anchor pads are 1.1(2) nm thick. Deposition of small DNA nanostructures (8 nm x 37 nm x 2 nm) or DNA origami (60 nm x 90 nm) was conducted in 0.1-1.0 micromolar solution. 85% of the small anchor pads attracted a single DNA nanostructure, and the binding energy was estimated as at least -11 kcal/mol. In preliminary work, 63% of the larger anchor pads attracted a single DNA origami. The DNA nanostructures are persistently attached and could be imaged in air after rinsing the substrate in flowing water. The origami have lithographic dimensions and the ability to bind non-DNA components at designed sites just 6 nm apart. They could thus be useful as "packages" for assembling nanoscopic parts on silicon.

DNA origami did not orient on the APTES anchor pads, so we studied origami binding to a series of SAMs made from mixtures of APTES and trimethylaminopropyl trimethoxysilane chloride (TMAC). Increasing the mole fraction of TMAC tunes the surface charge density of the mixed monolayers, which in turn controls the binding of DNA nanostructures. X-ray photoelectron spectroscopy shows separate signals at binding energies of 399.7 eV, 401.5 eV, and 402.9 eV, corresponding to the primary amine of APTES, the protonated primary amine, and the quaternary amine of TMAC. Thus, for each surface, the coverage and surface charge density can be quantified. At high surface charge density, DNA nanostructures and DNA origami both bind irreversibly; the DNA nanostructures are "jammed", and defects such as folded or rumpled origami are common. At low surface charge density, binding is weak and DNA does not attach persistently to the surface. On the optimal SAM (deposited from a solution with 75% TMAC/25% APTES precursors) the origami bind about as well as they do on unmodified mica. Work is currently underway to make anchor pads with these optimal SAMs.

7637-22, Session 5

Electron-beam directed material assembly

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Block copolymer lithography has been proposed as one route to pattern feature sizes in the 10-45 nm range via directed self-assembly on chemically nanopatterned surfaces. Diblock copolymers consist of two chemically different polymer chains connected at one end by a covalent bond that can spontaneously form ordered structures at the molecular scale with the size of the domains determined through control of the block molecular weights and the composition of the blocks. Traditional block copolymer lithography typically involves the deposition of a polymer brush followed by photoresist application, patterning, pattern transfer and resist removal to define the nanopattern that will direct the assembly of the block copolymer film.

We have developed a processing method that employs direct surface imaging of a surface-modified silicon wafer to define a chemical nanopattern that directs material assembly, eliminating most of the traditional processing steps. Our initial experiments involved exposure of alkylsiloxane-modified silicon wafers with a 157-nm interference system to generate chemically nanopatterned surfaces that directed the assembly of poly(styrene-block-methyl methacrylate) (PS-b-PMMA) into periodic lines of alternating materials. By employing a block copolymer blend to match the lithographic pitch of our interference exposure system, we demonstrated a wide dose latitude, which could also be numerically modeled by analysis of the surface energy aerial image. Once assembled into periodic structures, the PMMA block was removed with an additional 193-nm blanket exposure, and the resulting

polystyrene features were used as an etch mask to transfer periodic lines-and-spaces into a silicon substrate with >2:1 etch selectivity.

We have performed initial studies to extend this concept to other wavelengths as well. Irradiation at 193 nm showed that the surface energy of arylsiloxane-modified silicon wafers can be changed as a function of exposure dose, and we are currently employing a 193-nm interference exposure system to form nanopatterns by the directed assembly of PS-b-PMMA films in a manner analogous to our prior results at 157 nm. EUV exposure also changes the surface energy of the exposed areas, thereby controlling the bulk orientation of the block copolymer, and we employed this effect to generate EUV-induced chemical nanopatterns.

In this present paper, we will show that electron beam lithography can also be used to define chemical nanopatterns to direct the assembly of PS-b-PMMA films. Half-pitch patterns resulted in the directed assembly of PS-b-PMMA films. Electron beam lithography can also be used to prepare surfaces for pitch division. Instead of the deposition of an HSQ pinning structure as is currently done, we will show that by writing an asymmetric pattern, we can fill in the space with smaller lamellar period block copolymers to shrink the overall pitch and allow for 15-nm features.

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7637-23, Session 5

Self-assembling nanosphere lithography process for gated carbon-nanotube field emission arrays

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Carbon nanotubes (CNTs) have many unique properties ideal for field emission such as narrow diameters, high aspect ratios, high temperature stability, good conductivity, and structural strength. A gated array is preferable to a diode type array due to the lower extraction voltages and reduced screening effects. An inexpensive fabrication process has been developed using self assembling nanoshpere lithography for sub-micron gate dimensions of a CNT field emission array. The array fabrication process consists of a silicon wafer with a 20 nm titanium diffusion barrier followed by 10 nm nickel catalyst layer covered with 1-2 µm of silicon dioxide. Self-assembling polystyrene spheres are deposited in a monolayer across the substrate to create the gate mask. The diameter of the spheres is reduced to the desired gate dimensions using an oxygen plasma ash. The gate metal (Ti/Au) is then deposited via evaporation. The gate openings are created through lift-off facilitated by dissolving the polystyrene spheres in an acetone bath. Reactive ion etching is used to remove the silicon dioxide and expose the nickel catalyst layer for CNT synthesis within the gate openings. The process is demonstrated for both 1 µm and 500 nm diameter polystyrene spheres for gate dimensions and gate pitch of 500 nm and 250 nm respectively. The resulting array is analyzed using a scanning electron microscope. Further development of the polystyrene monolayer deposition method is necessary to decrease defects in the monolayer structure. Future work will investigate the reduction of gate dimensions to 20 - 50 nm to facilitate a single CNT per gate array.

7637-24, Session 5

Field-based simulations of directed self-assembly in a mixed brush system

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Graphoepitaxy-type techniques to control and stabilize self-assembly of block copolymer systems have been widely tested and are considered as a particularly promising nano-lithography tool for the creation of next generation information storage and electronic devices. Block copolymer systems that are laterally confined by a topographically patterned substrate develop a close-packed microdomain ordering along the walls that can serve to refine long-range in-plane order and stabilize desirable nanoscale structures for a variety of applications. In this study, we have expanded the scope of such lateral confinement techniques to include mixed polymer brush systems, in which one end of the polymer chains is tethered to the substrate. When two different A and B homopolymers are randomly grafted to a substrate, dissimilar A and B chains prefer to phase separate, but the grafted chain ends limit the phase separation to ~10 nm distances. If the top surface of such a mixed A/B polymer brush does not attract a specific component, the polymers have comparable lengths, and they are grafted at similar areal densities, a lateral microphase separation is observed that is similar to the perpendicular lamellar phase of symmetric block copolymers. In the mixed brush context, this phase is called the “ripple” phase. Unfortunately, experimentally observed ripple phases in mixed brush systems have very short-range order and are defective, reducing the usefulness of such systems for advanced lithography as compared to block copolymers. One possible strategy for addressing this shortcoming would be to adapt successful topological confinement methods for block copolymers, i.e. graphoepitaxy, to mixed polymer brushes. Here, however, we explore a different type of “chemical” (rather than “topological”) confinement in which a “pure” polymer brush of either A or B homopolymer is used to laterally confine the mixed A/B brush into a region of prescribed shape. Such confinement masks can be created by a variety of low resolution (micron-scale) soft lithographic methods to pattern orthogonal polymerization initiators that are subsequently elaborated into polymer brushes. To explore the efficacy of such a scheme, we have conducted three-dimensional self-consistent field theory (SCFT) simulations to examine phase-separated morphologies in confined mixed brush systems. Without a confining pure brush region, our simulations for mixed brushes with uniform grafting show defective micro-domain ordering in accordance with experiment. However, simulations conducted with lateral confinement indicate that a pure A brush region draws polymer A from the mixed brush to the mask perimeter, thereby reducing the interfacial energy. This in turn creates a polymer B-rich region that follows the contour of the mask and thereby guides phase-separation aligned with the interface between pure and mixed brush regions. Using similar SCFT tools, we have also studied various phase-separated morphologies and mechanisms as a function of the relevant parameters in this system: grafting densities, interactions between all molecular components and with the substrate, temperature, and the relative size of the polymers to the scale of the chemical confinement.

7637-25, Session 6

NIL template challenges and progress toward 2x nm node

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No abstract available

7637-26, Session 6

Imprint lithography defects in semiconductors and patterned media

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Imprint lithography has been shown to be an effective technique for replication of nano-scale features. When the imprint material is a photocurable liquid, it is possible to perform the patterning process at low temperature and ambient pressure, which enables accurate overlay and leads to low process defectivity. The resolution of the imprint approach is strictly dependent on the ability to create a 1X master mask or template, and improvements in resolution can be achieved without new optical systems or substantial changes in photoresist materials.

Acceptance of imprint lithography for manufacturing will require demonstration that it can attain defect levels commensurate with the requirements of cost-effective device production. This work summarizes the results of defect inspections of semiconductor wafers and hard disks patterned using Jet and Flash Imprint Lithography (J-FILTM). Inspections were performed with optical and e-beam based automated inspection tools.

For the semiconductor market, it will be necessary to detect defects less than the half pitch of the device. A test mask was designed which included dense features (with half pitches ranging between 32 nm and 48 nm) containing an extensive array of programmed defects. For this work, e-beam inspection was used to detect both random defects and the programmed defects. Examples of detected program defects are shown in Figure 1. Analytical SEMs were then used to review the defects detected by the inspection. In addition, defect trends over the course of >5,000 imprints were observed with another test mask using a KLA-T 2132 optical inspection tool. The primary source of defects over 5,000 imprints was shown to be related to micron-scale particles. Two such micron-scale particles that caused repeating defects are shown in Figure 2. Work is ongoing to improve the cleanliness of the system, wafer handling, and prior wafer processing steps to eliminate these large particles from the imprint process.

For the hard drive market, this work presents a methodology for automated pattern inspection and defect classification for imprint templates and disks. Candela CS20 and 6120 tools from KLA-Tencor map the optical properties of the disk surface, producing high-resolution grayscale images of surface reflectivity, scattered light, phase shift, etc. We have developed software that analyzes these images and identifies defect pixels distinctly from the pixels that correspond to data storage structures or servo patterns. Defects that have been identified in this manner are further characterized according to the morphology of the defect pixels as well as the defect location on the substrate.

7637-27, Session 6

Polymeric working stamps employed in fully automated hot-embossing processes

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The low-cost fabrication of disposable, polymer based devices needed for emerging point-of-care diagnostic or bio-sensing devices can be realized by hot embossing processes at low cost. The similarities in regards to process parameters and equipment specifications between wafer bonding and hot embossing processes have led to the modifications of wafer bonder systems used for thermo-compression bonding processes to accommodate embossing processes some years back [1]. Hot embossing processes are generally used to address different applications ranging from polymer-based lab-on-chip systems, where imprinting is done on thick polymers substrates, to the fabrication of sub 100 nm features for bio-sensing or data recording applications which requires imprinting into spin-on polymers. The first method requires hard stamps mostly made of Ni, brass or stainless steel depending on the expected feature size. Those replicated structures are used directly as functional devices deployed in microfluidic devices [2]. In the later case a pre-structured stamp made of Si is used to transfer a pattern into a spin-coated Si substrate. Those structures can be transferred into Si by dry reactive ion etching and their size can be in the nm-range if the stamp is fabricated by e-beam writing. Development of commercial applications based on the hot embossing NIL processes requires, however, fabrication systems and processes with throughputs that are beyond the R&D tools existing today. This requires fully-automated process implying an automated de-embossing process of stamp and imprinted substrate; a reliable and residual free separation of stamp and imprinted substrate post imprint by using an anti-adhesive monolayer on the stamp surface [3]; and the use of compliant layers that ensure imprints uniformity over large areas. The first fully automated hot embossing system was developed for the hard disc industry for double side patterning of hard disks using Ni-stamps [4]. S. Merino, et.al. have proposed a method for automated de-embossing by mechanically fixing a Si stamp on a top chuck and separating the substrate by an “air knife” using a mechanical frame to hold the substrate in place [5]. Another proposed way is to fixation of the substrate by utilizing the high adhesion force of a Si wafer to a PDMS layer described in the same paper. While both methods are successful in separating the stamp and the imprinted substrate in a fully automated way, a full automation process including substrate and stamp handling might be difficult to realize with the proposed method. This paper demonstrates the realization of a fully automated hot embossing system for spin-on polymers on the EVG®750 (Figure 1), the first one of its kind that includes both substrate and stamp handling as well as automatic embossing and de-embossing. In contrary to the process described above using hard stamps, the process we are reporting here on the EVG®750 system employs soft working stamps materials which exhibit manifold benefits over Si stamps: (1) soft working stamps can be fabricated at low cost from expensive e-beam written masters, (2) soft working stamp can be used for multiple imprints, (3) the use of soft working stamps does not require compliant layers as they already exhibit this trait and (4) these stamps are fully compatible with optical alignment to a structured Si substrate. UV-curable soft stamps are bonded to a glass backplane and can be used for top side live alignment, i.e., the alignment keys of both the polymer stamp and the Si substrate are visible at the same time. Features sizes in the µm range and down to 50 nm utilizing working stamps are demonstrated in Figure 2, 3 and 4 by applying a fully automated process mode in the EVG®750. This paper will provide detailed insights in the design and the functions of the fully automated hot embossing systems as well as details of the working stamp fabrication process, alignment, imprinting and de-embossing process.

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7637-28, Session 6

High-quality secondary templates for nanoimprint lithography from cubic Silsesquioxanes (SSQs)

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Nanoimprint lithography (NIL) is an exciting next-generation lithography combining the potential of a sub-5 nm patterning resolution with the high throughput, low-cost and inherent simplicity of a stamping process. However, one of the biggest impediments to the wide spread implementation of NIL is the availability of high quality molds. The fabrication of high resolution, 1× molds still requires costly and time consuming serial patterning techniques, such as electron beam lithography, followed by multiple etching or lift-off process. In many applications template fabrication and development are too formidable of a barrier to enable penetration of NIL into different technology sectors. Here we present a class of specially designed cubic silsesquioxane (SSQ) materials that can be easily patterned with nanoscale dimensions via single thermal nanoimprint lithography (NIL) and then used directly as daughter NIL templates. The hydrophilic SSQ precursors can be easily spin cast into films directly imprinted at elevated temperatures. During the NIL process the SSQ is converted into a hydrophobic (water contact angle of over 100 degrees) cross-

linked material, which facilitates the release of mold. After imprinting, the patterns are vitrified at elevated temperatures into a fully cross-linked organosilicate material with a low surface energy, high UV transparency, high modulus, and low coefficient of thermal expansion. These imprinted patterns can be directly used as secondary molds for both ultra-violet UV and thermal NIL, without applying a fluorinated mold release coating. In this presentation we will describe these materials in detail and quantify the fidelity of the pattern transfer process, with respect to dimension control from the NIL master to the secondary mold and through the imprinted pattern for both thermal and UV NIL systems, with critical dimension as small as 10 nm. Our examples of high quality imprints, without the use of mold release coatings, at high temperatures and pressures illustrate the utility of these materials for NIL mold replication.

7637-29, Session 6

Automating molecular transfer lithography at 25-nm on 200-mm wafers, including site-remote coating of resist on dissolvable templates

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Towards the development of a nanopatterning technology that can meet the requirements of sub-32nm CMOS processing for at least rapid prototyping and low-volume applications, an automated nanopatterning technology is described that conducts the molecular transfer lithography process, which bonds a water-dissolvable template, pre-coated with resist, onto a wafer and then dissolves away the template to reveal the pattern in resist. While this process has already found commercial application in the manufacturing of optoelectronic consumer components through semi-manual means, its transition for mainstream and demanding applications is enabled through automated equipment. Through a conformal method of contacting the polymer template to the wafer, a press-unit with automated wafer and template loading is described that achieves full wafer patterning at the rate of sixty per hour, to a line/space resolution of 25nm on 70nm pitch with a resist height of 70nm and a residual layer less than 20nm. Addressing challenges in contact methods of patterning, this cost-effective molecular transfer system is designed for applications that require a single layer of patterning on full-wafer substrates, which includes those with a significant amount of pre-existing topographical variation on the substrate, both higher-frequency patterns and general non-uniform topography across the substrate. Full-wafer nanopatterning results are presented on silicon substrates ranging from 50mm to 200mm, including patterns of 50nm half-pitch lines/spaces and multi-level three-dimensional patterns relevant to photonics, display and data storage applications.

In addition to the water-dissolvable template process, another unique characteristic of the molecular transfer lithography process, enabled with the automated tool-set, is the elimination of the need to handle wet pre-cured resists at the manufacturing facility. Since a dry bondable cured resist is pre-coated onto the water-dissolvable polyvinyl alcohol templates, which are replicated from silicon wafer master topography, and then shipped to the end-use facility, it is not necessary to stock, store and use resists, some of which contain hazardous solvents, and therefore the costs are reduced while improving convenience of use, efficiency and throughput. In this paper, the use of a dry epoxy-based resist that is bonded to the substrate by the automated press equipment using a low-temperature thermal adhesion method is described, including a discussion on its shelf-life compatible that has been demonstrated to more than a year in which the templates are photoresist coated, cured, stored, and then bonded to the substrate when needed.

7637-30, Session 7

Nanoprobe maskless lithography

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No abstract available

7637-31, Session 7

Conventional and reversed image printing in electron-beam direct-write lithography with proximity effect corrections based on dose and shape modification

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For shortening the writing time, especially in shaped Electron Beam Direct Writing (EBDW), it is crucial to reduce the number of shapes and the coverage of layout for exposure. The determination of conventional or reversed image printing according to the process integration is one of the concerns for time and cost-effective process in the EBDW lithography.

A study examining values such as CD control and registration errors has done for the both types of printing in EBDW.[1] The comparison of proximity effect correction (PEC) based on the dose and shaped modification either has been investigated in conventional images. [2] However it is not clear yet how well the known dose and shape modification PEC is working in conventional and reversed image printing. Furthermore it is expected this will be issued again in the future multiple beam developments and its applications.[3]

We have prepared the test patterns for conventional and reversed image printing. The two different PECs, dose and shape modification, were applied to each case of images using a same point spread function (PSF). It is used the MGS/PROXECCO for the preparation of exposure data mentioned above. Figure 1 shows the examples of prepared test patterns, two different images with two different PECs, for the exposures. The Vistec SB3050 shaped electron beam direct writer is used for the exposures of test patterns. The line edge roughness (LER), line width roughness (LWR) and CDs have been measured and imaged with an Applied Materials VeritySEM 4i. The CD comparisons that are obtained with the conventional image between the PEC of dose modification and that of shape modification are represents in figure 2.

In summary, we examined the capabilities of the different PEC, one based on dose modification and the other with shape modification, onto the different types of pattern, conventional and reversed image. It also shows the influences of PEC to LER and LWR in both images. Finally, we will suggest the strategies of efficient PEC for the EBDW of contrasting images and propose the available method of PEC for further multiple EBDW developments.

7637-32, Session 7

Full-chip e-beam lithography proximity effect correction modeling

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As the micro-electronics industry continues to shrink the size of the devices in integrated circuits, electron beam lithography is used more extensively either for direct wafer write or for mask fabrication, hence proximity effect correction (PEC) in e-beam lithography (EBL) for large layouts and masks is becoming more urgent. EBL point spread function (PSF) parameters such as forward scattered electron exposure distribution and backscattered exposure distribution are needed for aerial image formation to allow PEC to mimic the EBL effects. Usually for parameter determination special patterns are exposed, for which the proximity function can be solved analytically, allowing one to fit experimental results. In general, the forward scattered electrons exposure distribution, the backscattered exposure distribution, and their ratio are depend on electron energy E, atomic number, atomic weight, density, resist thickness, substrate, etc. Exact values of the parameters are needed for successful correction of the proximity effect in EBL. In this work EBL PEC models are developed for a full-chip layout. The PSF parameters can be extracted from the optimized EBL model. The main idea behind the method is model-based analyses and interpretation of non-corrected representative patterns generic pattern distortions in order to achieve the best possible matching of these effects with extracted empirical data. This method allows the

PSF parameters to be determined without the need for any special experimental test structure exposures or Monte-Carlo simulations. The EBL PEC model uses 3 or more Gaussian PSF convolution with representative patterns and resist development model. Model fits for various EBL effects will be demonstrated.

7637-33, Session 7

Description of the future data preparation and proximity effects corrections platform for multibeam lithography

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The incessant rise of optical lithography mainly due to the high cost of equipment and mask complexity pushes IC makers to think about alternative lithography options. Some engineering developments as design for manufacturing, computational lithography, source-mask optimization continue to extend the optical lithography limits for a while despite a constant manufacturing cost and complexity increase. Recent workshops and conferences in semiconductor lithography underlined that direct write lithography is one option to support sub-32nm technologies and tackle this cost trend [1]. Obviously, the direct write approach based on a variable shaped beam principle (VSB) is not sufficiently promising in terms of throughput. Massively parallel electron beam direct write systems under development today present a more attractive throughput perspective [2]. Beginning of 2008, the European Commission launched an integrated program "MAGIC", to support the take-off of this technology. The main objective of this project, gathering several IC manufacturers, is to bring multi-beam systems on its path to industrial maturity by the end of 2010.

This paper will give the global status of the data preparation and proximity effects of the current European ML2 platforms (5keV and 50keV approaches) being under development through the MAGIC program. As for the current standard electron beam direct write, the data preparation time, fracturing methodology and the influence of proximity effects represents critical parts that needs to be properly controlled. Experiments performed on both MAPPER and IMS nanofabrication pre-alpha tools show the needs to set a robust proximity effects correction methodology. We will give the last results obtained with the two platforms to pattern features based on 45nm and 32nm design rules. Each step of the data preparation flow will be described in details in this paper (from the design files until the final format ready for exposure). The overall data management and the files size being a critical item of the ML2 technology have to be controlled tightly for a manufacturing success. This paper will show what needs to be done. Finally, this work will state on the solutions to be deployed to study e-beam proximity effects for sub-32nm technologies and its possible influence on the data preparation cycle time.

The research leading to these results has received funding from the European Community's Seventh Framework Programme (FP7/2007-2013) under grant agreement n° 214945 - MAGIC

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7637-34, Session 7

New proximity effects correction strategy for critical designs of sub-22-nm nodes SRAM cells using VSB lithography

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The electron beam direct write (EBDW) lithography represents a strategic solution to support the early stage of the development of the new technology node. Those anticipated studies of advanced devices allow at low cost a faster learning on the required process developments [1]. To deal with the aggressive specifications of advanced nodes, EBDW lithography made the last years significant improvements in term of tool, process and resist performances, but also in the field of proximity effects controls. Several papers have shown that this last point is a strategic item which needs to be studied very tightly taken into account several parameters coming from the design, process, resist, tools, wafers. Several works [2,3] on data management and proximity effects controls permitted to demonstrate lithography capability down to the 32nm node. But for the 22nm node and below, the SRAM cells density and the design complexity emphasize the resolution limitations, especially if we have a careful look on the line end shortening (LES), isolated/dense bias (IDB) and CD linearity. All combined, they lead to a strong reduction of the process window. A new strategy needs to be deployed to tackle with the requirements asked by these aggressive design rules.

In this paper we will detail a new methodology to control the E-Beam proximity effects for those sub22nm nodes layouts. In a first part, a status of the current proximity effects correction methodology will be detailed. We will see that the current solution show deep limitations mainly due to a drop of the contrast value. A new methodology to avoid this contrast loss and thus allowing a better control of the proximity effects will be highlighted. This paper will propose a new process flow improving the EBDW proximity effects control models for the sub 22nm nodes. Results obtained with the critical layers of the 22nm node as the active, poly, contact and metal 1 levels will be shown. Figure 1 shows advanced patterning results obtained of the two first levels with this new solution. In both cases, a better control of the proximity effects can be seen as the overall CD errors is below 3nm and the line end shortening being below 5nm. We will also highlight how this solution can give a great flexibility down to, at least, the 16nm nodes with large energy latitude.

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7637-35, Session 8

Biomolecular architectures and systems for nanoscience engineering

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No abstract available

7637-36, Session 8

Performance evaluation of MOSFETs with discrete dopant distribution by one-by-one doping method

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This paper presents the fabrication and measurements of MOSFETs with various dopant distributions. Phosphorus-ions are "asymmetrically" implanted into one side of channels both with ordered and random distribution by single-ion implanter with capability of one-by-one doping. We observe deviation in subthreshold current when interchanging the source and drain terminals; larger current when dopants are introduced at drain-side than source-side.

In the 22-nm node technology node and beyond, the transistor channel region will contain small number of dopants and the uniform distribution models are no longer available. The result of this random discrete dopant distribution is significant-and inescapable-statistical fluctuation in the device performances. Numerous theoretical analysises regarding the random dopant fluctuation have been reported since 1990s. However there are few experimental studies for better understandings of the discrete nature of dopants. We have fabricated devices with ordered dopant arrays and demonstrated performance improvements. In this paper, we report fabrication of the devices with various dopant distributions and measurements of their current, focusing on the relationship between the current density and asymmetry of the dopant distribution.

The devices were fabricated on silicon-on-insulator (SOI) substrates with the initial doping concentration of 1E15 cm-3, which is low enough to observe effects of subsequently implanted ions on the electrical characteristics. The dopants are placed at only one side of the channels (source or drain-sides) with both ordered and random distributions. Phosphorus ions were implanted at 60 keV with dose of 1E11cm-2, yielding about 10 dopants in the implanted region of 100 nm x 100 nm. To electrically activate the implanted ions, the samples were then lamp-annealed at 900   for 1 min in N2. The influence of asymmetry of dopant placement on the drain current was evaluated by measuring the drain current difference before and after interchanging the source and the drain terminals.

Id-Vg characteristic of the devices with asymmetric dopant distribution shows the small deviation of the current in the subthreshold region by before and after interchanging the source and drain terminals, which correspond to the cases where the implanted region is the source and drain sides, respectively. We found that all the measured devices showed the same tendency; the current became larger when the dopants were located at the drain side. The drain current increases when the dopant atoms are distributed in the drain-side, particularly significant for the narrow width devices. We believe that this enhancement in current is caused by the suppression of injection velocity degradation in the source-side, which coincide with a theoretical prediction. We have also observed larger larger enhancement for the ordered distribution case in a range of several 10%, and more detailed investigation are in progress.

The impact of asymmetric dopant distribution on drain current has been experimentally investigated for the first time. We found that the subthreshold current is sensitive to the discrete dopant distribution, and the subthreshold current was always larger when the dopants are located at the drain side than at the source side for both ordered and random distribution cases.

7637-37, Session 8

Surface electron-emission lithography system based on a planar type Si nanowire-array ballistic electron source

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Surface electron emission lithography system (SEL) has been developed for high resolution parallel EB lithography. The Parallel EB lithography is performed on a 1:1 electron stepper. A planar type silicon nanowire array ballistic electron emitter (PBE) is employed as a patterned electron emitting mask in this system. The PBE projects the pattern on the target wafer in the electron optics of parallel electric and magnetic fields. In the electromagnetic fields, the emitted electrons from PBE follow spiral trajectories. If all emitted electrons have same initial velocity, they are focused at the same point. The pattern of the mask on the PBE is reproduced on the target wafer at a distance of the n (n=1, 2, ...) cycle of the spiral motion of the electron. The replica of the pattern is provided with an exposure time below 1sec. We have confirmed the exposure resolution below 30 nm in the test bench. The experimental exposure was performed over 10 mm square area.

The diffraction limit of this system is very high: l/NA=0.01 nm for 10 kV accelerating voltage. Since there is no aperture stop in this system, it becomes NA=1. Practical resolution is limited by the chromatic aberration in this system. We can improve the resolution either by reducing the initial energy spread and emission angle dispersion of the emitted electrons from PBE because of the characteristics of ballistic electron emission. We also demonstrated that the combination of high electric field and high magnetic field provides high resolution in the last report1. Increasing the strength of the electromagnetic field leads to decreasing the chromatic aberration in this electron optics. Under the electromagnetic field conditions with accelerating voltage of 30 kV and magnetic field of 0.36 T between PBE and target wafer, the estimated resolution becomes below 10 nm.

The position of the PBE and target wafer is adjusted with stages. The magnetic field parallel to the electric field is generated with Helmholtz-type magnets. SEL system has subsystems for focusing, alignment and PBE-target parallelism control. In order to focus patterned electron beam on the target, the system controls the electomagentic fields with compensators and the relative position of the PBE-target wafer. The compensators are composed of deflectors. The position of the PBE (xq, yq, z) is adjusted using 3 axis piezo-electric actuators according to the signals from the height sensors. PBE-target wafer alignment is carried out using the backscattered electron signals generated from metal marks on the wafer. In this report, we demonstrate the high resolution parallel lithography and the functions of the EB stepper (focusing, alignment and parallelism control).

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7637-38, Session 8

High-throughput maskless nanolithography using flying plasmonic lens

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Previous work was published by Nature Nanotechnology 3, 733 (2008). In the past year, we have been working on achieving better resolution aiming towards implementation of this novel nano-manufacturing tool.

Here we report a novel high-throughput maskless nanolithography using plasmonic lens levitated by advanced airbearing designs at ~10 meter/second. A plasmonic lens concentrates short wavelength surface plasmons into a sub-100 nm spot. The nano-scale focusing only exists at the near-field of the lens, typically 10-100 nm, making high-speed scanning of such arrays very challenging. Therefore, a unique air-bearing was desgined that flies the lens arrays 10 nm above the surface of a spinning disk with speeds of 4-12 meter/second. We experimentally demonstrated the capability of patterning 50 nm features and simulations show that the theoretical resolution limit can reach down to 5-10 nm8. This low-cost nano-fabrication scheme has the potential of a few orders of magnitude higher throughput than current maskless techniques, and promises a new route towards next generation nano-manufacturing. Besides its application in nanolithography, this technique may also apply to optical and magnetic data storage to achieve two orders of magnitude higher capacities in the future.

7637-60, Poster Session

Full-area pattern decomposition of self-aligned double patterning for 30-nm node NAND FLASH process

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Self Aligned Double Patterning (SADP) has the advantage of dense array definition with good pitch control and is hence useful for memory devices; but its feasibility of two-dimensional circuit patterns definition is restricted on the other hand. In SPIE 2009 [1], we had proposed the ideas of 30nm node NAND FLASH cell circuit critical feature (pickup, gate, contact array) definition by decomposing the target patterns to SADP defined dense array in conjunction with cropping and/or periphery masks steps, based on manual design. The concerns of process integration as well as SADP alignment algorithm for each mask step were investigated and countermeasures were presented.

In this paper, the previous works on manual-based pattern decomposition are extended to a more sophisticated use on full-area NAND FLASH critical layer layout decomposition by utilizing an automated electronic design (EDA) tool. The decomposition tool together with OPC and simulation tools are integrated to optimize the lithographic performance of local critical patterns in each decomposed mask step, and comparisons have been made as well to investigate the differences in layout splitting algorithm between EDA-based and

manual-based decomposition. Finally, the full-area (9350×12800um) layout decomposition has been successfully demonstrated on NAND FLASH critical layers (Gate and Metal) by using the EDA tool with improved 2D structure handling algorithms.

7637-61, Poster Session

A novel lithography process for TSV (through silicon via) using an optical direct-writing exposure system

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A novel lithography process for TSV (Through Silicon Via) was developed using an optical direct-writing exposure tool. A combination of the optical direct-writing exposure tool of Dainippon Screen MFG. Co., Ltd. with an infra-red alignment system and a resist coater of Tokyo Ohka Kogyo Co., Ltd. provides the lithography process for TSV. The infra-red alignment system allows a direct detection of alignment marks both on front-side and back-side of wafer, and consequently allows feasible micro-fabrication for TSV using the reversed wafer. The lithography process demonstrated 300mm wafer CSCM (Chip Scale Camera Module) development.

7637-63, Poster Session

3D optical nanofabrication at /130 for templates used in nanoimprint lithography

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In this paper we will discuss sub-5 nm resolution of 3D optical nanolithography based on fluorecent photosensitive glass-ceramic[1].

Imprint lithography, compared to other sub 32nm CD lithography methods, the resulting high resolution, high throughput through clustering, 3D patterning capability, and low process complexity makes it a widely accepted technology for patterned media as well as a promising mainstream option for future CMOS applications.

However, nanoimprint lithography involves some difficulies regarding templates fabrication (expensive cost and time-consuming to produce). The EBL and FIB techniques, used to produce templates, have been applied to various applications such as prototyping or small amount production of electronic devices. Many methods have been proposed in the past to replace template fabrication by EBL or FIB. Recentlly, R. Menon [2] used Absorbance Modulation to produce lines with an average width of 36nm.

In this presentation we will show the resolution capability of 3D optical nanolithography based on fluorescent photosensitive glass-ceramic. Experiments sustain 5 nm resolution (AFM, HRTEM, SEM) obtained by a Laser Direct Write system operating at 650nm. The writing speed could attain 20m/s. Different patterns have been 3D recorded inside fluorescent photosensitive glass-ceramic samples (disc diameter: 80mm; thickness: 1mm).

Based on these results, we are able to present an optimized material featuring a significant improvement of the resolution needed for cost-effective solution of nanoimprint lithography templates. Fluorecent photosensitive glass-ceramics, and the processes associated with their fabrication into working templates, should facilitate the movement of nanoimprint lithography into industrial applications.

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[2] L. Andrew, H-Y. Tsai & R. Menon, Science 324, 917 (2009).

7637-64, Poster Session

Architecture for next-generation massively parallel maskless lithography system (MPML2)

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Electron-beam lithography is promising for future manufacturing technology because it does not suffer from wavelength limits set by light sources. Since single electron-beam lithography systems have a common problem in throughput, a multi-electron-beam lithography (MEBL) system should be a feasible alternative using the concept of parallelism. In this paper, we evaluate advantages and disadvantages of different MEBL system architectures, and propose our novel Massively Parallel Maskless Lithography System, MPML2.

MPML2 system is targeting for cost-effective manufacturing at the 32nm node and beyond. The key structure of the proposed system is its beamlet array cells (BACs). Hundreds of BACs are uniformly arranged over the whole wafer area in the proposed system. Each BAC has a data processor and an array of beamlets, and each beamlet consists of an electron-beam source, a source controller, a set of electron lenses, a blanker, and a deflector. These essential parts of beamlets are integrated using MEMS technology to increase the density of beamlets and reduce the system cost. The data processor in the BAC processes layout information coming off-chamber and dispatches them to the corresponding beamlet to control its ON/OFF status. High manufacturing cost of masks can be saved in maskless lithography systems, however, immense mask data are needed to be handled and transmitted. Therefore, we apply data compression technique to reduce required transmission bandwidth. The compression algorithm is fast and efficient so that the real-time decoder can be implemented on-chip. Consequently, the proposed MPML2 can achieve 10 wafers per hour (wph) throughput in 300mm wafer.

7637-65, Poster Session

Nanoimprint template fabrication using wafer pattern for sub-30 nm

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It is necessary to form sub 30nm quartz template for high resolution nano imprint lithography (NIL). Various fabrication methods such as e-beam lithography, edge lithography, and focused ion beam lithography have been studied [1-3]. However, it takes long time and cost much for conventional methods to deliver a NIL template because features on NIL template are 4X smaller in size and larger in density than those on the projection optical lithography mask for which drawing time and cost are in medium level. In this paper, we report that realizing sub 30nm NIL template would be possible using low cost and simple fabrication method.

Using conventional Gaussian beam electron beam lithography, it could take several days to drawing sub-30nmHP resolution template. It is also difficult to transfer e-beam fabricated sub-30nm features on to Qz substrate by etching process. We propose low cost and simple fabrication process to make high resolution NIL template features using wafer pattern replication. We fabricated sub-30nmHP poly-silicon lines and spaces on silicon wafer using multiple patterning technique. Then this wafer pattern is replicated to NIL template using NIL technique.

Several types of features are being studied to be realized as a template using such kind of triple patterning technique described above. Wafer printing will be tried and analyzed using the template out of this study.

7637-66, Poster Session

CP-based EBDW throughput enhancement for 22-nm high-volume manufacturing

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Rising mask cost threatens the profitability of custom LSI especially for 65nm node and beyond. EBDW with character projection (CP) function is one of the most promising technologies to the solution of this issue. We have already established the basic technology for 65nm and 45nm [1].

However, drastic improvement of throughput is indispensable for HVM (high volume manufacturing).

Recently some multi-beam EBDW approaches for volume production, such as MAPPER, PML2 or REBL are actively studied.

On the other hand, multi-beam approach of MCC [2] seems to be most practical from the view point of the extension of single beam CP based methodology which we have already introduced to device production. But drastic enhancement approach is indispensable to attain higher throughput of 5-100 WPH for 28nm node and beyond. The three key factors are the multi-beam number, the cluster chamber number and the CP shot count reduction rate.

The number of multi-beam columns should be more than 100 to attain enough through-put for volume production by our estimation. As for cluster, we think its easiness is the main feature of MCC which we expect as the high volume manufacturing tool. Electrical columns should be discretely placed within a wafer at the narrow pitch of 25mm or below to keep the beam numbers at the value of more than 100. So this system could work with very small stage stroke which corresponds to the position pitch of each column and requires very small floor space.

As for CP shot number reduction, we have already announced the EB friendly approach of DFEB tracing back to upstream design flow [3], but needs more advanced methodology of CP based RDR (restricted design rule) to attain higher shot count reduction which we will report in this work.

Preliminarily, from our production experience, we estimated the exposure CP shots and resist sensitivity trend for 28 nm node and beyond. Then we extracted the factors to attain the throughput target. In this report, we show the estimation results of beam number, cluster chamber number, CP reduction rate, and current density to attain the throughput of 5-100 WPH by MCC.

Except for throughput, we examined the countermeasures against resolution limits.

For the higher productivity, we have already introduced the following features such as infrastructure of proximity effect correction tool and charge-up stabilizing system for both CD and overlay accuracies at 50kV CP exposure with ozone in-situ cleaning. We will also discuss the advantages of our CP based EBDW system from the above features.

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7637-67, Poster Session

Monte Carlo modeling of BSE reflection in e-beam writers

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The reflection of back-scattered electrons (BSE) at the objective lens of an electron beam writer leads to a diffuse resist exposure which extends over several millimetres. The deposed energy of this unintentional exposure is much lower than the direct one. However, if the area of the direct electron beam exposure is large enough the accumulated energy is no longer negligible and may cause significant CD variations. Therefore, it is of crucial importance to study possible ways of reducing this dose contribution to a minimum and in order to perform a correct proximity correction targeting to determine its radial distribution.

In this work a model of a 50kV E-Beam writer was developed, consisting of a resist-coated silicon wafer and an opposing low-reflection disk mounted at the pole piece of the objective lens. In order to improve the low-reflection disk, different material compositions (see Figure 1) as well as optimized surface topographies of the disk are modeled. We also analysed the resulting energy dose as a function of the wafer radius (see Figure 1). For simple unstructured cases a comparison of the experimental and simulated radial dose distributions is performed too.

All simulations were executed using the Monte Carlo simulation program MCSEM, which was developed at the PTB for the modeling of electron beam - specimen interactions. This program is written in C++ and uses object-oriented programming techniques. The simulation program uses a modular design, thus individual modules can be easily exchanged and adapted to new simulation tasks. It is possible to apply various physical models for elastic and inelastic electron scattering. MCSEM allows to be utilized for modeling of electron beam imaging (e.g. in scanning electron microscopy) as well as for electron beam lithography. Complex three-dimensional specimen structures can be integrated in the model.

7637-69, Poster Session

Investigation of pre- and post-etch feature characteristics using UV cure as a pitch doubling stabilization technology for the 32-nm node and beyond

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Pitch doubling technologies are seen as necessary for the 32nm node and beyond in order to extend optical lithography. Many different techniques have been examined including Litho-Litho Etch (LLE), Litho Etch, Litho Etch (LELE), and Sidewall Image Transfer (SIT). Keeping all of the processes inside the litho cluster (as LLE does) automatically allows for the lowest cost of ownership for pitch doubling. Within LLE alone, there are varying approaches from spin on chemical freeze materials to thermal cure, UV curable materials, among others. The challenge is to provide robust process performance while still achieving the lowest cost of ownership.

For this paper, we are concentrating on the UV cure process. Our findings are the results of optimization of the UV cure dose and bake conditions and it's affect on the lithographic performance. The optimized process was investigated for defectivity, CD, repeatability, pattern distortion, through etch performance and readiness for high volume manufacturing. With respect to CD, the investigation included absolute value change (shrinkage or growth) and CD uniformity (CDU). For pattern distortion, we investigated line shrinkage, corner rounding, and line end pull back. Defectivity checks were conducted for full wafer comparison of with and without the UV cure process. Manufacturability measures include throughput, cost of ownership and process stability.

7637-70, Poster Session

Model-based proximity effect correction for electron-beam direct-write lithography

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A model-based proximity effect correction methodology is proposed and tested for electron-beam-direct-write lithography. It iteratively modulates layout geometry by intensity-based feedback compensation until the correction error converges. The energy intensity distribution is efficiently calculated by fast convolving the modulated layout with a point-spread function which models electron beam shape and proximity effects primarily due to electron scattering in resist.

The effectiveness of this methodology is measured by iteration numbers required for meeting the patterning fidelity specifications in International Technology Roadmap for Semiconductors. It is examined versus process parameters including acceleration voltage and resist thickness with several regular mask geometries and practical design layouts. Preliminary experimental results indicate that electron proximity effects can be well corrected for the 32-nm half-pitch node and beyond.

7637-71, Poster Session

Step and repeat high-resolution large-area master fabrication utilizing working stamps from EUV-IL fabricated master templates

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Nanoimprint lithography (NIL) is used in R&D environments for the fabrication of a range of devices such as waveguides, ring resonators and hard discs. Since the first publication [1] NIL has experienced a rapidly growing interest in many applications. Its key benefits are the resolution of fine features of smaller than 50 nm at low cost. Therefore is has been acknowledged by leading experts and was put onto the International Technology Roadmap for Semiconductors (ITRS) as prospective next generation technology for the fabrication of nano-electronics devices at the 32-nm node and beyond. Herein we report on imprinting of 35 nm half pitch line and space structures, from a template fabricated by extreme ultraviolet interference lithography (EUV-IL). This template (Fig. 1) was replicated in a polymer working stamp and imprinted in a step & repeat (S&R) mode. Rigid templates are conventionally fabricated using electron beam lithography and subsequent reactive ion etching, which is a time consuming and therefore expensive process [2]. EUV-IL is a new, higher throughput technology for the fabrication of periodic nano-patterns with half pitch structures below 50 nm [3]. In EUV-IL two or more coherent EUV beams are crossed to form interference pattern, which are recorded on a photo resist film. Interference of two beams leads to the formation of linear gratings while interference of three or more beams creates 2D patterns such as a grid or an array of dots. The interfering beams are obtained from a single EUV beam by transmission diffraction gratings. Polymer working stamps were fabricated from these valuable templates to avoid the risk of damage during a direct patterning process. These polymers are cheap, disposable materials, which can be fabricated quickly compared to the production of the template [4]. Their main advantages are based on its high transparency, flexibility and low surface energy, which do not require surface treatment due to the anti sticking nature of the molecules' end group of the stamp material [5]. The step-and-repeat system imprints small areas (called dies) of a wafer at a time and then moves to a new area of the wafer. The process is repeated until the entire wafer is imprinted. One advantage of the step-and-repeat method is the achievable higher alignment accuracy on smaller areas than on larger areas. A second advantage, and probably the most significant for many applications, is that it allows the use of small high resolution templates to create large area imprints. In case of whole wafer templates the master die pattern is fabricated using conventional techniques. The structure, pattern fidelity and critical dimension uniformity of the master, replicated polymeric stamp and patterned wafer will be shown. A high-quality 1 inch x 1 inch template can be prepared with EUV-IL or e-beam technology depending on the pattern requirements. Using step-and-repeat imprint lithography, this template can be used to pattern a much larger substrate (e.g., a 200 mm wafer) in fractions of an hour. Fig. 2 shows 35 nm half pitch line and space structures on a polymeric stamp. The 35 nm polymeric stamp is bonded onto a S&R template (6,25 cm x 6,25 cm) for handling in the equipment and replicated multiple times on 200 mm substrates. Due to the ability of the S&R system to actively control and measure the embossing and de-embossing force [6], properties such as degradation of anti sticking behaviours and imprint force against residual layer thickness can be as well recorded and adjusted.

This paper will provide detailed information on the pattern fidelity from master template to the final imprint, residual layer thickness and uniformity as well as polymer properties concerning anti- sticking behaviour and durability.

7637-72, Poster Session

High-volume manufacturing of nanoimprint lithography produced devices: addressing the stamp supply challenge

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High volume manufacturing using Nano Imprint Lithography requires a steady supply of stamps. This is one of the keystones in the industrialisation of Nano Imprint Lithography. Obducat's Nano Imprint Lithography systems have developed into an enabling platform for next generation optoelectronic devices.

In order to realise industrial level manufacturing, one of the key challenges is to supply the high volume machines with stamps or molds. The master mold is typically time consuming to produce and thus expensive. It is therefore critical to be able to use each master mold for as many imprints as possible without losing yield. This can be achieved in several ways. Perhaps the two most significant is stamp replication (i. e. the ability to produce many copies from one master stamps) and for each stamp copy to deliver as many imprints as possible without losing yield. Another often forgotten but still important aspect of volume manufacturing using Nano Imprint Lithography is handling of stamps and substrates. Using Sindre 400, the world's first truly industrial automated production platform, manual handling of stamps and substrates are almost completely avoided, which, together with advances in stamp replication significantly lowers the Cost of Ownership for manufacturers.

Currently, stamp replication is an area of intense development. How to replicate a stamp and how many replicas that can be achieved from each master depend both on feature sizes as well as aspect ratio of the structures. Several different techniques can be combined in order to obtain a large amount of stamps from each master stamp. Combinations include master stamps of different materials, electroplating to obtain Nickel copies as well as imprint on substrates followed by etching. The ability to combine several different techniques enables the choice of the ideal technique suited for each structure type.

This paper will focus on how to adress stamp replication challenges in order to secure an adequate supply of stamps to enable high volume manufacturing using Sindre 400. The paper will present results on the number of stamps that can be manufactured from each master as well as how long each individual stamp is able to produce nanostructured surfaces without losing yield.

7637-73, Poster Session

Operation and performance the CNSE Vistec VB300 electron-beam lithography system

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At the end of 2008, the College of Nanoscale Science and Engineering (CNSE) formally accepted a Vistec VB300 Gaussian electron beam lithography system. The system is a key component of the overall lithography strategy of the College and complements existing state of the art tooling for 193nm immersion, Extreme Ultra Violet and nanoimprint. The demonstrated resolving power of the system easily exceeds that of the facility's scanners. Together with 300mm wafer compatibility and a class 1 mini environment, the system is well poised to execute its primary mission of supporting a variety of programs in post CMOS device integration. For a 300mm tool to be able to exchange wafers with other tooling in a full flow line it is necessary to pass stringent backside metal contamination testing. TXRF (total reflection x-ray fluorescence) testing performed with 300mm wafers on the VB300 satisfied the permitted metal contamination levels and cleared the way for introduction of ebeam patterned wafers into the process flow. Most of the tooling in the 300mm line handles wafers in front opening universal pods (FOUPS). With the relatively low

throughput of the system (hours per wafer, not wafers per hour), this type of interface is not required. In order to maintain a low level of defects, 300mm wafers are removed from the FOUPS in the class 1 mini environment and loaded into the system.

In addition to the 300mm capability, the system supports a wide range of wafer sizes, photomasks and piece parts. This enables the platform to support the 200mm activities at the College as well as the small samples frequently encountered with novel materials that have no support tooling available for 200mm and 300mm wafer sizes.

The VB300 platform readily met the Vistec standard acceptance test specifications. The paper will present further details of the acceptance test together with examples of additional work in progress that includes implementation of rigorous tool monitor standards, true grid exposures for mask patterning, imprint template fabrication and mix and match overlay between the VB300 and optical patterning tools.

7637-74, Poster Session

Throughput enhancement technique for MAPPER maskless lithography

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MAPPER Lithography is developing a maskless lithography technology based on massively-parallel electron-beam writing with high speed optical data transport for switching the electron beams. With 13,000 electron beams which each deliver a current of 13nA, a throughput of 10 wph is realized for 22nm node lithography [1]. By clustering several of these systems together high throughputs can be realized in a small footprint. This enables a highly cost-competitive alternative to double patterning and EUV.

The most mature and reliable electron source currently available that combines a high brightness, a high emission current and very uniform emission is the dispenser cathode. For this electron source a reduced brightness of 106 A/m2SrV has been measured, with no restrictions on emission current [2]. With this brightness however it is possible to realize a beam current of 0.3nA (@ 25nm spotsize), which is almost a factor 50 lower than the 13nA that is required for 10 wph.

Three methods can be distinguished to increase the throughput:

1) Use an electron source with a 50x higher brightness

2) Increase the number of beams and lenses 50x

3) Patterned beams: Image multiple sub-beams with each projection lens

MAPPER has selected option 3) ‘Patterned beams’ as the method to increase the beam current to 13nA. This because an electron source with a 50x higher brightness is simply not available at this time, and increasing the number of beams and lenses 50x leads to undesirable engineering issues.

During the past years MAPPER has been developing the concept of ‘Patterned beams’. By imaging 7x7 sub-beams per projection lens the beam current is increased to the required 13nA level. This technique will also be used to maintain throughput at 10 wph for smaller technology nodes by further increasing the number of sub-beams per projection lens.

In this paper we will describe the electron optical design used to image these multiple sub-beams per lens, as well as experimental demonstration of this electron optical configuration. Also the writing strategy will be discussed that will be used, as well as the first patterning results. One of the key components for ‘Patterned beams’ is the beam blanker array, since each sub-beam must be switched on and off individually. The design of the blanker deflectors, the circuitry, as well as experimental results of the blanker will be shown. Finally the roadmap to further technology nodes will be discussed.

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7637-76, Poster Session

Electron-beam lithography(EBL) for design and fabrication of Si-based photonic crystal stamps

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In this work we report on using e-beam lithographically technology for enabling the mass replication of custom-designed and prepared structures via establishing nanoimprint processes for pattern transfer into UV curable pre-polymes. By EBL, the new nano-fabrication technology based on the concept of disposal master technology (DMT) is suitable for mass volume manufacturing of large area arrays of sub-wavelength photonic elements.

To show the potential of Electron beam lithography On the nanoimprint technologies ,we choose as an example the fabrication of a photonic crystal (PhC) structure with integrated light coupling devices for low loss interconnection between PhC light wave circuits and optical fiber systems. We will present two kind of PhC for fabrication of nanoimprint Electron beam lithography stamps in Si. (a) a photonic crystal of Si-rods in air optimized in that with electron beam lithography (EBL) pattern create on resist and after lift-off, there is a mask of Cr on Si, then the pattern transfer into Si was performed using reacting ion etching (RIE) with SF6 as etch gas. We use 200nm of positive resist 950K PMMA for EBL exposure. Resist thickness, exposure dose, development time and parameter for etching have been optimized in this method was fabricated (b) in the second method lift-off was not performed and metal mask was used as master. The subsequent steps of EBL for fabricating the master will be presented detail in our contribution.

7637-77, Poster Session

A first order analysis of scatterometry sensitivity for NIL process

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It is necessary and important to control the residual layer thickness (RLT) in order to keep a high -resolution performance for nano imprint lithography (NIL). And scatterometry is one of the CD measurement meteorology tools for NIL process (including RLT-measurement). In our earlier paper, the CD measurement results of resin patterns of 90, 65, and 45nm half pitch (HP) by not only a scatterometry tool but also the cross section of CD SEM have been reported. In this paper, the first order analysis of the scatterometry sensitivity up to 45nm HP resin pattern and beyond by using RCWA (Recognized Coupled Wave-analysis) simulation is described. The criterion of this analysis is defined as the quantification of the sensitivity comparing with 65 nm HP resist pattern of ArF immersion process. And this criterion is the sum of the absolute difference of the reflectivity values between the nominal and varied conditions thorough the spectrum, which are used in scatterometry tools. Furthermore, the simulated result in this analysis can be used to discuss the extendibility of scatterometry.

7637-40, Session 9

Optical maskless lithography

T. Sandstrom, Micronic Laser Systems AB (Sweden)

No abstract available

7637-41, Session 9

Multishaped beam proof of lithography

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Maintaining the rapid pace of half pitch reduction and increasing integration density of integrated circuits down to the 22nm node and

beyond requires the development of next-generation lithography (NGL) such as EUV, nanoimprint lithography and maskless lithography (ML2). Additionally, more complicated masks will be needed, which will require new and improved mask-making equipment too [1]. For ML2 several revolutionary electron-beam lithography concepts are under development since several years [2], [3]. For mask-making the leading equipment suppliers seem to be focused on a continuous enhancement of their Variable Shaped Beam (VSB) systems so far [4].

In this paper a full package high throughput multi electron-beam approach, called Multi Shaped Beam (MSB), for applications in mask making as well as direct write will be presented with complex proof-of-lithography results. In contrast to fixed pixel based approaches [2-3] the MSB system operates with shaped beams of variable size analogously to the proven and mature VSB technology [5].

The concept enables a significant exposure shot reduction for advanced patterns compared to standard VSB systems or cell projection (CP). Moreover, it allows full pattern flexibility to be retained by concurrently using MSB, VSB and CP. Many field proven tool components as well as the required technology infrastructure from the established 50kV single VSB technology can be reused without modification, which keeps the technical risk on a manageable level.

Proof of lithography was demonstrated by exposing complex patterns, which required a fully operating electron-beam system including data path and substrate scanning by stage movement. The POL exposures have been performed using a setup with 4x4 (16 beamlets) MEMS deflector arrays for individual shape size control. Figure 1 shows the MSB POL-system. Further details of the configuration of the POL system especially about the fast data path as well as initially measured performance numbers will be disclosed. First exposure results will be presented (as an example see Figure 2). On the basis of real pattern analysis work some throughput estimations will be presented. Finally, the paper will give an outlook on the MSB product roadmap.

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7637-42, Session 9

Hardware implementation of Block GC3 lossless compression algorithm for direct-write lithography systems

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Future lithography systems must produce chips with smaller feature sizes, while maintaining throughput comparable to today's optical lithography systems. This places stringent data handling requirements on the design of any direct-write maskless system. To achieve the throughput of one wafer layer per minute with a direct-write maskless lithography system, using 22 nm pixels for 45 nm technology, a data rate of 12 Tb/s is required. In recent years, we have developed a datapath architecture for direct-write lithography systems, and have shown that lossless compression plays a key role in reducing throughput requirements of such systems. Our approach integrates a low complexity hardware-based decoder with the writers, in order to decode a compressed data layer in real time on the fly. In doing so, we have developed a spectrum of lossless compression algorithms for integrated circuit rasterized layout data to provide a tradeoff between compression efficiency and hardware complexity, the most promising of which is Block Golomb Context Copy Coding (Block GC3).

In this paper, we finalize the hardware implementation of Block GC3 decoder. First, we limit the bucket size of Golomb run-length code to reduce the area and avoid complex routing problems. Then, we fix the code table for the Huffman code to reduce size of the data stream and eliminate the related updating issues. With these modifications, we present the FPGA synthesis and emulation results for the Block GC3 decoder. For one Block GC3 decoder, 3233 slice flip-flops and 3086 4-input LUTs are utilized in a Xilinx Virtex II Pro 70 FPGA, which corresponds to 4% of its resources. The decoder also has 1.7 KB internal memory, which is implemented with 36 block memories, corresponding to 10% of the FPGA resources. The system runs at 100 MHz clock rate, with the overall output rate of 495 Mb/s for a single decoder.

In addition to the decoder implementation results, we discuss the other hardware implementation issues in order to integrate Block GC3 decoders into the writer system data path. Regarding on-chip input FIFO buffering, we can reduce the input data rate with a smaller memory as compared to our previous work, by utilizing the simultaneous read/write property of FIFO. Meanwhile, with additional output data buffering, we can synchronize the data between multiple decoders and writer devices, so that multiple decoders can run their own data flow without corrupting the final output. In addition, error propagation control techniques such as memory refreshing and Hamming codes are introduced to minimize the impact of error propagation caused by imperfect data retention ability of the memory. Finally, input data stream packaging is proposed to reduce the number of input data streams, which can also reduce the I/O complexity if multiple decoders are applied. This hardware data path implementation is independent of the writer systems or data link types, and can be integrated with arbitrary direct-write lithography systems.

7637-43, Session 9

Characteristics of production-worthy massive e-beam direct writing

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E-beam direct writing (EBDW) is one of the potential solutions for multiple nodes from 32nm half-pitch (HP) and beyond. In the past, its throughput limitation curbed the EBDW development mostly for small volume, prototyping purposes. It has then been proposed to achieve throughput greater than 10 wafers per hour (WPH) by a single column with >10,000 e-beams writing in parallel, or even greater than 100 WPH by further clustering multiple columns within a certain tool footprint. The MAPPER concept contains a CMOS-MEMS blanker array driven by high-speed optical data path architecture to simultaneously control more than ten thousand e-beams writing in parallel and switching on and off independently.

The Pre-Alpha Tool with a 110-beam, 5-keV column with a 300-mm wafer stage has been installed in the semiconductor manufacturing cleanroom environment and is ready for imaging test at 45-nm HP resolution. While the resolution beyond 30-nm HP by 5-keV Gaussian beam has been demonstrated by using a Lab-level tool. Characteristics of the Pre-Alpha Tool, such as beam current, spot size, focal plane deviation, and beam-to-beam (BtB) position deviation, during 110-beam simultaneously raster-scan writing have been collected. Applying dose corrections by using tool characteristic information onto each individual beam, the BtB CD uniformity is then improved. To implement the multiple e-beam direct writing in mass production, the conventional indices of describing process window such as energy latitude, depth of focus, and CD uniformity, are discussed. Similar to mask-error-enhanced-factor (MEEF), a new factor called writing-error-enhanced-factor (WEEF), to describe the impact of writing error is introduced.

7637-44, Session 9

Advances in DMD-based maskless lithography reliability below 320 nm

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Texas Instrument's spatial light modulator chip, the DMD (digital micromirror device) has been used in multiple maskless lithography applications for the past 5-7 years. Typically these applications have been relegated to PCB lithography with minimum linewidths well above

1um because of the shortened lifetime of the device at wavelengths below 365nm. Recent advances in DMD processing have made significant improvements in the operational lifetime of the DMD. This paper will cover the background of UV-A DMD maskless lithography, explain the typical lifetime failure mechanisms (both at UV-A and shorter wavelengths) and demonstrate the increased lifetime with the new processes.

Multiple papers on maskless lithography using DMDs have been published by many universities, research centers and end equipment manufacturers. Production systems utilizing the DMD have been launched by multiple OEMs, including DNS, Fujifilm and Hitachi. Typically these tools have been configured to use multiple mid to high resolution DMDs for high throughput, and operate in the 365-410nm regime. Typical operating conditions are 3-5W/cm2 illumination on the DMD, with temperature held below 30C. Using these conditions, manufacturers have been able to match the throughput on the DMD systems with the mask-based systems.

Devices have consistently demonstrated operation in excess of 3000 hours at 3.4W/cm2, 25C in the UV-A range. Failure mode is usually a build-up of residue on the surface of the mirror that results in degradation in the reflectance of the DMD surface. Decrease below 70% of nominal reflectance is considered unoperational.

The standard UV window used in current production qualified DMDs has a usable transmission over 320-400nm. To test and operate the device at wavelengths lower than this, a special window is needed with high transmissibility below 320nm. Because of the chemistries involved in the production of the DMD, operational life is strongly dependent on power density, wavelength and temperature. For testing at 311nm (UV-B) and 266nm (UV-C), the operational life of the device degrades significantly faster than UV-A. Latest performance data for both the current baseline process as well as the extended performance process will be presented.

7637-45, Session 10

Advances in roll-to-roll imprint lithography for display applications

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There is significant interest in large-area, low cost, flexible electronics for displays, RFID tags, and MEMS applications because of the escalating costs of photolithography on such large areas and the desire for light weight rugged devices. Progress has been limited because of the technical difficulty of achieving critical layer-to-layer alignment on dimensionally unstable substrates and the photolithography production bottleneck. In this talk, a solution to the problems of roll-to-roll lithography on flexible substrates is presented. We have developed a roll-to-roll imprint lithography technique to fabricate active matrix transistor backplanes on flexible webs of polyimide that have a blanket material stack of metals, dielectrics, and semiconductors. Imprint lithography produces a multi-level 3-dimensional mask that is then successively etched to pattern the underlying layers into the desired structures. This process, Self-Aligned Imprint Lithography (SAIL), solves the layer-to-layer alignment problem because all masking levels are created with one imprint step. In this paper, the processes and equipment required for complete roll-to-roll SAIL fabrication will be described. First, a polyimide web substrate containing a material stack of bottom Al, silicon oxide, silicon nitride, hydrogenated amorphous silicon, and a top Cr layer are deposited using roll-to-roll sputtering and PECVD deposition. Second, for the SAIL imprint process, a silicon master is replicated in PDMS and recombined to form a larger shim. From this shim, a full-sized stamp is cast and attached to a quartz roller which is then used in conjunction with a gravure coating head to imprint a web coated with a photopolymer masking material. Tight control of the coating thickness is necessary since the thickness has a direct effect on the uniformity of the imprinted mask and the allowable margins for etching. The stamp material was chosen for good air permeability and chemical inertness. This allows us to achieve bubble-free imprints at atmospheric pressures and stamp lifetimes exceeding 2000 impressions. Control of the quartz roller and the imprint nip roller surface textures has proved to be important for imprint uniformity. Third, subsequent reactive ion etching is done in a roll-to-roll vacuum chamber in which fluorine-based plasmas etch away the silicon-containing layers and thin the imprint mask. A roll-to-roll wet etcher is used to pattern the metals. Through a series of these plasma and wet etching steps, the transistors and pixels of the backplane are defined. Working active matrix backplanes have been made using this roll-to-roll process. With this SAIL imprint process, we can reproduce features with submicron resolution on a web 1/3 m wide at speeds of 0.5 m/min and higher.

7637-46, Session 10

High-volume jet and flash imprint lithography for patterned media

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The Jet and Flash Imprint Lithography (J-FIL®)1 process uses drop dispensing of UV curable resists for high resolution patterning. Several applications, including patterned media, are better, and more economically served by a full substrate patterning process since the alignment requirements are minimal. Patterned media is particularly challenging because of the aggressive feature sizes necessary to achieve storage densities required for manufacturing beyond the current technology of perpendicular recording. In this paper, the key process steps for the applications of J-FIL to pattern media fabrication are reviewed with special attention to vapor adhesion layer application and imprint performance at >300 disk per hour throughput.

It is anticipated that bit patterned media will be required for very high density hard drives (~ 1Tb/in2). It is possible, however, that an interim solution such as discrete track media will be adopted for earlier insertion. Discrete track media consists of an array of concentric lines (or tracks), with half pitches on the order of 50nm and below. The formation of the tracks is challenging because of the line densities required over substantial distances. The focus of this paper is imprint patterning for discrete track media.

The process flow in Figure 1 depicts the process steps needed for of pattern media integration into the existing magnetic media fabrication flow. The process steps which are important for imprint success include disk cleaning, adhesion layer coating and imprinting. The adhesion promoter and imprint steps require new processing know how for the hard disk drive fabrication companies. However substrate cleanliness for imprint is an essential factor to enable high yield processes and the present cleaning techniques are generally applied to bare substrates not the sputtered films. The cleanliness requirements for the disk coming into and out of the imprint process require generally < 1 particle per disk of < 0.1 nm. Such cleanliness levels are required to experience suitable process longevity.

Low cost of ownership in the fabrication of patterned disk media (PM) is an essential requirement for manufacturing. As such a material and process enabling a vapor coated adhesion layer were developed. The as-deposited adhesion material is ≤ 1 nm thick and the coating uniformity is < 0.3 nm. The adhesion layer film growth is self-limiting so that only a monolayer forms with no excess material provided process conditions are such that material condensation is eliminated. The process requirements and performance of the adhesion layer material including associated throughput considerations necessary for achieving 1000 disks per hour are described in detail. Figure 2 demonstrates an example of the normalized adhesion of the vapor coated adhesion material demonstrating the adhesion is uniform across a full cassette owing to the vapor coating process design.

With a low cost adhesion layer available the imprint process must also deliver high throughput and favorable lithography performance for 100 nm pitch and below patterning at an acceptable cost. Figure 3 depicts feature fidelity of 100 nm pitch discrete track features where both fine pitch data tracks and large pitch servo features are patterned at the same time. An imprint tool and process capable of imprinting >300 double sided disks with exceptional lithographic quality will be described with a focus on the quality of the imprints. Imprint quality such as residual layers of < 15 nm with uniformities of < 6 nm can be

produced using the J-FIL process at high throughput. Imprint residual layer uniformity is achieved using special drop generation software which enables uniform imprinting irrespective of the pattern density. Discrete pattern media possess pattern density variations between the data tracks and servo regions that can be imprinted with uniform residual layers by applications of such drop generation algorithms. An example is shown in Figure 4. Feature fidelity of < 100 nm pitch full surface 65 mm diameter disk drive substrates will be discussed. Finally, the prospects for printing smaller bit arrays and finer track pitches will also be discussed.

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7637-47, Session 10

Nanoimprint lithography for novel memristive devices

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Transition metal oxide based resistive switches exhibit non-linear resistance that changes with the amount and polarity of applied voltage. They have recently been linked to the memristive devices as predicted over 3 decades ago [1, 2]. High density memristive device arrays with crossbar architecture [3] can be fabricated using nanoimprint lithography (NIL) [4] with high throughput and low cost, making this device family a promising candidate for the next generation non-volatile random access memory (NVRAM).

A typical memristive device consists of a thin layer of switching material (e.g., TiO2) that is sandwiched in between two metal electrodes [5]. Usually the bottom metal electrode is first deposited on a flat surface, followed by the deposition of the switching layer and the fabrication of the top electrode. Due to the thickness of the bottom electrode, a protrusion is created and preserved after the device is finished, ending up with kinks at each junction. These kinks are usually the mechanically and electrically weakest part in the devices that lead to device failure due to the heating/electromigration.

To avoid this problem, we propose and demonstrate a planar device structure that eliminates the kinks in the vertical stacks by embedding the bottom electrodes into the substrates. Consequently, the switching layer and the top electrodes are built on flat surfaces, resulting in new device geometry with a planar structure. Our electrical measurement showed that the planar memristive devices exhibit improved endurance. This new all planar structure is also easy to be integrated with other components, enabling the path to multi-stack structures.

Others novel devices such as sub-5 nm lateral memristive devices will also be discussed.

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7637-49, Session 10

Micro- and nano-patterning of functional polymers and organic monolayers by ESNIL imprint lithography

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Nanoimprint lithography (NIL) has been embraced by a number of users as a practical and cost effective means for patterning surfaces and an extensive body of work compiled thus far on NIL has shown its usefulness in producing nanoscale devices and topological platforms for various surface chemistries. While thermal-NIL and UV-NIL are effective, they tend to require special apparatus to apply heat and/or pressure during the imprint, although the cost of this equipment is a fraction of the expense of a photolithography fabrication facility. Soft-Nanoimprint Lithography (S-NIL) is a promising alternative nanopatterning approach where PDMS molds are used to imprint UV curable resist or to mold polymer films by capillary force. Despite the many successful demonstrations of imprinting into the surface of various resists by Soft-NIL, it is important to note that there is a dearth of reports of its use for true lithographic pattern transfer to fabricate useful sub-micron structures and only one report of successful pattern transfer exists which involved chemical modification of the PDMS mold surface. Hence, reports of the use of S-NIL to fabricate operating devices has been nearly non-existent or in cases where it was used, serious materials issues were encountered.

We report the exploration of a new, simpler, more reliable means of S-NIL which overcomes the aforementioned limitations on resist film thickness and does not require modification of the PDMS mold. Easy Soft Imprint Nano-Lithography (ESINL) enables the use of molds made from inexpensive PDMS in a simple and effective lithographic process to fabricate operating transistor devices. ESINL is enabled by imprinting into a thiol-ene resin (NO60) that has undergone a partial cure prior to contact with the imprint mold. This simple pre-cure prevents the resist from being absorbed into the PDMS molds and allows for high resolution pattern transfer during the ESINL process. ESINL is the first imprint technique to demonstrate the simplicity and effectiveness of PDMS molds in a true lithographic process capable of fabricating technologically useful nanostructures and as a demonstration has been used to fabricate functional transistor devices. We also report the latest results in the NIL patterning of active organic monolayers and the properties of resulting devices.

7637-50, Session 11

Tip-based nanofabrication: an approach to true nanotechnology

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No abstract available

7637-51, Session 11

Direct-write three-dimensional nanopatterning using probes

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Progress in nanotechnology is intimately linked to the existence of high-quality methods for producing nanoscale objects and patterns. Scanning probe technologies are intrinsically capable of addressing real space with atomic resolution. However, high-resolution patterning combined with sufficient throughput remains challenging. Here we present a novel high-resolution probe based patterning method exploiting organic resist materials that are highly responsive to the presence of a hot tip and react by local material desorption. Thereby, arbitrarily shaped structures can be written with e-beam-like patterning capabilities. In addition, controlled depth profiling enables the creation of 3D structures.

Two resist strategies have been studied. In the first approach a phenolic molecular glass with a molecular weight of 715Da serves as patterning layer. Below the glass transition temperature of Tg ~ 130C the material has excellent shape preserving properties owing to mutual hydrogen bonding mediated by dangling OH groups. On the other hand, the material can be readily thermally desorbed because of the low molecular weight of the monomers. Using our heated probe technology we have demonstrated reproducible material removal with

nanometer-scale precision using write-pulse durations of 5 μs and tip heater temperatures of 300-500ºC. In the second approach, the patterning layer consists of a polymer, polyphtaladehyde in our study, with a low ceiling temperature Tc ~ 150C. The polymer backbone is thermodynamically unstable, i.e., the polymer auto-unzips into its monomer constituents upon the breaking of a single bond. This process is efficiently triggered by contact to a heated tip and can be exploited to fabricate patterns in a similar way as for the molecular glass materials.

The patterning quality is excellent for both materials . The material is cleanly removed and no pile-up or redeposition of material can be detected. The patterning resolution is determined by the size of the tip. Line gratings with a half-pitch of 15 nm have been fabricated. The method does not suffer from proximity effects. Thus, arbitrary 2-D patterns represented by a simple pixel map can be readily transcribed. Moreover, the material removal can be cumulated, thereby enabling the fabrication of 3D relief structures. We have written a micron size replica of the famous Matterhorn mountain by consecutive removal of molecular glass layers. The almost perfect conformal reproduction of the original proves that the final structure is a linear superposition of well-defined single patterning steps.

The 2D and 3D structures created were transferred into silicon substrates using standard RIE technology. In addition, to enhance the aspect ratio, a three-layer transfer process has been developed yielding a vertical amplification of the written structures by a factor of 50 without significant loss of lateral resolution. Using this new technology, it is possible to fabricate complex three-dimensionally textured substrates, e.g. for the guided and directed assembly of shape-matching objects. The technique also offers a cost-effective and competitive alternative to high-resolution electron-beam lithography in terms of both resolution and speed.

7637-52, Session 11

High-throughput plasmonic lithography for sub-50-nm patterning with a contact probe

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For the purpose of high-throughput plasmonic lithography, we have designed a plasmonic contact probe that can scan on a photoresist (PR) surface without external gap control unit (Fig.1). The probe holds a ridge aperture (bowtie-shape, outline size 140nm x 140nm and ridge gap size 20nm) perforated by focused ion beam in 120nm aluminum film. The aperture generates a light spot of 50nm x 40nm in size at 10nm depth in PR, enhancing the light transmission by waveguide propagation and localized surface plasmon at opposite ridge. It is filled and covered with glass silica for protection and a spacer for keeping a physical gap (~10nm) between probe and PR during the scanning. Self assembled monolayer (SAM) is coated on the bottom surface of the silica spacer for lubrication. Without external active gap control unit, we can achieve scan speed ~ 10mm/s (Fig.2). It takes about 1hour to pattern over 1cm2 area and the throughput enhancement factor is larger than 100, compared to a conventional near-field optical probe scanning lithography. The pattern results show sub 50nm resolution arbitrary patterns. In this presentation we will introduce dense line patterns and arbitrary-shaped patterns to evaluate the performance of the plasmonic nano patterning. For the purpose of practical application, we also evaluate line pattern quality by line width roughness (3 ~ 5nm) and the results show comparable value with conventional optical mask lithography. Thus we expect this system can be developed for the purpose of small volume fabrication of photonic, plasmonic and any other nano-scale devices.

7637-53, Session 11

Maskless plasmonic lithography for patterning of one- and two-dimensional periodic features

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Photolithography has played a vital role in almost every aspects of modern technology for the past 50 years. Advances in this field have allowed scientists to improve the resolution of the conventional photolithographic techniques, which is restricted by the diffraction limit. New research suggests that we may be able to develop new low cost photolithographic technique beyond the diffraction limit. The key in achieving this goal lies in the use of a concept called surface plasmon resonance. Surface plasmon enabled lithography, which is not restricted by free space diffraction limit, is one of the potential research thrust areas as it offers the possibility for high resolution nanopatterning [1-3].

In this paper, a maskless single step multiple beams (two and four) surface plasmon interference lithographic configuration is proposed and illustrated experimentally so as to obtain interference pattern with resolution several orders less than the illumination source wavelength. This technique utilizes a custom made prism layer configuration to pattern both one dimensional (grating line) and two dimensional (dot array) periodic nanostructures on the recording medium. Both aluminium and silver metal films are used for the experimental study. The effect of angle of incidence, metal thickness and exposure depth on the pattern size fabrication will also be analyzed. Large area patterns of grating lines and dot arrays with feature size as small as 90nm on a 172nm period were experimentally obtained using an exposure radiation of 364nm wavelength, as shown in Fig.1. This technique is expected to provide a convenient route for patterning high throughput nanoscale structures without employing expensive equipments or complex mask fabrication approaches. This concept and methodology uses a prism instead of metallic grating mask as a coupler, which makes the structure of lithographic system simple and reduces the cost of fabrication. The application of this proposed concepts and methodology can find not just silicon-based pathway etchings for semiconductors, but also expects to serve a host of emerging fields that require nano-scale patterns.

7637-54, Session 11

Scaling inkjet printing to nanodimensions

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Inkjet printing is now being developed as a highly flexible method for direct additive patterning of electronic materials for electronics, MEMS, and optoelectronics applications. Current ink-jet printing systems have relatively large droplet size (>10 m diameter, or about 1 picoliter volume), and relatively small arrays of jets. For many applications, scaling down the droplet size, and hence the resolution of printed features to micro and even nanoscale dimensions would be of great benefit. Here we describe work on scaling inkjet printhead technology to droplet diameter below one micron (0.5 femtoliter). Our technology is based on monolithic silicon micro-machining fabrication methods and is amenable to large printhead arrays consisting of thousands of jets.

Our first generation printhead is composed of a large array of thermal bubble inkjet devices fabricated on a single silicon wafer. Each device is made up of a platinum heater stack, a fluid chamber formed by Ge sacrificial etching, a dry etched nozzle in a silicon nitride membrane, and a fluidic channel formed by deep reactive ion (DRIE process) through-wafer etching. Experimental results with a high resolution video imaging system show that this print head is capable of generating water droplets as small as 1um in diameter (0.5 femtoliter). The printing process is also found to be stable, uniform in droplet size and velocity, and free of satellite droplets at optimum operation condition. At small distances between the print head and substrate, droplet trajectory spreading due to collisions with air molecules is also small. Results of patterning experiments using this printhead will be discussed.

Our second generation printhead is also a large monolithic array, but is based on thin-film sol-gel PZT membrane actuation as opposed to thermal bubble actuation. It is therefore more compatible with a wide variety of ink materials since the ink is not heated. Simulations indicate that our jet design is capable of higher pressure and shorter duration pulses and thus even smaller droplets, potentially approaching 100 nm diameter (0.5 attoliter). Progress toward the realization of this printhead will also be presented.

7637-55, Session 12

Nanomanufacturing: emergent process techniques, tools and applications

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No abstract available

7637-56, Session 12

SLICE image analysis for diblock copolymer characterization and process optimization

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Introduction: Directed self-assembly processes based on block copolymers (BCP) offer great potential to extend conventional optical lithography due to the high throughput, low cost, and possible scalability down to sub-10nm, where the pattern size and shape depend on the properties of the synthesized polymers and templates, rather than on the lithographic tools. Due to the difficulties with long range ordering, BCP self-assembly is best utilized as a lithography sub-division technique which is guided by the topographic or chemical templates pre-patterned by conventional lithographic technologies [1]. In this light, the use of diblock copolymers for patterning 20 nm contact holes for Si CMOS devices have been recently demonstrated [2].

However, as yet no systematic and automated imaging analysis has been established to drive block copolymer research forward into commercialization. Statistical quantification of the quality of self-assembly (on large areas and at the wafer level) in relation to different guiding templates needs to be provided in order to develop device layout design rules for circuit applications. Furthermore, methods and equipment for statistical measurement and analysis as well as characterization of the BCP materials for various patterns should be developed to enable design-for-manufacturing (DFM). Once characterized, many of the essential features necessary for manufacturing integrated circuits can be patterned using BCP directed by pre-patterned guiding templates. The self-assembly behavior can thus be codified into EDA tools, systematically automating how the self-assembly process interacts with the guiding templates. In this respect, an image analysis software would enable circuit designers to focus on design layout without other process concerns to produce the final desired patterns.

SLICE: While directed self-assembly of diblock copolymers is an increasingly developed field in terms of process flow [3-4], the metrology and evaluation is the next crucial step in maximizing its effectiveness for integration into device design based on graphoepitaxy self-assembly trends. We present a novel image processing and data analysis program, SLICE (Sub-Lithography Imaging Computation and Evaluator), which enables a systematic, automated analysis to establish guiding template design rules for high-density MOSFET integration. SLICE has the capability to measure various parameters of directed self-assembly, such as size, shape, center, spacing, and edge distance, to help assess the effect of template properties on the quality of self-assembly. Furthermore, SLICE employs Voronoi diagrams [5] for identifying grains (defect-free regions), grain boundaries (defective regions), and their properties (area, relative orientation, etc.). Key features such as grain detection of ideal regions for contact hole alignment and trench-to-trench comparison of self-assembly quality (see supplemental figures) illustrate the potential impact of SLICE on design rule formulation and process integration.

Conclusion/Future: Knowing the statistical distributions and defect properties of the self-assembly in a given lithographical trench, device fabrication layout trends or standardized rules with respect to trench properties can then be established. In addition, SLICE outputs a data file with summary statistics essential to categorizing the self-assembly, which could be uploaded into a future public domain database as BCP sub-lithography guidelines for device designers in both academia and industry. With graphoepitaxial sub-lithography becoming an increasingly important technique, a unified image processing and analysis software designed for the ordered self-assembly of block copolymers would facilitate and expedite research.

7637-57, Session 12

Monitor and self-diagnostic technology for mask EB writing system

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The accuracy of image placement and line-width on masks become very serious according with reduction of rules in semiconductor device fabrication. The tiny deviations in circumstances during mask-exposure process give large damage to masks and these deviations make costs of masks high. In Association of Super-Advanced Electronics Technologies (ASET), Mask Design, Drawing and Inspection Technology Research Department (Mask D2I) started a 4-year development program* for optimization of mask design, drawing, and inspection to reduce costs in photo-mask manufacturing in 2006.

We are developing the monitor and self-diagnostic technology to monitor the situation of data transfer and check the outer circumstances during exposure to make the reliability of exposure high. The technology makes the efficiency of mask inspection high if the deviation points should be known before the inspection. This monitor and self-diagnostic system consists of three subsystems, the verification of the data processing system, the monitoring system for circumstances, and the integrated diagnostic system. We estimated performance of the monitor and self-diagnostic system in various conditions.

The verification of the data processing system, which is very important to monitor EB exposure system, monitors whether the figure information is correct or not during exposure. In this system, data to be exposed is simulated and compared by software in writing a mask. If there is the difference between exposed data and simulated data, the system informs us the information of the difference visually through the integrated diagnostic system. Time necessary to check exposure data is around 22GB/4hours using two 1.5-GHz CPU's now. Data that are not simulated, blanking signals and outputs of Digital-Analogue Converter (DAC), are monitored with criteria of less than 5nsec and 10-nm deviation by apparatus with self-diagnostic functions. In monitoring system for circumstances, 1-nm deviation in patterns is detected by monitoring of temperature, magnetic field, vibration, sound, and power source. The details will be reported in our presentation.

*This program is supported by NEDO (New Energy and Industrial Technology Development Organization).

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7637-58, Session 12

Lossless compression algorithm for REBL direct-write e-beam lithography system

G. R. Cramer, H. Liu, A. Zakhor, Univ. of California, Berkeley (United States)

Future lithography systems must produce microchips with smaller feature sizes, while maintaining throughputs comparable to those of today's optical lithography systems. This places stringent constraints on the effective data throughput of any maskless lithography system. In recent years, we have developed a datapath architecture for direct-write lithography systems, and have shown that compression plays a key role in reducing throughput requirements of such systems. Our approach integrates a low complexity hardware-based decoder with the writers, in order to decompress a compressed data layer in real time on the fly. In doing so, we have developed a spectrum of lossless compression algorithms for integrated circuit layout data to provide a tradeoff between compression efficiency and hardware complexity, the latest of which is Block Golomb Context Copy Coding (Block GC3). In this paper, we present a modified version of Block GC3 called Block RGC3, specifically tailored to the REBL direct-write E-beam lithography system. Two characteristic features of the REBL system are a rotary stage resulting in arbitrarily-rotated layout imagery, and E-beam corrections prior to writing the data, both of which present significant challenges to lossless compression algorithms. Together, these effects reduce the effectiveness of both the copy and predict compression methods within Block GC3.

Similar to Block GC3, our newly proposed technique, Block RGC3, divides the image into a grid of two-dimensional "blocks" of pixels, each of which copies from a specified location in a history buffer of recently-decoded pixels. However, in Block RGC3 the number of possible copy locations is significantly increased, so as to allow repetition to be discovered along any angle of orientation, rather than strictly horizontal or vertical. Also, by copying smaller groups of pixels at a time, repetition in layout patterns is easier to find and take advantage of. As a side effect, this increases the total number of copy locations to transmit; this is combated with an extra region-growing step, which enforces spatial coherence among neighboring copy locations, thereby improving compression efficiency. We characterize the performance of Block RGC3 in terms of compression efficiency and encoding complexity on a number of rotated Metal 1, Poly, and Via layouts at various angles, and show that Block RGC3 provides higher compression efficiency than existing lossless compression algorithms, including JPEG-LS, ZIP, BZIP2, and Block GC3.

7637-59, Session 12

Considerations for pattern generation in inkjet-printed electronics

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Printed electronics is a promising technique for the realization of a range of low-cost electronic circuits. To make printed electronics viable, it is necessary to develop algorithms and methodologies to describe the formation of patterns during printing. In particular, inkjet printing has received substantial attention as a means of realizing printed electronics due to its versatility and flexibility. Simple static and dynamic fluid relationships prove useful to explain phenomena observed in inkjet-printed electronics and in understanding the limits of such fabrication. For example, inkjet-printed uniform films on a partially wetting substrate have a minimum thickness determined primarily by contact angle and drop volume and a maximum equilibrium thickness set by contact angle (above which viscous spreading and drying must be considered). Jetted drops must overlap in order for a uniform thin film to form, and downscaling of the jetted drop size permits thinner films in a given ink-substrate system. With lower drop spacing, thicker films result until the film height is sufficient that hydrostatic forces exceed the capillary forces and viscous spreading occurs, limited by evaporation-enhanced viscosity. We demonstrate these results with inkjet-printed films of the insulating polymer poly-4-vinylphenol.

For printed circuits, patterned lines are required. We observe several line morphologies by varying drop spacing, temperature and jetting frequency. In order to account for these behaviors, we utilize the principle of surface energy minimization and note experimentally observed contact line pinning. We present a geometric explanation for the transition between several morphologies, considering how a new impinging drop meets the wetted already-printed line. Since viscous fluid spreading energy dissipation is lower on wetted rather than dry substrates, contact line position at this merging event is a primary consideration. Lines printed at small drop spacings show periodic bulging as the equilibrium contact angle of the printed bead is exceeded. Decreasing the jetting frequency or increasing the drop spacing leads to a uniform printed line. As the drop spacing increases to the point where the new impinging drop is larger than the cylindrical bead behind it, a scalloped line edge results. Further increasing drop spacing leads to bead separation, which can be periodic, and eventually to the printing of isolated drops.

Finally, we show layout dependence of the coffee ring effect whereby solute is transferred to the edge of a drying feature due to the geometry of a pinned contact line and enhanced vapor diffusion from the edge of an evaporating feature. We show that, as expected, thicker printed features have less viscous drag and consequently show more mass transfer to the edge during drying, a greater coffee ring. We further demonstrate that evaporating vapor diffusion from one printed line reduces the coffee ring effect seen in nearby lines.

Thus, we are able to accurately describe several important pattern generation effects during the inkjet printing of electronic structures. The concepts of surface energy minimization, contact angle, hydrostatic pressure, and viscous energy dissipation are key to understanding the possibilities of inkjet-printed electronics.

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7638-01, Session 1

3D-AFM enhancement for CD metrology dedicated to lithography sub-28-nm node requirements

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With the continuous shrinkage of feature dimensions on IC in the semiconductor industry, the measurement uncertainty is becoming one of the major components that have to be controlled in order to guarantee sufficient production yield. Already at the R&D level, we have to cope up with the accurate measurements of sub-40nm dense trenches and contact holes coming from 193 immersion lithography or E-Beam lithography. By using top-down CD-SEM it is impossible to extract profile information. Moreover, electron proximity effect leads to non-negligible CD bias in the final measurements. To enable measurement of challenging dimensions with better measurement and reduced measurement uncertainty we have explored and fine tuned an alternative 3D-AFM mode (so-called DT mode) for CD measurements purpose. Theoretically, this mode is supposed to be dedicated only for height measurement but for certain applications it could be extended to reach the nanometer scale accuracy of CD-measurements employing certain optimized scan parameters.

In this paper, we will present and discuss results obtained related to the use this particular mode for CD measurement purpose versus conventional 3D-AFM CD Mode that show important limitations for aggressive trenches measurements. We will also present some results related to the use of very advanced 3D-AFM tips (typically 15 to 20nm diameter) that have been used with the enhanced DT mode parameters. Example of applications will be shown with typical sub-40nm trenches measurements dedicated to advanced lithography process development that will demonstrate that we have succeed to push ahead the limit of the 3D-AFM technology in measuring the tight dimensions that would allow to continue its use for current and upcoming technology nodes.

7638-02, Session 1

Robust characterization of small grating boxes using rotating stage Mueller matrix polarimeter

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Recent studies comparing various metrological characterization methods emphasized the need to improve the total measurement uncertainty and not only measurement precision to satisfy the current requirements of semiconductor technology [1]. Classical ellipsometers have reached a high level of maturity, and provide very precise data over wide spectral ranges from near IR to UV. Nevertheless, these data may not be sufficient to solve the inverse diffraction problem satisfactorily; giving rise to non-negligible offset with respect to the "gold standard" reference values (typically provided now by AFM) of the dimensional parameters [1]. The main issue there is related to the choice of the model used to fit the measured spectra. On the other hand, it was shown recently that the redundancy of the data provided by spectral Mueller matrix polarimetry performed in different conical configurations allows a self-consistent test on the robustness of the model based on the stability of the dimensional parameters when the azimuth is varied [2-4].

In this work we present measurements by the new AutoSE polarimetric tool developed by Horiba Scientific, together with the optical modeling results showing consistency of the obtained parameters within a few nanometers. The samples were silicon etched gratings organized in 250x250 µm boxes with pitches ranging from 140 to 1320 nm, nominal CDs between 50 and 115 nm and nominal thicknesses equal to 100 or 200 nm. All the boxes were characterized by CD-SEM and selected ones also by 3D-AFM for comparison with the polarimetric results. The new polarimeter was operated directly in the clean room to avoid sample contamination, and provided spectrally resolved experimental Mueller matrices in the visible spectral range (450-850 nm), at 70° incidence and arbitrary azimuths via a motorized rotating stage. The projected spot size was 100x100 µm, to keep the illuminated area well within the boxes during sample rotation. Manipulation with the wafer was simplified by a dedicated video camera, which allowed an easy visualization of the beam spot.

The spectra were taken at azimuthal angles between zero and 90° in steps of 5°, and were fitted by using a standard trapezoidal model. Dispersion of the values provides standard deviations within a few nanometers and good correspondence with alternative CD-SEM and 3D-AFM values was established. These results also point out the limits of applicability of the standard trapezoidal model and expected deviations from the accurate values when using only single standard planar diffraction (zero azimuth) configuration.

[1] V. A. Ukraintsev, "A comprehensive test of optical scatterometry readiness for 65-nm technology production," Proc. SPIE 6152, 61521G (2006).

[2] A. De Martino, et al. "Decorrelation of fitting parameters by Mueller polarimetry in conical diffraction," Proc. SPIE 6152, 615253 (2006),

[3] A. De Martino et al. "Comparison of spectroscopic Mueller polarimetry, standard ellipsometry and real space imaging techniques (SEM and 3D-AFM) for dimensional characterization of periodic structures," Proc. SPIE 6922, 69221P (2008)

[4] M. Foldyna et al.,"Accurate dimensional characterization of periodic structures by spectroscopic Mueller polarimetry," Proc SPIE 7140, 71400I (2008).

7638-03, Session 2

CD-SEM focus/dose monitor for product applications

C. N. Archie, E. Solecky, P. Rawat, T. A. Brunner, K. Yoshimoto, IBM Corp. (United States); R. Cornell, Applied Materials (United States); O. Adan, Applied Materials (Israel)

Advanced 193 nm lithographic processes will require defocus control for product wafers in order to meet CD and profile requirements in the future. Dose control is already required. The interaction of product wafer materials with lithography requires additional controls beyond tool monitoring. While scatterometry has demonstrated excellent ability to extract effective defocus and dose information from monitor wafers, the addition of product film stacks introduces several issues for this technique. The additional complexity of model generation and the sensitivity to under-layer thickness and optical property variation are among these. A CDSEM technique for lithography focus monitoring overcomes these issues provided it has sufficient precision and relative accuracy. In this paper, we report on comparative studies of two CDSEM techniques including comparison to scatterometry measurements. One technique uses angled e-beam to better view the sidewall for edgewidth measurement. The tilt angle of the beam is considerably larger than previously explored thereby enabling sensitive measurements on shallower structures. The other technique introduces new target designs particularly suited to CDSEM measurement that have enhanced sensitivity to focus and dose. Implementation of these techniques requires expanded sampling during the course of a single measurement in order to suppress roughness. The small target size of these structures enables applications with targets in product kerf and

embedded within the circuit. In summary, these methods enable the measurement of dose and focus variations on product wafers.

7638-04, Session 2

Improving lithographic performance for 32 nm

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As optical lithography pushes towards the 32nm node and as the k1 factor moves toward 0.25, scanner performance and operational stability are the key enablers to meet device scaling requirements. Achieving these requirements in production requires a stable tool and process performance, in particular with respect to overlay, focus and CDU. Within our paper we will characterize the intrinsic lithographic performance of the scanner and will discuss a new method of machine control to improve the stability and thus the overall performance of the lithographic solution. This is achieved by measuring specific monitor wafers, modeling the results by a new software algorithm and constantly feeding back corrective terms to the scanner. Diffraction-based optical dimensional scatterometry was selected because of its accuracy, its ability to measure overlay and focus simultaneously and its capability to generate greater amounts of measurement data in a shorter time period than other metrology techniques and platforms. Within the metrology part, we will discuss new marker designs, innovative developments on measurement algorithms and its impact on measurement accuracy.

Within the lithographic part, we will discuss the impact of the new control loop on product. We will take a closer look on possible interactions with the existing process control loops and work through the configuration of both, internal and fab control loops. We will show improvements in the focus performance on product wafers by using scatterometry as well. However, most importantly, the newly implemented control loop resulted in a significant improvement of the CD and overlay performance of critical product layers. This had a very positive impact on overall process variation and the rework rate at lithography.

7638-05, Session 2

New exposure tool management technology with quick focus and dose measurement in half-pitch 22-nm generation

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According to the progress of lithography generations and the greater complexity of process, the impact of minor dose or focus errors on yield is becoming more critical. It is required to measure focus and dose with higher accuracy and higher frequency. It is important to get the exposure status in a field or over the wafer accurately and quickly. Current major tools, however, CD-SEM or OCD, have issues, such as low throughput or impact of noise from previous layers. The new method has been required.

In order to provide a solution for above task, we have developed the new technology to measure 2-dimensional pattern variations of entire wafer quickly, and we propose the exposure tool management with the new technology. Using the new technology, we can measure focus variations and dose variations separately, not only on pilot wafer but also on production wafers, with higher accuracy compared with the conventional methods.

With conventional focus monitor methods, focus is measured using dedicated focus monitor patterns. Measurement accuracy is limited, since its line width and illumination condition are different from those of production wafers. In case of dose monitor, CD (Critical Dimension) measurement by CD-SEM is general, but its accuracy is also limited, because not only dose errors but also focus errors make impact on CD.

We have presented the technology to measure pattern profile changes quickly (1). We separated and quantified CD and LER (Line Edge Roughness), but we needed further development, i.e. the new technology in this paper, to achieve the focus and dose monitor tool for production lines.

With the new technology, images of whole wafer are captured with multiple optical conditions including diffraction and polarization, and by analyzing those image signals, we are able to get focus variations and dose variations. Using the technology, we can measure focus and dose variations from exposed patterns. Furthermore we can measure the field inclination and curvature with the technology.

One of the most important features for this kind of technology is the reduction of noise from previous layers. The optical system has been designed for the purpose, so that we can apply the new technology to the production wafers.

The technology is applicable not only to L/S patterns but also to hole patterns. By using the technology, process window monitoring for hot spot management is available with production patterns.

We evaluated the technology on half pitch 4x nm process wafers, and we confirmed the separation of focus and dose, and we also confirmed that there was no impact by noise from previous layers. We are now evaluating the technology on 3x nm wafers, and based on the optical simulations, we believe that the technology is available on 22nm generations also.

K.Fukazawa, Y.Kudo, Y.Fujimori, K.Yoshino,Y.Yamazaki, “2-Dimensiona Dose and Focus Error Measurement Technology for Exposure Tool Management in Half Pitch 3x Generation”, Metrology, Inspection, and Process Control for Microlithography XXIII, Proc. of SPIE Vol. 7272, 72721I, (2009)

7638-06, Session 2

Full wafer macro-CD imaging for excursion control of fast patterning processes

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A powerful new inspection technology enables the excursion control of fast patterning processes. Full images of 300mm wafers are captured and processed to extract CD uniformity information of contact hole and line-space patterns. Using masking filters information from active logic and/or memory areas can be processed and analyzed separately. Characteristic process tool signatures can then be detected based on die, exposure field and wafer pattern variations. Based on inspection times of a few seconds per wafer, rapid monitoring of 100% of processed wafers at full surface is feasible. Use cases for stand-alone, integrated and smart sampling strategies are presented.

7638-07, Session 2

Focus and dose deconvolution technique for improved CD control of immersion clusters

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As CD control requirements increase and process windows decrease, it is now of high importance to be able to determine and separate the source of CD errors in an immersion cluster, in order to correct for them. It has already been reported that the CD error contributors can be attributed to two primary lithographic parameters: effective dose and focus [1]. In this paper, we demonstrate a method to extract effective dose and focus, based on diffracted based optical metrology (scatterometry).

A physical model [2] is used to describe the CD variations of a target with controlled focus and dose offsets. This calibrated model enables the extraction of effective dose and focus fingerprints across wafer and

across scanner exposure field. We will show how to optimize the target design and the process conditions, in order to achieve an accurate and precise de-convolution over a range of focus and dose larger than the expected dose and focus control of the cluster.

This technique is implemented on an ASML XT:1900Gi scanner interfaced with a Sokudo RF3s track. The systematic focus and dose fingerprints obtained by this de-convolution enable identification of the specific contributors among the track, the scanner and the mask. Finally, specific corrections are applied to compensate for these systematic CD variations and a significant improvement of CD uniformity is demonstrated.

[1] C. P. Ausschnitt, S. Y. Cheng, “Modeling for profile-based process-window metrology”, Proc. SPIE 5378-5 (2004)

[2] C. P. Ausschnitt, T. A. Brunner, “Distinguishing dose, focus and blur for lithography characterization and control”, Proc. SPIE 6520 (2007)

7638-08, Session 3

A single metrology tool solution for complete exposure tool setup

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Numerous metrology tools, techniques and methods are used by the industry to setup and qualify exposure tools for production. Traditionally, different metrology techniques and tools have been used to setup dose, focus and overlay optimally and they do so independently. The methods used can be cumbersome, have the potential to interfere with each other and some even require an unacceptable amount of costly exposure tool time for data acquisition.

In this work, we present a method that uses an advanced angle-resolved scatterometry metrology tool that has the capability to measure both CD and overlay. By using a technique to de-convolve dose and focus based on the profile measurement of a well characterized process monitor target, we show that the dose and focus signature of a high NA 193nm immersion scanner can be effectively measured and corrected. A similar approach was also taken to address overlay errors using the diffraction based overlay capability of our metrology tool. We demonstrate the advantage of having a single metrology tool solution, which enables us to reduce dose, focus and overlay signatures to a minimum.

7638-09, Session 3

Improved CD control for 45-40 nm CMOS logic patterning: anticipation for 32-28 nm node

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Since 2008, we have been presenting some papers regarding CMOS 45nm logic gate patterning hunt to reduce CD dispersion. After a global CD budget evaluation at SPIE08 (“Process Control for 45 nm CMOS logic gate patterning “ - B. Le Gratiet et al. SPIE2008; 6922-33) we have been focusing on Intrafield CD corrections using Dose Mapper (“Intrafield Process Control for 45 nm CMOS logic patterning “- B. Le Gratiet SPIE2009 et al.; 7272-107). The story continues and since then we have pursued our intrafield characterisation and focus on ways to get Dose Mapper Dose Recipe created before the first silicon is coming. In fact 40nm technology is already more demanding and we must be ready with integrated solutions for 32/28nm node.

Global CD budget can be divided in Lot to Lot, Wafer to Wafer, Intra wafer and Intra field component. We won’t talk here about run to run solutions which are put in place for Lot to Lot and Wafer to Wafer. We will emphasize on the intrafield / intrawafer process corrections and outline process compensation control and strategy. A lot of papers regarding intrafield CD compensation are available in the litterature but they do not necesserally fit logic manufacturing needs or possibilities. We need to put similar solutions in place which are comprehensive and flexible. How can we correct upfront an Etch chamber CD profile combined with a mask and scanner CD signature? How can we get intrafield map from random logic devices? This is what we will develop in this paper.

7638-10, Session 3

Process variation monitoring (PVM) by wafer inspection tool as a complementary method to CD-SEM for mapping field CDU on advanced production devices

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The PVM method in this work, demonstrated using a DUV laser-based BF wafer inspection tool (Applied Materials UVisionTM 3 Inspection), extends the capability of optically detecting defects, to monitor spatial varying process conditions across wafer surface, such as cross-wafer CD variation and LER issues. In addition, PVM provides a direct method to generate cross-wafer CDU and LER wafer maps and to identify “hot spots” (areas in which the CD’s or LER are significantly different).

The underlying principle of the PVM method is to measure variations in the scattered light from periodic structures, under optimized illumination and collection conditions. Structural changes in the periodic array induce variations in the scattered light. This information is collected and analyzed in real-time and enables highlighting defect density and LER on production wafers. By optimizing the illumination and collection conditions relative to the Exposure axis on an FEM wafer, higher sensitivity to variations can be achieved, and additional information on CD variation and LER of advanced designs are extracted. [Fig. 1] shows a wide dynamic range of GL values (from 204 on left hand side of the wafer to 51 on right hand side of the wafer) as measured on Flash 54nm design rule Gate Etch FEM wafer. The wide range allows the detection of variations across wafer. [Fig. 2] shows the resulting variation within die across the exposure axis. The information is collected during normal production run, and is extracted from a full wafer map. The resulted variation maps can support various application needs, such as:

1. Determine the Mask CDU, that will impact wafer field CDU 2. Expose wafer signatures of process variations across wafer / focus on center or edge fields 3. Reveal Hotspots 4. Supply means to correct scanner dose map across field and wafer

7638-11, Session 3

IntenCD aerial CD uniformity maps for masks with logic designs

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Lithographic process steps used in today’s integrated circuit (IC) production require tight control of critical dimensions (CD). With new design rules dropping below 3x nm and emerging double patterning processes, parameters that were of secondary importance in previous technology generations are consuming an increasing portion of the overall CD budget in the wafer fab. One of these parameters is mask CD uniformity (CDU). Consequently, it has become necessary to monitor and characterize mask related CDU in both the maskshop and the wafer fab.

IntenCD technology, developed by Applied Materials, is implemented on the Aera2 aerial mask inspection tool. It uses aerial imaging inspection data, which contains information about CD variation over the mask, to create a high definition, precise CDU map of the whole mask. IntenCD is now integrated in production of memory products.

Patterns on memory masks are typically made up of dense and repetitive structures covering large areas of the design. Logic designs, however, contain a much larger variety of patterns, shapes and densities. The extension of IntenCD technology to cover logic designs is not straight-forward.

This paper presents the methods and results of a study of implementing IntenCD on logic designs, as part of a joint collaboration between Samsung and Applied Materials.

7638-12, Session 3

Reducing the impact of reticle CD nonuniformity of multiple structures by scanner corrections based on aerial image measurements

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For many critical lithography applications the main contributor to wafer intra-field CD variation is coming from the reticle CD variation. Current practice is that the input data needed to correct the effect of the reticle on the wafer CD is gathered using actual wafer exposures and SEM or scatterometry analysis, a procedure which must be repeated for every single reticle used for a critical layer. This approach consumes valuable scanner time and adds wafer costs. Beyond this, the correction is mainly done for a single feature. In that case, exposure dose can be used as an efficient “knob” to counteract the effect of reticle CD-non uniformities. When looking at multiple and or complex 2D structures, this becomes more complex. First of all, to avoid extensive wafer CD measurements, a fast and accurate measurement technique needs to be available to characterize the relevant structures on the reticle. Second, the correction using only dose becomes less efficient when multiple features through pitch are involved. This especially holds for memory application with dense features in the core and looser periphery features [1]

The application selected for this feasibility demonstration is a 45nm rotated brick wall structure (active area DRAM). A total of 10 line / space structures (both horizontal and vertical) through pitch were selected to represent the periphery. Mask qualification was performed using the newly developed Zeiss WLCD32 metrology tool, which measures wafer level CD on masks using aerial imaging technology. By doing this, WLCD32 captures OPC and optical MEEF effects already on the masks. Furthermore, the WLCD32 offers the capability to measure easily 2D structures and to extract contour plots according to certain thresholds. A correlation analysis has been performed between intra-field wafer data and WLCD32 data. Furthermore, a comparison has been made between the correction potential of ASML DoseMapper recipes based on wafer data and WLCD32 mask data.

Excellent correlation between WLCD32 and wafer data for the brick wall CD of 0.94 was found. The correlation between the two techniques for the brick wall gap is 0.93. Intra-field CDU improvement for the core features is between 47% and 63% for the WLCD32 based correction (percentages are computed for the variance of the CD uniformity data). The maximum difference in resulting core intra-field CDU between the wafer data based approach and WLCD32 based approach is 4%. The intra-field CDU for the peripheral structures was found to deteriorate significantly by the dose correction. Corrected CDU for the peripheral features, however, was still below corrected CDU for the core features.

By using additional scanner knobs, we will demonstrate how to further improve the correction potential for the “loose” periphery structures, without sacrificing on the dense features.

[1] Sung-Woo Lee et al.: Comprehensive Approach to Determining the Specification for

Mask Mean to Target, Proceedings of SPIE Vol. 4889 (2002)

7638-13, Session 3

New measurement technology for CD and pattern profile variation using optical Fourier space

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To monitor the pattern profile variation is becoming new point of view to manage the process as well as measuring CD. Pattern profile changes in case of defocus error of exposure tool. Defocus monitoring in the lithography process is important to fix the process error and to quick feedback to the rework process. LER/LWR (Line Edge Roughness/Line Width Roughness) value suggests the pattern profile variation indirectly, since it comes from the two dimensional information by CD-SEM measurement. The direct monitoring of the profile change is needed for the critical management.

The previous technology presented in SPIE 2008 is useful to measure the CD value of the line and space pattern. It was a way to detect the polarization status change caused by CD change. The technology which we present here is more progressive and innovated method to monitor both CD and the pattern profile change simultaneously.

Using the same optical configuration as the previous; that is the white light illumination, polarizer, high NA objective lens, analyzer configured at the crossed-Nicol condition and the CCD camera located in the Fourier space. Reflective light intensity in the Fourier space includes the information of CD and pattern profile variation, since the reflected light from the line and space pattern is changed its polarization status according to the form birefringence effect. The great motivation is to separate the CD and the profile information in the Fourier space. We achieved successfully to detect CD and profile individually and simultaneously using D-PoP method (Dual Position on Pupil; the pupil is equivalent to the Fourier space)

Two kinds of wafer were prepared for the investigation. Those were exposed at the different condition; one was a Dose changed, the other was a Focus changed wafer. The Dose changed wafer was exposed the different Dose value by shot; therefore it represented the CD changed shot over the wafer. The Focus changed wafer was exposed the different Focus offset value by shot. In general, comparing pattern profile in the defocused wafer to the best-focused wafer, the defocused pattern is rougher wall, bigger wall angle and more rounded cross-section. The Focus changed wafer was represented the reformed profile as previously described. The results of the locational analysis in the Fourier space light intensity for both Dose changed wafer and Focus changed wafer presented that;

1) At the specified location which we called point D the intensity shows good sensitivity for Dose changed (CD change) and no-sensitivity for Focus change (Profile change).

2) At the other specified location the intensity showed less sensitivity for CD change, it showed Focus change sensitivity. We called point F there.

See attached figure showing the intensity (gray level of CCD camera) map of two kinds of wafer at both point D (Above) and F (Below), there were some Dose/Focus changed shots and other normal shots.

We will also present the simulation results about the detection sensitivity for CD/Profile and the locational dependency in the Fourier space.

The great advantage of our unique optics is that the Fourier space information includes many kinds of optical condition for the form birefringence; incident angle, incident plane orientation for line and space pattern and incident light polarization status S, P or mixed S/P. Those optical conditions depend on location in the Fourier space. Also white light illumination can enlarge the option for optimum detection of the CD/Profile. Therefore our unique technology suggests wider application for the lithography process and the further generation.

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7638-14, Session 3

Application of automated topography focus corrections for volume manufacturing

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Focus and overlay control of lithography tools for leading edge semiconductor manufacturing are critical to obtaining acceptable process yields and device performance. The need for these controls is increasing due to the apparent limitation of optical water immersion lithography at numerical aperture (NA) values of approximately 1.35 and the need to use the same equipment for 45nm, 32nm, and 22nm node production.

In particular, as the theoretical depth-of-focus (DOF) shrinks with reduced image size at a fixed maximum NA, compensation for the impact of topography and related induced focus errors becomes more critical. As has already been described in the literature, for modern semiconductor lithography equipment, product topography can induce two types of focus errors. Firstly, the topography itself may vary in such a way - frequency or amplitude - that modern exposure equipment cannot compensate during exposure. Secondly, the film stacks, patterns, and topography of semiconductor wafers can induce erroneous focus metrology for some types of optical focusing sub-systems. As previously described in the literature, ASML has developed an air gage sub-system which allows users of ASML lithography equipment to determine and apply actual surface-to-optical-leveling focus corrections during product exposure.

This work describes the implementation and performance of these focus corrections for volume production in IBM's 300mm facility. Of particular note, what has been implemented includes a logic hierarchy that manages the air gage sub-system corrections to optimize tool productivity while sampling frequently enough to verify process stability.

The information to be reviewed includes: general implementation approach; Outline of the IBM Advanced Process Control (APC) logic and system(s) that manage the focus correction sets; sample focus correction contours for critical 45nm, 32nm, and 22nm applications; long term, historical focus correction data for stable 45nm processes as well as development 32nm and 22nm processes; and practical issues encountered and possible extensions to the methodology.

7638-15, Session 3

Aerial mask inspection placement maps feed forward to scanner for double patterning

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Overlay increasingly becomes one of the biggest double patterning process challenges for the 2x node and below. The latest immersion scanner generation overlay specifications becomes increasingly stringent according to ITRS requirements [1]. Intrafield residuals placement errors, which cannot be so easily measured on product wafers due to limited number of overlay targets and metrology requirements, are part of the intrafield overlay challenge. Double patterning process involving two critical lithography steps as litho-etc-litho-etch (LELE) could benefit from residual overlay errors correction.

Low, intermediate and high order distortions originating from the mask and pellicle imperfections have been shown in recent publications to consume up to several nanometers from the global overlay budget. These types of errors originate from local or global surface variations and cause uneven dislocation distributions of critical features across the mask Therefore high precision placement measurements of critical features across the mask would be required for overlay correction process control.

Applied Materials Aera2TM, aerial imaging mask inspection tool is capable of generating such high precision placement maps. Using a feed forward mechanism to an APC system such as ASML GridMapper Intrafield, it will help to reduce the overall overlay errors of the double patterning process originated in masks sets and help to meet the tight budget requirements. This paper will present the placement measurements challenges and recent results of high precision placement maps, leading to improvement in overlay performance.

7638-16, Session 4

Defect metrology challenges at the 11-nm node and beyond

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Rapid, inline inspection of wafers and reticles for minimum pitch defects is expected to be a significant technical challenge at the 11nm node. With the possible future adoption of EUV lithography, increasingly exotic materials and complex device architectures, projecting end user requirements at the level required to make inspection tool architectural decisions is a difficult feat 4 to 5 years out. Critical area modeling and lithography simulations along with the development of canonical defect sets are important tools in arriving at these requirement projections.

Four high level tool architecture paths are available to meet these requirements:

1. Current wavelength and imaging modalities
2. Super-resolution techniques
3. Scaled inspection wavelength
4. Disruptive technologies

Retaining current platforms with existing wavelengths and imaging modalities implies pushing defect detection down to the lambda / 10 to lamda / 20 regime where both heuristic and rigorous modeling predict steep signal drop offs. Success at "low k1" metrology is projected to require the development of innovative super-resolution techniques.

A variety of super-resolution techniques can be applied both to existing and scaled wavelengths, particularly those that have seen success overcoming DUV contrast loss in biological microscopy, but there are no data from modern design rule VLSI wafers to support the applicability of many of these techniques. Additionally, many of these techniques have very aggressive system engineering requirements.

Solely shrinking inspection wavelength demonstrates limited defect sensitivity improvement. Imaging innovations will be needed to support this path.

The main disruptive technology under consideration in the industry is electron beam inspection. Current systems are projected to fall several orders of magnitude short of the inspection tool throughput requirements. Multiplexing and/or defect-to-pixel ratio improvements will be necessary to make EBI a successful alternative to optical inspection for physical defects.

The present work progresses through these argument and conclusions, including supporting FDTD simulations on full device stacks to model out signal scaling by technology node at fixed wavelength and the impact of wavelength scaling on 11nm devices. The main conclusion is that the industry needs to support three broad pathfinding projects:

1. Evaluation and development of super-resolution imaging techniques at current and scaled wavelengths, including the development of system engineering components to support tight DOF inspection.
2. Development of effective wavelength scaling approaches.
3. Development of highly multiplexed ebeam inspection tools with defect-to-pixel ratios < 1.

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7638-17, Session 4

Systematic and random defects control with design-based metrology

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As technology node of memory devices is approaching around 30nm, the process window is becoming much narrower and production yield is getting more susceptible to small defects which used to be not, if ever, so critical. So it would be very hard to expect the same production yield as now in near future.

It is possible to classify wafer defects into systematic and random defects. Systematic defects can be also divided into design related and process related defects. Narrow process window, generally, is thought to be the source of these systematic defects and we have to extend process window with Design for Manufacturing (DFM) and control process variation with Advanced Process Control (APC) to ensure the production yield.

The sensitivity of random defects, however, has something to do with the smaller design rule itself. For example, the narrower spaces between lines are subject to bridge defects and the smaller lines, to pinch defects.

Die to data base (DB) Design Based Metrology (DBM) has mainly been in use for detecting systematic defects and feedback to DFM and APC so far. We are trying to extend the application of DBM to random defects control. The conventional defect inspection systems are reaching its highest limit due to the low signal to noise ratio for extremely small feature sizes of below 40nm. It is found that Die to DB metrology tool is capable of detecting small but critical defects with reliability. Fig. 1 is an example of random defects which conventional defect inspection tool failed to detect but were found by Die to DB metrology.

In this paper, we explore the possibility of controlling random defects as well as systematic defects with Die to DB metrology and the results are presented in detail.

7638-18, Session 4

The limits and extensibility of optical patterned defect inspection

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Recently, there has been significant interest and research in evaluating the limitations and extensibility of optical technologies for patterned defect inspection. There are currently major challenges identified in patterned defect inspection beyond the 32 nm node and no known solutions have been identified to meet defect inspection requirements for the 16 nm generation. In this paper we will present a comprehensive evaluation of bright field and more advanced optical scatterfield techniques for defect inspection using both simulation tools and experimental methods.

This paper will focus on quantitative evaluation of optical inspection methods for a variety of defect types and process levels. Bright field and dark field optical inspection methods and recent developments in scatterfield microscopy, a technique which combines well defined angular resolved illumination with image forming optics have been investigated using simulation and experimental methods.

A three-dimensional finite difference time domain (FDTD) model was used to simulate an array of defect types using intentional defect array (IDA) wafers designed and fabricated by International SEMATECH. We have quantitatively evaluated the angle-resolved Scatterfield imaging technique and compared the results to conventional on-axis illumination techniques. Direct modeling results and sensitivity analysis for the zero-order imaging technique of dense target features is applied to image-based defect analysis on 32 nm poly and/or metal-1 stacks.

We will present evaluations of multiple fixed-angle illumination configurations to determine performance gains obtained by using combined, specific spatial frequency illumination components defined by dipole, quadrapole, or more complex illumination, based on simulation results. We have quantitatively evaluated bright field and angle-resolved Scatterfield imaging techniques as a function of wavelength. We will compare results obtained at different wavelengths, polarization states, and then quantify performance gains for poly gate and metal 1 process stacks. This will have, as an output, direct modeling results and sensitivity analysis for dense feature zero-order imaging techniques as a function of illumination wavelength, angle, and polarization state on 32 nm poly and metal-1 stacks.

We will present experimental data with analysis using angle-resolved imaging from a scatterfield optical tool at 450 nm wavelength. The main intent is to use a laboratory metrology tool to verify and validate the simulation results using the IDA wafers. This involves data acquisition in the zero-order imaging mode and all required aspects of wafer positioning, target recognition and data preparation and subsequent analysis.

We have also designed, constructed, and characterized a flexible 193 nm optical microscope capable of operation in scatterfield and bright field imaging modes. We will present data analysis and acquisition using angle-resolved 193 nm zero-order imaging approach. We have recently implemented polarization control for defect inspection at 193 nm. This involves data acquisition in the zero-order imaging mode on the 193 nm tool using angle and polarization control at the conjugate back focal plane. Simulation results with realistic sample and tool noise will be used to compare and contrast different combinations of optical techniques to evaluate the fundamental resolution limits of enhanced optical techniques.

7638-19, Session 4

Advance lithography: wafer defect scattering analysis at DUV

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Considerable effort is directed towards the development of next-generation lithography processes, addressing the need for transistor densification to meet Moore's Law. The aggressive design rule shrinkage requires very tight process windows and induces various types of pattern failure with lithography process variations. As lithography process is critical in the wafer fabrication process, the requirements for high sensitivity defect detection in the lithography process becomes tighter as design rules shrink. Analysis of the root cause of the defects and their interaction with various light sources and optics systems configurations for optical wafer inspection is essential for understanding the detection limits and requirements from advanced tools targeting future lithography inspection applications.

In this work, we present an analysis of wafer defects light scattering and detection for a variety of 3xnm design rule lithography structures with various polarizations and optics configurations, at the visible and at DUV wavelengths. The analysis indicates on the defect scattering and inspection performance trends for a variety of lithography structures and defect types, and shows that control of the polarization of the optical inspection tool is critical for enhanced scattering and detection sensitivity. The analysis is performed also for the 2xnm and 1xnm design rules showing the advantages of polarized DUV illumination over unpolarized and VIS illumination.

7638-20, Session 4

Studies of photoresist defectivity and effect of defect inspections on critical dimension of an advanced memory device

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Electron beam (e-beam) defect inspection system has been widely used in integrated circuit (IC) chip manufacturing for the advanced nano technology node. Because its higher resolution, it also provide an alternate solution for tiny physical defects that are beyond capability of optical defect inspection system.

ADI is very important in photolithography process because it allows engineers to catch DOI earlier so that wafer can be reworked to remove photoresist (PR) and redo the RP patterning. While device dimension shrinking, optical inspection system may start missing some killer defects, which are too small and beyond its resolution capability. In this case EBI could step in and play an important complementary role.

In this study, a 3x-nm after development inspection (ADI) wafer with focus exposure matrix (FEM) was inspected with both an advanced optical system and an advanced EBI system, and the inspection results were carefully examined. We found that EBI can capture much more defects than optical system and it also can provide more information about within reticle shot defect distribution. It has high capture rate of certain critical defects that are insensitive to optical system, such as nano-bridges. We also studied the variations of critical dimension (CD) caused by difference defect inspection methods, e-beam inspection and optical inspection.

7638-21, Session 4

Defectivity decrease in the photolitography process by AMC level reduction through implementation of novel filtration and monitoring solutions

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As a consequence of device reduction, Airborne Molecular Contamination (AMC) has become a key detractor of yield. This is particularly true in photolithography area where a large panel of species can impact the process:

- Ammonia deteriorates Critical Dimension (CD) by T-toping effect.

- Refractive Organic Compounds contaminate optics.

- Acids react with ammonia to create a salt deposit on lenses or reticles. This is especially true for 193nm tools where the reaction is catalyzed.

- Acids also increase defectivity by creation of satellite spots, especially on tools using base amplified resists.

Source identification and control, based on analytical methods, combined with air filtration is the appropriate corrective solution for process stabilization. This filtration can be deployed on tools or fab level, depending on the type, level and origin of contamination.

We have found that ammonia filters mounted on tracks to prevent any CD drift can have undesirable reactions with solvent used in photolithography area (here PGMEA) to create a by product, acetic acid, that is released in clean room air. It is mandatory to prevent the reaction with PGMEA to increase tool filters lifetime, reduce wafer defectivity and prevent lenses for salt deposition.

The solution chosen was an integrated, analytically supported approach which involved source reduction and the application of selective AMC filtration on tools and clean room level. For tracks, standard filtration products have been replaced with a filter type made of novel filter foam materials that prevent the unwanted reaction. In order to increase lifetime of these tool filters, the decrease of PGMEA level in clean room was a key issue. It was achieved after a model description of the photolithography zone both by source control and installation of VOC filters on the recirculation air treatment. These AMC filters for air treatment could have been installed at different places: we will show how an optimized cost solution was chosen for facilities filters with very good associated results.

The resulting reduction of the PGMEA concentration at fab basement compared to the baseline before installation of the cited VOC filters on intake position of the fan tower will be illustrated by results obtained with a real time continuous AMC monitor. This monitor is based on Proton Transfer Reaction - Mass Spectrometer (PTR-MS). It analyses VOC chemically ionized by a source of H3O+ ions which gives high ion counts even at low analyt concentration. We will show that the PTR-MS monitor is able to render AMC-filter removal efficiencies, monitor global level of solvent as PGMEA at any point of the clean room or detect leakage of solvent from tools. It is thus the key point to source control.

The drastic improvement of wafer defectivity on i-line tools due to acid acetic reduction will be outlined. The similar positive effect is observed on deep UV tools where satellite spot defects are reduced as a result of the actions. Finally, the mechanism of creation of these defects will be discussed based on results from TOF-SIMS analysis.

7638-22, Session 5

Statistically accurate analysis of line-width roughness based on discrete power spectrum

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Present and future large-scale-integrations (LSIs) are facing a challenge of variation in device characteristics. Line width roughness (LWR) of gate electrodes of metal-oxide-semiconductor (MOS) transistors is one of the factors that cause the variation. To characterize and control LWR, we need to extract the correlation length of LWR as well as its variance or standard deviation. Previous studies investigated the correlation length mostly by analyzing the power spectral density (PSD) of LWR. However, the conventional results fall short of the required accuracy due to the following reasons. Firstly, the conventional experimental PSDs were too jagged for accurate analysis. Secondly, the theoretical PSDs of continuous cases were used in fitting the experimental PSDs even though the latter were intrinsically discrete. To solve the problems, we based this study on the original physical definition of PSDs of stochastic processes and proposed to average experimental PSDs of many samples that were prepared under the same condition. In addition, for the purpose of use in fitting, we developed analytic formulas of discrete PSDs under the assumption that the autocorrelation function exponentially decays with distance, or equivalently the spectral line shape is Lorentzian. To confirm the validity of the formulas, we created LWR data with given correlation lengths by using Monte-Carlo (MC) method. As expected, the PSDs by the MC method completely agreed with those by the analytical calculation. By using the MC data, we also confirmed that the jaggy of the PSDs decreases approximately in inverse proportion to the square root of the number of averaged PSDs. The experimental PSDs of photoresist LWR that were obtained by averaging the results of 400 samples were almost free of jaggy and excellently fitted by the PSDs that were calculated by using the above-mentioned formulas. The result shows that the photoresist LWR of this study has an autocorrelation function of exponential decay. The best fit was achieved when we assumed a standard deviation of 2.5 nm and a correlation length of 35 nm. The standard deviation of this study was the same for different intensities of scanning-electron-microscope (SEM) image noise, so-called “bias-free”, because the two PSD components, LWR and SEM-image noise, were independently determined. Nonetheless, it is still important to reduce the noise component in order to confirm that the PSDs have the Lorentz line-shape, a prerequisite of this study. To reduce the noise effect, we averaged the SEM images perpendicularly to fine lines before edge detections. The variance produced by the noise decreased with the number of averaged pixels, but their relationship was exponential-like rather than the usual inverse proportion. As

theoretically expected, the procedure did not reduce the variance unlike averaging along the lines. The correlation length and average line width (critical dimension) also remained constant for different numbers of averaged pixels. All these results are clear supports for the accuracy of the method of this study. Accordingly, the method of this study forms the basis for developing technologies to reduce LWR of fine patterns and device variation caused by LWR.

7638-23, Session 5

Measurements and sensitivities of LWR in spacers

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LER and LWR have long been considered a main issue in process development, with more and more layers monitored each technology node. With every such technological advance, more aspects of the device were found to be sensitive to roughness, starting with transistor performance and leakage when considering LER in the gate and active area, and going to resistance and reliability in back-end layers. However, consideration of the spacers has always been less intense, due to lack both in measurement capabilities and in consideration of importance.

Following research done on sources of leakage, we found Ioff in some processes to be highly sensitive to changes in the width of the spacers - even more strongly so than to the actual gate CDs. A very logical conclusion would be consideration of its sensitivity to LWR in the spacers as well, which led us to begin exploring the possibility to measure spacer LWR, its correlation to the LWR in the poly, and its sensitivity to changes in layout and OPC. Our study refers to the work we presented last year, in which we defined the terms LLER and LLWR - the local roughness that was presented then for the poly, and is measured as the 3-sigma value of the line edge/width in a 10-nm segment around the measurement point.

A dedicated test chip was designed, for the experiments having various transistors layout configurations with different densities to cover the all range of process design rules. AMAT LER and LWR innovative algorithms were used to measure and characterize the spacer roughness relative to the distance from the active edges and from other spacers.

In this paper we present the characterization of poly spacer LLWR and LLER compared to that of the poly gate in various transistor shapes, showing that the relation between them depends on the layout of the transistor (final layout, including OPC). We will show how the spacer deposition may reduce, keep or even enlarge the roughness seen in the poly, depending on the layout of the transistor, but surprisingly not dependent on proximity effects

7638-24, Session 5

LER/LWR detection using dark-field spectroscopic methods

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Line Edge Roughness (LER) and Line Width Roughness (LWR) are becoming increasingly important as lithography drives for lower CD values. Detection of LER/LWR during the production process is therefore a potentially required tool for in-line process monitoring in future fabs. Currently the existing methods for LER/LWR monitoring and measurement are the SEM and AFM techniques which suffer from either damage to the layers or a very slow throughput. An optical technique for the monitoring of LER/LWR is therefore of interest as it avoids the problems of other techniques.

In this work we explore different directions for the detection of LER/LWR on line arrays using Dark Field (DF) optical methods. In these methods the detected signal is a result of scattering due to the non-regular aspects of the structure while avoiding the regularly-diffracting parts of the signal. The benefit of using dark field optics is clearly that the whole of the signal is fully attributable to the random properties of the structure. This is in contrast to recently published works in which LER/LWR was detected by optical techniques in which a significant signal exists also in the absence of LER/LWR, hence the measurement of LER/LWR has to rely on differentiating an experimental signal, which is in general less robust. To validate the possibility of detecting non-uniformity using dark field techniques we have carried out a simplified simulation which clearly shows the correlation between the signal between (i.e. outside) diffraction orders and LER/LWR.

By exploring experimentally all possible combinations of mounting (conventional/conical), polarization (TE/TM/45) and analysis (parallel/crossed) we find that in best conditions LER/LWR lower than 4nm can be clearly identified (as verified by SEM measurements) with the actual detection limit being probably closer to 1nm. This result was verified on structures with both intentional and un-intentional roughness. Exploring the intensity of the scattered signal on Focus/Exposure conditions we find intensity increase at the edge of the FEM matrix, as expected from SEM measurements. We further find an interesting dependence of the scattered signal on the period of the lines, showing a reduced signal intensity and a red-shift as period is increased, as could be expected. We therefore conclude that we have sufficient evidence to support the potential of Dark Field measurements for the monitoring of LER/LWR.

7638-25, Session 5

CD-SEM metrology of spike detection on sub-40-nm contact holes

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The effect of pattern edge roughness on the performance of LSI devices is becoming an increasingly serious problem as these devices are scale downed. Consequently, line-edge roughness (LER) in gate pattern has been studied extensively [1, 2]. Comparably, there has been less focus on the study of contact hole edge roughness (CER) [3] and its electrical impact on LSI. However, as hole-radius becomes 20 nm or less, CER of several nanometers is no longer negligible.

In the light of above-described circumstances, it is necessary to establish a meaningful CER measurement method based on its electrical impacts. The most serious problem caused by CER is acceleration of dielectric breakdown by electric field concentration at the tip of sharp spikes protruding outside of the hole [3, 4]. However, conventional roughness metrics were not directly correlated to the sharpness. In this study, we propose new CER metrics which represent the sharpness of the spikes on the hole-edge, and show examples of their practical use.

A new CER metric, spike sharpness (SS), is proposed and calculated as follows. First, edge points of a hole are extracted from a CD-SEM image. Second, the positions of the extracted points are approximated with a perfect circle. Third, distances of each edge point from the perfect circle, are calculated. Fourth, well-known CER metric, 3sigma, the maximum value of the distances, and the autocorrelation length of the series of the distances are calculated. The new metric SS is defined as the ratio of the maximum distance or 3sigma to the autocorrelation length. Since the maximum distance and 3sigma represent amplitude of the spike in the hole and the autocorrelation length represents the width, SS directly represents the sharpness of the spike [4].

We applied the above metric to examine its sensitivity to the lithographic condition variation. Three wafers with 40 nm diameter holes of photo resist were observed by CD-SEM (Hitachi High-Technologies, CG4000). The wafers were fabricated with slightly different lithographic conditions. The critical spike was defined as the hole whose SS was 0.5 or more. The number of the critical spike holes was counted out of 250 holes for each wafer. Although it is difficult

to distinguish the lithographic conditions of the three wafers using conventional CER 3sigma, we can clearly distinguish the three wafers and find the lithographic condition that has smallest spike probability using critical spike count. We also evaluated ellipse hole using this method with the deviation of the edge points from the perfect ellipse. This proposed method will be helpful to detect failures to improve yield in contact-hole process and in the mass-production line for future scale downed devices.

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7638-26, Session 5

Model-based analysis of SEM images to automatically extract linewidth, edge roughness, and wall angle

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Accurate measurement of critical dimensions (CD) in scanning electron microscope (SEM) is one of the most important tasks in metrology. Methods of extracting this information based purely on analysis of images could be far from the actual CD values. Indeed, extracting the brightest spot or the largest derivative at the edge of a line are often used, which do not represent the edge of a line, neither at the top nor bottom. Furthermore, the measurement error depends on many factors such as materials, beam size, and accelerating voltage. So, the CD values calibrated for a specific pattern or SEM setup cannot be applied to the analysis of other patterns or images received in slightly different conditions of observation.

The myCD software was developed to analyze an SEM image and extract the information regarding linewidth, line edge roughness, line width roughness, and wall angle of features. The analysis is based on an understanding of physical principles involved in the formation of the SEM signal. Some parameters such as beam voltage and materials should be known to the operator as the input data along with SEM image.

Extensive simulations using CHARIOT Monte Carlo software [1] helped us to understand the signal formation and relationship at a variety of parameters involved with the formation of SEM image: beam voltage, materials, wall angle, distance to the neighboring feature, layer thickness, detectors, etc.

The output of the software is linewidth at the top, bottom, and in the middle of the line, line edge roughnessess at each edge, line width roughness, and wall angles at each edge. In addition, averaged values over all lines present in the image are also displayed.

1. S. Babin, S. Borisov, A. Ivanchikov, I. Ruzavin, J. Vac. Sci. Technol., B6 (2006) 3122

7638-27, Session 6

Estimating proximity associated errors in contour metrology

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In contour metrology the critical dimension scanning electron microscope (CD-SEM) assigns a continuous boundary to extended features in an image. The boundary is typically assigned as a simple function of the signal intensity, for example by a brightness threshold or gradient. However, the neighborhood of different points along the feature boundary may vary considerably. Some parts of the boundary may have close neighboring features while others are relatively isolated. At some places a boundary may need to be followed around an outside corner, in others around an inside corner. Neighboring features can obstruct the escape of secondary electrons; varying proximity of neighbors therefore represents an influence on detected intensity, one that can be incorrectly interpreted as a contour shift when the contour passes, for example, from an isolated neighborhood to a dense one. The magnitude of this offset variation has been estimated using images produced by JMONSEL, a Monte Carlo simulator of SEM secondary electron imaging, from simple model test patterns with varying neighborhoods. Shifts of approximately 1 nm per edge (2 nm width change) are indicated for isolated vs. 30 nm separated 60 nm tall lines. The magnitude of the shift varies with beam size, wall angle, and edge assignment algorithm.

7638-28, Session 6

Monitoring and characterization of metal-over-contact based on edge-contour-extraction measurement followed by electrical simulation

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The aggressive design rules of deep sub-micron technology's using Cu metal over W-plugs, makes process monitoring and characterization into a real challenge. Not enough coverage of the metal above Contact (Figure-1) may cause yield degradation due to un-predicted contact resistance. Due to proximity effects and OPC restrictions, different layout configuration of metal-over-contact may results in different contact coverage by the metal. From metrology point-of-view, the ability to control process latitude of two constituent layers in the semiconductor process is critical. The fundamental way to develop and control Metal over Contact process with a CD-SEM is to measure the contact plugs through the metal trenches. This approach proposes a significant metrological challenge. There is no edge topography, only material contrast, and only part of the Contact can be seen. Hence, innovative algorithms and image processing techniques are required to accurately measure the metal-over-contact area coverage.

The aim of this paper is to demonstrate a reliable characterization and monitoring method. A dedicated test chip was designed for this purpose, having hundredth of different layout configurations, in one nanometer variation. The methodology flow consists of using systematic Edge-Contour-Extraction (ECE). The physical parameters extracted from the ECE measurements analysis and used for several purposes: (i) identification of design-rule verification, (ii) contact resistance calculation based on the metal-over-contact coverage area, (iii) reliable feedback for OPC correction efficiency.

PRELIMINARY SUMMARY OF DATA

In Figure 1 the contact is properly centered relative to the metal trench, but may be partially opened under the trance.

Figure-1: Metal trench over contact test structure, combine various designs of metal trances with overlay variations.

In Figure 2, the trench is not properly overlapped with the contact at the line-end, it may yield relatively small area connection between the contact the Metal 1ine on top of it. Therefore, it may impact contact resistance. The OPC Model can not provide any correction to the line, due to other lines drown around it.

Figure 2 CD-SEM image of a “hot-spot”, contact that is not overlapped with the Metal line (Picture is taking after Metal trench etch, and before Cu plating). The contact coverage by Metal is ~80%, only.

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7638-29, Session 6

Electrical validation of through process OPC verification limits

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Electrical validation of through process OPC verification limits in 32nm process technology is presented in this paper. Correlation plots comparing electrical and optical simulations are generated by weighting the probability of occurrence of each process conditions. The design of electrical layouts is extended to sub ground rules to force failure and derive better correlation between electrical and simulated outputs. Some of these sub ground rule designs amplify the failures induced by exposure tool, such as optical aberrations. Observations in this regard will be reported in the paper. Further, electrical data is collected from a wafer with programmed process offsets, distributed on the wafer to cover the inter field behavior of some of the downstream processes after lithography. Sensitivity with respect to dimensions, orientations and wafer distribution will be discussed in detail.

7638-30, Session 6

Computational inspection and its applications on a mask inspection system with both high-resolution and aerial image mode

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At the most advanced technology nodes, such as 32nm and 22nm, aggressive OPC and Sub-Resolution Assist Features (SRAFs) are required. However, their use results in significantly increased mask complexity, making mask defect disposition more challenging than ever. In an attempt to mitigate such difficulties, hardware emulation and software simulation to obtain aerial images at the wafer plane are coming into common use. In the software approach, an accurate lithography simulation from a high-resolution mask inspection image is required; however, due to limited resolution and the difference in wavelength between the mask inspection system and wafer scanner, many small mask defects are blurred, or even disappear. Therefore, recovering the real mask pattern from the mask inspection image is critical for any simulation-based aerial/wafer image level mask defect disposition to work. Furthermore, , a simple defect filtering based on intensity difference is no longer adequate for aerial/wafer image level mask defect disposition; a fast and accurate automated disposition is needed, just as in OPC verification.

To address these challenges in mask inspection and defect disposition, new mask inspection technologies have been developed that not only provide high resolution mask images made using the same wavelength as the scanner, but that also provide aerial images both by using software simulation and hardware emulation. The original mask patterns stored by the optics of mask inspection systems can be recovered using a patented algorithm based on the Level Set Method. More accurate lithography simulation models can be used to further evaluate the defect on simulated resist patterns. An automated defect classification based on lithography significance and local CD changes is also developed to disposition tens of thousands of potential defects in minutes, so that inspection throughput is not impacted.

Results on both programmed defects and production defects are presented which demonstrate the accuracy and speed of this aerial/wafer image based mask automatic disposition. Mask and wafer images are compared with the inspection results, and then aligned with the printline of an AIMS tool.

7638-31, Session 7

Hybrid reference metrology exploiting patterning simulation

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Workhorse metrology such as CD-SEM is used during process development, process monitoring, optical proximity correction (OPC) model generation and verification. Such metrology needs to be calibrated to handle various types of profiles encountered during IC fabrication.

Reference metrology is used for calibration of workhorse metrology. When possible the preferred reference metrology technique at IBM is CD-AFM to calibrate CD-SEM and scatterometry. There is an astounding need for sub half and sub quarter nanometer measurement uncertainty in near future technology nodes as envisaged in the International Technology Roadmap for Semiconductors (ITRS 2007).

In this regime of desired measurement uncertainty all metrology techniques are deemed limited and hybrid metrology appear promising to offer a solution (Rick Silver SPIE 09). Hybrid metrology is the use of multiple metrology techniques, each with particular strengths, to reduce the overall measurement uncertainty.

CD-AFM makes use of a flared probe in order to scan the sidewalls and bottom of the pattern on a wafer to provide 3D profile and CD measurements at desired location on the profile. As the CD shrinks with technology nodes especially the space, the size of the AFM probe also needs to shrink while maintaining the flared geometry specifications. Unfortunately the fabrication of such probes is a challenge and new techniques are required to extend reference metrology to the smallest space and hole of interest.

This paper proposes a reference system combining CD-AFM and patterning simulation. This hybrid metrology system enables CD metrology in a space not measurable directly by conventional CD-AFM probe. The key idea is to use the successfully measured profile and CD information from the CD-AFM to calibrate or train the patterning simulation optical and resist model. Ability of this model to predict profile and CD measurement is verified on a physically measured dataset including cross sections and additional CD-AFM measurements. It is hypothesized that this model will be able to predict profile and CD measurements in otherwise immeasurable geometries. Being based on optics and materials fundamentals, this approach is presumed to be more accurate compared to mere extrapolation approach in use today.

We report on the measurement uncertainty improvement with this approach. Situations with highest prediction confidence involve CD-AFM scanning resulting in partial information. For example, using carbon nanotube probes or CDP where there is little flaring of the tip, the CD-AFM cannot detect significant undercutting of the structure. Achieving agreement with the calibrated patterning model for measurement metrics such as height, top and middle CD permits the prediction of the bottom CD to be used as an authentic reference measurement.

7638-32, Session 7

Scatterometry metrology validation with respect to process control

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The scatterometry or OCD (Optical CD) metrology technique has in recent years moved from being a general purpose CD metrology technique to one that addresses the metrology needs of process monitoring and control, where its strengths can be fully utilized. With the significant advancements that have been made in both hardware and software design, the setup time required to build complex models and solutions has been significantly reduced. This has allowed scatterometry metrology to be extended beyond measurement of simple gratings on film stacks to measuring extremely complex structures and stacks such as metal gates and FinFets. Whilst the application of scatterometry to process control has clearly shown its merits, the question still arises as to how accurately the process corrections to feed forward or feed back for process control can be extracted, and how the complexity of the stack affects this ability?

In this work we critically examine the accuracy of scatterometry with respect to process control by comparing three hardware platforms, on both a simple litho stack and a complex FinFet stack. The impact of hardware design is discussed as well as the 'setup' of the modeled parameters on the final measurement result. It will be shown that corrections extracted based on scatterometry measurements must be true to process variation and independent of the hardware design. Our results will show that the ability to use scatterometry effectively for

process control ultimately lies in the ability to accurately determine the changes that have occurred in the process and to be able to extract appropriate process corrections for feedback or feed forward control; allowing these changes to be accurately corrected. To do this the metrology validation extends beyond the typical metrology metrics such as precision and TMU; metrology validation with respect to process control must encompass accurate determination of process corrections to ensure a process tool and/or process stays at the set point.

7638-33, Session 7

Smaller, smarter, faster, and more accurate: the new overlay metrology

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With the introduction of double patterning, overlay capability below 5nm is required for optical lithography density scaling to the 22nm node and beyond. Commensurate overlay metrology must enable dense sampling of all patterned area to control single-nanometer systematic sources of error among an increasing number of device layers. This translates to the need for sub-second measurement of microscopic targets representing multiple layers within a metrology tool field of view, all while improving accuracy.

Blossom (BLO) is the overlay metrology of record for the IBM 32nm technology. As we will describe here, the densely packed array of layers represented in a single BLO target has enabled us to conduct within-field in-line sampling on our most critical layers. We will also report the significant improvements to metrology performance that have resulted from our migration of BLO technology to a new measurement platform.

As 22nm development proceeds, we are shrinking our overlay targets further. Figure 1 shows the image of a target suitable for within-chip insertion: a 10um square micro-Blossom (uBLO) accommodating 8 layers. Correlation of uBLO to BLO measurements on a layer pair is shown in Figure 2; despite an approximately 10X area shrink relative to BLO, the BLO measurement uncertainty remains comfortably below 0.5nm.

Our paper presents details of our target layout, measurement, and analysis approach. In addition, we detail data representative of overlay variation in state-of-the-art lithographic processes, along with our outlook for overlay metrology implementation for future technologies.

7638-48, Poster Session

3D-AFM tip to tip variations and impact on measurement performances

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The CD metrology requirements for advanced node developments and process control are becoming more and more restrictive with shrinkage of dimensions. Currently in R&D, and more particularly in the process development in lithography or etching step, we have to cope with sub-40nm trenches CD measurements for sub-28nm node development.

For such requirements, we are using the 3D-AFM technology as a complementary technique to CD-SEM. Indeed, as CD-SEM is limited in giving information about profiles, the 3D-AFM technology must be considered. To succeed in measuring on a repeatable way and accurately sub-40nm trenches and contact holes, the 3D-AFM tips diameter has to be manufactured within tight specifications and the relative accuracy tip to tip must remains constant and reliable.

In this paper, we will present a large set of data related to the use of various 3D-AFM tip models (diameter, tip edge, tip material, stiffness...) from large model to tiny model with typical tip diameter of 15nm. We compare the performance of each model in term of accuracy and repeatability, and extrapolate the industrial requirements that are necessary for tip manufacturing in order to be compatible with advanced roadmap requirements. Finally, we will present as function of tip model the relative accuracy of CD measurements.

7638-69, Poster Session

Immersion lithography micro-bridge defects: characterization and root cause analysis

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Defect review of immersion lithography specific defects is becoming more and more challenging as feature sizes decrease. Previous studies using a defect review SEM have resulted in a defect classification scheme which, among others, includes a category for micro-bridges (Ref. [1]). Micro-bridges are small connections between two adjacent lines in photo-resist and are considered device killing defects. Micro-bridge rates also tend to increase as feature sizes decrease, making them even more important for the next technology nodes in immersion lithography.

Especially because micro-bridge defects can originate from different root causes, the need to further refine and split up the classification of this type of defect into sub groups may become a necessity.

Whereas for a large percentage of immersion specific defects the main root cause is known and the right measures to reduce or prevent those defects are available (Ref. [2]), this is not the case for micro-bridge defects. Among others, image and resist contrast implications, developer contributions, BARC contributions, the location and size of particles and bubbles in immersion fluid, and resist manufacturing filtration may all be contributors to micro-bridge defectivity.

This paper focuses on finding the correlation of the different types of micro-bridge defects to a particular root cause based on a full characterization and root cause analysis of this class of defects.

Regular top-down SEM-images have not proven useful in breaking down the classification of micro-bridges into subgroups due to their very small size (on the order of half-pitch size), so the scope of this work is to define a more detailed sub-classification of this class of defect and identify their (probable) root causes by using advanced SEM review capabilities like high quality imaging in very low FOV, MPSI (Multi Perspective SEM Imaging), tilted and rotated stage imaging and even FIB (Focused Ion Beam) cross sectioning.

All these features combined will contribute to form a 3D-like representation of any micro-bridge, which is essential for a thorough characterization of these defects. To achieve this, a two-step approach has been adopted (Figure 1). First step has been to deliberately detune several lithographic parameters, which are known to be candidate root-causes for micro bridging defects, to generate wafers with intentionally high levels of micro-bridges and perform regular SEM defect review. This way, it has been possible to have a statistical number of defects generated by the root cause source. Following, a characterization procedure has been used for each of those wafers based on manual tilt and rotation stage imaging and FIB cross sectioning in order to define the predominant type of micro bridge defect.

A completed conclusion matrix which will allow correlating the type of micro-bridge to the possible root-cause will be generated in this work. Figure 2 reports an example of final characterization where, by use of combined advanced SEM review capabilities additional information needed to finalize the root cause and analysis of micro-bridges, a masking defect type of micro-bridge has been fully characterized.

7638-70, Poster Session

Evaluation of wafer intelligent scanner to detect immersion pre-exposure defects

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(United States)

Defectivity control continues to challenge advanced semiconductor manufacturing, especially immersion lithography processes. Immersion exposure tools are sensitive to incoming wafer defects, including top coat voids, surface defects, and other random or systematic anomalies. A single defective wafer could contaminate the exposure tool's immersion hood resulting in lengthy and costly repairs. To mitigate this problem, TEL developed an integrated and real-time macro inspection solution to identify defective wafers which could potentially damage immersion exposure tools.

The Wafer Intelligent Scanner (WIS) module integrates within the CLEAN TRACK LITHIUS Pro platform without impacting footprint or throughput. By utilizing user defined inspection criteria, wafers can be inspected prior to and after exposure for macro defects. Wafers failing to meet inspection criteria prior to exposure are automatically re-routed to bypass the exposure tool and following process modules.

Micron recently evaluated TEL's WIS module in order to assess its capability to identify defects prior to immersion exposure. This paper will outline the evaluation and provide data on the effectiveness of this module to prevent defective wafers from damaging the immersion scanner. Additionally, using this module for post develop macro inspections will be investigated.

7638-72, Poster Session

HVM die yield improvement as a function of DRSEM ADC

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Given the current manufacturing technology roadmap and the competitiveness of the global semiconductor manufacturing environment in conjunction with the semiconductor manufacturing market dynamics, the market place continues to demand a reduced die manufacturing cost. This continuous pressure on lowering die cost in turn drives an aggressive yield learning curve, a key component of which is defect reduction of manufacturing induced anomalies. In order to meet and even exceed line and die yield targets there is a need to revamp defect classification strategies and place a greater emphasize on increasing the accuracy and purity of the Defect Review Scanning Electron Miscrope (DRSEM) automated defect classification results and placing less emphasis on the ADC results of patterned/un-patterned wafer inspection systems. The increased emphasis on DRSEM ADC results allows for a high degree of automation and consistency in the classification data and eliminates variance induced by the manufacturing staff.

7638-73, Poster Session

Minimizing the outgassing of spin-coated organic materials to reduce defects

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Maintaining low-defect spin-applied films is paramount to the success of semiconductor manufacturing. While some spin-on films have a low number of defects as coated, defect levels can rise with the number of wafers processed. Thin organic films may outgas or sublime during the post-coat baking process, or even during subsequent exposures to deep or extreme ultraviolet radiation. If these outgassing components collect on the lid of the hot plate chamber, there is an increased risk of "fall-on" defects on later processed wafers. To increase throughput, preventive maintenance and cleaning schedules are pushed to the limit to provide maximum output from the track. New materials must be designed to produce minimal outgassing to ensure maximum throughput without defects. Early tests for measuring outgassing provided qualitative results gained from collecting the condensed outgassing components on a quartz wafer and measuring the absorbance of the resulting film. A more advanced technique involves the use of a newly designed quartz crystal microbalance (QCM) to more carefully quantify the amount of outgassing.[1] As the industry continues to mature, more sensitive measurements are required to design new materials with even lower outgassing from sublimation. Described in this paper is the use of the next generation of QCM testing for the development of low-subliming coatings. Improvements in sensitivity and repeatability have led to a better understanding of how to mitigate outgassing through synthesis and formulation of materials.

7638-74, Poster Session

High-resolution defect metrology for silicon BARC analysis

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Detecting the small defects in anti-reflective coatings capable of creating a blocked etch, bridge, defocus, or similar problem is a continuing challenge. The critical minimum defect size is currently approaching 20 nm, and state-of-the-art filter pore size for lithography materials is in a similar range. This investigation examines the types and sizes of defects in various silicon hardmask spin-on layers using an Hitachi LS-9000 Surface Scanning Inspection System (SSIS) and RS-5500 Defect Review Scanning Electron Microscope (DRSEM). These systems have advanced capabilities enabling detection, classification and characterization of defects in the size range of interest - smaller than 50 nm - for current technology. Silicon spin-on hardmasks are chosen due to their unique chemistry and rising popularity in the industry for the most challenging patterns. The number and types of anomalies such as pits, bumps, particles, and other defects are adjusted by various formulations including interactions with the spin-on carbon underlayer in a trilayer stack, depicted in Figure 1, highlighting the sensitivity of the metrology as well as the material understanding. The LS-9000 is equipped with a short wavelength probe source and a sophisticated signal processing module. SEM review with the RS-5500 resulted in very low false counts and insights into the defect mechanisms from multiple detectors. Energy dispersive X-ray analysis (EDX) allows further cataloging of defect type, which is very helpful for root cause analysis.

7638-75, Poster Session

Monitoring acidic and basic molecular contamination in leading-edge lithography and metrology applications: quantitative comparison of solid state and impinger-based sampling methods

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Assessing molecular contamination (MC) at part-per-billion (ppbV) or part-per-trillion volume (pptV) levels in cleanroom air and purge gas lines is essential to protect lithography and metrology tools optics and components. Current lithography and metrology tool manufacturer's specifications require testing of some contaminants down to single digit pptV levels. Molecular contaminant certification, that typically also includes organic and refractory compounds, is mandatory to maintain the tool optics warranty. The constant certification exercise allows leading edge lithography and metrology end users to verify their purifier or active filter removal performance avoiding optics hazing and laser light transmission degradation in the long term. Ideally this analysis would be performed with an on-line analyzer (capable of providing almost instant results): the best analyzers currently available are only capable of providing 100 pptV detection. Liquid impinger sampling has been the dominant sample collection method for sub ppbV acidic and basic MC analysis. Impingers draw the sample gas through a solution, typically DI water, and analyze the resulting solution

by Ion Chromatography (IC). Impinger sampling suffers from some inherent problems that can dramatically reduce the collection efficiency such as analyte solubility and evaporative losses. Additionally, most impingers are made of Teflon which is known to leach fluoride ions into the DI solution making accurate assessments of gas phase fluorine and fluorides almost impossible. An innovative solid-state trapping technology has been recently developed by SAES Pure Gas along with the CollectTorr sampling system. NIST traceable gas phase standards have been used to compare the collection efficiency for both acids and bases of the traditional impinger technology to that of the solid state trapping method at both ppbV and pptV levels. Two impinger samples were collected for each sampling event along with three solid-state samples installed in the CollectTorr sampling system. Results varied greatly for the different acid gases with sulfur dioxide showing comparable collection efficiencies while hydrofluoric acid and hydrochloric acid showed much lower recoveries in the impingers than the solid-state traps. Ammonia collection efficiencies were slightly higher for the solid state traps and were improved in the impingers when an acidified solution was used as the collection media. The use of solid-state traps, besides being much simpler from both the handling and logistical stand point, eliminates the analyte solubility and evaporation problems frequently seen with the impinger sampling.

7638-76, Poster Session

Method for wafer edge profile extraction using optical images obtained in edge defect inspection process

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Immersion Lithography has been introduced as the only candidate for high volume production of 45nm or less technology node in recent years. Wafer edge conditions have attracted the attention of process engineers more than ever.

In a coating process the beveled area has to have hydrophobic profile such as a topcoat down to some height from the wafer top. Therefore the wafer edge profile should be taken into account in order to analyze the water behavior around the wafer edge.

Two methods for examining the edge contour are defined in SEMI MF928-0305. One is a destructive method and for discrete points' inspection. The other is nondestructive but requires collimated back lighting to define a sharp shadow on the screen.

A newly developed method has been proposed in this study where the brightness data of optical images are converted to wafer edge profile. This new method can calculate all points on the wafer periphery with the high speed for both contour at each point and also the wafer outer shape.

Unique illumination system and optics are used as the main sensors in a Nikon edge inspection tool WES-3000. Its upper bevel camera is installed nominal to the wafer surface and can capture the bevel area from the bevel boundary to Apex area with its diffusion illumination system and deep DOF optics.

The edge profile is calculated from the entire bevel area in optical images that are in focus. Profile of all the edge area from top surface border to the bottom surface border is then calculated by combining it with the Apex camera images and the lower camera images. The upper camera images provide the wafer outer shape information.

Interference from particulate contaminants is discussed in the SEMI document. Those defects may reduce the brightness, and as a result the profile calculation process may be affected. However, the system can automatically output the location of defects such as particles and stains because our image capturing process is exactly the same as the normal edge inspection process.

Several tests performed on bare wafer samples show that even newly shipped bare wafers may not have constant shape over 360 degree periphery. In some case, some repeated deformations with 90 degree pitch are observed.

So far it is not clear that there is a relationship between wafer edge shape and performance in an immersion process.

All the wafers' profile should be monitored and traced whether it has something to do with immersion process performance as a scenario for wafer shape monitoring.

Such a scenario would be realistic on this new method since the tool can process wafers up to 100wfr/hr. It makes it possible to monitor all the incoming bare wafers to FAB tagged with wafer ID, and trace the performance of each wafer in an immersion process.

7638-77, Poster Session

Influence of error distribution shape on process capability analysis and process control

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Process control and management are based on statistics. The parameters for process control are determined from descriptive statistics such as mean, median, variance, standard deviation and many more calculated from metrology data. Process capability is generally derived from mean and standard deviation.

Such statistics include uncertainty in describing the behavior of a population. The uncertainty comes from measurement error and sampling plan in which measurement positions and frequency are defined. Continuous shrinkage of device design requires the reduction of the uncertainty as well as the reduction of process tolerance.

The shape of error distribution (i.e. probability density function) is the most critical for the uncertainty. When an error distribution is skewed, only a standard deviation is insufficient to express the error behavior.

Overlay (OL) distributions and critical dimension (CD) distributions are likely to be assumed as normal distributions. In many cases, however, actual error distributions appear skewed and/or peaked or flat relative to a normal distribution. Mismatch between assumed distribution and actual distribution yields risks in various aspects such as lot acceptance sampling, statistical process control (SPC), and advanced process control (APC).

In this paper, we discuss the impact of shape of error distribution on process capability analysis. Process capability analysis with Cp and Cpk is widely used for the assessment of process maturity. Classical conventional Cp and Cpk are calculated with a standard deviation on the assumption that distribution is followed as normal distribution. We found that CD distributions of advanced CMOS devices are likely to be flat compared with normal distributions. It is because initial errors at the tails of distributions are corrected by OPC or DfM tools to be within a tolerance range in the early stage of device development. In the case of such non-normal distributions, the classical process capability analysis may lead to the wrong conclusion. Adequate data conversion such as Box-Cox transformation or Johnson transformation converts a non-normal distribution to a normal distribution, or another metric for process capability is needed. We investigate risks in process capability analysis by Monte Carlo simulation and experimental data analysis.

7638-78, Poster Session

Monitoring and control of photoresist properties and CD during photoresist processing

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Current approaches to control critical dimensions (CD) uniformity during lithography is primarily based on run-to-run (R2R) methods where the CD is measured at the end of the process and correction is done on the next wafer (or batch of wafers) by adjusting the parameter set-points. In this work, we proposed a method to monitor the various photoresist parameters (e.g. photoresist thickness, photoactive compound) and CD in-situ and in real-time. Most of these parameters are sensitive to temperature variations. A spatially programmable

thermal processing system that can provide a desired nonlinear temperature distribution across the wafer is developed in this work. Such a system will provide us with the control authority to manipulate the temperature across the wafer so as to control the with-in wafer photoresist properties and CD uniformity. Through modeling and real-time identification, we develop new in-situ measurement techniques for the various parameters of interest in the lithography sequence using existing available data in the manufacturing process. The correlation between these parameters and CD variations are modeled and with increased real-time in-situ measurement data, real-time prediction and control of the parameters will be performed to compensate for CD non-uniformity within wafer and from wafer to wafer.

An array of spectrometers is used to extract various photoresist properties such as resist thickness and absorption coefficient. Resist thickness and absorption coefficient may be estimated from the reflectance signals of a multi-wavelength spectrometer using a thin film optical model [1]. When light is focused onto the resist film, phase difference between the incident and reflected light creates interference effects within the resist. An optimization can then be used to fit the various resist parameters from the reflectance signals. The CD information is obtained via a scatterometer system integrated into the thermal system. In-situ measurement of wafer temperature is achieved using proximity pins with embedded temperature sensors which the wafer sits on. In-situ estimation of wafer temperature can also be achieved by monitoring the bake-plate temperature profiles and system identification techniques [2]. The wafer temperature can thus be controlled in real-time. Detailed modeling and analysis based on first principle heat transfer principles demonstrate the feasibility of the proposed approach.

Real-time monitoring of the photoresist processing steps is enabled with the array of different integrated metrology. This information can then be used to control the various processing steps. Experimental results demonstrate the feasibility of the proposed approach.

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7638-79, Poster Session

Utilizing run-to-run control to improve process capability and reduce waste in lithography: case studies in semiconductor and display manufacturing, and a vision for the future

J. R. Moyne, Applied Materials (United States)

Run-to-run (R2R) control is now a required component of microlithography processing. Recently, the focus has turned to methods for getting the maximum return on investment (ROI) out of R2R control solutions by improving performance and reducing cost. Experience in deployment has revealed that keys to an effective, high ROI solution include (1) flexibility and reconfigurability, (2) re-usability (e.g., control solution libraries), (3) a phased approach to deployment that begins with simply automating existing practices, (4) robust control algorithms that can reject common microlithography disturbances such as product, reticle, layer and maintenance events, and (5) an extensible solution that can accommodate new control technologies as they are developed. A process control solution infrastructure meeting these requirements has been deployed in semiconductor and display manufacturing, and is being utilized to extend process control capabilities to support virtual metrology.

In a case study of solution application to semiconductor manufacturing, a full feed-forward / feedback overlay control solution was developed and applied at a leading semiconductor manufacturer. Results indicate 100% process capability improvement (Figure 1). These results were achieved by improving process centering as well as reducing process variability. In a case study of solution application to display manufacturing, improved process centering has been demonstrated for TFT overlay (Figure 2), while reduced process variability has been demonstrated for CF overlay (Figure 3). In all of the above cases, solution ROI was further enhanced though utilization of event driven process control development and integration environments that allows for the graphical configuration and maintenance of control strategies, and the easy integration of process control results with other components of the fab manufacturing execution system such as fault detection, and the equipment automation infrastructure.

The high cost of microlithography metrology, lack of consistent wafer-to-wafer or shot-to-shot metrology, and delays in metrology data feedback often means that effective feed-forward/back process control cannot be achieved at the wafer or shot level. A move to more granular process control can improve productivity and reduce waste. Virtual metrology (VM) offers promise in this area as it is a less costly software solution, provides information with much less delay, and can be augmented and adjusted by actual metrology data as available. VM is a modeling and metrology prediction solution whereby equipment and process data, such as in situ fault detection information, is related to post-process metrology data so that this same equipment and process data can be used to predict metrology information when actual metrology information is not available. In one realization of a VM enhanced process control solution (Figure 4), fault detection summary information is used along with adaptive partial least squares (PLS) modeling to predict metrology information. The prediction models are regularly “tuned” when actual metrology data is made available. The VM predictions are then used to fill in the measurement gaps in feed forward and feedback control thus enabling wafer-to-wafer or even shot-to-shot feed-forward/back control. It is anticipated that VM will become an integral part of microlithography process control solutions in the near future, enabling tighter and more granular process control, guiding intelligent measurement strategies (i.e., when to use actual metrology), as well as providing input to predictive maintenance and even yield management solutions.

Figure 1: Implementation of lithography overlay process control in semiconductor manufacturing resulting in improvement in process capability of over 100%. Figure 2: TFT lithography control in display manufacturing shown here improving process centering

Figure 3: R2R Control applied to CF overlay in display manufacturing, reduces process variability

Figure 4: Virtual Metrology enhanced R2R control can enable more granular control

7638-80, Poster Session

Improve scanner matching using scanner fleet matcher (SFM) and automated real-time feedback control via scanner match maker (SMM)

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The cost of state-of-the-art semiconductor fabs is sky-rocketing. Photolithography equipment (scanners) represents the largest portion of that cost. Overlay performance requirements of modern device designs have forced chipmakers to follow scanner-dedication strategy; the scanner that exposed the critical layer must also expose the subsequent layer. This strategy helps guarantee the required overlay performance. However, it reduces the flexibility of the scanner fleet; the scanners required for dedication become a production bottleneck. If mix-and-match strategy can be used, and still achieve the overlay performance required for the critical layer budgets, these bottlenecks can be avoided or reduced.

Scanner overlay matching performance is typically separated into grid-level and field-level performance. Grid-level performance is

(and traditionally has been) controlled in two phases: 1) preventative maintenance (using test wafers) and 2) run-time adjustment (using scanner alignment measurements, per wafer). Field-level (distortion) performance typically does not have a corresponding run-time correction phase, because the number of alignment measurements required is prohibitively large. Therefore, fleet matching is typically characterized by a "matching matrix" strategy; each scanner pair is compared, using a "representative" illumination condition.

One faulty assumption of the "matching matrix" strategy is, that the distortion performance of each tool is static, and that the fleet matching performance is dictated by the collection of static conditions. However, the only conditions that matter at run-time are the conditions of the current and previous scanner. The latest scanner models can adjust the distortion condition of the current layer scanner, at run-time. By making run-time adjustments for the current/previous pair in question, the effective matching performance of the entire fleet is improved, compared to the static "matching matrix" characterization.

The Scanner Match Maker (SMM) system facilitates and optimizes the calculation, delivery and application of the required corrections, automatically at run-time.

The SMM system is implemented in two phases: 1) preparation and 2) run-time correction. The preparation phase consists of exposing and measuring characterization data sets, a small hierarchical subset of all possible scanner/illumination pairings for previous and current layer. At run-time, the scanner requests a correction from the SMM system before exposing the lot; SMM responds with the necessary corrections.

SMM calculates the corrections needed for the current/previous pairing by transitive combination of the characterization data sets. This method allows the total number of characterization data sets to be minimized. The required number of characterization data sets is equal to the total number of scanner/illumination conditions in the fleet, minus one; this is much smaller than the number of pairings required for traditional "matching matrix" strategies. Therefore, the SMM system allows real characterization of multiple illumination conditions per scanner, instead of just one "representative" illumination per scanner.

The SMM system was used to perform dynamic, run-time scanner distortion mix-and-match to improve overlay |mean|+3s by significantly for two critical layer pairs that were originally subject to scanner dedication. Also, the |mean|+3s performance was improved significantly for a layer pair that is allowed mix-and-match pairing.

7638-81, Poster Session

Achieving optimum diffraction-based overlay performance

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Diffraction Based Overlay (DBO) metrology has been shown to have significantly reduced Total Measurement Uncertainty (TMU) compared to Image Based Overlay (IBO), primarily due to having no measurable Tool Induced Shift (TIS). However, the advantages of having no measurable TIS can be outweighed by increased susceptibility to WIS (Wafer Induced Shift) caused by target damage, process non-uniformities and variations. The path to optimum DBO performance lies in having well characterized metrology targets, which are insensitive to process non-uniformities and variations, in combination with optimized recipes which take advantage of advanced DBO designs.

In this work we examine the impact of different degrees of process non-uniformity and target damage on DBO measurement gratings and study their impact on overlay measurement accuracy and precision. Multiple wavelength and dual polarization scatterometry are used to highlight grating damage and the range of process variation over which various types of DBO grating design (sub-segmentation, dummies etc.) remain useable will be characterized. These measurements will be benchmarked against SEM cross-sections and by use of simulations we investigate how well the effect of different degrees of process damage on DBO target gratings can be modeled. In conclusion, we describe the robustness of DBO metrology to target damage and show how to exploit the measurement capability of a multiple wavelength, dual polarization scatterometry tool to ensure the required measurement accuracy for current and future technology nodes.

7638-82, Poster Session

Advanced diffraction-based overlay for double patterning

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Diffraction-based overlay (DBO) has been a well-established candidate for overlay metrology solutions. Previously data of high accuracy and high precision were reported for double patterning process using normal incidence spectroscopic reflectometry (NISR) on specially designed targets composed of 1D gratings in x and y directions.[1-2] Two analysis methods, empirical (eDBO) and modeling based (mDBO) algorithms were performed. mDBO enables measurement with reduced number of pads per target, reducing the total target size and MAM time for overlay measurements.

In current work we evaluate DBO performance using complex 2D targets. The targets comprise of patterns that are similar to those used in conventional imaging metrology, e.g., box in box. The patterns are repeated in two dimensions to form gratings. Pitch, CD and offset between two sets of boxes are optimized to maximize diffraction efficiency and overlay sensitivity. Overlay errors in x and y directions can be detected and de-correlated by measuring diffraction signals in two orthogonal polarization states. One motivation of 2D target over 1D target is to further reduce silicon real state occupied by DBO targets. Secondly mDBO performance may be more superior for 2D over 1D targets because total number of fit parameters is reduced due to symmetric design in x and y directions, while for 1D targets the parameters for x and y gratings are usually independent of each other due to process variation.

In additional to NISR, we perform ellipsometry measurements on both 1D and 2D targets. Each type of targets is designed to optimize overlay sensitivity and de-correlate x and y directions for a specific technology. For each of the measurements, data are analyzed using eDBO and mDBO approaches. Data accuracy is checked with image-based overlay (IBO) measurements on bar-in-bar and blossom targets printed nearby. In addition, we report precision, TIS and TMU. We evaluate and optimize DBO performance from aspects of target design, hardware configuration and analysis algorithm for double patterning process.

7638-83, Poster Session

Combining image and diffraction-based overlay technologies for advanced process control in DPT regime

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The double patterning (DPT) process is foreseen by the industry to be the main solution for the 32/28 nm technology nodes and even beyond. The requirements of process compatibility, enhanced performance and large number of measurements make the choice of overlay metrology for DPT very challenging. Double patterning approach requires state-of-art [1] overlay metrology performance but, beyond the necessary improvements in terms of metrology uncertainty, an advanced modelling of overlay errors is required in order to enable an effective close loop control for high volume manufacturing. In this paper we propose a combined control strategy that offers the strengths of diffraction based (DBO) and image based overlay (IBO) metrology techniques. The feedback to the scanner is determined using an optimized combination of the two techniques. Diffraction

based overlay metrology is today mature. This technique is very precise and potentially more accurate because TIS insensitive but the size of these targets is still too large to enable high density in-field sampling and high order distortion control. On the other hand, small image based overlay requires a minimum amount of space (down to 5x5 um) but these targets type (small or large IBO) are, in principle, more susceptible to TIS/WIS mean determination and variation. DBO is used to remove TIS sensitive parameter (Translation). Small IBO is used to remove TIS insensitive parameters (Intrafield) and to enable high order Intrafield corrections. We analyze pros and cons of each technique and suggest the optimal metrology strategy. Proof-of-concept of this new methodology is shown experimentally on double patterning processes (Litho-Etch-Litho-Etch (LELE); Litho-Process-Litho-Etch (LPLE).

7638-84, Poster Session

In-depth overlay contribution analysis of a poly-layer reticle

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Wafer overlay is one of the key challenges for lithography in semiconductor device manufacturing, increasingly challenging following shrinking of the device node. Some of Low k1 techniques, such as Double Exposure add additional burden to the overlay margin because on most critical layers the pattern is created based on exposures of 2 critical masks. Besides impact on overlay performance, any displacement between those two exposures lead to a significant impact on CD uniformity performance as well. Mask registration is considered a major contributor to wafer overlay, especially to in-field overlay.

We investigated in-die registration performance on a critical poly-layer reticle in depth applying adaptive metrology rules on registration performance evaluation and performed sophisticated data analysis using Thin-Plate-Splinefit (TPS) and Fourier analysis. Several systematic error components were observed.

7638-85, Poster Session

The impact of total measurement uncertainty (TMU) on overlay error correction

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As device node shrinks, scanner overlay specification is properly upgraded. How about the overlay metrology tool? International technology roadmap for semiconductor does not provide enough information in this criterion. The motivation of this work is to suggest a guide-line to define a proper overlay metrology requirement for a given device node. Total measurement uncertainty, TMU, of overlay metrology is defined as square root of square sum of following items: TIS-mean, TIS-3 sigma, dynamic precision and tool-to-tool match. It is important to remind that TMU depends on process condition. In other words, high TMU is obtained at a back-end layer, while low TMU is measured at a front layer. The impact of TMU on overlay error correction, which includes process and measurement noise, is investigated in terms of the stability of high order correction parameters. By defining the variation range of correctable parameters as a specification, proper TMU of a given device node can be determined. By applying this methodology, preliminary results shows that TMU should be less than 2.1 nm for 40 nm node DRAM device. In a similar manner, TMU requirement for 30 nm DRAM device is defined as 1.0 nm. Detailed methodology and simulation results are presented.

7638-86, Poster Session

Overlay sampling optimization by operating characteristic curves empirically estimated

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Current lithography requires that overlay inspection is more accurate but impacts less on process cost. For these requirements, it is important to reduce sample size without increasing risks of acceptance errors.

For visualizing these risks, there is a powerful method by means of Operating Characteristic (OC) curves, which are probabilities of lot acceptance as a function of fraction defectives, where probability of lot acceptance is defined as the ratio of accepted lots at some sampling criterion out of the total number of lots inspected, and fraction defective is the rate of inspection points which are off specification. OC curves are used for estimating a risk of rejecting a good lot (producer's risk) and accepting a bad lot (consumer's risk). A typical usage of OC curves can be found, for example. In this way, the optimal sampling plan is determined by means of OC curves. The authors have applied the OC curves to the optimization of overlay sampling plans.

Theoretical OC curves are estimated under two assumptions that sampling is random and distribution of overlay data is normal. One of the authors already studied the gap between theoretical and empirical OC curves when the latter assumption is not true. The authors found that even though the latter assumption is true, the theoretical OC curve sometimes looks far from actual data. Actual probability of lot acceptance has a tendency that it lies lower than the theoretical OC curve for a small fraction defective and lies higher for a large fraction defective. In such cases, we would underestimate both producer's and consumer's risks using theoretical OC curve.

The authors find that the gap is originated from stratified sampling: the magnitude of the gap is determined by the ratio of inter and intra strata variance. Some results of overlay sampling optimization using empirically calculated OC curves will be reported.

7638-87, Poster Session

Improvement of alignment and overlay accuracy for sub-40-nm DRAM

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In recent years, DRAM technology node has shrunk below to 40nm HP (Half Pitch) patterning with significant progresses of hyper NA (Numerical Aperture) immersion lithography system and process development. Especially, the development of DPT (Double Patterning Technology) and SPT (Spacer Patterning Technology) can extend the resolution limit of lithography to sub 30nm HP patterning. However it is necessary not only patterning technology but also tighter overlay control to develop the sub 40nm DRAM because of small device overlap margin. Since new process technologies such as complex structure of DPT and SPT , new hard mask material and extreme CMP process have also applied as design rule is decreased, the improvement of scanner alignment performance is very important.

In this paper, we will present the characterization of alignment and overlay performance for sub 40nm DRAM.

First, alignment performance on several alignment key design and complex hard mask structure is investigated through simulation. The predication of alignment performance is useful for alignment key design and reduction of mask cost because alignment key design is determined on mask level. From comparison with experiment and simulation result on alignment performance for sub 40nm DRAM, we are able to expect alignment performance and optimize the alignment key for each structure. Then we have studied the overlay controllability with various methods such as the optimization of overlay vernier, application of the high order process correction and reduction of process effect.

7638-88, Poster Session

Mask registration and wafer overlay

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Overlay continues to be one of the key challenges for lithography in semiconductor manufacturing. It becomes even more challenging due to the continued shrinking of the device node. Some low k1 techniques, such as Double Exposure and Double Patterning also add additional loss of the overlay margin due to the fact that the single layer pattern is created based on more than 2 exposures. Therefore, the overlay between 2 exposures requires very tight overlay specification.

Mask registration is one of the major contributors to wafer overlay, especially field related overlay. We investigated mask registration and wafer overlay by co analyzing the mask data and the wafer overlay data. To achieve the accurate cohesive results, we introduced the combined metrology mark which can be used for both mask registration measurement as well as for wafer overlay measurement.

Coincidence of both metrology marks make it possible to subtract mask signature from wafer overlay without compromising the accuracy due to the physical distance between measurement marks, if we use 2 different marks for both metrologies. Therefore, it is possible to extract pure scanner related signature and analyze the scanner related signature in details to support the root cause analysis and finally drive higher wafer yield. We applied the exact mask registration error for the wafer overlay decomposition into mask, scanner, process and metrology. We also studied the impact of pellicle mounting by comparison of mask registration measurement between pre-pellicle mounting status and pos-pellicle mounting status in this investigation.

7638-89, Poster Session

Effect of wafer geometry on overlay

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Wafer geometry variations result in elastic deformation during wafer chucking that can cause significant in-plane distortion and overlay errors in lithographic patterning. As feature sizes shrink, overlay errors due to wafer geometry on a scanner before patterning become a larger fraction of the error budget and must be controlled. In this work, a finite element mechanics model and lithographic correction post processing scheme was developed to predict overlay errors from high-density wafer shape measurements on KLA-Tencor's WaferSight 2 tool. Using the model, overlay errors due to chucking were examined for multiple wafers with different geometries. The results show that long spatial wavelength corrections cause significant distortion, but can be largely mitigated through the use of simple first-order corrections applied on a typical lithography scanner. In contrast, higher frequency spatial variations cause distortions that cannot be corrected and hence lead to meaningful overlay errors. The results presented provide fundamental insight into chucking-induced overlay errors and can serve as a basis for the development of higher order scanner correction schemes that explicitly account for the wafer geometry. Wafer geometry measurements can also be used by the scanner to meet the overlay requirements at smaller nodes.

7638-90, Poster Session

Overlay control strategy for 45-nm/32-nm RD and production ramp up

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The tight overlay budgets required for 45nm and beyond makes overlay control a very important topic. High order overlay control is becoming an essential methodology to remove the immersion induced overlay signatures. However, to implement the high order control into dynamic APC system requires FA infrastructure modification and a stable mass production environment. How to achieve the overlay requirement before the APC-HO system becomes available is important for RD environment and for product early ramp up phase. In this paper authors would like to demonstrate a methodology to improve high order overlay signature without changing current APC-linear control system.

From author's previous works, high order overlay component was a significant factor in overlay control. Lithography engineer could improve the high order overlay component by implementing scanner high order alignment or zone alignment while wafer was on scanner stages. However, scanner throughput reduction is the price to be paid. In contrast, author's methodology is to improve the non-linear (or high order) overlay component while no-high order alignment or minimum zone alignment was implemented on scanner. The non-linear high order signature was monitored during product ramp up phase to understand the stability of high order component. Through simulation, by removing a common high order signature from all the monitored lots, 1~2nm overlay improvement was observed from all the lots excluding the RD lots.

Non-linear overlay signature was analyzed using user defined data model in KLA-Tencor's K-T Analyzer (KTA). Then a field-by-field correction (FxFc) file by averaging linear residual signatures among all the monitored lots was generated in KTA and thereafter sent into scanner as a fixed scanner lookup table to correct high order component. Since high order component could drift due to many reasons, hence frequent update the lookup table is required. It is important to have a continuous monitoring system to compare the current high order signature with scanner stored FxFc lookup table. Once the current high order signature goes beyond the threshold of tolerance, this indicates the FxFc lookup table should be updated from scanner. To maintain overlay control within spec and not to update the FxFc file too frequent, author would characterize the long term overlay signature and then determine the optimal threshold for updating scanner FxFc file.

In summary, before APC-HO control becomes available for mass production, in the RD or early product ramp up phase overlay performance requirement can be achieved by using a threshold triggered updating FxFc file without changing the APC-linear control system. However, the drawbacks of this methodology are (1) it requires all fields to be measured (2) it is less dynamic on responding the drift of high order signature.

7638-91, Poster Session

Development for a 2D pattern quantification method on mask and wafer

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We have developed a novel 2 dimensional metrology on both mask and wafer features. The purpose of this method is to evaluate the printability on wafer corresponding to Hotspots on mask. The method adopts a novel metrology system for DBM (Design Based Metrology), by utilizing a highly accurate measurement-based contouring on mask and wafer CD-SEMs (Critical Dimension Scanning Electron Microscope).

Downsizing semiconductor manufacture necessitates more aggressive optical proximity correction (OPC) to drive the super-Resolution Enhance Technology (RET), which leads to a trade-off between highly precise RET and mask manufacture. For complicate OPC pattern optimization, wafer printability analysis and hotspot verification, 2-dimensional pattern shape quantification becomes a challenging topic on metrology, instead of conventional 1 dimensional CD measurement technique.

In this study, a measurement-based edge detection algorithm is applied for the contour generation. A novel average contouring method for 2 dimensional pattern evaluation to quantify pattern variation has been developed. Moreover, for the first time, contour results of identical points on mask and wafer were studied under the same metrology systems. It becomes feasible to evaluation / optimize the following items on mask by comparing the same pattern printed on wafer:

Analysis the shape variability correlativity between mask and wafer and process margin.

Optimization for 2-dimensional OPC pattern on mask.

Verification of the performance of the pattern of various kinds of Hotspots.

In this report, we present both experimental and simulation results on mask and wafer features, and results are compared with the simulation results based on mask CAD (Computer Aided Design) data. As a consequence, it indicated that it is very crucial to develop such methodology to analysis the 2 dimensional pattern shape of the same location on mask design, real mask pattern, and wafer pattern. We consider that such metrology can be very useful for complicate shape optimization on mask production, which will make a huge contribution to mask yield-enhancement and DFM solution on mask quality control process.

7638-92, Poster Session

Contour self alignment for OPC model calibration

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SEM contours have been used to complement CD measurements in OPC model calibration. The use of contour data is as an attempt to capture 2D-shaped information of features into the model while CD measurement data is kept to maintain accuracy for 1D feature. As the method progresses, there are emerging challenges that are normally not found in CD based calibration. One such challenge is the need to align contours on the calibration feature. This is particularly important in determining model accuracy since contour calibration typically involves a cost function to compare the SEM contours to the features' simulated prints.

This work explores a technique to include evaluating contour alignment/misalignment in the calibration cost function. For each contour and its corresponding simulated print, the cost function returns an error value for a given set of model parameters. The error represents how well the model simulation compared to input contour. In addition, it also contains information on how far or how close the contour is aligned to simulation. Misalignment is to be eliminated on the fly during calibration and to be reported at the end of calibration. In this paper, we describe the proposed technique and compare the results of calibration between aligned and misaligned contour data.

7638-93, Poster Session

From pin-point design-based critical dimension metrology toward comprehensive evaluation of IC patterning integrity

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Semiconductor manufacturers bringing a new product to market go through several phases: design, manufacture, debug, and ramp to production volume. Debugging the first silicon of a product contributes significantly to the product development cycle time. The debug cycle time contribution is significant in part due to the fact that current defect filtering approaches don't capture all of the defects. Hot spots identification via simulation is a typical such defect filter. Eventually defects on the wafer are found that slipped through the filter(s), requiring a further cycle of adjustments to be made to the models and design. This rework takes time and delays market entry proportionately. Overall, the debug phase represents an opportunity for shortening the time it takes to bring a product to market by improved defect detection. Simulation tools used during the design and manufacturing phase are critical to identifying design/process interactions that may reduce product yield or impair product functionality. In this paper we will discuss a supplemental approach to these tools, which has the potential to more quickly detect and correct the defects that escape the current approaches, by opening up the full chip to review and adjustment, layer by layer, largely while the wafers are still running in the line.

Currently CD-SEM is used mostly for analyzing small areas on a clip-by-clip basis, with clips in the approximate range of 1-10 microns on a side. An array CD-SEM images, taken side by side may be collected, rarely, but arrays of images are not used as a regular part of the debug process, at least to the knowledge of the authors. Use of full chip CD-SEM maps of the critical layers, in combination with a defect or hot-spot identification engine, has the advantage of enabling a complete capture of the unfiltered defects or hot spots, and make information on them available earlier in the debug cycle.

It has been determined by the authors that individual SEM images, taken across the entire chip/critical area can be processed and assembled, or stitched together, accurately to create an image of each separate process layer. Experiments to date have verified that CD-SEM has the required accuracy, and image maps have been successfully created. It has also been found that feature contours, across SEM image boundaries can be made to align, and that the assembled view can then be extracted to provide detailed information of the physical edge profiles of all of the features. Extracted features from this exercise were compared with lithography simulations of the same features, and differences identified for further inspection and analysis. Data and contours from such a system can then be exported to other simulation tools for further analysis.

In this paper we demonstrate the process of creating a full-chip SEM view of a chip, for multiple critical layers, as the wafers progressed through typical logic manufacturing process steps, including critical layers like metal 1, via and metal 2, using an older generation technology and older generation CD-SEM; however, it is expected that the approach would apply equally well to newer generation equipment and technology. We demonstrate the utility of the methodology by comparing the extracted features to both the product design and simulation. Finally we show results of identification of defects that were missed during the simulation-based hot-spot identification phase.

7638-95, Poster Session

Application of model-based library approach to photoresist pattern shape measurement in advanced lithography

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The availability of immersion lithography has opened the way to higher NA (Numerical Aperture). In pattern formation using a higher NA, the shape of resist patterns is affected by a variety of factors, and a great variety of patterns can be deposited. The reduced depth of focus particularly affects pattern formation. The variety of patterns due to various layouts and OPC (Optical Proximity Correction) calibration also occurs. An etching process will later be influenced by the pattern, and

the feature patterns of the processed layer exhibit variation. The etched pattern's width and sidewall angle vary depending on the shape of resist pattern. The current design can't be achieved to take the etching bias (litho-etch bias) model using the cross-section shape into account. For the correction of etching bias caused by the pattern shape, the etching bias model using the cross-section shape is required. There is a growing importance to measurement the shape of resist patterns along with CD (Critical Dimension) value. Therefore it is necessary to evaluate not only a conventional pattern width but also the shape of pattern such as the sidewall angle, the top width, and the bottom width. However it is not easy to perform non-destructive measurements of 3D structures on actual sample patterns.

For these issues, we have been developing the 3-dimensional measurement method using MBL (Model-Based Library) approach with a CD-SEM (Scanning Electron Microscopy). This technique estimates the dimensions and shapes of a target pattern by comparing a measured SEM image profile to a library of simulated line scans. MBL matching uses a physics based mathematical model of the SEM image generation process and is expected to be capable of eliminating measurement bias that depends on the pattern shape. Most previous studies improved the measurement accuracy, the physics based mathematical model and the library. In this study, application of Model-Based Library Approach has been evaluated experimentally in advanced lithography. MBL matching measurements were applied to the litho-etch bias evaluation. To evaluate layout-dependent photoresist pattern shape variation and its effect on the litho-etch bias, photoresist patterns of various layouts were exposed by a leading-edge immersion lithography system of NA 1.35. The cross-section shapes were estimated using MBL at initial photoresist patterns, also were estimated after the etching process. The relationship between the etching-bias and the cross-section shape at initial photoresist patterns was evaluated. Through an investigation, we studied the effectiveness of the cross-section shape information. As a result of the evaluation, it was found that the cross-section shapes at initial photoresist patterns are associated with the etching-bias. These results show that the effective margin evaluation is possible for advanced lithography process and suggest that the efficient lithography-etching process development can be achieved using MBL approach.

7638-96, Poster Session

Study on practical application to pattern top resist loss measurement by CD-SEM for high-NA immersion lithography

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With the semiconductor technology of small further pattern after 45nm hp node, introduction of a high-NA immersion lithography technique progresses, and the decreasing process latitude becomes big issues to lithographers. The decreasing depth of focus margin by lithography tool is mentioned to one of the important problems which are feature issue of a high-NA immersion lithography process. As for that, especially tool focus fluctuation has impact on resist pattern shape sensitively, and the decreasing pattern height (the resist loss) occurs to resist patterns, not only CD changes. As a result, it is understood that the resist loss influenced pattern formation of after etching process, [1]. It is important to feed back the quantified pattern shape information to a Litho-process for the issue of the decreasing process latitude. As for using quantified 3D pattern information by CD-SEM, we have to discuss the practical process control in epoch of high-NA immersion lithography.

We have been studying the technique for monitoring the resist pattern shape from the top down image by using CD-SEM. It was shown to be able to monitor a slight change in the resist pattern shape as a quantified amount of the SEM signal wave fluctuation, [2]. Previously, only a qualitative decision was possible for detecting the slight change in resist pattern shape. We are promoting the research which the amount of SEM image characteristics is used for, a resist loss measurement function as that one, is proposed. We observe correlation between the resist top roughness and the resist loss, and evaluate the resist loss measurement function by the quantified resist top roughness. This principle of resist loss detection by measuring roughness is that a changing roughness of resist pattern top is detected as the fluctuation of SEM image brightness. A measurement idea is proposed, and performance evaluation has already been enforced by using one kind of sample, [1].

In this study, we demonstrate the validity of resist loss detection by investigating the various condition of wafer which is contained the dependency by the kind of resist or the resist shape change by the difference process. We finally discuss the limit of the resist loss measurement function and consider the applicability of this definitely.

[1].Mayuka Osaki, Maki Tanaka, Chie Shishido et al., "Advanced CD-SEM metrology to improve total process control performance for hyper-NA lithography," SPIE, 6922-45, 2008

[2].Toru Ishimoto, K.Sekiguchi, N.Hasegawa, K.Watanabe et al, "Further study on the verification of CD-SEM based monitoring for Hyper NA Lithography," Proceeding of the SPIE, vol.6922, 6922O-1, 2008

7638-97, Poster Session

Comparison of different algorithms to determine areas from SEM images

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We present a comparison of different methods to extract area information from images. Two different algorithms were tested which determine the areas of arbitrarily shaped 3D nanostructures on wafers or photomasks (e.g. contact holes) using secondary electron (SE) images of scanning electron microscopy (SEM). One was developed by the PTB based on physical modeling, the other one is the software package MaskEXPRESSTM developed by Toppan Printing.

Additionally, we used Monte Carlo generated SEM images of different shaped contact holes to test the algorithms with simulated structures of exactly known size. For this, the Monte Carlo simulation program MCSEM, developed at PTB, was applied. MCSEM simulates the electron diffusion and SE generation and transport in solid state and provides simulated SEM images of arbitrary 3D specimen structures.

The PTB algorithm uses pre-evaluated edge information to extract one-dimensional profiles which intersect the structure boundary perpendicularly. A one-dimensional edge detection algorithm detects the edge position on each profile. Finally these detected edge positions are used to calculate the polygon area by triangulation. The PTB algorithm showed a very small overestimation with regard to the Monte Carlo simulation of about 1-2 % of the area.

MaskEXPRESSTM has a similar approach, however employs a different edge detection algorithm. For the two tested programs a very high correlation coefficient cc larger than 0.99 of the CDs was seen with an observed offset of about 13 nm for quadratic contact holes (Figure 1). Here, the CD is defined as the square root of the area. The CD deviations were smaller than 1 nm over the whole investigated range. For arbitrary shape analysis we used a double T shaped structure. Also here, almost perfect correlation was found (cc = 0.977). The mean offset was about 17 nm (Figure 2). The offset values depend on the length of the boundary and can vary with the shape of the structure.

The excellent correlation found for both algorithms is an important prerequisite for standard area measurement based on independent algorithms and pave the way to standard area determination and reporting of photomask structures.

7638-98, Poster Session

Evaluation of 25-nm pitch SiO_2/Si multilayer grating reference using CD-SEM

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We have proposed a novel multi-layer grating reference having sub 50-nm pitch size for CD-SEM magnification calibration [1]. In this paper 25-nm pitch grating pattern was evaluated by CD-SEM. Such fine pattern was fabricated by SiO2/Si multi-layer deposition and material selective chemical etching. Amorphous Si and SiO2 thin film were alternately deposited on silicon wafer. After polish process of the cross-section surface, HF: H2O (1:200) solution was used for SiO2 selective chemical etching. Due to deep line and space pattern of Si/SiO2 multi-layer, high-contrast SEM image of grating pattern was obtained under 1 kV acceleration voltage with CD-SEM. The uniformity of the pitch size of the grating with 25-nm pitch size was smaller than 1 nm in 3-sigma. Also the line edge roughness of the grating pattern was smaller than 1 nm. The pitch size accuracy was assured by X-ray surface diffraction method [2]. Such fine and uniform grating pattern will fulfill requirements of next-generation CD-SEM magnification calibration reference.

1. Y. Nakayama et al., SPIE 7272(2009)727224-1.

2. to be presented in SPIE 2010.

7638-99, Poster Session

Improved recipe quality control: from development to mass production

Y. Nakata, S. Koshihara, H. Kawada, K. Yang, J. Kakuta, T. Ishijima, Hitachi High-Technologies Corp. (Japan)

Process monitoring and control is critical to maximizing yield and efficiency in the semiconductor manufacturing process. For some time, critical dimension scanning electron microscopes (CD-SEM) have been used for the process monitoring and dimensional control of semiconductor devices within a mass production line. In order to support higher speeds and to reduce energy consumption, semiconductor devices continues to evolve. Consequently, the manufacturing process must also adapt in order to meet the stringent process control requirements of these more complex devices. Hence, the role of the CD-SEM has become an increasingly more important tool in the process monitoring of a mass production line.

The CD-SEM performs automatic measurements according to the recipe conditions programmed in advanced. Traditionally, CD-SEM recipe creation requires not only a knowledgeable engineer but also suitable wafers and scheduled down time on the production equipment. At times when the CD-SEM is under heavy utilization, the time required for creating these voluminous recipes has a significantly negative impact to overall productivity. Additionally, errors in these recipes require operator intervention further impacting the production line.

Adding to the complexity, the wafers used for recipe creation are frequently not suitable for creating robust, error-free recipes. Often times short flow wafers are used for these setups making it extremely difficult to allow for inherent process variations. When errors do occur during recipe execution, it is normally possible to continue with the measurement sequence if an operator manually assists the CD-SEM but this is at best a temporary solution and contributes to inefficiency. Ultimately a correction of the recipe is necessary, again requiring engineering time, tool time and additional cycle time for the product.

The ideal solution is to create high quality, robust recipes that have a very low frequency of error and does not require wafers, tool time, or a the time of a skilled engineer. This concept of improved recipe quality control is the impetus behind this paper. The use of DesignGauge, a Design Based Manufacturing (DBM) tool, allows for wafer-less recipe creation at the development phase utilizing reticle design information and requiring no down time on the production CD-SEM tool. The ability to create high quality recipes for volume manufacturing, before the first wafer is even produced, contributes to improving overall cycle time during the introduction phase of new designs to the manufacturing line. Leveraging the automated recipe creation process increases production time available to the CD-SEM and minimizes the reliance on experienced engineers to create and/or correct wafer-based recipes.

In this paper, we will evaluate the benefit of this new DBM-based metrology for the volume manufacturing fab.

7638-100, Poster Session

Investigation of signal and noise along the path of LV SEM

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Generation of signal and noise and their propagation through the path of LV SEM is investigated. This path is composed of heterogeneous components and processes: random and deterministic, discrete and analogic.

Generic methodology for description of all these components and corresponding processes is proposed. It is based on specially defined first and second order statistical characteristics. Generic relations between characteristics of processes at inputs and outputs of components and components characteristics are developed. All components are classified into 3 types: random excitation components, random lossy media, deterministic components. Generic relations are specialized for each component type.

Expressions for characteristics of signal and noise at different points of the path are found according to the general theory. These expressions allow evaluating contribution of each component to signal, noise and their influence on SNR.

Some practical applications for the theory are indicated. They include simulator of the LV SEM path, which gives simulation of signal corrupted by noise statistically equivalent to noise of SEM, selection of cut-off frequency of antialiasing filter on the input of ADC etc.

7638-101, Poster Session

CD-SEM utility with double patterning

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Requirements for increasingly integrated metrology solutions continue to drive applications that incorporate process characterization tools, as well as the ability to improve metrology production capability and cycle time, with a single application. All of the most critical device layers today, and even non-critical layers, now require optical proximity correction (OPC), which must be rigorously modeled and calibrated as part of process development and extensively verified once new product reticles are released using critical dimension-scanning electron microscopy (CD-SEM) tools. Automatic setup of complex recipes is one of the major trends in CD-SEM applications, which is adding much value to CD-SEM metrology. In addition, as integrated circuit dimensions and pitches continue to shrink, double patterning (DP) has become more common. Thus automatic recipe setup has needed to incorporate capabilities to deal simultaneously with two layers. This has the benefits of allowing the user to measure the two different CD populations and the image shift in the lithography (i.e., the overlay). Local line width variation influences the statistical confidence of a measured CD's representation of the process; a feature called "Average CD (ACD)" measures multiple targets within the field of view (FOV). ACD allows not only measurements of a single data point representing one discrete feature, but also sampling of the mean and variance of the process. These two applications together-automatic recipe creation and ACD-can be used to characterize the DP pattern with statistical significance in both CD and variation.

DesignGauge V5, the automatic recipe utility for Hitachi CD-SEMs such as the CG-4000, is not only capable of offline recipe creation, but also

has the ability to directly transfer design-based recipes into standard CD-SEM recipes for use with DP processes. These recipes can be used for OPC model-building and verification as with previous DesignGauge applications. The software also provides design template-based recipe setup for production layer recipes, which improves production tool utilization, as production recipes can thus be written offline for new products, improving first silicon cycle time, engineering time to generate recipes, and CD-SEM utilization. Another benefit of the application is that recipes are more robust than with conventional direct image-based pattern recognition. Matching a two-layer GDS pattern to features in an image allows the more complex measurements involved in DP characterization.

This work will show an extensive evaluation of DesignGauge V5 with two different types of DP-spacer self-aligned DP (SADP) and double litho double etch (DLDE DP)-including rigorous tests of navigation, pattern recognition success rates, SEM image placement, throughput of recipe creation, recipe execution, and verification of proper measurement of dual CD populations and overlay.

7638-103, Poster Session

Scatterometry simulator for multicore CPU

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Critical dimension (CD) and profile measurements are needed to measure with high precision for use in semiconductor manufacturing process control and nanoimprint technology. Scatterometry is capable of measuring the CD of grating structure down to approximately 22nm. Scatterometry is easy due to having no high vacuum. At present, the scatterometry analysis is developed for the shape measurement in two-dimensional period line division. In the 3D analysis, the enormous calculation times were problems. The last papers on Microlithography in 2004-2008, the 3D-FDTD (finite difference time domain) analysis of the arbitrary shapes for vertical and oblique incidence were completed for isotropic and anisotropic mediums. The sub-grids, alternating-direction-implicit (ADI) and nonstandard (NS) FDTD methods are used for the time shortening analysis.

Scatterometry uses Maxwell's equations to simulate what the light signature might look like, based on input such as grating pitch, film properties, angle of incidence, CD and film thickness. The practical application is to first simulate a large set of possible parameter combinations, generating a large set of spectral signatures, and when the measurements are actually taken on the wafer's grating structures, we find the simulated signature with the closest match to the measured signature. The quality of the results depends not only on the measurement setting parameters, but also algorithms used by the analysis software. The scatterometry equipment is very expensive, and it cannot easily check the performance.

In this paper, we show scatterometry simulation software which has the spectroscopy calculation and optimization algorithm systems. First, the calculation is sped up by parallel computing using a multi-core CPU which makes it easy to do without connecting many PCs. OpenMP and Threading Building Blocks (TBB) techniques are used in the parallel computing. OpenMP is used for the designated repetition loops in a program. TBB makes all parts of the program into the multithread efficiently. Second, we calculate the spectroscopy using the rigorous coupled wave analysis (RCWA) which provides a method for calculating the diffraction of electromagnetic waves by periodic grating structures and periodic holes. We can analyze the two scatterometry methods: 1. Angular two theta scatterometry using a single wavelength light beam and changing the incident and reflected light beam. 2. Spectral scatterometry using the wavelength range at 190nm to around 900nm. In this simulation, we can check the sensitivity for several CD and profile measurements. The implementation of the RCWA for several CD makes spectrum distribution libraries. Next, a genetic algorithm (GA) and a conjugate gradient (CG) method are used as the technique which automatically searches the data which resembles the given spectrum distribution. The optimization using GA is excellent in the global search, but it takes time for the detailed optimization to get the best value. The CG method's solution falls in the localized solution by the multi-crestedness. Then, we get the rough solution by GA and optimize the solution by the conjugate gradient (CG) method. And finally, the results using this simulator are provided.

7638-104, Poster Session

Monitoring of critical dimensions in the sidewall-transferred double-patterning process using scatterometry

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Due to immaturity of extreme ultra violet lithography (EUV) and resolution limitation of 193 nm immersion lithography for 32 nm node and beyond, various double patterning processes have been developed as an alternative process to shrink device size other than improving resolution of photo lithography. Double patterning has been accepted as a process bridging between 193 nm immersion and EUV lithographic process for 32 nm and 22 nm nodes. Recently, a sidewall transferred double patterning process has been introduced to reduce cost and keep enough process margins in device fabrication. For the development of the double patterning process and deployment of the double patterning process to fabrication lines, it is necessary to monitor and control the critical dimensions and profile shapes in the double patterning process. In this paper, we report monitoring of critical dimensions and profile shapes at several process steps of the double patterning process using spectroscopic ellipsometry based scatterometry.

7638-105, Poster Session

Scatterometry measurement for Gate ADI and AEI critical dimension of 32-nm HK+MG technology

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For reducing gate leakage and enhancing device performance, a lots of IC foundries decide to enter novel HK/MG technology and 32-node is a good starting point for novel device introduction. This paper discusses the scatterometry-based ADI and AEI measurement of a gate layer structure with high-k material and metal films. The Wall Angle (WA) and Critical Dimension (CD) of grating structure are critical measurement parameters for 32-node gate process control and characterization. WA and CD of photo-resist (PR) grating structure are gate ADI critical parameters. WA and CD of poly/metal/High-K films grating are the gate AEI critical parameters.

First, the paper discusses the dispersion analysis challenges and approaches for this 32 nm node structure with high-K material and metal films. Verifying all film stacks is very important for building the simulation model. Critical High-k film stack consists of two layers: one interfacial layer and high-k material. Metal film (on the top of high-K material) CD bow profile measurement is a challenge on the gate AEI stage. It is very difficult to measure metal CD bow by traditional CDSEM hardware. Metal CD is a key factor to electricity test for gate AEI stage and OCD model and hardware can provide helpful information on this stage.

Second, the brand-new scatterometry next-generation hardware was used to measure the critical parameters. CDSEM and TEM are both utilized as reference metrology to assess the accuracy performance of next-generation hardware. The next-generation hardware extending wavelength range down into the deep UV (DUV) can provide a noticeable improvement in measurement accuracy owing to the enhanced sensitivity in the shorter wavelength range.

The authors have a lot of experiences on the standard poly gate device on the node 90/65/45/40 by using OCD tools to measure gate ADI and AEI layer. OCD tool has been proven on the inline APC control system to improve process variation compared to traditional CDSEM tool. This paper proving the next-generation OCD hardware is working on the novel HK/MG gate ADI and AEI layer measurement. In the future, this

next-generation hardware will help ramp up new process development and research.

In summary, OCD next generation hardware can achieve HK/MG gate ADI PR CD and WA measurements. ADI results can provide data for Auto Process Control (APC) in-line system and reduce HK/MG gate AEI CD variation. OCD next generation hardware can achieve HK/MG gate ADI poly/metal/high-K CD and WA measurements. AEI results will provide real time information to improve AEI CD variation and allow later implantation process to enhance device performance. OCD next generation hardware with DUV wavelength is helpful for the HK/MG film stack structure.

I have been an UMC LT RD engineer for nearly three years. My major jobs are to develop and maintain advanced LT process, and research SCD(SpectraCD) for 28-node applications. Besides, 45/40-nm POLY-layer process maintenance is also my routine job. HK-MG utilization is a promising candidate for 28-node and beyond. Thus, combining processes with metrology tool experiences, HK-MG(High-K/Metal Gate) applications with SCD are hopefully to provide sufficient process control and yield improvement.

7638-106, Poster Session

Mask defect inspection by detecting polarization variations

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State-of-the-art lithography is often severely influenced by smaller defects than the resolution limits of the mask inspection system. The mask inspection system is required to obtain such small defects in quite low contrast image. However, the mask inspection suffers from noises comparable to signal of the small defect, due to illumination nonuniformity, laser speckle, and fluctuation of the sensor signal. Thus the defect detection sensitivity is restricted by signal-to-noise ratio (S/N) of the defect in the mask inspection images.

In order to overcome this issue, we propose a novel mask defect inspection method that uses detection optics for polarization variation. In this proposed optics, the mask is illuminated by linearly polarized light. The polarization variation image for inspection is then created by the light component that is polarized orthogonally to the illuminated light. Since the variation of the polarization is cased by form birefringence in the mask feature, the defect signal in the polarization-variation image is improved with the defects size shrinking. Thus the mask inspection system can detect small defects with high S/N.

While the defect signals in the polarization variation images can be obtained with sufficient intensity for much smaller defects than the wavelength, the signals for relatively large defects are decreased. Moreover, since the polarization variation images are emphasized especially at pattern edges, the images can not faithfully acquire the mask pattern. To avoid these problems, we simultaneously use conventional transmitted inspection images and the polarization variation images.

This paper discusses the validity of the mask inspection method that detects the polarization variation by using numerical simulation. The simulation results show that this new inspection method is quite effective for 20-nm-size defect and smaller ones.

7638-107, Poster Session

A novel defect detection optical system using 199-nm light source for EUVL mask

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Lithography potential expands for 45nm node to 32nm device production by the development of immersion technology and the introduction of phase shift mask. We have already developed the mask inspection system using 199nm wavelength, and is a effectual candidate for hp 32nm node mask inspection. But, applying 199nm optics to complicated lithography exposure tool option for hp2x nm node and beyond, further development such as image contrast enhancement will be needed. A feasibility study was conducted for EUV mask pattern defect inspection using DUV illumination optics with two TDI (Time Delay Integration) sensors.

Mask inspection optics using 199nm wavelength DUV light has high defect sensitivity because of its high optical resolution, so as to be utilized for leading edge mask to next generation lithography. We developed high sensitivity defect inspection system using 199nm UV light source, simultaneous transmitted illumination and reflected illumination optics. EUV lithography with 13.5nm exposure wavelength is dominant candidate for the next generation lithography because of its excellent resolution for 32nm half pitch (hp) node device and beyond. EUVL-mask has different configuration from transmitted type optical-mask. EUVL-mask is utilized for reflected illumination type exposure tool. Its membrane structure has reverse contrast compared with optical-mask. This nature leads image profile difference from optical-mask. To optimize the inspection system configuration, by using two TDI sensors, which are normally used for simultaneous inspection of reflected and transmitted illumination, concurrent image acquisition optics of different illumination setup is possible. This capability greatly enhances inspectability of EUVL mask.

Figure 1 shows a schematic diagram of the newly designed high and low power illumination image acquisition optics for EUVL mask. In this system, the laser beam for the illumination optics is split into two beams to enter the high and low power illuminator as a reflective light. The two beams are merged to an imaging optics at the bottom side of the objective imaging lens and works as the reflective signal. The XY stage scans the mask so as to capture the two different type of mask image respectively. Each mask image enters the two sets of TDI sensors respectively. Figure 2 shows the TDI sensor signal overview that shows normal inspection image by TDI sensor-A and contrast enhanced image for precise pattern by TDI sensor-B. By using the beam for the high power and low power reflection illuminator, each captured image has different image contrast. One reflected illuminator which has light intensity to achieve image signal within the sensor output range for all pattern profiles on the mask at TDI sensor-A (light intensity: 1). The other illuminator irradiate N times amount light to the mask that of former illuminator. By illuminating the mask pattern with higher power, TDI sensor-B acquire N times output signal to extend the fine pitch pattern contrast, compared to TDI sensor A.To observe the 199nm wavelength optical system potential with two different illumination condition method get to the 20nm node, several type of illumination results also will be presented.

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7638-108, Poster Session

Aerial imaging inspection and IntenCD for source mask optimization

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As the semiconductor industry moved to 4 X technology nodes and below, Low-k1 ArF lithography has practically reached the theoretical limits of single patterning resolution, a regime typically plagued by marginally small process windows. In order to widen the process window (PW) bottleneck, projection lithography must fully and synergistically employ all available degrees of freedom. The holistic lithography source mask optimization (SMO) methodology targets an increase in the overall litho performance with improved process windows for the most challenging patterns by balancing between the mask and illumination source design influences.

The typical complexity of both mask and illumination source that result from a generic SMO process exceeds what the lithographic industry

has been accustomed to. In particular, the SMO literature reports on masks that fully operate as diffractive optical elements, with features that have little resemblance to the final wafer-level pattern; Additionally, SMO illumination sources are characterized by parametric or pixelated shapes and a wide range of transmission values.

As a consequence of the new mask and source designs needed for very low-k1 lithography, qualifying the mask for printing and non-printing defects and accurate assessment of critical dimension becomes one of the main mask inspection challenges.

The aerial imaging technologies of Applied Material's Aera2 mask inspection tool provide enabling solutions for this mask inspection challenge by separating out only the defects that matter and accurately measuring aerial imaging critical dimensions. The unique linear property of aerial defect signal intensity vs. CD variation, is able to supprt the new SMO illumination solutions.

This paper presents the latest SMO mask qualifications research results performed at Applied Materials with a mask containing two dimensional DRAM production structures.

7638-110, Poster Session

Considerations for chemical filter performance for low-molecular weight silicon AMC

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Chemical filtration has become a standard protective barrier to prevent process degradation, UV exposure tool lens contamination as well as for general fab protection in photo-lithography environments.

Silicon containing ("refractory") hydrocarbons are a class of airborne molecular contamination (AMC) causing persistent degradation of UV exposure tool optical surfaces. Many of these chemicals, such as siloxanes with two or more silicon atoms are captured effectively by chemical filters. However, trimethylsilanol (TMS), a low molecular weight / low boiling point silicon AMC is not captured well by carbon-based filters, and hexamethyldisiloxane (HMDSO), even though captured well, can be converted to TMS when using common acid-based or acid coated filter media.

For our studies, we used a versatile wind tunnel facility for the testing of semi- and full-size filters at various flow rates and with controlled temperature and humidity, as well as an advanced analytical method for the measurement of TMS and HMDSO at the parts per trillion level (ppt, 10-12) in semiconductor applications. We can demonstrate that the configuration of chemical filter media can both cause and prevent the production and release of TMS from mixed media.

The two compounds co-exist in a chemical equilibrium, which is affected by the acidity and moisture of their environment. We will show

a) that HMDSO is converted to TMS by acidic media at concentrations typically found in cleanroom environments. This is contrary to published results that show a re-combination of TMS to HMDSO on acid media;

b) that this conversion is concentration dependent, potentially leading to the misinterpretation of laboratory test results, and

c) which configurations of filter media produce or prevent TMS formation.

We will also demonstrate that, based on its conversion to TMS, HMDSO is not a suitable test compound for hybrid chemical filter performance, as the apparent lifetime/capacity of the filter can be substantially skewed towards larger numbers when conversion to TMS is involved. We will show lifetime test results with toluene and HMDSO on acidic and non-acidic filter media.

Finally, even on purely carbon-based filter media, the lifetime performance of filters can yield differences between using HMDSO or toluene as a test agent, depending on the flow rate (linear speed) through the filters. We will illustrate how filter lifetime/capacity varies in different applications and flow regimes.

7638-111, Poster Session

Mask data rank and printability verification function of mask inspection system

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As the semiconductor technology node becomes minute, it approaches the limit to inspect the entire surface of a mask in the unique defect judgment algorithm without a pseudo defect. In addition, a nuisance defect including a pseudo defect increases by raising the defect detection sensitivity, and the review time after inspection increases. Mask total inspection time also increases and this will raise the mask inspection cost. Practical mask inspection can be conducted now by inputting the judgment level based on directions of design data there and by making a defect judgment level of every domestic area changeable. We can also shorten the review time by analyzing the printability on the wafer of the detected defect by the simulation, and by using the result for the defect judgment.

In this paper, we presented that the latest research and development results about mask data rank (MDR) function and printability verification(PRV) function. We verified the decrease of the number of pseudo defects by applying the defect judgment technology using MDR (pattern importance information) in the inspection of actual mask. We also evaluated the PRV function that is a computer simulated, virtual wafer lithography for the printability evaluation. Moreover, we verified that these technologies can enhance the efficiency of the defect judgment in the review process by applying them to the 199nm inspection system.

7638-112, Poster Session

Fast and precise measurements of the two-dimensional birefringence distribution in microlithographic lens materials

H. T. Katte, ilis gmbh (Germany)

Highly homogeneous glasses and crystalline materials such as CaF2 are used in high-end microlithographic applications. Residual stresses in the material lead to stress birefringence and thus to imaging errors, which is undesirable for semiconductor manufacture in view of the ever smaller structure sizes. Testing for residual stresses directly in the production process is therefore an important part of quality control and production optimization.

In many cases, testing is still performed visually using manually operated polariscopes or polarimeters. However, this type of measurement strongly depends upon the respective user and the results cannot be documented automatically. If demands on precision are high, automatic measuring systems which scan the test specimen are already in use. However, since the requirements on surface quality and ambient conditions are high, and the measuring speed is rather low because of the scanning mode of operation, such systems cannot always be used for 100% inspection.

In order to meet the increasing requirements regarding repeatability, lateral resolution and measuring speed, a new type of automated imaging polarimeters has been developed. The measuring apparatus applies the well-known Sénarmont method to determine the two-dimensional stress birefringence (magnitudes and axis orientations) within a large field of view (currently up to 320 mm diameter) and offering a high lateral resolution (up to 400 pixels/mm²).

By the use of high-quality optical components and sophisticated measuring algorithms, a RMS repeatability of better than ±0.005 nm optical retardation can be achieved. The lateral resolution of up to 0.05 mm makes it possible to make reliable statements not only regarding the average value (RMS), but also for the maximum and minimum values. In addition, the high resolution enables the detection of tiny flaws in the glass or crystal structure which become visible only through the stress halos generated by them.

The short measuring time of less than 60 seconds realizes a high sample throughput and makes it possible to analyze time- and

temperature-dependent alterations of the birefringence distribution or to analyze the specimen under different viewing angles.

The main application of the developed apparatuses is the inspection of fused silica, i-line glass and CaF2 crystals which are widely used as starting materials for wafer stepper lenses. Specimens larger than the field of view can be measured in multiple sections using a motorized x-y-table and a stitching algorithm to generate an overall, high-resolution stress birefringence map.

7638-113, Poster Session

Scanner qualification with IntenCD-based reticle error correction

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Scanner introduction into the fab production environment is a challenging task. An efficient evaluation of scanner performance matrices during factory acceptance test (FAT) and later on during site acceptance test (SAT) is crucial for minimizing the cycle time for pre and post production-start activities. If done effectively, the matrices of base line performance established during the SAT are used as a reference for scanner performance and fleet matching monitoring and maintenance in the fab environment.

Key elements which can influence the cycle time of the SAT, FAT and maintenance cycles are the imaging, process and mask characterizations involved with those cycles.

This paper will focus on the mask characterization aspects and suggest how initial and periodic aerial mask inspections with IntenCD can help in maintaining scanner performance and fleet matching with short cycle time.

Discrete mask measurement techniques are currently in use to create across-mask CDU maps. By subtracting these maps from their final wafer measurement CDU map counterparts, it is possible to assess the real scanner induced printed errors within certain limitations. The current discrete measurement methods are time consuming and some techniques also overlook mask based effects other than line width variations, such as transmission and phase variations, all of which influence the final printed CD variability.

Applied Materials Aera2 mask inspection tool with IntenCD technology can scan the mask at high speed, offer full mask coverage and accurate assessment of all masks induced source of errors simultaneously, making it beneficial for scanner qualifications, performance monitoring and fleet matching maintenance.

In this paper we report on a study that was done to improve a scanner introduction and qualification process using the IntenCD application to map the mask induced CD non uniformity. We will present the results and discuss the benefits of the new method.

7638-114, Poster Session

Resist-based polarization metrology with phase-shift masks at 1.35 numerical aperture: tool-to-tool comparison

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This paper will provide an across slit and a tool-to-tool comparison at numerical apertures up to 1.35 of a previously introduced resist-based polarization monitoring technique1,2. Previous publications have provided single tool monitoring over time, generally in the center of the imaging slit. This paper will provide the first comparison among imaging tools and a comparison with on-board metrology. This technique involves the analysis of resist images printed with a specialized, multiple phase-shift, test reticle that employs an array of pinhole apertures in an opaque layer on the backside of the reticle. Calibration of the reticle is required to account for the inevitable imperfections from the mask fabrication process and enables measurement of the Stokes parameters of any illumination configuration.

Experimental results across slit will be discussed from a third-generation test reticle designed to measure polarization at numerical apertures from 0.8 to 1.35. As an example, Figure 1a shows resist images printed with highly off-axis illumination and a set of chromeless phase-shift mask patterns. Figure 1b is evidence that the intensity at the center of the resist is very sensitive to the incident polarization state, showing a 3 to 4x difference in dose required to print the image center. Multiple patterns are analyzed within an illuminator pupil-fill, allowing for an understanding of the across-pupil polarization behavior. Figure 2 shows a comparison of the intensity in the preferred polarization state between two tools, as measured by on-board metrology. Ability of the resist based technique to replicate this prediction will be shown.

To achieve this measurement accuracy in practice, various issues will be addressed to include the mask manufacturing capabilities and status, test reticle design, calibration and measurement procedure, metrology requirements and capabilities, and methods to reduce metrology time requirements and reduce experimental error. The impact of and methods to overcome various non-idealities such as mask making limitations, resist stack variations, projection lens polarization aberrations, and metrology imperfections will be addressed.

[1] G. McIntyre and A. Neureuther, “Monitoring Polarization and High-NA at 193nm and Immersion with Phase Shifting Masks,” Proc. SPIE, vol. 5754, pp. 80-91, 2005.

[2] G. McIntyre and R. Tu, “Monitoring polarization at 193nm high-numerical aperture with phase shift masks: experimental results and industrial outlook,” Proc. SPIE, vol 6924, 2008.

7638-116, Poster Session

Roadmap for traceable calibration of a 5-nm pitch length standard

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Production of objects with 5 to 25 nm width or pitch requires metrology with picometer-scale accuracy. The foundation for routine metrology using microscopes is provided by transfer standards such as 1-D or 2-D gratings whose pitch is used to calibrate the microscope’s magnification. Traceability is most useful when the expanded uncertainty (k=2, 95% confidence) is better than +- 2% for single pitch values and +- 0.5% for mean pitch.

High-quality, general purpose SEMs and AFMs are capable of providing metrology at this level when operated with care and when the images are analyzed properly. In a typical measurement run, one makes images of an appropriate magnification calibration specimen along with the test samples. The resulting images are then analyzed offline with purpose-built calibration and measurement software. When these procedures were applied to measure individual pitch values of the calibration specimens themselves, the relative pitch variation (standard deviation/average pitch) was < 0.5% for 7 different specimens whose pitch values cover 3 orders of magnitude (from 2000 down to 35 nm). Such measurements demonstrate the basic performance of the calibration standards, the microscope and the method itself.

We have previously shown that the method is not only precise, it is also accurate. A 144-nm pitch 2D grating was measured by optical diffraction at PTB, the national standards lab of Germany, and by AFM in our lab. The average pitch values agreed within 0.023% (or 33 pm). This value was less than our uncertainty due to random effects, indicating that unknown effects that might cause bias were small.
[1] We now present a metrology roadmap that applies the SEM and AFM methods to measure patterns down to 5 nm pitch. This roadmap assumes a chain of 5 comparisons to transfer calibration from the 144 nm standard to a hypothetical 5-nm pitch standard. At each step in

the chain, one would capture a data set consisting of multiple images of the current and new standards. The measured data include 300 independent pitch measurements of the new standard. We assume that the relative standard deviation of single pitch measurements is 0.5%. This random variation contributes 0.03% (1 sd) to the uncertainty of the new standard's mean pitch value. Additional error components include the uncertainty of the current standard's mean value and various instrumental factors. After 5 calibration transfers, we expect that the uncertainty of the 5-nm pitch standard will be 8 pm (1 sd) for the mean value and 26 pm (1 sd) for single values. These uncertainties easily meet the target given above (1 sd=12.5 and 50 pm, respectively).

Recently we have completed the first step in this chain, providing traceable calibration of a 70-nm pitch standard. The relative standard deviation for single pitch values was 200 pm (0.3%), leading to uncertainties (1 sd) of 17 pm for the mean value and 212 pm for single values. These results are better than required by the roadmap.

1. Donald A. Chernoff, Egbert Buhr, David L. Burkhead, and Alexander Diener, "Picometer-scale accuracy in pitch metrology by optical diffraction and atomic force microscopy", Proc. SPIE 6922, 69223J (2008)

7638-117, Poster Session

Advanced 3D lithometrology with the crosstalk eliminated (XE) atomic force microscopy

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With continuous feature size reduction in the lithography process, Atomic Force Microscope (AFM) has been widely used to measure and characterize the surface of a sample in nanometer scale. In the first generation AFM based on piezoelectric tube scanners, the scanner movements are coupled in such a way that an extension in the XY plane will directly influence the scanner's position and sensitivity in Z, varying from different centre positions of a scan and respective scan speeds. Therefore, it suffers from poor repeatability and inaccuracy due to the inherent background curvature as a result of the crosstalk between the x-y-z axes, making it inadequate for quantitative metrology. One of the latest advancements in AFM industry has been the elimination of this cross-talk (XE) in the XY scan. Here, the XY flexure scanner, driving a sample, is decoupled from the Z scanner to which a probe is attached. The new AFM platform has a highly orthogonal and ultra flat scan. These key attributes of the new AFM is central to the accurate and reproducible measurements of the critical dimensions.

Building upon the strength of its platform, the new AFM added a ground-breaking capability of non-contact AFM in ambient atmosphere by adopting the high speed Z scanner, actuated by dedicated high force piezostacks, with minimized drive mass, hence gaining much higher Z-scan bandwidth and a faster Z-servo response than a conventional tube scanner. The new non-contact AFM enables an ideal methodology to characterize soft materials surface of photoresists.

In overcoming the limitation of the vertical wall imaging by a flared tip, the design concept of the second generation AFM was utilized to measure under-cut structures by intentionally changing the angle of the Z scanner, enabling sidewall roughness characterization in nanoscale for the first time. Combined with non-contact AFM imaging, the new 3D AFM provides the ideal method to measure the sidewall roughness of soft materials such as photoresists.

7638-118, Poster Session

Reconstruct FinFET cross section using CD-SAXS

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In order to meet future challenges of performance including speed, thermal and power efficiency of sub 32nm technology node and beyond, transistor architecture is migrating from a planar to non-planar structures, for example, a Tri-Gate or FinFET type architecture. In FinFET type transistors top rounding and undercut are expected to affect their performance. Critical dimension small angle x-ray scattering (CD-SAXS) has been applied successfully to measure high-k dielectric thickness of a few nanometers. In this work its capability to quantify 3D non-planar structure is further exploited with an objective to quantify top rounding and undercut in FinFETs. The scattering characteristics in the Qx-Qz map attributed to top rounding and undercut will be numerically analyzed followed by quantitative fitting of the experimental Qx-Qz data. The fitted CD-SAXS results will be compared with those obtained from high resolution cross sectional transmission electron microscopy (X-TEM).

7638-119, Poster Session

Characterizing physical structures of irregular shaped patterns utilizing x-ray reflectivity as a pattern shape metrology

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Specular X-ray reflectivity (SXR) is a powerful methodology to quantify the complete cross section of periodic, nanoscale line and space patterns with complimentary use of critical dimension-small angle X-ray scattering. To utilize SXR as a pattern metrology, the coherence length of incident X-ray beam should be greater than the characteristic dimensions of the pattern structures being investigated. In this limit the effective medium approximation holds and the X-rays measure an average density, averaged over both the lines and spaces, for the patterned region. Since the effective density is reduced proportionally by volume fraction defined by the line-to-space ratio, the line-to-space ratio can be deduced as a function of pattern height by fit SXR data with a multilayer recursive model. Previous studies on periodic patterns showed that this SXR metrology is applicable for patterns with periodicities as large as 25 μm, when the incident X-rays are perpendicular to the grating axis.

Here we extend this study to the characterization aperiodic or irregular patterns that would be more representative of the large patterned areas in various devices. Diblock copolymer (di-BCP) films are used as a model system to create random two dimensional patterns without long range order. A di-BCP consists of two different linear polymers covalently connected at a single junction into a single chain molecule. When the two blocks are symmetric in their length but dissimilar chemical composition, the material will self assemble into a lamellar structure with alternating layers of the two blocks. One of the blocks usually has a stronger preference to wet the surface of a silicon wafer, resulting in the lamella being parallel to the surface in a thin film structure. This preferred orientation causes a quantization of the film height to (n + 1/2) Lo, where Lo is the bulk value of the copolymer lamellar period and n is an integer. The layer at the free surface of the film only forms a smooth film if the volume of the material in the film is commensurate with a uniformly flat surface. If it is incommensurate the top layer becomes terraced with either discrete islands, a bicontinuous structure, or holes with the integral height of Lo. In this presentation we extend the applicability of SXR to the symmetric diblock copolymer thin films with various irregular shaped terraces to determine the terrace shape and the ordered lamellar structures. Symmetric di-BCP films of poly(styrene-b-methyl methacrylate) (PS-b-PMMA) are spun cast onto smooth Si substrates annealed at elevated temperature where they self-assemble into their striated lamellar structures. Terrace structures are controlled by changing the initial film thickness of di-BCP through varying the concentration of di-BCP solution and spin speed during coating films. SXR is used to characterize the density profiles as a

function of height of the discrete surface layer. By comparing the structural characteristics from SXR with AFM images of the in-plane surface morphology, we conclude that SXR can be a powerful tool for characterizing the shape profile of irregular as well as periodic patterns.

7638-120, Poster Session

Proximity effects correction for sub-10-nm patterning node

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Electron Beam Direct Writing (EBDW) has been extensively used in various applications such as prototyping or small volume production of electronic devices. It was suffering from proximity effects which, originally, were considered as a presence of the background energy difference caused by the pattern density distribution. However, when the critical dimensions of target patterns are getting smaller, we cannot ignore the influence of the forward scattering. Indeed, when the critical dimension is close to 2 times of forward scattering range, its influence must be taken care of. In case of fabricating of sub-10 nm pattern dimensions by Nano Imprint Lithography (NIL) proximity effects correction system which considers forward scattering is of utmost importance. This is mostly because it requires the original dimension (1:1) molds.

We have developed simulation-based proximity effects correction system combined with data format conversion which works in Linux PC cluster environment.

Usually, 2-Gaussian approximation of Energy Intensity Distribution (EID) function has been used to simulate energy deposition. In contrast to that, our system is able to carry out EID function convolution without Gaussian approximation in reasonable time, which is necessary to assign optimum dose for each element of the pattern. This means precise simulation method which considers energy distribution of complete scattering effects.

In this communication, we will report on our experimental results with emphasis on the application of Direct Monte Carlo Convolution. Successful sub-10nm patterning with dimension controllability better than 10% of the CD was achieved. Experimental setup use JBX-9300FS (100keV acc. Voltage) as exposure tool, HSQ (FOx-12) as resist with EID function being calculated by CHARIOT.

7638-121, Poster Session

High-brightness EUV light source performance for EUV interferometer and microscopy

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EUV interference lithography is powerful for the evaluation of EUV resist in the 22 nm node and below. The coherence, divergence and spectral characteristics of the light emitted by a high brightness EUV source are presented. This source is based on a hollow cathode triggered micro plasma pulsed discharge, with an intrinsic photon collector, the i-SoCoMo. The discharge was operated at 20-25 kV, using a gas mixture of Helium, Argon and Xenon. A full description of the source and its operating parameters is described elsewhere [1]. The input electrical energy is approximately 0.5 J; producing a light pulse of 10 ns with an in-band EUV output energy of about 100 µJ. A monochromator consisting of two multilayer mirrors was located along the light emitted beam and was used to select the emitted spectra at a wavelength of 13.6 nm with a bandwidth of 2 nm.

The experimental setup used to investigate the optical coherence of the source, consisted of a capillary source aligned with a pinhole followed by two slits located on a plane behind the pinhole. All components were held in vacuum and kept at the same pressure as the discharge. The interference produced by these two apertures was recorded on a CCD camera, which allowed an analysis of the image. In addition a transmission grating with an 80nm period will be incorporated into the system where the results of the printing of structures onto a mask will be presented. This is a technology demonstration although other printing pitch requirements can be fitted as required. On this demo, it will have a manual motion control for a 200mm wafer. A set of experiments were done varying the parameters of the optical setup (pinhole size, apertures dimensions and relative distance between them) as well as the operated regime of the discharge, in order to study the different plasma regimes of the discharge and its relation with the characteristics of the emitted beam. A second series of experiments were carried out in order to investigate the characteristics of the emitted spectra of the source when a single pinhole was used as a spatial filter. A single grazing incidence spectrometer was located after the pinhole and the spectra were also recorded on a CCD camera. A conclusion of the experiments will be presented and its relation in the use of the discharge for different applications, such as soft EUV microscopy and particularly in the field of metrology where highly coherent and monochromatic sources are required. Due to the very low etendue and the compact form factor of the i-SoCoMo source, the higher irradiance for aerial imaging microscope requirements can be obtained by spatial multiplexing of multiple units, the HYDRA design.

[1] P. Choi, S. Zakharov, R. Aliaga-Rossel, Y. An, C. Dumitrescu, C. Leblanc, O. Sarroukh, V. Zakharov, Proceeding website, EUVL Symposium, Barcelona, Spain, Oct 15-18 (2006).

7638-122, Poster Session

Metrology qualification of EUV resists

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The main topic of this paper is the examination of the measured pattern roughness (LWR/LER) contributed by measurement (SEM), exposure (EUV exposure tool) and the resists itself. The authors also examined suspected metrology SEM challenges on different EUV resist types exposed by one of the EUV demo tools. Standard CD SEM tests, such as precision and shrinkage were performed in order to get best working conditions. As part of the research, special attention was given to expected electron - material interactions, such as resist's slimming, low contrast and contamination build up on both lines and contact holes. LWR, LER and CER were analyzed in order to determine separately the contribution effect of the exposure tool and the different resists.

7638-124, Poster Session

Error analysis of absolute testing based on even-odd functions method

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Recently most of modern absolute measurement rotation the flats or sphere in the interferometer. In the high accuracy interferometer system the more errors are removed the more accuracy we can get. So it is very important to exactly know how some errors such as angle rotation error, center excursion error, environment error, vibration error influence the metrology. This paper analyses the influence of coordinate direction motion errors and gives the improved arithmetic to improve the measurement accuracy. High accuracy interferometeric surface metrology is constantly gaining importance, not only in the classical area of optical fabrication, but also for new applications, such as semiconductor wafer flatness or lithography lens. Requirements for measurement resolution in the sub-nanometer range have become quite common. In the lithography system, we will use more precision lens to satisfy the shorter and shorter lithography wavelength. Before

this we need more precision testing technology to satisfy the need of fabrication and integration. It is frequently the case in interferometric optical testing that the required uncertainty in the measurement is of the same order as the systematic errors, including the reference surface, of the instrument to be used. Absolute testing method can improve the precision of the interferometer through removing the system errors. We review traditional absolute testing of flats methods and emphasize the method of even and odd functions. The flat can be expressed as the sum of even-odd, odd-even, even-even and odd-odd functions. Through six measurements the profile of the flat can be calculated. In theory, if the flats and the environment remain unchanged during the multiple measurements, the two corresponding measurements should have no difference. This difference represents the measurement reproducibility error, which is mainly due to the changes in the environment during the long period of measurements and the changes of the surfaces during the rotation manipulation. We can put the measurement systems in the space full of to reduce the temperature and the air fluctuate influence. The temperature and vibration errors can be reduced through the common-path interferometer. But to the modern absolute testing technology, it always contains the rotation. The rotation of the lens can lead to some errors such as angle rotation error, center excursion error and other coordinate system motion error. If we can test these errors from the detector, the error can be reduced from the improved arithmetic. Then the accuracy of the systems can be enhanced by remove these errors. We analyze the errors by using Zernike polynomial. The flat or sphere can be expressed as Zernike polynomial which can also be divided into even-odd, odd-even, even-even and odd-odd functions. We can use 36 Zernike polynomials to generate 3 plats A, B, C. Then the six measurements can be generated from the three plats. For the angle rotation error, we can simulate the angle error distribution and substitute in the systems. Then the influence of the angle rotation error can be analyzed. According the error distribution we can change the arithmetic to improve the measurement accuracy. The results of errors analysis by means of Matlab are shown that we can through change the arithmetic according the coordinate direction motion errors which can be detected to improve the accuracy. The errors analysis can also be used in other interferometer systems which have the motion of the coordinate system.

7638-125, Poster Session

Detection of photoresist residue on high-K metal gate layers using optical scattering and advanced analysis techniques

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As CMOS scaling continues below 45nm, conventional SiO_2 cannot sustain equivalent oxide thickness (EOT) and leakage current requirements set in the International Technology Roadmap for Semiconductors (ITRS). Due to the limitation of physical thickness scaling and high tunneling current, next-generation CMOS devices require the introduction of high-K and metal gate electrodes to reduce gate leakage and poly depletion.

The manufacturing infrastructure for high-k and metal gate stacks is reasonably mature. On the reliability front, however, much work remains to be done. Dual metal gate CMOS integration steps require multiple wet etch process steps to separate two different metal gates within transistors on the same wafer. Integration schemes as well as wet etch chemistries must be developed to completely remove the first metal gate material without damaging the underlying gate dielectric. Photo resist material specific for High K/Metal Gate (HK/MG) layers must be chosen carefully and effective resist strip processes have to be developed and extensively characterized as incomplete removal of the photo resist leads to the presence of residue.

Detection of such resist residue after Cap2 resist cleaning step is critical as it has been known to impact yield and affect device performance. This residue, when exposed to subsequent thermal process steps, transforms into solid hard spot(s), and can then be detected by an inspection tool, but this is unfortunately too late. A unique & innovative process control solution was developed to detect the presence of residue. This solution used a simple litho checkerboard technique, Surfscan SP2 wafer inspection tool which can measure the optical scattering from the surface of the wafer & SURFmonitor (A Process Signature & Metrology Proxy add-on module for SP2). In this study, the litho checkerboard technique involved creating wafers where some of the regions of the wafer were left un-exposed and some regions were exposed with a line space pattern. These wafers were then inspected on the above mentioned optical scattering tool and the data was analyzed using techniques such as SURFimage Overlay Differential Analysis (SODA) and Regions of Interest (ROI) analysis. The result of this analysis indicated the presence of residues on the exposed and un-exposed regions of the wafers.

Thickness measurements conducted by an Optical Film Metrology tool validated the results. The thickness measurements indicated that the film thickness was noticeably higher than the expected thickness in certain areas even after photo resist strip and wash. These were exactly the same regions identified by above analysis as having resist residue. This unique process control solution provides superior sensitivity, quicker time to results and significant cost benefits. Although this study was conducted on a set of epitaxial test wafers, this solution can be easily implemented in a typical production process flow for <45nm design rule HK/MG manufacturing process.

7638-126, Poster Session

Making polarization-neutral high-NA DUV objective lenses for inspection: a case study

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With shrinking design rules optical defect inspection on semiconductor devices becomes more and more challenging. It was shown [1], that using polarized light will help to increase signal-to-noise ratio for defects in lines-and-spaces structures.

Because of the limited number of materials for lenses and coatings which can be used to manufacture optical devices for the deep UV making a nearly polarization-neutral high-NA lens is a serious technological challenge.

In the paper we present a theoretical analysis for a number of different options to influence the coating properties which will lead to more polarization-neutral lenses. Also, an assessment for the practical manufacturability of the different options will be given.

[1] B.-H. Lee et al., Proc. SPIE, Vol. 6152, 61521Q (2006); DOI:10.1117/12.656004

7638-127, Poster Session

AMC control in photolithography: the past decade in review

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The focus of airborne molecular contamination control within the semiconductor industry, specifically photolithography, has changed significantly over the past decade. As the focal point of concern has shifted from ammonia (or base gases), to acid gases, and recently to organic contaminants, the filtration industry has adeptly grown in order to provide the necessary filtration solution. This paper attempts to provide an overview of these changes while reviewing the primary contaminants, how they are removed, the control technologies in use, and how they are applied.

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7638-128, Poster Session

CD bias reduction in CD-SEM of very small line patterns: sidewall shape measurement using model-based library matching method

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Critical-dimension scanning electron microscopy (CD-SEM) is commonly used to measure critical dimensions (CDs) when developing and manufacturing semiconductor devices. However, conventional CD-SEM measurements may contain a measurement bias (defined as the difference between the measured CD and the actual CD). To complicate matters, this measurement bias is not constant, but rather varies with variations in the pattern profile, such as the sidewall shape. To reduce this variation in the measurement bias, the measurement algorithm should account for the effect of the pattern profile on a SEM image.

The model-based library (MBL) method, which was originally developed at the National Institute of Standards and Technology, is anticipated to solve this problem. The MBL method employs a physically based mathematical model to describe the SEM waveform generation process. It compares a CD-SEM waveform with a library of simulated waveforms and estimates the pattern profile and tool parameters.

The purpose of this study is to reduce the bias variations, especially for extremely small patterns that have an MPU gate length of <13 nm at the 32-nm node and beyond. We modified the MBL method to accurately estimate pattern profiles.

A peculiar difficulty associated with measurements of extremely small patterns by the MBL method is that many solutions can exist in its parameter space, which consists of pattern profile parameters and tool parameters. Thus, it is a multiple-solution problem. This problem occurs because the pattern profile information is degraded in a small pattern due to interference between the secondary electron signals from the left and right edges. A typical example of interference is the merging of left and right waveform peaks. This interference must be considered when the MBL method is applied to extremely small patterns; however, it is not taken in account in conventional MBL.

To overcome the problem of multiple solutions, we propose:

1) Modifying the simulation model by including the concepts of line width and line pitch in the library.

2) Reducing the number of parameters that need to be estimated by deciding the tool parameters in advance.

We used simulated SEM images generated by a Monte Carlo simulation to demonstrate that the modified MBL method improves the measurement precision of the sidewall shape and reduces the bias. These effects are verified by applying the MBL method to actual SEM images of a sample. The pattern profiles estimated by the MBL method agreed well with the pattern profiles of cross-sections measured by atomic force microscopy and scanning transmission electron microscopy.

7638-129, Poster Session

Evaluating CD-SEM performance from the contrast transfer function

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The performance of a CD-SEM is usually described in terms of a single number - its 'resolution' - but this is of little or no help when attempting to evaluate the quality of an instrument and how it compares with other similar tools. The scanning electron microscope pixelates, processes, and then displays, a data stream to provide the images that are ultimately viewed. Such a process is considered and analyzed most appropriately as being the transfer of a digitized signal though a band-pass filter whose characteristics are described by a characteristic Fourier response. This response, here called the contrast transfer function (CTF) of the tool, plots the relative efficiency of transferring spatial frequency information as a function of the spatial frequency. The CTF can be derived from a single image of a suitable target, ideal examples being specially fabricated structures such as a nanoscale Fresnel lens or a pseudo-random arrays, or films of sub-nanometer particles such as Iridium deposited on to substrates such as clean silicon. High resolution images of these materials give a Fourier spectrum which is sensibly constant across a wide range of spatial frequencies (millimeters to sub-nanometer) so any deviations from this ideal behavior that are displayed by the CTF are evidence of performance short-falls at one or more points in the imaging chain.

An analysis of the CTF can therefore provide much quantitative data including:

(a) a measurement of the spatial frequency at which signal content becomes indistinguishable from noise. This is the true ultimate resolution limit of the tool and this measurement can immediately be extended to predict the variation in resolution as a function of signal to noise (i.e. beam current and scan time).

(b) evidence of the effect on performance of operational choices such as accuracy of focus and the choice of beam limiting aperture, by comparing experimental and simulated CTF plots

(c) a diagnostic for stage drift, and sample and beam instabilities, with nanometer sensitivity

Finally the CTF contains the information needed for the 'apodization' of the SEM image so as to remove the image ringing and edge artifacts induced by the band limited behavior of the SEM. These artifacts represent a fundamental impediment to the application of the CD-SEM at the nanoscale and the ability to numerically reduce or remove such effects would enhance the utility of the tool for nano-metrology tasks such as the measurement of the size and shape of nanoscale particles.

7638-130, Poster Session

CD uniformity correction on 45-nm technology non-volatile memory

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For the next years optical lithography stays at 193nm with a numerical aperture of 1.35. Mask design becomes more complex, mask and lithography specification tighten and process control becomes more important than ever. Accurate process control is a key factor to success to maintain a high yield in chip production.

One of the key parameters necessary to assure a good and reliable functionality of any integrated circuit is the CDU (Critical Dimension Uniformity).

There are different contributors which impact the total CDU: scanner repeatability, resist process, lens fingerprint, wafer topography, mask error factor, mask CD uniformity etc.

In this work we focus on improvement of intrafield CDU at wafer level by improving the mask CD signature using a CDC200 tool from Zeiss Pixer Technology.

The mask layout used is a line and space dark level of a NVM (Non Volatile Memory) for the 45 nm node. The full area of the reticle includes 12 identical devices and 3 test patterns of the same technology. The CD target on wafer of 51 nm line with a CDU 3sigma of 2.0 nm is lithographically reached using an ASML XT 1700i exposure tool with off-axis illumination (polarized dipole).

A prerequisite to improve intrafield CDU at wafer level is to characterize the mask CD signature precisely. For CD measurement on mask the newly developed wafer level CD metrology tool WLCD32 of Carl Zeiss SMS was used. The WLCD32 measures CD based on aerial imaging technology. All relevant scanner illumination schemes can be applied. The WLCD32 captures OPC and optical MEEF effects already on the mask and is therefore a perfect tool to provide the input for the CDU correction.

The WLCD32 measurement data show an excellent correlation to wafer CD data. For CDU correction the CDC200 tool is used. By utilizing an ultrafast femtosecond laser the CDC200 writes intra-volume shading elements (Shade-In Elements) inside the bulk of the mask. The laser writing is done through the backside of the mask with the mask pattern and pellicle faced down. By adjusting the density of the shading elements, the light transmission through the mask is locally changed in a manner that improves wafer CDU when the corrected mask is printed. The CDU map measured by WLCD32 is converted into an attenuation map and processed by the CDC200TM.

The mask CDU improvement after CDC correction is measured with WLCD32.

In the present work we will demonstrate a closed loop process of WLCD32 and CDC200 to improve mask CD signature as one of the main contributors to intrafield wafer CDU. Additionally we will emphasize the capability of CDC200 to improve intrafield CDU.

7638-132, Poster Session

Overlay breakdown methodology on immersion scanner

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In the last years a flourishing number of techniques such avec High Order Control or mappers have been proposed to improve overlay control. However a sustainable improvement requires sometimes to understand the underlying causes of the overlay limiting factors in order to remove them when possible or at least to keep them under control. Root cause finding for overlay error is a tough task due the very high number of influencing parameters and the interaction of the usage conditions.

This paper presents a breakdown methodology to deal with this complexity and to find the contributors of overlay error. We use a Partial Least Squares (PLS) algorithm to isolate the key contributors for correctable terms and a field-to-field linear regression technique to highlight the main causes of residuals. We present a study carried out on 45nm CMOS contact-gate overlay over 687 production wafers exposed in an ASML XT1700i Immersion scanner. We deliver the results of the correlations with the 180 process and equipment variables used for this study. For each isolated contributor we propose an explanation of the underlying physical phenomenon and solutions.

7638-133, Poster Session

Electrical effects of corner Serif OPC

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Today's Optical Proximity Correction (OPC) is becoming increasingly complex and necessitates using smaller and smaller grid sizes to produce the fine patterns required. These small grids lead to very high overhead in data handling, as well as for the tools that will write and inspect the mask; which together make masks extremely expensive. For two dimensional structures such as corners, we use complex structures incorporating either additive or subtractive OPC features to produce the desired shape. In previous work we showed that polysilicon corner structures were electrically very sensitive to the size of the corner serif on the inner corner of the feature, but relatively insensitive to the size and position of the serif on the outer corner. However, technology is moving forward and polysilicon gates are being replaced by metal gates for 32nm node. In this work we replace the polysilicon with a metal and investigate the size and position of OPC applied to both the outer and inner corners of the structures. The electrical effect of OPC on the outer corner was found to be minimal, whereas the inner corner shape had a significant effect upon the electrical resistance of the circuit feature. The data suggests for metal structures similarly to polysilicon, that OPC on the outside corner has little impact upon a simple circuit's performance, but care should be taken with OPC on the inner corners, particularly with regard to the size of the OPC serifs used.

7638-134, Poster Session

Automatic measurement of electro-beam size using BEAMETR chip and software

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Monitoring and tuning the beam size is critical for any electron-beam system. The performance of defect inspection systems, electron beam lithography (EBL) systems and scanning electron microscopes (SEM) depends greatly on beam size. The knife edge method usually used for beam size measurement is time consuming and inaccurate; the results are operator dependent. Analytical methods based on Fourier transform analysis were developed [1] which showed that the measurement can be done in a more precise way. Still, an operator had to determine the beam size out of the spectral data, which can involve an operator dependent error. The first results on BEAMETR technique which use spatial spectral measurement for automatic beam size measurement were reported in our previous works [2,3].

In this paper, BEAMETR technique was further developed to allow for robust operator independent measurement of electron beam sizes in two coordinates. BEAMETR involves software and a specific pattern design. In the developed method, the pattern is scanned using an electron beam. A spatial spectrum of the signal is analyzed in few seconds using a software program and beam size is automatically determined. The technique is independent of operator's decision. This allows for non-subjective comparison of system tuning and performance, as well as comparison of different e-beam systems.

Results of design, fabrication and analysis of the BEAMETR test pattern are presented. A specially designed and fabricated test pattern is used with the known spectral characteristic. Special attention was given to optimizing the size and shape of a pattern, so that the high resolution of the method does not require a large number of pixels in SEM image. 100 KeV electron beam lithography and metal electroplating is used to fabricate BEAMETR pattern. Proximity correction was applied to improve pattern quality. An example of electron beam size and shape measurement is presented in Figure 1. We will present a comparison of electron beam shapes and sizes for different SEM tools.

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7638-136, Poster Session

Application of analytic SEM to CD metrology at nanometer scale

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Critical dimension metrology is the most needed feedback in nanofabrication. SEM based methods are most commonly used because images of features are readily available. Analytical SEMs are not optimized for the task of quantitative metrology; nevertheless this is the only tool available to most companies at R&D stage. The dimensional measurements from SEMs consist of two steps, the first being image acquisition and the second being the algorithm treatment on the generated intensity profile for the dimension determination. However, SEM metrology involves uncertainty of the measurement in

the signal processing step. This is because the SEM signal formation is an extremely complex process depending on the pattern geometry, materials, detector setup, and beam voltage; so the image brightness profile is of complex relationship to the feature shape.

In this work, we used an analytical SEM for CD metrology applications on quartz nanoimprint template. The SEM was tuned first to find the best reasonable condition for consistent manual operation. Beam characterization was done using BEAMETR beam measurement technique. SEM images were taken at optimum conditions. The measurements were done using a) regular imaging processing software and b) using physical model based processing tool myCD. The quartz template was then measured using TEM crossections at selected sites to reveal profile information as metrology comparison reference. Through our exercise, the metrology capability and fundamental limitation of analytical SEM operation with regular imaging processing was identified. The considerable improvement was found with physics based imaging processing that involves SEM setup along with material information. We concluded that physics based image analysis resulted in data almost identical to the TEM references.

7638-137, Poster Session

A paradigm shift in scatterometry based metrology solution addressing the most stringent needs of today as well as future lithography

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Advanced lithography is becoming increasingly demanding when speed and sophistication in communication between litho and metrology (feedback control) are most crucial. Overall requirements are so extreme that all measures must be taken in order to meet them. This is directly driving the metrology resolution, precision and matching needs in to deep sub-nanometer level as well as driving the need for higher sampling (throughput).

Keeping the above in mind, a new scatterometry-based platform is under development at ASML. Authors have already published results of a thorough investigation of this promising new metrology technique which showed excellent results on resolution, precision and matching for overlay, as well as basic and advanced capabilities for CD. In this technical presentation the authors will report the newest results from this ASML platform. This new work is divided in two sections: monitor wafer applications and product wafer applications.

Under the monitor wafer application: overlay, CD and focus applications will be discussed for scanner and track hotplate control.

Under the product wafer application: first results from integrated metrology will be reported followed by 3D CD reconstruction results from hole layers as well as overlay-results comparison between programmed overlay values (programmed on the scanner) and measured overlay by this new technology will be discussed. Also reported are a thorough target-to-target matching and tool-to-tool matching data using an advanced analysis method called “similarity index”. Results from standard-size targets as well as small, process-robust overlay target results are reported. A complete front-end (FEOL) and back-end (BEOL) layer measurement strategy that minimizes the scribe-line consumption will be discussed. Finally, fab application and integration of this new technology will be discussed along with some early results from focus-dose control activity.

7638-138, Poster Session

Investigation of periodical microstructures using coherent radiation

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Low-cost effective characterization methodology was developed that allows indirect evaluation of mechanical, geometrical and optical parameters of periodical microstructures in the cases when traditional measurement techniques are not suitable. Proposed methods are applicable for optimization and control of technological processes.

Laser diffractometer is used in the experimental works for measurement of optical parameters of periodical microstructure and estimation of geometrical parameters with an error of less than 5% by comparing theoretical and experimental values of diffraction efficiencies of periodical microstructures. This method is suitable for geometry control of periodical microstructures during all technological process.

Also an efficient method was developed that is capable to estimate with an error of 5% the depth of periodical microstructures, which have characteristic depths that are larger than the wavelength of coherent light used in the experiment.

Quality of periodical microstructures is sensitive to thermal conditions during replication process. Therefore an experimental setup based on Michelson interferometer was developed for the investigation of induced thermal deformation. The radius and stress kinetics could be analyzed for different thickness of coated polymer.

These are the problems that are considered in this paper.

7638-139, Poster Session

Predictive chrome-film haze mask management for mass production

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This study enable us to setup a strategy for “predictive” management for chrome-film haze phenomenon. We define “Chrome-Film Haze”, as an invisible film residing on the chrome surface. This type of Haze may be poised as a “silent killer” because it cannot be seen by naked eyes, nor can be easily detected by our inline inspection tool. Over a period of time with increased exposition activity, this “invisible” chrome-film haze will eventually block its transmission at chrome-side, thus causing its dosage trending on one direction & its intra-field corners/centre CD drifting. This type of “haze” if not properly managed, especially on a “Darkfield Low-Transmission” mask (i.e..Contact)... can cause “Contact Bridging” as a matter of time, resulting catastrophe yield loss on thousands of wafers, in a mass production FAB environment. Therefore, understanding chrome-film haze phenomenon, will help us to deploy a more effective mask management control strategy, in order to prevent this kind of haze occurrence impacting on wafers’ yield loss. In addition, being able to predict its next haze occurrence, would allow better planning & WIP management, so that we can minimise interruption to production due to reticle being sent for repel, as a result of chrome-film haze. (Especially for certain mass production scenario where backup mask may not be available.)

7638-140, Poster Session

First results from a novel EUV mask inspection system

S. Mangan, A. Sagiv, Applied Materials (Israel)

The semiconductor industry recently converged on EUV lithography as the most promising candidate to replace ArF for the 22nm node and beyond. Whereas in the realms of EUV scanner technology and EUV source a significant progress was made, that puts EUVL as a viable solution, the issues related to EUV mask defectivity and inspection remained practically unanswered. This gap posits EUV masks as the leading risk to the entire technology, and requires a robust solution already during the introduction phase of EUVL. In this paper we present first results from a novel EUV mask inspection system. We demonstrate pattern image formation, and consider detection of various defect types that represent realistic mask defectivity scenarios.

7638-141, Poster Session

Study of the prospects and limitations of EUV mask inspection by DUV inspection system

A. Sagiv, S. Mangan, Applied Materials (Israel)

Recent assessments of the remaining gaps in the EUV roadmap posit EUV mask defectivity and related infrastructure as the leading risk to EUVL technology. The short EUV wavelength translates into extremely stringent constraints on both absorber pattern and multilayer stack, which in turn translate into a significant mask inspection challenge. The inspectability demand for the early introduction and learning phase over the 22nm half-pitch node may only be answered by extending present DUV solutions. This paper examines defect detection prospects and inherent limitations, by means of both numerical simulations and analytic calculations. Special attention is paid to signal maximization using various possible manipulation of the DUV optical setup. The results indicate that extended existing DUV solutions may serve effectively as a bridging solution until the introduction of the currently lacking EUV-dedicated solutions.

7638-142, Poster Session

SI-traceable calibration of line-width roughness of 25-nm NanoCD standard

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SI-traceable 3DAFM was used to characterize 25 nm NanoCD standards. The standard has a uniquely low LWR and can be used as a benchmark during development of advanced patterning technologies. The following results were obtained: (a) Mean LWR for two standards with uncertainty ±0.02 nm (0.95 CL). The LWR is below 0.7 nm (1s). (b) Distribution of LWR and LW at 3 heights (20, 50 and 80% from the line top) along 3 mm segment of standard. Variations are below 0.25 nm and 0.07 nm (1s) for LW and LWR, respectively. (c) Spatial power spectra of LWR of the standards.

7638-34, Session 8

Grazing incident x-ray scattering for characterizing nanopatterns on flat substrate

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Over the past few years the number of grazing incident X-ray scattering (GIXS) activities continues to increase owing to its unique ability to acquire highly intense scattering signal even for films of nanoscale thickness. This is because that at grazing angle the X-ray beam has a large footprint on the film in addition to a signal enhancement near the critical angle of the substrate. The GIXS experimental method is now well established and the angular resolution of the scattering experiments is improved by using highly collimated beam at synchrotron X-ray sources. For data analysis there exist many algorithms to account for the multiple reflection-scattering events; for the investigation of coatings, films and particles on surfaces these algorithms are found to be adequate. In this work the application of GIXS for characterizing highly ordered nano-structured surface will be exploited. A New dynamical scattering never been reported before was observed. The origin of the observed dynamical scattering as well as its potential for defect detection will be discussed.

7638-35, Session 8

Characterization of cross-sectional profile of nanostructure line grating using small-angle x-ray scattering

Y. Ishibashi, T. Koike, Y. Yamazaki, Toshiba Corp. (Japan); Y. Ito, Y. Okazaki, K. Omote, Rigaku Corp. (Japan)

Mass production manufacturing requires higher resolution characterization of cross sectional profile with decreasing the pattern size. The values of critical dimension (CD), height (HT) and side wall angle (SWA) are so important that CD and HT have been measured by CD-SEM and Scatterometry. Recently the demand for metrology of fine structure such as top rounding (RT) and bottom rounding (RB) has also been more severe. There are many tools for characterization of cross sectional profile such as CD-SEM, Scatterometry, Atomic Force Microscopy (AFM), and Transmission Electron Microscopy (TEM). The influential candidate is Scatterometry because this tool is nondestructive and can observe the cross sectional structure of grating pattern rapidly. However it is difficult to measure rounding instead of a lot of efforts for example an improvement for using shorter wavelength. A measurement technique using small angle x-ray scattering (SAXS) has been introduced as an alternative methods to characterize cross sectional profile with high resolution. The two kinds of measurement system have been proposed. The one is transmission geometry [1-3] and the other is reflection geometry [4]. Synchrotron radiation high-intensity beams are mainly used for the transmission geometry measurements. High signal to noise ratio can be obtained. Another merit is a smaller spot size, which make it possible to measure small area. The weak point is the scattered signal is affected by the structure of underlayers and by absorption of the thick substrates. The other side, a conventional laboratory x-ray source can be used in the reflection grazing incidence (GI) geometry. X-ray penetration depth can be controlled with glancing angle to the surface and scattered x-ray from surface structure can be detected without effect of absorption of substrates. But the irradiation length of the beam is very large due to grazing incidence geometry. The power of the laboratory x-ray source is lower that MAM time is longer. In this report, measurements of nanostructure line grating on a wafer surface have been carried out using GISAXS with laboratory x-ray source. The cross sectional profile of the pattern is modeled by employing five modeling parameters: CD, HT, SWA, RT and RB. The experimental data is analyzed by comparing experimental and calculated scattered intensity and minimize the residual by least square method. The cross sectional profile of the nanostructure is determined by the optimized values of five modeling parameters. In this presentation we compare the results of the present GISAXS with other metrology tool and discuss capability of GISAXS.

7638-36, Session 8

A new x-ray metrology for profiling structure of semiconductor device patterns

K. Omote, Y. Ito, Y. Okazaki, A. Nakano, Rigaku Corp. (Japan)

The scale of semiconductor device is still continuously shrinking and line width of the device pattern will become close to ten-nanometer in the near future. The present metrology tools have to overcome many difficult challenges in order to control the mass production processes for measuring such a small critical dimension (CD). For example, the electron beam size of CD-SEM is comparable with the measured CD itself, the sensitivity of optical proves will be reduced because a wavelength of them are much longer than the CD, and so on. In addition, uniformity of the CD, for example line width roughness (LWR), becomes more crucial for the device performances and the metrology has to have enough sensitivity for detecting such a kind of non-uniformity. Small angle x-ray scattering (SAXS) method is one of a candidate having such capabilities for measuring CD and its uniformity. Jones et al. demonstrated SAXS measurements with transmission geometry [1]. It is suited for measuring relatively small area (40 × 40 µm2), however, longer collecting time should be necessary due to small

scattering volume and a pattern of underlayers can affect the scattering data because x-rays transmit all the layers. On the other hand, grazing incidence surface scattering (GISAXS) is sensitive to the surface nanostructures and capable to analyze two-dimensional structure without affecting by the underlayer, even.

We have developed GISAXS measuring system for optimizing semiconductor device patterns and also developed the analysis software for profiling their structures. GISAXS data can provide the average value of many structural parameters of periodic gratings; pitch, line width, height of grating, sidewall angle, rounding of edges, and fluctuations of the width and height. We have successfully determined such structural parameters of a 100-nm pitch-grating sample. X-rays are irradiated on the sample surface with shallow incident glancing angle and scattering intensity from the grating structure is collected by a pixel-type two-dimensional area detector. Very nice two-dimensional intensity distribution, which reflects two-dimensional profile of the grating structure, has been successfully detected. We can see many diffraction ridges along the horizontal QY direction and clear intensity modulation along the vertical QZ direction on each ridge. The analysis is done by optimizing the intensity ratio of the each diffraction line and its intensity decay in the QY direction and intensity modulation in the QZ direction. We can clearly figure out the cross-sectional profile of the grating by using optimized parameters. We are very much emphasized that GISAXS methods can analyze such precise structure nondestructively. It suggests x-ray metrology has a capability to use device inspection of the production line. Precise comparison with cross-sectional TEM result and sensitivity of x-ray metrology will also be presented.

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7638-37, Session 8

Calibration of 25-nm pitch grating reference by grazing incidence small-angle x-ray scattering

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Recently, a sub 50-nm pitch grating reference for critical-dimension scanning electron microscope (CD-SEM) based on Si/SiO2 multi-layer thin-film structures has been developed [1]. So far, a 100-nm pitch grating reference for CD-SEM has been calibrated by adopting deep ultra violet (DUV) laser diffraction with wavelength of 193 nm. For the diffraction theory, the minimum measurement pitch is defined by a half of wavelength. It means the wavelength of DUV laser no longer satisfies Bragg condition for the sub 50-nm pitch grating.

In order to calibrate such a fine pitch grating, we have developed a high-accuracy grazing incidence small-angle x-ray scattering (GISAXS) system with crystal collimator and analyzer (SuperLab, RIGAKU Corp.) [2]. CuK 1 radiation, 0.1540593 nm in wavelength, is used and lots of diffraction peaks can be observed for the grating reference, because x-ray wavelength is much shorter than the pitch size of the grating. In addition, characteristic x-ray, such as CuK 1 radiation, is suitable to use for the calibration, because wavelength of characteristic x-ray is always stable and an uncertainty of the wavelength is much smaller than that of required for the calibration.

The proposed GISAXS system, employing crystal optics, enables to calibrate pitch grating not only for the size of nanometer but also for that of sub-micrometer. In order to confirm the present x-ray metrology, we measured a 100-nm pitch grating reference in advance, and compare with the results of DUV laser calibration system [3]. It is now using for the calibration of 100-nm pitch grating standard for CD-SEM [4]. The average pitch size calibrated by the proposed GISAXS system agrees very well to that calibrated by the existing DUV laser system in the range of uncertainty.

We evaluated a fine 25-nm pitch Si/SiO2 multi-layer grating reference. Even the fine 25-nm pitch grating reference is fabricated in very limited area of 1 μm × 10 mm [1], we have successfully detected more than ten sharp diffraction peaks corresponding to the 25-nm period. From the observed peak positions, the average pitch of the grating is calculated in very high-accuracy with standard uncertainty of less than 10 pm. This accuracy should be good enough for the calibration of the future grating reference for CD-SEM.

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7638-38, Session 8

Metrology with the scanned helium ion microscope (SHIM): benefits and limitations

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Recently, Carl Zeiss SMT Inc. has introduced its Scanning Helium Ion Microscope (SHIM), a sensitive surface inspection apparatus with sub-nanometre resolving power. [1]. This paper presents the assessment of critical dimensions of patterns that are written with the latest generation ASML optical and EUV lithography apparatus using both the SHIM [2] and the industry-standard CD-SEM.

The left figure shows a SHIM Secondary Electron (SE) image of nano-structured resist on a Silicon wafer after exposure with an ASML DUV immersion scanner, after resist development. The darker regions represent approximately 27 nm wide resist lines, the lighter regions represent the Silicon surface. The brighter parts of the image in the lower-left corner show the effect of carbon-contamination due to earlier exposure to the He+ beam. This is probably due to the higher SE-yield of the deposited thin Carbon layer as compared to the SE-Yield of the native photo-resist and Silicon.

The right image shows a CD-SEM Secondary Electron (SE) image of the same nano-structured resist. At first sight the SHIM image shows tighter white bands at the edges of the sample, indicating an improved resolution wrt the SEM image. Improving the resolution is important to keep up with the decreasing feature sizes of the coming technology nodes.

A possible benefit to the SHIM image above the SEM image is the smaller range over which SEs escape from the sample. This reduces the systematic error in measurement of the true structure topology. Another benefit of SHIM is its larger Depth-of-Focus at similar resolution, enabling simultaneous and accurate imaging of top and bottom CD of the trenches in the resist. Resist shrinkage is not (yet) observed, probably due to the transparency of the thin resist films for 25-30 keV Helium. A possible drawback may be damage to the resist and/or wafer due to either enhanced sputtering. Helium bubble creation in the Silicon substrate will occur only at very large dose, and is not (yet) observed in this application.

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7638-39, Session 8

IR microscopy as an early electrical-yield indicator in bonded wafer pairs used for 3D integration

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Microscopy of 3D interconnect structures is challenged by the opaque nature of silicon. Infrared (IR) microscopy provides a way of “looking”

through silicon where microscopes based on visible wavelengths fail. Perhaps the most prevalent application of IR microscopes in 3D manufacturing is imaging sub-surface features at the interface of a bonded wafer pair. The ability to see through silicon using IR microscopes enables a variety of metrology techniques, including the overlay of circuit layers (e.g., metal 2 to via). IR microscopy is a non-destructive technique, and as such, it is an ideal candidate for in-line metrology for the bonded wafer pairs required for 3D interconnects.

This paper reviews overlay metrology capability for an IR microscope. The ability to measure the overlay of bonded wafer pairs according the 2007 International Technology Roadmap for Semiconductors (ITRS) is demonstrated. Overlay tolerances for a variety of copper interconnect test structures is predicted based on electrical designs, and overlay results are compared to electrical test results. The use of IR microscopy as an early indicator of electrical yield is clearly demonstrated.

7638-40, Session 9

Enhanced capture rate for haze defects in production wafer inspection

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Photomask degradation via haze defect formation is an increasing troublesome yield problem in the semiconductor fab. Wafer inspection is often utilized to detect haze defects due to the fact that it can be a bi-product of production wafer inspection; furthermore the detection of the haze is effectively enhanced due to the multitude of distinct fields being scanned. In this paper, we demonstrate a novel application for enhancing the wafer inspection tool's sensitivity to haze defects even further. In particular, we present results of bright field wafer inspection using the UVision on a production photo layer wafer suffering from haze defects.

One way in which the enhanced sensitivity can be achieved in inspection tools is by using a double scan of the wafer: one regular scan with the normal recipe and another high sensitivity scan from which only the repeater defects are extracted (the non-repeaters consist largely of noise which is difficult to filter). Our solution essentially combines the double scan into a single high sensitivity scan whose processing is carried out along two parallel routes (see Fig. 1). Along one route, the sensitivity is reduced and defects follow the standard recipe thresholds to produce a defect map at the nominal sensitivity. Along the alternate route, only field repeater defects are identified using an optimal repeater algorithm that eliminates "false repeaters". At the end of the scan the two defect maps are merged into one with optical scan images available for all the merged defects. It is important to note that there is no throughput hit; in addition, the repeater sensitivity is increased relative to a double scan, due to a novel runtime algorithm implementation whose memory requirements are minimal, thus enabling to search a much larger number of potential defects for repeaters.

We evaluated the new application on wafers on a photo wafer which consisted of both random and haze defects. The evaluation procedure involved scanning with 3 different recipes.

1. Standard Inspection: Nominal recipe with a low false alarm rate was used to scan the wafer and repeaters were extracted from the final defect map.

2. Haze Monitoring Application: Recipe sensitivity was enhanced and run on a single field column from which on repeating defects were extracted.

3. Enhanced Repeater Extractor: Defect processing included the two parallel routes: a nominal recipe for the random defects and the new high sensitive repeater extractor algorithm.

The results showed that the new application (recipe #3) had the highest capture rate on haze defects and detected new repeater defects not found in the first two recipes. In addition, the recipe was much simpler to setup since repeaters are filtered separately from random defects.

We expect that in the future, with the introduction of mask-less lithography and EUV, the monitoring of field and die repeating defects on the wafer will become a necessity for process control in the fab.

7638-41, Session 9

Preliminary results for photomask haze mitigation in a fab environment

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A persistent industry problem impacting photomask yield and costs has been haze formation. The haze nucleation and growth phenomenon on critical photomask surfaces has periodically gained attention as it has significantly impacted wafer printability for different technology nodes over the years. A number of process solutions have been promoted in the semiconductor industry which have been shown to suppress or minimize the propensity for haze formation, but none of these technologies can stop every instance of haze. Thus some capability will always be needed to remove haze on photomasks with their final pellicles mounted both at the manufacture and long term maintenance stages of a mask's lifetime. A novel technology is reviewed here which uses a dry (no chemical effluents) removal system to sweep the entire printable region of a pellicilized photomask to eliminate all removable haze regardless of the mask substrate materials or the presence of critical patterns. Operational process techniques for this system and performance in removal will be shown for haze located on the mask pattern surface, mask backside, and underside of the pellicle membrane. Finally, preliminary data from tool acceptance and preliminary use in a production environment will also be reviewed.

7638-42, Session 9

Use of wafer backside inspection and SPR to address systematic tool and process issues

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Defects on the backside of wafers can be either tool or process induced and can cause lithography-related issues such as focus deviation or chuck contamination. Tool induced scratches, process induced contamination, or residues on the back of wafers often have unique signatures, such as a repeatable scratch caused by wafer handling equipment or a chuck imprint on the backside of a wafer. Certain backside defect signatures such as large scratches or divots can contribute to wafer breakage or reliability issues.

Spatial Pattern Recognition (SPR) is a method of comparing defect patterns at the wafer level with known defect signatures stored in a library that is created from process data. These defect signatures can represent systematic issues with process tools, handling equipment, or the process itself.

This paper describes a backside inspection method for identifying wafers with both known and new spatial pattern signatures. By reporting the frequency of each signature category, process partitioning can efficiently trace the source of these problems. In addition, new defect signatures can be automatically learned and added to the library. The paper also includes examples of how this method was used to identify backside defect patterns caused by process and tool excursions in a 300mm fabricator.

7638-43, Session 9

Reticle haze control: global update and technology roadmap

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Three year ago authors pioneered a novel method of controlling ammonium sulfate haze by maintaining 193 nm reticles in low humidity environment [1]. Since then this approach became industry standard and is widely used in production fabs around the world. Based on analysis of practical applications in HVM fabs, paper describes

successful approach to reticle haze control, outlines its critical elements and explains limiting factors.

In addition to actual fabs' data paper provides large body of comparative experimental data on humidity dynamics in different reticle storage schemes and arrangements. With these data authors explain why some designs work much better then others and give practical recommendations to lithography practitioners on haze control equipment selections and developing appropriate reticle management strategies.

Using chemical kinetics approach authors attempted to predict reticle haze severity progression at future technology nodes. Analysis revealed that haze severity will progress as CD^-3 (CD- critical dimension) and that current means of the reticle haze control may become insufficient in the near future. Authors outline roadmap for reticle haze control technologies and propose further steps and improvements to extend the current success of reticle haze control.

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7638-44, Session 10

Multidexel-based image simulation and surface reconstruction in CD AFM

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Atomic force microscopy (AFM) provides a vital tool for dimensional measurement of topographic features at up to atomic resolution. Recently, probes with lateral protrusions and feedback systems with bi-directional servo control have been incorporated into the newer AFM instruments in order to allow dimensional characterization, e.g., side-wall angles, side-wall roughness, and width variability of lines and trenches, of reentrant surfaces at the nanometer-scale. Critical dimension (CD) AFMs with such capabilities are urgently needed in the semiconductor industry as feature size is reduced to follow the ITS roadmap.

In order to match such hardware progress in AFM instruments, the underlying algorithms for AFM imaging of reentrant surfaces have become increasingly important. Algorithms to correct the tip dilation effect appear all to use erosion, whether explicitly or implicitly[1], but with differing limitations of implementation. Recent approaches applicable to undercut structures in CD AFM include some based on erosion by slope-matching [2], swept-volume subtraction [2], and morphological dilation and erosion within a dexel representation [3-5].

The most common image representation uses pixels discretized horizontally (conventionally x and y) with a single height that represents a boundary of the sample along a vertical line at x, y. Limitation to a single height means objects (e.g., reentrant ones) with more than one boundary along this line cannot be represented. Dexels use a discrete lattice like pixels, but unlike pixels they may have multiple heights in each column. This allows under-cut features to be represented. The multi-dexel representation is a further generalization of dexels, in which objects are described by combinations of dexels oriented along multiple axes (e.g., not only z, but also x and y). Multi-dexel algorithms allow more efficient and accurate processing of 3D data.

In this paper, we present an implementation of multi-dexel based morphology operations and their applications to image simulation and surface reconstruction in critical dimension (CD) AFM. Figure 1 shows an example of a bi-dexel representation of a scanned image, tip shape and reconstructed surface, where the scanned data from a CD-AFM is converted into a dexel representation with sampling grids in both the z and y directions.

Figure 1 Morphological operations on bi-dexel representation, z-dexel in red and y-dexel in green: a) scanned image, b) tip shape and c) reconstructed surface.

The application of the software to line-width measurement based on both synthetic and actual AFM data is also presented. Examples with the Veeco CD AFM (X-3D) are shown. We detail the conversion of scanned data from Veeco X3D to a multi-dexel representation and the simulation results of morphological operations. We then compare the accuracy and efficiency of multi-dexel based approach with the slope-matching based approach. We further extend this multi-dexel approach to image simulation and surface reconstruction for 3D structures.

In summary, this paper presents a software implementation of multi-dexel based morphological operations that are applicable to complex 3D structures with under-cut features. Practical examples demonstrate its validity, usefulness and its accuracy improvement on nano-scale line-width measurement.

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7638-45, Session 10

Reference material (RM) 8820: a versatile new NIST standard for nanometrology

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NIST is introducing a new standard for dimensional metrology and the calibration of the scanning electron microscope (SEM) scale identified as Reference Material (RM) 8820. RM 8820 was primarily intended to be used for calibrating the X and Y scale (or magnification) in SEMs from less than 10 times magnifications to more than 100 000 times magnifications (but, can be used for an array of other purposes). RM 8820 has been lithographically fabricated in collaboration with SEMATECH and its Advanced Metrology Advisory Group (AMAG). The NIST pattern is only one part of a very large array of test structures that were designed for various dimensional metrology purposes useful to semiconductor production technologies. All the AMAG test structures are included on the RM. However, only the NIST pattern has been qualified. The RM 8820 parts of the chip are marked with letters "NIST" and are readily visible with the naked eye as small bright squares within the large chip. The RM structures have pitches ranging from 200 nm to 1.5 mm in both X and Y directions. In the center of the RM 8820 pattern, there is a large expanse of structures for focusing, astigmatism correction and for scan linearity measurements. There are two sets of identical X and Y pitch calibration structures. These are marked with numbers 1 and 3 for the X direction and 2 and 4 for the Y direction. Most SEMs require a set of calibration structures to cover the full range of possible magnifications and this standard is designed to meet that need. Like its predecessor RM 8090, the new standard RM 8820 was designed to provide good contrast at both low and high electron landing energies (accelerating voltages). RM 8820 can also be used for non-linearity measurements, especially at lower than 10 000 times magnifications. For these and other purposes, discussed in the presentation, RM 8820 can also be used on/in any other type of microscope, such as optical and scanning probe microscopes and for scatterometry measurements.

7638-46, Session 10

Dimensional metrology with sub-nanometer uncertainty: unique role of AFM as the reference

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The 2007 edition of International Technology Roadmap for Semiconductors (ITRS) has introduced a new metric for metrology quality - measurement uncertainty (MU). For decades reproducibility of measurements or precision was used as a metrology metric. The new metric, MU, has precision as one of many uncertainty components. Additional significant components are tool matching, sampling uncertainty, sample-to-sample bias variation, probe-sample interaction (shrinkage, charging, carbonization), etc. The ITRS keeps the list open-ended concluding with the "other" component.

Once critical dimensions (CD) reach range of 100 nm and, therefore, needed for proper process control metrology MU reaches 1-2 nm, sampling and bias variation components usually start to dominate. It is a real challenge to keep sample-to-sample bias variation of scanning electron microscopy (SEM) and optical scatterometry (OCD) at a nanometer level. Unless special measures are taken MU of CD SEM and OCD could easily exceed 2-4 nm. This fact is well documented. MU can be measured accurately only if a reference metrology (RM) is employed. Therefore, use of RM becomes a must if true MU to be evaluated. Unfortunately, choice of RM tools is very limited. CD atomic force microscope (AFM) is a possible choice. Independence of CD AFM bias from proximity effects, sample material, dimensions, shape as well as thorough sampling statistics and SI-traceability make AFM a good candidate for RM in many practical cases. Recent developments and studies suggest that CD AFM may provide sub-nanometer MU for some key semiconductor applications.

How one may achieve a long-term sub-nanometer MU of in-line process control metrology? In this work we suggest a simple but efficient and tested way of establishing CD metrology with sub-nanometer MU in industrial environment. The method consists of 3 steps:

- Creating technology representative set of "golden" samples calibrated using SI-traceable CD AFM.

- Minimizing MU of in-line metrology using pre-calibrated "golden" samples (tool choice, settings, model tuning and calibration).

- Employing in-line RM tool for systematic verification of bias of in-line "work horse" metrology. Preventing of in-line metrology bias excursions.

We conclude that RM is a must for achieving needed today sub-nanometer MU of CD metrology. To insure long-term performance of in-line metrology and, therefore, reliable process control we recommend employment of in-line RM system. SI-traceable CD AFM is a proper RM tool for the task.

7638-47, Session 10

Calibration of 1-nm SiC step height standards

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We aim to develop and calibrate step height standards for nanotechnology, especially for the calibration of scanned probe microscopes operating at their highest levels of magnification. In previous work we fabricated and calibrated step height standards consisting of the monatomic steps on the (111) surface of single crystal Si and provided a recommended value of 312 pm ± 12 pm [1]. In the current work we have performed traceable measurements of 1 nm step height specimens fabricated on the (0001) 4H-SiC surface [2]. The step height measurements were performed using a calibrated atomic force microscope (C-AFM) [3], calibrated with respect to the wavelength of light along all three axes of motion. A preliminary analysis of the measurements yields an average step height value of 0.97 nm with a statistical (Type A) uncertainty of ± 0.03 nm (k = 1). The expected value is 1.008 nm, derived from the parameters of the crystal lattice [4]. We are in the process of working out a complete analysis of the data for the 4H-SiC step height and an uncertainty budget, which will also include the Type B sources of uncertainty.

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7638-49, Session 11

Sub-50-nm critical dimension measurements using a 193-nm angle-resolved scatterfield microscope

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Resist on silicon sub-50 nm Critical Dimensions have been investigated using a 193 nm angle-resolved scatterfield microscope. This microscope, in addition to having both high-magnification and Fourier-imaging paths, allows customization of the Conjugate Back Focal Plane (CBFP). Here, angle-resolved Fourier-plane images are collected as target is illuminated over a range of all possible azimuthal angles (E [0, 360] degree) and limited polar angles corresponding a Numerical Aperture (NA) from 0.12 to 0.74 (E [7, 45] degree). Direct experimental data fitting using Levenberg-Marquardt algorithmic optimization coupled with Modal Method of Fourier Expansion (MMFE) and Finite Element Method (FEM) have been performed. Uncertainties on CD parameters have been estimated under normal distribution theory. We show quantitative measurements of 20 nm and 35 nm linewidths for different space/line ratios. These CD measurements are compared to AFM and CD-SEM measurements.

7638-50, Session 11

Effect of converging optics on the accuracy of scatterometry measurements

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Scatterometry measurements are often interpreted with theoretical simulations that assume plane wave illumination with an incident direction given by the centroid of directions appropriate for the tool. However, in order to maintain the illumination beam within the bounds of a very small target, relatively large numerical apertures are required. Evaluation of the effects of the non-zero numerical aperture can be computationally expensive, since the simulations must be performed over multiple directions, and even if the centroid direction is along the grating direction, some simulations must be performed in a conical geometry. In this presentation and paper, we will discuss the effects of finite numerical aperture on the accuracy of scatterometry measurements. While the largest effects appear near Wood's anomalies, when diffraction orders propagate along the surface, the effects are not limited to those regions of data. Methods for assessing these effects will be compared, with an eye towards minimizing the number of required simulations. For example, it is found in many cases, that only three simulations are needed, of which only one requires a conical geometry. Data obtained from a nanoimprinted polymer grating using a spectroscopic ellipsometer will demonstrate some of the effects.

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7638-51, Session 11

Use of multiple azimuthal angles to enable advanced scatterometry applications

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The ability to extract critical parameters using scatterometry depends on the parameter sensitivity and correlation at different wavelengths. These, in turn, determine the key metrics: accuracy, precision, and tool-to-tool matching. Parameter sensitivity and correlation can vary drastically, depending on whether the oblique incident light beam is parallel (azimuth angle = 90 degrees), perpendicular (azimuth angle = 0 degrees), or at an intermediate angle to the measured structures. In this paper, we explore the use of both variable- and multiple-azimuth (AZ) angle spectroscopic ellipsometry (SE) to optimize the measurement performance for different applications.

The first example compares the sensitivity and results using SE at 0- and 90-degree AZ angles for a BEOL post-litho metal trench application. We observed up to a sixfold improvement in key metrics for critical parameters using 90-degree over 0-degree AZ angle spectra.

The second example illustrates the benefits of a multiple-AZ angle approach to extract critical parameters for a three-dimensional logic FinFET structure. Typically, this approach simultaneously fits two sets of SE spectra collected from the same location on the wafer at different AZ angles with the same physical model. This helps both validate and decorrelate critical parameters, enabling robust measurements. This approach measures the critical parameters of the FinFET with good repeatability while accurately tracking a designed DoE.

7638-52, Session 11

Simultaneous measurement of optical properties and geometry of resist using multiple scatterometry gratings

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Shrinking design rules and reduced process tolerances require tight control of CD linewidth, feature shape, and profile of the printed photoresist geometry. Scatterometry, a high-throughput model-based technology, replaces the traditional CD-SEM linewidth measurement by providing fast characterization of process windows across multiple pitch and CD structures, multiple points across the reticle field, and multiple lithography cells. In a typical scatterometry measurement, the profile information is extracted by theoretical modeling of the spectral response of the structure under measurement. During such measurement, a number of “educated” assumptions are typically made - one of them concerning the optical properties (n&k) of the material films under measurement. The most common assumption is that of “non-variability” of optical properties - using fixed optical properties for generating the physical model for the measurement. This assumption has the advantage of reducing the number of variable parameters of the model, thus enhancing the precision of the extracted geometrical parameters.

However, if the optical properties vary slightly across wafer (due to slight differences in photoresist bake temperature, for example) or between batches of photoresist material, this real - but not modeled - optical variation can alter the reported geometrical profile and induce unwanted bias to the reported numbers. A more accurate modeling assumption considers the possible variability of the optical properties in the full parameterization of the model. With the “floating materials” assumption, the accuracy of the modeling is augmented at the expense of precision of the measurement, which is typically reduced due to the additional floating parameter(s). Some trade-off optimization of the modeling is possible, but both typical assumptions lead to uncertainty of either type A (precision) or type B (bias) in the measurement of the profile.

Previously, we presented the use of a novel methodology (based on simultaneous analysis of multiple CD and pitch targets) to critically enable the offline measurement of optical properties of films directly on scatterometry structures on product wafers, thereby improving the time to solution. In this paper, we extend this technology to enable online simultaneous measurements of optical properties and geometrical profiles. We improve the measurement performance by augmenting the spectral information with multiple patterned and unpatterned targets. This use of spectra from multiple targets increases the accuracy (type B) of the measurement by accounting for possible variability of optical properties while maintaining good precision (type A) for the measured geometrical profile. This work compares existing scatterometry solutions (models with fixed optical properties) with our newly extended methodology. We apply the improved method to quantify the limits of expected variability in materials properties and compute the impact of variable optical properties on the measured geometrical profile (like CD, SWA, etc.). We also investigate the uncertainty in computing scanner parameters like dose and focus due to this variability when using the traditional scatterometry approach (fixed optical properties).

7638-53, Session 11

Stability of polarimetric grating characterization with beam spot larger than grating box

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Recent work on the characterization of gratings using the depolarizing Mueller matrices measured on the boundary between the grating and the substrate [1] has shown good performance provided the substrate was sufficiently well known to allow accurate modeling of its spectral reflectivity. Basically, the measured data were fitted by a model describing the spectral reflectivities and normalized polarimetric responses of both the grating and the substrate, together with their relative weights in the measured data. These relative weights could be described by a single, wavelength-independent parameter (equal to the ratio of the illuminated areas of the grating and the substrate if the incident intensity is spatially uniform).

Further work on decompositions of depolarizing Mueller matrices into sums of non-depolarizing contributions [2] removed the need to know or model the absolute spectral reflectivity of both components: only the normalized Mueller matrix Ms of the substrate is needed. Briefly, the grating Mueller matrix MG can be extracted from the depolarizing matrix M measured in the mixed conditions as MG = M - alpha MS , where the weighting coefficient alpha is determined independently of any model, by requiring that the extracted matrix MG is non-depolarizing. Of course this procedure may be implemented at each spectral point to recover the full spectral dependence of MG. As it is often possible to measure spectrally resolved normalized Mueller matrices of the region outside the grating (or other targets of interest) this development opens new interesting perspectives for the practical implementation of the method.

In this work we report results of the optical characterization of a grating with a beam spot larger than the grating itself. We used a commercially available spectral polarimeter (Horiba Scientific MM-16) with projected beam spot size of 200x300 µm at incidence angle of 45 degrees. The grating (160 nm pitch, 80 nm nominal CD and 100 nm nominal depth), was a 250 µm wide square box. The measurements were taken at different azimuthal angles with the beam spot positioned partially outside of the grating. The normalized matrix Ms of the substrate surrounding the grating box was also measured alone, as mentioned above.

The spectrally resolved MG matrices retrieved from the measured depolarizing matrices M were fitted using rigorous coupled-wave

method (RCWA) and a standard trapezoidal model with three free parameters: the middle CD, the grating depth and the side-wall angle. For all azimuthal angles, the results are very close to those obtained by standard characterization of a similar grating (produced by photolithographic process with the same mask on the same wafer), except in a few cases where the grating contribution was only 5% of the total signal. The overall dispersion of the three parameters is within a few nanometers from the statistical mean, a performance comparable to that of standard grating characterization with all the beam spot within the grating box.

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7638-54, Session 11

Scatterometry characterization of spacer double patterning structures

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Optical lithography adopts double patterning as an attractive solution to circumvent the fundamental technological barrier with no alternative like EUV for 22nm technology node and beyond. Double patterning (DP) overlay errors result in CD errors and vice versa demanding increased critical dimension uniformity (CDU) and improved overlay control. In our previous work, we apply scatterometry measurements with rigorous coupled-wave analysis (RCWA) approach to characterize litho-freeze-litho-etch and self-aligned double patterning (SADP) structures1. Overlay errors and CDs are successfully measured by fitting the optical signals with spectra calculated from a model of the target and the results are compared with other approaches (CD-SEM, IBO and multi-pad DBO).

Scatterometry techniques have been used to characterize the performance of scanner in terms of CD uniformity and stability and exhibited very good agreement with CD-SEM2. In this paper, spacer stack (Figure 1) will be used to characterize the CD uniformity (CDU), sidewall angle (slope) and resist thickness variation across the wafer by various scatterometry techniques. We will also study the contribution of CD variations to overlay errors.

The sensitivity simulations for spacer target showed a very strong TETM response. Similar sensitivity response for spacer grating was also observed for profile parameters of interest (CD, side wall angle and stack thickness) by spectroscopic ellipsometry (SE) at azimuth angle of 45 degrees (Figure 2).

Wafers of different spacer double patterning film stacks will be used. Measurements will be made in 16 cells per field in all fields across the wafer, and also 64 cells per field (dense mapping) in one field. The data collection and analysis will be performed on Atlas tool with normal-incidence spectroscopic reflectometry (NISR) and spectroscopic ellipsometry (SE) measurement techniques. We will present the Optical Critical Dimension (OCD) metrology results for double patterning spacers with NISR and SE analysis.

We will show the optimization of CDU and profile characteristics for spacers at various process steps - litho, etch and spacer with SE and NISR methods using RCWA calculations. We will also show the correlation of CDU at various process steps (litho, etch, and spacer) and validate against CD-SEM results.

7638-55, Session 12

Sub-nanometer calibration of CD-SEM line width by using STEM

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The novel method of sub-nanometer accuracy (uncertainty) for the line width measurement using STEM (Scanning Transmission Electron Microscope) images is proposed to calibrate CD-SEM line width measurement. In the proposed method, the traceability and reference metrology of line width standards are established using Si lattice structures and the uncertainty evaluations.

The standard of line width on the Si wafer is sliced on Si 110 surface as a thin specimen of 100 nm thickness by FIB (Focused Ion Beam) micro sampling system. Then the bright-field STEM images of the specimen are obtained by STEM (HD-2700) with accelerating voltage of 200 kV and magnification of x70,000 to x3,000,000. The high magnification STEM images show Si lattice structures clearly.

From the images, the line width is calculated the following procedure:

1) The STEM image is transformed to the frequency domain image by 2D-FFT (Fast Fourier Transform). The peeks of the frequency domain image indicate the image magnification and inclination angle of the STEM image by the relationship between the Si lattice structure and image pixels.

2) The images are rotated by the inclination angle. Therefore, the positions of Si lattice are on the same line of the image with distances of Si lattice size.

3) The size of image pixel is evaluated comparing with Si lattice size and the uncertainty of the size and image magnification is evaluated.

4) A novel noise reduction method using Si lattice structures is proposed. In the method, 5 or 9 pixels at the Si lattice positions is averaged using Si lattice size on the images, therefore, the image contrast within Si lattice area is increased and the edge of Si lattice area is clearly recognized.

5) The edge position on the each Si lattice line is defined at the 50% intensity between outside and inside of Si lattice area.

We applied the above methods to the 50 nm Si line width standard. The edge position on each Si lattice is calculated and the edge positions are estimated as the parabolic curve. The standard deviation of the edge positions is less than 0.1 nm.

The expanded uncertainty of the line width is evaluated from the uncertainty contributors of repeatability, image magnification, Si lattice counting by edge detection, environmental condition and so on. The contributors of Si lattice counting and image magnification are estimated as the large uncertainty contributors in the case. From these calculation, the expanded uncertainty ($k = 3$) will be estimated less than 0.5 nm (3 sigma).

In future works, we will compare the line width by STEM images using proposed method, the results by CD-SEM images and AFM images on the same line position. Then the detailed estimation of the uncertainty of the proposed method is calculated for establishment of the traceability and the reference metrology of the line width measurement.

7638-56, Session 12

Electron-beam induced photoresist shrinkage influence on 2D profiles

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For many years, lithographic resolution has been the main obstacle in keeping the pace of transistor densification to meet Moore's Law. For the 32 nm node and beyond, new lithography techniques will be used, including immersion ArF (iArF) lithography and extreme ultraviolet lithography (EUVL). As in the past, these techniques will use new types of photoresists with the capability to print smaller feature widths and pitches. Also, such smaller feature sizes will require the use of thinner layers of photoresists, such as under 100nm.

In previous papers [1,2], we focused on ArF and iArF photoresist shrinkage. We evaluated the magnitude of shrinkage for both R&D and mature resists as a function of chemical formulation, lithographic

sensitivity, scanning electron microscope (SEM) beam condition, and feature size. Shrinkage results were determined by the well accepted methodology described in ISMI's CD-SEM Unified Specification [2]. A model for resist shrinkage, while derived elsewhere [3], was presented, that can be used to curve-fit to the shrinkage data resulting from multiple repeated measurements of resist features. Parameters in the curve-fit allow for metrics quantifying total shrinkage, shrinkage rate, and initial critical dimension (CD) from before e-beam exposure. With these parameters and exhaustive measurements, a fundamental understanding of the phenomenology of the shrinkage trends was achieved, including how the shrinkage behaves differently for different sized features. This work was extended in yet another paper [4] where we presented a 1-D model for resist shrinkage that can be used to curve-fit to shrinkage curves. Calibration of parameters to describe the photoresist material and the electron beam were all that were required to fit the model to real shrinkage data, as long as the photoresist was thick enough such that the beam could not penetrate the entire layer of resist.

In this paper, we extend this work yet again to a 2-D model of a trapezoidal photoresist profile. This model thus allows for solving the CD shrinkage in the thin photoresist case, which is now of great interest for upcoming realistic lithographic processing. It also allows us to predict the change in resist profile with electron dose, and also to predict the influence of initial resist profile on the shrinkage characteristics. In this work, the results from the previous paper will be shown to be consistent with numerically simulated results, thus lending credibility to these papers' postulations [1,4]. Also, results from this 2-D profile model can also give clues as to how we might, in the future, model the shrinkage of contour edges of 3-D shapes.

Furthermore, we developed a multi-dimensional analytical model that is based on the presumptions set forth in the previous publications. The model has been validated for 1-D case (straight endless lines) and for some simple 2-D geometries such as circles and ellipses. It may be extended on shapes that are more complicated and on the 3-D case as well.

With these findings, we can conclude with observations about the readiness of SEM metrology for the challenges of future photoresist measurement, as well as estimate the errors involved in calculating the original CD from the shrinkage trend.

7638-57, Session 12

CD-decrease caused by ArF-shrink in 20-nm node process

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Immersion ArF photo-regist (PR) line features shrink by electron dose during CD-SEM measurements in after development inspection (ADI). This is a big issue because the ArF-shrink in ADI may cause a-few-nanomber CD-decrease in after etch inspection (AEI). However, in 20nm node process the ArF-shrink issue might not be so serious as we think.

In our experimental results an ArF-shrink in ADI for 20nm node processed line caused no significant CD-decrease in AEI. Thus, it would be better to use high acceleration voltage and high electron-dose in ADI, in order to high repeatability CD for precise process control.

In the experiments, line features about 40nm in ADI were developed by immersion ArF lithography. In ADI we caused various ArF-shrink patterns in each by measuring 1, 3, 5, and 10 times by a CD-SEM. Obviously by ArF-shrink, CD in ADI decreased with increase of the measurement time. Then, in dry-etch process we had PR-slimming etch to the PR feature's side wall, i.e., from 40nm became down to 20nm in linewidth. Subsequently by poly silicon etch process the line feature about 20nm is created. Again, we measured the features that have been measured in ADI to evaluate the AEI's CD decrease caused by the ADI's ArF-shrink. Contrary to our experience, evaluation results showed no significant change in the AEI feature's CDs that have been measured by 1, 3, 5, and 10 times in ADI. In other words, various ArF-shrinks in the ADI did not cause CD change in the AEI.

A possible explanation is electron penetration that is as deep as 20nm or less. In the 40nm PR features the probe-beam electrons penetrate into 20nm deep from both sides of the features. As the ADI linewidth is about 40nm, entire of the line feature is electron dosed. Such dosed PR may be easily removed in the PR-slimming etch. Thus, a-few-nanometer change in the ArF-shrink may not cause significant change in the PR-slimming etch.

Note that these results are only seen in 20nm linewidth of AEI features. In 40nm and larger linewidth features the evaluation results were presumable from our experience that AEI CD decreased with the ADI's ArF-shrink. An Atomic Force Microscope (AFM) with contact-free probe tip, by Park Systems Corporation, showed good agreement to the ADI and the AEI by the CD-SEM.

7638-58, Session 12

CD-SEM metrology of non-topographical features

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Traditional target of CD SEM metrology is to provide accurate and precise identification and analysis of topographical features. At the same time with the progress of semiconductor technology arises the need to measure the properties of features that does not have distinct topographical properties. In particularly when we strive to explore the relations of Poly over Active and Metal over Contact, where the reference layer is after CMP. The ability to measure the various distances between Active and Poly layers at the transistor area, the accuracy of polished features overlay with the next layers is very important for yield enhancement in the frame of advanced technology nodes. The measurement of these features with the help of CD SEM tool could be provided on the base of the utilization of its SEM signal contrast behavior. The difference of secondary electrons yield between feature with very shallow or no edges and its surround could help to collect data that is necessary for the outlining of its border.

The following main challenges can be mentioned while developing measurement process for contrast (non-topographical) features: provide analysis of the behavior of SEM signal on its border and to check the applicability of usual SEM metrology topopoints for border identification; find the best tool working parameters to obtain the SEM signal with the optimal contrast properties; provide new metrological methods that will be suitable for the detection of contrast features contours.

In the first part of this paper we provide analysis of the peculiarities of contrast features SEM signal and specify what efforts should be made for the adaptation of the currently used metrology methods for contrast features measurement. Poly over Active and Metal over contact wafers were provided by Tower Semiconductor to evaluate metrology algorithms. At the second part we discuss the results of the tests provided for the investigation of measurement results precision obtained for contrast features layers. At the final part of paper we sum up results of the provided analysis and outline next steps for development of effective metrology methods for contrast features.

7638-59, Session 12

SEM image modeling using the modular Monte Carlo program MCSEM

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A new Monte Carlo simulation package MCSEM, developed at the Physikalisch-Technische Bundesanstalt (PTB), is presented. The program was designed mainly for SEM metrology of semiconductor and photomask structures, however e-beam lithography can be simulated as well. A key feature of the program is its modular design which allows an easy adaptation to new simulation tasks. Time-critical

routines are programmed in C++, embedded in a Matlab or Octave environment, respectively. Three dimensional specimen structures are defined using a simple script language based on the Constructive Solid Geometry (CSG) technique.

The program uses two types of secondary electron (SE) tracking: Macroscopic SE movement in the specimen chamber and SE detection is modeled by an external SE raytracing program. Due to time constraints, the implementation in the Monte Carlo simulation is done by pre-calculated look-up tables. For microscopic SE tracking directly above the specimen surface, the electrostatic field is calculated by a Poisson solver and the equation of motion is solved for the SE trajectories.

The model allows to apply point-shaped or Gaussian distributed electron probes, both for parallel and conical electron beams. Different physical models for electron-specimen interaction can be chosen, namely the Bethe continuous slowing down approximation (CSDA) in the modification of Joy and Luo [1] for inelastic scattering and tabulated Mott scattering cross sections [2] for elastic scattering.

The Monte Carlo simulation package has been tested in comparison with other Monte Carlo programs as well as with measurement results. Different applications of the program are presented including contrast variations at iso/dense photomasks patterns and their impact on CD evaluation, modeling of charging effects, and the CD influence of structure imperfections (e.g. line edge roughness and corner rounding).

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7638-60, Session 13

A comparison of advanced overlay technologies

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We report the results from a study comparing different image-based (IBO) and diffraction-based (DBO) overlay methods. The DBO measurements used both model-based regression (mDBO) and empirical self-calibrating DBO (eDBO) analysis. mDBO enables measurement with only a single target per measured axis, which can reduce the total target size needed for overlay measurement to 25% of that needed for an eDBO measurement1.

Each of the twelve test wafers used in the study had a different film stack, allowing the quality of overlay data obtained under a range of film conditions to be tested. Measurements were made in six test cells in 23 fields distributed evenly across the wafer. Each test cell contains nominally identical pairs of bar-in-bar and Blossom IBO targets, and four DBO targets with different grating CD and pitch. The DBO targets were divided into eight separate grating pads with different positional shifts between layers, permitting eDBO two-dimensional measurements2 as well as mDBO using a subset of the eight pads. IBO measurements were performed using a Caliper Mosaic imaging tool, and the DBO measurements with both Atlas and Impulse normal-incidence spectral reflectometry (NSIR) tools.

The total measurement uncertainty (TMU) of the IBO measurements was in the range 0.2 to 0.6nm, and was dominated by TIS variability (TIS 3). TIS can be removed by combining 0° and 180° measurement pairs at all locations, though at the expense of halving the tool throughput. In this mode TMU using Blossom targets was 0.18nm or less.

TIS in DBO measurements was very small, which is consistent with our previous work3. eDBO TMU was 0.18nm or less without TIS correction. mDBO and eDBO TMU results were very similar, with mDBO TMU increasing slightly when fewer measurement pads were used.

A further indication of measurement accuracy can be made using the method known as Optical Mark Fidelity4 (OMF), which measures the difference in results from closely located, nominally identical targets. Figure 1 shows the correlation between TIS-corrected measurements made with two nominally identical Blossom targets in each cell. OMF (calculated as three times the standard deviation of the measurement difference) was 0.63nm.

We applied the same test to our mDBO measurements using different groups of 4 pads to perform two independent mDBO measurements from each target. Figure 2 shows the mDBO results from the same wafer used for the IBO data. TIS correction was not used. The OMF of 0.35nm was just over half that of the IBO result.

Model-based DBO allows us to make high quality overlay measurements with smaller targets than other, empirically-based DBO methods. DBO TIS is virtually zero, and the lower OMF than IBO data points to superior accuracy. NISR DBO measurements can achieve both the measurement uncertainty and cost of ownership needed for future process nodes.

7638-61, Session 13

Detection of lateral CD shift with scatterometry on grating structures in production layout

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In 32nm/22nm advanced technology node, double patterning lithography is considered for semiconductor manufacturing. It necessitates tightened requirement of overlay measurement, i.e. to measure the position of a pattern with respect to that of a pattern in the underlying layer. The measurement target design plays a fundamental role in overlay precision and accuracy. Typical alignment target, such as bar-in-bar or box-in-box, has precision, accuracy, and size restrictions. This prompts us to look into better alignment targets. Recently, scatterometry-based metrology and profile model capability have been extended to measure multi-level grating structures. In addition, scatterometry has been shown to be the best choice for integrated metrology to perform wafer-to-wafer control. Therefore, it makes sense to consider using scatterometry for overlay measurement.

In this research, the modeling analysis is performed on the spectra taken directly from a real pattern area with grating-on-grating structure. The CD at the grating on top and the lateral shift between the top and the bottom gratings can be detected simultaneously. The lateral shift between the layers can be verified with the traditional overlay box. Unlike the traditional box-in-box target that has micrometer CD size, the CD size of the scatterometry OVL target is much more closer to that on the real device. So, it can much better reflect the OVL shift on real devices. We also studied the non-model-based scatterometry OVL measurement using a 673-nm semiconductor laser with a 10μm X 20μm target size, wafer-to-wafer control of CD and lateral shifts on some critical layers with grating-on-grating structure, as well as the CD and OVL variations within layer and from layer to layer for double patterning.

7638-62, Session 13

Automated optimized overlay sampling for high-order processing

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This project is the continuation of work reported previously at this conference (Kato, et. al., SPIE 2009). Overlay control is one of the most critical domains for successful advanced microlithography. Overlay sampling, balancing the needs of increased information versus the constraints of throughput, has been a topic of considerable interest for many years. Two significant inflections in the semiconductor industry require even more careful consideration. First, the transition from linear to high order overlay control and the impact of immersion creates significant requirements on both sampling and the impact

of outliers (or flyers). Second, the transition to DPL schemes (dual patterning lithography) involves significantly tighter tolerances, and hence increased requirements on sampling. To address sampling challenges, an analysis tool has been developed to enable quantitative evaluation of sampling schemes for both stage-grid and within-field analysis. The automated analysis tool optimizes the sampling based on considerations such as layout geometry, model, and tolerances for uncertainty. This allows the improvement of the uncertainty of prediction and the residuals over typical sampling by up to 50% while keeping sampling reasonable and providing optimal sampling/error rates. In addition, a Monte Carlo validation based on many sampling iterations of "omniscient" data sets provides an additional tool to understand trade-offs between sampling schemes. The tools developed here automatically provide sufficient sampling for product development and ramp up as well as mature processes based on user criterion. Previous studies indicated (1) the need for fully automated solutions taking individual judgment calls out of the decision tree, and (2) the need for improved algorithms, both of which are described here.

7638-63, Session 13

A novel robust diffraction-based overlay metrology concept for the measurement of critical layers of memory device

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Current image based overlay metrology is not suitable for the critical layers of near future memory production. At this node, measurement reproducibility of 0.6nm or better is required. Also the number of sampling points is expected to increase due to the need for higher order process corrections for the exposure tool. To maintain or improve on total measurement cost, these requirements should be met without negatively impacting throughput.

ASML YieldStar is a novel diffraction based metrology system especially designed to meet these challenging requirements for next generation memory device. In addition to overlay metrology, the system is capable of measuring CD and SWA within the same measurement cycle. It can also be used to monitor exposure tool overlay and focus stability. The YieldStar platform is designed such that it is extendable to the advanced lithography node and beyond without sacrificing productivity performance.

Preliminary measurement of the critical layers of memory device demonstrated the promising capability of YieldStar. Total Measurement Uncertainty (TMU) below 0.6nm was obtained for all critical layers. Best TMU result that was achieved was below 0.1nm, substantially lower than conventional image based metrology. These high precision results were obtained whilst still meeting the desired throughput of in excess of 90wph at volume production sampling conditions.

7638-64, Session 13

Concerning the influence of pattern symmetry on CD-SEM local overlay measurements for double patterning of complex shapes

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The continuing trend to reduce feature sizes and pattern pitches down to 22 nm technology node and beyond requires the introduction of double patterning technology (1) (2). Stringent overlay and CD control are some of the most critical issues for double patterning. According to the ITRS, 22nm technology node requires 8-10 nm overlay control. In LELE (Litho-Etch-Litho-Etch) double patterning scheme, the measurement of overlay on or near actual device patterns, which we call "local overlay measurement", ensures that stringent overlay budget is also satisfied in the device area. We discuss a new local overlay measurement technique on actual device patterns using CD-SEM, which can be applied to 2D device structures such as an SRAM contact hole array or more complex shapes. CD-SEM overlay measurement can provide additional local overlay information at the site of device patterns, complementary to the conventional optical overlay data.

The methodology introduces a local overlay vector which is defined as the displacement vector between the experimentally determined centroids for each complex layout containing many 2D shapes and sizes in the CD-SEM field of view. In general the geometric arrangement of shapes can be different for each set of patterns in a double patterning process. This can lead to a non-zero local overlay vector even when there is perfect alignment. One method for dealing with this is to choose symmetrically arranged patterns. A more general method is to calculate the displacement vector from design information assuming perfect alignment and then subtract that from the raw local overlay vector. The symmetry of the pattern arrangement can also affect how the local overlay responds to process variation. It may be desirable to simultaneously measure such process induced overlay and to minimize it by exploiting symmetry to better reveal other contributors. In this presentation we give several examples.

We have studied the reproducibility of the CD-SEM local overlay measurement to confirm measurement uncertainty small compared with the overlay budget. The repeatability of measurement was evaluated for 22nm node contact hole double patterning layers, and a 3-sigma of ~0.3nm was obtained. Measurement reproducibility based on using neighboring sites rather than repeating measurements on the same sites introduces sample roughness into the measurement uncertainty. This measure is seen as a more realistic estimate of the true measurement uncertainty of a technique. We show it can be less than ~2nm by applying an appropriate sampling plan.

(1) M. Burkhardt, et al., "Overcoming the challenges of 22-nm node patterning through litho-design co-optimization", Proc. SPIE 7274, 727404 (2009)

(2) K. Lai, et al., "32 nm logic patterning options with immersion lithography", Proc. SPIE 6924, 69243C (2008)

7638-135, Session 13

Metrology and process control: dealing with measurement uncertainty

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Metrology is often used in designing and controlling manufacturing processes. A product sample is processed, some relevant property is measured, and the process adjusted to bring the next processed sample closer to its specification.

This feedback loop can be remarkably effective for the complex processes used in semiconductor manufacturing, but there is some risk involved because measurements have uncertainty and product specifications have tolerances. There is finite risk that good product will fail testing or that faulty product will pass. Standard methods for quantifying measurement uncertainty have been presented, but the question arises: how much measurement uncertainty is tolerable in a specific case? Or, How does measurement uncertainty relate to manufacturing risk? Should the process be adjusted based on this (or these) measurement(s)? Since the result of a measurement is best characterized as a probability distribution of estimates of the true value, and product samples represent a distribution of the measured property, a probabilistic risk analysis is called for.

There is a "Decision" box between the "Measure" and "Adjust" boxes in the process control feedback loop, along with "Uncertainty" and "Tolerance" branches. In addition, the "Measure" box contains "Object Image" and "Image Data" components especially relevant to

semiconductors. These processes and their uncertainty contributions will be described in simple terms, along with the importance of image modeling and its contribution.

Then the relationship between the measurement probability distribution and the part tolerance will be shown. The example of deciding whether or not a part is in tolerance will be described. This is a binary decision based on the continuous probability distributions. Costs can be assigned to possible outcomes in the truth table, and an “expected cost” can be assigned to the possible decisions of passing the part or not. The same reasoning can be applied to decisions regarding adjusting the process.

7638-65, Session 14

Spatial signature in local overlay measurements: what CDSEM can tell us and optical measurements can not

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As multiple patterning techniques such as pitch/pattern splitting, become ubiquitous at the 22nm node and beyond, the overlay performance between the patterning layers becomes paramount. Although there have been steady advances in the overlay capabilities of step & scan tools and the ability to enhance the process control stability of overlay (ex. higher order corrections), the ability to measure the overlay on actual device features between multiple patterning levels is quite limited, since overlay metrology is dominated by either optical overlay or to a limited extent scatterometry techniques. Additionally, while there have been attempts to study intra-field overlay at multiple points within the exposure field, the spatial variation of overlay between multiple patterned device features, especially two-dimensional shapes like contacts, below the spatial scale of the distance between optical overlay marks is poorly understood.

Using a SEM-based methodology proposed by Hotta et al.(1), we have determined the “local” overlay vectors at different spatial lengths scales 2 -10 um, 100 um, 1mm, between two groups of patterned contacts formed from a double patterning process. For the group of contacts at the smallest length scales, the local overlay vectors are found to have only small uniformly sized vectors from 1-2 nm, with single orientation, while the larger length scales are found to vary in size with significantly larger vectors ~ 5-7 nm, with varying directions. This methodology is applied to a few different contact design layouts over different spatial length scales. Using the SEM-based method, the centroid for each contact relative to the centroid of patterned grouping of contacts on an FEM gives the lithographic process variation contribution of a patterned contact to the layer to layer overlay, which is found to be ~2-4 nm. A discussion of the relationship of the SEM-based local overlay to optical overlay is presented.

(1) Hotta et al., abstract submitted to SPIE Advanced Lithography 2010.

Example of a small length scale vector plot of local overlay from double patterned contacts. The local overlay between one ensemble of contacts to another ensemble of contacts in shown as a composite image within the dashed lines in the SEM picture. The local overlay (nominal size 1-2nm) is measured at 16 sites within the ~3 x~ 4 um length scale. This is repeated three times across the ~12.5um x ~14 um test array.

Example of large length scale (~8 mm) vector plot of Local Overlay of Double Patterned Contacts, across 3 chips. The local overlay vectors have a large variation in both size and orientation.

Example of the lithographic process contribution vectors of a given contact (shown as contact #3) from a single ensemble. The vectors are determined from the centroid of a given contact relative to the centroid of an ensemble of contacts through a focus exposure matrix.

7638-66, Session 14

Metrology data cleaning and statistical assessment flow for modeling applications

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Modern optical proximity correction (OPC) relies on process measurement data for model calibration. This data, typically taken using Scanning Electron Microscopes (SEM), is expected to be precise to a nanometer, which is not achievable by a single SEM measurement. To overcome precision limitations, multiple measurements are averaged together. At the same time, the amount of data required to calibrate an OPC model increases at each technology node, causing increased reliance on automated data measurement recipes. Unfortunately, SEM engineer time available to review the measured data typically has not changed. This decrease in review time per measurement increases the likelihood of a bad measurement being used for OPC model calibration. Worse yet, a single bad measurement may be averaged with good measurements, making it impossible for bad data points to be identified and removed during the model calibration process.

The combination of multiple data measurements per unique test pattern and increased number of measurement points, with no similar increase in SEM engineer time, has created a situation where bad data points may not be identified prior to model calibration. Incompatible file formats between metrology and modeling tools require manual editing and may add manual data manipulation errors. If the bad data is not identified by the modeler, or has been obscured via statistical processing with good data points, the bad data can prevent calibration of an acceptable model. In the worst case, a fundamentally flawed model may be produced.

Fortunately, this situation can be addressed with a few tools. First, a tool is required for metrology data analysis. For analysis to be efficient and effective, all information relevant to each measurement must be immediately available and accessible to the user. Thorough single-measurement analysis can be performed on the CD-SEM or offline SEM recipe tool, but it is easier and more intuitive for most engineers to view measurement data trends. When viewing data trends, such as CD through pitch curves, the engineer would examine detailed measurement information and SEM images only for questionable data points. Next, statistical assessment of the data is required. Assessments can be used to identify suspected bad data points, allowing the engineer to focus on the data points that are likely erroneous. Assessments are also important for automating data cleaning operations, such as averaging multiple measurements together to create a single measurement value with smaller error. The third tool required to improve the metrology to model flow is automatic translation of data from the CD-SEM to data analysis and cleaning environment to the modeling tool. No manual file editing or manipulation should be necessary. The final tool provides the ability to automate all of the tools discussed previously. The ability to save, store, and reuse settings is critical to maximizing SEM engineer efficiency.

This paper will examine the SEM engineer productivity enhancements enabled by implementing these tools in a post-metrology data assessment and cleaning flow. The improvement in data quality used for the modeling process will also be analyzed in terms of reduced bad measurements and easier to apply statistical assessment methods. Finally, the impact of the data on resulting model quality will be presented.

7638-67, Session 14

High-accuracy OPC-modeling by using advanced CD-SEM based contours in the next-generation lithography

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OPC-modeling is traditionally based on measured CD-data.. As design rules shrink, and process window become smaller, there is an unavoidable increase in the complexity of OPC/RET schemes required to enable design printability. The number of measurement points for OPC-modeling has increased to several hundred points per layer, and metrology requirements are no longer simple limited to simple one-dimensional measurements. Contour-based OPC-modeling has recently arisen as an alternative to conventional CD- based OPC-modeling. Contour-based OPC-modeling is interesting because there is more information about the layout and process that can be generated from one contour rather than hundreds of CD-measurements. Obtaining more information from 2D sites and arbitrary structures would not only be beneficial for accurate modeling but could also save measurement time as it acquires more information in less time.

Hitachi High-Technologies has continued to develop “Technology for generating real contours from SEM-images”. SEM-Contours are generated from the top-down SEM-images by the same algorithms as CD-measurements that are taken automatically using CD-SEM and its recipe. The CD-SEM is able to deliver contours directly in GDS format. There are many key technologies to generate contours accurately. In SPIE2009, a newly developed contour alignment and averaging method was applied to three kinds of basic structures: line/space, contact hole and end-of-line (EOL). The alignment method eliminates rotation errors and XY shifts, and the averaging method minimizes contouring errors and pattern roughness effects. The ‘Measurement Based Averaged Contour’ (MBAC) that had been obtained as a result, was applied to OPC model calibration and verification. It was reported in SPIE 2009, that the effectiveness of MBAC is confirmed for model calibration and verification.

In this study, the application of alignment and averaging was extended from three basic patterns to 2D sites and arbitrary structures. OPC model calibration was done by MBAC in 2D sites and arbitrary structures. Then, the effectiveness of the model calibration by using SEM-contours was examined by doing model verification. The contour extraction accuracy in 2D sites and arbitrary structures was examined as well. The evaluation result of the model quality by using advanced CD-SEM based contours will be reported. It will make the best use of the advantage of the contour-based OPC-modeling in the next generation lithography.

7638-68, Session 14

OPC model error study through mask and SEM measurement error

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Optical Proximity Correction (OPC) is one of the key optical lithography enablers to improve the achievable resolution and pattern transfer fidelity in IC manufacturing. Immersion lithography scanners are now reaching the limits of optical resolution leading to more and more constraints on OPC for increased simulation fidelity. In order to achieve the required accuracy OPC model needs reliable input data for model calibration.

Unfortunately, OPC models often start on spurious basis: as an example, the mask writing errors are currently not taken into account and thus leads to the first mistakes in OPC modelling. Metrology errors such as CD-SEM (Scanning Electron Microscopy Critical Dimension) measurement errors also lead to wrong model parameters causing inaccuracies in model prediction.

In this study, we used a dedicated design of 352 features exposed through a Focus Exposure Matrix (FEM) of 28 defocus conditions and 28 dose conditions. We investigated the mask bias from target for these structures and got an absolute error inferior to 2nm at wafer scale. The mean value is 1nm and the standard deviation 0.7 nm. This mask data error may seem to be small, but it turn out that it has a great impact on model reliability and precision. Another significant contributor to model reliability is SEM measurement error. In order to get insight into this source of modelling error, we compared the SEM measurements to AFM measurements for as much as 105 features exposed in different process conditions of dose and defocus. To find AFM-SEM error tendency through process conditions and features types.

In the paper, we will show that some OPC models try to compensate for such systematic errors by adding non physical fitting parameters in the resist model. In this study, our goal was to identify these errors before model calibration in order to get clean input data. This eventually provides more physical resist model and thus improve the OPC model reliability. We finally discuss on the importance of taking into account these effects in order to improve the reliability of the OPC models for current and future technology nodes.

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7639-01, Session 1

The evolution of patterning process models in computational lithography

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It has been thirty five years since the first lithography process models were presented, and since that time there has been remarkable progress in the predictive power, performance, and applicability of these models to different use models within the semiconductor industry. The impact has been profound, and this paper will attempt to highlight some of the key contributions which have been made, particularly as patterning simulation has moved beyond the realm of process development to full chip production enablement. In addition, this paper will outline the simulation challenges which remain as the industry approaches sub 0.25 k1 patterning. These challenges lie principally in driving towards ever improved accuracy for an expanding set of processes and failure modes, while maintaining or improving full chip data preparation cycle times.

7639-02, Session 1

Materials chemistry for next-generation lithographies

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No abstract available

7639-03, Session 2

Resist material for negative tone development process

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Double patterning process with 193 nm immersion lithography process is one of the candidate for 32 nm half pitch device manufacturing, and the possibility of extension to 22 nm half pitch device is now hot topic in 193 nm immersion lithography evolution. At the initial phase, several kinds of double patterning method were proposed. Today, spacer defined process are now going to be applied to the flash memory devices manufacturing. Freezing process is one of the candidates as cost reduction process of litho-etch-litho-etch (LELE) double line process, and has been studied by material supplier and equipment supplier in the viewpoint of material and process respectively. However, all lithography process of freezing process is positive tone imaging. It is well known that it is very difficult to open narrow trenches below 40 nm with positive tone 193 nm immersion lithography process. Of course it is possible to form a trench pattern with LELE double line or freezing process, however, the trench size depends on the first line size, the second line size, and overlay error of exposure tool, therefore, it is difficult to control trench size not only among wafers, but also across a wafer. This fact indicates that trench pattern should be formed just as trench pattern in one exposure step. However, there was no solution in narrow trench patterning with single exposure process.

Negative tone development (NTD) process has been proposed as one of double patterning method with 193 nm immersion lithography process for 32 nm below half pitch devices manufacturing. NTD process has big advantages for narrow trench and contact hole pattern imaging, since negative tone imaging enables to apply bright mask for these pattern with very high optical image contrast compared to positive tone imaging. Not only single exposure and single development process, but also extended applications were proposed with NTD process. Combination of double exposure with vertical and horizontal line and NTD process was proposed as good candidates for through-pitch and complex array contact hole imaging process. Moreover, pitch frequency doubling can be realized by dual tone development (DTD) process, that is combination of NTD and positive tone development. Although the resist materials for positive tone development (PTD) have been also applied to NTD process, it is supposed that resist materials dedicated to NTD is preferable, since an organic solvent system is selected to NTD process. We have found that larger our first platform resist material has slower dissolution rate at un-exposed area, and higher dissolution rate at exposed area, thus, this resist has smaller dissolution contrast compared to those of PTD process. If dissolution contrast can be enhanced with material optimization, the lithography performance should become much better. In this paper, we will show our recent result of resist material study dedicated to NTD process, and application result examples.

7639-04, Session 2

Double-exposure materials for pitch division with 193 nm: lithography results

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We present an overview of lithography results achieved so far for materials to support “leave-on-chuck” double exposure pitch division patterning. These materials attempt to make use of a non-reciprocal photoresponse in order retain image information well beyond the pitch limit of the lithography tool. Such behavior could be produced, for example, by a reversible two-stage PAG. Accompanying papers in this conference report on both the photochemical details of the reaction pathways of these materials in film, as well as modeling of the kinetics of these reactions and the resulting implications for lithography.

Several stages of lithography testing were done on candidate systems. First, thermal stability and casting behavior were investigated, then single-exposure (SE) contrast curves were run. The purpose of such tests were to determine whether the system behaved as a usable photoresist. The next stage of testing probed non-reciprocal response: does the system show a marked difference if the 193nm dose is received in two installments, versus all at once? These tests were run in the form of double-exposure (DE) contrast curves, possibly with an intervening whole-wafer flood exposure at a longer wavelength (necessary to enact reversibility in many of the systems tested). The key criteria for a material to pass this stage was to show a shifted contrast curve for DE vs SE, eg the photospeed should be markedly different for DE vs SE. From a practical viewpoint, such a shift implies that there should be a dose for which the thickness remaining after DE exposure would be much different than that after SE. Such a thickness difference would then suggest pitch division imaging is possible. We have found at least one system which indeed produces said contrast curve shift.

Following sucessful SE vs DE contrast curve shift, the next step is actual DE patterning. Since the laboratory tool used for these exposures does not have the precise alignment needed to interleave the two exposures for pitch division, we have employed a technique in which the second exposure is rotated slightly with respect to the first exposure. This results in a Moire’-type pattern in which the two aerial images transition from overlap to interleave as one scans across the wafer. Simple modeling confirms that a material with the proper shifted contrast curves should produce pitch division at the interleaved regions.

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7639-05, Session 2

A new materials-based frequency doubling technique

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Several techniques have been recently proposed to obtain higher resolution from 193 nm optical lithography. Most of these techniques require the design of new exposure tools or implementation of costly extra process steps. We now report a study of a new materials-based frequency doubling technique, which would double the resolution of conventional lithography tools. This technique employs a resist system that involves a linked series of photochemical reactions (A Acid B) in which a strong acid is the intermediate species, but a neutral, inert compound is the final product. The intermediate acid accumulates at lower doses, but it is largely consumed at higher doses. At medium doses, the concentration of acid reaches a maximum. This property could, in principle, be utilized to double the frequency of a grating on masks as the maximum of the acid concentration appears on both left and right edges of single lines. A simulation of this process was performed for a 50 nm line and space pattern on mask using PROLITH and customized codes. The results showed generation of a 25 nm half pitch relief image after development. In principle, the process demands a photodegradable acid, which is very rare. Therefore, an alternative resist formulation, consisting of a photoacid generator and a photobase generator, was simulated and discovered to produce acid in the same fashion as the linked mechanism described above. The results of the simulation work and the proposals for candidate materials will be presented.

7639-06, Session 2

The important challenge to extend Spacer DP process toward 22nm and beyond

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Double patterning processes are technique that may be adopted for forming etching mask patterns for the 32nm node, and possible also for the 22nm node. The self-aligned spacer process has drawn much attention as an effective means of enabling the formation of repetitive patterns easily.

Although self-aligned spacer process is utilized in actual device manufacturing at the present, it has many process steps and pushes the process cost. In addition, it makes limited 1D pattern assumption.

In this paper, the extendibility for several device lay-out would be proposed by using enhanced 2D positive spacer process and the demonstration results of newly developed spacer DP process by using1D negative spacer.

- The result of 1D Positive-type spacer like NAND/DRAM gate is shown in Fig-1.
- The result of 2D Positive-type spacer like SRAM gate is shown in Fig-2.
- The result of 1D Negative-type spacer process is shown in Fig-3.

According to those results of Fig-1 and Fig-2, we proved the formation of not only 1D simple pattern but also enhanced 2D pattern by using self-aligned spacer process. We could reconfirm the applied possibility of self-aligned spacer process to 22nm device.

On the other hand, as shown Fig2, we fabricated 20nm half pitch PR pattern through newly proposed "negative-spacer process". This periodical PR pattern can be described in single exposure, therefore, significant cost saving will be enable.

7639-07, Session 2

Carbon-rich spin on sidewall material for self-aligned double-patterning technology

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Double exposure (DE) and double patterning (DP) have emerged as leading candidates to fill the technology gap between water immersion and EUV lithography. Various approaches are proposed to achieve 3x-nm half-pitch dense lines and beyond. DE with two resist processes and double patterning (DP) both require two separate exposures, and they will face very tight overlay margin by the scanner tool. In contrast, self-aligned double patterning (SADP) requires one exposure only, and provides high feasibility for 3x-nm node at this moment. However, a sequential order of multiple non-lithographic steps (film deposition, etch, and CMP) will cause a complicated and expensive process for SADP. Instead of using complicated sacrificial layers, the spacers can directly form at the sidewall of the resist patterns by low-temperature CVD deposition or spin on sidewall (SoS) material coating. In this paper, lower cost-of-ownership of SoS material will be studied for SADP process.

Si-content SoS material was chosen to be developed in the beginning because high Si-content material can meet the requirement as hard mask for etch process. The Si-content material is coated on resist pattern and aimed for chemical reaction with resist acid for getting sidewall as a spacer. However, there are two concerning points of this material and process. The first one is that Si film was remained too much on resist open area because of the reaction with under layer surface. The second one is that it is too difficult to get wider sidewall CD due to the controlled factors like exposure energy and bake temperature are not effective. Therefore, a new polymer system for spin on sidewall process is developed.

In this paper, a novel Carbon-rich polymer is introduced as a spin on sidewall material. It is easy to apply Carbon-rich SoS material for conventional litho film stacks. The sidewall is controlled by cross-link reaction with similar concept as organic BARC. The driving force of cross-linking reaction is acid diffusion from resist and cross-link chemistry between resin and cross-linker. By above system, it was confirmed that sidewall CD was increased over 40-nm without residue on resist open area. The formulation, combination of SoS material and BARC, and process will be discussed in depth. The initial test on wafer will be demonstrated on 3x-nm half-pitch patterning and shown in this paper. Finally, other investigated schemes will be discussed.

7639-04, Session 3

Characterization of line-edge roughness (LER) propagation from resist: underlayer interfaces in ultra-thin resist films

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It has been understood for some time that physical properties of thin polymeric films coated on substrates are dominated by their surface interactions with the substrate. For glassy polymers such as those employed in photoresists, perturbation of bulk properties at the substrate interface may propagate more than 50 nm into the polymer film.1

As semiconductor lithography moves toward pitches below 80 nm, resist films with thicknesses of 100 nm and below will be required. Behavior of these films will become increasingly dominated by their substrate interactions. Numerous previous studies have demonstrated that properties of photoresist materials such as glass transition temperature, acid diffusivity, and imaging behavior change

systematically as film thickness is decreased.2 Recent work in EUV photoresist development has highlighted that substrate materials play a critical role in affecting imaging performance and can improve LER, resolution, and process window.3

In this presentation, we describe another aspect of ultrathin resist behavior, specifically LER evolution along the resist sidewall of EUV resists. We amplify on Foucher's observation4 that LER both increases and becomes less isotropic as the resist sidewall approaches the substrate interface. We observe that the sidewall topography of multiple EUV photoresists is dominated by striated features that originate at the substrate and propagate toward the top of the resist film. These findings are in contrast to observations of isotropic, pebbled roughness of larger resist sidewalls described in previous studies5 and predicted by recently developed stochastic models.6 We detail systematic efforts to reduce these striated structures based on resist and substrate characterization (chemical, AFM, etc.) and engineering of the surface interaction between EUV resists and high-silicon content spin-on hardmask materials.7 We use the results of these studies to assess several hypotheses regarding the origins of the striated structures.

7639-05, Session 3

Mechanistic studies of arylsulfonate photoacid generators (PAGs) for EUV lithography

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One of the requirements of photoacid generators (PAG) in extreme ultraviolet (EUV) lithography is an increase in quantum yield and higher acid generation. Arylsulfonates are a new class of neutral photoacid generators being developed for EUV lithography. These neutral photoacid generators have shown sufficient thermal stability, potential for high loadings in resists, and functionalization to triflates, nonaflates, tosylates or other potential acid producing molecules.

This research focuses on elucidating the mechanism of activation and acid production in arylsulfonate PAGs to improve the overall acid production and photospeed in future PAGs. At this time arylsulfonates are much less potent acid generators than the ubiquitous triarylsulfonium salts. The study focuses on diarylsulfidotriflates such as 1 which have shown great potential with fast photospeeds (relative to other neutral aryltriflates) and straightforward structural tuning. Based on product analysis following pulse radiolysis, DUV photolysis, electrochemical reduction and e-beam exposure, we propose that aryltriflate PAGs can undergo one of two major cleavage pathways (Scheme 1). In the case of PAG 1, one pathway involves C-O cleavage producing triflic acid, CF_3SO_3H, and phenyl compound 2. The other path leads to S-O bond cleavage which produces the weaker triflinic acid, CF_3SO_3H, and phenol 3. The reactivity of PAG 1 is compared to related compounds where varying ratios of C-O vs O-S cleavage products is observed depending on molecular structure. The proposed reaction pathways are used to understand and predict performance of arylsulfonate PAGs in EUV resists.

7639-06, Session 3

Thin EUV resist and underlayer stacks: correlating Tg, surface polarity, density, and image quality

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Traditionally, one of the best ways to improve the resolution of a resist has been to reduce its thickness. Unfortunately, however, the lithographic properties of today's many advanced resists degrade dramatically when coated to thicknesses of < 50 nm. Figure 1 shows how the LER of resists prepared by us (OS1 and OS2) and by commercial resist suppliers degrade in thinner films. This is an important problem, independent of wavelength, which needs to be understood and resolved by the electronics industry so that resists capable of meeting the goals of the 22 nm node and beyond can be produced. More mechanistic investigations into the physical properties of these films are necessary to further understand the imaging degradation in thin photoresist films. We assert that inserting organic underlayers between the resist and substrate with specifically designed physical properties can help improve the overall performance of the resist.

In this work, we physically characterized the glass transition temperature (Tg) of multiple EUV resist systems using thermally programmed ellipsometry and x-ray reflectometry as a function of thickness. The density profiles of these resist systems as a function of thickness was also measured using x-ray reflectometry. The measured Tg's and density's were directly compared to the imaging quality of the resist materials as a function film thickness. A series of organic underlayers were specifically designed to cover a range of glass transition temperatures and surface polarities. The image quality of resist/underlayer stacks as a function of Tg and surface polarity of the individual resist and underlayer materials will be presented.

7639-08, Session 3

Study on approaches for improvement of EUV-resist sensitivity

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Extreme ultra violet (EUV) lithography process is one of the most promising candidates for half-pitch 22nm generation device manufacturing and beyond. In EUV lithography, great evolution of resist materials is as important as that of light source, exposure tool, and mask quality. The important performances required for EUV resist material are high sensitivity, excellent resolution, low line width roughness (LWR), and low out-gassing level. It is well known that there is triangle-tradeoff relation among the performances of sensitivity, resolution, and LWR. A lot of efforts have been paid to make a breakthrough in the tradeoff relation, however, these three performances can not simultaneously satisfy the ITRS roadmap target of hp 22 nm node at this moment. There are some resists satisfying sensitivity (10 mJ/cm2), however, such resists usually showed poor resolution or / and LWR performances. Therefore, the technology for improvement on sensitivity with keeping good resolution and LWR performances is keenly desired.

In this paper, study on approaches for improvement of EUV resist sensitivity will be discussed. It is well known that high chemical amplification efficiency is one of the effective methods to improve sensitivity. Enlargement of generated acid diffusion length at post exposure bake (PEB) step can increase chemical amplification efficiency, however, resolution performance should become worse due to the large chemical blur caused by long diffusion length. This fact indicates that it is important to enhance the chemical amplification efficiency without increase of chemical blur.

Larger acid loading amount can improve sensitivity without chemical blur increase, since larger density of photo acid generator (PAG) results effective secondary electron trapping by PAG cation unit. However, we have found that there's limitation in sensitivity improvement with this method, because the PAG density increase leads decrease on density of EUV light sensitizer that generates secondary electron.

To enhance the efficiency of sensitization to EUV light, and to enhance the efficiency of secondary electron generation are also effective to improve sensitivity. We have found that several low ionizing potential polymer showed high acid generation efficiency with e-beam radiation, however, the sensitivity to EUV of the resist is not as high as expected.

Another viewpoint is de-blocking reaction step. If the reaction efficiency can be enhanced without any acid diffusion length increase, the

sensitivity should be increased. We have found that a generated acid with large molecular size showed less acid diffusion length dependence on temperature compared to the conventional smaller molecular size acid. Higher sensitivity with keeping resolution and LWR can be expected with such large molecular size acid by higher temperature at de-blocking reaction, if the de-blocking reaction efficiency depends on temperature strongly. We have newly designed the large molecular size acid for PAG and appropriate blocking group, and sensitivity improvement with keeping resolution and LWR performance was confirmed by e-beam direct writing patterning. Evaluation results with EUV lithography will be also discussed.

7639-09, Session 3

Polymer photochemistry at the EUV wavelength

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Polymer photochemistry depends on photon absorption, which leads to the production of an excited electronic state of the polymer. If the excitation level is greater than the bond dissociation energy, the excited polymer dissociates into free radical fragments that can then further react to produce chain scission or polymer crosslinking. The energy associated with wavelengths of light commonly employed in lithography gradually increases as the wavelength is decreased, going from 115 to 147 to 182 kcal per mole at 248-nm, 193-nm, and 157-nm respectively. This level of energy can be compared with typical carbon-carbon bond dissociation energies of 90 to 120 kcal per mole implying that significant bond breaking photochemistry occurs.

The insertion of EUV, with a 13.4-nm wavelength, into the lithographic roadmap greatly increases the energy available for deposition into the resist polymer to 2133 kcal per mole. The higher energy associated with EUV coupled with the high molecular absorptivity for most organic polymers at EUV should lead to increased excited state population and higher quantum yields of photoproducts. The pathway in which different polymers respond to this light energy, be it chain scission or crosslinking, will determine in large part the ability of resists designed at 193 or 248-nm to operate as EUV resists.

Polymers representative of those commonly employed in resists as well as some model polymers were selected for this study. Polymer photochemistry at EUV was catalogued as to the effect of absorbed 13.4-nm radiation on a polymer's propensity toward chain scission (s) versus crosslinking (x). In selected cases, the chain scission and crosslinking quantum yields were also compared to those previously determined at 157-, 193- and 248-nm. Quantum yields were determined by following the change in molecular weight, both Mn and Mw, as a function of different absorbed doses, D, by a GPC (gel permeation chromatography) method. Solving Equations [1] and [2] simultaneously allows both s and x to be determined.

Equation 1 1 / Mn,D = 1 / Mn,0 + [s - x] * D / NA

Equation 2 1 / Mw,D = 1 / Mw,0 + [s / 2 - 2 x] * D / NA

In the case where molecular weight decreases, it is important to determine if material outgassing is occurring and whether the outgassing occurs from small molecular weight fragments caused by chain scission or by side change fragmentation. The nature of the material loss was determined for selected polymers where chain scission and material loss are significant. This knowledge can be used to design polymers that minimize undesired photochemical transformations and reduce material outgassing.

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7639-10, Session 3

Analysis of trade-off relationships in resist patterns delineated using SFET of Selete

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The small-field exposure tool (SFET) installed to Semiconductor Leading Edge Technologies, Inc. (Selete) is an indispensable tool for the development of resist materials for extreme ultraviolet (EUV) lithography. In the development of next-generation resist materials, the trade-off relationships between resolution, sensitivity, and line edge roughness (LER) are the most serious problem. Among three requirements, LER is known to be inversely proportional to the chemical gradient. In this study, we investigated line-and-space resist patterns delineated using SFET in terms of the trade-off relationships. By changing the exposure dose and half-pitch of line-and-space patterns, the width of line patterns and LER were measured. The range of half-pitch was 22-60 nm. The exposure dose was changed from 9.5 to 13.5 mJ cm-2 with a step of 0.5 mJ cm-2. The experimental results were analyzed using a simulation on the basis of EUV sensitization mechanisms. The relationships between resolution, sensitivity, and LER were successfully reproduced. On the basis of experimental and simulation results, the reaction mechanisms of chemically amplified EUV resists are discussed.

7639-11, Session 4

Advanced patterning solutions based on the space patterning assisted by double exposure (SPADE)

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We developed two different pattern curing techniques to stabilize first lithography (L1) patterns for the single-etch double patterning process. The first method uses a surface curing agent (SCA) that is coated on top of the patterned surface to form a protective coating layer during the curing bake process. The second method uses a thermal cure resist (TCR) that is cured after hard bake to form an insoluble film.

It was found that the resist curing process with TCR often results in the CD loss with L1 patterns after double patterning. This is probably due to the loss of a leaving group in the L1 resist patterns during the L2 process. Even though the L1 patterns can be cured to form 3D network, it's inevitable to avoid the deprotection reaction within the L1 patterns during the L2 process where L1 patterns are exposed and baked again. In order to minimize the CD loss with TCR, we developed a double patterning primer (DPP) which enhances "positive" interaction between L1 and L2 patterns. While CD loss of 5~6nm is observed without DPP treatment, 10~12nm CD growth was observed with DPP treatment. The L1 CD after double patterning was precisely controllable by post-priming bake process with the rate of 0.3nm/°C in the temperature ranging from 120 ~ 150°C.

Taking advantage of the CD growth with DPP treatment, we also developed a novel shrink process calld "Shrink Process Assisted by Double Exposure" (SPADE). Contact hole CD was reduced by 10~30nm after SPADE and excellent through-pitch performance was observed. SPADE was also used to improve LER/LWR in the formation of smaller trenches. SPADE technology was further extended to contact hole "double patterning" where a second set of contact hole patterns are printed in between the first set of contact hole patterns. Not only CD but also pitch is reduced after double patterning and the original contact hole pitch is reduced by 30% after double patterning. In addition to contact hole double patterning, we will describe advanced patterning techniques using SPADE to print donut shaped patterns and post shaped patterns.

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7639-12, Session 4

Design, synthesis, and characterization of fluorine-free PAGs for 193-nm lithography

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With the demand in the shrinkage of microelectronic feature size of the circuitry integration, dry 193 nm lithography and its immersion extension are the most popular tools to realize feature dimensions below 100 nm. Chemically amplified (CA) photoresist technology, invented by IBM for MUV lithography, had been adopted as the mechanism to generate the desirable patterns by resist exposure, leading to acid generation from photoacid generators (PAGs), thermal acid proliferation and reaction upon post exposure baking, and resist dissolution. Because of the relatively low intensity of 193 nm laser and high binding energy of tertiary esters in photoresist polymer, PAGs were designed to produce very strong Brønsted acid with much higher sensitivity are required to realize such chemical amplification. For these reasons but not limited to the same, onium salts such as, perfluoronated octyl sulfonates (PFOS) and other perfluoronated alkyl sulfonates (PFAS), are generally adopted as PAGs in 193 nm photoresists.

Meanwhile, ever increasing concerns have been raised on the environmental impact of PFOS and PFAS due to their chemical persistency, bioaccumulation and toxicity (PBT). The semiconductor industry has largely reacted to public calls to ban the use of PFOS/PFAS chemicals by taking incremental steps, such as, prohibiting the use of longer and only allowing the use of shorter chain molecules, which are shown to be more readily biodegradable. To further minimize the PBT concerns and solve them once for all, it is a general interest to find environmentally benign PAGs which are free of fluorine atoms (fluorine-free).

Here we describe the design, synthesis and characterization of a series of novel fluorine-free onium salts as PAGs for 193 nm photoresists. When these fluorine-free PAGs are incorporated into resist formulation to replace industry standard PFAS-based PAGs, they demonstrate desirable physical properties such as film forming quality, optical density, thermal stability, photospeed and low leaching content. These fluorine-free PAGs are compatible with both dry and immersion 193 nm lithography tools. When screened against PFAS-based PAGs, their resulting photoresists formulations also demonstrated comparable line width roughness (LWR), process window (PW), good profile, and good resolution at CD of 50 nm under immersion lithography condition. Theses results and the continuous materials innovation at IBM have the potential to benefit the existing environment benign efforts of PFOS elimination in the semiconductor industry, including IBM's Fabs.

7639-13, Session 4

Development of an inorganic-based photoresist for DUV, EUV, and e-beam imaging

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The trend of ever decreasing feature sizes in subsequent lithography generations is paralleled by the need to reduce resist thickness to prevent pattern collapse. Thinner films limit the capability to transfer the pattern to the substrate during etch, obviating the need for a hardmask layer and thus increasing processing costs. For the 22nm node, the critical aspect ratio will be less than 2:1, meaning 40-45 nm thick resists will be commonplace. To address this problem, we have developed new inorganic nanocomposite photoresists with much higher etch resistance than the usual polymer-based photoresists. Hafnium oxide nanoparticles are used as a core to build the inorganic nanocomposite into an imageable phototresist. During the sol-gel processing of nanoparticles, a variety of organic ligands can be used to control the surface chemistry of the final product. The different ligands on the surface of the nanoparticles give them unique properties, allowing these films to act as positive or negative tone photoresists for 193nm or electron beam lithography. The development of such an inorganic resist can provide several advantages to conventional chemically amplified resist (CAR) systems. Beyond the etch resistance of the material, several other advantages exist, including improved depth of focus (DOF) and reduced line edge roughness. This work will show etch data on a material that is ~5 X greater than a PHOST standard. The refractive index of the resist at 193nm is about 2.10, significantly improving the DOF. Imaging data, including cross-sections, will be shown for 50nm lines/spaces (L/S) for 193nm, EUV, and e-beam lithography. Further, images and physical characteristics of the materials will be provided in both positive and negative tones for 193nm and e-beam lithography.

7639-14, Session 4

A silicon-containing resist for immersion lithography

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Immersion lithography enables lens designs with NA greater than 1.0, thus resulting in an increased resolution of optical scanners. While the higher NA allows for improved resolution of smaller feature sizes, it also reduces the depth of focus of aerial images projected onto the resist film. When the depth of focus is relatively shallow, the thickness of the resist film becomes a factor in achieving proper exposure. Thus, thinner resist films may be required for proper exposure at high resolution, but such films often do not yield acceptable overall performance, especially when considering etch requirements for the underlying substrate.

One approach that enables the use of a thinner photoresist film in a higher NA tool is multilayer resist processing. One type of multilayer resist processing uses a bilayer (two layer) imaging scheme by first casting a highly energy absorbing underlayer on the semiconductor substrate then casting a thin, silicon-containing imaging layer (photoresist film) on top of the underlayer. The silicon-containing resist provides good etch selectivity between resist and underlayer for anisotropic dry etch processing, such as reactive ion etch (RIE) using an oxygen-containing plasma.

Protective topcoats are currently considered vitally important for water immersion lithography in preventing the leaching of resist components into water. Therefore, a silicon containing resist used in immersion lithography has to be compatible with current topcoat formulations comprising alcohol solvents (eg. 4-methyl-2-pentanol). But, the silicon containing resists currently available generally are not compatible with such topcoat formulations. Therefore, in order to achieve higher resolution by utilizing a bilayer imaging scheme under immersion conditions, there is a need to develop bilayer resists that are compatible with alcoholic solvents. In this presentation, we will describe such a bilayer resist system with high resolution potential (Figure 1).

7639-15, Session 4

Novel self-assembly strategies for next-generation lithography

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Future demands of the semiconductor industry call for robust patterning strategies for critical dimensions below twenty nanometers.

The self assembly of block copolymers stands out as a promising, potentially cheaper alternative to other technologies such as e-beam or nanoimprint lithography. One approach is to use block copolymers that can be lithographically patterned by incorporating a negative-tone photoresist as the majority (matrix) phase of the block copolymer. Three strategies are presented, one using a styrenic block copolymer designed for 248nm patterning, one based on methacrylate platform suitable for 193nm patterning, and another featuring a molecular glass resist templated by a nonionic triblock copolymer surfactant. In all three of these cases, the self-assembly of the block copolymer only occurs in select areas as defined by photopatterning due to the crosslinking of the matrix phase, while the minority phase is removed cleanly through a variety of simple processing steps. A room-temperature solvent-annealing approach is used to reproducibly gain long-range order in the thin films. Varying affinities of each of the polymer blocks to solvent show the ability to change the morphology of the block copolymer, enabling the ability to “lock-in” one polymer microdomain orientation by crosslinking and “switching” the non-crosslinked areas using a different solvent. Enthalpic interactions such as hydrogen bonding are used to increase the effective segregation strength in the block copolymer, which decreases interface width between the block domains and shows promise to reduce LER. We demonstrate how lithographically patternable block copolymers such as these might fit in to future processing strategies to produce etch-resistant lines, contact holes, and pillars at length scales impossible with conventional lithography.

7639-16, Session 4

Design and development of production-worthy developable BARCs(DBARCs) for implant lithography

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As device scaling continues according to Moore’s Law, an ongoing theme in the semiconductor industry is the need for robust patterning solutions for advanced device manufacture. One particularly attractive solution for implant lithography is the use of DBARC to improve reflection control while still affording an “implant ready” substrate following development.

While developable BARCs have been known for some time they have received little market acceptance despite their potential benefits. For example, in the implant area some of the key concerns in DBARC implementation include limited process latitude in terms of post apply bake and develop time as well as post develop residue. However, recent progress in DBARC performance, has prompted many device makers to revisit DBARC technology for their advanced patterning needs.

In this paper, we report our recent progress in the development of production worthy DBARCs for both KrF and ArF implant lithography. In addition, to general design concepts we will share performance criteria in key areas including resist/DBARC profile integrity, overlapping process window and performance over topography. DBARC Performance will be compared with existing technologies including dyed resist and TARC options.

7639-17, Session 5

Fabrication of dual-damascene BEOL structures using a multilevel multiple exposure (MLME) scheme, part I: lithographic patterning

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The integration of BEOL functional elements such as dual damascene dielectric structures requires a complex and costly sequence of steps that involves the alternating patterning and etching of metal and via levels, accomplished through a combination of imaging and transfer layers composed of either spin-on or vapor phase-deposited materials. Tool and wafer cycle time for processing such layers directly impacts throughput and adds to the mounting cost of high-volume semiconductor nanofabrication. In this work, the conventional via-first dual damascene (DD) patterning scheme is replaced by a cost-efficient Multi-Level Multiple Exposure (MLME) patterning and etching approach. A two-layer positive-tone photoresist stack is sequentially imaged using 193 nm dry lithography, to produce a DD resist structure that is subsequently transferred into an auxiliary dual organic underlayer stack, and then further into a dielectric layer. This novel integration approach eliminates inter-tool wafer exchange sequences as performed in a conventional litho-etch-litho-etch process flow, while simultaneously being applicable to all BEOL layers, ensuring throughput increase. The top and bottom resist layers are chemically designed in such a way that they feature differential solubility in organic solvents making it possible to coat the top photoresist onto the bottom resist layer without intermixing to enable a strict litho-litho-etch processing sequence. Independent registration of the via and metal structures in the bottom and top resist layers is achieved by selective photospeed decoupling of the respective layers, so that the bottom resist is largely insensitive at nominal resist exposure dose for the top resist. Imaging performance evaluation of the newly introduced MLME technology includes the resist materials selection process and their required properties (solvent compatibility, adhesion, photospeed, defectivity), metrology work (correction of via dose bias due to trench exposure, mask error enhancement factor analysis, trench layer linewidth roughness, overlay), as well as outlook for immersion-compatible MLME materials and processes. Image transfer of the patterned DD resist structure into an underlying transfer layer stack and the further into a dielectric layer using Reactive Ion Etching (RIE) followed by electroplating, polishing and electrical testing was also thoroughly investigated and is described in detail in an accompanying paper.

7639-18, Session 5

Multilevel integration of patternable low- material into advanced Cu BEOL

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The continuous down scaling of semiconductor devices, while improving performance and increasing device density, has been increasingly achieved at the expense of higher complexity and manufacturing costs. These highly-complex and high-cost processes are evident in almost the entire semiconductor fabrication process beyond 65 nm technology nodes, from lithography, FEOL, to BEOL. They include replacement gate process for high- /metal gate in FEOL and double patterning in lithography at the 45 nm technology node. In BEOL, the introduction of low- materials at the 90 nm technology node has also significantly increased process complexity due to the need for several sacrificial layers to form dual-damascene Cu BEOL structures. This trend of increasing process complexity is expected to continue in the fabrication of future generations of computer chips.

In this paper, we wish to update our work on a simple, low-cost, novel patternable low- dielectric material concept which was first introduced at the 2009 SPIE Advanced Lithography Conference. A patternable low- dielectric material combines the functions of a traditional resist and a dielectric material into one single material. It acts as a traditional resist during patterning and is subsequently converted to a low- dielectric material during a post-patterning curing process. No sacrificial materials (separate resists or hardmasks) and their related deposition, pattern transfer (etch) and removal (strip) are required to form dual-damascene BEOL patterns. As a result, dual-damascene BEOL structures can be formed with remarkable simplicity and efficiency using this novel approach. We will report on the demonstration of multi-level dual-damascene integration of a novel patternable low- dielectric material into advanced Cu BEOL. This =2.7 patternable low- material is based on the industry standard SiCOH-based (silsesquioxane polymer) material platform and is compatible with 248 nm optical lithography. Multi-level integration of this patternable low- material at 45 nm node Cu BEOL fatwire levels has been demonstrated with very high electrical yields using the current manufacturing infrastructure. Patternable low- materials capable of higher resolution with 193nm optical lithography will also be discussed.

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7639-19, Session 5

Advantages of BARC and photoresist matching for 193-nm photosensitive BARC applications

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As the semiconductor industry approaches smaller and smaller features, applications that previously used top anti-reflective coatings have now begun using developer-soluble bottom anti-reflective coatings (BARCs). However, there are several drawbacks to a wholly developer-soluble system, mainly because many of these systems exhibit isotropic development, which makes through-pitch and topography performance unsatisfactory. To solve this problem, we have developed several photosensitive BARC (PS BARC) systems that achieve anisotropic development. One issue with the PS BARC, as with traditional dry BARCs, is resist compatibility. This effect is compounded with the photosensitive nature of the BARC materials. The acid diffusion and quenching nature of the resists has been shown to have a significant effect on the performance of the acid-sensitive PS BARCs. Some resists contain a highly diffusive acid that travels to the PS BARC during the post-exposure bake (PEB) and aids in clearance. Other resists cause the opposite effect, and the same PS BARC formulation is not able to clear completely.

In order to address the lack of compatibility, the ideal solution is to properly match PS BARC and photoresist performance. Initially, PS BARC formulations were modified with various photoacid generators (PAGs) and quenchers that offered similar chemical behavior as the photoresist's PAGs and quenchers. Various resists were screened and then modified for optimal performance. Optimization of lithographic performance was accompanied by other factors such as residue and developer sensitivity. The resulting system exhibited good dark field/bright field and iso/dense performance with little mask biasing and common depth of focus (DOF).

While this approach resulted in acceptable performance for the 32-nm node, further improvements were needed for decreased residue, PEB sensitivity, and better resolution. The next path of development was to design the PS BARC polymer platform to behave more similarly to the photoresist polymer via matching of the deprotection mechanism and solubility properties. PS BARC platforms were designed with lower activation energy (Ea) protecting groups and various levels of crosslinking/decrosslinking functionality. The various polymer platforms were formulated and tested for desired BARC properties such as solvent resistance, optics at 193 nm, basic contrast behavior, and post-develop residue. Lithography was also performed with several resists of varying activation energies. The best PS BARC candidates had lower Ea than the previous generation, matching trends shown by newer photoresist platforms. Two candidates were selected for optimization, and formulation DOEs were performed individually with a selected resist. Performance of the optimized systems showed considerably lower post-develop residue and better PEB sensitivity along with promising lithographic results with a good common DOF of dense and isolated features. Matching of the PS BARC coinciding with optimization of the resist yields a combination package that is better understood and can easily be incorporated into a lithographic process. As features shrink and more customers begin using PS BARCs, this process will become even more important for decreasing the amount of time chip manufacturers spend on finding the best BARC/photoresist combination for their applications.

7639-20, Session 5

Sub-millisecond post exposure bake by CO_2 laser spike annealing of chemically amplified resists

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Chemically amplified photoresists require a post-exposure bake (PEB), typically on a hot-plate at 100-150°C for 30-120 seconds, to catalytically deprotect the polymer backbone. During PEB, excessive diffusion of the photo-generated acid results in loss of line edge definition, blurring of latent images and changes in the line edge roughness (LER). Both acid diffusion and deprotection are thermally activated processes, with the relative rates affected by the time/temperature profile of the PEB. While hot plate PEB is limited to the seconds time regime, we have instead explored sub-millisecond PEB using a CO2 laser-based scanned annealing system.

Laser spike annealing is primarily used for shallow junction formation following ion implantation. A scanned "line source laser" heats the surface to a controlled temperature (up to ~1400 °C), followed by a thermal quench into the bulk substrate as the line source passes. The profile of such spike anneals can be controlled by beam shape and scan speed between 50 us and ~2 ms.

Several polymer and photoacid generator (PAG) resist systems have been studied under 800 us spike annealing at temperatures estimated between 200 and 400°C. All of the resist systems exhibit remarkable stability at these temperatures - a direct consequence of the short thermal duration. Dose to clear is significantly affected for some resist systems while others are relatively insensitive to the PEB conditions. Quantitative determination of the acid diffusion rates and activation energies were obtained using resist bilayers (PAG loaded / PAG free).

Investigation of the possibility of low dose to size for patterning contacts and resolution of shorter line-end patterns using laser anneal would be explored.

7639-21, Session 6

EUV-RLS performance tradeoffs for a polymer bound PAG resist

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New resist materials and hardware processes are sought to address the resolution, LWR and sensitivity (RLS) performance tradeoffs for EUV lithography. While progress has been made on improving resolution and sensitivity, LWR continues to be a major challenge [1]. LWR has been shown to decrease as acid generation increases in the film through both experiment and simulation [2]. Acid shot noise models appear to mathematically describe the general trend between LWR and acid concentration [3,4]. Historically, these models assume that the initial distribution of photoacid generator in the film is random and uniform. However, our studies at ArF have indicated that PAG segregation can create a non-uniform acid profile through the thickness of a film, especially in thin films with high PAG loadings [2]. Non-uniform acid distributions have the potential to create higher roughness in areas with low acid concentration (like the resist foot). New polymer bound PAG resist systems are being designed to maintain a uniform distribution of PAG as well as control acid diffusion in the resist. These materials are likely to also affect the randomness of the PAG distrbution.

The goal of this work is to use a combination of experiment and calibrated resist models to understand the impact of PAG and sensitizer loading on the performance of a polymer bound PAG resist based processes for EUV lithography. Model resists where PAG and sensitizer loading are systematically varied are used in order to quantitatively study these effects experimentally. Physical simulation models are created for these materials that allow to simulate the effects of loading on the chemistry and physics that is ongoing in the polymer thin films during exposure, deprotection and development.

1 Putna, E. Steve, et al., “EUV lithography for 30 nm HP and beyond: Exploring resolution, sensitivity and LWR tradeoffs” Proceedings of SPIE, Vol. 7273, 2009.

2 Rathsack, Benjamen, et. al., “Resist fundamentals for resolution, LER, and sensitivity (RLS) performance tradeoffs and their relation to micro-bridging defects,” Proceedings of SPIE, Vol. 7273, 2009.

3 Lawson, Richard, et. al., “Mesoscale simulation of molecular glass photoresists: effect of PAG loading and acid diffusion coefficient” Proceedings of SPIE, Vol. 6923, 2008.

4 Biafore, John, et. al., “Statistical simulation of photoresists at EUV and ArF” Proceedings of SPIE, Vol. 7273, 2009.

7639-22, Session 6

Characterization of polymer-bound photo-acid generators: fundamental studies and lithographic performance

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Polymer bound photoacid generators are currently under investigation for use in next generation EUV resists. Binding the PAG anion to the polymer backbone in principle should result in reduced acid diffusion, lower image blur and ultimately higher resolution photoresists. However the performance tradeoffs and the ultimate improvement to resolution are not clear at this time.

Recently we reported PAG - bound resist polymers based on a new triphenyl sulfonium fluoroalkyl sulfonate-containing a methacrylate monomer. We described the synthesis of a low activation ester terpolymer containing this onium salt monomer and the importance of polymer purification to remove unreacted ionic monomers in the preparation of polymer-bound PAGs1. In this report we describe in greater detail the characterization of this and other polymers prepared with bound PAGs. We will present data on measurements of acid diffusion, deprotection chemistry and photoacid volatilization and contrast these results with those obtained from conventional PAG’s . We will also present results from 193 nm immersion, EUV and electron beam lithography.

Reference 1. R. D. Allen et al Photopolym. Sci. Technol. 22, 25 (2009).

7639-23, Session 6

Aqueous and solvent developed negative-tone molecular resists

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EUV patterning for the 22-nm node and beyond require a combination of resolution, sensitivity, and line edge roughness (LER) that is difficult to meet in current resist systems due to the now well known RLS tradeoff. Conventional chemically amplified resists (CARs) based on photoacid diffusion and deprotection reactions provide high sensitivity, but have a number of limitations that negatively affect their resolution and LER. These resists also have additional concerns such as pattern collapse and outgassing that can limit their application for EUV lithography. Over the last year and half, our group has designed, synthesized, and characterized several negative tone molecular resists based on epoxide polymerization and cross-linking (Figure 1). These resist undergo a solubility change by a different mechanism than conventional CARS based on cationic polymerization and cross-linking; this different mechanism allows for high resolution while maintaining good sensitivity and improved pattern collapse. These new resists have shown resolution down to sub-25 nm half-pitch, sensitivity as low as 20 µC/cm2, and LER (3) of 2.3 nm (Figure 2) under 100 keV e-beam lithography. The initial resist formulations were improved through reaction engineering to give a resist formulation that showed 25 nm half-pitch, dose-to-size of 15 mJ/cm2, and LER (3) of 4.0 nm (Figure 3) under EUV exposure at the Paul Scherrer Institute. These resist had excellent performance, but were solvent developed rather than developed using the industry standard aqueous base. To overcome this problem, new resists have been synthesized that are capable of both aqueous and solvent development. Some of these new systems have only one type of molecular glass that contains both epoxide functionality and phenolic hydroxyl groups that provide base solubility and other formulations include two or more different molecular glass compounds, one with the epoxide functionality and the other that is not epoxide functionalized. This paper will discuss the imaging performance of these new resist systems and discuss the effect of changing functionality and structure on imaging and the reaction mechanism. These new resists have a slightly different cross-linking mechanism that can occur by both cationic polymerization and acid catalyzed ring opening of the epoxide by the phenol to create an ether. These two different mechanisms have been compared using infrared spectroscopy and the results will be reported. We also investigated the effects of solvent development compared to aqueous development on patterning performance. Early results indicate that aqueous base development may increase the contrast in these materials which could improve patterning even further (Figure 4). This paper will report on the synthesis and characterization of these new compounds and discuss the different mechanisms in each system. We will also report on high resolution imaging of these systems under EUV and e-beam and compare identical systems developed in aqueous base versus organic solvent.

7639-24, Session 6

Comparison of star and linear-ArF resists

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An oligo-initiator with 8 initiating sites based on the sugar saccharose forms the core of a star shaped photoresist. Three standard ArF photoresist monomers, -gamma butyrolactone methacrylate (GBLMA), methyl adamantyl methacrylate (MAMA) and hydroxyl adamantyl methacrylate (HAMA), are polymerized onto the core using ATRP (atom transfer radical polymerization) and the core-first method. The growth of the star polymer was monitored by periodically removing

aliquots from the reactor for nuclear magnetic resonance (NMR) and Gel Permeation Chromatography (GPC) analysis to determine monomer conversion and polydispersity, respectively. In the molecular weight regime studied, the GPC traces did not show the characteristic recombination peak at conversions of 45% and below. Feed ratios of the monomers were adjusted to achieve a previously reported polymer composition of 50% GBLMA, 30% MAMA and 20% HAMA. Furthermore, following initiation, NMR analysis of the aliquots indicates a steady 50% GBLMA, 30% MAMA and 20% HAMA composition throughout the entire polymer rather than an average overall composition.

The resulting polymer has a 6kg/mol molecular weight, making it significantly smaller in size than most reported star polymers. Its arms are oligomers, (average degree of polymerization is approximately 5 mers). Due to each short chain being tied to the core, rather than attached end-to-end, the molecule has a smaller hydrodynamic radius than that of a linear photoresist control of an equivalent molecule weight synthesized according to the same scheme. Beyond having a smaller size, stars resists may have additional advantages over linear photoresists. As the number of arms of a star is increased, star polymers have been noted to transition from an interpenetrating chain behavior, as is typical for a linear polymer, to a hard sphere behavior in the opposite extreme. Both entanglements and hard sphere behavior can lead to line roughness and there is a possibility of finding a minimum between the two regimes that exhibits reduced roughness. Compared to linear polymers, which expand greatly upon dissolution, star polymers exhibit more mild expansion. Minimizing this expansion from the sidewall into the developer could prevent development damage and lead to roughness reduction.

Preliminary lithographic evaluation is performed using a 100kV electron-beam exposure. Roughness analysis is performed using SuMMIT software from EUV Technology. Wafers are baked with a thermal gradient stage calibrated by IR. This combinatorial method increases the efficiency in determining the processing conditions that result in lowest roughness. Therefore a direct comparison between the minimum roughness for the star resist and control can be achieved. In addition, dissolution behavior is studied using a Quartz Crystal Microbalance to observe differences between the star and linear photoresist.

7639-25, Session 6

Characteristics of main-chain decomposable star-shaped polymer on EUV lithography

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The Extreme Ultra Violet lithography (EUVL) is expected to be the most promising semiconductor fabrication technology for 22 nm node and beyond. It was reported that promoted acid diffusion coefficient at exposed area have a significant impact to maintain the latent image quality in very narrow half pitch region. Main chain decomposition system would be an ideal pathway to realize above idea because it accompanies great molecular weight reduction at exposed area.

We prepared a novel main chain decomposable star shaped polymer (STAR polymer) to confirm the concept. STAR polymer consists of a core unit and several arm units which connect to the core unit with easily acid cleavable bonding.

The STAR polymer showed great molecular weight reduction with exposure and decrease in Tg , regardless of increase in Tg for the linear polymer. This Tg decrease of STAR should affect the acid diffusion coefficient and obtain a promotion of the acid diffusion in exposed area.

Based on the concept, better lithographic property of the STAR polymer than that on linear polymer on EUV exposure has been reported. In this article, changing number of arm connecting to the core unit and length of arm based on PHS unit, STAR polymers having similar but different structure which would show different thermal property were prepared and investigated. Showing thermal property of those polymers, lithographic performance on EUV exposure will be represented.

7639-26, Session 6

Development of EUV-resists based on various new materials

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The development of high-performance EUV resists is still one of top three critical issues in EUV lithography. To accelerate EUV resist development, we have developed the small field exposure tool (SFET) which is linked with a coater & developer track system under chemically controlled environments.

This presentation summarizes the systematic development of new EUV resist platform: the evaluation results of more than 50 numbers of new EUV resists based on various low-molecular-weight materials and fluorine-polymers from resin manufacturers and universities.

It is well-known that calix[4]resorcinarene derivatives are widely used as base resin for molecular resists. Especially, resists based on phenylcalix[4]resorcinarene derivatives show good lithographic performance because of their moderate solubility to a standard developer (aqueous solution of 2.38% TMAH).

Most of molecular resists, however, showed heavy pattern collapse in delineating fine-pitch patterns due to their weak mechanical strength. A molecular resist based on “Noria” derivatives (water wheel-like cyclic oligomer) is considered as a promising material, which has relatively large molecular weight and 24 numbers of hydroxyl group per a molecule, and then is expected to have a good adhesion to substrates and a stiff property to prevent pattern collapse.

“Fullerene” is one of typical nano-carbon materials and has very strong dry-etch durability. Recently, new alkali-developable fullerene derivatives for resist resin materials are synthesized.

An increase in the polymer absorption coefficient is expected to lead to the enhancement of acid production. It was known that the incorporation of fluorine atoms in the EUV resist led to an increase in acid generation efficiency per unit volume.

We will discuss EUV resist performance (sensitivity, resolution-limit, LWR, outgassing, pattern collapse) of promising materials such as phenylcalix[4]resorcinarene, “Noria”, fullerene derivatives, and fluorine contained norbornene polymer. We will scope their potential for 22nm-hp and below.

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7639-27, Session 6

High-resolution positive-working molecular resist attached with alicyclic acid-leaving group

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A new amorphous material, 1,3,5-tris(p-(p-hydroxy-phenyl) phenyl) benzene (THTPPB), was designed and synthesized. An alicyclic acid-leaving group, hyperlactyl vinyl ether (HPVE), was introduced into THTPPB to give a high resolution molecular resist material, HPVETPPB. Harf-pitch (hp) 36 nm line-and-space (1 : 1) positive pattern was fabricated using 100 keV EB with chemically amplified molecular resist based on a HPVETPPB.

As Integrated Circuit feature sizes continue to shrink, high resolution resists have been desired. Molecular resists are expected to high resolution and low line-width-roughness (LWR) resists owing to their smaller molecule size, and narrower molecular weight distributions

than common polymer resists. Additionally molecular resist can easy to synthesize the precisely controlled composition compared with polymers. However, the low molecular weight molecule tends to be crystallized and difficult to form the film. In this study, we have developed a new amorphous material, 1,3,5-tris(p-(p-hydroxy-phenyl) phenyl)benzene (THTPPB), and fabricated the high resolution pattern of chemically amplified molecular resist using THTPPB attached with alicyclic acid-leaving group, HPVETPPB.

HPVETPPB was obtained by the introduction of hyperlactyl vinyl ether (1-Vinyloxy-4-oxatricyclo [4.1.13.8] undecane-5-on) into THTPPB. THTPPB showed high glass transitiontemperature (Tg) and amorphous film can be fabricated by itself. We confirmed hyperlactyl group has higher surface energy than hydroxyl group by measuring contact angles. This result indicates HPVETPPB has a good adhesion property.

Patterning of chemically amplified molecular resist HPVETPPB was carried out as follows: HPVETPPB, a photo-acid generator (PAG) and quencher were dissolved in MMP. The resist solution was spin-coated onto substrates to form thin films. The patterns were exposed with single-line scan of 100 keV EB. After EB exposure, the patterns were post-exposure baked (PEB) at 80 ˚C for 90 s and developed with a tetramethylammonium hydroxide (TMAH) aqueous solution. As a results, the resist patterns of half-pitch (hp) 36 nm line-and-space (L&S) (1 : 1) were fabricated. The positive-working molecular resists based on HPVETPPB have the potential to fabricate high-resolution images of straight L&S patterns with good pattern profiles. This new resist have a potential to be applied for EUV lithography.

7639-15, Session 7

Self-assembled systems for extensible patterning

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No abstract available

7639-16, Session 7

Templated self-assembly of Si-containing block copolymers for nanoscale device fabrication

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Thin films of microphase separated block copolymers, which can form patterns consisting of dense arrays of lines, dots, rings and other geometries, are attractive materials for self-assembled nanoscale lithography. In this work, we discuss nanolithography applications of Si-containing block copolymers, including polystyrene-b-polyferrocenyldimethylsilane (PS-PFS) and polystyrene-b-polydimethylsiloxane (PS-PDMS) diblock copolymers and PS-b-PFS-b-poly(2-vinylpyridine) (PS-PFS-P2VP) and polyisoprene-b-PS-b-PFS (PI-PS-PFS) triblock terpolymers. These materials are advantageous for nanolithography compared to all-organic block copolymers because first, they are characterized by a high etch selectivity and high etch resistance of the Si-containing block, simplifying pattern transfer; and second, they typically have a high interaction parameter, which allows small period features with low edge roughness to be achieved.

We first discuss strategies for templating the self-assembly of these block copolymers to make patterns relevant to electronic devices. For example, the locations of 40 nm period spherical PDMS microdomains were controlled by a sparse array of posts, allowing templating of up to 20 microdomains per post to form large area dot arrays with excellent order. Linear patterns were formed from 20 - 32 nm period cylindrical morphology PS-PDMS templated using topographical posts or steps, to form arrays of straight parallel cylinders with controllable period and orientation, arrays with angles or junctions, or sharply curved, concentric toroidal structures. The overall morphology and period of the block copolymer microdomain arrays can be varied by solvent annealing in mixed solvent vapors. We then discuss the formation of self-assembled patterns with sub-20 nm periods and sub-10 nm feature sizes. Linear features of 8 nm linewidth and 17 nm period with excellent order were obtained from films of PS-PDMS of molecular weight 16 kg/mol which were solvent-annealed at room temperature. Unlike the larger molecular weight block copolymers, which order well under toluene vapor annealing, the smaller period structures must be annealed in a low vapor pressure of a poorer solvent. Finally, we describe pattern formation in PI-PS-PFS and PS-PFS-P2VP triblock terpolymers, to form respectively square arrays of dots and close-packed arrays of rings. In the former case, the square symmetry arrays were oriented within topographical steps and the direction of the axes of the lattice with respect to the step edges was controlled by substrate functionalization.

Patterns were transferred into a range of metals by overcoating the block copolymer patterns with a metal film, then etching back using a combined chemical and physical reactive ion etch to leave a reverse-contrast image. Transfer into silica and into other polymer layers was accomplished using reactive ion etching. Device applications, including the fabrication of interconnect lines, silicon nanowires, patterned media, and conductive polymer sensors, will be described.

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7639-17, Session 7

CMOS process compatible directed block copolymer self-assembly for 20-nm contact holes and beyond

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Conventional lithography technologies have been experiencing costly development to meet the demands for fine feature patterning for device fabrication in the semiconductor industry. So far, there is still no apparent solution for patterning feature sizes beyond the 22nm node. Directed block copolymer self-assembly is an emerging lithographic technique that has been receiving extensive attention due to its simplicity and cost effectiveness for realizing sub-20 nm features, and even down to 5 nm [1]. Furthermore, layout design rules have now evolved to the use of highly regular patterns and double-pattern/double-etch to achieve fine features. Block copolymer self-assembly is compatible with this recent trend since it yields highly regular patterns and can be combined with conventional lithography for pattern alignment. Block copolymer has been previously used for back-gated FinFET [2] and 300 mm wafer manufacturing for airgap formation in BEOL [3] where the self-assembled features were not aligned to any existing features on the wafer. We have demonstrated top-gated field-effect transistors featuring 20 nm contact holes defined by diblock copolymer self-assembly at full wafer level [4]. The self-assembly process is fully integrated with an existing CMOS process flow using conventional tools where the 20 nm contact holes are aligned (registered) by guiding templates defined by coarse conventional lithography to patterns on a previous level. Printing contact holes is one of the key challenges in advanced technologies. Our results highlight the potential of block copolymer lithography for CMOS technologies beyond the 22 nm node. As a further step, we need to extend this technique to pattern multiple-size contact holes for integrated COMS devices at the circuit level. A double patterning strategy can be used to pattern different guiding templates at different levels for self-assembling contact holes with different sizes. We illustrate the use of such a strategy by showing possible guiding templates for the patterning of multiple-size contact holes for a 22 nm node SRAM cell.

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7639-18, Session 7

Directed self-assembly for via patterning

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Limited critical dimension (CD) control is one of the major issues in printing tight-pitch interconnects using optical lithography. Directed self-assembly (DSA), which combines lithographically defined substrates and self-assembled polymers, provides a simple and effective method to improve CD uniformity. The intrinsic size of a self-assembled domain is determined by the block copolymer composition and molecular weight. Therefore, directed self-assembly of block copolymers can be used to produce patterns with both smaller CD and increased CD uniformity relative to the original lithographic pattern. Specifically, we show that self-assembly of cylindrical block copolymer domains within via arrays produces patterns with smaller CD and reduced %CD variation. We investigate the self-correcting behavior of block copolymer self-assembly as a function of the prepattern geometry and block copolymer composition. Quantitative characterization of CD variation reduction and pattern rectification will be presented. In practical terms, the DSA process can increase the effective process latitude and reduce the effective mask error enhancement factor (MEEF) when patterning tight-pitch vias and contact holes.

7639-19, Session 7

Low-molecular weight block copolymer surfactant/additive blends with hydrogen bonding induced phase segregation for use as sub-10-nm lithographic etch masks

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Block copolymer films with a thickness of a single domain layer have been shown to be effective etch masks for patterning features on the order of 10-20 nm. This work focuses on blends of low molecular weight, non-ionic triblock copolymer surfactant (Pluronics, PEO-b-PPO-b-PEO) with polymeric or molecular glass additives that provide access to domain sizes on the order of 10 nm and below. Specifically, hydroxyl or carboxylic acid-containing additives act as an important component of the resist blends by increasing the effective segregation strength between the PPO and PEO segments of the Pluronic surfactant. This increased segregation is a result of the hydrogen bonds occurring selectively between the PEO and additive components. Significant enhancements in the long-range order of the domains can also be attained. SAXS was used to observe the bulk phase behavior of blends of Pluronic surfactants and a phenolic-containing molecular glass, whereas films of these systems were characterized by AFM. Scattering data shows that the overall order and segregation strength clearly depend on temperature and additive concentration, while AFM of monodomain layer films exhibit a clear order-order transition (OOT) with increased additive loading. In addition to altering the phase behavior of the templates, these additives can have the additional benefit of increasing the fluorine-based reactive ion etch (RIE) resistance of the PEO domain, which helps to improve etch contrast between the two block copolymer domains. This contrast is a crucial property of an etch resist at the feature sizes of interest.

7639-28, Session 7

Integration of directed self-assembly into 193-nm lithography

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Directed self-assembly (DSA), which combines self-assembled polymers and lithographically defined substrates, has been considered as a potential candidate to extend optical lithography. Successful demonstrations of frequency multiplication and/or pattern rectification using patterned substrates transferred from features written by electron-beam lithography and EUV lithography have been reported. In order to move DSA from the research stage to a viable manufacturing technology, we seek to integrate DSA with state-of-the-art 193 nm optical lithography in a straightforward and process-friendly manner. In this paper, we discuss our recent progress with various integration strategies using 193 nm photolithography to produce topographical or chemical guiding patterns for DSA. This new ability to use 193 nm lithography to fabricate effective guiding patterns in a straightforward manner now enables DSA to be applied to large areas with conventional tools, opening the door to meaningful wafer-scale characterization of the impact of materials and process parameters on DSA performance.

7639-52, Poster Session

Negative-tone chemically amplified molecular resist based on novel fullerene derivative for nanolithography

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To circumvent the trade-off problems among sensitivity, resolution, and line edge roughness (LER) for nanolithography, novel chemically amplified resist materials must be developed. As feature sizes have been shrunk, nanoscale resist topology such as LER appears as the most serious problem in resist processes. LER control requirement currently approaches polymer size. Therefore, molecular resist technology is expected as material innovation because it can give the possibility of higher resolution and lower LER owing to the smallness in molecular sizes. In this study, we developed negative-tone chemically amplified molecular resist based on novel fullerene derivatives, evaluated the lithographic performance and investigated the effect of acid generator.

Fullerene derivatives were used as a resist matrix. A few kinds of acid generators were examined. Propylene glycol monomethyl ether acetate (PGMEA) was used as a casting solvent. Hexamethoxy methyl melamine was used as cross-linker. The wafers were primed with hexamethyldisilizane (HMDS). Resist solutions were spin-coated onto silicon substrates at 3000 rpm for 30 s to form thin films. Water-soluble conducting polymer (Showa Denko, Espacer) was also spin-coated at 2000 rpm for 60 s before exposure. The resist samples were exposed to 75 kV electron beam after baked at 110.0 °C for 90 s. After the exposure, they were baked in some temperatures for 60 s. They were developed in 1.36 N tetramethylammonium hydroxide (TMAH) solutions for 30s and rinsed in water before drying. Resist patterns were recorded with a JEOL JSM-6335F SEM.

When the fullerene derivative resist containing 10wt% triphenyl sulfonium triflate (TPS-tf) and hexamethoxy methyl melamine was used, a semi-isolated pattern with the line width of 60 nm (pitch: 500nm) was delineated. In addition, this pattern shows high aspect ratio (~6) with 60nm line width. Fullerene derivative resists are promising candidates for the resist material for nanolithography such as electron beam and extreme ultraviolet lithography.

7639-53, Poster Session

Nonchemically amplified resists for 193-nm immersion lithography: influence of absorbance on performance

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Non-chemically amplified resists (non-CARs) have recently been reintroduced as an alternative to CARs in an attempt to overcome line edge roughness (LER) and resolution issues to achieve high quality patterning at the 32 and 22 nm nodes. Unlike CARs, which operate by a polarity solubility switch, CARs function through a chain scission mechanism that results in a molecular weight-based solubility switch. The likelihood of a successful non-CAR platform has been significantly increased with the promise of ArF lasers with higher power levels. However, the sensitivity of non-CARs must be greatly enhanced to make them commercially viable. Our initial research has highlighted the importance of thin film effects in increasing the sensitivity of non-CARs. Furthermore, we have explored a range of polymer backbones for use in non-CARs.

In this presentation, we will report on the effect of increasing the absorbance of the resist on the performance of a variety of non-CARs, which include polysulfones and polycarbonates. Initial results have been promising. Significant increases in sensitivity have been achieved by increasing the absorbance of the resists in a controlled fashion.

7639-54, Poster Session

PBG/PDQ study for high-resolution photoresist application

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As the critical pitch continues to shrink for advanced technology nodes and the EUV tool is not yet mature, the demand for ArF high-contrast resist becomes stronger than ever. In this paper, we discuss the impact of photosensitive quenchers to lithography performance. Two types of photosensitive quencher, photo-base generator (PBG) and photo decomposable quencher (PDQ), are studied for its ability to extend the life of immersion ArF lithography. With conventional photoresists using conventional quenchers, the aerial image was substantially linearly transferred to the acid image of the photoresist stimulated by photo acid generator (PAG). The new PBG or PDQ serves as one additional photosensitive component. Such photosensitive quencher changes its base level after exposure. Thus, it modifies the aerial image for better imaging performance. We will present and discuss the imaging results from various formulations of photosensitive quencher and concentration. The defect performance of these new approaches will also be characterized.

7639-55, Poster Session

The optimizations of resist shrink process using track-based technology

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The development of double patterning processes/schemes are widely in progress for 3x nm node and beyond by using 193nm immersion lithography. It is realized that a resist shrink step is necessary in many double patterning process cases due to the resolution limit of the 193nm immersion exposure tool.

As the development work progresses into the mass-product transition phase, the requirement for technical performances has become more difficult to be achieved by existing resist shrink technologies. What are some of the difficulties?

In order to overcome these difficulties, we have developed “Wet Slimming Process” based on our Track technologies including the platform. The process is optimized for CD uniformity and defectivity. The process also has good robustness to the various possible resist materials and/or exposure conditions used by industry.

In this paper, we introduce the scheme of Wet Slimming Process together with basic performance data such as CD controllability, CD uniformity, defectivity and I-D bias. The evaluation data on actual double patterning processed wafers is reported as well.

7639-56, Poster Session

Dependence of 20-nm C/H CD windows on critical process parameters

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20 nm contact hole (C/H) patterning is applicable for sub-22 nm technology node logic applications or next generation non-volatile memories. Dependence of C/H CD window on critical process parameters is important for process stability and repeatability. Post applied baking (PAB) condition, resist thickness, develop time, and dry etch rate are considered to be the most important process parameters for e-beam chain scission resist ZEP520A C/H patterning. In this paper, PAB temperatures (TPAB) are investigated at temperatures (1) lower than glass transition temperature (TG), (2) of TG, (3) just starting to reflow (TF), and (4) much higher than TF. Effects of these process parameters on 20 nm +/-10% C/H CD window for various pattern densities and e-beam doses are studied. The critical process parameters are determined by their effects on CD window size, C/H sidewall profile, proximity effect immunity, CD/ Dose slope, and etch selectivity.

Experimental results are summarized below. Thinnest ZEP520A film has the largest 20nm +/-10% CD window on D-D plot (first D : density of pattern, second D : e-beam dose) for various L/S ratio and dosage. Dosage window of smaller C/H CD is larger. Proximity effect is negligible for 50 nm ZEP520A baked at 200 oC/300 sec. No apparent effect is found in CD window on D-D plot for develop time as short as 30 sec. PAB condition affects CD window most significant than the other process parameters by determining resist density and polymerization which affect e-beam scattering and chain scission in resist film and therefore affects CD resolution and window.. PAB condition of 140 oC/60 sec is most desirable due to largest CD window on D-D plot, straight C/H sidewall profile, lowest dry etch rate and weak proximity effect.

In summary resist thickness and PAB condition are the most critical process parameters for determining the CD window on D-D plot for 20 nm C/H. ZEP520A thickness of 50 nm with PAB condition of 140 oC/60 sec are most promising.

7639-57, Poster Session

Orthogonal lithography

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Photolithography has proven to be a high-resolution and high-throughput patterning method with excellent registration capabilities. However, the emerging field of organic electronics has been largely unsuccessful in adapting this well-established method as a viable approach to patterning, due to chemical compatibility issues between organic materials and the processing solvents and chemicals required by photolithography. This challenge has led us to identify a set of non-damaging processing solvents and to develop alternative imaging materials in order to extend photolithographic patterning methods to organic electronics.

We have identified segregated hydrofluoroethers (HFE) solvents as chemically benign to organic electronic materials and which are also suitable as processing solvents. We refer to these fluorous solvents as orthogonal in that they do not considerably interact with traditional aqueous and organic solvents. Multi-layered devices are easily realized by exploiting this orthogonality property; subsequent layers are deposited and patterned without damaging or otherwise adversely affecting previously deposited underlying layers. We have designed and synthesized new negative-tone photoresists, which are processible in

these solvents. We have shown these photoresists to be patternable under both 365 and 254 nm light, giving submicron resolution. Furthermore, we demonstrate the capability of the orthogonal properties of the system by patterning a multi-layer RGB passive matrix OLED employing these new photoresists and processing solvents.

7639-58, Poster Session

Grayscale lithography process study applied to zero-gap microlenses for sub-2-μm CMOS image sensors

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Microlens arrays are used on CMOS image sensors to focus incident light onto the appropriate photodiode and thus improve the device quantum efficiency. A common and well-known method to manufacture refractive microlens is the thermal reflow technique. This method consists in forming resist patterns using a conventional lithographic step with a binary mask and then melting them so that surface tension causes them to adopt hemispherical form. Several issues have been reported with such process. Among them, as the device CD shrinks, the space between microlens has to be kept to prevent lens merging during the melting step. It is also function of the lithographic process resolution capability and thus becomes more and more detrimental to the image sensor performance. Consequently zero-gap microlens processes have to be developed.

One elegant solution to perform zero-gap microlens is the use of a grayscale reticle with multiple, discreet “gray levels” which locally modulate the UV light intensity, allowing the creation of a uniform profile in the resist layer after development. This approach will rely on the accuracy of the resist development rate as a function of the exposure dose. This means that contrary to conventional photoresists for which high contrast are appreciated to achieve straight resist pattern profiles, we will be looking for very smooth resist contrast curve.

In this work, we will first discuss the resist requirements to obtain zero-gap microlens with grayscale lithography. The strong correlation between resist behavior, characterized by the resist contrast curve and grayscale mask design will be outlined.

Then, process parameters such as substrate type, developer normality, bake conditions and resist thickness will be considered to evaluate the process latitude of such lithography technique. Microlens shape variations as a function of proximity effects has been also considered.

Finally, the performance of the grayscale microlens process has been measured and compared to conventional zero-gap microlens techniques on sub 2um pixel devices.

7639-59, Poster Session

Improved thermalflow characteristic resist optimized for the manufacturing of microlenses

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CMOS image sensors and imager technology employ microlens arrays. Microlenses focus incident light onto the optically sensitive area of the pixel. Increased device efficiency can be achieved by increasing the focused light intensity and reducing the focal distance to the pixel. The gathering power of the lens depends on its spherical shape, which is proportional to the contact angle of the lens and the substrate. A new photoresist is introduced in this paper, which was optimized for improved thermal flow properties suited for microlens fabrication. This resist is capable of producing semi-spherical lenses with higher contact angle, at lower temperatures than conventional resists. This resist is identified as 40XT-M in this paper.

A common method for microlens manufacturing is to thermally flow resist structures printed on the wafer. Typically resist cylindrical or squared post structures are flown to form spherical shapes. These patterns are then transferred to the Si substrate using controlled dry etch techniques. Conventional i-line/g-line positive resist products have been used successfully in this process due to their lower thermal flow temperatures compared to negative resists.

Conventional i-line/g-line positive resists are based on novolak / diazonaphthoquinone (DNQ) chemistry. Although novolak glass transition temperatures (Tg) are typically below 130°C, most resists had to be heated at or above 180°C to form the desired lens shapes. This is caused by the resist thermal interactions of its components at elevated temperatures. Partial novolak crosslinking is formed during this process, causing progressive increases it the resist flow temperature. This limits the ability to fully flow the resist structures to form semi-complete spherical shapes. Surface wrinkling and similar defects are commonly observed at less optimum process conditions. The complexity of the re-flow method is primarily attributed to the novolak / DNQ resist chemistry, which gives rise to two competing mechanisms: a) resist thermal flow, reducing its surface tension and viscosity and b) resist crosslinking, which drastically increases resist viscosity, hindering microlens formation(1).

40XT-M is a newly developed chemically amplified (CA) i-line positive resist. This resist chemistry is designed to re-flow the resist structures below its Tg temperature while eliminating all thermal crosslinking mechanisms. Spherical lenses having greater than 90° contact angles were demonstrated with 40XTM resist. These lenses were formed by thermally flowing squared resist posts, 50μ and 80μ in size printed in 48μ resist thickness at 120°C. This also demonstrates the ability to produce a range of less spherical lenses, (less than 90° contact angles), if desired, using lower aspect ratio structures flown at 120°C or higher temperatures.

(1) S. Audran, B. Faure, B. Mortini, C. Aumont, R. Tiron, C. Zinck, Y. Sanchez, C. Fellous, J. Regolini, JP. Reynard, G. Schlatter and G. Hadziioannou, Proc. SPIE, 6153, 61534D-1(2006)

7639-60, Poster Session

Supercritical CO_2 processing of photoresists

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Supercritical CO2 (scCO2) has been considered as an environmentally friendly solvent for photoresist development. It is nontoxic, nonflammable, and inert under most conditions. It also possesses advantages such as liquid-like densities, gas-like diffusivity, and zero surface tension. Although scCO2 is a poor solvent for most polymers, certain fluorine-and siloxane-containing polymers have shown solubility in scCO2. However, the incorporation of fluorine degrades plasma etch resistance, and because of their persistence in nature, fluorinated compounds are coming under increased scrutiny. Some molecular glass photoresists without the incorporation of fluorine and silicon have been designed and synthesized to be processed in scCO2, but most conventional photoresists are insoluble without additives or cosolvents. Previously, negative-tone patterns of 100nm have been developed in scCO2 using conventional photoresists such as ESCAP and PBOCST with the aid of fluorinated quaternary ammonium salts (QAS). In order to make the process more environmentally benign, the elimination of fluorine in the additives is desireable. Therefore, we demonstrate the patterning of conventional photoresists in scCO2 with the aid of flourine free additives.

7639-61, Poster Session

Gap-fill type HSQ/ZEP520A bilayer resist process-(IV): HSQ-rod and HSQ-tip hardening processes

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HSQ island formed by directly e-beam exposure (DE) and wet development is used as a dry etching mask material. HSQ However, the islands with high aspect ratio are susceptible to collapse during wet development process due to surface tension. To improve this, HSQ-rod and HSQ-Tip structures were achieved by dry stripping of ZEP520A after thermal reflow of ultra-thin HSQ (hydrogen silsesquioxane) gap-filled (GF) ZEP520A contact holes (C/H) in previous study [1]. Aspect ratio of HSQ island formed by latter process is higher than that by the former since the latter is without wet develop procedure which tends to washout the HSQ island. In this paper, gap-fill processes followed by a hardening process to prevent bending of HSQ island are studied to form sub-50 nm HSQ islands (rod or tip) with high aspect ratio. Diluted HSQ is used to gap-fill the exposed ZEP520A C/H or C/H after thermal reflow. The hardening processes include high temperature baking and e-beam curing with high beam current. Detail process parameters are shown in Table I.

Experimental results are summarized below. Aspect ratio of GF type HSQ-rod larger than 7 is observed. Bending of GF type HSQ island (rod or tip) with high aspect ratio is also observed. HSQ-rod hardened by high temperature baking tends to fracture. E-beam curing prove to be efficient for HSQ island (rod or tip) hardening and the required curing doses are dependent on HSQ-rod CD. Smallest HSQ-Tip CD hardened by e-beam curing is ~12.5 nm. E-beam curing doses for GF type HSQ islands with CD of 12.5-75 nm are plotted together with e-beam exposure doses of DE type HSQ islands with designed CD of 50-100 nm. It is found that e-beam curing of GF type HSQ island and e-beam exposure of DE type HSQ island has the same effect and mechanism in cross-linking of HSQ molecules to increase mechanical strength (Fig. 2).

In summary high aspect ratio HSQ island can be hardened to prevent bending by e-beam curing (GF type) or e-beam exposure (DE type).

7639-62, Poster Session

LWR reduction by novel lithographic and etch techniques

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With the high integration and densification of the semiconductor devices, line width roughness (LWR) of resist, must be reduced and it must be strictly controlled for the semiconductor device performance and its reliability. According to the road map of ITRS 2007 [1], it is necessary to reduce the value of LWR 3sigma to 2.4 nm (2010) at half pitch (hp) 45nm of the DRAM, LWR 3sigma to 1.5 nm (2014) at hp 28 nm, but this roadmap also states “Manufacturable solutions are NOT known”. Exclusively in extreme ultraviolet (EUV) exposure which has been developing as the 2X nm node technology and beyond, resolution and LWR (and sensitivity) has a contradictory relationship. Reduction of the LWR is one of the critical issues of EUV lithography. Low molecular weight resists have been suggested and developed as one of the LWR reduction possibilities among the resist manufacturers and universities. However, these techniques need innovative improvement to apply to mass-production. So, additional process after resist pattering is expected to be a method for LWR reduction.

In our previous papers [3, 4], the LWR reduction process was introduced. This process is performed after the resist pattern is formed by the developer process, and improves the LWR by smoothing the resist polymer pattern in an organic gas atmosphere (litho-smoothing). Before the litho-smoothing process, vacuum ultraviolet (VUV) irradiates the resist pattern to accelerate the smoothing process. As a result, we reported that value of LWR 3sigma was reduce from 12.2 nm to 9.8 nm (LWR reduction rate: 20 %) at hp 80 nm patterned by KrF exposure [3].

In this paper, the results of the litho-smoothing process using hp 40 nm node resist pattern formed by ArF immersion exposure tool is reported, and also reports dry-etch results obtained by ‘dry-etch-smoothing process’. This process is applied for the BARC pattern and its detail is explained in this paper. Additionally, utilizing litho-smoothing and dry-etch-smoothing processes with stacked wafer (resist, BARC, SiN, poly-Si), the results of the LWR reduction are reported and discussed.

7639-63, Poster Session

193-nm non-CA and low-CA resist systems for reducing LER

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Chemically amplified resist (CAR) have been the workhorse for 248nm and 193nm lithography. As sub-32nm device generations are pursued, there is a concern whether these systems can meet lithography line-edge roughness (LER) requirements. An alternative to reduce the resist contribution to LER is to pursue materials that do not go through a diffusion induced amplification step by exploring photochemical routes with quantum efficiencies close to or less than unity. Although several approaches have shown potential in the past, they have been less attractive when compared to the throughput allowed with CARs, and have thus not been pursued. Some compromise in resist sensitivity may be tolerable for sub-32nm generations by using higher power excimer lasers together with calcium fluoride lens materials, making such options more attractive.

While there is significant understanding of direct photochemical systems for application in the UV and with ionizing radiation (such as e-beam, ion-beam, and X-ray), there has been very little activity in applying these concepts toward high resolution, low LER 193nm nanolithography. By developing systems combining concepts of high resolution scissioning polymers, low amplification photochemical schemes, copolymerized acrylate derivatives, non-CA solubility switching, and other designs and hybrids, we hope to achieve required values for resolution and LER for sub-32nm generations. We will report results on the synthesis and lithographic evaluation of several alternative 193nm resist systems for sub-32nm application including 1) dissolution inhibition (DI) systems involving diazonapthoquinone (DNQ), sulfone, and nitrobenzyl cholate inhibitors/accelerators, 2) photo-Fries and formyloxystyrene (FOxS) systems for 193nm application, and 3) scissioning enhanced low-CAR or non-CAR acrylate co-polymers based on methyl styrene and methacrylate derivatives. The goal is to achieve <200 mJ/cm2 sensitivity in 30-80nm film thicknesses with absorption less than 6 um-1 and LWR below 1.8 nm 3s in a aqueous base soluble system with adequate etch resistance. Details of the systems under study will be described along with contrast data and lithographic performance using interferometric lithography.

7639-64, Poster Session

Process techniques against pattern collapse

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As pattern size is approaching around 38nm, not only lack of process window but pattern collapse becomes a critical problem. Pattern collapse includes falling down, bending, rupturing, etc.

A lot of factors are involved with pattern collapse. For example, aspect ratio of pattern is one of the biggest contributors to pattern collapse. As photoresist thickness decreases, pattern collapse is not likely to occur. However, we can not decrease photoresist thickness as much as we want because it limits etch process window. In real process, a technique which is effective for the prevention of pattern collapse

should not hurt process window. In this regard, decreasing photoresist thickness is not a good idea to address pattern collapse problem.

We will focus on process techniques which are effective for the prevention of pattern collapse without any other side effects. Such techniques include the improvement of adhesion between patterns and substrate, decrease of surface tension of rinse solution during development process and others. In this paper, we will investigate on ways of avoiding pattern collapse by adhesion improvement and low surface tension rinse solution.

7639-65, Poster Session

Further analysis of the effect of point-of-use filtration on microbridging defectivity

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In a 2009 analysis of microbridging defectivity1, a design of experiment methodology was used to show the effect of filtration parameters on microbridging defectivity, specifically focusing on filter retention rating, filter media and design, filtration rate, and controlled filtration pressure. In that analysis it was shown that different filter architectures may provide the most effective filtration of microbridging defects with specifically-tuned filtration parameters. Ultimately, filter choice and filtration setup matter in removal of microbridging defects.

In the new analysis, a similar approach was taken with additional filter types. However, in the new study the retention rating of the filters was kept constant at 10nm and other filter parameters were varied, including membrane material and design. This study will show the specific effect of the membrane material and design on microbridging defectivity in addition to the effects of filtration setup.

1Braggin, J., et al, “Analysis of the Effect of Point-of-Use Filtration on Microbridging Defectivity”, SPIE Vol. 72730S, (2009).

7639-66, Poster Session

Point-of-use filtration methods to reduce defectivity

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While immersion lithography has been rapidly implemented in manufacturing environments around the world, a few defect challenges still remain. Bubble and water mark defects are well understood and have been addressed by equipment manufacturers. However, a few defects still bewilder the lithography community, including residues and microbridging. These defects are difficult to completely eliminate as they may have many root causes. However, through effective point-of-use filtration, they can be greatly reduced.

Point-of-use filtration has traditionally focused on selecting a filter membrane at a specific pore size that is compatible with the resist chemistry being utilized in the process. The research hereby discussed indicates that in addition to these important point-of-use filter choices, careful filtration parameter setup can improve defectivity results and impact the coating process.

7639-67, Poster Session

Fabrication of dual-damascene BEOL structures using a multilevel multiple exposure (MLME) scheme, part II: RIE-based pattern transfer and completion of dual-damascene process yielding an electrically functional via chain

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We have developed an innovative back end-of-line (BEOL) integration process which we call Multi-Level Multiple Exposure (MLME) technique. MLME simplifies the standard BEOL dual damascene (DD) integration scheme while simultaneously being applicable to all BEOL layers. It offers a patterning resolution reaching into the sub-100nm region and increases throughput in large-scale chip manufacturing. MLME employs a custom multilayer pattern stack upon which is spun one layer of via-resist and one layer of line-resist. This process implements a strict litho-litho-etch sequence for transferring the trench- and via-patterns into the dielectric layer. As opposed to conventional state-of-the-art DD processes, MLME performs both lithography steps, i.e. via and trench pattern generation, directly one after the other, and then applies a pattern transfer etch sequence to the lithographically-formed patterns. Hence, MLME does not only decrease the number of overall process steps for the full DD BEOL process but also eliminates several inter-tool wafer exchange sequences as performed in a conventional litho-RIE process flow. We have demonstrated all MLME process steps, i.e. combined 193nm-dry dual-resist layer MLME via- and trench-lithography, full pattern transfer of via- and trench-patterns into the dielectric layer using reactive ion (RIE) etching, as well as electroplating and polishing the DD pattern. Enabling an etch transfer process for patterns created through a dual-resist layer lithography process requires the design of a customized multi-layer stack. This paper provides a detailed description of both post-lithography steps of the DD process for a DD BEOL structure, i.e. (i) the RIE-pattern transfer process with the custom multilayer stack, and (ii) the metallization process completing the DD process for one BEOL layer. Furthermore, we demonstrated and characterized the integration capabilities of the MLME technique by generating an electrically functioning via-chain connecting two neighboring BEOL layers which we fabricated by subsequently performing MLME DD on both layers. A detailed introduction to MLME lithography including patterning characterization data is given in an accompanying paper.

7639-68, Poster Session

Resist residue removal using UV ozone treatment

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In a conventional lithography process, the resist pattern is removed by dry strip or wet chemical etch. The wet chemical etch includes Caros etch and solvent etch. The wet chemical etch process is always combined with the dry strip process to meet the residue process spec. However, in some applications, only the wet-etch process can be used to avoid substrate damage during the plasma step. In this paper, we investigate polymer residue stripping using only solvent as well as solvent in combination with UV treatment. For solvents only, some solvents different from the conventional PGMEA/PGME mixture in polarity, exhibited obvious improvements but the residue strip is still incomplete. When supplemented with UV treatment, the organic residue can be further decomposed and removed completely. The UV we used contains 185 nm and 254 nm wavelengths. Ozone is generated during UV exposure and acts as oxidant. The organic residue is thus decomposed and removed. It has been proven as an effective method to cleave the C-C bond without damaging the wafer substrate.

7639-69, Poster Session

The imaging study of a novel photopolymer used in I-line negative-tone resist

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By copolymerizaion of 2-(2-diazo-3-oxo-3-(4-dimethylamidophenyl) propionyloxy)ethyl methacrylate (DODPEMA), N-methylol methacrylamide (MMAA) and methacrylamide (MAA), a novel photopolymer for negative-tone resist is synthesized and its photolithographic properties are investigated. Since the maximum-absorption wavelength of the photoactive monomer DODPEMA is 356nm and it still has a comparatively large absorption at 365nm (I-line), the copolymer poly(DODPEMA-co-MMAA-co-MAA) is anticipated to be used in I-line single component negative-tone resist. Upon irradiaton, the diazoketo groups wich are in the side chains of the copolymers undergo the wolff rearrangment, affording ketens that react with amido to provide cross-linking photoproducts and a negative image is obtained. The photoinduced reaction of the photoactive polymes is showed below. Because the amido groups are present in the polymer, high sensitivity is expected. This kind of copolymer has great value in I-line non-CARs, TFT-LCD and IC discrete devices processing and the anti-dry etching ability is enhanced by the introduction of the benzene ring. In addition, this copolymer still has protential value in Ultra-violate lithographic plate.

7639-112, Poster Session

Development of spin-on hard mask materials under resist in nano imprint lithography

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Nano imprint lithography is a newly developed patterning method that uses a hard template for patterning micro and nano structures. This technique has many advantages such as cost reduction, high resolution, low line edge roughness (LER), and easy operation. However, resist pilling, defect reduction, higher degree of planarization, higher throughput is not acceptable for the mass production of advanced nanometer-scale devices.

In this study, the new approach of the spin-on hard mask materials under resist in nano imprint lithography was proposed to increase process latitudes, and was evaluated by using step and flash imprint lithography. We expect that our developed spin-on hard mask materials (NIL-UL) under organic resist will be one of most promising material in the next generation of nano imprinting lithography.

7639-113, Poster Session

Post exposure based-properties of CAR resists with different PAGs

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We analyzed the Post Exposure Bake (PEB) properties of resists under different conditions including no exposure bake and analyzed their behavior in relation to different PhotoAcid Generators (PAGs).

The tests consisted in processing the resists with various PEB temperatures (or no temperature at all), bake time and post exposure delay times.

The results showed that the resists would perform also with no PEB and they were sensitive to the delay between the exposure and the develop time.

We tested delay times up to 1 day and observed a relation between resist speed and delay time.

7639-116, Poster Session

Defect performance of a 2X-node resist with a revolutionary point-of-use filter

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In today's competitive lithography market, resist manufacturers are always striving to create a product to meet lithographic challenges while maintaining a low inherent defect level. While bulk filtration used in resist manufacturing removes a majority of the inherent defectivity, point-of-use filtration is still required to ensure that defects are not passed from the bottle to the wafer. As Moore's law drives lithographers to ever decreasing dimensions, resist manufacturers must find new ways of filtering their chemistries to make sure that the smallest defects cannot create the biggest yield detractors. In addition, IDMs must use new innovations to explore point-of-use filtration techniques to protect their valuable patterns.

This paper will show the conditions that can reduce defectivity in an immersion lithography scheme. More specifically, advanced point-of-use filtration techniques, including revolutionary filter membrane technology and advanced filtration settings, will be explored to understand potential 22nm node defect performance. By thinking ahead about the filtration needs of the future, resist manufacturers, IDMs, and equipment manufacturers can all work toward an understanding of the complex nature of filtration, ultimately yielding a new, low defectivity regime at the smallest pattern sizes.

7639-117, Poster Session

Practical results of new filter rating method in sub-30-nm lithography process filter

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As acceptable minimum defect size continuously shrinks with the pattern shrinkage in lithography process, greater demands will certainly placed on the finer pore filter in point of use filtration. Since no reasonable rating method for sub 30 nm filters was available, Pall Corporation has established a new absolute rating method for sub 30 nm filter, which employs gold nanoparticle as a contaminant, inductive coupling plasma mass spectrometry as a concentration detector and dynamic light scattering as a particle size detector. [1] This method was attempted for lithography process filters. As a result, correspondence between the new method and the current method, which employs polystyrene latex beads, was confirmed at 30 nm size which is compatible in both rating methods. Further, nominal 10 nm filter was confirmed to be rated at absolute 10 nm. Additionally, this new method was verified using field data and the results indicated validity from another angle. The method also attempted for market available filters labeled at sub 30 nm, and difference was found between the particle size removed and the labeled size. To address the market needs for finer pore size filter in advanced lithography, new method to indicate precise filter rating is needed. Gold nanoparticle challenge test is a promising candidate.

Reference:

[1] T. Mizuno., et al, IEEE transactions on semiconductor manufacturing, Vol. 22, No. 4, pp. 452-461, 2009

7639-70, Poster Session

Highly sensitive EUV-resist based on thiol-ene radical reaction

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Extreme ultraviolet (EUV) lithography is a leading candidate to meet the requirements of the microelectronic industry roadmap. Development of resist for EUV lithography is one of the most important matters. Chemically amplified (CA) resist systems have been used for the highly sensitive KrF and ArF resist processes and many types of EUV resists based on the CA process have been investigated. In CA resists, diffusion of acids from exposed regions to unexposed regions during PEB treatment is a major contributing factor for the line width roughness and resolution limits. To overcome the limitations, it is a good challenge to develop non-chemically amplified resist materials with high sensitivity. In this study, we have designed negative-tone EUV resist based on thiol-ene radical reactions. Hydroxyl units of poly(4-hydroxystyrene) (PHS) was partially modified with allyl units. The resists consisted with multifunctional thiol compound, allyl-modified PHS and photoradical generator. The resist was developable with TMAH aqueous solution. The sensitivity of the present resists was almost the same (~ 10 mJ/cm2) as reported for the acid-catalyzed CA resists for EUV lithography. Outgassing obtained by a method of pressure rise analysis was lower than that observed for MET-2D resist.

7639-71, Poster Session

Dynamics of radical cation of poly(4-hydroxystyrene) generated in thin film upon exposure to electron beam

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Chemically amplified resists have been widely used as a mainstream resist technology. Electron beam (EB) and extreme ultraviolet (EUV) lithographies have been a promising next generation lithography technique. Acid generation processes in chemically amplified resists for EUV or EB lithographies are different from those for photolithographies, such as KrF and ArF excimer laser lithographies. Because the energy of EUV and EB exceeds the ionization potential of resist material. Therefore, the reaction pass is not a photochemical reaction through the excitation of acid generation, but a radiation-chemical reaction through ionization. The reaction mechanism of acid generation in chemically amplified resists has been reported as follows. When EUV or EB enters resist materials, resist materials were ionized and secondary electrons are generated. Radical cations of resist polymer are deprotonated to form protons. The secondary electrons are thermalized by losing their energy through the interaction with surrounding molecules. Acid generator is decomposed through electron attachment, and then yields a counteranion of acid. However, as for proton generation, details of deprotonation of radical cations are still unclear. The elucidation of the dynamics of radical cation of resist polymer in solid films is important for understanding proton generation.

In this study, we investigated the dynamics of poly(4-hydroxystyrene) (PHS) using pulse radiolysis. PHS used in KrF lithography as a backbone polymer is also a promising material for EUV lithography. The dynamics of PHS radical cation in solid film has not been reported. In the experiment, PHS was dissolved in 1,4-dioxane and casted on a quartz plate to prepare PHS films. The films with approximately 1 mm optical length (film thickness) were irradiated at room temperature. The transient spectra of solid PHS films were observed. The dynamics of PHS radical cations in solid films is discussed.

7639-72, Poster Session

Novel protecting derivatives for chemically amplified extreme-ultraviolet resist

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Extreme ultraviolet (EUV) lithography is the most favorable process for high volume manufacturing of semiconductor devices at 22nm half-pitch and below. Many efforts have revealed that the phenolic hydroxyl groups of polymers are also an effective proton source in acid generation in EUV resists, and the effective proton generation and the control of the generated acid diffusion are required to improve the breakthrough of the resolution - line width roughness - sensitivity (RLS) trade-off. For the development of EUV resists, the novel protecting derivatives were designed. To clarify the lithographic performance of these derivatives, we synthesized the acrylic terpolymers containing these derivatives as model photopolymers and exposed the resist samples based on these polymers to EUV and electron beam (EB) radiation. On the basis of the lithographic performances of these resist samples, we evaluated the characteristics of novel protecting derivatives upon exposure to EUV and EB radiation. We discuss the relationship between the chemical structures of these derivatives and lithographic performances in the view point of the EUV sensitivity and the EB patterning.

7639-73, Poster Session

EUV photoresists by molecular layer deposition of polyurea thin films

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EUV lithography will require photoresists to be less than 50 nm thick and highly homogeneous. Current photoresists may not meet these requirements, leading to research of development of novel resist materials. Molecular layer deposition (MLD) is a powerful method offering Angstrom level control over the thickness and chemical composition of the resist film. As an analogue to atomic layer deposition (ALD), MLD utilizes a series of self-limiting reactions of organic molecules at the substrate. In this study, MLD nanoscale organic resist films are deposited on silica substrates via urea-coupling chemistry of isocyanate and amine functionalities in a layer-by-layer fashion. Ellipsometry measurements indicate a linear dependence of film thickness on number of MLD cycles. The urea linkages are confirmed by infrared spectroscopy, and films are shown to have stoichiometric composition by XPS. We have incorporated a variety of backbones contained within the amine precursors in order to make EUV resists. For example, we have incorporated ketal-based acid-labile groups into the backbone of the polymer film and have shown that after incorporation of photoacid generator (PAG), UV exposure, post-exposure bake and development, the films are cleaved, leading to potential use as photoresists. Moreover, electron beam exposure, mimicking secondary electron effects during EUV exposure has been carried out as well, and nanoscale features have been achieved. Results of applying the oligourea films for advanced photoresist application will be presented.

7639-74, Poster Session

Characterization of the effects of base additives on a fullerene chemically amplified resist

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The continuous drive to improve the performance of microelectronic devices has put ever more demanding requirements onto the lithographic process. In recent years molecular resists have been widely investigated as a route to shrinking the RLS tradeoff that limits current resists. Chemically amplified molecular materials have demonstrated a promising combination of resolution, line width roughness (LWR), and sensitivity. We have previously presented results of a fullerene derivative based three component negative tone chemically amplified resist. This had a sparse feature resolution of 12 nm, a half pitch resolution of 20 nm, sub 5 nm LWR, sub 10 microC/cm^2 sensitivity, and high etch durability. We have also investigated the effects of crosslinker variation on the resist as well as the process latitude, stability, and effects of casting and developing solvents. Here we present further characterization of the resist on the effects of base

additives.

The resist in this study was composed of the fullerene derivative MF07-01, the photoacid generator triarylsulfonium hexafluroantimonate, an epoxy novolac crosslinker, and various base additives. Resist films were prepared by spin coating on hydrogen terminated silicon, followed by a post application bake (PAB). Lithographic patterning was performed with an FEI XL30SFEG scanning electron microscope equipped with a Raith lithography system, and followed by post exposure bake (PEB), and development. Resist sensitivity was evaluated at a beam energy of 20 kV, whilst high-resolution lithography was performed at a beam energy of 30 kV with a current of ~ 30 pA. We varied types and proportions of base additive, and the casting and developing solvents to study the effects on resolution, LWR and sensitivity.

To test base additives the resist was cast with chloroform and developed in MCB:IPA [1:1]. The sensitivity of the resist without base was ~ 15 microC/cm^2. Base was added to the resist ranging from 0.5 - 8 wt%. Addition of 1,8-diazabicyclo[5,4,0]undec-7-ene caused a decrease in resist sensitivity to ~ 40 - 75 microC/cm^2 and a slight decrease of contrast. Other base additives showed no significant effect on sensitivity. The line width and half pitch were not significantly affected by base. Sub 20 nm line width and 25 nm half pitch could be achieved even at high base level. LWR was typically worse in the presence of base additive, although 4-phenylpyridine showed a small improvement in LWR.

7639-75, Poster Session

Study on acid diffusion length effect with PAG-blended system and anion-bounded polymer system

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Extreme ultra violet (EUV) lithography process is one of the most promising candidates for half-pitch 22nm generation device manufacturing and beyond. In EUV lithography, great evolution of resist materials is as important as that of light source, exposure tool, and mask quality. The important performances required for EUV resist material are high sensitivity, excellent resolution, small line width roughness (LWR), and low out-gassing level. It is well known that there is triangle-tradeoff relation among the performances of sensitivity, resolution, and LWR. A lot of efforts have been paid to make a breakthrough in the tradeoff relation, however, these three performances can not simultaneously satisfy the ITRS roadmap target of hp 22 nm node at this moment. There are some resists satisfying sensitivity (10 mJ/cm2) alone, or resolution (hp 22 nm) alone. On the other hand, no resist could achieve the target LWR level of hp 22 nm node (<1.2nm) even if resists are specialized for LWR performance.

In this paper, study on acid diffusion length effect with several resist material will be reported. It is well known that acid diffusion length relates strongly to resolution. Long acid diffusion length leads large chemical blur in the resist film, that results worse resolution performance. Therefore, it is good method to suppress acid diffusion length through the resist process for achieving better resolution performance. There are some method to suppress acid diffusion length, for example, application of low post exposure bake (PEB) temperature, high Tg resist film, large molecular size of generated acid, anion-bounded polymer to generate acid-bounded polymer with EUV exposure, and so on. This time, large molecular size of generated acid and anion-bounded polymer were studied with comparison to some conventional not large molecular size of generated acid and PAG-blended polymer, respectively. The diffusion length of generated acid was directly measured with electrical chemical analysis method or indirectly estimated with the pattern size dependence on PEB time. Lithography performances of resolution, LWR, and sensitivity were investigated with EUV lithography on SFET (Small Field Exposure Tool, at Selete), which has resolution capability of middle twenties nm even with annular illumination. Some consideration on the results of acid diffusion lengths and resolution or resolution-related parameter such as exposure latitude and pattern size differences between isolated line and dense line and space pattern will be discussed. It is well known that the suppressed acid diffusion length leads low sensitivity, since the chemical amplifying efficiency is decreased. Higher loading amount of PAG is one of the method for improving sensitivity, therefore, sensitivity dependence on PAG molecule or unit density in the film will be also discussed.

7639-115, Poster Session

Changes in vertical PAG distribution inside photoresist due to the variation of concentration

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Vertical distribution of PAG inside CA-type photoresist is inferred from X-ray reflectivity (XRR) analysis which gives the information on the vertical electron density profile of thin film. The difference between the density distribution of normal photoresist and pure resin indicates the approximate distribution of PAG. The electron density profile of each film is obtained by fitting method for the XRR results based on distorted wave Born approximation (DWBA) approach. In this study, trends in density distributions varied by concentration of PAG suggest that the inhomogeneous distributions of PAG near the surface or interface of photoresist film occurs due to interactions between PAG molecules and substrate, or polymer resin. Distributions with low concentration of PAG (2~4 wt%) show that the PAG molecules tend to be concentrated near the surface of photoresist, while over-load of PAG (20 wt%) results in the density increase near the interface region.

7639-76, Poster Session

Process parameter influence to negative tone development process for double patterning

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Double patterning process with 193 nm immersion lithography process is one of the candidate for 32 nm half pitch device manufacturing, and the possibility of extension to 22 nm half pitch device is now hot topic in 193 nm immersion lithography evolution. At the initial phase, several kinds of double patterning method were proposed. Today, spacer defined process are now going to be applied to the flash memory devices manufacturing. Freezing process is one of the candidates as cost reduction process of litho-etch-litho-etch (LELE) double line process, and has been studied by material supplier and equipment supplier in the viewpoint of material and process respectively. However, all lithography process of freezing process is positive tone imaging. It is well known that it is very difficult to open narrow trenches below 40 nm with positive tone 193 nm immersion lithography process. Of course it is possible to form a trench pattern with LELE double line or freezing process, however, the trench size depends on the first line size, the second line size, and overlay error of exposure tool, therefore, it is difficult to control trench size not only among wafers, but also across a wafer. This fact indicates that trench pattern should be formed just as trench pattern in one exposure step. However, there was no solution in narrow trench patterning with single exposure process.

Negative tone development (NTD) process has been proposed as one of double patterning method with 193 nm immersion lithography process for 32 nm below half pitch devices manufacturing. NTD process has big advantages for narrow trench and contact hole pattern imaging, since negative tone imaging enables to apply bright mask for these pattern with very high optical image contrast compared to positive tone imaging. Not only single exposure and single development process, but also extended applications were proposed with NTD process. Combination of double exposure with

vertical and horizonal line and NTD process was proposed as good candidates for through-pitch and complex array contact hole imaging process. Moreover, pitch frequency doubling can be realized by dual tone development (DTD) process, that is combination of NTD and positive tone development. Although good process maturity was already demonstrated in the viewpoint of etching property, CDU, and defectivity, we need to study process parameter influence to reduce chemical consumptions and tact time, for minimization of impact to environment and manufacturing cost. In this paper, we will show our process parameter study, especially for the development step parameter.

7639-77, Poster Session

Bottom antireflective coatings (BARC) for LFLE double-patterning process

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Double patterning process using ArF lithography has been developed as one of the most promising candidate for hp32 and beyond, however complicated process flow and cost of ownership are the critical issue for this process. LELE (Litho-Etch-Litho-Etch) is the one of the standard process, but in order to reduce the process and cost, LFLE(Litho-Freezing-Litho-Etch) and LLE (Litho-Litho-Etch) process have been investigated as the alternative process. In these processes, Organic Bottom-Anti-Reflective coating (BARC) is used 2 times with same film in both 1st Litho and 2nd Lithography process. In 2nd Lithography process, resist pattern will be print at space area where exposed and developed in 1st lithography process. Therefore, organic BARC needs to have process stability in Photo and development step to keep good litho performance between 1st and 2nd lithography in LFLE / LLE process.

This paper describes the process impact of 1st exposure and development for organic BARC, and the LFLE / LLE performance with optimized organic BARC will be discussed.

7639-78, Poster Session

Mesh-patterning process for 40-nm hole

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Contact hole pattering is more difficult than line/space patterning as mask error factor is higher in contact hole patterning which has 2-dimensional patterns. As the industry moves towards 40nm node and beyond, the challenges associated with printing contact hole with a manufacturable process window have become increasingly difficult. Current 1.35NA ArF lithography is capable of printing 50nm contact holes at best.

Conventional contact hole patterning processes such as resist reflow, RELACS, SAFIRE are no longer able to be used for sub-40nm contact hole patterns because we need to shrink not only hole diameter but pattern pitch.

In this paper, we will demonstrate and compare the patterning performance of the mesh patterning processes including litho-etch-litho-etch, capping freezing and non-capping freezing process.

7639-79, Poster Session

Advanced self-aligned DP process development for 2xnm node and beyond

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Double patterning processes are technique that may be adopted for fabricating etching mask patterns for the 32nm node, and possible also for the 22nm node. Although several double patterning processes have been introduced such as LELE,LLE and self-aligned spacer process, LELE LLE may still have disadvantage for over lay accuracy. The self-aligned spacer process has drawn much attention as an effective means of enabling the formation of repetitive patterns easily.

In this paper, innovative examination result to fabricate 22nm node pattern would be introduced.

7639-80, Poster Session

Nobel approaches to control photo-resist CD in double-patterning process

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Although Double patterning processes are technique that may be adopted for fabricating etching mask patterns for the 32nm node, and possible also for the 22nm node, the a ration of etching mask pattern have been reduced with scaling. On the other hand, etching durability of photo-resist has not been improved drastically.

In this paper, robust pattern slimming process keeping pattern height would be introduced.

7639-81, Poster Session

Simplified “Litho-Cluster-Only” solution for double patterning

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The most advanced immersion systems currently available are not capable of printing 32 nm 1:1 LS in a single exposure. These systems have a maximum NA of 1.35 resulting in a physical limitation of the resolution to 35.7 nm 1:1 LS (k1 = 0.25) according to the Raleigh equation. The urge to get to smaller feature sizes, which is economically driven, calls for innovative solutions. Several possible solutions are available to print line-space patterns beyond the single expose resolution limit of 193 nm hyper NA systems, e.g. Litho-Etch-Litho-Etch (LELE), Spacer technology, Litho-Freeze-Litho (LFL) and Litho-Process-Litho (LPL).

For both the Spacer and the LELE technology the wafer has to leave the litho-cluster (track-scanner combination) in order to reach the intended dense line pattern. This results in higher complexity of the process and lower throughput. Dual line processes (LFL and LPL) are processed completely inside the litho-cluster and therefore result in simpler processing and improved throughput, which makes these processes attractive for our customer since the costs of a simpler process will be lower.

7639-82, Poster Session

Process performance of novel resist material and novel coater/developer system for cross-line contact hole process

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Double patterning techniques are one of the dominant method to achieve the 32 nm node and beyond and LLE (Litho-Litho-Etch) is strong candidate for double patterning method. Contact hole resolution is limited by the low image contrast using dark field masks. Cross line contact hole process using LLE is applicable to fined contact holes. Contact hole patterns are formed by first Line and space patterns and orthogonal second Line and space patterns. Furthermore LLE process flow should be simple as possible as it can for cost reduction. Thus LLE process without freezing process is ideal one.

As recognized generally, LLE process is a process of resist on resist. The 1st lithography pattern might be dissolved in 2nd lithography resist or developer. Therefore LLE process needs new method to maintain 1st lithography patterns. Novel LLE process gives a solution for pattern maintaining without freezing process. The novel LLE process, "Posi/ Posi process", consists of two different resists and the resist for 2nd lithography has a specific solvent.

About the coater / developer process for LLE, it might be critical than single exposure process. For example, 2nd Resist coatings should not be impacted to 1st pattern and LLE process specific defect and so on.

In this paper, we examine the process performance using latest material for double patterning process, exposure tool and novel coater/developer system. The latest resist materials can form cross line contact hole with good pattern fidelity and CD uniformity. And the improvement of defectivity will be shown using these materials. It will be shown that novel coater/developer hardware is effective on enhancement of lithography performance like CD control and Defect control toward double Patterning technology for 193-nm immersion lithography.

7639-83, Poster Session

Improving CD uniformity for thermal-cured systems in double patterning

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The implementation of double patterning processes in 193 immersion lithography is moving forward. The industry is working hard examining several methods of producing a double pattern image including thermal cure resists and the use of a spin on chemical to cure the layer 1 resist. The thermal cure resist systems require fewer processing steps than the chemical curing process. The result of a good thermal cure process is improved process throughput, reduced chemical costs and reduced process complexity. In either case, the success of the double pattern process relies on the ability of the layer 1 resist remaining inert to subsequent processing steps with excellent CD Uniformity.

The goal of this paper is to break down the required processing steps in a double pattern system with thermal cured resists in order to improve CD Uniformity. The system includes a Layer 1 thermal cured resist and a standard Layer 2 resist. Processing occurs on a TEL Lithius I+ and an ASML XT Twinscan 1900i. The feature of interest is a 42 nm x-Hatch contact hole produced by Horizontal Lines exposed with Layer 1 and Vertical Lines exposed with Layer 2.

7639-85, Poster Session

Double-exposure materials for pitch division with 193 nm: reaction kinetics modeling

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We present simplified reaction kinetics for two approaches which theoretically yield a non-reciprocal production of photoacid. A fundamental result of non-reciprocal acid generation is the production of a spatial photoacid distribution which is a nonlinear function of the total dose received: $a(D1,D2) \neq f(D1 + D2)$. This property is necessary so that different amounts of acid will be produced depending on whether the 193nm dose comes in two installments or all at once, even for the same 193nm total dose. This in turn enables pitch division beyond the pitch limit of the exposure tool without removing the wafer from the chuck. The latter has significant benefits in terms of throughput and overlay.

Two basic schemes are considered: the two-stage PAG, and the PAG enabling scheme. In both schemes, the acid is generated in a two-photon process. In the former, the intermediate state reverses back to the starting state if a second photon is not received. In the latter, the intermediate state converts to an "enabled" state via a non-193nm reaction. This enabled state can then receive a second photon to produce photoacid. Thus, the PAG-enabling scheme does not require reversibility. While the two-stage PAG approach has been reported elsewhere [1,2], we believe this is the first report of the PAG-enabling scheme.

While the both schemes can produce a pitch-divided image, they have very different behavior as a function of various parameters. For example, while the reversible 2-stage PAG approach produces a maximum latent image contrast of 1/3, which then degrades with increasing dose, the PAG enabling scheme theoretically produces a latent image contrast of 1, even as dose increases. This comes at no penalty due to even/odd CD bias.

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7639-86, Poster Session

Development of reverse materials for double-patterning process

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Materials and processes for double patterning using 193nm immersion lithography has been developed for the 32/22 nm node device generations. As for double patterning , some patterning methods have already been reported. For instance, there are LELE (Litho Etch Litho Etch) process and LFLE (Litho Freeze Litho Etch) process. LELE process is complicate and low throughput compared to LFLE process. On the other hand, freezing process and freezing material are needed in LFLE process. Then, we examined the process and the material that was able to form a minute pattern without increasing the number of processes as much as possible.

The following is examined as a fine hole patterning process. At first, the pillar pattern is obtained by the X-Y double line dipole exposure. Secondly, the reverse material is applied on the pillar pattern and the subsequent process (dry etching or wet etching process) converts the pillar pattern into a hole pattern. We examined the reverse process and materials, including Silicon Glass for Etch Reverse Layer (SiGERL),and organic Bottom-Anti-Reflective coating (BARC) which is adequate for reflectivity control, lithography and the etching process.

Keywords: SiGERL, BARC, double patterning, reverse

7639-87, Poster Session

Study of post develop defect on TC-less immersion resist

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This study reports on post develop defect on TC-less immersion resist system. There are major defects on TC-less resist system, for example u-Bridging, Blob and pattern collapse defect, as is well known. Among these defect, we reported Blob and pattern collapse defect could be reduced by Acid rinse involving CO2. However, we also reported there was the difference in the effect for each resist.

In this work, we show the great effective and slight effective case for post develop defect and we discuss the cause of difference in acid rinse effect. We evaluated and confirmed the effect on each resist, pattern, exposed area location, develop process and so on. Furthermore, we made a mechanism of defect appearing based on the analysis of defect components and the measurement of resist surface condition for each develop process.

Finally we show the novel approach to post develop defect reduction on TC-less immersion resist system.

7639-88, Poster Session

Novel topcoat materials with improved receding angles and dissolution properties for ArF immersion lithography

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A topcoat material plays a significant role in achieving technology nodes below 45 nm via ArF immersion lithography. Switching the exposure medium between the lens and the phtoresist (PR) from gas (air, n=1) to liquid (H2O, n=1.44) may lead to leaching of the polymer, PAG, or solvent. These substances can contaminate the lens or cause bubbles, which can lead to defects during patterning. Previously reported topcoat materials mainly use hydrophobic fluoro-compounds and carboxylic acids to provide high receding contact angles (RCA) as well as high dissolution rate to the basic developer. However, RCA and base solubility are in a trade-off relationship as increasing RCA generally results in base solubility. The demand for an improved topcoat material arose since the previously reported materials have insufficient RCA's, causing water-mark defects during high-speed scans. Included in this report are novel polymers with high-fluorine contents, used to produce new topcoat materials with improved dissolution rates (~120 nm/s in 2.38 wt% TMAH) and RCA's (>70o). In addition, a strategy to control the pattern profile according to potential needs of customers was found.

We already tested lots of things like the relationship with hydrophobicity and receding contact angle, dissolution control of top-coat materials, and defect control. As a result, Novel materials (we called the "COFP") were developed. These materials have a strong electron withdrawing group as a structurally, alcohol group's acidity can increase. Beside, electron withdrawing group have increase the fluorine content, we get more hydrophobicity than a HFA (hexafluoro alcohol).

A top-coat material with high RCA and dissolution rate(DR) to the basic developer plays a significant role in sub-45 nm immersion lithography. Novel materials (COFP) were developed that improve on the limitations posed by the previously reported materials. These new materials(COFP) have RCA's greater than 70o as well as DR greater than 1.7 times that of previously reported topcoat materials. In developing these materials, (i) a novel monomer that simultaneously fulfills both hydrophobicity and base solubility was synthesized. (ii) Various hydrophobic additives were used to control the pattern profile according to potential needs of customers. As a result, a clean lithographic profile was achieved at 50 nm resolution. Although these polymers were developed for topcoat materials application, they also have potentials to be used in other applications that require high hydrophobicity and high base solubility, such as in topcoat less PR.

7639-89, Poster Session

Evaluation of next-generation hardware for lithography processing

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Through collaborative efforts ASML Netherlands B.V. and TOKYO ELECTRON LTD. are continuously improving the process performance for the latest hardware for lithography processing . In this work, the CLEAN TRACKTM LITHIUS ProTM -i/NXT:1950i litho cluster was evaluated. The CLEAN TRACKTM LITHIUS ProTM -i has been modified with the newest offering in bake plate technology as well as hardware for defect reduction and edge cut control. The NXT:1950i has a maximum numerical aperture (NA) of 1.35 - the highest in the industry. With airdrag immersion it enables low defect count at high scan speed while the gridplate stage position measurement ensures excellent overlay. In-situ measurement and correction of optic aberrations enable maximum imaging performance for each wafer exposed when imaging at very low k1.

By combining scanner capabilities of enhanced image resolution, unprecedented overlay, productivity performance and focus control with Coater/Developer performance for precise thermal control, defect reduction and total critical dimension (CD) uniformity, the CLEAN TRACKTM LITHIUS ProTM -i/NXT:1950i cluster will address the challenge of single exposure and double patterning and be a cost-effective solution for the 32nm node and beyond.

In this work, process performance with regards to CD uniformity and defectivity are investigated to confirm adherence to ITRS roadmaps specifications . Specifically, process capability and imaging capabilities are tested for 40nm line 80nm pitch with the new bake plate hardware for below hp 3Xnm generation. Additional achievements in performance improvement will be shown with temperature and dose control. For defectivity, the combination of Coater/Developer defect reduction hardware with the novel immersion hood design will be tested.

7639-90, Poster Session

Topcoat-less resist process development for contact layer of 40-nm node logic devices

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ArF immersion lithography has been introduced in mass production of 55nm node devices and beyond as the post ArF dry lithography. Because of existence of water between resist film and lens, we have many concerns such as leaching of PAG and quencher from resist film to immersion water, resist film swelling by wafer, keeping water in immersion hood to avoid water droplet on wafer and so on. We have applied an immersion topcoat process in order to ensure the hydrophobic property as well as for protecting the surface to the ArF dry resist process. We investigate top coat less resist process to improve CoO, the yield and productivity in mass production of immersion lithography.

In this paper, we will report top coat less resist process development for contact layer of 40nm node logic devices. It is important to control the resist surface condition to reduce pattern defects, especially in case of contact layer. We evaluated defectivity and lithography performance of top coat less resist with changing hydrophobicity before and after development. Hydrophobicity of top coat less resist was controlled by changing additives with top coat function introduced into conventional ArF dry resist. However, the hydrophobicity control was not enough to reduce Blob defect compared with top coat process. Therefore we introduced Advanced Defect Reduction (ADR) rinse[1,2] which was new developer rinse technique effective against hydrophobic surface. We have realized Blob defect reduction by hydrophobicity control and ADR rinse. Furthermore, we will report device performance, the yield, immersion defect data at 40nm node logic device with top coat less resist process.

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7639-91, Poster Session

Productivity improvement in the wafer bevel and backside cleaning before exposure

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With the increasingly finer pattern size, the patterning by use of the immersion exposure system is gradually predominating in the

photolithography process. The immersion exposure process, however, carries potential to allow a blocked image: particles adhered to the wafer bevel can be brought onto the wafer surface through a process in the immersion exposure system, which may form a blocked image. In addition, countermeasures against defocus affected by the particles on the wafer backside are consequently gaining more importance with the trend of finer pattern size. These situations indicate that the particle control on the wafer bevel and the wafer backside will become more and more critical.

With the above background, Tokyo Electron Kyushu has developed a module that can simultaneously clean the wafer bevel and the wafer backside. The module was implemented in the immersion process at Inotera Memories, which demonstrated its effectiveness on reducing the exposure errors and prolonging the maintenance cycle of the exposure system. As a result, this has successfully contributed to better production efficiency, details of which this paper will be reporting.

7639-92, Poster Session

High contact-angle fluorosulfonamide-based materials for immersion lithography

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Fluoroalcohol-containing materials have found considerable use in 193 nm photoresists as well as immersion topcoat and topcoat-free immersion resist materials due to their good water contact angles and base-dissolution properties. Trifluoromethanesulfonamide-containing materials are another alternative which have been explored for use in 193 nm photoresist and immersion topcoat applications; however, known fluorosulfonamide materials typically exhibit lower water contact angles than fluoroalcohol materials. In this paper, we report the synthesis of a series of fluorosulfonamide-containing materials with water contact angle and base-dissolution performance that rivals or exceeds that of comparable fluoroalcohol-based materials. An initial assessment of their utility in immersion lithography applications will be presented.

7639-95, Poster Session

Photoresist-induced development behavior in DBARCs

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The 193-nm developable bottom anti-reflective coating (DBARC) platform described in this paper is dependent on the diffusion of photogenerated acid from the photoresist in order to behave as a photosensitive (PS) DBARC. In the absence of any significant photoacid diffusion, the behavior becomes that of a traditional dry BARC. Therefore, selecting the proper photoresist to use in conjunction with this platform is essential in determining whether the platform performs as a PS DBARC or a regular dry BARC.

In instances where the photoresist used has high acid mobility, the DBARC exhibits a passive photosensitive behavior. As such, the DBARC is highly sensitive to acid diffusion, but diffusion into unexposed areas is minimal. Process conditions usually employed to manipulate photoresist performance, such as post-application bake (PAB) and post-exposure bake (PEB), can also be used to adjust the DBARC performance. Furthermore, the performance of these systems can be tuned by the addition of various additives. The potential advantages for this type of chemistry, as opposed to a PS DBARC with a built-in photosensitivity, include improved exposure uniformity across the wafer surface, less sublimation, increased shelf life, broad DBARC bake window, reduced residue after development, and compatibility with a variety of resists.

In instances where the photoresist used has low acid mobility, traditional dry BARC behavior is observed. The BARC film then remains insoluble to developer after exposure and PEB, and is removed by reactive ion etching (RIE).

The work presented in this paper demonstrates the ability of this DBARC chemistry to behave as a dry BARC as well as a PS-DBARC. The BSI.W09008 platform shows good lithographic performance as a DBARC with different resists and has advantages over the previous generations of PS-DBARCs. Lithographic evaluations of BSI.W09008 on a different photoresist platform demonstrate its performance as a dry BARC.

7639-96, Poster Session

Noble design of Si-SOH in trilayer resist process for sub-30-nm logic device

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In hyper NA immersion lithography which has over 1.0 numerical aperture (NA) exposure system, reflectivity control between PR and substrate is key technique to overcome resolution limit. Trilayer resist process, which has two layers of spin-on hard mask (SOH) composed of silicon and carbon, was introduced and applied to various generation of ArF lithography from dry to immersion process. However, lack of adhesion between PR (hydrophobic) and Si-SOH (hydrophilic) can cause pattern collapse problem. Moreover, PR profile was not easily adjusted to optimum shape because some side reaction may be occurred at the interfacial layer between PR and Si-SOH. Herein, we studied how to control interfacial side reaction between PR and Si-SOH layer in Trilayer process. We approached three conceptual items: acidity control to PR, uniformity control of Si-SOH itself, and intermixing control of Si-SOH with PR. First, we checked PR lifting margin with line and space pattern. Although vertical profile was obtained in contact pattern, it was useless if line pattern was collapsed. With first screening tests, we made a conclusion that a major factor for side reaction at interfacial layer was penetration of proton into Si-SOH layer produced exposed region. To solve that problem, intermixing control of Si-SOH with PR was the best solution. We introduced network structure formation with Si-O-Si bond by cross-linking catalyst. AFM and contact angle data showed improved surface morphology. We could obtain improved pattern profiles with several PR samples. This result can be optimized to various generations of ArF immersion lithography and further more.

7639-97, Poster Session

Process optimization consideration for 193-nm developable bottom antireflective coatings (DBARCs)

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Developable anti-reflective coatings (DBARC) are an emerging material technology. The biggest advantage of DBARC is that it eliminates the plasma etch step thus avoiding any concerns of damage to the plasma sensitive layers during implantation. In addition, DBARCs also help in addressing scum related defect issues.

We have extensively studied 193nm DBARCs in view of various processing factors. The influences of the thickness, baking temperature, development condition, priming, substrates, prewet and delay time on lithographic performance are discussed and process guidelines are proposed. This paper includes detailed simulation, DBARC contrast curve analyses, and recent dry and immersion exposure results of DBARC.

7639-98, Poster Session

Improving material-specific dispense processes for low-defect coatings

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Minimizing defects in spin-on lithography coatings requires a careful understanding of the interactions between the spin-on coating material and the filtration and dispense system used on the coating track. Two types of spin-on bottom anti-reflective coatings (BARCs), a silicon hardmask and a wet-developable BARC, are examined for their interaction with polyamide, UHMWPE (UPE), and Teflon® filtration media in an Entegris IntelliGen® Mini dispense system. In addition, a new method of priming the filter and pump is described which improves the wetting of the filter media, preventing bubbles and other defect-generating air pockets within the system. The goal is to establish plumb-on procedures that are material and hardware specific to avoid any defect problems in the coating process, as well as to gain a better understanding of the chemical and physical interactions that lead to coating defects. Liquid particle counts from a laboratory-based filtration stand are compared with on-wafer defects from a commercial coating track to establish a correlation, and allow better prediction of product performance. This in turn will provide valuable insight to the engineering process of product filtration and bottling at the source.

7639-114, Poster Session

Accelerating the dual-damascene process time by new filling material

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Dual Damascene technique has been widely applied to IC device fabrication in copper interconnect process. For traditional via-first dual damascene application, a fill material is first employed to fill via to protect over-etching and punch-through of the bottom barrier layer during the trench-etch process. Etch-back process is then applied to remove excess overfill thickness and maintain a greater planar topography. To get better CD control, a thin organic BARC is finally coated to reduce reflectivity for trench patterning. It is a multi-step and costly dual damascene process.

In this study, a new gap-filling BARC material with good via fill and light absorption features was adopted to explore the via-first dual damascene process by skipping etch-back and BARC coating steps. The results show not only the reduction of process cycle time and cost saving but also the CP yield improvement based on data from pilot production of 0.11/0.13 µm logic device.

7639-99, Poster Session

Developments of new phenyl calix[4] resorcinarenes including carboxy groups and phenolic hydroxy groups: their application to positive-tone molecular resists for EB and EUV lithography

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One of the critical issues for the 32-nm rule and below is Line Edge Roughness (LER). The LER of previous resists are 3 to 4 nm, so LER reduction has been hoped. However, manufactuable solution is not known. Early solution is expected.

The previous resist materials were polymer. However, the polymers have large molecules, the polymer chains get twisted up each other, and these compositions are non-uniform, so it is difficult to reduce the LER. It is expected to be a smaller size of molecular and to form a uniform matrix are regarded as one of the method for the developments of resist materials for resist patterns with small LER.

Therefore, we have developed new molecular resist materials based on phenyl calix[4]resorcinarenes containing carboxy groups and phenolic hydroxyl groups. These compounds were synthesized from resorcinols and aromatic aldehydes including alkoxycarbonyl groups. These compound showed high solubility in both resist solvents such as propylene glycol methyl ether acetate (PGMEA), propylene glycol monomethyl ether (PGME), cyclohexanone and conventional alkaline developer of 0.26N TMAH aq.. These compounds possessed good amorphous characteristics suitable for preparing fine uniform resist films. There was no remarkable glass transition temperature (Tg) and melting temperature (Tm) below 250 degrees Celsius in DSC profile of these compounds. Their high performances as molecular resist materials were due to asymmetric structures and calixarene typed ring structures of these compounds. Furthermore, these compounds have two kinds of alkaline soluble groups, carboxy groups and phenolic hydroxyl groups. They are expected to control the protected position and number using the difference of reactivities between carboxy groups with protecting reagents and phenolic hydroxyl groups with them.

These phenyl calix[4]resorcinarenes are applied for positive-tone molecular resists for EB and EUV lithography. The positive-tone molecular resist systems using phenyl calix[4]resorcinarenes of carboxy groups with acetal typed protections were evaluated by EB Lithography. Sub 50nm line and space pattern were resolved.

We will present the EUV patterning results using the small field exposure tool (SFET).

7639-100, Poster Session

All-dry processible molecular glass photoresists for high-resolution lithography

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A new class of molecular glass (MG) resists has been designed and developed for all dry processing conditions. This method has completely eliminated the need for solvent in the lithographic process. These phenolic cores have been functionalized with methoxy moieties, as well as chloromethyl substituents that will crosslink upon E-beam exposure. MGs have been deposited via physical vapor deposition (PVD) onto silicon wafers. PVD deposits a uniform film of controlled thickness free from impurities that are introduced by spinning solvents used in traditional spin coating methods. These impurities have been known to contribute to decreased resolution upon patterning. The high temperature bake after exposure decomposes and drives off the uncrosslinked molecules, leaving negative tone patterns. Since these molecules are self-crosslinking, issues such as increased line edge roughness (LER) from acid diffusion have been eliminated. Comparison of the lithographic performance of these molecules processed with and without solvent is discussed.

7639-101, Poster Session

Molecular glass positive i-line photoresist materials containing 2,1,4-DNQ and acid labile group

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Molecular glass photoresists are low molecular-weight organic photoresist materials that readily form stable amorphous glasses

above room temperature. They can lead to high resolution patterns with lower line edge roughness. Recent years increasing attention has been given to molecular glass resist materials. In this paper, maleopimaric acid, cycloaddition reaction product of rosin with maleic anhydride, was reacted with hydroxylamine and then further esterified with 2-diazo-1-naphthoquinone-4-sulfonyl chloride to give N-hydroxy maleopimarimide sulfonate. The carboxylic acid group of the compound was then protected by the reaction of this compound with vinyl ethyl ether and dihydropyran. Thus obtained compounds were amorphous and have high Tg. When irradiated with i-line light, the 2,1,4-DNQ group undergo photolysis not only to give off nitrogen gas but also generate sulfonic acid which can result in the decomposition of acetal groups at room temperature. So, a novel chemically amplified positive i-line molecular glass photoresists can be formed by the compounds. The lithographic performance of the resist materials is being evaluated.

7639-102, Poster Session

Novel molecular glass photoresist materials for next-generation lithography

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Molecular glass resist is one of the most expected candidate for next generation lithograpy, due to its high resolution and small line edge roughness properties. Many of compounds are synthesized, but there is no compound that satisfies expected properties.

In this study, we synthesized a series of adamantine-phenol compound, protected with acetal group. These compounds show high solubility for common resist solvent, for example, PGMEA, PGME, CHO. They show no significant glass transition temperature or melting point less than 150 degree C in DSC analysis, and amorphous thin film can be formed by conventional spin-coating method. And they can be easily decomposed by acid generated from photo acid generator, and become soluble in alkali developer. Chemically amplified positive tone resist was prepared with adamantine-phenol compound, PAG, base, and solvent. Lithographic properties of these compounds are now under evaluation.

7639-103, Poster Session

Non-traditional resist designs using molecular resists

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Conventional chemically amplified resist (CAR) designs are unable to obtain the combination of resolution, line edge roughness, and sensitivity required for 22 nm node patterning and below. These conventional CAR designs consist of a resist matrix with protected base soluble sites are loaded with a few percent of photoacid generator (PAG) that generates photoacids which diffuse and react to deprotect the base soluble sites. While the photoacid diffusion is the key to the high sensitivity, it is also the cause of many of the problems in these resists. We propose five different new resist designs which can potentially overcome these problems, four of which will be discussed in this paper (Figure 1); negative tone resists based on epoxide cross-linking will be discussed in another paper. While some of these concepts have been previously investigated using polymers, we have found that molecular resists provide an excellent platform to directly compare performance, and can show superior performance to a similar polymer. One design concept is the use of single component molecular resists. This approach uses a single molecule with all the functionality required to act like a CAR; protected base soluble groups with a covalently attached photoacid. This approach eliminates component segregation and inhomogeneity which increases LER and also allows imaging with very high photoacid concentration to improve LER. Early designs have shown low LER of 3.9 nm while maintaining good resolution of sub-40 nm with no base quencher (Figure 2). Non-chemically amplified (non-CA) resists such as PMMA, HSQ, and some calixarenes have shown superior resolution and LER to CARs, but at the cost of very high sensitivity. The second design concept is the use of molecular resist dissolution inhibitors that use photo-sensitive protecting groups that become dissolution promoters after photolysis. An early set of formulations using this approach has shown adjustable dose-to-clear down to 1 mJ/cm2 and contrast ratios up to 8.3 under 248 nm exposures (Figure 3). High resolution patterning is underway. The third design concept is the use of molecular resists that are fully cross-linked in a processing step before exposure and cleaved by acid catalyzed reactions during the PEB. The fragmentation of the cross-linked film should increase the diffusion coefficient of the photoacid in the highest dose region, but the unexposed, cross-linked film should have very low photoacid diffusivity. The cross-linked unexposed film should also be more mechanically robust to improve pattern collapse. The fourth concept is the use of photoacids that have two or more PAGs attached to them. These act like photoadjustable diffusion coefficient photoacids; when only one PAG has been activated, the photoacid has a very low diffusion coefficient that rapidly increases when the second PAG on the photoacid has been activated. This should act like an aerial image contrast enhancement mechanism that improves the RLS performance. The performance of compounds from each of these four design concepts will be discussed and compared to determine which approach or combination thereof is the most promising for obtained the desired performance.

7639-104, Poster Session

Investigation of alternative resist designs using a mesoscale resist model

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As feature sizes continue to shrink to 32 nm and below, it is clear that resist designs must also advance to improve or overcome the RLS tradeoff. A number of different resist designs have been proposed by our group and others as a means to improve the RLS tradeoff, e.g. single component resists, acid amplifiers, etc. Deterministic modeling of resist physics and behavior has been used to improve process development and predict the effect of exposure tool and process changes on lithographic process performance, but it is no longer sufficient for complete modeling of resist behavior at the length scales of interest and with these new resist designs. This is especially clear when investigating line edge roughness (LER), as the movement and properties of individual molecules can greatly effect LER. The non-deterministic behavior of these individual molecules, e.g. random walk diffusion, must be taken into account. We have previously discussed the development of a three-dimensional mesoscale resist model that is a kinetic Monte Carlo simulation of all pertinent resist physics (Figure 1). The 3D model produces LER values that are consistent with experimental values (4-8 nm). This model is also able to accurately capture experimentally observed trends as resist formulation and processing parameters are changed such as increasing LER with decreasing film thickness. Using this model, we have systematically investigated the effect that these new proposed resist designs could have on RLS performance. The effect of PAG loading through different patterning conditions has been investigated and will be discussed. Acid amplifiers were also studied, and the effect of loading levels, acid diffusion coefficient, and acid generation efficiency will be discussed. PAG segregation to and away from interfaces will be discussed as well. Patterning assist layers, e.g. BARCs containing additional PAGs, will also be discussed and their effect on total film stack absorption of EUV photons and the diffusion of acid from the additional layers will be investigated. Another new concept that we are proposing that appears to hold promise is the use of photoacids that have two or more PAGs attached to them (Figure 2). These act like photoadjustable diffusion coefficient photoacids; when only one PAG has been activated, the photoacid has a very low diffusion coefficient that rapidly increases when the second PAG on the photoacid has been activated. This effectively provides two acids with higher diffusivity in the higher dose regions (the center of the exposed area), but a single acid with lower diffusivity in lower dose regions (near the line edge). This acts like an aerial image contrast enhancement mechanism that improves the RLS

tradeoff in these systems. This can also be imagined using a PAG with protecting groups on it; the diffusivity of the photoacid is higher in regions with higher acid content (higher dose) than in lower dose regions because the protecting groups can only be removed by an adjacent photoacid. The performance of these different resist designs will be discussed and compared (Figure 3) to determine which design scheme, or combination of schemes, holds the most promise for improving the RLS tradeoff.

7639-105, Poster Session

Evolution of resist roughness during development: stochastic simulation and dynamic scaling analysis

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Resist Line Edge Roughness (LER) is considered one of the main obstacles in the successful evaluation of the proposed near future lithographic schemes and materials. Thus it is of primary interest to pinpoint the contribution of the lithographic process steps and materials to LER formation. Resist development is a standard step in all lithographic techniques and quite early its important role to LER has been recognized [1]. Furthermore, it is the step during which the contribution of material properties can be manifested and examined. However, during development of a line and formation of the rough sidewalls, roughness is influenced by aerial image contrast, and post exposure bake in addition to material properties alone. This difficulty can be overcome with the examination of the evolution of the surface roughness of open-surface resist films during development (depth-profiling method). This method has been employed experimentally and revealed the principal role of PAG in LER. [2-4].

In this paper, we implement the above method in a simulation framework. We use a home-made stochastic simulator of the lithographic process which takes into account the molecular structure of resist film and employs the critical ionization model for the development [5, 6]. Since development of resist films is a dynamic phenomenon evolving in time, dynamic scaling theory could be applied to give valuable information. Thus, the focus is on the estimation of the exponents of the assumed power law increase of rms roughness and correlation length (and 1/z respectively) with thickness loss. The relationship of the ratio of these dynamic scaling exponents with the roughness exponent   (or fractal dimension) of surface roughness reveals the kind of kinetic roughening that dissolution-induced resist roughness exhibits. A similar approach using a simpler simulation tool. has been presented in the previous SPIE conference [7].

Our simulation approach shows that the rms roughness of conventional resists with no PAG increases very slowly with ~0.1-0.2 in agreement with the experimental results. Also, the three afore mentioned exponents (,1/z,) obey the Family-Viscek ansantz (z= /) indicating the normality of the resist kinetic roughening during development. However, their values do not seem to belong to known universality classes and may define a new one.

Following the experimental work, we will extend the simulation to resists with monomeric and polymeric PAGs and examine their effects on roughness evolution and exponents. Also, a systematic study of the impact of simulation parameters on its predictions and their link to the physicochemical behaviour of the dissolved resist will be performed.

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7639-106, Poster Session

Macroscopic and stochastic modeling approaches to pattern doubling by acid catalyzed cross linking

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Pattern doubling by cross-linking of a spacer triggered by residual acid diffusion from a previously developed primary structure into the spacer is a possible option to create structure widths below the nominal resolution of the optical process. An advantage of such a process step would be the self-alignment to the primary structure, which would render a second exposure step unnecessary.

A primary structure, containing a deposit of acid is overcoated by a new spacer. During the bake process, a certain amount of residual acid leaves the primary structure by diffusion, initiating cross-linking of the spacer. It is desired that the cross-linking process is self-limiting, that means that the front of the cross-linking reaction stops after some finite time. Finally, non-crosslinked material is developed and removed together with the original pattern.

We present two modeling approaches to the bake step of this process.

In [1], a macroscopic modeling approach based on a coupled system of reaction-diffusion equations has been developed. The model takes into account the catalytic nature of the cross-linking step by assuming a two step reaction involving a catalytic intermediate. A controllable front movement takes place when the second step is significantly slower than the first one. As a control parameter, one can use the initial quencher concentration in the spacer. We assume a free volume based model for the acid diffusion coefficient depending on the state of cross-linking. The macroscopic model shows, that under certain circumstances, initial quencher concentration can be used to control the CD of the new pattern.

Similar results have been obtained using a stochastic modeling approach [2]. It has been shown that quencher concentration reduces overall both CD and LWR, while both of them increase with acid diffusion length. The process potentially allows the creation of very fine structures (CDs less than 10nm). In order to produce features with CD > 10nm, long acid diffusion length is necessary. However, this demand creates unacceptable LWR levels.

Concluding, we discuss the particular issues and merits of the modeling approaches.

The results have been obtained in the framework of the European collaborative MD3 project.

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7639-107, Poster Session

Simulation on resist-filling process in UV-nanoimprint lithography

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Resist filling process and bubble trapping are investigated by numerical simulation in UV-nanoimprint lithography. The resist is assumed to be in-compressive Newton fluid and the Navier-Stokes equation and the continuous equation are solved. The confined air in the cavity is also considered as a compressive fluid and the flow equations are solved. At the boundary between the resist and the template, contact angle is defined due to valance of the surface tensions, where the resist is pulled up into the pattern cavity by capillary force. The resist flow and gas (air) flow are solved, simultaneously.

In this model, there are two patterns on the template and air is confined in the pattern cavities. The results show that the confined compressive gas is enough condensed by capillary force and the bubble will be eliminated by compressed pressure in a small pattern cavity. However, there remains some afraid that the gas in not enough compressed in wide patterns. The dependence on the aspect ratio of the patterns is discussed.

7639-108, Poster Session

Comparison study of 248-nm/193-nm LWR using dynamic Monte Carlo molecular scale modeling

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Current minimum feature sizes in the microelectronics industry dictate that molecular interactions affect process fidelity and produce stochastic excursions like line width roughness (LWR). The composition of future resists is still unknown at this point, and so simulation of various resist platforms should provide useful information about resist design that minimizes LWR. In the past, researchers developed a mesoscale model for exploring representative 248nm resist systems through dynamic Monte Carlo methods and adaptation of critical ionization theory . This molecular modeling uses fundamental interaction energies combined with a Metropolis algorithm to model the full lithographic process (spin coat, PAB, exposure, PEB, and development). Application of this model to 193nm platforms allows for comparison between 248 and 193nm resist systems based on molecular interactions. This paper discusses the fundamental modifications involved in adapting the mesoscale model to a 193nm platform and investigates simulating LWR in both 248 and 193nm resist systems. The relationship between LWR and resist formulation components will be discussed. Furthermore, the impact of non-uniform component distribution on LWR will be investigated and compared against historical industry findings.

7639-109, Poster Session

Dynamical scaling in stochastic photoresist development

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While traditional lithographic modeling assumes a continuum model of the world, when features are at the tens-of-nanometers level a stochastic worldview begins to dominate. In contrast to continuum modeling, a stochastic approach to modeling chemical events treats each fundamental microscopic event as a probabilistic event, typically represented by a binary random variable. By using the continuum (mean field) result as the probability function for this random variable, the properties of complex chemical reactions can be derived.

While stochastic modeling has been successfully applied to photoresist exposure and post-exposure bake processes in recent years, the stochastic behavior of resist dissolution is much less understood. Dissolution rate variance comes from both the variance in the polymer solubility itself and the resulting variation in the development path required to bypass randomly insoluble polymer molecules. In this paper, fractal surface growth/etching models [1] will be applied to photoresist dissolution to predict the difference in dissolution rates between the stochastic and continuum models, and to predict the resulting surface roughness. Building on past work [2], dynamical scaling concepts will be used to predict the relative importance of roughness created during development versus the roughness inherent in the blocked polymer concentration at the start of development. Using a stochastic model of development, open frame development will be simulated with varying uncertainties and correlations of blocked polymer concentration. The resulting surface properties (RMS roughness, correlation length, and roughness exponent) versus development time will be related to the same properties of the input blocked polymer concentration.

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7639-110, Poster Session

Simulation study of directed self-assembly for 10-nm pattern formation

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Top-down approaches under development, such as extremely ultraviolet (EUV) technique, the high-index fluid-based immersion ArF lithography, and the double patterning technology (DPT), may be cover one or two generations. The technology combined with the top-down lithography and the bottom-up assembly can extend lithography patterning beyond current resolution limits. The mass production for the directed self-assembly requires easy to process, low critical dimension (CD) variation, low edge roughness, good plasma etch selectivity and resistance, high throughput, low number density of pattern defects, scale down to sub-10 nm domain sizes, long-range order formation of regular patterns, control of multi-level (three-dimension) assembly. The process simulation can help to solve the above problems. Molecular simulation is an exceptionally useful method for predicting self-assembled structures in various macromolecular systems, enlightening the origins of many interesting molecular events such as protein folding, polymer micellization, and ordering of molten block copolymer. In this paper, a template-assisted self-assembly and graphoepitaxy are described and simulated in molecular scale for 10-nm pattern formation. Impacts of block polymer components and heating on pattern formation are analyzed and discussed.

7639-111, Poster Session

Theoretical analysis of energy dissipation of electron in the resists II

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Incident electrons in the electron-beam (EB) lithography or photoelectrons generated by the extreme-ultraviolet (EUV) lithography collide with resist materials and bring out the ionizations and electronic excitations of them. The generated secondary electrons continue to ionize and excite the resist molecules until their electron energies become lower and unable to ionize or excite the resist. The cations produced by the ionization make the de-protonation reaction contributing to the production of photo acids. The thermalized electrons react with the photo-acid generator (PAG) to produce the anion which is a source of the photo acids in resists. Therefore the degradation mechanism of the electrons in resists plays the important role to determine the resist properties such as sensitivity, resolution and line-edge roughness. The electrons lose their energies by these inelastic collisions to form the broad distribution in kinetic energy. The energy distribution of electrons may influence the above-mentioned mechanism of electron reactions. The electron scattering in the resist was studied by using the binary-encounter collision theory and the effects on the ionization and electronic excitation of resist molecules were reported in the previous paper, where the analytical expression is valuable to study the degradation spectrum. [1] However the degradation spectrum was derived by the summation of “all collisions” of electrons with the resist molecules. The obtained property is the average value of “all collisions”. For instant, it can not evaluate the depth dependence of ionization and electronic excitations in the resist film. Therefore the Monte Carlo simulation using the analytical cross

section is used to study precise information such as the depth profile of ionization and electronic excitations in this paper.

In the EB lithography and EUV lithography electrons mainly react with the polymer molecules of resists because of their larger molecular numbers than the smaller indignant such as PAG. The phenol molecule was used as a model of resists based upon phenol resins. The Monte Carlo simulation was used using the analytical cross sections. [2] The home-made simulation program has almost developed now. The simulation program will be checked with the results of the precious analytical calculations. And depth profiles of ions and electronic excited states produced by the electron collisions will be simulated. At the conference the results of ionizations and electronic excitations and other resist film will be discussed.

Reference

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7639-29, Session 8

Methods to explore and prevent pattern collapse in thin film lithography

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Pattern collapse is becoming a critical issue as integrated circuit fabrication continues to advance towards the 32 nm node and below. Though line edge roughness and resolution are certainly important, other issues such as pattern collapse by both bending and adhesion failure must be addressed in order for technology to continue to progress. In this work, the pattern collapse of a hydroxystyrene-based positive tone copolymer has been thoroughly investigated. An e-beam lithography pattern was specifically designed with a series of line/space widths (Figure 1) which allowed the calculation of the critical stress at the point of collapse as a function of the feature width and the film thickness. It was found that the critical stress decreased both as the thickness and the feature width of the resist line decreased (Figure 2). Using an elastic beam-bending model, the modulus of the resist was also determined as a function of both feature width and film thickness, and displayed a similar trend. In order to evaluate the effectiveness of our model, thin-film buckling experiments were performed on our photoresist and characterized using atomic force microscopy in which the effective modulus of the thin films was determined (Figure 3). Furthermore, studies were also performed on mondisperse polymer samples in order to elucidate the effect of molecular weight on the modulus of polymer thin films. Additional models are currently being developed in order to accurately compare the 3-d beam bending modulus data to the modulus values obtained from the results of the 2-d thin film buckling experiments and will be discussed.

A post-development strategy to reduce pattern collapse was also developed whereby the hydroxyl functional groups of the resist were cross-linked via a dicarboxylic acid using carbodiimide chemistry. Application of the reactive rinse resulted in a clear decrease in pattern collapse behavior as observed by SEM. A reactive surface modifier capable of covalently attaching to the photoresist was fabricated in the form of a vinyl-ether-modified silane. Application of such surface modifiers, including their ability to effectively improve resist-substrate adhesion, will be shown.

7639-30, Session 8

Latent image formation in chemically amplified molecular resists: a neutron reflectivity study

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Continued advancements to achieve sub 22 nm features are enabled by chemically amplified photoresists. The development of new EUV resist materials, either through novel architectures, new photoacid generators, or base quenchers would be accelerated by a rapid measurement methodology to independently characterize the photoacid diffusion length. Using a well-defined photoacid generator gradient we characterized the photoacid reaction-diffusion kinetics in a variety of resist formulations from commercial EUV formulations to model polymer and low-molar mass molecular resists. Resolution predictions were verified by EUV lithography. While photoacid diffusion ultimately limits resolution, the spatial-extent and shape of the latent image remains strongly correlated to line-edge roughness. In order to test available models, we have applied high-resolution neutron reflectivity to directly measure the latent image composition profile in novel molecular resists. The propagation of the photoacid reaction-diffusion front in molecular resists has quantitative differences with polymer resists and directs at the importance of a phenomenological photoacid trapping mechanism. Further, the shape of the reaction front provides an explanation for the observations of the short diffusion lengths. Experimental results will be presented as a function of post-exposure bake temperature, time and degree of protection in novel calix[4]resorcinarenes.

7639-31, Session 8

Fundamental studies of the effect of acid amplifiers and sensitizers on ArF and EUV resist performance

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Acid amplifiers (AA) and sensitizers are currently being investigated as additives to improve the performance of next generation 193 nm, e beam and EUV chemically amplified resists. Both types of additives are designed to improve photospeed, AA's by increasing acid concentration via thermal reactions catalyzed by photoacid, sensitizers by increasing the effective quantum yield of photoacid. A key consideration is that the use of these additives does not result in a degradation in resolution or an increase in line width roughness (LWR).

We have prepared several types of resist containing either acid amplifiers or sensitizers and investigated the additive effects on resist sensitivity at DUV and EUV. Photo speed gain was achieved for several resist formulations containing either acid amplifier or sensitizer at DUV and EUV. The resist physico-chemical properties and the magnitude of photo speed improvement varied depending on the resist, additives and processing conditions. We have used UV-VIS and FT- IR spectroscopic techniques to measure the yield of acid formation and the extent of deprotection reaction of resists containing these additives. This paper describes the results of our fundamental studies on understanding the reasons for the observed differences in resist performance, acid yield formation and the extent of deprtoetction reaction for ArF and EUV chemically amplified resist systems containing either acid amplifiers or sensitizers as additives.

7639-32, Session 8

Fluorinated acid amplifiers for use in EUV photoresists to help beat the RLS trade off

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EUV lithography is the leading candidate for the 22 nm lithography node. A major challenge posed to EUV resists are the simultaneous inprovement of resolution, line-edge roughness (LER), and sensitivity, commonly refered to as the RLS trade-off. We predict that the best way

to get the required resolution, LER, and sensitivity all in the same resist is to create more acid molecules per absorbed photon. One method of increasing the amount of acid is through the use of acid amplifiers (AAs). Acid amplifiers are compounds that decompose in the presence of acid to generate more acid (Figure 1). This kind of decomposition kinetics is called autocatalysis.

Acid amplifiers have been shown to improve the sensitivity of EUV resists. In this paper, we describe the synthesis and reactivity of twelve acid amplifiers specifically designed for use in EUV resists. We looked at three different platforms capable of producing three different fluorinated sulfonic acids. We show the molecular structures and synthetic procedures for making these compounds.

The reactivities of these compounds were explored in solution using 19F NMR. We studied the rate of acid formation at 100 °C under acid catalyzed and uncatalyzed conditions. The experimental results were compared to thermodynamic calculations using the computer program Spartan.

We also explored the influence of AAs on the imaging characteristics of resist films. We prepared EUV resists with and without acid amplifiers and compared their resolution, line-edge roughness and sensitivity.

7639-33, Session 8

Pattern density effects: develop loading as a cause of chemical flare

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Pattern density effects have been featured as a problem in both electron-beam and optical lithography in many publications over the last few years.[1,2] These effects are manifested as a systematic variation in critical dimension as a function of position on the wafer. It is becoming an increasing problem as the pattern density and diminishing critical dimensions are needed for production nodes 32nm and beyond.

The term develop loading refers to the effect of local depletion of developer in highly exposed regions; this can result in deviation in feature size that may be difficult to correct for during the exposure process. Develop loading is one potential source of chemical flare. An alternate cause of chemical flare, where photogenerated acid evaporates and then redeposits during post-exposure bake, has earlier been proposed.[1]

Here we will describe how to separate the detrimental effects of pattern density, focusing on chemical flare and develop loading. We are using 248 nm exposures and a controlled develop process within a custom liquid flow cell to study the effects of developer depletion in a systematic manner.

References:

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7639-34, Session 8

Is the resist sidewall after development isotropic or anisotropic? effects of resist sidewall morphology on LER reduction and transfer during etching

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Line Edge Roughness (LER) is considered one of the critical sources of variation to sub-45nm transistor generations and a lot of studies have been devoted recently to its investigation. The main emphasis has been on post-litho resist LER since lithography is the first step in which the sidewall roughness (LER) is formed. However, what eventually affects device performance is the variations in gate length along gate width. These emanate from resist LER through the application of a number of etching steps. The first etching step may be a resist trimming process aiming to the reduction of both CD and hopefully LER. The effects of these plasma etching processes on LER are still unclear and under both experimental and modeling investigations.

In a previous paper [1], we compared modeling and experimental results for the effects of plasma etching on photoresist Line Edge Roughness (LER) and its anisotropic transfer into underlayer films. In particular, we investigated the roughness formation and evolution on both photoresist and underlayer sidewalls during a) isotropic trimming of photoresist, b) anisotropic plasma etching and LER transfer to substrate.

In the models developed, we assumed that resist sidewall morphology after lithography is isotropic (i.e. statistically invariant under any rotation around a perpendicular axis).

The trimming process is modeled with an (2D or 3D) isotropic movement of the resist sidewall not affecting the underlayer, while in the anisotropic plasma etching process, the resist sidewall is used as a mask to anisotropically transfer the pattern to the underlying film. From these models, we captured the experimental qualitative trends (reduction of rms roughness and increase of the correlation length in trimming and reduction of rms and unchanged correlation length in pattern transfer) but failed in the quantitative comparison since the models predicted much slighter rms and correlation length variations.

In this paper, we bring in question the assumption of isotropic resist sidewalls after lithography, and demonstrate that its correction is crucial for the quantitative agreement of model predictions with experimental findings.

More specifically, analysis of CD-AFM images of resist features indicates that their sidewalls exhibit a strong anisotropy in the form of striations perpendicular to line direction. Also, experimental measurements of sidewall roughness by various CD-AFM tips seem to suggest dependence of the obtained correlation length on tip dimensions.

These experimental findings have been taken into account in the simple models for the resist trimming and pattern transfer.

We demonstrate that the consideration of post-litho resist anisotropy improves model predictions for LER reduction during pattern transfer and confirms the beneficial effect of the resist trimming process before pattern transfer on total LER reduction. Also, the models give stronger LER reduction especially during trimming for lower correlation length of the initial post-litho resist sidewall. Thus, using input correlation length in the models smaller than the measured one brings model predictions closer to experimental results.

[1] Constantoudis et al., Proc. of SPIE 7273, 72732J (2009).

7639-35, Session 9

Inactivation technology for pitch doubling lithography

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We propose inactivation technology which improves resolution limit. We have developed novel material, which can inactivate activated acid with thermal treatment or exposure.

In order to push forward pattern pitch finer, various litho litho Etch (LLE) double patterning processes have been proposed. However, most of all LLE have several issues, including pattern deformation and CD shrink caused by severe curing condition and deterioration of the manufacturability due to multiple steps needed for 1st pattern freezing process.

Inactivation technology realizes simple LLE process with good fidelity. In which, a positive resist containing base generator for 1st patterning and an alcohol solvent positive resist for 2nd patterning are employed. After 1st patterning, acid is inactivated by amine released from the thermal base generator (TBG) by 100-150oC bake treatment. Litho

inactivation litho etch process (LILE) has two advantages, 1) throughput improvement by facile freezing process of just only simple bake and 2) prevention of pattern deformation because of effective low temperature bake. Use of the alcohol solvent prevents 2nd resist from intermixing with 1st resist. 40nm square hole pattern was delineated by 1st and 2nd cross line of double patterning, 32nm and finer line pattern was formed by double parallel line patterning.

Inactivation technology also realizes frequency doubling. Photo base generator (PBG) is able to inactivate acid from PAG by irradiation. The combination PAG and PBG of different decomposition efficiency creates both of acid activation region and acid inactivation region versus irradiation dose. By combination of high efficiency PAG and low efficiency PBG, positive tone dissolution property at low dose region and negative tone at high dose were observed. The dual tone resist split a line in two and it has possibility of frequency doubling by single exposure.

7639-36, Session 9

Process feasibility investigation of freezing free litho-litho-etch process for below 32-nm hp

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Double patterning with 193nm immersion lithography becomes to most promising candidate for 32nm hp node and possibly below 32nm hp. Several double patterning methods have been suggested such as LELE (Litho-Etch -Litho-Etch), LLE (Litho-Litho-Etch) and Spacer defined process, however, LLE process is pointed out as low cost double patterning technique because of its simplicity. But LLE process needs new method to maintain 1st lithography pattern and additional freezing processes have been suggested.

In SPIE Advanced Lithography 2009, freezing free “Posi/Posi” process was introduced as candidate for LLE process. This is LLE process that uses two different positive tone photoresists without freezing process. The resist for 2nd lithography contains a specific solvent to prevent the mixing of two resists and there is an activation energy gap between 1st and 2nd resists to maintain 1st lithography pattern. The double patterning can be successfully processed by these specific resists without freezing process. It was proved that “Posi/Posi” process could work to obtain 32nm hp with pitch splitting and 40nm contact hole by cross-line method without freezing process. For process feasibility, the CD uniformity and the CD shift through process for 32nm hp were investigated. In addition, it was confirmed that “Posi/Posi” process could achieve 22nm hp resolution.

In this study, the performance of this freezing free “Posi/Posi” process is investigated for pitch splitting pattern using 1.35 NA exposure tool. The imaging results including CD control capability, defectivity and etching results are collected for 32nm hp and below. Additionally the two dimensionals pattern imaging is also obtained for 32nm minimum pitch.

7639-37, Session 9

Evolution of thermal cure photoresist for double-exposure processes in advanced logic applications

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To extend immersion based lithography to below 32nm half pitch, the implementation of Double-Patterning lithography requires that cost be contained by as many means possible. In addition to CDU and defectivity, simplifying the process flow is a viable approach to helping accomplish cost reduction. For Litho-Litho-Etch processes, this entails replacing the flows that require spin-on chemical freeze with a solely thermally cured resist approach, thereby eliminating materials and several process steps from the flow [1]. As part of ongoing efforts to allow Double-Patterning techniques to further scale semiconductor devices, we use DETO (Double-Expose-Track-Optimized) methods for producing pitch-split patterns capable of supporting 16 and 11-nm node semiconductor devices. In this paper we present the results from systems of thermal cure Double-Patterning patterning resist; looking at process window, CDU, defectivity, and resolution limit.

References

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7639-38, Session 9

Process characterization of pitch-split resist materials for application at 16-nm node

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Lithographic scaling beyond the 22 nm node requires double patterning techniques to achieve pitch values below 80nm. The semiconductor industry is focusing on the development of track-only lithographic processing methods in order to reduce cost, cycle time and defects. Initial efforts for track-only double expose processes have relied on the use of chemical freeze materials to prevent inter-mixing of resists, and also by means of a thermal cure process to alter the solubility properties of the first pattern layer. These two techniques may be complementary, in the sense that a chemical freeze may be very robust for protection of exposed regions, while thermal cure systems may provide strong protection of large unexposed areas.

We will describe our results with both chemical-freeze and thermal-cure double patterning resist materials, and the application of these materials to the fabrication of sub-80 nm pitch semiconductor structures. We will summarize the process window and defect capability of these materials, for both line/space and via applications. Figure 1 shows an example of a resist pitch-split pattern at 64 nm effective pitch, and the RIE transfer of this image into silicon ARC (SiARC) with organic underlayer (OPL), and then into a hard mask for image transfer into dielectric.

Figure 1. SEM cross-section views of pitch split resist pattern on left, with image transfer by RIE into SiARC and organic underlayer (center), and image transfer into hard mask (right).

7639-39, Session 9

Simplified double-patterning techniques based on LFLE process

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Double patterning is one of the most promising techniques for sub-30nm half pitch device manufacturing. Several ways of double patterning processes have been reported, including LELE (Litho-Etch-Litho-Etch) and LFLE (Litho-Freezing-Litho-Etch) process. LFLE process attracts the most attention because of its simple process and will achieve higher throughput and lower cost compared with LELE process.

The key material to accomplish LFLE process is to provide resistance to prevent any damage of first patterns from second lithography processes. We have already reported “freezing” process to provide the resistance to first patterns with applying chemical materials and have succeeded in forming 22nm LS and sub-40nm CH patterns.

Recently, we have developed a new double patterning technique, so called "self-freezing" for further process simplification and succeeded in forming sub-30nm LS and sub-50nm CH patterns. This technique requires only one step bake to provide the resistances to first pattern thus expected to accomplish higher throughput and lower cost compared with chemical freezing process.

In this study, we focus on the performance of the "self-freezing" process. Imaging results including process window, LWR, critical dimension uniformity and defectivity obtained under an immersion exposure condition will be shown to discuss its feasibility to high-volume manufacturing.

7639-40, Session 9

Application of spin-on and reactive ion-etch critical dimension shrink with double patterning for 22-nm elliptical contact level interconnects

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It has been demonstrated that to create round contact holes for 32nm technology nodes and beyond it is possible to use both spin-on chemical shrink and reactive ion etch [RIE] shrink in tandem to reduce the critical dimensions [CD's] and extend the process capability of optical lithography.1 Elliptically shaped contacts are commonly used in logic devices. The need to shrink the CD's for elliptical contact holes will also be required for future technology nodes.

The application of chemical and RIE shrink techniques allows for creation of 32nm contacts using the imaging processes of 65nm contacts and traditional 193nm immersion lithography.1 However the integration of these techniques into the process adds several layers of complexity. The addition of elliptical contacts further complicates the shrink processes because the ratio of CD's along the minor and major axis of the contact holes must be maintained. The exact control of levels of shrink for both axes as well as both shrink techniques must be preserved. Traditionally with circular contact holes, both lithography and etch share the responsibility for the shape and size of the contacts. However with elliptical contacts, a larger burden in controlling the critical parameters [CD, length/width ratio] lies with the lithography process. Since pitch doubling will also be utilized, the same stringent CD control and overlay will be required for the second layer patterning. It will also be necessary to maintain very low defectivity throughout each step of the process.

The focus of this paper will be on the application of chemical and RIE shrink technologies on elliptical contact holes in a litho-etch-litho-etch [LELE] double patterning scheme. This work will show the capability of an optimized lithographic and chemical shrink process to accurately control CD, CD ratio, and shape of the contacts. Defectivity post litho and shrink will also be addressed as well as overlay for second layer DP. Etch shrink performance will be evaluated for the same parameters. In addition we will analyze this process for opens/shorts margins.

7639-41, Session 10

Roughness characterization in the frequency domain and LWR mitigation with post-litho processes

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In this paper we will use previously developed Line Width Roughness (LWR) analysis techniques to characterize post-litho process LWR reduction methods in the frequency domain.

Post-litho processes are likely to be required to reach the ITRS 3 LWR target for the 32nm and 22nm half pitch technological node. The aim of these lithographic processes is to mitigate the roughness of the resist and ultimately the etched patterns without a dramatic change in Critical Dimensions (CD). Varies techniques have been proposed: in-track chemical processes, ion beam implantation and plasma treatments as dedicated etch-step. Each technique manifested a characteristic smoothing in the frequency domain , , reducing the LWR up to 30%. Exploiting the different frequency mitigation, and combining these techniques, our target is to determine whether the 50% in overall LWR reduction is feasible.

A preliminary analysis in the frequency domain was done on in-track Hard Bake (HB) post-litho process step and an e--beam resist curing simulated with an Hitachi CDSEM tool. Both these techniques showed resist-dependent roughness mitigation in the Low and Middle frequencies, which mostly determine the CD uniformity and the MOSFET performances . Comparing the obtained Power Spectrum Density (PSD) analyses, we noticed HB curing effect is strictly dependent on resist platform (Table 1). The PSD differences between the black and the red curves are 15% and 1% LWR reduction respectively for Resist A (our reference) and Resist B. Increasing the temperature up to the Tg., both the platforms increase the LF roughness (blue curves) worsening the transistor's performances.

7639-42, Session 10

Line-edge roughness and the ultimate limits of lithography

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It seems that by scaling wavelength down, numerical aperture up, and cleverly reducing k1, optical lithography has defied all predictions of a "resolution limit". But these ingenious efforts at resolution enhancement may ultimately find a limiter that defies further scaling: line-edge roughness. For while traditional lithographic scaling theory assumes a continuum model of the world, when features are at the tens-of-nanometers level a stochastic worldview begins to dominate.

In contrast to continuum modeling, a stochastic approach to modeling chemical events treats each fundamental microscopic event as a probabilistic event, typically represented by a binary random variable. By using the continuum (mean field) result as the probability function for this random variable, the properties of complex chemical reactions can be derived. In this paper, a stochastic modeling approach is used to predict the results of a reaction-diffusion system governing the exposure and post-exposure bake of a chemically amplified photoresist used in semiconductor lithography. Unlike continuum approaches, the stochastic modeling approach allows the prediction of both the mean value and the standard deviation of the resulting chemical concentrations within the resist at the end of the post-exposure bake. In this way, basic predictions can be made concerning line edge roughness based on the fundamental stochastic mechanisms at work.

In particular, the statistics of chemical concentration, photon shot noise, exposure, diffusion, amplification, and full reaction-diffusion for a chemically amplified resist are derived. The result is a prediction of the probability distribution, mean and standard deviation, of the final concentration of blocked and deblocked polymer in the resist using simple, analytical expressions. Combining this result with a prediction of the gradient of blocked polymer concentration at the resist line edge provides a function proportional to the line edge roughness of a resist feature. Additionally, the dynamical scaling approach to roughness formation during development allows the stochastics of reaction-diffusion to propagate as a variation in development rate that dynamically grows as a propagating rough interface.

Finally, after a review of the state-of-the-art in stochastic modeling of lithography, a research program to fill in the missing pieces of a comprehensive understanding of the stochastic nature of lithography will be proposed. With all pieces in place, a very fundamental question may finally be answered: what are the ultimate limits of optical lithography?

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7639-43, Session 10

Meso-scale simulation of the line-edge structure based on polymer chains in the developing and rinse process

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As already shown in roadmap of semiconductor, the line width becomes smaller and smaller. Along the decreasing line width, the line-edge roughness (LER) becomes one of the important problems to obtain the high resolution patterns. Many researchers study the origin of the LER and try to decrease LER, and several origins of LER are proposed; the diffusion of PAG, the distribution of PAG inside the film, inhomogeneity of the dose, etc. We expected that the meso-scale simulation is also the useful tool to clarify the mechanism of LER.

In the last year, we proposed the simulation method of formation process of line edge based on the meso-scale simulation of dissipative particle dynamics (DPD) method. We first prepared the polymer thin film constituted by DPD particle. The simulation box was filled with the air and polymer particles, and the surface was represented by the interface between the phases of air and polymer in the initial structure. In the experiments, the coated film was exposed by EUV light. In our simulation, the exposure process was modeled by the conversion process from insoluble particle to soluble particle inside the film. After the exposure process, the air particles are replaced by the solvent particles, and the simulations for the development process have been done. As time goes on, the soluble polymers begin to diffuse into the solvent phase, and the line edge has constituted, and the roughness of the interface can also be estimated. In our previous simulation, we estimated the LER from the structure in the development process. However the real LER must be estimated the rinsed structure and the simulation for the rinse process must be needed. In this study, we developed the simulation model for the rinse process and we also estimate the more realistic LER structure based on meso-scale simulation.

In the developing process, at the line edge, there are the blocked polymers in which the soluble and the insoluble blocks are connected. The soluble blocks are stretched out into the developing liquid. This is due to the attractive interaction between the developing liquid and the soluble blocks. On the other hand, the rinse liquid is insoluble liquid for the all the polymers, and all the part of the polymers may be shrunk.

After the developing process, the dissolved polymer is eliminated and the space in which the dissolved polymer exists is filled by the rinse particles. The interactions between the rinse particle and all the polymer particles are set as the repulsive interaction. As time goes on in our simulation for rinse process, the chain at the line edge is shrunk and the real line edge structure can be obtained. The value of roughness is a little decreased than that at the developing process. In this point of view, the some modification of the process may be decrease the LER. Detail will be shown in the presentation.

7639-44, Session 10

A study of LER and particle generation during photoresist dissolution

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A lattice type Monte Carlo based mesoscale model and simulation of the lithography process has been described previously1. The model includes the spin coating, post apply bake, exposure, post exposure bake and development steps. This simulation has been adapted to study low frequency, high amplitude LER that arises from statistically improbable events. These events occur when there is a connected pathway of soluble material that envelops a volume an insoluble material.2 Development erodes the insoluble material into the developer stream as an insoluble particle. This process produces a cavity on the line edge that can be far larger than a single polymer molecule. The insoluble particles generated may coalesce in developer to form large aggregates of insoluble material that ultimately deposit on the wafer surface and the tooling. The effect of several process variables on the formation of LER and the generation of insoluble residues has been studied. The relative contribution of the development step and pre-development processes (deprotection kinetics, shot noise, etc.) to the low frequency LER has been examined under different process conditions. These simulations can be used to assess the commonly proposed measures to reduce LER such as the use of low molecular weight polymers, addition of quenchers, varying acid diffusion length, etc.

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7639-45, Session 10

Predictive linewidth roughness and CDU simulation using a calibrated physical stochastic resist model

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Virtually all lithography simulation used in the semiconductor industry relies on the continuum, or mean-field, approximation. Such models assume that the exposing illumination can be treated as a series of interfering plane waves and that the distribution of chemical components within the photoresist (PAG, photo-acid, quencher etc) is completely homogeneous and can vary continuously. Although this approach ignores statistical effects, due to the quantization of light into photons and the fact that resist components are discrete molecules, it has been used successfully for decades to predict core lithographic behaviors. However, as lithography approaches its fundamental physical limits, phenomena driven by quantized statistical processes, such as line-edge roughness, contact hole circularity and CD distribution, are becoming increasingly important. If virtual lithography is to help address these new industry challenges, then simulation tools need to, at least partially, transition from their current deterministic domain into a probabilistic one.

At SPIE 2009, a stochastic exposure and resist model was proposed [1] which accurately described some basic, experimentally observed, lithographic behaviors, specifically mean CD and 3 LWR through exposure dose (i.e. exposure latitude) for one photoresist irradiated at two different exposure wavelengths (ArF and EUV).

In this work, the same model is calibrated to a comprehensive experimental data set for a commercially available immersion ArF photoresist, EPIC2013 (Dow Advanced Materials). The experimental data comprise of full FEM data for multiple feature pitches. At each point in the FEM, mean CD and LWR statistics are available and repeat matrices were run on separate wafers.

The dataset allows more extensive testing of the models ability to describe complex lithographic behaviors such as Bossung curve shape, proximity effects and LWR (including its power spectrum response).

Finally, the predictive power of the calibrated model is tested by comparing simulation results to experimental CD variance data for various 1D and 2D mask patterns under scanner optical settings (NA and source-shape) which differ from those used for model parameter calibration.

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7639-46, Session 10

Reflectivity metrics for optimization of antireflection coatings on wafer with topography

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Anti-reflection coatings are commonly used in advanced photolithography in order to minimize CD variability caused by deviations in resist thickness and in the films and structures comprising the substrate. For a planar film stack, reflectivity calculations are a critical tool for optimization of parameters such as coating thicknesses and optical properties of anti-reflection coatings (TARCs and BARCs). However, with the exception of the first lithography layer, all layers on a production wafer have some degree of topography, so that reflectivity calculations for a planar film stack are not strictly correct. In this study, we evaluate four different reflectivity metrics that can be applied to wafers with topography: reflectivity for simplified planar film stacks, standing wave amplitude, amplitude of upward propagating modes, and reflected diffraction efficiencies. Each of these metrics has a simple, physical meaning that will be described in detail in the presentation.

We then evaluate how well these reflectivity metrics correlate with CD variability for two different example lithography steps: Litho-Etch-Litho-Etch (LELE) applied to FEOL and BEOL structures, and implant layers with STI (where a TARC or developable BARC might be used). In general, we find that all of the metrics can be used for film stack optimization when the printed feature edge is far from the topography on the wafer or when the materials on the wafer have similar optical properties -- this is usually the case for LELE for BEOL, because the optical properties of the BARC and hard mask are similar. For implant layers and LELE for FEOL, the contrast between the optical properties of the BARC and the materials on the wafer is high, and the printed resist features are typically very close to the topography. Here we find that the more sophisticated metrics are needed to optimize the anti-reflection strategy.

7639-47, Session 11

Synthesis and photochemistry study of anthracenyl photoswitches for 193-nm double-exposure lithography applications

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To realize pitch division patterning through double exposure proccess, novel materials should meet the requirement of demonstrating non-reciprocal photochemical behavior. In response to this requirement, a series of photoswitch molecules, in which two chromophores including anthracene and naphthalene are connected by flexible O-CH2-O link, were synthesized and investigated for their photochemical behavior in both solution and in polymer films.

These molecules were synthesized based on Williamson ether synthesis routes, linking two chromophores, each bearing halide and alcohol group respectively (see scheme below). The photochemical behaviors of such photoswitches were characterized by both UV-Vis spectroscopy and 1H-NMR. Upon exposures of 350 nm photons these molecules underwent efficient intramolecular cycloaddition in solution at relatively low concentration, forming bridged cycloadducts. With a higher concentration, some of these molecules underwent intermolecular photodimerizations resulting in product with a lower solubility. Incorporation of electron-donating groups, such as methoxy groups, resulted in a promotion of dimerization efficiency. These dimers cleaved reversibly under exposure of photons with a shorter wavelength, such as 254 nm and 193nm.

These molecules were dispersed in polymer film and tested for their photochemical behavior under similar exposures as above. Cycloaddition of these molecules did not proceed as efficiently in film as observed in solution. In contrast, cleavage of dimers in the film was observed to proceed efficiently. The most intriguing observation was that a new reaction between these photoswitches and oxygen molecules was observed during film exposure. Oxygen, either in the exposure environment or existing inside the film, excited by the chromophores, reacted with the photoswitches, forming endoperoxide in the film, which was confirmed by 1H-NMR analysis.

When these photoswitchable sensitizers are included in poly-acrylate photoresists containing transparent trialkylsulfonium PAG's, decreases in E0 values have been observed. The specific interplay of these sensitizer molecules with PAG and other resist components has been studied and will be presented with a goal to producing true non-reciprocal photoresists for consideration for 193nm technological extensions.

7639-48, Session 11

Continuous evolution of lithographic film through process steps: an example with 193 chemically amplified resists

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In the field of advanced lithography, the influence of the different bake steps (PAB and PEB) is recognized to be one of the most critical parameters as its choice will greatly impact the quality of the final patterns [1]. Defining the optimum bake conditions is often the result of several trials at different temperatures combined with the observation of the resulting pattern. In this paper we studied the impact of the different bake steps (PAB and PEB) on the lithographic performance of a model 193 nm chemically amplified resist (CA) and the correlation with its thermal properties.

Chemically amplified resists are governed by diffusion mechanisms that greatly depend on their physico-chemical properties [2]. In order to get a clear understanding of the mechanisms involved, a 193 nm resist material was selected with a high glass transition temperature (Tg = 170°C). This 193nm photoresist is based on a methacrylate model polymer from Dow Electronic Materials. The polymer is a functionalized terpolymer dissolved in an organic solvent (PGMEA) with other additives including the Photo-Acid Generator (PAG). Today's PAGs are chosen with large steric sizes in order to control their diffusion and consequently the final resolution, contrast and edge roughness. Varying PAG content implies a potential plastifying effect and a larger range of glass transition temperature (Tg) variations of the formulation. This, therefore, leads to the possibility of switching from non-annealing to annealing conditions [3] (bakes below and above Tg) depending on the PAB temperatures. In this work we have selected the desired physico-chemical properties of the resist in order to have access to a large range of free volume content and diffusion conditions for the PAG.

When applying PAB temperatures under Tg, the resist only shows slight thickness variations and consequently small free volume variations. When PAB temperatures reach Tg and temperatures superior to Tg, a large decrease in thickness can be observed and hence a high reduction in free volume .

To understand the influence of free volume, we worked first with a single PEB temperature and different PAB temperatures around Tg. The impact on resist sensitivity (i.e. on the dose to clear value : E0) can be approached for different PAB temperatures from 110°C to 200°C, keeping PEB temperature constant and equal to 110°C, therefore well below Tg. Different regimes can be detected. From 110°C to 140°C, E0 increases. This could be attributed to a small free volume decrease (i.e. decrease in diffusion rate). From 140°C to 200°C, unexpectedly, E0 decreases. Another diffusion regime appears. In order to explain this new regime, physical modifications in the polymer matrix as well as the behaviour of additives such as PAG and quencher were investigated.

The impact of various PEB temperatures for fixed PAB temperatures

was also studied. In this case, it became possible to separate the effect of PAG mobility and deprotection kinetics from that of steric environment. Finally, the different PAG diffusion mechanisms were correlated with patterning capabilities (edge roughness and process windows).

The results obtained give a greater insight in PAG diffusion behavior for very different process conditions and should help finding a better modeling [4] of these complex systems.

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7639-49, Session 11

High-resolution cleavable-polymer resists for EUV lithography

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EUV resists must continue to make simultaneous improvements in resolution, line edge roughness (LER) and sensitivity. One chemical approach for advanced EUV resist uses relatively small molecular glasses instead of polymers in pursuit of better line edge roughness (LER). We have recently designed a revolutionary new positive resist platform that uses acid-catalyzed polymer cleavage reactions to transform starting polymers with Mw = 6-20 Kg/mole into much smaller fragments during acid catalyzed polymer cleavage reactions upon exposure. These smaller fragments have faster dissolution rates than the starting polymers.

Here, we describe synthetic and formulation details, and lithographic performance of this new approach. We have synthesized several new monomers that allow us to control the solubility and reactivity of the resist polymers using a monomer blend strategy. Molecular weights are measured for each polymer film before and after exposure to show the extent of Mw reduction. Our first imaging experiments using a non-optimized polymer, formulation or process demonstrated better than 32 nm resolution.

7639-50, Session 11

Development of spin-on high-carbon hard masks for high-resolution photolithography

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Silicon and carbon rich hard masks such as SiON and amorphous carbon (ACL) have been widely used for high resolution pattern generations in integrated circuit (IC) chip fabrications. Those hard masks are conventionally prepared through chemical vapor deposition (CVD) processes. CVD process requires extra investment on CVD tools and reduces manufacturing throughput. Preparations of hard masks using polymer solution based spin-on formulations employ regular wafer processing tracks, reduces process complexity and therefore the manufacture cost. There are many challenges in developing quality formulations for carbon spin-on hard masks (C-SOHM). In general, high carbon containing organic polymers (> 85wt%) with good solubility in regular solvents are required as platform polymers in order to have good etch resistances during oxygen and fluorocarbon based plasma etch processes for good pattern transfer fidelity. In this publication, lithographic performances of a group of high carbon C-SOHM formulations will be reported. Correlation between film plasma etch resistance and its carbon content, and material thermal stability upon high temperature bake like 400 in air will be discussed as well.

7639-51, Session 11

Topcoat-less resist process development in 30-nm Dram devices

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In recent years ArF immersion lithography in Dram devices, topcoat process has become baseline process in mass production in spite of its additional process steps and high cost-of-ownership. In order to overcome low process efficiency of topcoat process, high throughput scanner with higher scan speed and advanced rinse modules for decreasing defectivity are under development. Topcoat-less resist is also upgraded gradually which contains hydrophobic additives enables the extreme patterning without topcoat and high speed scanning. But current topcoat-less process has not matured yet for the dark-field mask compared to bright-field because of the blob defect in unexposed area. To minimizing blob defect level both material and process sequence should be optimized effectively. The authors have focused on feasibility of the blob defect and litho performance of topcoat-less resist process for dark field application in 30nm Dram devices.

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7640-01, Session 1

Super-lens and plasmonic lithography

X. Zhang, E. S. Kuh, Univ. of California, Berkeley (United States)

No abstract available

7640-02, Session 1

Shaping the future of nanoelectronics beyond the Si roadmap with new materials and devices

M. Heyns, IMEC vzw (Belgium)

No abstract available

7640-03, Session 1

Getting there together: a multi-disciplinary approach to lithography's renaissance (at the limit of the scaling roadmap)

L. Capodieci, GLOBALFOUNDRIES Inc. (United States)

No abstract available

7640-04, Session 2

Generation of arbitrary freeform source shapes using advanced illumination systems in high-NA immersion scanners

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Today a strong interest is visible in further extending ArF immersion lithography to smaller nodes in order to bridge the gap until EUV is ready for high volume production. A variety of resolution enhancement techniques like strong off-axis illumination, double exposure, different double patterning schemes, and litho friendly designs (Design for Manufacturing, DfM) are under evaluation to enable further shrinks, to increase yield, or to reduce manufacturing cost. One of the key parameters in shrinking k1 close to the physical limit is the proper shape of the illumination pupil. Especially for complex patterns like SRAM cells the co-optimization of mask layout and illumination pupil (source mask optimization, SMO) is an important enabler for future process development.

In this paper we will present the capabilities of the Diffractive Optical Element (DOE) based Aerial XP illuminator and the new programmable FlexRay illuminator in the context of customized or freeform illumination pupils. First we will explain the principle of illumination optics using DOEs to form a desired pupil. Then we will discuss how arbitrary illumination pupils can be generated by the new programmable FlexRay illuminator. We will show that despite a different pupil forming mechanism, the resulting pupil shapes are compatible regarding lithographic imaging performance. In addition to the quick generation of new illumination pupil shapes, the FlexRay system will enable fine tuning of source shapes in order to optimize tool matching. We will show for both illuminator types that practical constraints like minimum spot size do not limit the imaging capability of the system.

One section of the paper will deal with the characterization of measured freeform source shapes. We will also discuss the differences of reticle level source shapes and wafer level source shapes and how these differences impact simulation results. We will outline how to get to the desired pupil in the system, how to use these for simulation and how to properly interpret the results of the onboard source metrology in the context of simulation. Finally we will demonstrate the matching of illumination source shapes generated with the Aerial XP and the FlexRay illuminator, proving that processes can be transferred between the two illuminator types.

With this work we demonstrate that ASML's illumination systems fully support the use of customized or freeform illumination pupils for lithographic process optimization and therefore will help to push the extension of ArF immersion lithography.

7640-05, Session 2

Demonstrating the benefits of source-mask optimization and enabling technologies through experiment and simulation

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In recent years the potential of Source-Mask Optimization (SMO) as an enabling technology for 22nm-and-beyond lithography has been explored and clearly documented. It has been shown that intensive optimization of the fundamental degrees of freedom in the optical-system allows for the creation of nonintuitive solutions in both the mask and the source, which leads to improved lithographic performance. These efforts have driven the need for improved controllability in illumination and have pushed the required optimization performance of mask optimization. This paper will present recent experimental evidence of the performance advantage gained by intensive optimization, and enabling technologies like pixelated illumination. Controllable pixelated illumination opens up new regimes in control of proximity effects, and we will show corresponding examples of improved through-pitch performance in 22nm Resolution Enhancement Techniques (RETs). Simulation results will back-up the experimental results and detail the ability of SMO to drive exposure-count reduction, as well as a reduction in process variation due to critical factors such as Line Edge Roughness (LER), Mask Error Enhancement Factor (MEEF), and the Electromagnetic Field (EMF) effect. The benefits of running intensive optimization with both source and mask variables jointly has been previously discussed. This paper will build on these results by demonstrating large-scale jointly-optimized source/mask solutions. The potential impact on design-rules will also be explored.

7640-06, Session 2

Tolerancing analysis of customized illumination for practical applications of source and mask optimization

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The k1 factor continues to be driven downwards, even beyond its theoretical limit of 0.25, in order to enable the 32 nm feature generation. Due to the extremely small process window that will be available for such demanding imaging challenges, it is necessary that active techniques that can expand the process window and robustness of the imaging against various kinds of imaging parameters be implemented. Source & Mask Optimization (SMO) is a promising candidate for such techniques.

One of the most effective applications of SMO is optimization of the second exposure of line/space features plus the "cutting lithography" technique. This is one of the candidates for 18nm halfpitch patterning. This technique uses two beam interference patterning for the first exposure and random cutting for the second exposure.

Although many applications of SMO are expected, tolerancing and specifications for aggressively customized illuminators (an example of which is shown in figure 1) have not been discussed yet. In this paper we are going to study tolerancing of a pupilgram which is a solution of SMO.

We have analyzed several types of error in the pupilgrams, categorizing them into intensity distribution error and scaling error. We express each error functionally. In some cases, we used the Zernike polynomial based functions. Subsequently, sensitivity analysis of each component of the error to several imaging performance items has been done. Then, we defined a tolerance for each component of the errors in the pupilgram.

In addition, the impact of constraints upon imaging performance, such as allowed gray-scale levels and spatial resolution of the pupil, has also been studied. In order to minimize the imaging performance degradation from performance level predicted as a result of SMO, the constraints of the illuminator need to be taken into account in the original SMO process.

Finally, we have compared the tolerance of each category and the expected performance of the illuminator. As a result of the comparison, we verify that the required imaging performance can be expected from our illuminator.

7640-07, Session 2

Freeform illumination sources: an experimental study of source-mask optimization for 22-nm SRAM cells

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A strong demand exists for techniques that can further extend the application of ArF lithography. Among these techniques are litho-friendly design (DFM), dual exposure or patterning schemes, extreme off-axis illumination modes, the use of alternative processing materials, ... Typically, state-of-the-art achievements in the lithography steps of IC manufacturing are based on an integrated approach of the above techniques.

In this paper, we make an experimental assessment of the use of freeform illumination source shapes. The experiment is set up on an ASML XT:1900Gi scanner at 1.35 NA, and focuses on the (double/single) patterning of the Contact and Metal1 layers of a 22 nm node SRAM, including etch into a hard-mask. The designs, with small gaps and minimum pitches corresponding to k1 values of 0.38 and below, are aggressive cases for ArF immersion lithography for SRAM patterns.

With freeform illumination, the pupil source shape can consist of a collection of bright spots of varying sizes and intensities, and ultimately optimized for the patterning of a specific design. In particular for this work, a study is made of the achievable gain in terms of process latitudes (EL, DoF and MEEF) for an optimized freeform source with respect to the optimal standard 'library' source shapes (e.g. CQuad, Annular, ...).

To obtain the optimized source shapes, ASML/BRION's Source-Mask-Optimization software package was used (Tachyon SMO). In SMO, a simultaneous co-optimization of the source (e.g. freeform) and the mask (OPC & assist features) takes place.

Additionally, we address several topics related to the manufacturability of SMO, like the impact of minimum source fill factor on imaging performance and lens heating, the comparison to parametric source shapes, across field CDU and scanner budget calculations.

This work demonstrates the capabilities of freeform source shapes over the standard illumination modes, and thereby evaluates the added value of source-mask co-optimization for advanced ArF lithography.

7640-08, Session 3

Evaluation of double-patterning techniques for advanced logic nodes

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The development of Double-Patterning techniques continues to push forward aiming to extend the immersion based lithography below 32 nm half pitch. There are widespread efforts to make Double-Patterning viable for further scaling of semiconductor devices. We have developed DE2 (develop/etch/develop/etch) and DETO (Double-Expose-Track-Optimized) techniques for producing pitch-split patterns capable of supporting 16 nm and 11 nm node semiconductor devices. The IBM Alliance has established a DETO baseline, in collaboration with ASML, TEL, CNSE, and KLA-Tencor, to evaluate the manufacturability of DETO systems that are available commercially. In this paper we present the long-term performances results of the systems, and will focus on defectivity, overlay, and CD uniformity.

Key words: 32nm half pitch / 22nm; spin-on chemical freeze; Litho-Litho-Etch; manufacturability

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7640-09, Session 3

Actual performance data analysis of overlay, focus, and dose control of an immersion scanner for double patterning

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Double patterning (DP) requires extremely high accuracy in overlay and uniformity in CD control. For the 32 nm half pitch the CDU budget of double patterning requires less than 3~4 nm overlay and less than 2.5 nm CD uniformity for the exposure tool. Overlay requirements are 3 nm for LELE type DP and 4 nm for spacer type DP.

To meet these requirements, Nikon has developed the NSR-S620. It includes a new encoder metrology system for precise stage position measurement. The encoder system provides better repeatability by using a short range optical path. Since encoders suffer from relatively poor measurement linearity, the absolute position is calibrated using a conventional interferometer system. Using encoder and interferometer systems, overlay performance has been significantly improved.

For CD uniformity control, various factors such as focus control, stage control, dose control and lens aberration uniformity affect the results. Focus uniformity and stability are evaluated using phase shift focus metrology. Stage synchronization variability through the scan will also influence CD control. Dose uniformity is evaluated across the exposure slit, along the scan direction, across the wafer. Aberration uniformity within the exposure slit will also influence the CDU along the slit direction of the exposure field.

For focus control, a streaming autofocus system has been developed. It measures wafer surface topography by pre-mapping at the same time wafer alignment is performed, reducing the tool overhead and drastically improving throughput. For stage synchronization control, the NSR-S620 has an improved body structure, which completely isolates the wafer stage and reticle stage motions from the main body. Preliminary performance has already shown better than 20 nm focus control and less than 3.0 nm stage synchronization MSD.

For the 32 nm half pitch generation, overlay and dose control requires tighter control and greater control flexibility. The Nikon scanner is capable of overlay grid control and distortion intra-field control, and inter-field and intra-field dose control.

In this paper, we will show the actual performance data and analysis of the metrology system and the overall performance of the NSR-S620 for the 32 nm DP generation and below, and will compare them to previous exposure tool generations.

7640-10, Session 3

Modeling of double-patterning interactions in litho-freezing-litho-etch (LFLE) processes

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Litho-freezing-litho-etch (LFLE) processes belong to the most promising versions of double patterning techniques. Different freezing or curing techniques are applied to stabilize the photoresist pattern which is obtained in a first lithography step [1]. Afterwards, a second resist is spin coated on the top of the patterned and frozen resist. A second exposure and lithographic processing results in a final resist pattern which consists of the resist patterns from both resist materials. This paper uses advanced modeling techniques to explore interactions between the two lithography processes and to qualify their impact on the final resist profiles and process performance. It highlights the results of the simulation workpackage of the European MD3 project.

Differences between the optical properties of the first (frozen) and the second resist result in wafer side scattering effects during the second lithographic exposure. Such effects were already investigated in a previous publication [2]. Similar wafer side scattering effects can be observed for modifications of the optical properties of the bottom antireflective coating (BARC) due to the first lithography process. Despite of the curing procedure, there is still a certain impact of the second lithographic exposure on the resist pattern from the first lithography step. Generation of photoacid inside the frozen resist and partial deprotection results in reduced linewidths and thickness loss. On the other hand, diffusion of photoacid between the second resist and the frozen resist (or the BARC) depletes the concentration of acid in the vicinity of the frozen resist (or the BARC). The resulting effects provide a possible explanation for a linewidth growth and footing effects which were experimentally observed for certain resist formulations. The curing procedure and the interaction between the BARC and the second photoresist can have also a direct impact on the development behavior of the second resist. Finally, details of the curing treatment and acid diffusion between resist layers influence the linewidth roughness of the final resist profiles.

The paper investigates the described effects for several exposure geometries including interlaced and crossed lines and compares the simulation results to experimentally observed phenomena. The lithographic effects are evaluated in terms of linewidth differences, resist profiles, and process windows.

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7640-11, Session 3

Litho and patterning challenges for memory and logic applications at the 22-nm node

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While EUV lithography matures rapidly, it is still expected that primary lithography option at 22nm nm node, for both logic and memory applications, to be 193i combined with pitch doubling techniques. Previous work has indicated that using a spacer process for 32nm L/S will pose new patterning challenges due to the more complex processes which require innovative control techniques to meet CDU tolerances of multiple CD populations We have demonstrated that measuring the final CDU performance of multiple populations and feedback this information to the exposure tool, the final CDU variability can be improved by 20..40% [1].

Continuing on this, we will report on the impact of different integration schemes like direct spacer deposition on resist vs. spacer deposited on sacrificial hard mask material, on the final CDU performance.

In this paper we will extend previous control approach by addressing smaller CDU tolerances at 22nm node. Due to the tighter requirements on CD control, it is anticipated that deposition and etch steps have to be controlled to significantly tighter levels than it is usually used during a normal processing flow. In addition, due to spacer specific characteristics, lithography control necessitates extra levels of control on pattern profile, transforming the x-y dimensional control into a x-y-z control. Using correction schemes at litho level might alleviate some of the additional requirements.

Furthermore, we will expand to logic applications where, in some cases, CD control for multiple patterns and multiple pitches is required. As every distinct feature in the litho will lead to 4 populations (2 lines, 2 spaces) at the final stage, this plurality of n features times 4 populations poses new questions to be answered. This amount of different features to be controlled will strongly depend on device layout choices and device architecture. (e.g. Planar or FINFET layout)

[1] Jo Finders et al. Process control for 32nm dens lines created by spacer process, Proceedings Spie Vol. 7274, 2009

7640-12, Session 3

Comparative study of resolution limits for double patterning and EUV processes for the 32-nm contact hole case

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Currently, EUV and double patterning (DP) are competing technologies for the 22nm node, both having their own unique advantages and challenges. The purpose of this paper is to perform a case study based on a 32nm contact hole array. We explore the resolution limits and investigate capabilities of both EUV and DP processes, and evaluate options to optimize the litho performance.

In order to explore the resolution limit for a DP process quantitatively, considering the substrate topography structure is crucial. We used rigorous wafer topography simulations to take this into account.
In a first step, we performed a sensitivity analysis for a ArF double patterning technology process. Through pitch simulations show that both aerial image and developed resist shapes depend on the substrate process as well as hard mask (HM) properties. The bulk aerial image distribution shows reflection from substrate topography structure, not only inside resist but also substrate stack region, which contributes substantially to resist shape and CD variation.

To perform a comparative study between ArF DP and EUV lithography we first analyzed the resolution limit for DP process. We assumed a LDLD (litho-develop-litho-deposition) process to fabricate contact holes (32nm CD size). In the LDLD process, lithography for a contact dot pattern is performed by using a first mask (y-line) and a second

mask (x-line). After the periodic resist dots are fabricated, a deposition step is performed, and the resist is stripped in order to create the contact holes array. This process can be seen similarity with LFLE (litho-freeze-litho-etch) process, if the spacer region created by the first development is considered analogous to “freeze”, although freezing resist doesn’t exist but spacer. Since the second exposure takes place on the existing film stack.

We investigated the performance of the LDLD process by decreasing pitch until the resolution limit was reached. The possible minimum x- pitch (with y-parallel line, first mask) is 85nm, the minimum y-pitch generated for the second litho step with x-parallel lines is 90nm. This x-y anisotropic phenomenon is caused by the second litho step, where oblique incident light propagating through space regions (first litho result, now filled by immersion liquid) contributes to total image. The bulk image distribution is sensitive to the material in the spacer region (refractive index), therefore further process optimization is possible by tuning material properties.

On the other hand, the fabrication of 32nm size contact holes with EUV lithography was simulated by using a physical resist model. Pattern shift due to shadowing, slit position dependence, aberration and flare effects have been considered. A pitch of 64nm (1:1) can be realized at low flare levels, but a correction for shadowing and flare is essential.

Resist performance is a critical component in the EUV process. We investigated the LWR characteristics for EUV resist by applying a stochastic resist model. By calibrating stochastic parameter against measured data obtained by Selete (SSR3 resist), LWR = 7nm (3), comparable distribution of LWR around 7nm was reproduced. Simulation results for the 32nm contact hole are presented.

7640-13, Session 4

Advances in dual-tone development for pitch doubling

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Dual-tone development (DTD) has been proposed as a potential cost-effective double patterning technique . Dual-tone development was reported as early as in the late 1990’s . The basic principle of dual-tone imaging involves processing exposed resist latent images in both positive tone (aqueous base) and negative tone (organic solvent) developers. Conceptually, DTD has attractive cost benefits since it enables pitch doubling without the need for multiple etch steps of patterned resist layers. While the concept for DTD technique is simple to understand, there are many challenges that must be overcome and understood in order to make it a manufacturing solution.

Previous work demonstrated feasibility of DTD imaging for 50nm half-pitch features at 0.80NA (k1 = 0.21) and discussed challenges lying ahead for printing sub-40nm half-pitch features with DTD. While previous experimental results suggest that clever processing on the wafer track can be used to enable DTD beyond 50nm half-pitch, it also suggest that identifying suitable resist materials or chemistries is essential for achieving successful imaging results with novel resist processing methods on the wafer track. In this work, we present recent advances in the search for resist materials that work in conjunction with novel resist processing methods on the wafer track to enable DTD. Recent experimental results with new resist chemistries, specifically designed for DTD, are presented in this work. We also present simulation studies that help and support identifying resist properties that could enable DTD imaging, which ultimately lead to producing viable DTD resist materials.

7640-14, Session 4

Spacer-defined double patterning for sub-72-nm pitch logic technology

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In order to extend the optical lithography into sub-72 nm pitch regime, spacer defined double patterning which is known to cause minimal overlay impact among many double patterning processes [1] was investigated. In this article, by depositing the spacer film directly on the resist pattern which acts as a sacrificial layer, it will be demonstrated that the process simplification, cost effectiveness and low defectivity are achieved. In addition, key technology elements / challenges that enable successful insertion of the spacer defined double patterning technique into a logic technology node will be discussed. The elements encompass the sacrificial pattern / spacer CDU and LER, defocus-driven sacrificial layer sidewall angle variation, design ground rule definition and integration impacts on the process. Finally, patterns of effective k1 < 0.14 will be also shown as a product of an aggressive spacer double patterning scheme.

7640-15, Session 4

The impact of optical non-idealities in litho-litho-etch processing

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In previous work[1], we have shown that non-planar interfaces induced by spin-coat processes over topography can result in significant variations in imaging that are not accurately predicted by considering the limiting cases of either a planarizing or a conformal coating. In the same work it was observed that when two coatings are applied by spin coat processes over topography the upper surface of the second material is near planar, assuming that the combined thickness exceeds the topography step height.

In most imaging cases, this leads to scenarios where the upper resist surface is close to planar and any topographical excursion from a flat interface is confined to the lower resist surface. The principal exception to this, occurs in litho-litho-etch (LLE) double patterning processes, using some kind of resist freeze technique. In such schemes, a resist film for the second pass is spun over a previously imaged resist structures. Typically, the thickness of the first and second resist layers will be approximately equal, thus the upper surface of the second resist will have significant topology.

Moreover, when considering LLE techniques, it is usually assumed that the optical properties of the two layers are matched and negligible diffraction will occur at the internal interfaces.

In this work, we set out to explore the imaging impact a non-planar upper resist surface has upon LLE imaging using lithographic simulation by comparing the planar surface case against the actual surface topology observed in example LLE processes. Thus we determine whether it is desirable to design materials which exhibit better planarization or ones which accentuate the existing topology. Likewise we explore the impact of resist index mismatch has upon imaging properties and determine whether the matched index case is in fact the optimum situation

To facilitate the study, experimental work is undertaken to determine the actual surface topology on the second imaging step of state-of -the-art LLE processes. The optical parameters are determined for the first resist through the process (as coated, Post exposure, post-PEB and Post-Freeze) for comparison with the second resist. The results of the practical and theoretical work identify goals for material design improvement with respect to spin coat and refractive index properties.

[1] - Robertson, Reilly, et al., ‘Simulation of optical lithography in the presence of topography and spin-coated films’, Proc. SPIE 7273, 727340 (2009)

7640-16, Session 4

Double-patterning lithography study with high-overlay accuracy

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Double patterning (DP) is widely regarded as the most likely lithography technology for 32 nm half pitch semiconductor manufacturing. Previously, several types of DP have been proposed. Spacer DP is proposed for memory manufacturing, but because of limitations on complicated patterns, a pitch splitting type of DP, either Litho-etch-litho-etch (LELE) or litho-process-litho-etch (LPLE), where a resist cure or freeze is used to replace the first etch, is most likely for logic manufacturing. Previously, we presented an error budget to achieve CDU for 32 nm half pitch. This budget highlights the importance of CD control between first and second exposures for the lines in a DP process. This type of process is most important for the gate layer at 32 nm half pitch. It also shows the relationship between overlay and CDU for the spaces in a DP process, a key factor for metal layers. In particular, CDU performance for a single exposure of 2.4 nm (after etch), and overlay accuracy between the two layers of around 3 nm is shown.

To meet these requirements, Nikon introduced the S620 ArF immersion scanner. To achieve the 3 nm overlay requirement, it employs an encoder system to measure the position of the wafer stage. This eliminates the interferometer fluctuation that previously limited exposure tool accuracy. This system can achieve the challenging requirements for DP.

In this paper we will show the overlay accuracy, CD and CDU control, and resulting CD uniformity of a LPLE DP process using the S620. These results will verify DP can be practically achieved for the 32 nm half pitch and below using the high accuracy exposure tool.

7640-17, Session 4

Litho-process-litho for 2D 32-nm hp LOGIC and DRAM double patterning

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Over the last couple of years a lot of attention has gone to the development of new, more cost effective double patterning process alternatives to litho-etch-litho-etch or spacer-defined double patterning. Alternative Litho-Process-Litho (LPL) processes typically use a coat freezing layer, a special combination of 2 resists together with an intermediate hard bake of pattern 1 or a thermal freezing resist. Much progress has been made on the material side to improve the resolution of these processes and resolution down to 22 nm 1:1 Lines/Spaces has been demonstrated. This shows that from a resolution point of view these processes can bridge the gap between ArF immersion single patterning and EUV lithography. These results at small pitches are typically obtained using dipole illumination making them only useful for one pitch-one orientation. Applying the combination of double patterning and dipole illumination is thus limited to restricted designs. For this paper, the patterning of more random 2D and through pitch designs is investigated using the double patterning LPL alternatives for the POLY layer.

To assess the readiness of various double patterning alternatives, the printability of simple lines/spaces gratings through pitch and typical logic and DRAM representative 2D test structures are investigated using annular illumination.

Using annular instead of dipole illumination results in a sharp decrease in aerial image contrast. The impact on exposure latitude and depth of focus is quantified for simple 1D 1:1 line/space gratings and compared for the various processes.

In a first step to assess process capability beyond the simple 1D-1 pitch case, the through pitch performance for 1D line/space gratings is determined. Besides simply comparing the processes, this data also serves as an estimate of what can be achieved in best case for the 2D designs under investigation.

2D specific issues are looked at next. Special attention is paid to the influence of the LPL process and process asymmetry on line-end pull-back, turns and gaps printing as well as on stitching.

Design constraints are needed that ensure a robust 2D double patterning through process variations. Stitching robustness and design constraints as a function of process are evaluated.

Using the best available design and process settings, through batch performance is investigated. Specifically, CD uniformity, gap and turn printing and stitching quality across the wafer and wafer to wafer are generated as proof of whether the processes can be used to print 2D structures repeatedly and reliably.

7640-18, Session 4

Exploration of reversible contrast enhancement layers for double-exposure lithography

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The optical nonlinearity of reversible contrast enhancement layers (RCEL) can be used to push double exposure techniques to smaller feature sizes. Wide band semiconductor nanocrystals en-able the realization of strong optical nonlinearities in terms of light induced bleaching and refrac-tive index changes. This paper applies efficient rigorous electromagnetic field modeling to in-crease the understanding of image formation in the photoresist below the RCEL and to identify the most appropriate material parameters and imaging conditions.

The image formation below an RCEL can be understood as a complex interplay between the opti-cal nonlinearity of the RCEL and the (near field) light diffraction from the RCEL. The optical nonlinearity of the RCEL introduces high spatial frequencies which improve the intensity contrast and the normalized image log slope (NILS) inside the RCEL. Both contrast and NILS increase with the nonlinearity of the RCEL, which can be characterized by the bleaching parameter ARCEL and the light induced refractive index change nRCEL, respectively. However, a high optical nonlinearity of the RCEL is not sufficient to achieve large contrast and NILS values inside the photoresist. It is necessary to transfer the high spatial frequency components into the resist. For a lithographic exposure close to the resolution limits the high spatial frequency components do not propagate inside the photoresist. These components can be considered as evanescent waves which are exponentially damped inside the resist. High values of image contrast and NILS can be only observed in the upper part of the photoresist. The achievable contrast and NILS inside the resist depends on the coupling efficiency between the high spatial frequency components in the RCEL layer and the evanescent waves in the upper part of the photoresist, which in turn depends of the material parameters of RCEL and photoresist and on the imaging conditions.

An efficient implementation of the Waveguide method is used for a quantification of the de-scribed effects and for the identification of the most appropriate material and exposure parame-ters. It is demonstrated that the consideration of the bleaching dynamics is important to achieve correct results. A large refractive index of the resist improves the achievable lithographic per-formance. It will be also shown that RCEL layers can be used to enhance the performance of a NA=0.6 scanner to create a high contrast images with a pitch of 80nm.

7640-19, Session 5

Improving aberration control with application specific optimization using computational lithography

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As the industry drives to lower k1 imaging we commonly accept the use of higher NA imaging and advanced illumination conditions. This illumination in turn will make use of the latest in DOE (Diffractive Optical Element) design which no longer exhibit simple and diffuse pupil fill functions such as Annular or Conventional illumination. These increasingly complex pupil fill functions play a key role in the overall imaging fidelity where they are matched to the printed image. The advent of this technology shift has given rise to very exotic pupil spread functions that have some areas of high thermal energy density creating new modeling and control challenges. The intent of this paper is to address these challenges with respect to the current tool aberration control capabilities and map out a method to obtain the best tool state possible.

Modern scanners are equipped with advanced lens manipulators that introduce controlled deformation of the lens elements to counteract the lens aberrations existing in the system. These manipulators are managed by scanner software which aims at minimizing the total aberration in a dynamic manner, irrespective of the product design that is being imaged. In most cases this optimization scheme yields very good aberration control. However, since the degree of freedom of the lens manipulators are typically far fewer than the order of aberration levels, represented as Zernike coefficients from Z2 to Z37, it is not possible to simultaneously drive all Zernike coefficients to zero. The lens manipulators may also lack the ability to control some specific aberration modes that are detrimental to important structures in the design. The order of the problem is even higher considering the slit dependency of aberrations, which makes the total aberration minimization problem even more challenging.

In this paper, we introduce a methodology for minimizing the impact of aberrations for specific designs at hand. We employ computational lithography to analyze the design being imaged, and then devise a lens manipulator control scheme aimed at optimizing the aberration level for the specific design. The optimization scheme does not minimize the overall aberration, but directs the aberration control to optimize the imaging performance, such as CD control or process window, for the target design. Through computational lithography, we can identify the aberration modes that are most detrimental to the design, and also correlations between imaging responses of independent aberration modes. Then an optimization algorithm is applied to determine how to use the lens manipulators optimally to drive the aberrations modes to levels that are best for the specified imaging performance metric achievable with the tool. We show an example where this method is applied to an aggressive memory device imaged with an advanced ArF scanner. The design exhibits imaging performance degradation through the lot due to thermal induced aberrations. We then design an application specific aberration control scheme using optimization algorithms with accurate litho modeling and simulation engines, executed in a high speed, high performance computation platform. The lens manipulator control mechanism is delivered via a scanner control software interface which allows user defined process stabilization criteria to be selected in the exposure recipe on a per image basis. We demonstrate with both simulation and experimental data that this application specific tool optimization technique successfully compensated for the thermal induced aberrations dynamically, improving the imaging performance consistently through the lot.

7640-20, Session 5

Evaluation of lithographic benefits of using ILT techniques for 22-nm node

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As increasing complexity of design and scaling continue to push lithographic imaging to its k1 limit, lithographers have been developing computational lithography solutions to extend 193 nm immersion lithography to the 22 nm node. In our paper, we investigate these beneficial mask solutions with respect to pattern fidelity and process variation (PV) band performances for 1D through-pitch patterns, SRAM, and random logic Standard cells. This work compares the performance of two different computational lithography solutions: idealized un-constrained ILT mask and manhattanized mask rule constraint (MRC)-compliant mask. Additionally, we compare performance benefits for process window-aware hybrid assist feature (AF) to traditional rule-based AF. The results of this study will demonstrate the lithographic performance contribution that can be obtained from these mask optimization techniques in addition to what source optimization can achieve.

[1] Y.F. Deng, Y. Zou, K. Yoshimoto, Y.S. Ma, C. Tabery, J. Kye, L. Capodieci, and H. Levinson, “Considerations in Source-Mask Optimization for Logic Applications”, (Paper will be submitted to SPIE 2010)

7640-21, Session 5

A computational method for optimal application specific lens aberration control in microlithography

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As semiconductor feature sizes continue to shrink, the allowable error margins for CD and overlay control are getting increasingly tight. One of the contributors to CD and overlay errors is the scanner lens aberration. These aberrations can be inherent in the system due to manufacturing imperfection of the lenses, or caused by thermal induced lens deformation due to the use of extreme off-axis illumination combined with high scanner throughput. These aberrations, though typically controlled to very small levels, could still have severe impact on certain features of the design that are extremely sensitive to these aberrations. This leads to degradation in CD and overlay control, and overlapping process window.

Modern scanners are equipped with sophisticated lens manipulators. These manipulators can be controlled by scanner software to counteract the external aberrations to minimize their effects. For example, the manipulators may be optimized to produce the least squares sum of Zernike coefficients in residual aberration. It is important to note that the response of critical features’ printing properties to lens aberration is highly dependent on specific lithographic conditions and mask designs. As a result, the least squares Zernike state may not be the best state from the point of view of controlling critical features’ CD and overlay drift, unless the residual aberration can be reduced to zero. In reality, due to limited degrees of freedom of lens manipulators as compared to the number of significant Zernike coefficients, the residual aberration generally cannot be reduced to zero for every coefficient. To address this issue, the lithographer must supply application-specific aberration sensitivity data of critical features in order to drive the optimization to the best state specific to the given application.

In this paper, we will describe a computational method and software tool developed to produce the application-specific aberration sensitivity data required by a scanner for lens manipulator optimization. We will discuss how to deal with the large number of critical features as often found in full-chip applications, high dimension of variable space (i.e., Zernike coefficients), non-linear effects and interactions among the variables. We will introduce a novel method that transforms a complex non-linear system to a compact linear system that enables the scanner to do the optimization in real time. We will demonstrate via simulation that this application specific aberration control yields better CD and overlay control performance compared with generic aberration control. An example is shown in Fig.1 where we simulated across-field overlay error as a result of thermal induced lens aberration for critical features in a memory chip design. It shows that new optimization method greatly reduces the error as compared to the standard method. Experimental validation of this method in actual chip manufacturer applications has been carried out and will be presented in a separate paper.

7640-22, Session 5

Aerial image calculation by eigenvalues and eigenfunctions of a matrix that includes source, pupil, and mask

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Various eigenvalue and eigenfuction approaches for aerial image calculation in partially coherent imaging have been introduced. The partially coherent imaging consists of three fundamental elements; a partially coherent source, mask and pupil. Each eigenfunction approach defines a matrix that contains at least one element out of the three fundamental elements. By analyzing the eigenfunctions obtained by decomposing the matrix, the property of the matrix can be determined.

Eigenfunctions obtained by a matrix defined only from a partially coherent source show a set of coherent sources [1]. The transmission cross coefficient (TCC) is defined by the source and pupil function. Decomposition of the TCC matrix referred to sum of coherent system (SOCS) [2] generates eigenfunctions that show interaction between features. Eigenfunctions of a matrix defined by the source and mask show coherent systems formed by source and mask [3]. In all cases, the first eigenfunction, which has the greatest corresponding eigenvalue of all eigenvalues, gives physical insight to the system. For example, the first eigenfunction of SOCS shows the constructive and destructive interference area [4].

In this paper, a matrix that contains source, mask and pupil is introduced in the pupil plan. We show there are two different matrices E and Z that contain source, mask and pupil. The matrix E, which is similar to the TCC matrix, is obtained by shifting the pupil function while the matrix Z is obtained by shifting the mask diffraction. By decomposing the matrices, we can obtain eigenvalues and eigenfunctions. The square sum of Fourier transform of eigenfunctions simply weighed by corresponding eigenvalues gives the final aerial image in both cases. The matrices E and Z have different elements, leading to different sets of eigenvalues and eigenfunctions. In addition, the number of eigenvalues of the matrix E is not equal to that of the matrix Z. Nevertheless, the final aerial image results are identical in both cases. For illustration, aerial image simulations are performed with various layouts. For an isolated contact and quadrapole illumination, the matrix E generates a set of 92 eigenfunctions while the matrix Z generates a set of only 14 eigenfunctions. Aerial images calculated by the both sets result in the same image. This example is a better case for the matrix Z. In other layout cases, the matrix Z shows no advantage to the matrix E. We show that the convergence characteristic of the matrix Z is related to von Neumann entropy. The entropy is affected by the illumination and its mutual coherence distribution. In the presentation, basic theory, algorithm and simulation result will be shown. Especially, the physical nature of the eigenfunctions for each approach and their convergence as well as how various mask patterns alter and reduce the entropy in the image will be illustrated.

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[2] N. B. Cobb, Ph.D. dissertation (UC Berkeley, 1998).

[3] H. Gamo, Progress in Optics, vol. 3,, chapter 3, (Publishing Company, North-Holland, 1964).

[4] R. Socha et al., Proc. SPIE 5377, 223-254 (2004).

7640-23, Session 5

Optimization from design rules, source, and mask, to full chip with a single computational lithography framework: level-set-methods-based inverse lithography technology (ILT)

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For semiconductor manufacturers moving toward advanced technology nodes -32nm, 22nm and below - lithography presents the greatest challenge, because it is fundamentally constrained by basic principles of optical physics. Because no major lithography hardware improvements are expected over the next couple years, Computational Lithography has been recognized by the industry as the key technology needed to drive lithographic performance. This implies not only simultaneous co-optimization of all the lithographic enhancement tricks that have been learned over the years, but that they also be pushed to the limit by powerful computational techniques and systems.

The Level-Set Method, invented by Professor Stan Osher (Luminescent's co-founder) and James Sethian in the 1980s, has been applied in many engineering fields, and is regarded as one of the most efficient mathematical methods for solving problems involving dynamic change of 2D patterns with topology changes. Level-Set-Method-based Inverse Lithography Technology (ILT) has been developed by Luminescent Technologies, Inc. over the last 6 years to address mask optimization efficiency, effectiveness, and complexity. Recently, the same Level-Set methodology has been applied to source optimization and Source-Mask optimization (SMO). Using this unified computational framework, consistent results and performance are easily obtained in both SMO (in the lithography development stage) and full chip mask optimization (in the OPC stage). By replacing the complicated segmentation setup, which requires exacting input from OPC experts, with a simple lithography-oriented configuration, the same framework can be used in both the design and lithography development phases to perform design rule optimization, source-mask optimization, and the combination of both, as well as full-chip correction. This also guarantees that the same lithography performance can be achieved when applying results obtained in design rule optimization and SMO to full chip OPC and SRAF.

The enabling technology in Level-Set-Method-based ILT is the level-set representation of the design, mask, wafer patterns and scanner source. Representing the 2D design pattern, mask pattern, and wafer pattern by level-sets is the most mathematically efficient way to represent 2D patterns, and gives the mask pattern practically infinite degree of freedom to change shapes during optimization (i.e., mask pattern OPC). It also solves the discontinuity problem in the mathematical formation when Sub-Resolution Assist Features (SRAF) are added into the mask patterns to enable printing of wafer patterns with better CD uniformity and larger process margin. Representing the scanner source as a level-set enables a free-form and gray-scale representation of the scanner source, and enables the source to change shape, size, and even topologies during the optimization. Another huge benefit of level set representation is that it provides a mathematically closed-form expression for the derivative of the function, which significantly improves the speed of any optimization by obviating numerical gradient calculation.

In this paper this single computational lithography framework will be explained in non-mathematical language. A number of memory and logic device results at the 32nm node and below are presented to demonstrate the benefits of Level-Set-Method-based ILT in applications covering design rule optimization, SMO, and full-chip correction.

7640-24, Session 5

Quadratic blur kernels for latent image formation modeling

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We present a bilinear photoresist model that is accurate, fast and reversible. Similar to other image-processing style (blur kernel) models, this model represents a transformation of an aerial image signal into a latent image signal. The key difference is an explicit recognition of the non-linearity of the process while retaining a standard signal processing architecture. By applying a Volterra series expansion to the reaction-diffusion functional, a high-accuracy yet intuitive approximation of the process is obtained. The method is compared to the Kelly model for photographic latent image formation, and is found to be equivalent under certain conditions. The Fourier transform of the Volterra kernel

is similar to the transmission-cross-coefficient function used in the analysis of optical image formation, and commonality is discussed. Several methods for identifying the double impulse response in the position space, or the bilinear transfer function in the frequency space are presented. Characterization is carried out for several of the calibrated photoresist models present in physical simulators. Differences in shapes of the bilinear transfer functions are discussed, including the impact of transfer function's shape on noise propagation. Expansion of the double impulse response into resist kernels for rapid forward calculation is presented. A method of aerial image synthesis from latent image or Bossung curves is discussed. The bilinear photoresist model is applied to the specification creation process of a k1=0.35 ArF scanner, and aerial image specifications are synthesized from process window shape requirements by projection. The aerial image requirements are in turn projected onto the eigenfunctions of the Karhunen-Loeve expansion in the aerial image space, identifying a suitable subspace. This subspace is finally projected into the space of possible pupil transmission function and source shape errors, creating a low-dimensionality requirement subspace for the optical system design process.

7640-25, Session 6

In-situ Mueller matrix polarimetry of projection lenses for 193-nm lithography

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For immersion lithography with aggressive polarization illumination settings, it is important to newly construct two systems for diagnosing lithography tools; one is Stokes polarimetry of illumination, and the other is Mueller matrix polarimetry of projection lenses. At the SPIE conference on Optical Microlitography XXI, the authors had already reported on the Stokes polarimetry. True polarization states of several illumination settings were clearly shown to the audience. On the other hands, the Mueller matrix polarimetry that the authors constructed is thought more complecated than the Stokes polarimetry. Therefore, the Mueller matrix polarimetry is reported seperating into two papers. The new theory has reported at the SPIE conference on Lithography Asia 2009.

The test mask for the Mueller matrix polarimetry also comprises thin-plate polarizers and wide-view-angle quarter-wave-plates, both which are developed by collaboration with Kogakugiken corporation. Mueller matrices of the sample projection lens are reconstructed by several measurements of Stokes parameters of a light travelling through the test mask and the projection lens with a polarization measurement system at the wafer plane.

7640-26, Session 6

Experimental result of polarization characteristics separation method

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Extension of immersion lithography requires the use of innovative resolution enhancement techniques such as computational lithography. Therefore, an effective image forming simulation that incorporates a well characterized vectorial fingerprint of hyper-NA optics is necessary. Within the vectorial lens treatment, the polarized light diffracted by the reticle pattern is subject to transformations quantified by Jones matrices whose formalism complicates the lens fingerprint model considerably.

Even though the Jones matrix is more complicated than scalar parameters, we successfully obtained a Jones matrix at the pupil plane of NA1.30 immersion test optics installed on a test bench. The reconstruction method is based on the concept of the first canonical coordinate of the Lie group, which conjures up a geometrical approach. The basis of Jones matrices, i.e., Jones polarization N-matrix (JPN matrix), proposed by R. C. Jones in the 1950's, is also included in the concept of the first canonical coordinate of the Lie group.

Hyper-NA illumination optics are also necessary to characterize the hyper-NA optics en bloc for high precision polarization characterization. However, inserting polarization optics to control the polarization status of the incident light for inspection between the hyper-NA illumination optics and the measured hyper-NA optics is practically impossible because of the high incident angle. Therefore the polarization optics have to be inserted before the illumination optics, which also have finite polarization characteristics to be measured. We have constructed a method for separating the Jones matrices of the hyper-NA optics and the illumination optics so that we can obtain the true polarization characteristics of the hyper-NA optics excluding the impact of the measurement system. This method is also able to handle the Jones pupils of the optics in JPN space. The simulated results of the separation method have shown that the separated wavefront error is 0.12 m lambda peak-to-valley and the separated diattenuation error is below 0.1 percent using vertical and horizontal linear polarized illumination.

In this paper, we will present the experimental results of this method for separating the Jones matrices of the two test optics on the test bench.

7640-27, Session 7

Implementing and validating double patterning in 22-nm to 16-nm product design and patterning flows

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In double patterning technology (DPT) we study the complex interactions of layout creation, physical design and design rule checking flows for the 22nm and 16nm device nodes. DPT methods decompose the original design into two individual masking layers. The decomposition of the original design for a double patterning process has an inherently global problem in which the influence of a local decomposition decision can be felt across an entire pattern. On account of complexity in double patterning steps, DPT decomposition and verification are critical steps for both physical design creation and the mask synthesis flow.

Decomposition includes the cutting (splitting) of original design intent features into new overlapping polygons where required; and the coloring of all the resulting polygons into two mask layouts. We discuss the advantages of geometric distribution for polygon operations with the limited range of influence. Further, we find that even the naturally global coloring step can be handled in a geometrically local manner. In some practical cases, up to 85% of the work can be distributed geometrically. Some of these methods of geometric distribution result in superior output symmetry and hierarchic preservation, reducing output file size. Wafer data on these topics will also be presented. We analyze and compare the latest methods for designing, processing and verifying DPT methods including for 22nm and 16nm nodes.

7640-28, Session 7

Comparative study of line-width roughness (LWR) in next-generation lithography (NGL) processes

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Line width roughness (LWR) is one of the many challenges we must overcome for sub-40 nm half pitch lithography. In this paper, we conduct a comprehensive comparative study of next-generation lithography processes in terms of their LWR performance. We investigate mainstream options such as litho-freeze-litho-etch double patterning, self-aligned double patterning (SADP), and EUV as well as alternatives such as directed self-assembly (DSA) and nano-imprint lithography (NIL). Given the distinctly different processing steps, LWR arises from different sources for these patterning methods, and a unified, universally applicable set of metrics must be chosen for useful comparisons. For each NGL, we evaluate the LWR performance in terms of three descriptors, namely, the variation in amplitude ( ),

correlation length ( ) and the roughness exponent ( ). In certain cases, we evaluate the LWR performance both before and after etch. However, given that each technology is at different level of maturity, fair post-etch comparisons between NGL options are not straightforward. Approaches for meaningful comparison of post-etch LWR across technologies will be considered and assessed.

Based on our study, we find that the roughness exponent (which corresponds to the relative contribution of high-frequency components) is close to one (1) for all NGL processes considered. The correlation length (which indicates the distance along the edge beyond which any two linewidth measurements can be considered independent) for NGL processes is found to range from 10 to 25 nm. The LWR percentage (defined as 3 LWR divided by half pitch) ranges from 8 to 21 percent.

Using EUV as an example, we show the importance of process optimization as these methods mature. We show the effects of resist type, resist thickness, under-layer type, and post-develop processing in determining the LWR of the final profile.

Finally, we conclude by reflecting on the 2008 updated ITRS roadmap.

7640-29, Session 8

Toward perfect on-wafer pattern placement: stitched overlay exposure tool characterization

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Continued lithographic pattern density scaling depends on aggressive overlay error reduction.1,2 Double patterning processes planned for the 22nm node require overlay tolerances below 5 nm; at which point even sub-nanometer contributions must be considered. In this paper we highlight the need to improve the single-layer matching among the three pattern placement mechanisms intrinsic to step&scan exposure - optical imaging, mask-to-wafer scanning, and field-to-field stepping. Without stable and near-perfect pattern placement on each layer, nanometer-scale layer-to-layer overlay tolerance is not likely to be achieved.

Conventional paired-layer overlay sees only the relative error between two layers; it is blind to the absolute placement accuracy within each layer. Stitched overlay provides an easily accessible window on single-layer pattern placement performance. Stitched overlay is enabled by a mask layout and single-pass exposure strategy that interlocks targets along the sides of intentionally overlapped neighboring fields, without requiring alignment to a prior-level pattern.3 We use dense sampling to capture the high spatial frequency discrepancies between the field-to-field and the intrafield pattern placement; it allows us to investigate placement error on individual tools and layers with sub-nanometer resolution.

Figure 1 shows a 300mm wafer map of stitched overlay error vectors, where our sampling of 13 targets along each side gives a detailed view of the stepping, scanning and optical errors present in each field on the wafer. We have developed a model to deconstruct the complex behavior of the observed errors into systematic root-cause constituents. Figure 2 illustrates the measured and model agreement as a function of the along-slit and -scan sides of an average of sixteen fields. Stitched overlay is commonly used to discern intrafield errors, but we will also show that, with appropriate modeling, it can pinpoint interfield errors.

Stitched overlay testing is an effective and efficient way to quantify many (alas, not all) sources of exposure tool overlay error. Our paper presents data representative of state-of-the-art 193 immersion tools, details of our mask layout, measurement and analysis approach, and our outlook for the pattern placement optimization of current and future lithography tools. We expect that the densely sampled stitched overlay method we describe here will be a key basis for that optimization.

7640-30, Session 8

Impact of scanner signatures on optical proximity correction

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Low pass filtering of image diffraction orders in the projection tools used for leading-edge microelectronics manufacture, leads to a range of optical proximity effects, OPEs, limiting the control of the integrated circuit pattern images. To correct these predictable OPEs, the Electronic Design Application, EDA, industry developed various, model-based optical proximity correction, OPC, methodologies, the success of which strongly depends on the completeness of the imaging models they use. Commonly used OPC models are capable of correcting OPEs driven by the fundamental imaging conditions, such as reticle technology and scanner setup.

For any given pattern reticle, the image formation in scanners is driven by the illuminator settings and the projection lens NA. These images are modified by the scanner engineering impacts due to: 1) the illuminator signature, i.e. the distributions of illuminator field amplitude and the polarization, 2) the projection lens signatures representing projection lens aberration residue and the flare, and 3) the reticle and the wafer scan synchronization signatures. These scanner impacts modify the critical dimensions of the pattern images at the level comparable to the required image tolerances. Therefore, to reach the required accuracy, the OPC models have to imbed the scanner illuminator, projection lens, and synchronization signatures.

OPC models imbedding scanner signatures are now available to the integrated circuit designers through collaboration of scanner and EDA vendors. The effectiveness of these models has yet to be fully quantified for the accuracy, database volumes and runtimes. To study their effects on OPC and OPC verification, we set up such imaging models imbedding various scanner signatures, and we used them to conduct the OPC of a poly gate level of 4x nm SRAM. By applying the scanner-based OPCs and verifying their performance, we were able to quantify the impacts of various scanner signatures on the OPC accuracy.

In this presentation, we review various scanner signatures and their roles in image formation. We show that imbedding scanner signatures result in dramatic improvements in imaging model accuracy. We show examples of OPC applied to the layouts of the current generation of ICs, and we present the results of OPC verification.

7640-31, Session 8

Overlay characterization and matching of immersion photoclusters

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Many factors are driving a significant tightening of the overlay budget for advanced technology nodes, e.g. 6nm [mean + 3] for 22nm node. Exposure tools will be challenged to support this goal, even with tool dedication. But tool dedication has adverse impact on cycle time reduction, line productivity and cost issues. There is a strong desire to have tool to tool (and chuck to chuck) matching performance which supports the tight overlay budgets without tool dedication. In this paper we report improvements in overlay metrology test methods and analysis methods which support the needed exposure tool overlay capability.

In this paper we describe a new methodology to fully characterize the overlay performance on the scanner. A dedicated reticle with 13x13 measurement sites across the image field is used, allowing more than 15000 data points per wafer. To avoid reticle pattern placement error contributions, both 1st level and 2nd level overlay test patterns are on the same reticle, and engage via a small shift between exposure passes. For convenience, we use a process in which the same layer of resist is used for both exposure passes. For overlay metrology we use a novel scatterometer method with high accuracy and throughput.

This paper will present data from both dry and immersion expose tools. Our experimental exposures, data sampling and data analysis methods seek to decompose the many individual components of overlay error. Figure 1 shows examples of overlay vector maps exposed in three different ways from a single immersion tool. Changing chuck between

the two passes, Fig. 1b, increases the overlay residuals relative to dedicating the same chuck, Fig. 1a. By forcing the two passes to have reversed scan direction, as in Figure 1c, we observe new overlay error components. Detailed analysis methods will be used to quantify grid, intrafield, scan direction and many other overlay error components. Exposure tool stability and matching issues will be assessed.

7640-32, Session 8

Topcoat-less resist approach for high-volume production and yield enhancement of immersion lithography

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Immersion lithography has become the mainstream for patterning IC features below 40 nm half pitch. Continuous demand for enhanced productivity has been pushing the scanner suppliers to improve scan speed of their scanners. The NSR-S620 is the latest immersion lithography scanner by Nikon with greatly enhanced scan speed compared to previous generation scanner, S610C.

Topcoat-less (TC-less) resist is an attractive process candidate compared to a topcoat process because it reduces both the cost of topcoat and its related process optimization time, and at the same time, it generally can attain higher hydrophobicity. Higher hydrophobicity is advantageous for high speed scanning because of stable movement of water meniscus, resulting in better defectivity performance. Using a Hydrophobicity Measurement Tool (HMT), developed by Nikon, dynamic receding contact angle (D-RCA) of various TC-less resists and topcoats can be analyzed. Correlation between D-RCA and defect performance will be discussed in this paper.

Blob defect reduction is one of the challenges with highly hydrophobic TC-less resist process, because hydrophobic surface repeals rinse water applied during development rinse process hence generating blob defect. In order to overcome these challenges collaboration between resist and track suppliers in improving TC-less resist material and optimization of development rinse process are crucial. In this paper we will present some of the achievements.

Higher resist sensitivity is another key factor for high scan speed lithography. Resist sensitivity is generally associated with a trade-off known as Line Edge Roughness (LER). The imaging and defectivity performance of the latest high sensitivity TC-less resists after an extensive collaboration with resist suppliers will be discussed.

Due to continuous pattern size shrinkage smaller size defects have become more pronounced and must be taken into account. Detection of such small size defects is trivial and their generation mechanisms are not very well known. To understand their generation mechanism a defect review before and after development was conducted which revealed small and faint changes in surface condition of a TC-less resist or topcoat, caused by immersion water contact, could be a cause of small size defects. Detailed experimental results will be shown.

To achieve steady and low defectivity performance, not only material and process improvement but also enhancements in immersion lithography tool are an important factor. Periodical tool cleaning greatly improves defectivity performance and for this reason in-situ cleaning proves to be indispensable. In-situ cleaning allows more frequent cleaning without the potential downtime associated with offline cleaning or possible parts exchange. Several in-situ cleaning methods have been developed and their effectiveness will be presented in this paper.

7640-33, Session 8

Analysis of pupil shape variation by pupil fit modeling

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As K1 factor for mass-production of memory devices has been decreased down to almost theoretical limit, the process window of lithography is getting much smaller and the production yield has become more sensitive to even small variations of the process in lithography. So it is necessary to control the process variations more tightly than ever. In mass-production, it is very hard to extend the production capacity if the tool to tool variation of scanners is not minimized.

We have explored a lot of scanner parameters to discover the main contributors of the variations and we have found that one of the most critical sources is pupil shape. So it is very critical to qualify the shape of pupils in scanners to control tool to tool variations.

Generally the pupil shape has been analyzed by using a few basic parameters to define pupil shape, but these basic parameters, sometimes, cannot distinguish the tool to tool variations caused by differences in pupil shape. It has been found that the pupil shape can be changed by illumination misalignment or damages in optics and theses changes can have a great effect on critical dimension(CD), pattern profile or OPC accuracy, etc. These imaging effects are not captured by the basic pupil parameters and the correlation between CD and pupil parameters will become even more difficult with the introduction of more complex illumination pupils.

In this paper, pupil shapes with more parameters were analyzed and the impact of pupil shape variations on critical features using new algorithm was discussed. The tool to tool mismatching in gate layer of flash memory device was demonstrated for an example. Also, we have tried to interpret which parameter is sensitive to CD and profile of the features through the simulation with the pupil parameters after pupil measurement at scanners. It was found that CD difference in critical feature can be corrected by pupil matching between the tools with new diagnostic technology.

It was also demonstrated that the extension of this new model was very effective to hot spot detect at full chip level through model based verification(MBV) and it was possible to predict hot spots caused by abnormal pupil shapes. In conclusion, new analysis on the pupil characteristics and the filtering system to detect narrow process window will be presented.

7640-34, Session 9

Predicting and reducing substrate-induced focus error

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The ever shrinking lithography process window has prompted us not only to maximize our process window and minimize tool-induced process variation, but also to quantify the disturbance to an imaging process caused upstream of the actual imaging step. Such factors include across-wafer and wafer-to-wafer film thickness variation, Si-wafer flatness, wafer edge effects as well as design-induced topography. We have quantified these effects and are presenting efforts to reduce their harm to the imaging process. With respect to topography induced focus error, we are presenting our effort to predict design-induced leveling hot-spots at the edge of our process window. This effort is geared towards enabling a constructive discussion with our design team and thus allowing us to mitigate focus hot-spots upstream of the imaging process.

7640-35, Session 9

Lithographic scanner stability improvements through advanced metrology and control

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As the k1 factor moves towards 0.25, scanner performance and operational stability are the key enablers to meet device scaling

requirements at and below 32 nm. Achieving these requirements in production calls for a dual approach. First, the intrinsic lithographic performance of the scanner is accurately characterized and the optimum machine setup is verified. Secondly, scanner setup performance is maintained using monitor wafer based control loops fueled with high speed, accurate and precise metrology information. To achieve the optimum scanner performance and control required for 32nm design rules, diffraction-based optical dimensional scatterometry was selected. This is the metrology of choice, because of its capability to generate greater amounts of data in a shorter time than other metrology techniques and platforms.

The paper focuses on using scatterometry for scanner stability control on monitor wafers. We will also present initial results from lithography-specific metrology on product wafers. For this, the primary parameters to control are across-wafer and across-field focus and overlay. The required metrology accuracy and precision of focus and overlay were achieved through new developments in the area of marker design and measurement algorithms. This optimization is characteristic to scatterometry. In a typical flow, comparisons are shown between measured versus induced scanner disturbances on monitor wafers. Robustness against process variations and rework was also evaluated. These results are then used in conjunction with a number of innovative developments in the area of control algorithms. The potential stability improvements achieved will be shown.

7640-37, Session 9

Scanner-to-scanner automatic OPE matching: experimental tests

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As is now widely known, the design variations of lithographic scanners from different vendors cause them to have slightly different optical-proximity effect (OPE) behavior, meaning that they print features through pitch in distinct ways. This in turn means that their response to OPC is not the same, and that an OPC solution designed for a scanner from Company 1 may or may not work properly on a scanner from Company 2. Since OPC is not inexpensive, that causes trouble for chipmakers using more than one brand of scanner. We previously reported a method and a software system to perform vendor-to-vendor scanner OPE matching. Further development of the software system yielded three separate methods: an aerial-image matching method, requiring detailed scanner information, a resist-CD methods, requiring detailed process information, and a hybrid or simple-resist method, requiring resist CD and minimal scanner information. Each uses the same sophisticated statistical techniques. Selection of each method depends on the information available to the engineer.

The aerial-image technique is the easiest and may be expected to be the most reliable. It requires detailed information from not only the Nikon scanner but also from the target scanner. Generally this information is simply a pupilgram collected from the target tool using on-board diagnostics. The advantage of this method is that it requires no resist information. Previously we have demonstrated theoretical support for the assertion that matching aerial images also matches resist images. The full resist CD method can be used when a target pupilgram is not available (e.g. for confidentiality reasons). It requires a full calibrated resist model of the process in use. Resist CDs are calculated for the Nikon tool and matched to experimental data from the target tool. The hybrid method is used when neither target-scanner details nor a calibrated resist model is available. It constructs a kind of primitive resist model to transform from resist CD data back into the aerial-image space. It is the most flexible but possibly the least accurate. The Nikon scanner is tuned (in modeling) using at least lens NA and illuminator adjustments. Other tuning knobs are under evaluation. All three methods use the same sophisticated nonlinear mathematical techniques to model the Nikon scanner and arrive at the best matching solution. Response of the system to tuning knobs is inherently nonlinear and we believe that this treatment is necessary. We expect to present experimental data validating this tuning and matching system.

7640-38, Session 9

Using scanner metrology and design data to reduce reliance on CD metrology in simulation-based pattern matching

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Traditional scanner matching methods have relied heavily on wafer-based CD metrology to characterize both the initial mismatch as well as the sensitivity of CDs to scanner tuning knobs. While these methods have proven to be very successful in reducing the mismatch, their actual deployment in manufacturing has been hampered by the effort involved in obtaining the wafer CD data. In this paper, we explore the possibility to use simulated CDs based on models (an improved AI-based method) that maximize the use of scanner metrology & design data thereby reducing the dependence on wafer CD metrology.

We focused our study on the case of matching an XT:1900i immersion ArF scanner to an XT:1400 ArF dry scanner in 55nm device making. As a control, we established the baseline improvement in matching performance from the unmatched state, using identical nominal scanner settings, to the matched state, based on manipulator adjustment recipes derived from extensive wafer CD measurements. We then compared this baseline improvement to the results we obtained from matching the same two scanner based on simulated CDs, using models with maximal reliance on scanner metrology and design data in combination with minimal reliance on wafer CD data.

In this paper we describe both methods and present their predicted and actual improvement in matching performance as well as a cost benefit analysis by comparing the relative performance of the methods to the amount of metrology involved with the methods. The paper concludes with a set of recommendations on the relative merits of each method for a variety of use cases.

7640-39, Session 9

The GridMapper Challenge: how to integrate into manufacturing for reduced overlay error

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More sophisticated corrections of overlay error are required because of the challenge caused by technology scaling faster than the fundamental tool improvements. This talk will briefly review the basic challenges of overlay error and previous standard correction practices. It will then describe implementation of a new correction technique, which has been applied in IBM manufacturing, successfully utilizing GridMapper. This paper also describes the challenges we have faced and the improvements in overlay control that have been observed with the use of this technique.

Specifically, this paper will illustrate several improvements:

1. The difference in non-linear grid signatures between tools is minimized
2. Optimization of overlay corrections across all fields
3. Decreased grid errors, even on levels not using GridMapper.
4. The grid is maintained for the lifetime of a product.

5. Effectiveness in Manufacturing - cycle time, automated corrections for tool grid signature changes, overlay performance similar to dedicated chuck performance, etc.

7640-40, Session 9

Simultaneous optimization of dose and focus controls in advanced ArF immersion scanners

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ArF water immersion lithography is expected to be used down to 22nm hp node until EUVL becomes mature. The process margin is therefore very small from 45nm hp node and double patterning techniques are required below 35nm hp. In order to obtain sufficient CD uniformity (CDU), optimization of dose and focus controls is indispensable in determining the proper inter- and intra-field control parameters.

A technique of the simultaneous measurement of dose, focus and blur from scatterometry (OCD) measurement data on grating patterns was reported by C.P.Ausschnitt and T.A.Brunner in 2007 [1]. We apply a similar technique for dose and focus with the optimized design of measurement marks in order to obtain better CD uniformity. Blur analysis is not included here because a flexible blur control is not realistic in current ArF immersion scanners.

The procedure for the improvement of CD uniformity is as follows;

1)Wafer exposure with dose/focus variation and OCD measurement,

2)Modeling of dose = f (MCD, Height), focus = g (MCD, Height),

3)Wafer exposure with nominal dose/focus and OCD measurement,

4)Making error maps of dose and focus using modeled dose and focus functions,

5)Determination of inter- and intra-field control parameters for dose and focus,

6)Wafer exposure with optimized control parameter values.

Here NSR-S610C(NA=1.30)(exposure tool) and KLA-SCD100 (OCD tool) are used.

In this paper, experimental results of CDU improvement using this method are introduced and its effectiveness is clearly proven.

References:

[1]C.P.Ausschnitt and T.A.Brunner, Proc. SPIE 6520, 65200M (2007).

7640-69, Session 9

Printing the metal and contact layers for the 32- and 22-nm node: comparing positive and negative tone development process

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A strong demand exists for techniques that can further extend the application of ArF immersion lithography. Besides techniques like litho-friendly design, dual exposure or patterning schemes, customized illumination modes, also alternative processing schemes are viable candidates to reach this goal. One of the most promising alternative process flows uses image reversal by means of a negative tone development (NTD) step with a FUJIFILM solvent-based developer. Traditionally, the printing of contacts and trenches is done by using a dark field mask in combination with positive tone resist and positive tone development. With NTD, the same features can be printed in positive resist using a light field mask, and consequently with a much better image contrast.

In this paper, we present an overview of applications for the NTD technique, both for trench and contact patterning. This experimental work was performed on an ASML XT:1900i scanner at 1.35 NA, and targets the contact/metal layers of the 32 & 22 nm node.

For trench printing, we demonstrate the use of light field line patterns on mask in combination with negative development. With this flow, trenches in resist are achieved that do not only have remarkably better imaging properties (EL and MEEF) through pitch, but also can reach down to smaller target sizes in comparison to traditional dark field trench printing (see figure below). We study not only one-dimensional patterns, but also perform an experimental study of the printing performance of line ends and two-dimensional structures as we believe this to be one of the important benefits of light field trench imaging for double patterning of the metal layer.

For contact hole printing using NTD, we consider both single and dual exposure schemes. In particular for single exposure of contacts, we demonstrate how the imaging resolution for light field with NTD is much better compared to traditional dark field printing (see figure below). For dual exposure schemes, the applicability of dual line exposure for contact patterning is demonstrated for a large variety of use cases.

This experimental study proves the added value of the negative tone development scheme. For contacts and trenches, it allows achieving smaller pitches and/or smaller litho targets, which makes this process flow attractive for the most advanced lithography applications, including double patterning.

7640-62, Poster Session

The impact of resist model on mask 3D simulation accuracy beyond 40-nm node memory patterns

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Beyond 40nm lithography node, ArF lithography requires strong RET resulting in optical proximity effects which impact pattern transfer significantly. Precise and accurate forecasting of the wafer pattern requires that mask topography effects are fully considered during lithography simulations. Many studies have focused on the difference of aerial image between Kirchhoff and rigorous EMF simulation, however, ArF resist kinetics also play an important role which impacts the real image obtained on the wafer .The purpose of this work is to predict the wafer CD and process window precisely using 3D mask simulation and a resist model.

Although a full physical resist model mimics the behavior of a resist material with rigor, the required iterative calculations can result in an excessive execution time penalty, even when simulating a simple pattern. Simplified resist models provide a compromise between computational speed and accuracy. We will calibrate both the full physical and simplified resist models for 2D and 3D mask simulations.

We will quantify the difference of the CD and process window between experiments and simulations for the carious model combinations across a range of 40nm node flash memory patterns. The experimental results will also be compared against aerial image and image in resist threshold models to gauge the importance of using any resist model.

The most efficient simulation approach (i.e. accurate prediction of wafer results with minimum execution time) will have an important position in mask 3D simulation.

7640-63, Poster Session

Comparison of OPC models with 3D mask effect

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In lithography textbooks, it is told that 3D-mask effect should be taken care of when mask CD is smaller than the scanner wavelength. Nominal mask CD has reached the limit a year ago, but still, OPC models do not consider the 3D-mask effect in common. In large amount, this is because the resist part of OPC model overfits optical properties like the 3D-mask effect.

We give some examples in which the resist models fail to compensate the 3D-mask effect. In some cases, models without the 3D-mask effect can not reduce model RMS (of residuals) enough. In other cases, models without 3D-mask effect show good model RMS but fail to predict some critical CD tendencies. Rigorous simulations predict the CD tendencies, which confirm that the discrepancy really comes from 3D-mask effect.

Runtime should be further reduced to fully adopt OPC modeling with 3D-mask effect.

7640-64, Poster Session

Virtual fab flow for wafer topography aware OPC

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The introduction of immersion processes in combination with aggressive resolution enhancements techniques have enabled device shrinkage down to the current 45nm technology node. Small feature sizes, complex mask stacks. and strong off axis illumination require optical proximity correction (OPC) models to take mask topography effects into account. However, in spite of wafer planarization process steps, wafer topography effects induced by different optical properties of the patterned materials start playing a significant role, and correction techniques need to be applied in order to minimize the impact of those effects.

In this paper, we study a methodology to create models taking into account both the optical proximity effects originating from the imaging system as well as from the patterned wafer substrate, with the goal of performing OPC as well as wafer topography proximity correction (WTPC).

A comprehensive data set is required to build a reliable OPC model. We present a “virtual fab” flow using extensive test pattern sets with both 1D and 2D structures to capture optical proximity effects as well as wafer topography effects.

A rigorous lithography simulator taking into account source maps, topographic mask effects as well as wafer topography is used to generate virtual measurement data, which are used for model calibration as well as for model validation.

For model building, we use a two step procedure: in a first step, an OPC model is built using test patterns on a planar, homogenous substrate; in a second step. a model for WTPC is fitted, using results from simulated test patterns on a shallow trench isolation (STI) layer. This approach allows to build models from experimental data, including hybrid approaches where an existing OPC model can be retrofitted with capabilities for correcting wafer topography effects.

We analyze the relevant effects and requirements for model building and validation as well as the performance of fast models for WTPC.

7640-66, Poster Session

Interlayer self-aligning process for 22-nm logic

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Line/space dimensions for 22nm logic are expected to be ~35nm at ~70nm pitch for metal 1. However, the contacted gate pitch will be ~90nm because of contact-to-gate spacing limited by alignment. A process for self-aligning contact to gates and diffusions could reduce the gate pitch and hence directly reduce logic and memory cells sizes.

Self-aligned processes have been in use for many years. DRAMs have had bit-line and storage-node contacts defined in the critical direction by the row-lines. More recently, intra-layer self-alignment has been introduced with spacer double patterning, in which pitch division is accomplished using sidewall spacers defined by a removable core.[1] This approach has been extended with pitch division by 4 to the 7nm node.[2]

The introduction of logic design styles which use strictly one-directional lines for the critical levels gives the opportunity for extending self-alignment to inter-layer applications in logic and SRAMs. Although Gridded Design Rules have been demonstrated to give area-competitive layouts at existing 90, 65, and 45nm logic nodes while reducing CD variability[3], process extensions are required at advanced nodes like 22nm to take full advantage of the regular layouts.

The critical step in the proposed process is a blanket illumination of the wafer after the PMD (pre-metal dielectric) deposition and planarization. After the PMD CMP step, an additional dielectric material is deposited, followed by hard-mask deposition and photoresist coating.

The film stack thickness and optical properties were developed using the KLA Prolith 11 simulation software. This allowed rapid selection of films with the proper n and k values, as well as iteration to the right thicknesses and illumination dose. Figure 1a shows a cross-section of the post-develop resist profile.

A film stack was prepared at SVTC using the Prolith results. Blanket illumination was done on an ASML 1250 scanner using a dose meander program with no reticle. The top-down SEM view of a 250nm line/space pattern is shown in Figure 1b, after resist development. The actual dose needed matched the simulation results.

Further simulations are in progress with gate layouts more representative of the 22nm node.

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7640-67, Poster Session

Process-window and integration results for full-chip model-based assist-feature placement for the 32-nm node and below

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Model-based assist-feature (MBAF) placement has been shown to have considerable lithographic benefits vs. rule-based assist-feature (RBAF) placement for advanced technology-node requirements. For very strong off-axis illumination modes, MBAF-placement methods offer improved process window, especially for so-called forbidden pitch regions, and greatly simplified tuning of AF-placement parameters. Historically, however, MBAF-placement methods had difficulties with full-chip runtime, friendliness to mask manufacturing (e.g., mask rule checks or MRCs) and implementation of methods to ensure that placed AFs do not print on wafer. Therefore, despite their known limitations, RBAF-placement methods were still the industry de facto solution through the 45nm technology node.

In this paper, we highlight recent manufacturability advances for MBAFs by a detailed comparison of MBAF vs. RBAF methods on several large full-chip products. The MBAF method employed uses inverse mask technology (IMT) to optimize AF placement, size, shape and software runtime, to meet the production requirements of the 28 nm technology node and below. MBAF vs. RBAF results are presented for full-chip runtime, memory usage, MRC compliance, full process window, assist-feature printing and final optical proximity correction (OPC) accuracy. The method of integrating the MBAF placement method to the OPC routines is shown to be a key enabler of more accurate OPC and preventing unwanted feature printing. Different optimization parameters accurately modeling IMT and assist feature printing are also discussed. The final results show that MBAF methods are not only full-chip manufacturing capable but have increasing process-window and manufacturability advantages for each successive technology node below 45 nm.

7640-68, Poster Session

The role of mask topography effects in the optimization of pixelated sources

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Ongoing technology node shrinkage requires the lithographic k1 factor to be pushed close to its theoretical limit. The application of customized illumination with multi-shaped or pixelated sources has become necessary for improving the process window. For standardized employment of this technique it is crucial that the optimum source shape and the corresponding intensity distributions can be found in a robust and automated way. In this paper a pixelated source optimization procedure and its results are presented. A number of application cases are considered with the following optimization goals: i) enhancement of depth of focus, and ii) improvement of through-pitch behavior. The optimization procedure is performed with fixed mask patterns, but at multiple locations. In order to reduce optical proximity errors a mask biasing can be introduced. The optimization results obtained for the pixelated source shapes are analyzed and compared with the corresponding results for conventional sources. Starting with the 45nm node, mask topography effects as well as source polarization conditions in high-NA projection have significant impact on imaging performance. So, including these effects into the optimization procedure has become a must for advanced process nodes. The advanced topographical mask illumination concept (AToMIC) for rigorous and fast electromagnetic field simulation under partially coherent illumination is applied. The impact of mask topography effects on the results of the source optimization procedure is shown by comparison to corresponding Kirchhoff simulations. The effects of polarized illumination sources are taken into account.

7640-36, Poster Session

Experimental study of effect of pellicle on optical proximity fingerprint for 1.35 NA immersion ArF lithography

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To ensure defect-free printing, pellicles are mounted on the masks used in optical lithography for IC manufacturing. The pellicle, a thin transparent polymer film, protects the reticle from dust. It is mounted on a frame with a few mm's stand-off such that dust particles that land on the pellicle are so far out-of-focus that their image is not projected on to the wafer.

Because the 193 nm light transmittance through the pellicle has an angular dependency, the pellicle works as an apodization filter. The importance of this effect on optical proximity grows with increasing NA. Detailed simulation studies exist on the effects of a pellicle on the proximity, concluding that the pellicle's influence on CD may be non-negligible. Up to now, however, only very limited experimental data has been available showing the pellicle effect on resist CDs.

In the current work, we present both simulation and experimental results at 1.35 NA showing the effect of a pellicle on wafer CD in resist for a wide range of 1D and 2D light and dark field structures for the 32 nm node. Two types of pellicles, with different film thicknesses, are considered, each having their own effect (up to 2 nm) on the resist CDs (see Figure below).

These results indicate that the contribution of the pellicle to the scanner's optical fingerprint is important to consider when using thick pellicles. As a consequence, (dis-)mounting or changing an existing pellicle from a reticle will influence the optical proximity and thus may affect yield. Also Optical Proximity Correction should take the pellicle presence into account.

7640-70, Poster Session

Demonstration of sub-22-nm interference lithography through self-aligned double patterning

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Double patterning by interference lithography (ILDP) bears the promise of printing lines smaller than 22nm based on current technology. The inherent disadvantage of any interference lithography, namely the inability to define features but line/space, made the technology mainly the test platform for new resist materials and optics. As fewer options are available at printing ever smaller dimensions, interference lithography may play a more important role than it ever has. Two possible paths are available. One is to restrict the design rule to be ILDP compliable, i.e. 1D critical features only; the other is to make 2D structures through multiple exposures of multi-hardmask film stack. The latter obviously comes with the added process complexity and manufacturing cost. This paper demonstrates for the first time sub-22nm interference lithography through the use of self-aligned double patterning (SDDP). A hyper NA (NA>1.5) interferometer setup, known as the Amphibian system, was used to print resist gratings with sub-45nm 1:1 halfpitch. It was then chemically modified to 1:3 L/S. The patterned wafer was then processed using the standard SDDP flow at Applied Materials. The final pattern has sub-22nm 1:1 halfpitch. The feasibility of patterning 2D features through multiple exposures of multi-hardmask film stack is also investigated.

7640-71, Poster Session

Novel ATHENA mark design to enhance alignment quality in double patterning with spacer process

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A variety of double patterning schemes have been developed to pattern the 40nm technology node and beyond. Among them the DPS (Double Patterning with Spacer) is one of the most promising solutions in flash memory device manufacturing. Apart from the process complexity inherent with the DPS process, the DPS requires more engineering efforts compared to the single patterning alignment technique. Since the traditional alignment marks defined by the core mask has been altered [1]. As a result of subsequent process operations in DPS, the pitch and duty cycle of alignment marks have been very different to the original design, as shown in the Figure 1. The alignment mark recognition could be challenging for the subsequent process layers, accordingly the overlay performance could be worrisome.

In this paper, various types of sub-segmentations within the ASML VSPM and RVSPM marks were carried out to address alignment and overlay challenges in DPS process. The design of the transverse and vertical sub-segmentations within the ASML marks is aimed to enhance the alignment signal strength and mark detectability. Hence enhanced alignment and overlay performance can be obtained. Alignment indicators of WQ (Wafer Quality), MCC (Multiple Correlation Coefficient) and ROPI (Residual Overlay Performance Indicator) were used to judge the alignment quality and stability. Besides, process variations such as hard mask film stack, spacer height and spacer width were also employed to verify the robustness of the alignment strategy.

7640-72, Poster Session

Modeling of dry etch and film deposition in multispacer patterning technology

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The spacer patterning technique is an attractive way to fabricate patterns at resolutions far beyond the limits of traditional optical lithography. In this paper, we have simulated film deposition and dry

etch in spacer patterning at 32 nm and 22 nm designs. The spacer patterning technology is based on the fabrication of a spacer by conformal deposition of a material at the edge of a sacrificial layer followed by anisotropic etch of this material. When the sacrificial layer is removed, the spacer can be used as a hard mask to define structures in underlying layers.

Various resist thicknesses and profiles, as well as process conditions for film deposition and dry etch were used. Dynamics of etch profiles, resulting profiles, and critical dimensions (CDs) were extracted.

Multi-spacer patterning was also simulated. In the multispacer technique, the process was applied several times, resulting in the reduction of the lithographic pitch by a factor of 2n, where n is the number of spacer processing steps. Fabricated spacers were used as a sacrificial layer for the following processing.

7640-73, Poster Session

LENS (lithography enhancement toward nano scale): a European project to support double-exposure and double-patterning technology development

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In 2009 a new European initiative on Double Patterning and Double Exposure lithography process development was started in the framework of the ENIAC Joint Undertaking. The project, named LENS (Lithography Enhancement Towards Nano Scale), involves twelve companies from five different European Countries (Italy, Netherlands, France, Belgium Spain) and includes: IC makers (Numonyx and STMicroelectronics), a group of equipment and materials companies (ASML, LAM, JSR, FEI), a mask maker (Dai Nippon Photomask Europe), an EDA company (Mentor Graphics) and four research and development institutes (CEA-Leti, IMEC, Centro National of Microelectrónica, CIDETEC).

The LENS project aims to develop and integrate the overall infrastructure required to reach patterning resolutions required by 32nm and 22nm technology nodes through the double patterning and pitch doubling technologies on existing conventional immersion exposure tools, with the purpose to allow the timely development of 32nm and 22nm technology nodes for memories and logic devices, providing a safe alternative to EUV, Higher Refraction Index Fluids Immersion Lithography and maskless lithography, which appear to be still far from maturity.

The project will cover the whole lithography supply chain including design, masks, materials, exposure tools, process integration and metrology and its final objective is the demonstration of 22nm node patterning on available 1.35 NA immersion tools on high complexity mask set.

The paper aims at giving an overview of the LENS project, its activities and results to a broad audience of lithographers.

7640-74, Poster Session

Novel continuously shaped diffractive optical elements enable high-efficiency beam shaping

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Optical lithography with its 193 nm technology is pushed to reach and shift its limits even further. There is strong demand on innovations in illumination part of exposure tools. Current illumination systems consisting of diffractive and refractive optical elements offer numerous benefits such as optimized laser beam shape with extremely high homogeneity and high numerical aperture enabling high efficiency and improved throughput.

LIMO's unique production technology is capable to manufacture free form surfaces on monolithic arrays larger than 250 mm with high precision and reproducibility [1,2]. Different kinds of intensity distributions with best uniformities or customized profiles have been achieved by using LIMO's refractive optical elements.

Recently LIMO pushed the limits of this lens production technology and was able to manufacture first diffractive optical elements (DOE) based on continuous relief's profile. Beside for the illumination devices in lithography, DOEs find wide use in optical devices for other technological applications, such as optical communications and data processing [3].

Up to now DOE designs follow the principle of phase diffraction gratings. Its diffraction structure with a periodic phase profile performs a superposition of beams with predefined energy ratios. Due to the application for high precise laser-beam shaping and beam splitting in optical technologies and optical fiber networks, number of grating orders is increased up to some tens or even hundreds. Classic lithographic technologies lead to quantized (step-like) profiles of diffractive micro-reliefs [3], which causes a decrease of beam splitter's diffractive efficiency [3, 4]. The newest development of LIMO's microlens fabrication technology allows us to make a step from free programmable microlens profiles to diffractive optical elements with high efficiency. Our first results of this approach are demonstrated in this paper. Diffractive beam splitters with uniform distribution are presented. A special mathematical method [5] is used to design diffractive optical elements with continuous surface profiles. Comparison between theoretical simulations and experimental results shows very good correlation.

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7640-75, Poster Session

Advances in DOE modeling and optical performance for SMO applications in immersion lithography at the 32-nm node and beyond

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As alternative lithography approaches such as EUV and nanoimprint lithography continue to experience delays in their ability to meet the needs of the industry at the 32nm node and beyond, the requirements placed upon conventional optical lithography are increasing in complexity. The Diffractive Optical Elements (DOEs) used for off-axis illumination (OAI) have additional capabilities that have been relatively untapped for addressing these requirements. With the introduction of source mask optimization (SMO), it is important to understand the capabilities DOEs can provide with regard to pupil resolution and grey

tone intensity level control for freeform OAI solutions (see Fig. 1) in order to take full advantage of them.

In addition, many physical properties of the illumination that were assumed to have negligible impact on performance are becoming significant contributors to the CD budget. Factors like pole imbalance, stray light and zero-order hot spots can be unique to each given custom design. Understanding, minimizing and controlling these factors is vital to achieving optimal solutions for the most challenging designs.

To come up with a truly optimized SMO design, an understanding of what capabilities DOEs already have that can be employed, and how the physics and manufacturing tolerances of DOEs can change the output from the ideal design is required. It is possible to incorporate these factors and models up front in the iterative SMO design algorithms to find the most robust design. The result will then be a much needed improvement in the process window of critical layers and reduction of OPC rework required during process development to minimize development cycle timelines. To aid in these efforts, we present a comprehensive analysis of DOE constraints and capabilities, including both fundamental design aspects and manufacturing tolerances; as well as our recent advancements in the modeling and optical performance of DOEs for OAI.

7640-76, Poster Session

VLSI microlithography simultaneous source and mask optimization using Abbe-PCA with incremental Eigen decomposition

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With the growing need for high quality optical proximity correction (OPC) for deep-sub-wavelength microlithography. Not only the mask shape need to be complexly altered such as scattering bar, or phase shift mask, the light source shape, polarity, and intensity also acted as another optimization variable.

It is easy to see that one of the difficulties of developing simultaneous source mask optimization (SMO) algorithm is the kernel generation time for different set up. If we utilize the well-known Hopkin's method, then numerous expensive SVD operations for huge TCC matrices are required.

In the last SPIE conference, we proposed Abbe-PCA algorithm to perform eigen-decomposition on the correlation matrix (PCA) of the Abbe kernels. Since Abbe-PCA directly deal with Abbe kernel, it is very suitable to deal with SMO applications since only parts of kernels need slightly modification when changing sources setup.

Secondly, we discover that by taking advantage of the incremental properties of the optimization process, the PCA eigen-decomposition operation of the correlation matrix can also be performed incrementally as well. Therefore, exceptional runtime improvement is observed.

Finally, from the PCA-SVD relationship, i.e., H=USV', HV=US, (HH* is the TCC Matrix), we discover that through the tracking of V matrix, the importance of each Abbe kernels are observed during the optimization. This also provides precious info during SMO optimization.

Extensive experimental results demonstrate the efficiency and accuracy of our Abbe-PCA-SMO method.

7640-77, Poster Session

Optimization on illumination source with design of experiments

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In advanced photolithography process for manufacturing integrated circuits, the critical pattern sizes that need to be printed on wafer are much smaller than the wavelength. Thus, source optimization (SO) techniques play a critical role in enabling a successful technology node. However, finding an appropriate illumination configuration involves intensive computation simulations. EDA vendors have been developing source mask optimization (SMO) tools that co-optimize both source and mask for a set of patterns. As an alternative approach, we have introduced design of experiment (DOE) methodology for parameterized source optimization to minimize computation efforts while achieving comparable CDU control for given design patterns.

In the DOE approach, simulation runs generate multiple responses for design patterns that individually vary on input settings. An objective function of the several responses is constructed based on minimizing averaged relative CD variations, which simplifies the goal to the minimization of a single response. A response surface (RS) design, center composite face (CCF), is proposed to solve the problem with reduced runs. With an input dimension of eight, we choose a CCF of 273 runs, while 6,561 runs are usually run for a full factorial design. This approach identifies several optimal settings by adjusting inputs according to the second-order RS model. Verification runs showed that these solutions generate values smaller than the minimum of observed data but larger than the global minimum. Sequential experiments were designed and analyzed to explore the optimal region further.

The proposed approach largely improves the efficiency by reducing the number of experiments 30 times. It also enables us to explore a wide range of illuminator options and to understand the impact of illuminator parameters as well as trade offs among 1D, 2D, and SRAM design patterns.

7640-78, Poster Session

Source-mask optimization (SMO): from theory to practice

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As optical lithography continues to extend into the low-k1 regime with 193nm immersion NA practically limited to 1.35, it becomes increasingly important to extract the most from RET techniques, primarily illumination sources and masks. Source Mask Optimization (SMO) methods have therefore gained considerable interest over the last few years.

Inverse Lithography Technology (ILT) methods developed at Luminescent utilize its patented level-set algorithms which have already been proven to provide substantial process improvements over traditional OPC masks [1,2], both in simulations and production. The same level-set methods have been extended to source optimization, enabling computation of source-mask solutions that are most suited for a desired target or set of target patterns [3]. Such sources can be freeform, pixelated and/or a composite parameterized source which approximates the pixelated source. Furthermore, with access to scanner signature files, including scanner aberration data, scalar and vector, SMO solutions can be developed that are tuned to actual scanner characteristics.

In this paper, we present SMO solutions computed for a desired set of 22nm patterns, followed by experimental wafer data of the same. The gap between simulations and experiment are bridged by modeling and capturing as much of scanner, mask, and resist effects during the simulation/SMO computation phase itself.

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7640-79, Poster Session

Partial spatial coherence in an excimer-laser lithographic imaging system

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Excimer lasers operating in the Deep UV (193nm and 248nm) have been used in lithographic systems for the last couple of decades. The output from a pulsed excimer laser is spatially partially coherent. This adds complexity to simulations of light propagation through excimer imaging systems as partially coherent calculations require four-dimensional calculations. The reason for this is the correlation between fields at different points in space must be taken into account, so integration must be performed not just over all points of a two-dimensional field distribution, but over all pairs of points.

We have recently explored the Elementary Function method [1,2], previously presented by Wald et al [3] and, in the space-time and space-frequency domains, by Vahimaa and Turunen [4] and Friberg et al [5]. We have demonstrated under what circumstances this method can be used to reduce the propagation calculations of partially coherent light to two dimensions. This increases the speed of the calculations and reduces the need for high memory capacities.

In this paper, we extend our existing elementary function model to represent a lithographic system. We include spatial coherence measurements to improve the accuracy of our simulations and to make the model system-specific. In addition, the effect of homogenization of the beam on the coherence properties has been explored. Beam scrambling optics are often included in modern excimer laser based systems to condition the beam and improve beam uniformity over the full area of the object. We extend the existing simulation to include an imaging homogenizer with twin microlens arrays and propagate the cross-spectral density (partial coherence) through it. Results will be presented at the conference.

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7640-80, Poster Session

Flexible and reliable high-power injection-locked laser for double-exposure and double-patterning ArF immersion lithography

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ArF immersion technology is spotlighted as the enabling technology for the 45nm node and beyond. Recently, double exposure technology is also considered as a possible candidate for the 32nm node and beyond. We have already released an injection lock ArF excimer laser, the GT61A (60W/6kHz/10mJ/0.35pm) with ultra line-narrowed spectrum and stabilized spectrum performance for immersion lithography tools with N.A.>1.3, and we have been monitoring the field reliability data of our lasers used in the ArF immersion segment since Q4 2006.

We show GT series reliability data in the field. GT series have high reliability performance. The availability that exceeds 99.5% proves the reliability of the GT series.

We have developed flexible high power injection-lock ArF excimer laser for double patterning, GT62A (Max90W/6000Hz/Flexible power with 10-15mJ/0.35pm(E95)) based on the GigaTwin (GT) platform. Number of innovative and unique technologies are implemented on GT62A.

- Support the latest illumination optical system

- Support E95 stability and adjustability

- Reduce total cost (Cost of Consumables, Cost of Downtime and Cost of Energy&Environment)

7640-81, Poster Session

Laser-bandwidth effect on overlay budget and imaging for the 45-nm and 32-nm technology nodes with immersion lithography

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The laser bandwidth and the wavelength stability are among the important factors contributing to the CD Uniformity budget for a 45 nm and 32nm technology node Flash memory. Longitudinal chromatic aberrations are also minimized by lens designers to reduce the contrast loss among different patterns. The residual effect of laser bandwidth and wavelength stability are investigated and quantified for a critical DOF layer. Besides the typical CD implications we evaluate the “Image placement error” (IPE) affecting specific asymmetric patterns in the device layout. We show that the IPE of asymmetric device patterns can be sensitive to laser bandwidth, potentially resulting in nanometer-level errors in overlay. This is compared to the relative impact of other parameters that define the contrast of the lithography image for the 45nm node. We extend the discussion of the contributions to IPE and their relative weight in the 32 nm double-patterning overlay budget.

7640-83, Poster Session

Laser spectrum requirements for tight CD control at advanced logic technology nodes

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Tight circuit CD control in a photolithographic process has become increasingly critical particularly for advanced process nodes below 32nm, not only because of its impact on device performance but also because the CD control requirements are almost at the limit of measurement capability. Process stability relies on tight control of every factor which may impact the photolithographic performance. The variation of circuit CD depends on many factors, for example, CD uniformity on reticles, focus errors, lens aberrations, partial coherence variation, photoresist performance and laser spectrum. Laser bandwidth and illumination partial coherence are two of the largest contributors to the proximity CD portion of the scanner CD budget. It has been reported that bandwidth contributes ~9% to the CD budget, which is equivalent to ~0.5nm at the 32nm node. In this paper, we are going to focus on controlling laser spectrum effects to reduce circuit CD variation for the 32nm node and beyond. Laser parameters, e.g. central wavelength, spectral shape and bandwidth, will be input into the photolithography simulator, Prolith, to calculate their impacts on circuit CD variation. Mask-bias dependent lithographic performance will be calculated and used to illustrate the importance of well-controlled laser performance parameters. Stable though-pitch proximity behavior is one of the critical topics for foundry products, and will also be described in the paper. Recommended laser parameter requirements will be proposed, based on both simulation results and experimental data to ensure that the tight CD control required for advanced technology node products can be achieved.

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7640-125, Poster Session

Lithography light-source fault detection

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High productivity is a key requirement for today's advanced lithography exposure tools. Achieving targets for wafers per day output requires consistently high throughput and availability. One of the keys to high availability is minimizing unscheduled downtime of the litho cell, including the scanner, track and light source. From the earliest excimer laser light sources, Cymer has collected extensive performance data during operation of the source, and this data has been used to identify the root cause of failures on the system. Recently, new techniques have been developed for more extensive analysis of this data to characterize the onset of typical end-of-life behavior and allow greater predictive capability for identifying both the type of upcoming service that will be required and when it will be required.

The new techniques we will describe are reliant on two core elements of our lightsource data management architecture. The first is Cymer On Line (COL) which facilitates collection and transmission of lightsource data; the second is enhanced performance logging features added to our newer-generation lightsource software that capture detailed performance data around events of interest. Extensive analysis of the performance data collected using this architecture has demonstrated that many lightsource issues exhibit recognizable patterns in their symptoms. These patterns are amenable to automated identification using a Cymer-developed model-based fault detection system, thereby alleviating the need for detailed human review of all detailed lightsource performance information. Automated recognition of these patterns also augments our ability to predict the performance trending of light sources.

Such automated analysis provides several efficiency improvements for light source troubleshooting by providing more content-rich standardized summarization of lightsource performance along with reduced time-to-identification for previously classified faults. The scale of automation provides the ability to generate lightsource performance metrics based on the performance of a single light source, or the performance of multiple light sources. However, perhaps the most significant advantage is that these recognized patterns are often correlated to a known root cause, where known corrective actions can be implemented, and subsequently minimize the time that the lightsource needs to be offline for maintenance. In this paper, we will show examples of how this new tool and methodology, through an increased level of automation in analysis, is able to realize reduced fault identification time, correspondingly reduced time for root cause determination for previously experienced issues, and hence enhance our light source performance predictability.

7640-84, Poster Session

Reduced overlay due to scanner lens aberrations

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Lens aberrations described by the Zernike coefficients can create mismatch between the registration marks and the die pattern. Therefore, the corrections calculated from the registration measurement may not be accurate which could result in yield loss. Since the die features and the box-in-box (BIB) registration marks have different directionality they can move differently with large lens aberrations. With simulations we were able to show that in the presence of lens aberrations BIB marks would move differently than the die and that some of the Zernikes have larger impact than the others. We further show that the attenuated BIB mark matches the smaller features better than the binary BIB mark. This simulation data was verified by placing binary and attenuated BIB marks on the same reticle and measuring the alignment marks in the presence of manually introduced aberrations. Additionally, we evaluated BIB mark designs which match the die features better, and we provide an analysis to improve the BIB mark to die matching.

7640-85, Poster Session

Pattern deformation caused by deformed pellicle with ArF exposure

J. You, I. An, H. Oh, Hanyang Univ. (Korea, Republic of)

Step-and-scan mode of wafer patterning requires masks with no killer defects in order to achieve good yields. While masks are made without any defects that result in nonfunctional die, preventing particles from depositing on masks during extended mask usage is a challenge, even in the state-of-the-art clean rooms. Pellicles are attached to photomasks to avoid new printable defects. However, a high energy of ArF laser directly affects pellicle degradation because the energy of C, F, O single bonding composing the ArF pellicle film is quite smaller than the energy of 193 nm ArF. It is known that the exposed part of pellicle goes thinner as the exposed energy is built up during the exposure process. This will make a sloped pellicle surface and will act like a prism. As a result, the incoming straight light will be bended at the boundary of pellicle, thus, the outgoing light after the pellicle will be deviated from the on axis. So, outgoing light has information of smaller space than mask size. Consequently, the pattern deformation can occur due to pellicle deformation. Preliminary study shows that several kJ/cm2 makes several nm local pellicle thinning, and this local pellicle thinning can cause more than 5 m position shift from the original pattern position. This pellicle deformation with the increased deposit energy will be a serious problem for patterning. In order to offer some tip to find the appearance of pellicle thinning caused defect, several types of pattern deformation caused by pellicle degradation will be reported using EM-SUITE.

7640-86, Poster Session

Icut-based process optimization of dense contact-hole patterning

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Optical lithography is limited by diffraction, especially when the dimensions of objects are comparable to the wavelength of light in size. So every effort in lithography has been put so far on the increase of capturing efficiency of diffraction light. But as low-k1 lithography became popular, there is not much room remained for engineering of diffraction orders though source-mask optimization is still one of popular topics.

Recently various process techniques of CD adjustment have been suggested such as etch trimming or chemical attachment. Furthermore, as image reversal techniques by negative tone development or CMP/etch-back assisted methods,there arises a growing possibility of Icut engineering.

Now pitch split techniques are almost ready for lines and spaces patterning of leading edge memory devices. However patterning of dense contact hole is remained sole and very crucial challenge in optical lithography. In this paper, we will provide lithographic performances of various techniques according to cutting levels, that is different CD bias and polarities. Pillar and contact hole patterns are directly compared with each other by using same resist processes. Then contact hole pattern evaluate with positive and negative tone development. Double and single expose cases are compared also to investigate whether there are any room for image contrast improvement.

In conclusion, optimized setting of Icut level can be promising way of extending optical lithography to the ultimate design rule of 3X node DRAM.

7640-87, Poster Session

Misalign residual improvement by supression of silicon dislocation

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We study highly photo overlay mis-align by effect of silicon dislocation. As we use SOG(spin on glass) material as sharrow trench isolation, overlay residual increase in RCAT to active. Shrinkage of SOG is about 20% higher than other isolation. These high shrinkage make residual of overlay aggravate because of silicon dislocation. These dislocation is occured by trench etch damage. We have the experiment about plasma damage by trench etch process. The more plasma power increase, the worse residual of overlay aggravate. We interpret silicon dislocation occur by ion bambardment during etch process and silicon slip occur by heat process. We suggest that silicon oxidation is good candidate to cure damaged silicon layer after trench etch process. Based on this model, we can improve residual of overlay by curing damaged silicon layer.

7640-88, Poster Session

Study for lithography techniques of hybrid mask shape of contact hole with 1.35 NA polarized illumination for 28-nm node and below logic LSI

Y. Setta, K. Kobayashi, T. Chijimatsu, S. Asai, Fujitsu Microelectronics Ltd. (Japan)

Demand for scaling of integrated circuit device has continued, however, the backup of improvement of RET (resolution enhancement technique) and supply of high NA exposure tool has made it possible. In recent years, in order to improve the resolution, different approaches compared with traditional way such as double patterning and EUV lithography are focused. In addition, computational lithography such as SMO (source mask optimization) and ILT (inverse lithography technology) has been explored.

Dry ArF exposure tool has become general at the mass production of 90nm to 65nm node. Those day demands of minimum pitch are about 1.0 to 1.5 times larger than the light source wavelength. Those situations were even very difficult but litho engineer could establish for mass production with research and enthusiasm. On the other hand, demand of minimum pitch for 28nm node has reached a half of the light source wavelength. Patterning of contact hole is one of difficult issue for optical lithography and this minimum pitch have an influence to shrink design rule. Our strategy as lithographers is to push it costly and robust than before.

One of characterizations in lithography is to use reticle for making pattern. As DR (design rule) scaling, demand of mask cost of ownership has been sever. In this situation, data preparation time, writing time, and inspection time become a big component in the mask cost. Lithographer should concern some approach to reduce it.

In the 28nm and below, polarized illumination are discussed and explored. This technique has some merit to get higher image contrast and reduce the MEEF for nested region. The situation that cannot increase NA of immersion exposure tool has made this technique the last stronghold. Among contact-hole lithography, we would like to use this advantage as possible as we can.

In this presentation, the advantage in the use of combination of polarized illumination and technique of optimum mask shape for contact-hole lithography will be discussed. Both simulation and experimental work were carried out to characterize performance of this technique. It is said that quadrupole illumination is suitable for nested pattern of hole. But that's only said in textbooks. Setting of quadrupole illumination with polarization is often difficult because each aperture of quadrupole is located on slit position. So several polarized condition with annular were explored. We confirmed that some polarizations show improvement in image contrast, MEEF, and DOF for contact-hole than non-polarized condition. In addition, certain mask shape shows more improvement. Totally 15% DOF improvement from traditional rectangle shape with non-polarized condition was confirmed. In final single exposure era for contact-hole, this result with techniques of hybrid mask shape and polarized illumination is very attractive.

7640-89, Poster Session

Applications of MoSi-based binary intensity mask for sub-40-nm DRAM

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Since advanced lithography has been a driving force for high density memory device implementations, lithography community have concerned on the resolution improvement by developing viable imaging solutions. In order to improve the limitation of optical lithography, resolution enhancement technology (RET) such as hyper-NA immersion lithography, polarized illumination, double patterning technology (DPT) and spacer patterning technology (SPT) have been examined intensively. Currently, all technical efforts are focused on the sub-40nm patterning by applying hyper-NA (NA>1) immersion lithography system.

As long as the features on the mask were close to the exposure light wavelength, degree of polarization is changed dramatically by 3D mask structures on the mask. Since bigger NA means larger incident angles on the mask, three dimensional consideration of illumination light becomes more important, especially in the area of NA larger than 1. In previous paper, we have reported 3D mask effect using hyper-NA immersion lithography for sub-45nm era. It was observed that thick Cr binary intensity mask for sub-45nm has advantage for one dimensional line and space pattern compared to attenuated PSM. Recently, many papers are reporting better performance from MoSi based BIM compared to Cr based BIM and attenuated PSM for sub-40nm half pitch with respect to process window, CD uniformity, and mask-making consideration by using hyper-NA immersion scanner.

In this paper, we will discuss MoSi based BIM for hyper-NA immersion lithography with polarized illumination. Also we will evaluate several types of mask, such as MoSi based BIM, Cr based BIM and attenuated PSM, to compare patterning performance. In addition, we also analyze optimum mask materials for sub-40nm DRAM and polarization for each DRAM cells.

7640-90, Poster Session

Study of OMOG mask topography effect on 32-nm contact hole patterning

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This paper investigates the topography effect of Opaque-Molybdenum-Over-Glass (OMOG) mask on 32nm contact hole patterning by comparing simulation of both thin mask model and electromagnetic field (EMF) mask model against experiment measurement. OMOG mask has been adopted since 32nm node contact hole as it provides better critical dimension (CD) uniformity over conventional binary mask and lower mask error enhancement factor (MEEF) over attenuate phase shift mask (PSM). This paper shows that, for 32nm contact hole printing, OMOG mask topography effects can be significant and may account for up to 20nm CD error when a thin mask approximation is employed, regardless of its improvement over conventional binary mask.

Rigorous resist model is calibrated using FEM data of one selected dense pitch for both thin mask model and EMF model. Both models, in conjunction with its respective set of resist parameters, are used to compute FEM results for multiple pitches. FEM simulation results are then compared with experimental data. The study shows that, although a thin mask model can fit FEM result of single pitch very well, it is unable to predict FEM data of multiple pitches. For semi-dense pitch, the discrepancy between thin mask simulation and experimental measurement can be as much as 20nm. In contrast, an EMF mask model predicts FEM data of multiple pitches with much better accuracy.

This paper also uses dose sensitivity to characterize mask topography effect, wherein dose sensitivity is defined as CD change per dose variation and believed to be highly dependent on image contrast. It is

well-known that, if mask topography effect is significant, the "effective" mask opening becomes smaller than the actual opening due to light absorption on mask sidewalls. As a consequence, thin mask modeling usually overestimates mask opening, which results into lower image contrast and higher dose sensitivity for binary type of mask. This paper shows that, a thin mask model overestimates dose sensitivity by 66% while an EMF model gives more accurate prediction. Further studies show that thin mask model underestimates image contrast for 32nm dense contact pitch. The fact that thin mask model overestimates the dose sensitivity again indicates significant topography effects of OMOG mask on 32nm contact hole patterning.

Acknowledgement

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7640-91, Poster Session

Fast-converging iterative gradient decent methods for high-pattern fidelity inverse mask design

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Semiconductor fabrication is the cornerstone of the current IC (Integrated Circuit) industry. With recent advances in microlithography now pushing towards nano-scale features, the problem of printing circuit layouts on wafers has become more intricate and convoluted. Optical Proximity Correction (OPC) is a resolution enhancement technique that modifies mask layout designs in order to minimize their distortion when transferred to silicon. A good OPC implementation may prove sufficient for a given process technology, precluding the need for a more expensive alternative like Double Patterning, Alternating Phase-Shift Masks (AltPSM), Immersion Lithography and so on. Clearly, OPC has obvious advantages in terms of efficiency and manufacturing cost.

Segment-based OPC has been the general industry approach and has proven successful through many CMOS generations. Because it only modifies existing edges in the layout, segment-based OPC has the advantage of being easy to implement, particularly in iterative algorithms. However, as the Critical Dimension (CD) becomes ever smaller, this type of edge-only compensation is not flexible enough to exploit the full range of possible mask corrections. Therefore, inverse mask design, also called Inverse Lithography Technology (ILT), has been suggested as an alternative due to its more relaxed constraints and full-mask approach. However, inverse calculation is faced with several problems, including bad convergence and the existence of local minima. To get rid of these issues, many approaches have been proposed, such as pixel-flipping, gradient strategies and so on. Still, these approaches need to be further developed and refined to become the next-generation OPC.

In this paper, we propose an inverse algorithm that employs an iterative gradient-descent method to improve convergence and reduce the Edge Placement Error (EPE). The algorithm achieves fast convergence by defining a digitized gradient vector and a cross-weighting matrix to determine the corresponding weighting factors. The digitized gradient vector of the cost function depicts an optimized step direction for the iteration, while the cross-weighting matrix is a tensor expression that takes into account the correlations of EPEs of different edges on the weighting factors.

7640-92, Poster Session

Radial segmentation approach for contact hole patterning in 193-nm immersion lithography

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In this paper, a novel optical proximity correction (OPC) method for contact hole patterning is demonstrated. Conventional OPC for contact hole patterning involves dimensional biasing, addition of serifs, and sub resolution assist features (SRAF). A square shape is targeted in the process of applying conventional OPC. As dimension of contact hole reduces, features on mask appear to be circular due to stronger diffraction effect. The process window enhancement of conventional OPC approach is limited. Moreover, increased encounters of side lobes printing and missing contact holes are affecting the process robustness. A new approach of changing the target pattern from square to circular is proposed in this study. The approach involves a change in shape of mask openings and a radial segmentation method for proximity correction. The contact holes patterns studied include regular contact holes array and staggered contact holes. Process windows, critical dimension (CD) and aerial image contrast is compared to investigate the effectiveness of the proposed contact holes patterning approach relative to conventional practice.

7640-93, Poster Session

Binary mask optimization for forward-lithography based on boundary layer model in coherent systems

X. Ma, G. R. Arce, Univ. of Delaware (United States)

Due to the resolution limits of optical lithographic systems, the electronics industry has relied on resolution enhancement techniques (RET) to compensate and minimize mask distortions as they are projected onto semiconductor wafers. In optical proximity correction (OPC), mask amplitude patterns are modified by the addition of sub-resolution features that can pre-compensate for imaging distortions. Most of current model-based OPC optimization algorithms, however, were developed under the thin-mask assumption, where Kirchhoff's boundary condition is directly applied to the mask topology and consequently the mask is treated as a 2-D object. As the critical dimension (CD) printed on the wafer shrinks into the subwavelength regime, the thick-mask effects become very pronounced such that these effects should be taken into account in the mask optimization. Thick-mask effects include polarization dependence due to the different boundary conditions for the electric and magnetic fields, transmission error in small openings, diffraction edge effects or electromagnetic coupling and so on. The thick-mask effects can be rigorously represented by the near-field pattern of the mask, which is different from the Kirchhoff approximation of the mask topography. During the latest decades, a set of rigorous mask model have been developed. However, these models are so computationally complex that the model-based OPC optimization problem is very practically challenging. Recently, Azpiroz et al. introduced a novel boundary layer (BL) model for fast evaluation of the near-field of a thick mask. Different from other computationally complex and resource consuming rigorous mask models, the BL model treats the near field of the mask as the superposition of the interior transmission areas and the boundary layers, which have fixed dimensions and determined locations. The BL model effectively compensates for the inaccuracy of Kirchhoff's approximation, which is attributed to thick-mask effects, different polarizations, and phase errors. The simplicity and accuracy of the BL model enables the formulation of a model-based optimization algorithm for binary masks.

This paper thus focuses on the formulation of a model-based forward OPC optimization algorithm based on the BL model to take into account the thick-mask effects under coherent illumination. This is accomplished as follows: First, the optical lithography process under coherent illumination is formulated as the combination of the BL model and the Hopkins diffraction model. The cost function of the OPC optimization problem is formulated as the square of the l2-norm of the difference between the real aerial image and the desired pattern on the wafer. Then the gradient of the cost function, referred to as the cost sensitivity function is developed and used to drive cost function in the descent direction during the optimization process. Topological constraints of the binary mask is introduced and used to limit the minimum opening size of the optimized mask pattern.

7640-94, Poster Session

Improvement in process window aware OPC

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The use of optical lithography for 32nm node and beyond requires hyper-NA immersion optics in combination with advanced illumination and mask technology, which, however, leads to a significant shrinkage of tolerable lithography process window. This is exacerbated by the fact that 1.35-NA, the limit of water-based immersion lithography, has a focus window of less than 150nm. The exposure dose window is also decreasing because contrast decreases as semiconductor manufactures attempt to maximize the benefit of modern scanners. As a result, a small process variation (focus and exposure dose variation) may cause some catastrophic failures at these more advanced technology nodes. Traditional Optical Proximity Correction (OPC) only uses nominal model (nominal focus and nominal exposure dose), which may result in an unacceptably small process window. Therefore process window aware OPC (PWOPC) is becoming more and more important to improve process robustness and enhance yield.

In our previous study, we have demonstrated the effectiveness of PWOPC based on Synopsys OPC software - Proteus at full chip scale. In this study, we present some important improvements on our PWOPC approach. First, PWOPC has the flexibility of being applied only at the selected areas of a layout. By selecting the PWOPC areas either with rule-based or model-based technique properly, we can greatly improve the runtime without missing potential catastrophic locations. Secondly, different requirements to avoid pinching or bridging can be specified for different areas and different feature types. This is implemented with the highly-programmable interface provided by Proteus. Third, we measure the actual contour space and width and compare directly to the bridging and pinching specifications during PWOPC. Comparing to PWOPC methods only considering EPE with chosen process window models, this approach works directly towards meeting the specifications. Finally, a new correction method that uses prioritization rules is developed. Compared to a typical PWOPC algorithm which may involve minimizing of a cost function that is the weighted sum of EPE with chosen process window models, this approach makes final results more controlled and predictable. Overall, the improved PWOPC approach was constructed as sequence of independent modules, and it is easy for users to modify its algorithm and to build original IPs. We will apply PWAOPC to several circuit and test patterns and use a verification tool to demonstrate how process window will be improved compared to traditional OPC methods.

7640-95, Poster Session

Delta-chrome OPC with intensity based feedback compensation

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Delta-Chrome OPC has been widely adopted in lithographic patterning for semiconductor manufacturing. During each OPC iteration, a predetermined amount of chrome is added to or subtracted from the mask pattern. The exposure intensity change is then calculated based on proximity models. Linear approximation is used to predict the proper chrome change to remove the correction error. This approximation can be very fast and effective, but must be performed iteratively to capture interactions between feature changes. As IC design shrinks to the deep sub-wavelength regime, previously ignored nonlinear process effects, such as 3D mask effects and resist development, become significant for accurate prediction and correction of proximity effects. These nonlinearities challenge the delta-chrome OPC correction methodology. Computation of the model response to the mask geometry perturbation is no longer computationally cheap. A non-delta-chrome OPC methodology with intensity-based feedback compensation is proposed and tested. It determines chrome change based on intensity error without intensive computation of mask perturbation response. Its effectiveness in reducing OPC iteration numbers with the presence of nonlinear effects are examined with several regular mask geometries and practical design layouts.

7640-96, Poster Session

A new etch aware lithography after development inspection technique for OPC modeling

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As etch effect becomes a more important component of CD error budgets, OPC modeling requires an accurate and fast way to predict the pattern transfer between lithography and etch. Non-uniform etch bias leads to difficulties in traditional etch models and degrades overall stage modeling capabilities. This problem becomes one of the main challenges in OPC modeling, especially as manufacturing proceeds to advanced technology nodes where multiple etch techniques become main solutions to improving printing resolution. In this paper, we propose a new etch aware lithography After Development Inspection (ADI) model with a new etch bias function that will provide friendly and compatible output to the After Etching Inspection (AEI) model and hence improve the staged AEI model performance. Also, new targeting techniques will be introduced which could speed up and simplify etch modeling and corrections, and maintain lithography modeling and corrections at a good accuracy level. This new approach to lithography-etch process modeling has been shown to be very promising in full-chip OPC.

Since this is a patent related paper, the supplemental files will be provided on request. Thanks a lot!

7640-97, Poster Session

An optimized OPC and MDP flow for reducing mask write time and mask cost

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As tech node shrinks to 65nm and beyond, the Model-Based Optical Proximity Correction (MBOPC) are indispensable. To get better OPC result, the fragmentation are getting more and more fine and the post OPC become more and more complex. This inevitably increases the mask writing time because the writing time is proportional to the fragments.

In this paper, an optimized fragmentation and OPC method was proposed to reduce the fragments without sacrificing OPC accuracy. It automatic merges the adjacent two fragments when the difference of their correction value is under specific value. At the same time, it also assures the EPE of these aligned fragments is under specific range. In addition, the jog was aligned in Mask Data Preparation to reduce mask shot count in mask writers. With these two technologies, the writing time and cost of mask was reduced and OPC accuracy is not affected.

7640-98, Poster Session

Wafer LMC accuracy improvement by adding mask model

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To Improve verification at wafer level of simulation accuracy and decrease false alarm. We must consider mask effect like corner rounding and line-end shorting...etc in high-end mask. So we combine mask model and wafer model then build up a new model that called M-FEM. We compare the hotspots prediction between M-FEM model and baseline wafer model by LMC verification. Some different hotspots

between two models were found. We evaluate whether the hotspots of M-FEM is more close to wafer printing results.

7640-99, Poster Session

Study of model-based etch bias retarget for OPC

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Model based Optical proximity correction is usually used to compensate for the pattern distortion during the micro-lithography process. Currently, almost all the lithography effects, such as the proximity effects from the limited NA, the 3D mask effects due to the shrinking critical dimension, the photo resist effects, any some other well known physical process, can all be well modeling with the OPC algorithm. However, the micro-lithography is not the final step of the pattern transformation procedure from the mask to the wafer. The etch process is also a very important stage. It is well known that till now, the etch process still can't be well explained by physics theory. As we all know, the final critical dimension is decided by both the lithography and the etch process. If the etch bias, which is the difference between the post development CD and the post etch CD, is a constant value, then it is simple to control the final CD. But unfortunately this is always not the case. For advanced technology nodes with shrinking critical dimension, the etch loading effect is the dominate factor that impacts the final CD control. And some people tried to use the etch-based model to do optical proximity correction, but one drawback is the efficiency of the OPC running will be hurt. In this paper, we will demonstrate our study on the model based etch bias retarget for OPC.

7640-126, Poster Session

Intra-field CD uniformity correction by Scanner Dose Mapper™ using Galileo™ mask transmission mapping as the CDU data source

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Intra-field CD variation can be corrected through wafer CD feedback to the scanner in what is called the Dose Mapper (DOMA) process. This will correct errors contributed from both reticle and scanner processes. Scanner process errors include uncorrected illumination non uniformities and projection lens aberration .However, this is a tedious process involving actual wafer printing and representative CD measurement from multiple sites. A novel method demonstrates that measuring the full-field reticle transmission with Galileo can be utilized to generate an intensity correction file for the scanner DOMA feature. This correction file will include the reticle transmission map and the scanner CD signature that has been derived in a preliminary step and stored in a database. The scanner database is periodically updated after preventive maintenance with CD from a monitoring reticle for a specific process. This method is easy to implement as no extra monitoring feature is needed on the production reticle for data collection and the new reticle received can be immediately implemented to a production run without the need for wafer CD data collection. Correlation of the reticle transmission and wafer CD measurement can be up to 90% depending on the quality of CD data measurements and repeatability of the scanner signature. CD mapping on the Galileo tool takes about 20 minutes for 1500 data points, which is more than enough for the DOMA process. Turn Around Time (TAT) for the whole DOMA process can thus be shortened from 3 Days to about an hour with significant savings in time and resources for the fab.

7640-100, Poster Session

Accelerated lifetime tests of 193-nm optical components

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One challenging problem in the development of 193 nm immersion lithography tools is to improve throughput and reliability of these systems.Throughput can be enhanced by use of more powerful lasers. For higher reliability lifetime improvement of the used optics is needed. Because lifetime testing of optics is very expensive a lot of short term tests have been developed.

In our company we have developed and built a lifetime test setup allowing not only the test of 193 nm optical elements at enhanced energy densities.It is also possible to measure reflection,transmission ,absorption and scattering of our components and analyzing this way degradation of the components before they do really fail.

We have successfully tested and qualified a lot of different optical components in our setup.A special aim of our tests was to introduce a new class of optical thin film elements based on ion assisted deposition of oxides being less sensitive against contaminations than state of the art fluoride based ones.Limitations of the tests are discussed and results for high end components are presented.

fig.1 Possible arrangement of components in our lifetime test equipment

7640-101, Poster Session

Metamaterials for enhancement of DUV lithography

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The unique properties of metamaterials, namely their negative refractive index, permittivity, and permeability, have gained much recent attention. Research into these materials has led to the realization of a host of applications that may be useful to enhance optical nanolithography, such as a high pass pupil filter based on an induced transmission filter design, or an optical superlens. A large selection of materials has been examined both experimentally and theoretically through wavelength to verify their support of surface plasmons, or lack thereof, in the DUV spectrum via the attenuated total reflection (ATR) method using the Kretschmann configuration. At DUV wavelengths, materials that were previously useful at mid-UV and longer wavelengths such as silver, no longer act as metamaterials, but composites bound between metallic aluminum and stoichiometric aluminum oxide (Al_2O_3) exhibit metamaterial behavior, as do a select few other materials such as tin and indium. This provides for not only real opportunities to explore the potential of the use of such materials for image enhancement, it does so with easily obtainable materials at desirable lithographic wavelengths.

7640-102, Poster Session

Chemical contamination analysis for advanced lithography

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Detailed abstract.

To control lithography yields, all optical surfaces must be kept clean. Since clean is a relative term, quantitatitve test methods are required by the ITRS, and tool manufacturers, purifier companies and users, to give reasonable optics lifetimes in the field. Both gas phase tests (for purge gases, cleanroom air) and surface tests are needed to quantitate the thresholds that contribute to early failures of optics, lenses, masks, lasers, metrology equipment.

For gas phase contaminants, compounds of interest include organics, refractory organics, ionics (acids + bases that create salts, such as ammonium sulfate). Organics are typically trapped on adsorbents, then desorbed into a GC-MS. Ionics are often trapped into ultrapure water, or water with additives, then analyzed by IC (Ion chromatography), down to 10 pptrv (parts per trillion by volume) levels. Some publications have questioned the validity of bubbler trapping methods at pptrv levels. Typical instrument blanks, shipping blanks, and recovery studies are presented for ammonia and key acids, using high efficiency bubblers vs standard bubblers.

Other contaminants of interest may be discussed as time allows (urea, organic acids, N2 impurity tests, SOx etc).

7640-103, Poster Session

Lithography simulation formulation and approximations, and its impact to simulation accuracy

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Lithography model has been extended greatly in the past two decades: from low-NA to high-NA to hyper-NA, from scalar to vector optics, from dry to immersion lithography, and from thin mask to thick mask model, to name just a few of the major breakthroughs. These developments did not happen over-night: they were achieved through the collective efforts of many researchers over years. Usually, the extensions are presented focusing on one or two aspects of the subject matter; Inconsistency between different formulas among different authors abound, and confusing among different implementations cause difficulty from the user's point of view to evaluate the consistency between them. Despite the appearance of several review papers in the recent years, a systematic and consistent presentation of the formulation that includes the above mentioned extension seems still lacking.

In this paper, a systematic and consistent approach to projection optics modeling is presented. The vector nature of light and polarization effect are considered beginning with the source, through the mask and projection lens, and then down into the film stack. The model also includes High-NA effect and lens signature. Of particular interest is the mask diffraction model that is compatible with a 3D mask-solver (and under the Kirchoff boundary assumption is the same as the Smythe formula). A compact film-stack model is formulated and presented, first using Abbe's source-integration approach and then using Hopkins' TCC approach, which is computationally more efficient for fixed optical setting. Post-optics resist models such as exposure, PEB and development model are also presented. Critical views of the approaches are presented. Efficient numerical implementation of the model is briefly discussed.

7640-127, Poster Session

High-fluence testing of optical materials for 193-nm lithography extensions applications

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As next generation immersion lithography, combined with double patterning, continues to shrink feature sizes, the industry is contemplating a move to non-chemically amplified resists in order to reduce line edge roughness. Since these resists inherently have lower sensitivities, the transition would require an increase in laser exposure doses, and thus, an increase in incident laser fluence to keep the high system throughput.

Over the past several months, we have undertaken a study at MIT Lincoln Laboratory to characterize performance of bulk materials (SiO2 and CaF2) and thin film coatings from major lithographic material suppliers under continuous 193-nm laser irradiation at elevated fluences. The exposures are performed in a nitrogen-purged chamber where samples are irradiated at 4000 Hz at fluences between 30 and 50 mJ/cm2/pulse. For both coatings and bulk materials, in-situ laser transmission combined with in-situ laser-induced fluorescence are used to characterize material performance. Potential color center formation is monitored by ex-situ spectrophotometry. For bulk materials, we additionally measure birefringence spatial maps before and after irradiation. For coatings, spectroscopic ellipsometry is used to obtain spatial maps of the irradiated surfaces in order to elucidate the damage mechanisms.

Results obtained in this study can be used for identifying potential areas of concern in the lens material performance if the incident fluence is raised for the non-chemically amplified resist introduction. The results can also help to improve illuminator performance where such high fluences already occur.

7640-104, Poster Session

Stepwise fitting methodology for OPC modeling

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As integrated circuits continue to shrink the device sizes to the 32nm, 22nm technology nodes and beyond with 193nm wafer immersion lithography, there is a need for an improved methodology to increase lithography process simulations robustness for optical proximity correction (OPC) and process window predictability. One of the problems in OPC model optimization is the determination of the optimized values of all the model fit parameters involved in the OPC model. A straight forward approach for determination of the OPC model parameters is a global search over the entire set of model fit parameters to find a cost function minimum. OPC models are usually based on a large numbers of fit components such as resist thickness, bake temperature, illuminator shape, etc. In the case of the global model optimization method, there is a potential risk of overweighting one component versus another and as a result loosing the physicality of the final model. This physicality loss reduces model quality in terms of fit and prediction. In this work a stepwise fitting methodology based on staged fitting of the OPC model components will be presented. The first step is to optimize the optics and the mask, which are considered the most physical components in the OPC model. The optimized parameters are locked and are not regressed in followed stages of the model optimization. Next, more components are added in the order of more physical to less physical parameters. This method has been tested and compared with global search regression method on real wafer measurement data sets. Small model residual and superior resist edge contour predictions have been observed.

7640-105, Poster Session

Automatic numerical determination of lateral influence functions for fast CAD

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A methodology is introduced for utilizing rigorous image simulation tools to derive lateral influence function kernels that facilitate fast-CAD pattern matching techniques to evaluate pattern dependent lithographic effects at advanced imaging nodes. In evaluating the manufacturability of circuit layouts a large number of layout scenarios must be evaluated for their sensitivity to illumination, focus, high-NA, and immersion effects. Convolution with lateral influence kernels has been introduced that are capable of rapidly approximately estimating process effects [1]. First principles physics based methodologies have been developed for determining these lateral influence kernels [2,3,4,5,6]. Yet there is a daunting task of integrating all of these physical effects and their potential confounding into a set of kernels.

This paper introduces a novel methodology for automatically generating lateral influence functions under the influence of combinations of simultaneous physical effects. The methodology

utilizes the representation of the physical effects as a perturbation of the complex representation of the electric field in the pupil and moves this perturbation to the mask plane where it can be convolved with the layout for quantitative assessment. Physical effects include non-idealities in illumination, masks edge effects, focus and lens aberrations, high NA effects and immersion imaging. Incorporating these effects in any rigorous image simulator (with access to the pupil plane) can be used to generate the lateral influence kernels.

This paper demonstrates the automatic numerical determination of lateral influence functions and prediction of imaging non-idealities through a study of mask edge effects at 45, 32 immersion and 22 nm double patterning. It has been shown that boundary layer modeling can be used to model thick mask phenomenon in a thin mask model, when operating outside the cross-talk regime [1,2]. By combining boundary layer modeling with pattern matching capabilities, we are able to assess mask locations sensitive to electromagnetic errors in the presence of defocus and other lens aberrations while taking into account polarization effects

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7640-106, Poster Session

Aberration measurement using principal components of aerial image

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In this paper, we present a streamlined aerial image model that is linear and quadratic with respect to projection optic’s aberrations. The model includes the impact of the NA, partial coherence, as well as the aberrations on the full aerial image as measured on an x-z grid. The model allows for automatic identification of image’s primary degrees of freedom, such as bananicity and Y-icity among others.

The model is built based on physical simulation and statistic analysis. Through several stages of multivariate analysis a reduced dimensionality description of image formation is obtained, using principal components on the image side and lumped factors on the parameter side. In parallel, an ensemble of transmission-cross-coefficients due to each of the Zernike polynomials and NA/   settings is analyzed for covariance, with its principal components also identified. The covariance matrix of TCCs is compared to one obtained via path analysis of formed images, and is used to tune the factor composition. The modeling process is applied to the aerial images produced by the alignment sensor in a 0.75NA ArF scanner while the tool is integration mode and aberration levels are high. Approximately 20 principal components are found to have a high signal-to-noise ratio in the image set produced by varying illumination conditions and considering aberrations represented by 33 Zernike polynomials. The coefficients are extracted and the measurement repeatability is presented. The analysis portion of the model is then applied to the measured coefficients and a subset of projection optic’s aberrations are solved for. Random error analysis indicates that 26 Zernike coefficients can be extracted with 2 nm error using a linear model, and all 33 can be extracted using a quadratic model. Impact of systematic error on the solutions is discussed.

7640-107, Poster Session

Methods for benchmarking photolithography simulators

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As the semiconductor industry moves to double patterning solutions for smaller feature sizes, photolithography simulators will be required to model the effects of non-planar film stacks in the lithography process. This presents new computational challenges for modeling the exposure, post-exposure bake (PEB), and development steps. The algorithms are more complex, sometimes requiring very different formulations than in the all-planar film stack case. It is important that the level of accuracy of the models be assessed.

For these reasons, we have extended our previous papers in which we proposed standard benchmark problems for computations such as rigorous EMF mask diffraction, optical imaging, PEB, and development (1-4). In this paper, we evaluate the accuracy of the new PROLITH wafer topography models. The benchmarks presented here pertain to the models (and their associated outputs) most affected by the switch to non-planar film stacks: imaging at the wafer (image intensity in-media), PEB (blocked polymer concentration), and development (resist profile). Closed-form solutions are formulated with the same assumptions used in the model implementation. These solutions can be used as an absolute standard and compared against a simulator. The benchmark can then be used to judge the simulator, in particular as it applies to speed vs. accuracy trade-offs.

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7640-108, Poster Session

Selective inverse lithography methodology

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Selective Inverse Lithography (ILT) approach recently introduced by authors [1] has proven to be advantageous for extending life-span of lower-NA 193nm exposure tools to achieve satisfactory 65nm contact layer patterning. In this paper we explore possible region selection criteria for ILT application based on pitch, mask error enhancement factor (MEEF), depth of focus (DOF), normalized image log slope (NILS), and their combinations for a full chip optical proximity correction (OPC). Through studying the impact of a given selection criteria on runtime, resolution, process window we recommend an optimal combination. With a justified choice of an ILT selection criteria, we construct a hybrid OPC flow comprising a recursive sequence of direct assist features generation, selective ILT application, layout repair, model OPC and hot spots screening.

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7640-109, Poster Session

CDU linear model based on aerial image principal components

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In this paper we present a process window model that is linear and quadratic with respect to common pupil and source shape errors. Similar to other CDU models in its simplicity; our model expands linear representation to a large focus-dose grid, identifying corrections to the full Bossung curve or process window shapes that are proportional to aberration levels or source shape errors.

The aerial image formed by a lithographic system is treated as a random field, and a Karhunen-Loeve expansion is applied with respect to common pupil, source and mask errors. Using Zernike polynomial representation for wavefront errors and Tatian polynomials for the source shape errors, coefficients of the expansion are fitted to the original error levels by using a second order model. Applications to focus averaging and scanning aberration averaging are discussed. The eigenfunctions of the image ensemble are then projected onto the Bossung curve space and process window. Accuracy of the projection is analyzed.

By applying a second Karhunen-Loeve expansion in the CD/Focus space, orthogonal principal components of Bossung curves and process window are also identified, enabling latent image synthesis. An approach to perform simulation-based process window analysis is discussed, and several types of CD eigenfunctions are presented.

The process is applied to specification generation process for a latent image formed in a k1=0.35 ArF scanner. The latent image subspace is analyzed via a direct projection from the CD/Focus space onto the latent image space using the primary principal component which is independent of the pupil and source errors. A method to project a latent image subspace into an aerial image subspace is also discussed.

7640-110, Poster Session

Impact of illumination on model-based SRAF placement for contact patterning

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Sub-Resolution Assist Features (SRAFs) have been used extensively to improve the process latitude for isolated and semi-isolated features in conjunction with off-axis illumination. These SRAFs have typically been inserted based upon rules which assign a global SRAF size and proximity to target shapes. Additional rules govern the relationship of assist features to one another, and for random logic contact layers, the overall ruleset can become rather complex. It has been shown that model-based placement of SRAFs for contact layers can result in better worst-case process window than that obtained with rules, and various approaches have been applied to affect such placement. The model comprehends the specific illumination being used, and places assist features according to that model in the optimum location for each contact hole. This paper examines the impact of various illumination schemes on model-based SRAF placement, and compares the resulting process windows. Both standard illumination schemes and more elaborate pixel-based illumination pupil fills are considered.

7640-111, Poster Session

A novel decomposition of source kernel for OPC modeling

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The improvements of accuracy and efficiency for OPC (Optical Proximity Correction) modeling become necessary at the low k1-factor process. However the accuracy of OPC model has to compromise with the efficiency of model setup and pattern correction, since the model accuracy is improved as more kernels are used to represent the model but that the runtime of model setup and pattern correction is proportional to the number of kernel. The OPC process model is constructed from a fitting of empirical CD data, and it consists of optical simulation and resist simulation components. In the optical simulation, ideal source kernel is too primitive in original OPC model that it can't sufficiently cover the proximity behavior of various line widths and pitches. The KIF (Kernel Import Facility) is accordingly implemented to OPC kernel for increasing model accuracy [1-2], but at the cost of longer runtime and lower efficiency.

A novel decomposition of source kernel for OPC modeling was presented in this study to maintain the model accuracy and reduce the OPC runtime. Firstly, the source kernel was decomposed into multiple source kernels and then the magnitude of electric field for each decomposed source kernel was modulated in frequency domain. Finally, the resultant source kernel can be the combination of many different source kernels and it will be more flexible to manage the model behavior in different line widths and pitches. The preliminary result has showed that model residuals can be reduced and the efficiency of model fitting is also improved. The methodology of source kernel decomposition, implementation flow and model stability will be further described in this paper. Besides, the real case validation and run time will be compared with ideal source model and KIF model.

7640-112, Poster Session

Methods for assessing empirical models

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Assessing an empirical model is a non-trivial task, because the model's fit to calibration input data must be balanced against its robustness in prediction in reality, and often its efficiency in full-chip operations. Here we define a few quantitative methods for model assessment. Both theoretical foundation and practical use cases are presented.

Estimation theory of statistics is the primary mathematical tool we adopt for analyzing parameter uncertainty and estimating simulation uncertainty. We will define a metric - Model Effectiveness Standard Index (MESI) - for assessing the total variation of a calibrated model. We will also present a method of objectively identifying outliers in experimental input data set. For model prediction error, we will present an estimate of the simulation variance at any given input point.

7640-113, Poster Session

A simplified reaction-diffusion system of modeling chemical-amplified resist process for OPC modeling

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As semiconductor manufacturing moves to 32nm, 22nm technology nodes with 193nm wafer immersion lithography, the demand for more accurate OPC modeling is unprecedented to accommodate the diminishing process margin. Among all the challenges, modeling the process of Chemical Amplified Resist (CAR) is a difficult critical one to overcome. The difficulty lies in the fact that it is a super complex

physical and chemical process. Although there are well-studied CAR process models, those are usually developed for lithography simulators, making them unsuitable for OPC simulation tasks in view of their full-chip capability at an acceptable turn-around time. In our recent endeavors, a simplified reaction-diffusion model capable of full-chip simulation was investigated for simulating the Post-Exposure-Bake (PEB) step in a Chemical Amplified Resist (CAR) process. This model uses aerial image intensity and background base concentration as inputs along with a small number of parameters to account for the diffusion and quenching of acid and base in the resist film. It is appropriate for OPC models with regards to speed, accuracy and experimental tuning. Based on wafer measurement data, the parameters can be regressed to optimize model prediction accuracy. This method has been tested to model numerous CAR process with wafer measurement data sets. Model residual of 1nm RMS and superior resist edge contour predictions have been observed. Analysis has shown that the so-obtained resist models are separable, i.e., the calibrated resist model with one illumination condition can be carried to a process with different illumination conditions. It is shown that the simplified CAR system has great potentials of being applicable to full-chip OPC simulation.

7640-114, Poster Session

Improved process window modeling techniques

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Current OPC models need to accurately predict process window changes, usually taken to be focus or dose changes. The increased number of process conditions adds to the model calibration time since a new optical model needs to be generated at each focus condition. This study shows how several techniques can reduce the calibration time by appropriate selection of process conditions, features, and algorithms. Experimental data is used to calibrate models using a reduced set of data and compared with the model resulting from the full set of data. The results indicated that using a reduced set of process conditions and using process sensitive features can yield a model with similar accuracy as with the full set in a shorter amount of time.

7640-115, Poster Session

Technological approach to short-interval scheduling in photolithography

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As Photolithography and other factory manufacturing processes become more complex, and as traditional heuristic rule-based dispatching systems start reaching their full potential, an optimization solution based on short-interval scheduling can pave the way for additional efficiency gains. Where successful heuristic rule-based systems are simple to deploy and fast in execution, their ability to evaluate alternate scheduling strategies to improve system performance are limited. Semiconductor manufacturers recognize the need for an optimization solution that provides real-time short-interval scheduling, but practical success of implementing such a solution in Photolithography has been difficult to quantify.

This paper presents results of an implementation of a short-interval scheduling solution in the Photolithography area of a 300mm semiconductor manufacturer.

Description of Approach:

Our approach combines real time data support, simulation based prediction, and an optimization algorithm for schedule generation that provides a solution that produces real time, near optimal short interval schedules. Each of these components plays a critical role in the ability to quickly and successfully generate near-optimal schedules.

The solution technology overview will detail the use of a high speed data collection system to build complete factory level prediction and scheduling model data sets. The prediction module relies on event-based simulation technology to predict future lot arrivals to key scheduled steps. The schedule generation technology is implemented using constraint programming, including custom constraints, propagation, and heuristics. Execution of the schedule is done through the existing dispatch system, which makes the final decision on the accuracy of the schedule based upon any potential changes in the factory that may have occurred during the generation of the schedule.

Prior to production deployment, we tested the scheduling system using a simulation-based fab emulator. The emulator included a detailed model of the entire 300mm fab. The emulator runs in two modes: in the simple mode it modeled the fab as it behaved originally, including modeling of the customer's current dispatching rules. In scheduling mode, the model calls out to the prediction and scheduling executables every 30 minutes of simulated time, then uses the returned schedules for its decisions until the next schedule is run.

For this project, we generated schedules for a portion of the fab's photolithography area. We scheduled 30 tools over a twelve hour time horizon.

Evaluation of Results:

We first ran the fab emulator in both modes: one where it was designed to imitate the fab using the current dispatching policy and another using the scheduling solution for the photolithography area. Simulation analysis allowed us to weigh multiple scheduling objective configurations, and the result range from stable cycle time and throughput increases > 6% to stable throughput and priority lot cycle time reduction of > 10% with overall cycle time reduction > 3%. In addition, supporting metrics were defined to add further validity to the findings.

The fab emulator approach helped us first to identify and correct errors in our model, and then to demonstrate the effectiveness of our model prior moving into production. At time of the abstract, the scheduling solution has only just been deployed to a production environment. The paper will include an evaluation of production results.

7640-116, Poster Session

The impact of scanner modeling parameters for OPC model of sub-40-nm memory device

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It is necessary to apply extreme illumination condition on real device as minimum feature size of the device shrinks. As k1 decrease, ultra extreme illumination has to be used. However, in case of using this illumination, CD and process windows dramatically fluctuate as pupil shapes slightly changes. For past several years, new Pupil Fit Modeling (PFM) is developed in order to analyze pupil shape parameters which are independent from each others. The first object in this work is to distinguish pupil shape of different scanner by separating more parameters. According to pupil parameter analysis, the major factors of CD or process window difference between two scanner systems obviously appear. Due to correlation between pupil parameter and scanner knob, pupil parameter analysis would be clearly identified which scanner knob should be compensated. The second object is to define specification of each parameter by using analysis of CD budget for each pupil parameters. Using periodic monitoring of pupil parameter which is controlled by previous specification, scanner system in product lines can be maintained at ideal state. Additionally, OPC model accuracy enhancement should be obtained by using highly accurately fitted pupil model. Recently, other application of pupil model is reported for improvement of OPC and model based verification model accuracy. Such as modeling using average optics and hot spot detection of scanner specific model are easily adopted by using pupil fit model. Therefore, applications of pupil fit parameter for process model are very useful for improvement of model accuracy.

In our study, the quantity of model accuracy enhancement using PFM is investigated and analyzed. OPC and hot spot point detection capability results with pupil fit model would be shown. Also, in this paper, trends of CD and process window for each scanner parameter are evaluated by using pupil fit model. As of result, we were able to find pupil parameter influence in critical layer CD and application of this test resulted in better accuracy in detecting hotspot for model based verification.

7640-117, Poster Session

Topography aware BARC optimization for double patterning

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Bottom anti-reflective coatings (BARCs) are applied to reduce the reflection of light from the wafer substrate. By applying a simple parameter variation routine to standard thin film layer algorithms, such as the transfer matrix method (TMM), appropriate optical parameters and thickness values of the BARC are identified. For higher NAs and a large range of incidence angles, it becomes increasingly difficult to determine single layer BARCs with an adequate performance, even more in the case of double patterning processes. The first lithographic exposure and subsequent process steps modify the properties of the BARC and impact its performance in the second lithography stage. For example, an exposure with a lines and spaces pattern can result in a laterally and sinusoidally modulated refractive index of the BARC. The reflectivity analysis for such a configuration has to be carried out with rigorous electromagnetic field solvers. To deal with this requirement, the Waveguide Method has been extended. A comparison of the reflectivity curves of the homogeneous BARC layer in the first lithography step and the modulated BARC layer in the second lithography step shows a difference of the optimum BARC thickness. This difference depends on the BARC modulation, on the exposure geometry, and on other parameters of the waferstack.

Advanced optimization techniques are employed to identify the most appropriate parameters of dual layer BARCs. Since the BARC has to perform well at different angles of incidence, and for both the first and the second lithography step, the given problem can be regarded as a multi-criteria optimization task. This allows for a mutual optimization of different incommensurable figures of merit. Rather than one best solution, a multi-criteria search approach yields a number of solutions that have been assessed as equally fit. A final selection can be achieved either by supplementary selection routines or through user interaction.

In this paper, a multi-objective genetic algorithm (MOGA) is applied to the multi-criteria optimization problem. In a first step, the problem is formulated as bi-objective, with the two lithography steps constituting the two criteria. Then the figure of merit is divided more finely according to different ranges of incidence angles. Results and convergence behavior of different configurations are discussed.

In addition, a local search approach, based on the sequential quadratic programming (SQP) method, is applied. The multi-criteria nature of the problem is taken into account by employing a scalarization technique called epsilon-constraint method. Different variants and options, especially aiming at a good coverage of the solution space, are applied to the problem. The obtained results are discussed and compared with those of the genetic algorithm.

The application of the described optimization techniques is used to identify the most appropriate exposure and wafer stack parameters to minimize the impact of the BARC modulation and to achieve a good performance for both lithography steps. The results are evaluated using swing curves and lithographic process windows.

7640-118, Poster Session

Simultaneous litho and etch OPC model calibration for 22-nm metal and contact layers using 3D scatterometry metrology

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The precise characterization of complex 3D features represents a significant challenge for the lithography OPC process. The main difficulty lies in transferring sufficient information about

three-dimensional features into the OPC model building process. Current advances in scatterometry modeling software1,2 allow measuring more complex structures and obtain accurate information on parameters such as tip-to-tip distances and 3D shapes.

In this work we will report on litho and etch OPC model calibration and verification for complex 3D patterns for 22nm metal and contact layers (see Figure 1). The impact of side-wall-angle (SWA) makes it difficult to predict the behavior of OPC model while transferred through etch (see Figure 2). The lack of a good calibrated 3D OPC model would impact the etch data and might result in miscalculations for a device performance. In this work we indentify critical areas of the patterns affected by 3D geometry and verify the litho and etch OPC model corrections for such patterns.

In the case of complex 3D patterns we will discuss the specific feature parameter optimization through process window. In addition we will also review scatterometry metrology trade off for complex 3D patterns measurements.

7640-119, Poster Session

A novel method to reduce wafer topography effect in implant lithography

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The wafer topography in implant lithography includes STI wafer substrate and poly lines. Since bottom anti-reflection coating (BARC) is not preferred by implant layer for concerns of both process cost and contamination, the wafer topography will degrade implant layer printing significantly. In this paper, it is proposed to add sub-resolution feature on reticle to improve implant layer patterning on wafer substrate with topography.

This paper first illustrates the mechanism of pattern degradation on STI wafer substrate, wherein optical light passes through photoresist and silicon dioxide, and is reflected on silicon-SiO_2 interface. The optical beam of certain incident angle may be reflected back into resist film and interfere resist pattern thus resulting into a degraded resist profile and unexpected critical dimension (CD) change. This part of light reflection on wafer substrate is called destructive bottom reflection in this paper. Authors propose adding sub-resolution feature on reticle to reduce the destructive bottom reflection. This sub-resolution feature is placed at an optimized distance to the main feature on the reticle, which, through scanner imaging, forms a “dark” zone in resist film near the main feature. The function of this “dark” zone is equivalent to “block” the optical beam of certain incident angle that otherwise would generate destructive bottom reflection to degrade the main feature. The “dark” and “block” here are quoted because sub-resolution feature actually generates a low intensity zone on resist film instead of fully dark area that does not fully block light either.

The effectiveness of this new method will be demonstrated by simulating iso-line printing on top of silicon oxide bounded by substrate silicon. Simulations show that, without applying sub-resolution feature, a severe undercut is resulted. In contrast, by adding sub-resolution feature, resist undercut can be prevented and a straight resist profile is formed. The key to implement the sub-resolution feature in this technique is to optimize its placement and size, where the sub-resolution feature need be placed to prevent destructive bottom reflection and yet not to affect the process window. This paper will give one example of optimizing the sub-resolution feature by use of simulation.

Although the sub-resolution feature proposed in this paper appears similar to conventional sub-resolution assist feature (SRAF), their principle is very different. The sub-resolution feature in this paper works as beam “blocker” while the purpose of conventional SRAF is to imitate the most optimized dense pitch under given illumination condition.

Additionally, the placement of the present sub-resolution feature is mainly dependent on the location of silicon-SiO2 interface on wafer substrate. More detailed discussion will be given in this paper.

This paper will also investigate implant lithography on top of poly lines, wherein poly line induced diffraction is the main mechanism affecting implant patterning instead of bottom reflection. In this paper, source optimization using wafer topography model will be applied to improve implant layer patterning on top of poly line in SRAM cell.

All lithography simulations in this paper are done on Synopsis lithography simulation tool --- Sentaurus-Litho of version A2007.12, which solves Maxwell's equations to model the wafer topography. Its effectiveness has been verified by comparing simulation results with silicon experiment.

7640-121, Poster Session

Immersion BARC for hyper-NA applications

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Reflectivity control through angle is challenging at hyper NA, especially for Logic devices which have various pitches in the same layer. A multilayer antireflectant system is required to control complex reflectivity resulting from various incident angles. In our previous works, we showed the successful optimization of multilayer antireflectant systems at hyper NA for BEOL layers. In this paper, we show the optimization of new multilayer bottom anti-reflectant systems to meet new process requirements at 28nm node Logic device. During the manufacturing process, rework process is necessary when critical dimension or overlay doesn't meet the specifications. Some substrates like TiN are sensitive to the rework process. As a result, litho performance including the line width roughness (LWR) could change. The optimizations have been done on various stack options to improve LWR including cap oxide effect. Other patterning and defect performances have been evaluated. An immersion tool at 1.35NA was used to perform lithography tests. Simulation was performed using Prolith™ software.

7640-122, Poster Session

Methods and challenges to extend existing dry 193-nm medium-NA lithography beyond 90 nm

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In order to fulfill the demands of further shrinkage of our mature 90nm logic litho technologies under the constraints of costs and available toolsets in a 200mm fab environment, a project called "Push to the Limits" was started. The aim is to extend the lifetime and capabilities of existing dry 193nm litho toolsets with medium to low numerical aperture, coupled with the availability of materials and processes which were known to help up CD miniaturization and to shrink the 90nm logic litho process as far as possible. To achieve this, various options were explored and evaluated, e.g. optimization of illumination conditions, evaluation of new materials, usage of advanced RET techniques (OPC, LfD, DfM and ILT) and resolution enhancement by chemical shrink (RELACS). In this project we demonstrate how we were able to extend our existing 90nm technology capability, down close to 65nm node litho requirements on most critical layers. We present overall result in most critical layer generally and specifically on most difficult layer of contact. Typical contact litho target at 100nm region was enabled, while realization of 90nm ADI target is possible with addition of new process materials.

7640-123, Poster Session

Examining reflectivity criterion for various ArF lithography

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As the chip size becoming smaller and smaller in IC manufacturing, feature size of most critical pattern of IC devices shrinks as well. When the feature size keep shrinking to 4Xnm, ArF lithography has already proceed to immersion process and becoame mature enough. One of important factors that would affect photo process window is optical reflection from imperfect substrate design. In previous experience, reflection would be optimized to fine level by adjusting TARC (Top Anti-Reflection Coating) or BARC (Bottom Anti-Reflection Coating) thickness through index of reflectivity. However, actual criteria of reflectivity for various ArF lithography process are unlikely the same, e.g. different system type (wet/dry), node (feature size), illumination type, or even substrate effect, and also need to be examined to retain a decent process window. In this paper, experimental result of various above-mentioned ArF process have been compared with reflectivity index from prolith simulation engine, and distinctly clarified criteria of reflectivity for each case. Furthermore, effects of reflection to several optics caused patterning-related results, e.g. IDB (Iso-Dense Bias), OPC (Optical Proximate Correction) accuracy, will also be discussed. The result also shows severe criterion of reflection is requested as feature size getting smaller to 4Xnm node, and RET-applied (Resolution Enhancement Technology) process has opposite result on it. From experimental results, IDB has been obviously affected by reflection and become one important factor that influences reflection criterion examination.

7640-124, Poster Session

CD-uniformity for 45-nm flash memory on product stack

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CD uniformity budget for a 45-nm Flash memory device requires the analysis and compensation of each single contributor factor. A dedicated simulation tool "CDU Predictor" helps to quantify the impact of main scanner and process factors for a comprehensive study of the CD Uniformity for an ideal flat wafer. However this analysis could under estimate the real CD distribution on a real production wafer if arfefacts induced by thin-film effects and underling device topography significantly increase the contribution of the optical levelling-device to the total focus-error and hence spread the CD distribution for processes with low DOF. Such artefacts can be eliminated by application of an offset-map obtained by probing the mechanical top-surface of the resist-stack with an AirGauge (AirGaugeImprovedLEvelling, AGILE). The systematic variation of CD across the wafer, no matter whether due to fingerprints of the reticle, the device-topography, the track-process or the exposure-tool, can be mapped into dose-corrections for compensation (DoseMapper). We discuss an experimental case with a combination of both tools for an effective CD Uniformity optimization.

7640-128, Poster Session

Analysis of photoresist edge bead removal using laser light and gas

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Wafer edge defects are considered a major problem in obtaining maximum device yields from semiconductor wafers. A primary source of edge defects is from particles and flakes of photoresist originating from the edge bead of resist caused by spin coating. In this paper, photoresist edge bead removal is studied in a series of experiments

using a laser and gas cleaning system.

One goal of the experiments was to reduce the edge exclusion by gradually reducing the area cleaned by the laser and gas system. A number of varying exposure algorithms were tested, and are shown along with microlithographic photos of the resulting edge geometry and surface condition.

Another goal of the experiments was to significantly reduce particle contamination that occurs during edge removal processing. A matrix of varying laser parameters run to optimize parameters to meet this goal. Results are given in a series of wafer-edge photos.

7640-41, Session 10

Novel holistic verification method of mask layouts using coherence map technology

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Establishment of the technology for the “holistic” optimization of the mask layouts in lithography has been a long dream for lithography engineers. However as is well known, such an optimization is generally a difficult problem because the goal of this should be a “holistic” one. This means that it should be verified that the optimized mask layouts are robust not only against a single process variation but also against a number of those in order to gain the maximum process yield.

Recently several novel techniques have been developed for the ultimate level of optimizations, such as genetic algorithms (GA) [1,2], inverse lithography technology (ILT) [3], interference map technology (IMT)[4], and SRAF guidance map technology(SGM) [5]. Especially IMT proposed by Socha et al. and SGM proposed by Ye et al. are absolutely novel methods to optimize mask layouts with drastically smaller turn around time (TAT) relative to the hitherto known methods. They described a mask optimization algorithm using a “coherence map” which shows the optimum degree to be placed in a mask layout as to robustness against a specific process variation such as a contrast of the image, depth of focus (DoF), or exposure latitude (EL).

Although we can actually increase its robustness against a single process variation to the utmost extent with these intelligent methods, our extensive studies in a variety of mask designs have clarified that the acquired mask layouts do “not infrequently” result in poor robustness against the unconsidered process variations. For example in a contact layer, the positions of the sub resolution assist features (SRAF) which are best optimized to increase its DoF are further away from those which are best optimized to increase its EL. In a conventional way, when such cases have been found, we have to revise the mask layouts in precise and in some times, we should also review the SRAF generation rules. These retraces greatly slow down the development TAT of the OPC.

In order to overcome these problems, we will propose a novel method for the verification and optimization of the SRAF which are robust against all kinds of considerable process variations using coherence map technology. In our method, we have found that we can previously evaluate a score of the optimal degree of the mask layouts with respect to the different kinds of process variations quantitatively, and repair the immature mask layouts or improve its inapt generation-rules of the SRAFs.

In this presentation, we are going to discuss some model-based mask layout verification and optimization methods in more detail and take a panoramic view of the strategy for the future OPC technologies.

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3. D. Abrams et al., Proc. of SPIE Vol. 6154 (2006).

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5. Jun Ye et al. :Private communication 2008.

7640-42, Session 10

Ultimately accurate SRAF replacement for practical phases using an adaptive search algorithm based on the optimal gradient method

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SRAF (Sub Resolution Assist Feature) technique has been widely used for DOF enhancement. Below 40nm design node, even in the case of using the SRAF technique, the resolution limit is approached due to the use of hyper NA imaging or low k1 lithography conditions especially for the contact layer. As a result, complex layout patterns or random patterns like logic data or intermediate pitch patterns become increasingly sensitive to photo-resist pattern fidelity. This means that the need for more accurate resolution technique is increasing in order to cope with lithographic patterning fidelity issues in low k1 lithography conditions. To face with these issues, new SRAF technique like model based SRAF using an interference map or inverse lithography technique has been proposed. But these approaches don’t have enough assurance for accuracy or performance, because the ideal mask generated by these techniques is lost when switching to a manufacturable mask with Manhattan structures. As a result it might be very hard to put these things into practice and production flow.

In this paper, we propose the novel method for extremely accurate SRAF placement using an adaptive search algorithm. In this method, the initial position of SRAF is generated by the traditional SRAF placement such as rule based SRAF, and it is adjusted by adaptive algorithm using the evaluation of lithography simulation. This method has three advantages which are preciseness, efficiency and industrial applicability. That is, firstly, the lithography simulation uses actual computational model considering process window, thus our proposed method can precisely adjust the SRAF positions, and consequently we can acquire the best SRAF positions. Secondly, because our adaptive algorithm is based on optimal gradient method, which is very simple algorithm and rectilinear search, the SRAF positions can be adjusted with high efficiency. Thirdly, our proposed method, which utilizes the traditional SRAF placement, is easy to be utilized in the established workflow. These advantages make it possible to give the traditional SRAF placement a new breath of life for low k1.

7640-43, Session 10

22-nm logic lithography in the presence of local interconnect

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It is expected that most aggressive 22nm logic node will have a gate pitch of ~90nm and a 1x metal pitch somewhere between 80 to 70nm. Even with immersion scanners, the Rayleigh k1 factor is below 0.32 for 90nm pitch and below single exposure resolution limits when pitch is below 80nm. A line/cut approach has been proposed to achieve good pattern fidelity and process margin.

Although highly regular gridded patterns help [1,2,3], one of the critical issues for 22nm patterning is contact and via patterning. The lines / cuts approach works well for the poly and interconnect layers, but the “hole” layers have less benefit from gridded designs and remain a big challenge for patterning.

One approach to reduce the lithography optimization problem is to reconsider the interconnection stack. The Contact layer is complex because it is connecting two layers on the bottom - Active and Gate - to one layer on the top. Other layers such as Via-1 only have one layer on the bottom.

A potential solution is a local interconnect layer. This layer could be formed as part of the salicide process module, where a patterned etch would replace the blanket strip of un-reacted metal of the silicide layer. Local interconnect lines would run parallel to the Gate electrodes, eliminating “wrong-way” lines in the Active layer. Depending on the final pitch chosen, Local Interconnect could be single or double patterned, or could be done with a self-aligned process plus a cut mask.

An example of a test cell layout is shown in Figure 1a, with a conventional style of Active lines used for power supply connections and Metal-2 (not shown) for the vertical connections within the cell. In contrast, the same logic function laid out with Local Interconnect is shown in Figure 1b. The contact count is reduced by ~25%, and in this case all Via-1’s were eliminated.

The simplified Active pattern, along with reduced contact count and density, permit a different lithography optimization for the cells designed with Local Interconnect. Details of lithography optimization results for critical layers, Active, Gate, Contact, and Metal 1 will be presented.

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7640-44, Session 10

Lithography and layout co-optimization beyond conventional OPC concept

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Mask pattern layout has been conventionally determined by applying OPC on a design layout. OPC is applied under a lithographical condition and the design layout is basically composed of such figures as rectangles with the printed target CDs. These days k1 factor is being decreased and MEF is becoming larger. Under this condition it is very difficult to apply accurate OPC. Even if OPC is appropriately applied, the OPC pattern is complicated and the cost of mask fabrication becomes expensive.

Under our innovative method of lithography and layout optimization device layout is composed of several rectangles and the length of each side is defined as optimized parameter. Lithographical condition such as illumination is characterized by parameters such as inner /outer sigma and open angle for cross pole illumination and the parameters are defined as optimized parameters. Then both parameters are combined into an optimized space. Those parameters are optimized simultaneously by heuristic method. As a result in case that printed CDs are targeted, the optimized result is better than that by conventional OPC, though the mask layout is simple. The reason is considered that illumination has impact on optical proximity effect and an appropriate illumination makes the simple mask layout be printed to be the required pattern during co-optimization. The CD target of OPC is the entire edge of the mask pattern, though some local treatment is possible. On the other hand in this method evaluation points are clearly directed, so it can concentrate on the CD there neglecting other locations that are not important for device performance. Since each layout parameter is optimized between lower and upper limits, we can set mask fabrication constraint.

This technique is applied on an isolation layer of 65nm node DRAM and the above advantages are confirmed. In 45nm node DRAM the isolation pattern is composed by slant patterns to make the cell size smaller (8F2>6F2). In this case the data volume of OPC become huge due to stepwise OPC. However instead of using the stepwise OPC, we can get CDs very close to the target CDs by just optimizing the width of slant rectangle and the size of hammerhead together with illumination shape. Since the vertexes are very few, the data volume is small. Some OPC consider defocus characteristics. However they don’t handle DOF directly but just utilize the defocus data extracting the OPC model. On the contrary, since new method is based on general optimization, it can set the actual DOF as the optimized target. It is possible to set any optimization target explicitly. As a case it can even set a target of robustness against MSD.

Regarding memory devices it is recommended that memory cell patterns are defined by this innovative method with illumination optimized simultaneously and OPC is applied on the peripheral patterns with the optimized illumination. By this procedure better CD control than conventional OPC can be got and the mask cost can be reduced.

7640-45, Session 10

Mask enhancer technology for sub-100-nm pitch random logic layout contact hole fabrication

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Resolution enhancement technologies (RETs) have been developed to reduce the minimum feature size in optical lithography. For 32nm-node and below, a strong RET combined with the ArF immersion lithography with hyper NA projection system become necessary to realize sufficient resolution and depth of focus (DOF) simultaneously. But, even if applying the immersion lithography, the mast error enhancement factor (MEEF) issue is still remained. Furthermore, the DOF issue at forbidden pitch and isolated should be a big challenge for manufacturing random logic devices. In order to overcome these challenges, we have proposed a new RET using attenuated mask with phase shifting aperture, named Mask Enhancer. In this study, we apply Mask Enhancer on sub-100nm pitch contact hole printing with 1.35NA ArF immersion lithography tool, and ensure that Mask Enhancer can improve MEEF at resolution limit and DOF at semi-dense and isolated pitch region.

Mask Enhancer for contact hole fabrication consists of three features, those are the main aperture, the halftone background, and the shifter aperture. The phase of background is the same as main aperture, while that of the shifter aperture has the opposite phase. We can enhance the image contrast of the hole pattern with this mask configuration. In this study, we adopt a high transmittance blanks on Mask Enhancer to balance lithographic performance for the resolution limit to the isolated to ensure a sufficient process margin for random logic contact hole layout pattern. Furthermore, we newly design a shifter aperture structure taking into account light transmittance degradation caused by an effect of mask 3D structure.

In this study, we demonstrate the random 2D layout contact hole printing by using Mask Enhancer. As one of the general 2D layout, we successfully print a fine 100nm pitch line of contacts and isolated contact simultaneously with MEEF of less than 4. Thus, Mask Enhancer can achieve sub-100nm pitch random layout contact hole printing without any characteristic issues of random 2D layout printing, such as MEEF, sidelobe printing and hole roundness. We strongly propose that Mask Enhancer is one of the most effective solutions for random logic layout contact hole fabrication for 32nm node and below.

7640-46, Session 10

Suppressing ringing effects from very strong off-axis illumination with novel OPC approaches for low-k1 lithography

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With the delay in commercialization of EUV and the abandonment of high index immersion, fabs are trying to put half nodes into production by pushing the k1 factor of the existing scanner tool base as low as possible. A main technique for lowering lithographic k1 factor is by moving to very strong off-axis illumination (i.e., illumination with high outer sigma and a narrow range of illumination angles), such as Quadrapole (e.g., C-Quad), custom or even dipole illumination schemes. OPC has generally succeeded with either rules-based or

simple model-based dissection and target point placement schemes to date. Very strong off-axis illumination, however, creates pronounced ringing effects on 2D layout and this makes these simpler dissection techniques problematic. In particular, it is hard to prevent overshoot of the contour around corners while simultaneously dampening out the ringing further down the feature length. In principle a sufficiently complex set of rules could be defined to solve this issue, but in practice this starts to become un-manageable as the time needed to generate a usable recipe becomes too long. Previous implementations of inverse lithography demonstrated that good CD control is possible, but at the expense of the mask costs and other mask synthesis complications/limitations. This paper first analyzes the phenomenon of ringing and the limitations seen with existing simpler target placement techniques. Then, different methods of compensation are discussed. Finally, some encouraging results are shown with new traditional and inverse experimental techniques that the authors have investigated, some of which only demand incremental changes to the existing OPC framework. The results show that new OPC techniques can be used to enable successful use of very strong off-axis illumination conditions in many cases to further reduce lithographic k1 limits.

7640-47, Session 11

3D physical photoresist model build and verification for profile-based pattern correction

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Lithography prognosticators of the early 1980's declared the end of optics for sub-0.5 m imaging. However, significant improvements in optics, photoresist and mask technology continued through the mercury lamp lines (436, 405 & 365nm) and into laser bands of 248nm and to 193nm. As each wavelength matured, innovative optical solutions and further improvements in photoresist technology have demonstrated that extending imaging resolution is possible thus further reducing k1.

Over the past 40 years from the early development of photoresist parameters by Dill1 to recent work on calibrated models by Patsis2; major improvements in predictability have been achieved. Although these models are significant improvements they have not been used to predict resist profiles through a wide range of conditions. In the near future, predictive models will need to be accurate enough to predict nm variation across an entire field and across multiple device architectures.

The focus of this paper is to explore the limitations of contour based process models. We demonstrate the capabilities of 3D physical resist models and provide insight into etch effects from resist profiles not available with in contour based models. The authors will demonstrate the use of a full 3D resist model. Accuracy and the predictability of the model will be described and demonstrated in a full field over a range of structures and features. Additional data will be presented on the quality of these models along with required data needed to achieve targeted model accuracy specifications.

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7640-48, Session 11

The feasibility of using image parameters for test pattern selection during OPC model calibration

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Model Based Optical Proximity Correction (MB-OPC) is essential for the production of advanced Integrated Circuits (ICs). As the speed and functionality requirements of ICs production always require reducing the Critical Dimension (CD), the demand is continuously increasing for more accurate and representative OPC models.

Calibration of models using measured test pattern data is the most critical step in building accurate OPC models. Test patterns are selected to represent the final patterns to be printed in any specific technology that will use the OPC solution. As some aspect of the OPC model calibration includes empirical fitting of the data collected, it may seem that more data is better. On the other hand, reducing metrology time is also critical, and therefore a trade off must be made to obtain adequate number of data points without overloading the metrology tools and resources.

Image parameters (IPs) based selection is a technique that may identify important test patterns, as it is one of the basic principles of variable threshold resist modeling. The basic resist model equation is an empirical function in which coefficients to the IPs are found by fitting the experimental data. Therefore, it is logical to think that IPs are the most important aspect that the resist equation can "see". In this paper, we test the viability of this assumption by building a dense OPC model based on test patterns only selected for their importance for the IP consideration and compare it to the normal OPC model built with test patterns selected using other criteria. The result of the study will show whether or not IP space can be the sole selection criterion.

In the second part of the paper, we investigate the effect of the data volume on the quality of the OPC model, by reducing the number of data points gradually to see where the OPC model will break down and we start to see significant difference in the OPC model performance. The experiment is aimed to show when adding data is redundant and not necessary to OPC model calibration. This is again an attempt to reduce metrology resources without sacrificing the OPC model quality.

The study is important to the modeling engineers as well as to the metrology engineers, to demonstrate the effect of the trade off between data volume and metrology time.

7640-49, Session 11

Optical proximity correction enhancement by using model-based fragmentation approaches

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As the industry progresses toward smaller patterning nodes with tighter error budgets and narrower process windows, the ability to control pattern quality becomes a critical, yield-limiting factor. In addition, as the feature size of design layouts continues to decrease at 32nm and below, optical proximity correction (OPC) technology becomes more complex and more difficult.

From a lithographic point of view, it is the most important that the patterns are printed as designed. However, unfavorable localized CD variation can be induced by the lithography process, which will cause catastrophic patterning failures (i.e. ripple effects, and severe necking or bridging phenomenon) through process variation. It is becoming even more severe with strong off-axis illumination conditions and another resolution enhancement techniques (RETs). Traditionally, it can be reduced by optimizing the rule based edge fragmentation in the OPC setup, but this fragmentation optimization is very dependent upon the engineer's skill. Most fragmentation is based on a set of simple rules, but those rules may not always be robust in every possible design shape.

In this paper, we have tried to identify and solve the root cause of the problem. We have investigated the influence of illumination sources to the ripple effect for various pattern shapes and sizes, and then explored different problematic structures for a metal layer which showed localized CD variations. A model based approach for solving these imaging distortions has been tested as opposed to a previous rule based one. The model based approach is automatic correction techniques for reducing complexity of the OPC recipe. This comes in the form of automatically adjusting fragments lengths along with feedback values at every OPC iteration for a better convergence. The

stability and coverage for this model based solution has been tested throughout process variability. A comparison between rule based and model based ones for spent efforts and solution effectiveness has been conducted. Finally, the model based approach has been tested for its extensibility to the 22nm node, where double dipole is considered an option.

7640-50, Session 11

Automation of sample plan creation for process model calibration

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The process of preparing a sample plan for optical and resist model calibration has always been tedious. Not only because it is required to represent accurately full chip designs with countless combinations of widths and spaces, but also because of the constraints imposed by metrology which may limit the number of structures to be measured. There can be other limits on the types of these structures, and this is mainly due to the accuracy variation across different types of geometries. For instance, 1D measurments are normally more accurate than measurements from 2D patterns. Thus, only certain geometrical shapes are normally considered to create a sample plan for model calibration. In addition, as we move from technology to technology node, the time available for developing models along with the processes is either reduced or more people are need to work on the models and data collection. The desire to collect more data over more process conditions to assure model accuracy also puts more requirements on the sample plans and metrology.

In this context, an automated flow is proposed for sample plan creation. Once the illumination and film stack are defined, all the errors in the input data are fixed and simulation sites are centered. Then, bad sites are excluded. Afterwards, the clean data are reduced based on aerial image parameters analysis. Also, an editable database of measurement-reliable and critical structures are provided, and their percentage in the final sample plan as well as the total number of 1D/2D samples can be predefined. This methodology can be applied for creating calibration and verification sample plans. It has the advantage of eliminating manual selection or filtering techniques, and it provides powerful tools for customizing the final plan, and the time needed to generate these plans is greatly reduced.

7640-51, Session 12

SMO for 28-nm logic device and beyond: impact of source and mask complexity on lithography performance

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To realize wide process window with pattern shape fidelity in low k1 lithography, the selection of illumination-source shape is getting extremely important [1-2]. The lithography process window can be greatly improved by the co-optimization of the source shape and mask patterns [3-5]. This paper covers the application of source and mask optimization (SMO) techniques to the latest logic device patterns such as 28-nm node and beyond. We systematically study the impact of source and mask complexity on designs with different k1 and pitch distribution. To facilitate this study, a new advanced distributed computation platform is used to enable computation speed and optimization turn around time.

Logic design patterns with a range of pitch distribution and a SRAM pattern are investigated. The pitches are varied based on the smallest pitches used in 28 nm logic node and beyond. For these cases, we study the impact of the complexity of the source and mask on the co-optimization result. On the source side, we will compare the results for the new programmable illuminator (ASML's FlexRay) and for traditional DOEs (diffractive optical element) that meet scanner specific parameters. On the mask side, we control the mask complexity by enforcing the assist feature configuration to be either rectangular, freeform, or main pattern like while varying the mask manufacturing rule check (MRC).

We then evaluate the process window with different source and mask complexity through a range of k1 values. With the results, the cost effective approach for the device production is shown, based on the balance between lithography performance and costs in mask, source and computation time in OPC and SRAF generation. The impact of mask topology effect on source shape and assist feature printability is also investigated.

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7640-52, Session 12

Illumination optics for source-mask optimization

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Source Mask Optimization (SMO) is proposed and being developed for the 32 nm generation and beyond in order to extend dose / focus margin by simultaneous optimization of the illuminator source shape and a customized mask. For several years now, mask optimization techniques have been developed. At the same time, the flexibility of the illuminator must also be improved, leading to more complex illumination shapes. As a result, pupil fill is moving from a parametric model defined by sigma value, ratio, clocking angle, subtended angle and/or, pole balance, to a free-form condition defined by light intensity in the illuminator. In short, the illumination source shape is becoming a beautiful painting or a Rorschach test pattern.

Various illumination source shapes, using extremely small sigma, multi-illumination poles, such as cross-pole and dipole are currently used for critical layers. Currently, the most complicated illumination source shapes are combinations of small sigma and multi-pole illumination. Nikon has provided variable illuminator using sPUREs to meet the requirements of the source shapes used in current ArF lithography.

The feature size patterned by photolithography continues to shrink, driven by Moore's Law scaling. In immersion lithography, additional aggressive technology has been developed such as double patterning and mask enhancement technologies like PSM (phase shift masks, either attenuating or alternating) for RET (Resolution Enhancement Technology) where the projected feature size is below optical resolution. The illuminator is one of the key elements to realize strong RET. In the past we developed a polarized-light illuminator for ArF lithography as one way to enhance RET.

In this paper we will discuss the methods and hardware for achieving complicated source shapes in the Nikon S620 immersion scanner. In particular, we will discuss the requirements of high pixel resolution and gray scale levels in the pupil, and how this illuminator can be used for development of 32 nm technology.

7640-53, Session 12

Considerations in source-mask optimization for logic applications

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With the advance of semiconductor roadmap, optical lithography is close to its resolution limits because of the limited wavelength and numerical aperture (NA) scaling. Source-Mask optimization (SMO) [1,2] is one of key computation lithography techniques promising to deliver the improvements over traditional RET/OPC methods. It involves co-optimization of both source and mask patterns for series of ground rule patterns and deliver the final optimal source for full chip mask optimization. SMO provides the opportunity to utilize every pixel of illumination pupil and optimize the printing of all critical patterns together to push the ground rules closer to the physical limits.

To deliver the promise of improved process window, besides good optimization algorithms to search for optimal solutions, the SMO software also needs to have realistic merit functions and it needs to model the lithography process well together with accurate process data. This paper examined the important considerations when applying the SMO approach for global source optimization in random logic applications. The test patterns used in this study include 1D CD through pitch patterns, SRAM cells and 2D random logic cells. This study showed how the optimization outputs depend on the SMO inputs such as the selection of critical design patterns, the detailed requirements of lithography process, and accurate modeling of mask, optical and resist process. The results of this study demonstrated the importance of these critical factors which must be considered during optimization to achieve the best possible results before we can apply SMO results to lithography process successfully.

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7640-54, Session 12

Challenges for low-k1 lithography in logic devices by source mask co-optimization

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Resolution limit of ArF lithography is extended by introduction of immersion lithography. However, because of the limitation of NA at 1.35 for water immersion lithography, k1 factor should become lower and lower as the technology node advances. In fact, the k1 factor of 40 nm logic node with NA 1.2 is above 0.4, the k1 factor of 28 nm logic node with NA 1.35 is around 0.3, and the k1 factor of 22 nm node with NA 1.35 finally becomes less than 0.28.

To achieve the low k1 lithography, various methodologies such as double patterning techniques or source and mask co-optimization (SMO) technique are under investigation. The 22 nm node logic devices with minimum pitch smaller than 80 nm is almost close to the limitation of water immersion lithography. For some layers of the 22 nm devices, double patterning techniques seem to be necessary. However, considering the cost inefficiency and the complexities of pattern splitting in logic devices, double patterning should be escaped as long as possible.

For 28 nm node logic device, it is reported that both 90 nm pitch of metal layer and 110 nm pitch of contact layer are resolved by single exposure with optimized conditions [1-2]. We then investigated lower k1 region for 28 nm logic devices, keeping enough process windows. Through simulation and exposure experiment, we will verify lithography performance with free form illumination source generated by SMO, comparing to the performance with traditional diffractive optical elements (DOEs). Furthermore, we will verify the results for 22 nm node logic devices with single exposure. In this work, we will use the leading-edge programmable illuminator to produce the free form source shapes generated by SMO.

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7640-55, Session 12

A GPU-based full-chip source-mask optimization solution

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A simultaneous optimization of source and mask with full-chip capability is presented. To provide full-chip processing capability, the solution is intentionally based on GPUs and made scalable to large clusters while maintaining convergence. The approach uses a proprietary search algorithm to converge to an optimal solution while obeying existing mask manufacturing, lithography equipment and process technology constraints and geared toward maximization of process window.

At the advanced nodes, the computational lithography efforts to achieve commercially viable yields require heavy computations. As the feature sizes of on-chip structures shrink, the fundamental physical limits of traditional lithography impact design performance. At these sub-wavelength dimensions, the projecting light passing through a diffraction-limited system results in a severe distortion of patterns printed on silicon compared to those created in the semiconductor physical design process.

The ideal solution should be accurate, fast and should operate on full-chip. Toward this end, a complete solution that addresses the computational as well as speed and price requirements is presented. The solution is based on a proprietary optimization function that is applicable to both binary and phase shift masks.

In this work, we present a solution with

i) A unique mask synthesis algorithm that is based on a new mask representation: This invention advantageously and most generally represents the mask as a function with an exact analytical form over the mask region.

ii) Cluster scalability property while maintaining convergence: To implement a distributed optimization algorithm which comprises a specific cost function and a novel decoupling method, we address the scalability and overall convergence requirements.

iii) Reasonable computing requirements.

iv) Accuracy: The solution uses a complete lithography process model as a part of the mask synthesis methodology, including thick-mask effects.

v) Hierarchical processing capability for speed and fidelity, i.e., same patterns appearing at different locations of the chip are processed identically.

vi) GPU implementation: To address the need for full-chip source-mask optimization, we present a new optimization tool which leverages the capabilities of standard GPU (Graphical Processing Units) available in standard desktop computers and which simultaneously synthesizes both manufacturable mask shapes and light profiles.

The experimental results and computation run times will be provided in more detail in the regular paper submission. An exemplary result is shown in Fig 1 below. The particular platform utilized is a standard desktop computer with 4 Nvidia 260 GT series GPUs and a single Intel i7 CPU. For a random circuit pattern such as metal layer-1 at 22nm node, the full-chip computation was completed in less than 12 hours on a cluster with 100 desktop computers.

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7640-56, Session 12

Source mask optimization for advanced lithography nodes

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Source mask optimization is becoming increasingly important for advanced lithography nodes. In this paper, we present several source mask optimization flows, with increasing levels of complexity.

The first flow deals with parametric source shapes. Here, for every candidate source, we start by placing model-based assist features using inverse mask technology (IMT). This is done using the Proteus-MBAF tool. We then perform a co-optimization of the main feature (OPC) and assist feature (printability) using Proteus-OPC. The assist features are placed in the pixel domain whereas the OPC is performed in the edge domain giving a hybrid mask optimization flow, which is very fast and realizable on full chip. Finally, we do a statistical analysis of several lithography process metrics like NILS, ILS, MEEF, defocus and exposure latitude to determine the quality of the solution. There is also an option to use them as feedback to determine the next candidate source configuration. The proposed manuscript will discuss implementation of the above flow in the new Proteus-Work Bench environment. We will also present some interesting results for 22nm node for both line space (poly) and contact layer patterns. Our results obtain a good balance between often opposing metrics like MEEF and DOF. We also observe a strong dependency of the final source shape on the aggressiveness of the MBAF solution.

The second flow discussed in this manuscript is similar to above, except that a pixel-based source inverter is used to approximate the parametric source. Pixilated source optimization provides a more efficient way of exploring the source solution space. The latter can also be coupled with Synopsys mask synthesis tools to develop a joint source-mask optimization solution. Note that both source and mask are solved in the pixel domain, but the final solution consists of parametric source and traditional edge-based mask with simple rectangular AFs. Therefore, both source and mask are readily manufacturable. We also present performance analysis of the derived parametric source using Sentaurus Lithography, the Synopsys physical simulator.

The final flow consists of using the above source optimizer to obtain pixilated source solutions realizable using diffractive optical elements (DOEs) or the programmable illumination technology. This offers the maximum degree of freedom for representing the source shape. We also do a comparative analysis of the complex pixilated source with the derived parametric source, and study the loss in process window.

7640-57, Session 13

Toward ultimate optical lithography with NXT:1950i dual-stage immersion platform

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Optical lithography, currently being used for 45-nm semiconductor devices, is expected to be extended further towards the 32-nm and 22-nm node. A further increase of lens NA will not be possible but fortunately the shrink can be enabled with new resolution enhancement methods like source mask optimization (SMO) and double patterning (DPT). These new applications lower the k1 dramatically and require very tight overlay control and CD control to be successful. In addition, overall cost per wafer needs to be lowered to make the production of semiconductor devices acceptable. For this ultimate era of optical lithography we have developed the next generation dual stage NXT:1950i immersion platform. This system maximizes wafer throughput towards 200 wafers per hour and minimizes the layer to layer overlay error towards 2 nm.

The high productivity is achieved using a dual wafer stage with planar motor that enables a high acceleration and high scan speed. With the dual stage concept wafer metrology is performed in parallel with the wafer exposure. The free moving planar stage has reduced overhead during chuck exchange which also helps litho tool productivity.

In general, overlay contributors are coming from the lithography system, the mask and the processing. Main contributors for the scanner system are thermal wafer and stage control, lens aberration control, stage positioning and alignment. The back-bone of the NXT:1950i enhanced overlay performance is the novel short path encoder grid-plate positioning system. By eliminating the interferometer system used in the previous generation scanners the sensitivity to thermal and flow disturbances are largely reduced. The alignment accuracy and the alignment sensitivity for process layers are improved with the SMASH alignment sensor. A high number of alignment marker pairs can be used without throughput loss, and consequently the GridMapper functionality which is using the inter-die and intra-die scanner capability can reduce overlay errors coming from mask and process without productivity impact.

In this paper we will present the main design features and discuss the system performance of the NXT:1950i system, focusing on the improvements made in overlay and productivity. We will show data on imaging, overlay, focus and productivity supporting the 3X-nm node and we will discuss next improvement steps towards the 2X-nm node.

7640-58, Session 13

Latest performance of immersion scanner S620 with Streamlign platform for double-patterning generation

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It is widely recognized that the 32 nm half pitch node and beyond will be the age of Double Patterning. It follows that much higher productivity and overlay accuracy will be required for lithography tools in order to meet the miniaturization of devices and the increasing number of exposure steps. Previously, Nikon introduced the technical features of a new immersion lithography tool NSR-S620 based on the newly developed platform Streamlign as a solution for the Double Patterning generation.

NSR-S620 has three essential features. The first is a new metrology system called Bird’s Eye Control for high overlay accuracy. Laser encoders with a short optical path are used for wafer stage measurement in addition to interferometers, eliminating the air fluctuation error of the interferometer and leading to high accuracy. By using this hybrid metrology, the non-linearity of the encoder scale can also be easily calibrated by the interferometer. The second is a new alignment and focus mapping system called Stream Alignment for high throughput. In this new Streamlign platform, we adopt a newly developed system of five alignment microscopes named Five-Eye FIA, and an extremely wide area auto focus sensor array called Straight Line AF which covers the full wafer diameter. The configuration of Streamlign makes it possible to reduce the overhead time between the exposures remarkably. The accuracy can also be improved because many more alignment points and a continuous wafer height map without stitching are available. And third is the Modular square Structure for short setup time and easy maintenance. The main body of S620 consists of several independent modules, and some of them can be further divided into sub modules, which is the hierarchical module structure. Owing to this structure, the most appropriate unit, module, sub-module, or parts only, can be selected for replacement in accordance with the required maintenance level.

In this paper, we will show the latest performance of S620 during high scanning speed up to 700 mm/s. Some representative data of Stream Alignment including the achievement at some customer sites will be introduced.

7640-59, Session 13

Performance of FlexRay: a fully programmable illumination system for generation of freeform sources on high-NA immersion systems

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In this paper the principle and performance of FlexRay, the first fully programmable illuminator for a high NA immersion system, will be described. Arbitrary sources can be generated on demand, by manipulating an array of mirrors instead of the traditional way of inserting optical elements and changing lens positions.

This next generation illuminator is developed to give lithographers easy access to the enhanced process windows as predicted by state of the art Source Mask Optimization software (SMO) and to give virtually unlimited source tuning capability that can be used to improve matching or correct for example mask bias errors.

Besides being future proof the programmable illuminator is backwards compatible. Source shapes created using traditional illumination technology can be accurately reproduced. This allows existing recipes to run and allows same look and feel for the operator.

To evaluate the performance of FlexRay, the illuminator has been integrated in a 1.35NA TWINSCAN exposure system. We will present data of the key characteristics of FlexRay using measured traditional and freeform illumination sources: Long term and short term pupil stability and repeatability, system reliability, matching capability towards traditional Aerial illuminators and polarization performance. In addition basic system performance data on imaging, overlay and throughput will be shown.

The benefit of FlexRay for SMO is demonstrated using some application examples for memory and logic. We will show data on process window increase with SMO and enhanced proximity matching by making use of the pupil tuning capability of FlexRay.

7640-60, Session 13

High-reliability ArF light source for double-patterning immersion lithography

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Double patterning (DP) lithography is gaining widespread use in 32 and sub-32nm technology nodes as an extension to immersion lithography. While many resolution enhancement technologies (RET) have been developed recently, including source-mask optimization (SMO), and pixilated illumination schemes for the scanner, the overarching requirement for the light source in double patterning has been a need for improved optical performance stability and higher power. With the introduction of the XLR 600ix light source from Cymer last year, these requirements have been met and integrated on the most advanced DP immersion scanners on the market. Key areas of improvement include higher power with flexibility to address a wide range (60 to 90W), improved energy stability, improved bandwidth stability and improved wavelength stability. These characteristics have enabled improved CD uniformity along with higher throughput operation for the litho cell to counteract the impact of the higher cost of DP lithography.

In addition to providing improved performance, the light source needs to have higher reliability and uptime in a DP environment, as the impact of down time is magnified further when the litho cell throughput is increased dramatically. In this area, the XLR 600ix was designed to address this need by building on a proven platform and introducing features that further enhance reliability and uptime. In this paper, we will describe the challenges faced in delivering improved performance while achieving better reliability and uptime on the XLR 600ix. Areas of improvement include development of advanced optics materials and coatings to provide stable performance over a wide power range (60 to 90W), an improved control system delivering faster closed-loop feedback for optical stability over extended periods, and 'smart' on-board diagnostics with predictive capability to prevent unscheduled downtime. Data from extended life testing as well as field performance data will be presented to illustrate these improvements.

Furthermore, a novel feature has been developed to enable dramatic depth of focus (DOF) improvements for applications such as deep contact hole patterning through the use of fast bandwidth modulation. This capability has been demonstrated to show at least a 2x DOF improvement in a 32nm application, enabling higher yields in deep contact printing examples.

7640-61, Session 13

Advanced imaging with 1.35 NA immersion systems for volume production

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The semiconductor industry has adopted water-based immersion technology as the mainstream high-end litho enabler for 5x-nm and 4x-nm devices. Exposure systems with a maximum lens NA of 1.35 have been used in volume production since 2007, and today achieve production levels of more than 3000 exposed wafers per day.

In 2008 ASML introduced several improvements on immersion exposure systems to enable the production of 38-nm memory devices. With 1.35 NA, the k1 and thus process window for these applications is very small requiring tight control of system performance. Logic applications are preparing for 32-nm node and will need tight immersion defect performance and improved tool-to-tool matching control. These applications are expected to use double exposure and double patterning techniques. Additionally, more flexible illumination pupil control is needed to support the lower k1 in this semiconductor segment.

In this paper we will present the latest improvements on 1.35 NA immersion exposure systems and discuss results on imaging, overlay, defects and productivity for 38-nm memory applications and 32-nm logic applications. We will present stable and robust imaging, CDU and aberration control across the tool population. Stable sub 4 nm overlay performance is shown, with throughput levels that exceed 148 wafers per hour. Immersion defect performance is optimized for several resist processes and we will demonstrate single digit through lot performance at scan speeds exceeding 0.6 m/s .

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7641-01, Session 1

Observations of a photo engineer in the land of circuit designers

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No abstract available

7641-02, Session 1

Application of the cost-per-good-die metric for process-design co-optimization

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The extension of 193nm lithography for the volume production of sub-50nm technology nodes has required adoption of design restrictions and computational lithography. The tradeoffs between the design restrictions and computational lithography are negotiated among the engineers within the technology development group. Increasing design restrictions simplifies the lithography process at the expense of altering design practices, whereas, increasing the use of computational lithography sustains traditional design practices at the expense of increasing process complexity. It must be noted that the choice of lithography solutions and the corresponding layout design styles have severe implications on circuit topology selection. For example, transmission gate based circuits incur a larger area penalty in a uniform grating based layout. In order to continue extending 193nm lithography to future technology nodes we need to focus on process-design co-optimization by efficiently restricting circuit and layout styles to enable lithography processes with k1 factor of less than 0.35.

A metric that can quantify the impact of the various circuits, layout and lithography decisions during the early stages of technology development is required to facilitate the process-design co-optimization. The cost-per-good-die is the metric that enables a tradeoff between process cost, yield and silicon area requirements and provides a basis for holistic co-optimization. In this paper we will first outline the considerations for computing the cost-per-good-die. We will then apply the cost-per-good-die to evaluate the optimal library selection for the design of an ASIC in the 32nm technology node. Specifically, we will compare three different template libraries, each mapped to a different regular design fabric, to determine the implementation that minimizes the cost-per-good-die metric. Templates are physical instantiations of single staged logic functions that are implemented using circuits that are efficiently mapped onto regular design fabrics [1, 2]. For each one of these template libraries we determine the minimum die size required by performing a series of place and route experiments, computing the functional yield based on critical area analysis and systematic effects, and calculating process cost based on the optimal lithography solution [3]. These results are compared to an estimate of the same ASIC implementation based on using a typical standard cells designed to follow conventional design rules and a more regular standard cells designed using a recommended set of design rules.

In addition, we also describe the details of a framework designed to estimate the cost-per-good-die for SRAM arrays. The framework incorporates parameterized models for SRAM array area, post-repaired functional and parametric yield and process costs to evaluate the cost-per-good-die. We will discuss results on applying this framework to determine the optimal combination of lithography solution as well as bitcell topology for the 22nm technology node by comparing the double patterning (DPT), source mask optimization (SMO), and interference based lithography (Intf) for both 6T and 8T SRAM bitcell topologies.

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7641-03, Session 1

Taming the final frontier of optical lithography: design for sub-resolution patterning

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The persistent uncertainty regarding the timely availability of next generation lithography solutions is forcing leading edge semiconductor manufacturers and their designers to grapple with the reality of having to enable sub-resolution patterning solutions. After breaking through the k1=0.5 barrier in the 65nm technology node, the rapidly approaching 20nm node will be pushing high-NA 193nm immersion lithography well below the fundamental limits even of frequency doubled optical lithography. Maintaining the industry’s pace of cost-per-function scaling will rely on the development of wafer-level patterning enhancements that effectively double the lithographically achievable pattern density. While the general patterning feasibility of two such process enhancements: pitch splitting (PS) and sidewall image transfer (SIT), has been demonstrated, previous work on strong RET, such as altPSM, has also proven the need to include design’ability in the overall technology feasibility assessment and optimization. Resolution enhancement technology development once focused solely on process window optimization, but the times when patterning choices where completely transparent to designers are gone, and the degree to which specific patterning choices impact design is becoming a decisive factor in choosing the optimal patterning process.

Since frequency doubling patterning enhancements inevitably increase wafer process cost and can impact achievable chip area reduction, cost effective technology scaling to the 20nm node and beyond will depend on detailed optimization of every step in the design-to-silicon flow.

This paper outlines the topology restrictions imposed by wafer-level frequency doubling techniques and describes how the alliance program for Bulk CMOS technology development at IBM is developing an end-to-end solution for sub-resolution patterning. The impact of topology constraints on existing design methodologies, established standard cell layout approaches, anticipated IP migratebaility goals, and qualified physical design flows will be discussed and examples of holistic co-optimization will be given.

This work was performed at the IBM Microelectronics, Div. Semiconductor Research & Development Center, Hopewell Junction, NY 12533.

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7641-04, Session 1

Realising a 45-nm system on chip in the age of variability

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In this paper, we present the challenges of the realisation of a large 45nm modern Media Processing SoC with multiple design teams distributed across many countries and time zones. We also describe the complex design methodology deployed to ensure the design is "closable" in the timing and manufacturability domain.

NXPs latest 45nm design contains >150 individual soft and hard IPs many of which were being developed concurrently with the host SoC. All these design activities must converge predictably at tape-out time. With Time to Market such a crucial factor in today's fast moving semiconductor business there is often no time for a re-spin. Right First Time is the name of the game.

During the definition phase, the SoC Physical Design Team must underpin commitments on cost, performance, area, package choice, power and the tape-out schedule to the customer. These commitments must be made long before the IP content has matured into stable design components. How do we gain confidence that our design will meet timing within such a "framework of uncertainty"?

The "traditional" approach of using complex STA sign-off-tools that analyse mature design timing data to ensure the performance targets are met pre-supposes that with a low level of optimisation in the Physical Design space the performance requirements will be met during the "Closure Phase". Real problems occur if they are not! Sign-off tools are run so late in the activity that if any "out of band" problems are found, fixing them will result in schedule slip and potentially, missed market opportunity!

In 45nm the variability is so large that it must be taken into account at all stages of the design.

Silicon variability can impact both the physical integrity and the parametric performance of the design. On top of random variations, lithography and Chemical Mechanical Polishing (CMP) can cause enough context-dependent systematic variations, requiring exhaustive lithography and CMP physical verification and optimization of the layout.

Variability due to random sources and systematic effects such as Litho, CMP and stress create a real challenge at 45nm. We can no longer presume that timing will be met across all modes and for all process, voltage and temperature combinations when we emerge at the back end of our flow. We need to manage the convergence process very carefully to ensure the design is "closable" in the timing ECO phase. We also need to talk into account the context-dependent systematic proximity effects of litho and stress.

In this paper, we present the physical and electrical DFM methodology at NXP. We will show how NXP has developed a manufacturing-aware design flow based on early prevention, detection and fixing (see Figure 1). A hierarchical approach, from IP level to full-chip, was used to reduce the runtime impact on design schedule of the model-based litho checks without compromising accuracy (see Figure 2). We will also describe how CMP checks are applied at full-chip to take into account the long-range effects of CMP, and how mode-based fixing can make design CMP-clean (see Figure 3). We also present results of variability-aware timing sign-off (see Figure 4).

Combining the complexity of large scale SoC, the uncertainty of concurrent design and the variability of 45nm is a recipe for sleepless nights for the Physical Designer. We try to show how this multi-dimensional problem can be managed in the real world of product creation.

7641-42, Session 1

Integrated fabless manufacturer and technology development

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No abstract available

7641-05, Session 2

22-nm lithography joint optimization for SRAM and logic

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The 22nm generation for logic will be challenging for optical lithography, with a contacted gate pitch of ~90nm and a minimum metal pitch of ~70nm. A gridded design approach with lines and cuts has previously been shown to allow optimizing illuminator conditions for critical layers in logic designs.[1] The approach has shown good pattern fidelity and is expected to be scalable to the 7nm logic node. [2,3,4]

A regular pattern for logic makes the optimization problem straightforward if only standard cells are used in a chip. However, modern SOC's include large amounts of SRAM memory as well. The proposed approach truly optimizes both, instead of the conventional approach of sacrificing the SRAM because of logic layouts with bends and multiple pitches.

The biggest problem in co-optimizing logic cells and SRAM bit cells is the orientation of critical layers. For SRAMs, the Gate and Metal-1 layers have lines in parallel directions, while in standard cells they are perpendicular. This would require abandoning dipole illumination for the combined optimization, and at best using some form of quadradpole.

The alternative is to design the logic and SRAMs to be unified from the beginning. In this case, critical layer orientations as well as pitches could be matched and each of the layers optimized for both functional sets of patterns.

The layout for a typical standard cell is using Gridded Design rules is shown in Figure 1a. The Gate electrodes are oriented in the vertical direction, with Active regions running horizontally. Figure 1b shows a group of SRAM bit cells designed to be compatible with the logic cell. The Gate orientation and pitch are the same.

Illuminator optimization results will be presented for the co-optimization of critical layers for both the logic and SRAM cells. This includes the choice of pitch relationships between different critical layers to minimize area while permitting high fidelity patterning.

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7641-06, Session 2

Layout pattern minimization for next-generation technologies

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In presence of the resolution scaling challenge, source mask optimization (SMO) that simultaneously corrects the source and mask to improve the overall process window is being introduced at the

22nm technology node. SMO has been assigned the highly intractable problem of determining a lithography system that can provide sufficient process window for all arbitrary patterns at sub-wavelength dimensions that could occur in conventional design rule based IC designs. To make this problem tractable, it has been suggested that designers limit the diversity of patterns in the design. The use of regular design fabrics have been proposed and successfully used to create designs by introducing deviations to an underlying regular fabric[1,2]. In this paper we will outline how the creation of designs as deviations in the grating can define a pattern set that needs be considered for lithography process characterization and optimization.

We will first describe a methodology to determine a more realistic optical interaction range for deviations in regular design fabrics and apply it to the 32nm technology node to demonstrate that the optical interaction range can be limited to 2-3 pitches as compared to 10 pitches based on pessimistic theoretical estimates. We then employ the smaller optical interaction range to screen geometrically unique patterns that lead to electrical failures in the presence of physical failures such as opens, shorts, reduced line-end coverage, etc. These extracted patterns are individually simulated and their sensitivity to the corresponding yield detractors is determined based on printability metrics such as CD change, contact coverage, printed area, etc. Finally, patterns demonstrating similar sensitivities to yield detractors are classified into equivalent pattern classes, which can be used for lithography process characterization. Experimental results of applying this technique to both line-ends and holes will be discussed. We will also discuss the challenges with finding the equivalent pattern classes that can be used for lithography process optimization across all illumination conditions.

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7641-07, Session 2

16 nm with 193-nm immersion lithography and double exposure

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Achieving 16nm designs with 193nm lithography is difficult even with immersion technology. In this work we extend on our earlier 22nm results [1],[2] to show simulation-based simultaneous optimization of layout and lithography which produces a viable approach to 16nm. This is consistent with the emerging industry consensus that regular designs and multiple exposure techniques will extend 193nm immersion as far down as 7nm [3].

The approach relies on 1D Gridded Design Rules with Lines/Cuts (1D GDR LC) selective double patterning. Due to the highly regular patterns of 1D GDR LC we are able to determine a sharp lithographic optimum as a result of numerical co-optimization of key layout para-meters and lithography settings such as scanner illumination, etc.

Critical layers (cuts in 1D GDR LC) consist of a number of identical cut patterns with varying density. We use large cells considered the worst case from a standard cell library and show that after co-optimization CD error can be brought below 1nm at best focus conditions. We further consider manufacturability of the cell and show Depth of Focus (DOF) and Normalized Illumination Log Slope (NILS) metrics before and after co-optimization.

Finally, thanks to close ties to a leading scanner manufacturer we were able to consider realistic lens distortions using experimentally obtained Jones-Zernike expansions as well as realistic entrance pupil illumination. Imaging properties of idealized scanner lens and illumination are compared to a realistic scanner lens model at 16nm. Direct process optimization in scanner variables as well as scanner-specific optimization of lithography settings and manufacturability analysis are shown.

Co-Optimization of Layout and Lithography

Simultaneous optimization of layout patterns and lithography settings is made possible by the uniformity and repeatability of the lines/ cuts patterns (Fig. 1). We use direct optimization and experimentally validated lithography simulation for the critical cuts layers. Optimization variables are:

cuts geometry (width, height, hammer heads)

illumination of the scanner lens entrance pupil

each individual cut is biased (over/undersized) to account for proximity effects

The optimization cost function was the RMS CD error across all cuts. Minimizing this cost function also reduces variation among cuts by getting all CDs close to the same target value.

Link to Scanner Data

A data base capturing the measured lens entrance pupil illumination was built in collaboration with an industry leading scanner manufacturer. As a result, we were able to carry out optimization directly in equipment variables such as lens zoom settings, apertures, etc. This ensures practical relevance of results and provides an interesting comparison between idealized and realistic illumination patterns. In addition, measured lens polarization effects and distortions are included using Jones-Zernike expansions, providing scanner-specific manufacturability predictions (Fig. 2).

Results and Conclusions

Design-process co-optimization for 1D GDR standard cells was used to reduce CD variation and improve manufacturability of the critical cut layer. This reduction of variation substantially simplifies the layout and OPC and produces manufacturable designs at 16nm using 193nm immersion lithography.

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7641-08, Session 2

Exploring complex 2D layouts for 22-nm node using double-patterning/double-etch approach for trench levels

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With the delay of a next node lithography solution, lithographers are required to evaluate double patterning techniques such as double pattern/double etch (DP/DE) to meet scaling targets for the 22nm logic node. The tightest design rule level to pattern has traditionally been the first metal level. For this node, target minimum pitches are below 32 nm half pitch in order to meet cell area requirements. In this paper, we explore implications of the DP/DE approach when applied to complex 2D metal patterns. In addition to evaluating stitching rules for line ends, we move into complicated patterning structures such as line ends in close proximity to parallel and perpendicular metal runners, landing pads neighboring metal runners, and arrays of dense landing pads. These feature types are critical for area scaling; however, when these structures are patterned in a DP/DE scheme, the minimum area of the features needed for each pattern layer can be quite small. In this work, we explore minimum area rules for stitching together patterns as function of overlap with first pattern, minimum area and proximity to unrelated trench features on the same pattern. These results are shown

using aerial imaging technique and verified on the wafer scale using a DP/DE approach which uses current 28 nm node imaging techniques.

7641-09, Session 2

3D physical modeling for patterning process development

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In order to identify patterning process limitations, it is necessary to have a physical patterning model which would encompass the process space in 3D. Having a 3D model can complement existing OPC models and such a model can be a key enabler in patterning process development. In this paper we are going to demonstrate a 3D litho and etch model build methodology based on wafer data collection. Such a model will be able to predict, resist profile, and post etch pattern profile on integrated wafers with topography.

We will demonstrate how a physical model can act as a forensic tool for OPC and ground-rule development. As shown in fig, Fig 1 below, the 2D modeling shows no issues in printing gate lines but 3D modeling shows severe resist loss in the middle. In absence of corrective measure, there is a high likelihood of line discontinuity post etch. Such early insight into process limitations of prospective ground rules can be invaluable for early technology development. Fig 2 shows a broken poly-line after etch. S-litho resist simulation shows resist necking in the region of STI(shallow Trench Isolation) step height and can explain such broken line after RIE process.

In addition such a 3D physical model could be used for early resist evaluation and selection for required ground-rule challenges, which can substantially reduce the cycle time for process development.

Finally we plan to extend the such physical modeling through etch to generate a comprehensive physical model that could be used to predict process limitations at a much earlier time frame in technology development.

7641-32, Poster Session

A library based OPC methodology for run-time reduction

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Optical Proximity Correction (OPC) is a commonly used resolution enhancement technique (RET) for improving printing fidelity. Along with the shrinkage of critical dimension, conventional geometrical OPC approach often results in complicated mask and requires expensive computational effort. To address the mask complexity issue, a device performance-based OPC (DPB-OPC) algorithm which operates based on parametric current, rather than desired layout pattern as in conventional OPC, has been proposed to achieve considerable mask data saving. However, the performance gain is currently limited by the comparatively longer run-time. Due to the iterative performance evaluation of every transistor, the OPC run-time is also anticipated to be exponentially increasing with the number of transistors.

In the paper, we present a library-based DPB-OPC methodology for synthesized digital circuit. In order to improve the run-time efficiency of the previous work [1], the cell-wise OPC strategy is adapted into the proposed methodology. For any synthesized digital circuit, it is basically formed by instantiating and joining the standard cell layouts provided by foundry libraries. Hence by analogy, the OPC mask for the synthesized digital circuit can also be formed by stitching the respective cells' OPC mask per placement order. By first pre-characterizing the OPC mask for each standard cell during the library database construction, the computational time for generating full chip OPC mask can be shortened. However, it should be pointed out that different boundary cells introduce different optical proximity effects that subsequently contribute to different printing result between the standard cell wise DPB-OPC and conventional full chip DPB-OPC. Various methods were proposed in literature to reduce the discrepancy [2] but all are based on the aim of geometrical shape reproduction. With the renewed objective of minimizing the electrical performance in DPB-OPC, the electrical impact of the OPE will acquired and used to guide the dynamic correction.

The proposed methodology is illustrated in Figure 1. First, the DPB-OPC mask for each standard cell is generated using the framework proposed in [1] and stored as library database. Then, the full-chip DPB-OPC mask for synthesized digital circuit is initialized by stitching the pre-characterized DPB-OPC mask of the respective instantiated standard cell. As explained earlier, the proximity effects induced by different surrounding environment could affects the post-litho print image and thereby the device performance. Hence, a localized refinement step based on the diagnosed "device performance disturbance" is then performed to minimize the performance shift.

A benchmark circuit c432 is used in the simulation. Table 1 compares the run-time and performance matching of the two cases: full chip DPB-OPC and our library-based DPB-OPC. When compared to full chip OPC, run-time reduction of 13X is achieved with at most 8.98% of Ion performance deviation.

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7641-33, Poster Session

Tracking systematic defects hidden by random defectivity in mature technology yield

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For mature technologies, main yield detractor is random defectivity. Nevertheless, some devices present higher defectivity than rest of devices. Out of process accident, design related defect is one of suspected root cause. Also, design-based defect type is expected to increase as technology node decrease. Determining origin of these additional systematic defects is not easy as these defects are usually residual for technologies in production, not always predictable by OPC simulator (ex: void defect in active STI structure), and at least hidden by random defectivity after classical wafer inspection control. How much this systematic defectivity cost to yield, especially for mass production devices? If design dependency and contribution to yield loss is proven, feed-back mask correction by OPC is then a possible solution to solve the marginality. In this paper, an automatic flow to track systematic defects within global defectivity and estimate their yield impact is presented. This flow starts with a relevant selection of several inspection defect files for a given layer. Then the Design Based Binning (DBB) tool performs a fine alignment of the whole multi inspection defect data set with design file. The resulting aligned defect file is treated by an efficient pattern matching algorithm [1] to generate a design-based binning (DBB) defect file. The integration of this output defect file into a defect database allows easy defect analysis and statistical correlation to electrical results. Impact on yield loss is evaluated for every design-based defect found. Feed-back OPC correction on mask is performed afterward if needed (Fig. 1). An example of a suspected design-based defect analysis for a 90nm node device is presented at the end of this paper.

7641-34, Poster Session

Pattern-based OPC acceleration for performance and cost saving in mask synthesis flow

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At advanced technology nodes, computational and economical burden of model-based Optical Proximity Correction (OPC) has increased tremendously due to complicated process models for process window compensations in addition to proximity correction. There is a growing problem where OPC users at every new technology node must double OPC tool licenses and CPU numbers in order to complete one critical layer of OPC generation within a few days. In this paper, an easy-to-adopt pattern-centric OPC acceleration methodology is discussed, which will significantly shorten OPC cycle time and lower cost of ownership in mask synthesis flow.

Pattern-based OPC Accelerator (POA) analyzes full chip design space geometry information with Anchor's proprietary pattern-centric algorithms. A layout partition is performed to create unique patterns; and patterns are stored in a pattern library. Highly efficient structure of a pattern library organizes data so that OPC patterns can be quickly retrieved for pattern matching operation. OPC data is reused for matched patterns in the library to improve performance efficiency. The OPC pattern library can be built up incrementally. The more complete the library as pattern coverage goes, the more performance gain is recognized. There are no additional OPC models and recipes needed for using this acceleration approach.

In this paper, pattern-based OPC Accelerator application flow is demonstrated up to 10 times faster turnaround time for 45nm customer logic designs over conventional OPC flow. Production-worthy POA usage model, deployment and 3rd party OPC tool integration will be discussed.

7641-35, Poster Session

Device performances analysis of standard cells transistors using silicon simulation and build-in device simulation

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We developed a simple methodology to predict transistors performances due to systematic lithography and etch effects. In general, our methodology is based on full silicon simulation, followed by device modeling (derived from SPICE simulations). The equations for device modeling were incorporated into the silicon simulator, enabling easy and efficient analysis with one simulation tool. We used our method to analyze a small and large arrays of standard cell blocks, manufactured using Tower TS013SL (0.13um Standard Logic for General Purposes) Platform. Electrical parameters, like drive current (Idsat), Off current (Ioff) and transistor speed (Gate delay) were calculated. Comparison between different transistors types, having the same W/L but different layout configuration and different layout environment (around the transistor) was made in terms of performances as well as process variability.

7641-36, Poster Session

Detection of OPC conflict edges through MEEF/NILS analysis

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Semiconductor foundries at 65nm, 45nm, and more advanced technologies have witnessed high-yield mass production to be intimately correlated to the practice of adaptive DFM (Design for Manufacturability). Due to the interaction of design and process marginality, hotspot layout patterns have become a growing concern to achieve satisfactory chip yield. With device performance variance easily exceeding 50% for 65nm and below, adaptive actions by designers, like modifying layouts to relieve potential DFM risks, is found to be a very efficient approach to high yield manufacturing. Rigorous MEEF/NILS estimation based methods have been proposed to achieve adaptive DFM by predicting mask writing variations at early stages (cell/block levels) of designs.

In a recent study, we discovered that by adding MEEF/NILS check in simulation contour based OPC verification flow and by comparing MEEF/NILS changes of pre and post OPC hotspots, it is possible to separate OPC issues from design issues, in particular, for hotspot patterns with tight spaces with little room for any biases. We found that hotspot patterns with tight spaces usually create OPC conflict edges-correct one edge will result increasing MEEF at the other edge, or vice versa. While advancement in OPC technology continues to improve MEEF performance, nevertheless, OPC-conflicting edges almost always exist in designs at 65nm and below.

In this paper, we first demonstrate the existence of OPC conflict edge hotspots using MEEF/NILS analysis, in particular, the MEEF increase after OPC on those edges actually has smaller process window than pre-OPC ones. In certain cases, design modification is necessary to correct such OPC conflicting edges. Based on the finding, we propose a practical methodology of detecting design related OPC edge conflicting hotspots in a pattern centric software-based DFM flow. The methodology is aiming at detecting patterns containing such conflicting edges and pursuing layout actions on the design side to eliminate this issue. We will validate the flow using a real design case. In addition, the OPC edge conflicting hotspots can be clipped and saved in a designated pattern library as hotspot templates, and incoming designs can be quickly screened using exact and similar pattern search with those saved templates in the library.

7641-37, Poster Session

Practical use of the repeating patterns in mask writing

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Since May 2006, the Mask Design, Drawing, and Inspection Technology Research Department (Mask D2I) at the Association of Super-Advanced Electronics Technologies (ASET) has been researching and developing for reducing the mask manufacturing cost and TAT by concurrent optimization of MDP, mask writing, and mask inspection.

From viewpoint of MDP, we have thought that we can reduce the shot counts during the electron beam writing and contribute to cut the cost and TAT throughout manufacturing process by utilization repeating patterns extracted from OPCed mask data as Character Projection (CP).

We developed the extraction software which extracts common CP from multiple mask data.. And we also developed the mask data preparation software which considered the influence of proximity effect.

In this paper, we will report the practical use of the repeating patterns in mask writing.

7641-38, Poster Session

EM calibration based on post-OPC layout synthesis

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Design for Manufacturability (DFM) we know involves changes to the design and CAD tools to help increase pattern printability and improved process control. Design for Reliability (DFR) performs the same to improve reliability of devices from failures such as Electromigration, hot electron degradation and NBTI. For EM calibration, DFR based tool flows extract design geometries and perform RC extraction to obtain current density information that is used to estimate the Mean Time to Failure (MTTF) of the device. Extraction here is done using field solvers on drawn, pre-OPC layouts and layout modifications such as wire

sizing and spacing is done pre-OPC. As interconnect densities increase with each technology generation, the lithographic processes required to print all features with acceptable irregularities have become highly complex. RET techniques such as OPC and PSM implement changes to the drawn layout. Post-OPC layouts contain modifications to the drawn mask with extra features such as SRAFs, jogs, hammerheads and serifs that change their resistance, capacitance and current density values. Hence, calibrating EM based on drawn layouts leads to overly optimistic layout changes in some regions and overly pessimistic changes overall. Currently, there are no available tools that perform analysis on post-OPC layouts for EM calibration. In this work, we attempt to approach the design for reliable manufacturability (DFRM) problem by setting up a framework to perform effective EM calibration through post-OPC layout RC and current density analysis.

In this approach we classify the EM calibration into AC and DC flows. AC flow aims to analyze current density for interconnect lines that carry signals across the layout. The DC flow aims to model current density for global power rails. Global power rails are "slotted" to improve the pattern density that controls CMP induced thickness variation. Slotting is the process of embedding square holes filled with oxide within wide metal lines to improve pattern density. Slotting prevents dishing during the CMP process. OPC after metal fill synthesis performs external modifications to the power rails to improve their printability. The compounding effect of slotting and OPC is not considered when EM is calibrated for global power rails. The DC flow performs analysis to fill this void in the design flow.

The proposed solution uses a model based shape analysis coupled with current density based MTTF analysis using Black's Electromigration formulation. In the next step a DFM compliant layout modification is used to fix EM rule violations.

7641-39, Poster Session

OPC on a single desktop: a GPU-based OPC and OPV tool for fabs and designers

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In semiconductor manufacturing, software simulations and correction tools have been used for the past several years to minimize lithography-related yield loses and to improve printability. Unfortunately, these computations, commonly called Optical Proximity Correction (OPC), and Optical Proximity Verification (OPV) are very extensive, requiring CPU-based clusters with several thousands of nodes and taking weeks of iterations. The problem is becoming exponentially worse as the industry moves to more advanced nodes; since modeling the lithographic process requires extensive multi-physics computations and the number of elements increases geometrically as feature sizes decrease.

Due to the associated high cost of acquiring and maintaining the requisite computational hardware, only the chip manufacturers (the so-called "Fabs") have been able to afford this approach. Absence of similar tools for designers cause iterations between Fabs and designers, subsequently elongating the process to achieve commercially viable yields.

The ideal solution would be one that is accurate, fast and affordable; so that it is also accessible to chip designers. This implies that the cost of computational hardware should be affordable and that the speed and accuracy of the algorithm should be sufficient to complete a full-chip computation overnight. Toward this end, a complete solution, one that addresses the computational as well as price requirements, is presented. Given the issues associated with present tools, our solution uses graphics processors (GPUs) as well as CPUs as computation hardware to achieve a breakthrough improvement in speed and affordability. The solution can be simultaneously used by chip designers as well as manufacturers.

In this study we show that the solution is:

i) Capable of implementing the higher fidelity models of the lithographic process. To adequately capture the salient physics and chemistry involved in printing more advanced nodes, a far more complete multi-physics model is required than is used today. The proposed solution introduces a mechanism and computational power to achieve the required precision. All the requisite process models for the complete litho path simulation, such as thick-mask effects, have been included.

ii) Scalable to large clusters. To utilize such an approach requires the use of distributed algorithms; i.e., ones that support parallel computation.

iii) Extremely fast: By utilizing a set of proprietary algorithms, we have been able to improve the compute power of typical commodity desktop computer from GFLOP level to TFLOP levels for typical OPC/OPV tasks.

The experimental results and computation run times will be provided in more detail in the regular paper submission.

The solution enables a full-chip OPC work completed overnight on a single desktop computer. The particular platform utilized is a standard desktop computer with 4 Nvidia 260 GT series GPUs and a single Intel i7 CPU. For a random circuit pattern such as metal layer-1 at 45nm node, the full-chip OPC job was completed in less than 12 hours. Please note that, more detailed numbers will be presented in the regular paper submission.

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7641-40, Poster Session

A GPU-based full-chip inverse lithography solution for random patterns

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An inverse lithography solution based on optimization is presented. The optimization approach, in effect, operates as an inverse lithography tool, based on modeling and simulation of the manufacturing process. Given the associated computational requirements, the proposed solution intentionally uses graphic processors (GPUs) as well as CPUs as computation hardware. Due to the approach we employed, the results are optimized towards manufacturability and process window maximization.

In semiconductor manufacturing, software simulations and correction tools have been used for the past several years to minimize lithography-related yield loses and to improve printability. As the feature sizes of on-chip structures shrink, the physics of the lithographic process become highly complex and traditional OPC methods don't produce satisfactory results.

Studies on inverse lithography technology (ILT) have usually resulted in superb lithography. To date, though, ILT implementations in a production environment have, in general, proved impractical due to: intractably long computer run-times; and non-manufacturable mask designs. Due to the unrealistic computational requirements, utilization of ILT methods presented to date has been limited to process a smaller portion of layouts. In addition, the ill-conditioned mathematical process model has been a factor to use an approximation for the inverse lithography, limiting accuracy [LTI paper]. Some other approaches that introduce mask manufacturability constraints after a mask has already been synthesized are inherently prone to non-manufacturable or sub-optimal results[ ]. Since to the computational requirements for the pixel-based approaches are proportional to the grid density, these solutions generally sacrifice fidelity for run time.

In this work, we present a solution with

i) A unique mask synthesis algorithm that is based on a new mask representation: This invention advantageously and most generally represents the mask as a function with an exact analytical form over the mask region.

ii) Cluster scalability property while maintaining convergence: To implement a distributed optimization algorithm which comprises a specific cost function and a novel decoupling method, we address the

scalability and overall convergence requirements.

iii) Reasonable computing requirements: Fab houses already employ CPU clusters comprising several hundred to several thousand processors. Any practicable ILT solution should not require more than this many processors.

iv) Accuracy: The solution uses a complete lithography process model as a part of the mask synthesis methodology, including thick-mask effects.

v) Hierarchical processing capability for speed and fidelity, i.e., same patterns appearing at different locations of the chip are processed identically.

The experimental results and computation run times will be provided in more detail in the regular paper submission. An exemplary result is shown in Fig 1 below. The particular platform utilized is a standard desktop computer with 4 Nvidia 260 GT series GPUs and a single Intel i7 CPU. The ILT algorithms are implemented on GPU/CPU and run time is tested with a variety of layouts. For a random circuit pattern such as metal layer-1 at 22nm node, the full-chip computation was completed in less than 12 hours on a cluster with 100 desktop computers.

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7641-41, Poster Session

Line-edge roughness effects on transistor performance: the role of the gate-width design

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Line Edge/Width Roughness (LER/LWR) is one of the main sources of the statistical variability in the conventional bulk MOSFETs with increasing importance as device dimensions scale down. Up to now, the vast majority of works has focused on the origins and metrology of LER/LWR initially formed on resist lines during lithography. However, recently the question on whether and how layout design can control LER/LWR effects on device performance has been addressed. To this perspective, the LER implications on OPC methodology algorithm and the measurement and analysis of transistor layout effects on actual LER have been studied [1,2].

In this paper, the focus shifts to the role of a basic design parameter, the gate width, in the effects of LER/LWR on transistor performance. We investigate this role by using a 2D simulation approach and employing two mathematical results of statistical theory. The first statistical result says that the rms value of the LWR of the gates in an integrated circuit fabricated by the same manufacturing process depend on their width. More specifically, the mean rms value of gates with the same width (iso-width gates) decreases as the gates become narrower. The second mathematical result dictates that the iso-width gates have also a distribution of lengths (CD values) about the nominal gate length and the variance of this distribution increases as gate width decreases and the transistor becomes narrower. These dependencies of rms and CD variance are counteracting with respect to gate width changes [3,4].

In order to examine the implications of the above results to LWR effects on transistor performance, we generate long lines by the well-known inverse Fourier transform technique, which simulate the lines fabricated by manufacturing [3]. The LWR parameters of these lines, given as input in the generation algorithm, are considered characteristics of the used manufacturing processes. From these lines, we obtain segments representing the gates in a circuit with width equal to the segment length. These gates will have a distribution of rms values and average lengths, whose mean value and variance respectively depend on gate width according to the statistical results referred above.

The effects of the gate LWR on voltage threshold and off-state leakage current variations are simulated by the 2D approach proposed by Oldiges [5] in which the transistor is considered a parallel connection of 2D ultra-small sub-transistors with no roughness but with varied lengths. The results of the simulation approach reveal that for sub-50nm nominal gate lengths, larger gate widths lead to lower variations in voltage thresholds and leakage currents and thus to higher yields. Thus, it seems that appropriate changes in design parameters, such as gate width, can soften LER/LWR effects on transistor performance without altering the used manufacturing processes.

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7641-10, Session 3

Systematic failure debug and defective pattern extraction for FPGA product-yield improvement

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Finding systematic failures in designs and OPC/process related marginalities are critical for semiconductor product debug. How to integrate wafer defect inspection data, wafer sort yield, test pattern failures to the design circuit layout and physical verification flow has become the key to successful product development and fast yield ramping.

The conventional way to do FPGA product debug is to throw different diagnostic patterns to purposely test the readout results. The generated physical failure addresses (bitmaps) can produce memory cell failing signatures hinting the failing mechanism and physical coordinates of failing memory cells. The physical address is only approximate so it only indicates the layers and area where the failures are possibly located. Bitmaps are used to guide further debug such as micro-probing and cross-section. But this debug process is extremely resources consuming and requires extended knowledge of the circuits, test patterns and manufacturing process.

In this paper, we have extracted potentially problematic design patterns by matching the silicon wafer defect failure locations to design layout and memory cell test patterns failing addresses. The extracted defective patterns of the failing design patterns can help designers, OPC engineers and fab engineers to quickly pinpoint systematic failures thus improve product performance and yield.

The overlay method included two portions: one is to load KLA defect inspection results into design layout viewer, another is to load the bitmap results of memory cell blocks from the readback tests into the design layout viewer. After the KLA defects are overlaid to readback failure addresses, if the wafer defect location is within several microns to the failing test pattern address, we call it a match. We can extract the matched design patterns from the layout at this location. We can also extract all defect patterns based on pattern similarity and design cell names.

The defect inspection results from two different fabs and two different technology nodes (65nm and 45nm) have been used to demonstrate the effectiveness of this methodology. We showed some defect pattern extraction clips from one wafer where we have observed similar patterns on several wafer edge dice. They have failed v_dual bits or single bits readback tests. The KLA defect inspection SEMvision picture at one of these defect locations has confirmed possible

residuals on diffusion (active area). The tilted x-SEM picture at wafer edge further confirmed residual nitride layer from marginal STI CMP on narrow active width.

Another case involved high percentage of dual bits failures at wafer sort. We were able to correlate this type of test pattern failure to some dual contacts or vias on short metal islands. This systematic failure was finally resolved by metal litho and etch process change.

7641-11, Session 3

Modeling and characterization of contact edge roughness for minimizing design and manufacturing variations in 32-nm node standard cell

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Despite intensive attention on line-edge roughness (LER), contact-edge roughness (CER) has been relatively less studied. Contact patterning is one of the critical steps in a state-of-the-art lithography process; meanwhile, the design rule shrinking leads to larger CER in contact holes. Since contact resistance and capacitance depend on contact area and shape, larger CER results in significant change in a device current. In this paper, we present a comprehensive layout extraction methodology for analyzing process-induced CER effects on circuit performance. We first generate contact printimages from the systematic lithographic simulation and then directly implement the CER results into the contact print-images after modeling CER for various process conditions. The CER-implemented layout is saved as GDSII stream file for the subsequent non-rectangular contact extraction step, which decomposes the non-rectangular layout into several rectangular polygons to get parasitic components, e.g., resistance, capacitance, and stress parameters of an active diffusion for timing simulation. CER is modeled by power spectral density (PSD), which is a function of RMS edge roughness, correlation length, and fractal dimension.

Based on the CER variation of the contact pattern, we report a novel layout extraction model to determine systematic variability and then demonstrate the timing and power impact according to CER on circuit performance. Since a CER-generated contact makes a lot of noise on pattern edges, which may lead to larger (or smaller) electric fields, we decompose contact patterns and analyze electro-magnetic fields near the gate and contact area. To accurately calculate CER-generated contact, we propose a novel contact layout extraction method in which we first dissect the contact with a same distance of radius, and then calculate the effective resistance considering a directional factor and a weighting factor for each peel. After generating more accurate parasitic components, we back-annotate the parasitic values to the circuit netlist. In 32-nm node standard cell, MOSFET uses a stress enhancement technique in which the mobility of carriers in the substrate depends on the distance of contact and gate poly line because neighboring contacts may relax the actual strain in channel. To analyze the overlay impact due to contact pattern shifting, we use a rigorous 3D TCAD simulation tools combined with our CER-generated contact layout, and investigate the impact on the systematic and random lithographic variations on manufacturing as well as the timing and power variations on circuit performance.

Using the results of CER, we further analyze the impact of both CER variation and gate LER variation, which causes variability in the effective gate length, by combining the line roughness and the contact roughness into a single GDSII file. We believe a flow that is capable of characterizing CER variability will demonstrate significant advantages in terms of understanding the impact of CER and improving systematic yield and parametric yield as a result of reducing design-to-manufacturing miscorrelations.

7641-12, Session 3

Process sizing aware flow for yield calculation

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Critical dimensions of an integrated circuit continue to shrink to achieve higher logic functionality within a smaller die. Exposure and process techniques such as immersion lithography and double patterning are being introduced into high volume production to pattern these small features. Even with the use of these techniques, patterning features at minimum design rules continues to be one of the leading yield detractors at advanced nodes.

While many techniques are introduced to address the fundamental capability of patterning, opportunistic upsizing of small features remains to be a powerful method to improve patterning process windows and circuit yield. By opportunistic upsizing, we mean to upsize selected features, either during pre-tapeout or post-tapeout stages, so that many small features become larger than design rule minimum sizes without impacting circuit performance. These upsizing steps include increasing routing Poly width, contact/via sizes, metal wires width and spacing, etc. The impact on the electrical performance of the circuit from these upsizing steps is sometimes, not always, accounted for through layout parasitic extraction both at cell level and SoC level. However, for yield calculation based on critical areas in the layout, effects of these upsizing are rarely accounted for. This leads to pessimistic yield prediction in most cases, because of the unawareness of the upsizing step.

In this paper, we present a different flow to more accurately perform layout-based yield calculations by taking into account post-tapeout sizing. Specific examples will be provided to demonstrate the improvement of the flow accuracy. In this abstract, we use metal wire sizing to illustrate the flow. For metal layers, it is common to upsize isolated and semi-isolated wires to improve process windows during the post-tapeout step. To account for the changes of resistance and capacitance, which lead to changes of parasitic extraction and circuit timing, a sizing table (i.e., WEE table) is typically built into the interconnect technology files to convey this manufacturing information back to design. However, most of the layout-based yield calculation tools, either provided by EDA vendors or silicon foundries, do not consider this sizing effect. As a result, there is a discrepancy between the calculated circuit performance (which takes wire sizing into account) and the calculated yield (which does not).

For a 45nm SOI process, we compared the power consumption of 3 cases- original layout, widening wires by 30% and by 50% during the routing step. Because of the unique upsizing and downsizing steps performed by the fab during maskprep, the power consumption actually drops slightly when the wire is widened by 30% in the routing step (left figure). For yield calculation, if the existing flow is used, it is without the knowledge of the WEE table and so shows progressive yield gains by performing 30% and 50% widening (BLUE bars in right figure). When the process sizing aware flow is adopted, it shows 30% widening does not provide yield benefit (RED bars in right figure), which is now consistent with the results from the switching power calculation. Other examples from the Poly and Contact/Via layers will also be discussed in the paper.

7641-13, Session 3

Foundry verification of IP and incoming designs for manufacturing variability

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In this paper, we present the development of a variability methodology, its correlation with silicon, and application to cell and full-chip design verification and optimization. With process technologies advancing to 65nm, 45nm, and below, device timing uncertainty due to lithography

and other process variations has easily exceeded 50% and is still growing. As a semiconductor foundry of advanced technologies, we need an efficient method to accurately extract, analyze, and characterize these timing variations. This method must be model-based and also integrated with the existing design-to-manufacturing flow.

Systematic lithography is a major source of variations at 65nm and below. SMIC has developed a methodology to quantify, analyze, and minimize litho variability and its impact on timing. The first approach was deployed at the cell level (as shown in Figure 1) since it is the foundation of all System-on-Chip designs. Based on silicon measurement data of one of our 65nm cell libraries, this methodology has achieved significant improvement in accuracy of estimating timing variations compared to a traditional rule-based method, as shown in Figure 2.

Next, a full-chip screening has been developed to identify potential variability excursions. Foundries often receive layout database and cannot perform timing and leakage variability analysis due to a lack of sufficient data. However, a selective variability analysis can be done on transistor where litho variability is likely to create a problem (e.g where gate extension or poly-active distance is at the minimum design rules). This full-chip check comes as a complement to DRC and LVS and identifies gates where parametric variability exceeds a pre-defined threshold (See Figure 3 for more details).

In this paper, we will present the motivations of SMIC to develop variability analysis and describe the cell- level and full-chip analysis. We also provide results of this analysis on a representative set of standard cells and provide correlation data to silicon trend. This analysis done at typical (as shown on Figure 4) and across process conditions of dose, defocus and misalignment (as shown on Figure 5) shows clearly that lithography impact cell timing by up to 27% (across process window) and leakage by up to 25%. Context analysis was also performed and has shown significant impact on both timing and leakage. The paper includes results of 100 context analyses of a representative set of cells showing 9.5% timing variations and 17% leakage variations solely due to context (as shown on Figure 6 and Figure 7). Lastly, this paper describes the full-chip variability checks used to screen incoming layout design database.

7641-14, Session 3

45-nm transistor variability study for logic and memory characterization

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Presently available state of the art compact device models are limited when it comes to handling variability. During characterization, model parameters are estimated through fitting to measured or simulated device performance data. For variability purposes, common practice is to produce (in silicon or in simulation) transistor instances that presumably represent extreme slow or fast behavior, and to create model cards to represent those cases. During statistical modeling key model parameters are treated as Gaussian variables and use Monte-Carlo simulation (or its variants, including combinations of macro-models, importance sampling, principle component transformations, etc.) to generate distributions of circuit metrics such as speed or power consumption. However, this methodology is flawed as the chosen “extreme” cases do not represent reasonable IC behavior bounds, and the extracted parameters do not faithfully track the physical device properties they are supposed to represent.

It is well known that SPICE models cannot handle the systematic variability very well in the presence of large process variation. The main reason is that the physical source of the device variation cannot be reproduced by simply fitting presently available compact device models to experimental data. Indeed, the presence of many fitting parameters within modern compact device models tends to artificially bias and correlate the extracted values of the key physical model parameters.

To tackle this issue, we propose a modified parameter extraction flow as shown in Figure 1. In this flow model fitting is done over detailed I-V measurements of arrays of individually addressable transistors and a hierarchical spatial variability model [1, 2, 3] is imposed on the key model parameters. In this way, the extracted values of these parameters are forced to follow smooth deterministic functions (in addition to a small amount of white noise) across the wafer, the lithographic field, and the die.

We use data from one experimental wafer to highlight this method. The test patterns are designed and manufactured using a state of the art 45nm process with variable length ring oscillators and SRAM arrays [4, 5]. Padded out transistors are embedded within fully functional SRAM macros, allowing us to perform individual transistor measurements. A unique feature of this dataset is that within each lithographic reticle there are two copies of the same die. This allows for the investigation of long-range variability within each litho-field, and how that interacts with the across-wafer variability. Preliminary RO frequency measurement and I-V characterization results are shown in Figure 3, Figure 4 and Figure 5. The two copies of die in each litho reticle have shown significant and systematic ring oscillator speed difference, which is comparable to the across-wafer variations. It can be traced back to the Idsat difference measured from NMOS transistors of both copies of die, while extracted VTH shows little contribution.

Final comparison will be made among our metrology and actual logic/memory device measurement data. Spatial variability of ring oscillator frequency, SRAM read/write margin and extracted electrical parameters and their correlations will be studied.

7641-15, Session 3

Variability aware timing models at the standard cell level

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This paper presents a methodology for timing variability characterization at the standard cell level. Timing variations in standard cells are caused by process non-idealities that are not traditionally captured within traditional timing characterization tools. These process non-idealities, including variations from lithography, etch, and stress, affect physical device parameters that in turn affect standard cell and circuit performance. It remains a challenge to abstract these device level variations to the standard cell level as many of these variations are a strong function of layout context.

Our unique approach combines TCAD device simulation with layout level process simulation. Standard cells are placed in different contextual layout environments. Rigorous device and process simulations are performed to characterize each transistor under different layout context and process conditions. This generates a library of different standard cell placements and timing data under varying process conditions. This library is then used to establish compact parameter timing models for predicting timing variations caused by multiple sources of process non-idealities.

We utilize the FreePDK45 process design kit from North Carolina State University to generate compact parameter timing models at the standard cell level using the approach detailed above. Then we synthesize and place a design taken from opencores.org. Using our compact parameter timing models, we estimate the timing impact under different process conditions. In parallel, we perform a rigorous device and process simulation for example critical nets selected from the whole design. This enables us to compare the timings predicted through rigorous simulation and those predicted through our compact parameter timing models and assess the accuracy of our approach.

7641-16, Session 4

Electrical DFM methodology for variation-aware design at 45 nm and below

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Conf.7641: Design for Manufacturability through Design-Process Integration IV

At the 45nm VLSI technology node and below, steps in the IC manufacturing process like CMP, lithography and strain engineering have a predictably large impact on the electrical behavior of designs. For example, due to layout proximity dependence caused by lithography and strain, the timing of standard cells is placement-dependent, which is called cell-context variation. Rather than simply adding guard bands for these manufacturing variations, it is necessary to analyze, identify, and correct for them. To do so, an electrical design-for-manufacturing (eDFM) methodology is required during design analysis and timing closure in both digital and custom design implementation.

This paper will introduce such an eDFM methodology. After conventional timing closure in the place and route system, the eDFM flow consists of running CMP thickness simulation, litho and stress parameters extraction, followed by an analysis of their combined impact on transistor-level, interconnect-level and path-level timing and annotation back as the revised variation-aware path timing. Any timing outliers are analyzed and fixed in the place and route system. Instead of the traditional approach of adding larger guard bands to address intrinsic process variation, the eDFM flow is able to predict systematic layout variations in the performance of the design and correct any limitations associated with it. A Cadence tool flow of LEA, QRC and Encounter is used to demonstrate the whole integrated analysis and fixing methodology.

Using foundry-driven 45nm models for CMP, litho and strain engineering, analysis and optimization of manufacturing, variations and their impact on critical path timing on real designs will be shown. Analyses of several 45nm designs using the eDFM flow show that timing of a high performance design can see a difference up to 100ps when considering these systematic manufacturing variations. The variation can be reduced by the strategic insertion of fillers designed to reduce the proximity dependence around the critical paths of the design.

7641-17, Session 4

Measurement and optimization of electrical process window

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Process window (PW) is the range of process parameters such that designs produced within this range operate under the desired specifications. Conventional geometrical process window (GPW) uses critical dimension tolerance as the specification. This paper proposes electrical process window (EPW), which targets electrical specifications (delay and leakage power) instead of geometrical tolerances. We show that EPW can significantly reduce pessimism in process tolerances while retaining same circuit metrics.

Exposure, defocus and overlay (E/D/O) are taken as key process parameters and experiments are carried out on ISCAS-85 benchmark circuits implemented using a 65nm library. To find GPW and EPW, we generated post OPC layouts of circuits to extract the equivalent gate length and width of every transistor. A process value set {Ei, Dj, Ok} is said to belong to GPW if and only if 99% of the transistor Edge Placement Errors (EPE) fall within K*L, where K is maximum percentage variation and L is transistor gate length. A process value set {Ei, Dj, Ok} is said to belong to EPW if and only if both delay and leakage power fall within defined tolerances. Only layouts with no opens or shorts are considered within the process window.

Area of EPW is typically larger than GPW because averaging in transistor segments and gate lengths of transistors reduces variation in delay and leakage power despite the layout falling outside geometric tolerance. Since worst cases of GPW with 10% geometric tolerance correspond to 10% delay and 850% leakage power deviations, these tolerances are used in our experiments. The results show that area of delay-centric EPW, leakage-power-centric EPW and EPW with both delay and leakage power is 28X, 15X and 10X times the area of GPW, respectively.

In addition to process window evaluation, we use EPW to locate critical cells in designed layout. Once critical cells are identified, they can be fine-tuned by layout transparent gate length biasing to enlarge process window which can be implemented as part of OPC or retargeting. For example, gate lengths of 20 transistors on critical paths (ISCAS-85 c499) are reduced by 2nm, which increases delay-centric EPW (5% deviation) area by 9.7%, decreases leakage-power-centric EPW (200% deviation) area by 0.5% and increases area of EPW considering both delay and leakage power by 46%. The percentage increment in area of EPW considering delay and leakage power is higher than delay-centric EPW because its area is very small initially.

7641-18, Session 4

Development of a design-intent extraction flow for mask manufacturing

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The problem of mask cost has been highlighted recently due to the complex manufacturing process as the semiconductor node is getting smaller and smaller. It has been said that DFM methods can be useful for mask cost reduction. One of the ASET/Mask D2I target is the mask data prioritization and its effective uses for mask manufacturing issues from the viewpoints of mask DFM. The Mask D2I and STARC have been working together to build efficient data flow based on the information transition from the design to the manufacturing level. By converting design level information called as “Design Intent” to the priority information of mask manufacturing data called as “Mask Data Rank (MDR)”, MDP or manufacturing process based on the importance of reticle patterns is possible. Our main purpose is to build a novel data flow with the priority information of mask patterns extracted from the design intent.

In this paper, we introduce a design intent extraction flow which has been newly developed and we show the effectiveness of the fully automated MDR flow with actual chip data. In addition, we show how MDR flow can be applied to analog circuits.

Firstly, the background of ASET MaskD2I project is introduced. It will be shown how each team in MaskD2I is related to each other and what our common goals are. Then we introduce the idea of Mask Data Rank (MDR). We have defined the MDR format to describe mask data rank information so that the design intent can be converted to the information useful for manufacturing stages. The MDR format is based on the OASIS format and the priority is expressed as polygon records with several values of layer ID of data type which mean criticality of the area. The layer number is used for describing the data rank type and the datatype number is used for the area priority based on pattern importance.

We have developed the automated design intent extraction flow with help from STARC. We will show the experimental results that mask inspection time can be reduced by 26 to 40 % by utilizing design intent of LSI. The new design intent extraction flow consists of existing standard EDA tools and it does not require any special preparation.

Finally the future prospects for further improvement of MDR flow are discussed and several ideas will be addressed.

7641-19, Session 4

Design intention application to tolerance-based manufacturing system

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1. INTRODUCTION

Continuous shrinkage of design rule (DR) in ultra-large-scale integrated circuit (ULSI) devices brings about greater difficulty in the manufacturing process. The keys to meeting small process margin are adequate extraction of critical dimension (CD) tolerance for each object and budgeting the tolerance for each process step.

Furthermore, to extract adequate tolerance, design intent in terms of

electrical behavior should be carefully considered. Electrical behavior is carefully verified in both cell and chip design stages with respect to timing, IR drop, signal integrity, crosstalk, etc., using various electronic design automation (EDA) tools. However, once the design data is converted to layout data and signed off, most of the design intention is abandoned and unrecognized in the process stage. Thus, instead of essential tolerance according to layout-related design intention, uniform and redundant tolerance is used, and so excess tolerance is assigned for some layouts.

To solve the problem described above, a tolerance-based manufacturing system utilizing flexible layout-dependent speculation derived from design intention has been discussed 1-3). In this paper, a test flow is developed and application to 45nm node test chip is examined.

2. TEST FLOW OF TOLERANCE-BASED MANUFACTURING SYSTEM

A test flow of a tolerance-based manufacturing system utilizing design intention is examined. In cell design and chip design stages, electrical verification is performed such as clock tree synthesis, timing fix, and lithography compliance checking (LCC). In each stage, process sensitivity in terms of electrical behavior is examined, and CD tolerance is assigned to each object, including net, instance, path and other figures. At the time of layout data sign-off, designed data is converted to layout data and information on tolerances corresponding to each object is assigned to specific net, instance, path and other figures in the layout. These tolerances assigned for each figures are budgeted among process steps of mask data processing (MDP), optical proximity correction (OPC), lithography simulation, mask making and wafer process, considering proficiency of each process. In each process step, assigned tolerance budget is kept and the remaining tolerance is utilized in the following process. In this flow, tolerance derived from design intention is utilized in manufacturing.

3. RESULT AND DISCUSSION

In the test flow, utilizing essential tolerance flexibly assigned to each object, yield enhancement is expected. In our previous work2), we have shown that, with proper tolerance management, both alpha-risk and beta-risk of manufacturing are reduced. Another example showed that with flexible tolerance settings, OPC turnaround time was reduced according to the rate of non-critical path area. In this paper, a practical method for accurate tolerance extraction and tolerance assignment to design objects is examined and applied to test design as a trial.

The detailed result will be shown in the presentation.

7641-20, Session 4

OPC-aware layout modifications for improved standard cell metrics and enhanced ASIC design QoR

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Novel implementation techniques of OPC-aware, DRC-clean transistor layout modifications are proposed, and their effect on improving standard cell metrics has been quantitatively evaluated. First, three-dimensional TCAD simulations that are calibrated to industry 45nm technologies are performed to quantify the non-uniform distribution of drive and leakage current along the transistor width. It enables realistic assessment for state-of-the-art technologies of the drive current/leakage trade-off in a non-rectangular transistor where the edges of its width are increased. A novel OPC calibration technique is then proposed that can efficiently implement DRC-compliant layout modifications to the gate based on design intent without having to modify the OPC recipes. Second, opportunities to moderately increase the transistor width in standard cells have been identified to enhance the cells' drive strength. Its overall effect on cells' delay has been evaluated across standard cell library's arrays of input transition and load capacitance. Combining such an analysis with cell usage and cell context statistics from various designs, it has been shown that approximately 50% of the transistor's width percentage increase goes into cell delay improvement. Consequently, standard cell variants with both enhanced performance and reduced leakage result through OPC-aware, DRC-compliant layout modifications. Applications of these techniques include IC leakage power reduction, FMAX enhancement, and/or more efficient design timing closure.

7641-21, Session 4

Experimental results for parameter-specific ring oscillators for quantifying sources of variability at 45 nm

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Experimental results are reported for 45nm parameter-specific Ring Oscillator (RO) inverter layouts that identify and quantitatively model sources of circuit performance variation from source/drain stress, shallow trench isolation (STI) stress, gate stress, lithography, etch, and misalignment. Measurement of ring oscillator frequency response with automatic scan-chain selection has been shown to be an efficient method to screen for possible causes and levels of layout dependent variability in 90 nm and 45 nm generation circuits [1][2]. Wang et. al [3] demonstrated through dry-lab simulation the extension of this RO approach through tuning the design of layouts monitors for enhanced sensitivity and selectivity to specific physical parameters for a 45 nm technology. In this presentation, experimental RO frequency response will be reported for these designs as fabricated by ST Micro.

Thirty-two flavors of parameter-specific inverter layouts are included: 8 structures are designed to monitor variability in RO frequency response due to source/drain stress, 4 structures for STI stress, 4 structures for poly focus, 4 structures for etch, and 12 structures for poly to source/drain diffusion misalignment and source/drain diffusion focus. These test structures have evolved from lithography and etch effects at the 90 nm generation to stress effects at the 45 nm generation following the screening results from [1][2]. The lithography monitors have been guided by the ability to visualize a combination of off-axis illumination and wafer focus effects through Pattern Matching [4][5]. Over 20, 000 across-die RO frequency responses will be measured for one wafer. Twenty randomly selected chips across one wafer have been packaged, and three test blocks are available for measurement on each die.

The ring oscillator frequency normalized to that of a standard minimum sized inverter will be reported for each of the 32 test structures. Average ring oscillator frequencies will be used and will be obtained by taking the mean of 36 frequency measurements in a 1mm x 2mm die across 20 chips. The RO frequency data from initial testing were sensitive to the design intent of their specific physical effect. Layout dependent stress CESL effects of 5% were seen and saturated quickly at about 3 feature sizes.

A test-pattern for misalignment of the poly to the source/drain diffusion is shown below. Figure 1 is the layout of the test structure, and Figure 2 contains simulated SPICE RO frequency response for -15nm,-7nm, 0nm, +7nm, and +15nm offsets at in focus and out of focus. Figure 3 contains measured RO frequency data averaged over 12 data points for one chip at -15nm,-10nm, 0nm, +10nm, and +15nm offsets. The standard deviation-to-mean ratio is 0.79%. The minimum of the ring oscillation frequency curve corresponds to best alignment. Initial data shows that the desired parabolic frequency has an off-set from best alignment by 5 nm. The strength of the initial response is about 1/3 of that seen from simple image simulation without OPC. A careful comparison will be made including illumination details, OPC layout modifications, and capacitive loading effects.

7641-22, Session 5

A kernel-based DFM model for process from layout to wafer

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Even a design passes the design rule check (DRC) it still may have manufacturing problems, especially in the critical patterns of layout.

Thus a design-for-manufacturability (DfM) model, which can simulate the process from layout to wafer and predict the contour, is necessary. A new kind of DfM model called free-element-model (FEM) is proposed in this paper. The framework of FEM is determined by the forward process model, which is basically a set of convolution kernels in matrix form and the unknown variables are the elements of kernels instead of process parameters. The modeling process is transformed into a non-linear optimization problem with equality constraints. The equality constraints involve 2-norm regulation of kernels and inner production of any two kernels to guarantee the normalization and orthogonality of optimized kernels. Steepest-descent method with Lagrange penalty function is explored to solve the optimization problem to make the distance between simulated contour and given contour as small as possible. The dimension of kernels in FEM is determined by the cutoff frequency and the ambit, which should be larger than or equal to that of frequency kernel to keep accuracy. Since kernels are determined by optimization method not by decomposition of transmission cross coefficient (TCC), every element of kernels is a dimension to describe the process. FEM has more freedoms, and all effects that can be integrated into convolution kernels are integrated naturally, like resist deviation and asymmetry of the process. No confidential process parameters, like NA, defocus, etc., are needed in FEM modeling process, and thus the well-encapsulated FEM is suitable for foundries to publish. The enhancements and supplements of FEM are also discussed in this paper, like the usage of variable threshold resist model (VTRM) and variable bias model (VBM), the implementation of band prediction and the sufficiency of test patterns. Experiments take 4.7 hours to generate 51*51 kernels based on 300*300 test patterns and results show that simulated contours have an error ratio less than 3% compared to the given contour, and the probability that contour falls within the contour band can be higher than 95% with the help of 2-sigma criterion to determine the threshold interval.

7641-23, Session 5

Stat-LRC: statistical rules check for variational lithography

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As interconnect densities increase with each technology generation, the lithographic processes required to print all features with acceptable irregularities have become more complex. Restricted design rules (RDR) and model-based Design for Manufacturability (DFM) guidelines have been added to the existing Design Rule Check (DRC) software to prevent unprintable patterns to be drawn on the mask by predicting their imprint on the wafer. It is evident from analyses of various lithographic defects that the error sources can be systematic or random in nature and hence a pass/fail estimate of design feature yield is not sufficient. In this paper, we describe a methodology to perform Rules Check involving design yield estimation based on interconnect linewidth distribution for variation in lithographic input error sources. In the scheme we have developed, a list of error locations indicating polygons that have yield below the set user threshold for a metal layer is provided to the user. Further guidance is provided for yield recovery.

The central objective of this paper is to perform statistical design rules check. Variation in lithographic input results in changes in edge placement. This may lead to excessive narrowing in line width or separation contributing to potential errors. In traditional DRC, a design layout is either accepted or rejected based on error potential. In the proposed approach, such decision is not binary and a statistical metric that corresponds to yield is defined.

In the proposed approach, for each line segment, a cumulative probability function is computed for a range of acceptable line widths/shapes. Lithographic simulation is performed within the optical diameter for varying dose/focus/resist thickness/out of band radiation and other parameters. The key technical challenge is to reduce the computation through creation of library of shapes. We use Monte-Carlo based aerial imaging simulation to compute PDF for width of each line segment in the layout. To reduce the number of samples to be simulated (expensive) to obtain tail of the distribution, we perform stratified sampling.

Next, we define what constitutes acceptable yield (may also be user input) using EPE metrics and compute the CDF of the edge/corner EPE within acceptable limits. This represents the probability of yield of this shape. If this probability fails to meet certain threshold, it will be flagged for error. If a user decides to override this violation by manual means or automated thresholds, a marginal shape is accepted in the design process. This leads to some yield loss. The total yield loss/gap is computed before the VLRC objective changes to yield recovery.

In yield recovery, the goal is improving CDF of the edge/corner EPE in other parts of the design such that the design meets the overall yield goal. The process will be continued until all violations disappear. This allows trade-off poorer EPE distribution of one line with excellent distribution of other lines. In our simulation/analysis environment this process is fully automated. In the final paper, results will be included.

7641-24, Session 5

Layout analysis and ranking of standard cells by dedicated ‘continuous’ DRC rules

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In order to have a quantitatively comparison between layouts designed for the same purpose (standard cells for example), a ranking system is needed. The first generation of our ranking system (see SPIE 7275-29), was based on set of “classical” DRC rules, having discrete values in bins. Based on the score per bin for every rule, and per rule type, the overall design quality factor (DQF) was calculated. The main disadvantages of this system were: (i) limitations due to rule value binning, introducing some level of errors for values in between bins, (ii) limited complexity of the rule.

In this work, we have updated our “ranking” system, which analyzes the design and prioritizes the places to be modified. We used advanced modeling programmability, which provides values per any size. Instead of “bin score”, we used “score equations” that provide value for any size, giving the possibility to analyze complex structures. We also used custom scripts to process the outputs and to present the user both statistics on the design, final score and summary of changes to be made for higher DFM score. The rules or scoring were changed, to include several boundary conditions. For example, instead of using “space” we are now using space per parallel length that is more accurate to represent critical area sensitivity. We used our ranking analysis system and compared several standard cells libraries, designed by leading 3rd party IP houses. Based on the ranking results, guidelines and priority for layout modification are defined. We also discuss the impact of different DRC coding styles and coding methods on the ranking values. Finally, we show our analysis for several full-chip designs.

7641-25, Session 5

Applying DRCPlus in a router: automatic elimination of lithography hotspots using 2D pattern detection and correction

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As technology processes continue to shrink, standard design rule checking (DRC) has become insufficient to guarantee design manufacturability. DRCPlus is a powerful technique for capturing yield detractors related to complex 2D situations. DRCPlus is a pattern-based 2D design rule check beyond traditional width and space DRC that can identify problematic 2D configurations which are difficult to manufacture. This paper describes a new approach for applying DRCPlus in a router, enabling an automated approach to detecting and fixing known lithography hotspots using an integrated fast 2D pattern matching engine. A simple pass/no-pass criterion associated with each pattern offers designers guidance on how to fix these problematic patterns. Since it does not rely on compute intensive simulations,

DRCPlus can be applied on fairly large design blocks and enforced in conjunction with standard DRC in the early stages of the design flow. By embedding this capability into the router, 2D yield detractors can be identified and fixed by designers in a push-button manner without losing design connectivity. More robust designs can be achieved and the impact on parasitics can be easily assessed.

This paper will describe a flow using a fast 2D pattern matching engine integrated into the router in order to enforce DRCPlus rules. An integrated approach allows for rapid identification of hotspot patterns and, more importantly, allows for rapid fixing and verification of these hotspots by a tool that understands design intent and constraints.

The basis of this flow is the existence of a library of patterns that the router will check for in a given technology node. This paper will further illustrate a methodology for determining and using this library of patterns. A deck of pattern-based rules can be easily defined, used, and modified as needed.

Experimental results from this flow run on a routed block will be demonstrated. Equally important is determining the metrics of DFM quality for a given block. A discussion on what DFM attributes to measure and how to measure them will also be presented.

7641-26, Session 6

Demonstrating the benefits of template-based design-technology co-optimization

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The escalating design rule complexity resulting from increasing layout sensitivities in physical and electrical yield and the resulting risk to cost-effective technology scaling is a fundamental concern to the health of the semiconductor industry. In our 2009 paper we introduced the concept of template-based design-technology co-optimization as an end-to-end solution aimed at improving design efficiency while increasing manufacturability in challenging technology nodes. In that work, the key requirements for an optimal design to silicon solution were established as:

- late binding of logic to physical layout to preserve design-creativity
- optimally simplified layout to allow construct-driven process development
- targeted characterization and qualification test vehicles to drive yield ramp

We demonstrated that competitive logic designs can be generated from a highly constrained set of logic constructs and claimed that experiments have been designed to demonstrate:

- variability and design-margin reduction afforded by the predictable and regularized layout environment
- yield and manufacturability improvement facilitated by the simplified design environment
- predictable template composability achieved through layout regularity and control of boundary conditions
- performance and power benefits from the use of complex logic gates
- placement agnostic delay achieved through macroscopic layout regularity
- model-to-hardware correlation improvements through pre-characterized templates

This paper will report the results of these 32nm experiments completing the value assessment of template-based design-technology co-optimization.

7641-27, Session 6

The role of strong phase-shift masks in Intel’s DFM infrastructure development

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Intel has reported on three separate styles and applications of strong phase shift masks (PSMs) over the last decade including alt-PSM for gate patterning1, alt-PSM with assist features for contact patterning2 and Pixelated Phase Masks (PPMs)3 for metal layer patterning.
Each had a prominent role in Intel’s Design For Manufacturing (DFM) infrastructure development both in terms of design rules and DFM tooling.

Alt-PSM for gate patterning introduced and highlighted the advantages of restricting layout diversity to improve patterning performance. Limiting multi-directional gate usage resulted in improved patterning performance and CD control when coupled with alt-PSM. Alt-PSM also necessitated the creation to tools for phase assignment (coloring) that were capable of making decisions on optimal phase placement and coloring schemes. These tools ended up being the predecessors of some of the pattern splitting tools reported to be used for pitch division in the 22nm and 15nm nodes. Design rule checking for phase circulation conflicts and basic terminology were also created as part of the infrastructure development for alt-PSM. Alt-PSM were successfully implemented in high volume manufacturing upon completion of Alt-PSM consistent design rule modifications and automated tooling infrastructure creation.

Alt-PSM for contact patterning uncovered new DFM challenges in that it relied on the use of phase shifted assist features. Unlike alt-PSM for gate patterning where the phase locations were naturally placed next to the gate regions, phase shifted assist features could be placed with a high amount of flexibility and still produce the desired patterning. This resulted in the need for a more sophisticated phase shift placement and coloring approach. Furthermore, contact layout was much more prone to phase conflicts as contract are much more likely to form odd loop cycles. Design rule approaches to manage phase conflicts will be described that enable high volume manufacturing applications.

Pixelated Phase Masks (PPMs) for metal layer patterning was unlike many other resolution enhancement techniques in that was introduced to maintain the ability to pattern a diverse range of layouts as opposed to targeting improvement in patterning of a few key tight pitch or small sized features. PPMs are driven by an Inverse Lithography Technique (ILT) engine. ILTs have been shown in the industry as key methods for model based SRAF generation and design rule analysis tools. In developing and applying PPMs to full chip microprocessor designs, the requirement of including a rigorous treatment of thick mask effects with ILT was found to be essential.

Use of multiplicity of different types of strong PSM and its efficient co-optimization with design rules made possible by Intel’s Integrated Device Manufacturer (IDM) environment allowed for robust critical layer patterning throughout multiple generations of Intel Process Technology.

1 Schenker, Richard et al., “Alt-PSM for 0.10-um and 0.13-um poly patterning” SPIE Vol. 4000, 2000.

2 Schenker, Richard et al., “Alternating phase-shift masks for contact patterning” SPIE Vol. 5040, 2003.

3 Borodovsky, Yan et al., “Pixelated phase mask as novel lithography RET” SPIE Vol. 6924, 2008.

7641-28, Session 6

Decomposition strategies for self-aligned double patterning

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Spacer technology, a self-aligned double patterning (SADP) technique, has been drawing more and more attention due to its less stringent

overlay requirements compared to other double-patterning methods. However, use of SADP techniques was previously limited by the lack of flexibility in terms of decomposition options; until now, significant developments were mainly implemented for 1D-type applications for memory. In this paper, we extend the SADP technique into the logic field. We will present some SADP decomposition strategies suitable for 2D applications, and useful design rule extraction as a result of each decomposition strategy.

As we know, reticle cost dominates the cost of today's products for logic. The primary challenge facing the successful application of SADP in the logic field comes from whether we can decompose 2D layouts using two masks instead of three. Random 2D logic features may contain multiple critical dimensions, and how to realize them with a two-mask solution is the first problem we need to tackle.

There are two types of process flow associated with SADP:1 one is the so-called positive process in which the spacer defines lines, and the core and the space between spacers define trenches; the second is the so-called negative process in which the spacer defines trenches, the core and the space between spacers define lines.

In the paper, we will present our decomposition strategies for 2D features by using the additional decomposition dimension provided by the tones of masks, and evaluate their efficiencies, then discuss the possible design rules associated with each decomposition method.

7641-29, Session 6

Toward nanoimprint lithography aware layout design checking

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Just as the simulation of photolithography has enabled optical proximity correction to enter use, the physical simulation of nanoimprint lithography is needed to guide the design of products that will be manufactured using this process. Nanoimprint-aware design checks should assess whether a pattern can be fully imprinted in an acceptable time, and whether any residual layer of imprinted resist will be sufficiently thin and uniform. To these ends, we present an extremely fast method for simulating the deformations of a spun-on polymeric layer when imprinted with an arbitrarily patterned stamp.

We encapsulate the resist's mechanical behavior using an analytical function for its surface deformation when loaded at a single location. The stamp and substrate, meanwhile, are well modeled as linear-elastic. Our approach takes a discretized stamp design and finds resist and stamp deflections in a series of steps. The compliance of the resist is gradually increased with each step, and the algorithm iteratively finds the distribution of stamp-resist contact pressure that is consistent with the instantaneous compliances of the stamp and resist. Incremental changes in resist layer thicknesses are computed at each step by convolving the found pressure distribution with an appropriately scaled version of the resist's point-load response. At the final step, the modeled compliance of the resist equals that at the end of the imprinting cycle, and the distribution of the resist's residual layer thickness is reported.

We further accelerate the simulation of feature-rich patterns as follows. We pre-compute relationships between the applied imprinting pressure-time profile and the completeness of pattern replication, for stamps patterned with uniform arrays of a variety of common feature shapes. These relationships are encoded in a dimensionless form. We can then subdivide a given imprinting stamp into a grid of coarse regions, each one characterized as being patterned uniformly with features of a particular shape, size, and packing density. A spatially coarse solution for residual layer thickness is then found.

The technique is implemented in Matlab and we have faithfully simulated, in less than 50 s, the imprinting of an experimental test-pattern reported by Kehagias et al. Our simulation technique is fast enough to be used iteratively in the engineering process, both when selecting processing parameters and refining layouts.

Our technique can also be used to derive nanoimprint-aware design rules. Rules might include, firstly, an upper limit on the diameter of stamp protrusions, to restrict the time-integral of applied pressure needed for complete imprinting. Secondly, to minimize residual layer nonuniformity, there might be a requirement for the distribution of stamp cavity volumes to be spatially uniform across the stamp: our simulation technique could help decide over what length scale uniformity should be imposed. Thirdly, we show that elastic stamp deflections during imprinting can be minimized by requiring spatial uniformity of the product of the local areal density of stamp protrusions, the square of the local average feature-diameter, and a dimensionless feature-shape-dependent parameter.

7641-30, Session 6

Using a highly accurate self-stop Cu-CMP model in the design flow

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Effective design-for-manufacturing (DFM) requires the bridging of the manufacturing and design worlds. We will report on a flow that accomplishes this for the chemical mechanical polishing (CMP) process. The flow consists of building an accurate CMP model and then using it to reduce both manufacturing and electrical variabilities resulting in robust designs.

The need for detection of planarity hotspots is expanding as copper CMP (Cu-CMP) has become a key process that affects yield loss and circuit performance [1][2]. The Cu-CMP process has been aggressively improved with the development of a self-stop version to achieve a highly planarized surface. Such process advancements and the fact that a created model represents the first step in an extensive DFM flow have led to new requirements for improving the accuracy of Cu-CMP modeling.

An accurate model for the self-stop Cu-CMP process has been developed. It comprises of optimized copper electroplating (ECD) and CMP process models that have been calibrated to data measured at these key process steps in a typical copper metallization process. Multiple materials, including copper were polished at various stages. Figure 1 illustrates a die-level CMP simulation flow that was used to simulate the surface height [3]. It detects planarity hotspots that help identify potential problems in production chips before they are manufactured. It also outputs thickness values of metal and dielectric used to drive layout enhancement tools and improve the accuracy of timing analysis. The CMP simulation environment is driven by a process recipe that closely resembles the real-world manufacturing process.

The ECD and CMP models take into account layout pattern dependency, long range diffusion and planarization effects, as well as microloading from local pattern density. Variation in the surface height after each step is therefore accurately captured. Superfilling phenomenon related to ECD results in bump formation for wires close to minimum width. The developed ECD model not only captured this important effect but also accurately predicted erosion and dishing over the entire range of width and space combinations present on the test chip (figures 2, 3). Then, the results of the ECD model were used as an initial structure to model the Cu-CMP step. After thorough consideration of process characteristics and potential causes of modeling error, we concluded that our Cu-CMP model reasonably reproduces the measured data. Some mismatches between the predicted and measured data are attributed to measurement errors (figure 4). The robustness of the created model is demonstrated by the fact that it gives acceptable prediction of final copper thickness data although the calibration data included noise from line scan measurements. This is the most appropriate feature for the modeling of high precision CMP such as self-stop Cu-CMP.

An accurate model is essential for making valid decisions in the design flow such as extracting and fixing manufacturing hot spots (figure 5).

The connection between the CMP model and the specific design helps to reduce the guard-banding that were required in previous design flows. This paper will demonstrate how a CMP model is created by the manufacturing team and used in a design flow.

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7641-31, Session 6

Improving copper CMP topography by dummy metal fill co-optimizing electroplating and CMP planarization

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We present a new dummy fill method in this paper. As process technologies move to 65nm, 45nm, and smaller feature sizes, qualities of CMP (Chemical Mechanical Polishing) planarization become crucial to optimizing not only three-dimensional RC effects over multiple layers, but also depth of focus (DOF) for photolithography. DOF tolerance has been demanded to be significantly below 100nm for both 65nm and 45nm technologies. This level of small DOF can be easily violated in today's SoC designs, which contain conducting patterns having wide varieties of sizes and densities on each layer. Therefore, methods have been proposed and practiced to improve CMP planarization, many of which use dummy-metal-fill approaches that are verifiable with accurate CMP process simulations.

As a foundry using dummy metal fills, we have found it a very effective method to achieve DOF-friendly copper CMP topography by optimizing both post-ECP (Electroplating) and post-CMP height variations. Modeling technologies of copper CMP processes show that both pattern perimeter and density dominate topographies of the post-ECP stage, while density determines post-CMP topographies. Shapes of dummy metals resembling the original layout also improve CMP. A dummy fill method incorporating matching of these parameters co-optimizes both ECP and CMP and provides an easy problem for CMP to work on, as the models predict. Therefore, adoption of this method fundamentally resolves the DOF-tolerance issue and flattens copper topographies on multiple interconnect layers.

In this paper, we present the dummy fill method based on these models and show silicon proof. We present the layout dependent, minimum variance algorithm that matches not only metal densities across two-dimensional tiles of layout, but also the perimeters and shapes of metal lines in each tile. Using co-optimization as the fill criterion, our algorithm effectively minimizes the metal height differences as verified by model based CMP simulations. In addition, it also renders pre-characterization of fill constraints with respect to timing and signal integrity assurance. Our silicon data measured on a 65nm process provides proof of the method. We have designed and fabricated a testchip containing copper interconnect patterns with different sizes and densities sufficiently representing the varieties in today's SOC designs. Measuring post-ECP and post-CMP topographies, we identified variation of chip-level copper heights caused by different perimeters of patterns. Consequently, we measured much more uniform (400% improved) post-CMP topography results after co-optimizing ECP and CMP, as compared to results from the same test patterns without any fill. The height difference with our method is smaller than 20nm across the testchip. The results are also compared to those by another rule-based, fixed-size-and-density dummy fill method performed on the same test patterns and we found nearly 300% improvement of uniformity as well. The dishing effect measurements also show 24+% better results. The method results in effectively improved and DOF-friendly topographies for 65nm and below. It can also be integrated into production-level manufacturing data engineering flows.

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